An Online Testing Technique for the Detection of Control Nodes Displacement Faults (CNDF) in Reversible Circuits

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Abstract. With the advancements of Quantum Computing and its implementing technologies like NMR, IoN trap, the necessity of constructing fault-free quantum circuit is observed. But in way to ensure fault-free circuit, appropriate testing model to be invoked and here in this paper we present an online testing technique that effectively detects control node displacement fault (CNDF) in quantum circuit designed with reversible gates.

Our testing approach involves two steps. In the very first step, the input circuit is transformed to its corresponding testable design by appending additional gates and lines (auxiliary lines). Next, appropriate test vectors are generated and subsequently are applied to find possible node displacement faults in the circuit. The proposed online testing approach is suitable for all type of quantum circuits built with reversible gates (MCT gates). More interestingly, some small changes in the design turn this scheme very effective for ESOP based representation as well. We have extensively tested our approach over a large spectrum of benchmarks and comparison with existing testing algorithms is also summarized in the result tables.

Keywords: Multi control toffoli (MCT) · Reversible circuit · ESOP circuit · Control node displacement fault · Online testing · Auxiliary lines

1 Introduction

With the advancements of the fabrication technologies, the necessity of the developing high end circuit and the computing devices is observed. Quantum computing [1, 2] has evolved as one of such solutions that have the capacity to meet the asked challenges. Nowadays, it (quantum technology [3, 4]) is considered as one of the most promising research domains due not only its computing capacity but also for its wide range of applications in different fields like nanotechnology, cryptography, machine learning and bioinformatics. This highly emerging filed is not restricted to theoretical concepts only, enormous progress [5–7] has been made towards developing quantum circuit implementing technologies like NMR, IoN Trap and Super Conducting qubit. Successful implementation of the 2-qubit quantum gate in silicon [8], the conceptualization of lower qubit quantum computers [9] had again advanced this highly emerging computing field to a new dimension. Reversible circuit is one of the most promising means which can design quantum circuit as all the quantum operations are inherently reversible. In recent time, this filed has progressed significantly, where different well-established algorithms are proposed for the efficient synthesis and design of reversible logic, such as ESOP [10], BDD [11] and Reed-Muller [12]. In addition to circuit synthesis, identification of faults [13] in reversible circuits has also become a significant issue to fabricate the fault-free circuit. For example, some well-known fault models are Single Missing Gate Fault (SMGF), Partial Missing Gate Fault (PMGF), Multiple Missing Gate Fault (MMGF), and Repeated Gate Fault (RGF).

Several researches are ongoing in the domain of reversible circuit testing for the design of efficient fault detection and diagnosis algorithms. Here, we are presenting some well-known algorithms to perform the test operation in reversible circuits.

The test vector generation mechanism for the reversible circuit to detect the fault and also to localize the fault for different fault models is presented in [14]. Here, the deterministic approach and probabilistic approach of fault detection are described and compared. Special measurement of the internal states of gates is used to establish the probabilistic mechanism of fault detection. An efficient and complete test vector generation mechanism for the reversible circuit is reported in [15]. Apart from that, finding out minimal test set by integer linear programming for smaller circuits has been described in the work. The derivation of the optimal test set (OTS) and its effective use in the detection of missing gate faults in k-CNOT gate based reversible circuits is introduced in [16], where the authors have find out that the OTS is sufficient to detect all SMGFs and all detectable repeated gate faults (RGFs) in the circuit. Another approach of SMGF and RGF detection has been proposed in [17]. In this work, test vectors are generated with minimum test time to find out any kind of SMGF and RGF in the circuit. Here, 100% fault coverage has also been achieved. Apart from test vector generation and fault detection in reversible circuits, another aspect of testing is fault localization. The mechanism of fault localization for the reversible circuit is proposed in [18]. Here in this approach, the reversible circuit is divided into two parts. The first part of the circuit is represented as a symmetric adaptive tree and another part of the circuit is represented as a mirror image of the first part. Hence, it is quite easy to locate the exact fault in the circuit so that the fault can be corrected as early as possible. A new test vector generation technique is introduced in [19] where the concept of Boolean generator is used. An approach of fault

diagnosis is also presented in [20]. Till so far we have talked on different developments over offline testing techniques, now here we are discussing on progressed made over online testing. An online testing technique for all $(n \times n)$ and d depth reversible circuits using $2d$ garbage outputs along with $(2d + 1)$ auxiliary lines has been proposed in [21]. The formation of testable design for effectively finding faults is discussed in [22], where some redundant gates are added in the input side of the testable design to make the design simpler. Another approach of online testing using testable design approach has been presented in [23], where the existing gates are modified to design two new gates which efficiently detects faults in online circuits. As the testable design is formed with additional lines and gates, it creates design overhead in the testing process. Hence to minimize the design overhead in the testable design, an online testing scheme has been proposed in [24], where no auxiliary lines are used to detect the possible SMGFs in reversible circuits in online mode. So far, we mainly have talked about different offline and online testing algorithms for SMGF, PMGF, MMGF, and RGF. Apart from that, a reversible circuit may incur the control node displacement fault (CNDF) in a gate of the circuit. To deal with such a type of fault, here in this proposed approach, we have proposed an online fault detection mechanism of CNDF in reversible circuits.

The rest of the paper is presented as follows. Introduction to reversible circuit and the different fault variations are stated in Sect. 2. The proposed fault detection model with example is explained in Sect. 3. The different benchmarking and experimental evaluations are reported in Sect. 4 and finally, the paper is concluded in Sect. 5.

2 Preliminaries

Some basic concepts regarding reversible circuits and different fault models related to the reversible circuits are introduced in this section.

Definition 1: *A circuit that exhibits objective mapping between inputs to outputs and has equal number of input-output lines is known as reversible circuit.*

The circuit must also need to satisfy the fan-out free condition and all the gates in the circuit must be reversible only.

Some Familiar gates in the reversible domain are Feymen [25], Toffoli [26], Fredkin [27].

Definition 2 [2]: *ESOP (Exclusive Sum-Of-Products) based circuit can be expressed in Boolean function represented by the operator '$\oplus$'. Here, we will discuss some of the fault models for the reversible circuits.*

Definition 3**: *When a gate completely disappears or goes missing from a circuit then the infused fault is termed as Single Missing-Gate Fault (SMGF).*

Definition 4: *Unwanted occurrence of a gate by multiple times is known as repeated gate fault (RGF).*

Definition 5: *When a circuit has multiple and consecutive SMGFs in a circuit then the intensity of the fault in the circuit goes high which is known as multiple missing-gate faults (MMGF).*

Definition 6: *A fault is categorized as Partial missing gate fault (PMGF), when control nodes from gates go missing by causing change in functional behavior of the circuit then the infused fault is termed as Partial missing gate fault (PMGF).*

Definition 7 [28]: *Unlike PMGF, when control nodes of a gate get misplaced over different circuit lines but size of the gate remain same then the incurred fault in the circuit is termed as control node displacement fault (CNDF).*

For an example, If the control node at the line x in any gate G_i of the circuit is displaced to the through line y then the *CNDF* is denoted as $D_{G_i}^{x \rightarrow y}$, where $0 \leq i \leq (N\text{-}1)$ and N represent total gates in the circuit. Whereas the test vectors needed to detect any $D_{G_i}^{x \rightarrow y}$ are represented as $T(D_{G_i}^{x \rightarrow y})$ [28]. Here it is assumed that the target node is always fixed to its original position.

3   Proposed Technique

Here, we introduce two different variations in CNDF testing technique – 1) generalised CNDF testing scheme in any arbitrary reversible circuit, and 2) ESOP design specific CNDF detection procedure. Both the testing processes are divided into the following four phases: formation of circuit under test, establishment of fault detection mechanism, test vector generation, detection of the fault. We explain all the phases of this CNDF detection using a model circuit.

3.1   CNDF Testing Scheme for Any Reversible Circuit
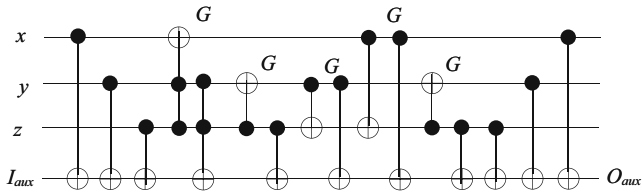
3.1.1   Formation of Circuit Under Test

To transform a Toffoli circuit to the form of circuit under test, at first an extra circuit line is added in the input design and then a series of copy gates are added (for all the existing gates in the circuit). Hence after, a list of CNOT gate is placed in the beginning and at the end of the circuit where the number of newly added CNOT gate is twice the number of circuit lines in the Toffoli network. The steps involving this transformation are outlined in Algorithm 1.

Let us take the circuit (C_{input}) of Fig. 1(a) and transform it to circuit under test ($C_{under-test}$) using Algorithm 1. From the circuit configuration, we see that the design has 5 CNOT/Toffoli gates placed over 3 circuit lines. Now in the initial step, an auxiliary line (having input as I_{aux} and output as O_{aux}) is appended after the input line z and place five copy gates for all the five gates in the circuit. As the initial circuit had three circuit lines, accordingly we add CNOT gates at beginning and end of the design. Finally, we obtain the testable design ($C_{under-test}$) as depicted in Fig. 1(b) and this transformed design also preserve the same logic functionality as the initial circuit had.
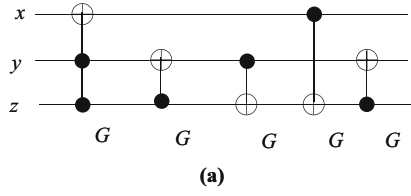
(a)

(b)

Fig. 1. (a) Input Circuit (C_{input})*"ham3\design#1" and* (b) Circuit Under Test ($C_{under-test}$) for (a).

ALGORITHM 1: Online Detection of CNDF in
Reversible (*Toffoli* gate based) Circuit

Input: Reversible (*Toffoli* gate based) Circuit C_{input}
Output: Detection of any CNDF in the $C_{under-test}$
begin

    Step1: Formation of Circuit Under Test:
        Transform the input circuit $C_{test}$to the testable form
    ($C_{under-test}$) using the ***circuit-under test()*** function.

    Step2: Test Vector Formation:
    For any control node displacement fault in gate
    $G_i (D_{G_i}^{x \to y})$, the test vector $T(D_{G_i}^{x \to y})$ is detected by fixing
    0 at the original position of the control node and 1 at
    the current position of the control node of the circuit
    under test. Also 1 is set to others control node and 0/1
    to the target line and through line of the circuit under
    test respectively.

    Step3: Fault Detection Phase:
    For any control node displacement fault in any gate
    $G_i(D_{G_i}^{x \to y})$, the test vector $T(D_{G_i}^{x \to y})$ is applied to the test
    able circuit and if $O_{aux} = I_{aux}$then it can be confirmed
    that CNDF is present in the testable circuit.
                //**Detection of CNDF**//

    Step4: *circuit-under test()*
        begin
            4.1 Add auxiliary line to the input circuit C_{test}
            4.2 Copy each gate of C_{test} in such a way that
                  target would be fix to the line I.
            4.3 Before the first gate and after the last
                  gate, add n number of CNOT gate whose
                  target is fixed to line I from each n line
             of the circuit.

3.1.2   CNDF Detection Mechanism

Any CNDF in any gate of the circuit is detected if and only if the following condition is true $O_{aux} = \overline{I_{aux}}$.

Lemma 1: For any CNDF in any gate $G_i(D_{G_i}^{x \to y})$, the test vector $T(D_{G_i}^{x \to y})$ can detect the CNDF if and only if $O_{aux} = \overline{I_{aux}}$.

Proof: From any input circuit (C_{input}), the circuit under test (C_{under_test}) is designed in such a way that it always satisfies the statement $O_{aux} = I_{aux}$ for any fault free circuit C_{under_test}.

To illustrate trueness of the statement, let us consider the fault free circuit C_{under_test} of Fig. 1(b). Now, it can be observed that $O_{aux} = I_{aux} \oplus z \oplus y \oplus x \oplus yz \oplus z \oplus y \oplus z \oplus x \oplus yz \oplus y \oplus x \oplus yz \oplus z \oplus y \oplus z \oplus x \oplus yz \oplus y \oplus z \oplus x \oplus yz \oplus y \oplus x \oplus yz = I_{aux}$.

So, for any fault free circuit C_{under_test}, it is always true that $O_{aux} = I_{aux}$. Now for any occurrence of CNDF in the circuit C_{under_test}, it is always true that $O_{aux} = \overline{I_{aux}}$. To check the accuracy of the statement, it is assumed that a CNDF ($D_{G_2}^{y \to x}$) has occurred in the circuit C_{under_test} of Fig. 1(b). Now, $O_{aux} = I_{aux} \oplus z \oplus y \oplus x \oplus \overline{yz} \oplus z \oplus y \oplus z \oplus x \oplus yz \oplus z \oplus z \oplus y \oplus x \oplus yz = I_{aux} \oplus x \oplus y \oplus z \oplus yz$.

At the time of the fault detection, as the control node moves from y to x, the node x always need to set to 1 and other terms would be nullified by default. Now, O_{aux} becomes $O_{aux} = I_{aux} \oplus 1 = \overline{I_{aux}}$. Hence, faults are detected when $O_{aux} = \overline{I_{aux}}$.

■

3.1.3 Test Vector Formation Method for the CNDF

Any CNDF is detected by fixing 0 at the original position of the control node and 1 at the current position of the control node of the circuit under test. Also 1 is set to others control node and 0/1 to the target line and through line of the circuit under test respectively.

Let us consider the circuit of Fig. 2(a) to evaluate the test vector formation method for the CNDF. According to the CNDF detection rule as discussed, the CNDF of $C_{G_0}^{y \to z}$ Fig. 2(a) is detected by $< xyzT > \ = \ < 1\,0\,1\,0 >$ and $< xyzT > \ = \ < 1\,0\,1\,1 >$. So, $T(D_{G_0}^{y \to z}) = \{<1\,0\,1\,0 >, < 1\,0\,1\,1 >\}$.
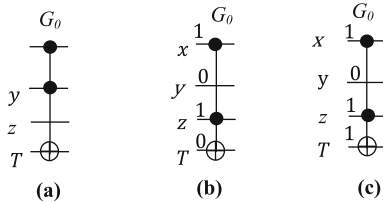

Fig. 2. Formation of Test Vector shown in (b), (c) for the $C_{G_0}^{y \to z}$ in (a).

3.1.4 Detection of the CNDF

Let us take the circuit of Fig. 1(b) which is the circuit under test of Fig. 1(a) to observe the detection mechanism of CNDF in Fig. 1(b). Different possible CNDF in Fig. 1(b) are $C_{G_1}^{z \to x}, C_{G_2}^{y \to x}, C_{G_3}^{x \to y}$ and $C_{G_4}^{z \to x}$. Based on the test vector formation method discussed earlier, generated test vectors for all the CNDF are $T(D_{G_1}^{z \to x}) = \ < 1\,3\,4\,7 >, T(D_{G_2}^{y \to x}) = \ < 1\,2\,4\,6 >, T(D_{G_3}^{x \to y}) = \ < 1\,2\,4\,6 >, T(D_{G_4}^{z \to x}) = \ < 2\,3\,6\,7 >$.

Let us assume that the fault $C_{G_2}^{y\rightarrow x}$ occurs in G_2 of the C_{under_test} in Fig. 1(b) where the control node moves to input line x from the input line y.

So, $O_{aux} = I_{aux} \oplus z \oplus y \oplus x \oplus yz \oplus z \oplus y \oplus z \oplus x \oplus yz \oplus z \oplus z \oplus y \oplus x \oplus yz = I_{aux} \oplus x \oplus y \oplus z \oplus yz$.

To detect the CNDF ($C_{G_2}^{y\rightarrow x}$), any test vector from the list $< 1, 2, 4, 6 >$ can be used. The vector 2 ($<xyz> = <100>$) is chosen from the list and applied over the C_{under_test}. Now, $O_{aux} = I_{aux} \oplus x \oplus y \oplus z \oplus yz = I_{aux} \oplus 1 \oplus 0 \oplus 0 \oplus 0.0 = \overline{I_{aux}}$.

Here, it is observed that $O_{aux} = = \overline{I_{aux}}$ which reveals that there is CNDF in the circuit of Fig. 1(b). Similarly, any CNDF in the circuit under test can be detected in online mode.

Till now, we have seen the behaviour of Algorithm 1 on any reversible circuit constructed with k-CNOT gates. The Example 1 is used to analyse the behaviour of the Algorithm 1 on the ESOP based reversible circuit..

Example 1: Let's consider an ESOP circuit as shown in Fig. 3(a) to see the outcome of Algorithm 1 on the ESOP circuit. The testable circuit implemented by Algorithm 1 is shown in Fig. 3(b).
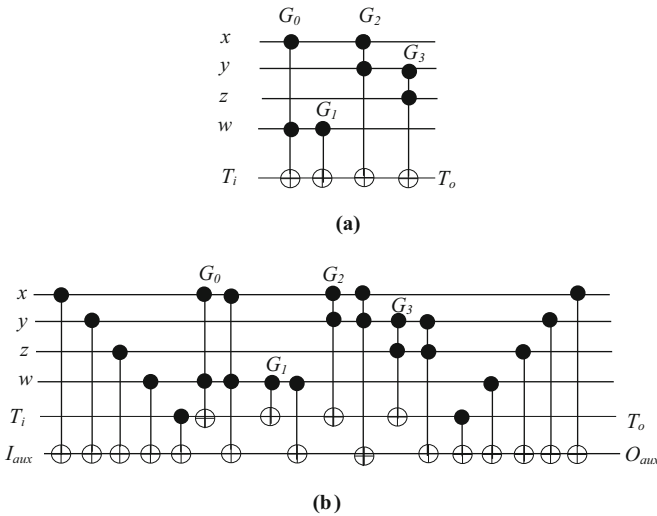

(a)

(b)

Fig. 3. (a) Input *ESOP* circuit (C_{input}) and (b) Circuit Under Test ($C_{under-test}$).

Let us assume that the CNDF ($D_{G_2}^{y\rightarrow z}$) has occurred in G_2 of Fig. 4(b). The said CNDF can be detected by $T(D_{G_2}^{y\rightarrow z}) = \{<xyzw> = <10\ 1\ 0>$ or $<xyzw> = <1\ 0\ 1\ 1>\}$. Due to the fault in the circuit, O_{aux} becomes $O_{aux} = I_{aux} \oplus x \oplus y \oplus z \oplus w \oplus T_i \oplus xw \oplus w \oplus xy \oplus yz \oplus T_i \oplus xw \oplus w \oplus xy \oplus yz \oplus w \oplus z \oplus y \oplus x = I_{aux} \oplus xy \oplus xz$.

Now, for the test vector $< xyzw > = < 1\ 0\ 1\ 0 >$, $O_{aux} = I_{aux} \oplus 1.0 \oplus 1.1 = \overline{I_{aux}}$. Hence, the fault $C_{G_2}^{y \rightarrow z}$ in the testable circuit of Fig. 4(b) is detected.

Here, in this example, it can be observed that total $(2n + G)$ number of more gates (circuit overhead) are required to design the circuit under test to detect CNDF for the ESOP circuit using the Algorithm 1, where n represents total input lines of the input circuit and G means all gates of the input circuit.

3.2 CNDF Testing Scheme Only for ESOP Circuit

It has been experimented that the circuit overhead can be reduced to perform the CNDF test on the ESOP circuit and that is the primary motivation to develop the Algorithm 2 that describes the CNDF detection only in ESOP circuit with minimized circuit overhead. Algorithm 2 is explained in detail in the next section.

3.2.1 Formation of Circuit Under Test

The very same fault detection condition ($O_{aux} = \overline{I_{aux}}$) discussed in Algorithm 1 is also used in Algorithm 2 for the detection of a fault in the testable circuit.
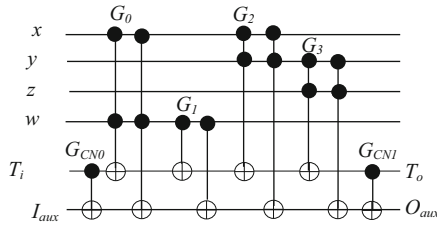

Fig. 4. (a). Final testable circuit $C_{testable}$

ALGORITHM 2: Online Detection of CNDF in
ESOP Based Circuit

Input: ESOP based Reversible Circuit C_{test}

Output: Detection of any CNDF in the $C_{testable}$ Circuit

begin

    Step1: Formation of the Circuit Under Test:

        Transform the input circuit C_{input} to the testable form ($C_{under\text{-}test}$) using the ***circuit-under test()*** function.

    Step2: Test Vector Formation:

    For any control node displacement fault in gate G_i ($D_{G_i}^{x \to y}$), the test vector $T(D_{G_i}^{x \to y})$ is detected by fixing 0 at the original position of the control node and 1 at the current position of the control node of the circuit under test. Also 1 is set to others control node and 0/1 to the target line and through line of the circuit under test respectively.

    Step3: Fault Detection Phase:

    For any control node displacement fault in any gate $G_i(D_{G_i}^{x \to y})$, the test vector $T(D_{G_i}^{x \to y})$ is applied to the testable circuit and if $O_{aux} = I_{aux}$ then it can be con firmed that CNDF is present in the testable circuit.

        //**Detection of CNDF**//

    Step4: ***circuit-under test()***

        begin

            4.1 Add line (ANC) to the input circuit C_{test} .

            4.2 Copy each gate of C_{test} in such a way that target would be fixed to the line ANC.

            4.3 Before the first gate and after the last gate, add a CNOT gate whose target is fixed to ANC line from each n line of the circuit.

3.2.2 Test Vector Formation Method for the CNDF

All possible CNDF for the circuit in Fig. 4(a) are $D_{G_0}^{x \to y}, D_{G_0}^{x \to z}, D_{G_0}^{w \to y}, D_{G_0}^{w \to z}, D_{G_1}^{w \to x}, D_{G_1}^{w \to y}, D_{G_1}^{w \to z}, D_{G_2}^{x \to z}, D_{G_2}^{x \to w}, D_{G_2}^{y \to z}, D_{G_2}^{y \to w}, D_{G_3}^{y \to x}, D_{G_3}^{y \to w}$, $D_{G_3}^{z \to x}$ and $D_{G_3}^{z \to w}$. Required test vectors needed for all the respective CNDFs are $T(D_{G_0}^{x \to y})$ = < 5, 7 >, $T(D_{G_0}^{x \to z}) = $ < 3, 7 >, $T(D_{G_0}^{w \to y}) = $ < 12, 14 >, $T(D_{G_0}^{w \to z}) = $ < 10, 14 >, $T(D_{G_1}^{w \to x}) = $ < 8, 10, 12, 14 >, $T(D_{G_1}^{w \to y}) = $ < 4, 6, 12, 14 >, $T(D_{G_1}^{w \to z}) = $ < 2, 6, 10, 14 >, $T(D_{G_2}^{x \to z}) = $ < 6, 7 >, $T(D_{G_2}^{x \to w}) = $ < 5, 7 >, $T(D_{G_2}^{y \to z}) = $ < 10, 11 >, $T(D_{G_2}^{y \to w})$ = < 9, 11 >, $T(D_{G_3}^{y \to x}) = $ < 10, 11 >, $T(D_{G_3}^{y \to w}) = $ < 3, 11 >, $T(D_{G_3}^{z \to x}) = $ < 12, 13 >, $T(D_{G_3}^{z \to w}) = $ < 5, 13 >.

3.2.3 Detection of the CNDF

Let's consider the CNDF ($D_{G_0}^{x \to y}$) that occurs in G_0 of Fig. 4(a). Hence, the $C_{testable}$ circuit becomes faulty and the expression from O_{aux} becomes $O_{aux} = (I_{aux} \oplus T_i) \oplus (xw \oplus w \oplus xy \oplus yz) \oplus (yw \oplus w \oplus xy \oplus yz) \oplus T_i = I_{aux} \oplus xw \oplus yw$.

The fault $D_{G_0}^{x \to y}$ is identified by $T(D_{G_0}^{x \to y}) = \, < 5, 7 >$. Now apply the test vector 5 i.e. $< xyzw > \, = \, < 0101 >$ over the circuit $C_{under\text{-}test}$ then $O_{aux} = I_{aux} \oplus 0.1 \oplus 1.1 = \overline{I_{aux}}$ is observed. As $O_{aux} = \overline{I_{aux}}$, hence it is confirmed that a CNDF occurred in the circuit of Fig. 4(b). Similarly, the other CNDFs in the circuit can be detected by the described mechanism.

4 Experimental Results

We have tested our technique over a wide range of benchmarks [29] and the obtained results are summarized in Tables 1 and 2 respectively. In Table 1, the overhead calculation (Garbage Output (GO) and Quantum Cost (QC)) of the testable design over non-testable design of our approach (Algorithms 1 and 2) is compared and tabulated for any reversible circuit.

Similarly, in Table 2, Algorithms 1 and 2 of our proposed work is compared to justify the efficiency algorithm when it works only for the ESOP circuit. It has been observed from Table 2 that the ESOP circuit can be tested with the reduced design overhead using Algorithm 2.

Table 1. Overhead calculation of the circuit-under test over the input circuit

Approach	Average overhead for testability feature	
	GO	QC
Approach in [24]	0%	300.67%
Approach in [23]	63409.48%	312.28%
Approach in [30]	5163.03%	388.67%
Approach in [22]	63409.48%	312.28%
Our approach (Algorithm 1)	0%	$(100 + 2n)$%, n is the number of input lines
Our approach (Algorithm 2)	0%	102%

GO, Garbage Outputs; *QC*, Quantum Cost.

Table 2. Comparison of Algorithms 1 and 2 only on ESOP circuit

Benchmark name	GC	Algorithm 1		Algorithm 2			
		GC	Circuit Overhead (%)	GC	Improvement in Circuit Overhead (%)	Reduced GC	Reduced Circuit Overhead (%)
Z4ml	48	110	130	98	102	12	28
Sym9	28	74	164	58	102	16	62
Ex2	15	40	166	32	102	8	64
Frg2	3724	7594	110	7450	102	44	8
apex5	2909	7868	171	5820	102	2048	49

5 Conclusion

Several well-established algorithms are available for fault models like SMGF, PMGF, and MMGF. But, till now no such algorithms are for the detection of the control node displacement fault in online mode. Here in this work, we have implemented a fault detection mechanism to detect the control node displacement fault in the running time of the circuit. The developed fault detection method has been successfully tested over different benchmark circuits and the obtained results have been disclosed in different tables.

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