Design of Diversified Evaluation System of College Teaching Quality Based on Deep Data Mining

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Abstract. At present, the mainstream teaching evaluation is dominated by students, supplemented by experts in or out of school. Under this evaluation method, only simple quantitative evaluation results can be obtained, and the evaluation data can not be analyzed. Therefore, it is proposed to design the diversified evaluation system of college teaching quality based on deep data mining. In the hardware design of the diversified evaluation system of college teaching quality, the ARM microprocessor based on diversified evaluation is designed, and the data manager based on data mining is designed. In the software design of the diversified evaluation system of college teaching quality, the diversified evaluation model of teaching quality is established, Design evaluation model database. The test shows that the evaluation accuracy coefficient of the system is more than 95, which is much higher than the traditional two systems.

Keywords: Data mining · Deep mining · College teaching · Teaching quality · Evaluation system

1 Introduction

The enrollment scale of colleges and universities has continued to expand in recent years, and the annual growth rate has remained at about two percentage points. As the scale of enrollment increases, the quality of students will inevitably decline. The faculty and teaching facilities of colleges and universities have grown relatively slowly, and insufficient teaching resources will inevitably affect the quality of education [1]. In recent years, various reports have often appeared, reflecting the decline in the quality of college graduates and poor work ability, and various aspects of society often comment and question the teaching quality of colleges and universities. Educational departments at all levels of the country continue to adhere to the scientific development concept and carry out in-depth education and teaching reforms [2]. In particular, we will continue to increase investment in college education, strengthen the construction of the teaching staff of colleges and universities, and pay particular attention to the evaluation of the quality of colleges and universities. Among them, the assessment of student abilities is the

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S.-H. Wang and Y.-D. Zhang (Eds.): ICMTEL 2022, LNICST 446, pp. 83–97, 2022.
https://doi.org/10.1007/978-3-031-18123-8_7

focus of teaching quality assessment. Data Mining Technology is a cross-discipline that integrates technologies and achievements in many different fields [3], bringing together multiple disciplines such as machine learning, pattern recognition, expert systems, data visualization, statistics, and high-performance computing. Data mining technology can automatically convert the massive data we collect in our work and life into various styles of information, providing a conversion channel between people and data, and providing us with a very important basis for judgment and decision-making.
Data mining technology has been successfully applied in retail, finance, telecommunications, scientific research and other fields. Provide customers with data analysis, predict potential customers, formulate sales strategies, avoid business risks and improve service quality. In the field of Education [4], data mining technology also has certain applications, mainly in network education. A large number of researchers obtain the information of teachers and students and their interaction information through the network online education platform, obtain relevant information through data mining technology, and then put forward suggestions to teachers, use more appropriate teaching methods [5], and constantly improve the teaching level and quality. However, this is only limited to network teaching, but data mining technology is rarely used in most classroom teaching.

Therefore, this paper designs a diversified evaluation system of college teaching quality based on deep data mining. Main design route of the system:

Step 1: in the hardware design of the diversified evaluation system of teaching quality in Colleges and universities, the ARM microprocessor based on diversified evaluation is designed;
Step 2: design the data manager based on data mining, establish the diversified evaluation model of teaching quality and design the evaluation model database in the software design of diversified evaluation system of teaching quality in Colleges and universities.
Step 3: experimental analysis.
Step 4: conclusion and future outlook.

2 The Hardware Design of the Diversified Evaluation System for Teaching Quality in Colleges and Universities

2.1 Design an ARM Microprocessor Based on Diversified Evaluation

The ARM architecture is the first RISC microprocessor designed for the low-budget market. In addition to some features of RISC, the ARM architecture also uses some special technologies to minimize the chip area and reduce the chip area while ensuring high performance. Power consumption [6]. The ARM microprocessor has the following main features: small size, low power consumption, low cost, high performance; support Thumb (16-bit) and ARM (32-bit) dual instruction set; a large number of registers are used, and the instruction execution speed is faster; Most data operations are completed in registers;—The addressing mode is flexible and simple, and the execution efficiency is high;—The instruction length is fixed; ARM microprocessors are mainly used in industrial control, wireless communication, network applications, consumer electronics, imaging products, and security products, Storage products, and the automotive industry.

The operating frequency of the system largely determines the processing power of the ARM microprocessor. The typical processing speed of ARM7 series microprocessors is 0.9 MIPSMHz, and the common ARM7 chip system main clock is 20 MHz–133 MHz. Different chips deal with clocks differently. Some chips only need one master clock frequency, and some chip internal clock controllers can provide clocks of different frequencies for the ARM core and USB, UART, DSP, audio and other functional components. Most of the on-chip memory capacity of ARM microprocessors is not too large. Users need to expand the memory when designing the system. However, some chips have relatively large on-chip storage space. Simplify the design of the system.

Serial interface circuit is used for short-distance two-way serial communication between S3C4510B system and other application systems. One serial port is a full-function serial port, and the other serial port is shared by RS232/RS485; the reset circuit can complete system power-on Reset and user button reset when the system is working. It also has a watchdog function, and can reset the system board core, system board and JTAG respectively;-The power supply circuit is a 5 V to 3.3 V DC-DC converter, which is S3C4510B And other peripheral circuits that require 3.3 V power supply; 10 MHz active crystal oscillator provides the working clock for the system, and is multiplied by the on-chip PLL circuit to 50 MHz as the working clock of the microprocessor; - FLASH memory can store the debugged user applications, Embedded operating system or other user data that needs to be saved after the system is powered off; SDRAM memory is the main area of the system when it is running, the system, user data, and stack are all located in the SDRAM memory; - 10M/100M Ethernet interface is the system Provides a physical channel for Ethernet access. Through this interface, the system can access Ethernet at a rate of 10M or 100 Mbps;-The USB interface provides two downstream ports and one upstream port that comply with the USB1.1 specification [7]. It can be used as a USB host to connect to a USB device, it can also be used as a USB device to communicate with a PC, and it can also work in a USB bridge mode. The JTAG interface is used to access all the components inside the chip, through which the system can be debugged, programmed, etc.; IIC memory can store a small amount of user data that needs to be stored for a long time;—LED digital display is used as the digital information of the system parameters Display; The configuration circuit is mainly used by the user to configure the operating state of the system by adjusting the level of some pins of the ARM microprocessor [8];—The keyboard module is an expansion board of the system, using 64 key functions and 8 A 7-segment digital display provides more human-computer interaction functions. LCD expansion board is mainly used to display Chinese and Western characters and simple graphics; CPLD expansion board is used to implement some user-defined logic and complete specific logic operations; a real-time clock expansion board is mainly used as a system clock reference;–ADC expansion board completes the conversion of analog quantity to digital quantity for further processing by ARM microprocessor; DAC expansion board converts the digital quantity calculated by ARM microprocessor into analog quantity, which acts on the controlled object; IDE expansion board is used Connect IDE hard disk to realize large-capacity storage of data;-Audio input and output expansion board can realize the collection, processing, amplification and output of audio information;-Video input expansion board

mainly completes the collection and compression of video information for ARM microprocessing The device is further processed; the system bus expansion leads to the data bus, address bus and necessary control bus, which is convenient for users to expand the peripheral circuit according to their own specific needs.

2.2 Design Data Manager Based on Data Mining

In addition to the ARM7TDMI core, the more important on-chip and off-chip function modules of S3C4510B include: 2 buffer descriptors HDLC channel, 2 UART channels, 2 GDMA channels, 2 32-bit timers and 18 programmable I/O ports. The on-chip logic control circuit includes: an interrupt controller DRAM/SDRAM controller ROM/SRAM and flash controller system manager, an internal 32-bit system bus arbiter and an external memory controller. The structural block diagram of S3C4510B is shown in Fig. 1:

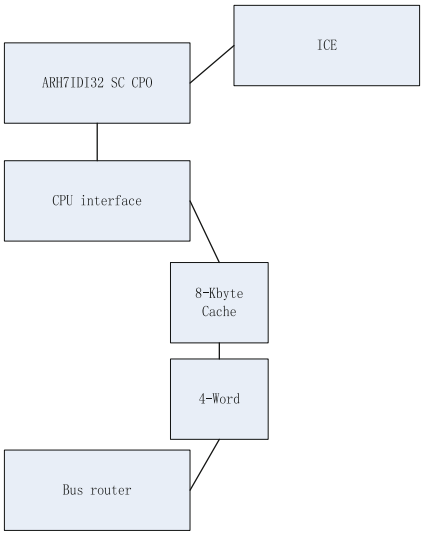

Fig. 1. Data manager structure

This manager is used in an integrated system for embedded Ethernet applications-full 16/32 RISC architecture-supporting large and small endian modes. The internal architecture is big-endian mode, and the external memory can be big-endian or small-endian mode. A high-efficiency and powerful ARM7TDMI processor core is included-a cost-effective, JTAG interface-based debugging solution, boundary scan interface.

The System Manager of the S3C4510B microprocessor plays a vital role in the work of the entire system. It mainly has the following functions: Based on a fixed priority [9], it arbitrates the system bus access requests from several main functional modules.—Provide necessary memory control signals for accessing external memory. For example, if the DMA controller or CPU wants to access a certain address of the DRAM group, the DRAM controller of the system manager will generate the necessary normal/EDO

or SDRAM access signals. The signal to access normal/EDO or SDRAM can be set by SYSCFG. It provides necessary signals for bus communication between S3C4510B and ROM/SRAM and external IO group. The difference in bus width is coordinated for the data flow between the data bus of the external memory and the internal data bus. For external memory and IO devices, S3C4510B supports both little-endian mode and big-endian mode access. By generating an external bus request signal, the peripheral can access the external bus of the S3C4510B. In addition, S3C4510B can access low-speed peripherals by inserting a wait period (WAIT signal). The WAIT signal is generated by the peripheral, which can extend the memory access cycle of the CPU.

2.3 Design System Storage Mapper

S3C4510B uses unified addressing to map the system's off chip memory, on-chip memory, special function registers and external I/O devices to a 64 MB address space. At the same time, in order to facilitate management, the address space is divided into memory groups as shown in Fig. 1. If there are multiple memory groups, they can be configured to include Base Pointer and End Pointer Set the size and position of each memory group. Users can use the base pointer and tail pointer to set continuous memory mapping. The specific operations are as follows: set the address of the base pointer of a memory group to the address of the tail pointer of the previous memory group. Please note that when setting the control register of the memory group, the address of each two connected memory groups Address spaces must not overlap, even if these groups are disabled [10]. The starting physical address of each group is "base pointer moves 16 bits left" and the physical address at the end of each group is "tail pointer moves 16 bits left - 1".

The starting address of external I/O group 1 is equal to the starting address of external I/O group 0 + 16 KB. Similarly, the starting address of external I/O group 2 is equal to the starting address of external I/O group 0 + 32 KB, the starting address of external I/O group 3 is equal to the starting address of external IO group 0 + 48 KB. Therefore, the total continuous addressable range of the four external groups is defined in the starting address of external I/O group 0 + 64 KB of address space. In the entire addressable address space, the start address of the external I/O group is not fixed. By setting the base pointer of the group, a specific group start address can be set, but the total address space is continuous 64 KB.

After power-on or system reset, the address pointer registers of all groups are initialized to their default values. At this time, all group pointers (except ROM/SRAM/Flash group 0 and special function register group) are cleared. This means: Except ROM/SRA MF lash group 0 and special function register group, all other groups are undefined when the system is started. When the user is designing a program, it is generally necessary to first define the storage space of the system by configuring the corresponding register.

The reset values of tail pointer and base pointer of ROM/SRAM/flash group 0 are 0x200 and 0x0 respectively. This means that after system reset, the address space of ROM/SRAM/flash group 0 will be automatically defined as 32 MB, and the actual address range is 0x00000000–0x02000000-1. This initialization definition of ROM/SRAM/flash group 0 enables the system to hand over the control of the system to the startup code written by the user after power on or reset. Of course, these startup codes should be stored in the external ROM and mapped to ROM/SRAM/flash group 0.

When the startup code is executed, it performs various system initialization tasks, and reconfigures the memory mapping of the system according to the actual situation of the external memory and equipment of the application system.

The base address pin of the special function register group is initialized to 0x3ff0000 during system reset, and generally will not be changed. The mapper is described in Table 1:

Table 1. System storage mapper parameters

Mapper element	Offset	Operate	Describe	Reset amount
SYSCFG	0.0000	Read, Write	System configuration Register	0 × 37FFFF91
CLKCON	0.3000	Read, Write	clock control register	0 × 37FFFF91
EXTACONO	0.3008	Read, Write	Register 1	0 × 37FFFF91
EXTDBWTH	0.3000	Read, Write	Register 2	0 × 37FFFF91
ROMCON1	0.3018	Read, Write	Controller	0 × 37FFFF91
ROMCON2	0.3011	Read, Write	Controller	0 × 37FFFF91
ROMCON3	0.3024	Read, Write	Controller	0 × 37FFFF91

The S3C4510B microprocessor can detect and respond to the bus request signal (Ext MREQS) generated by the external bus master. When the CPU sends out the external bus response signal (Ext MACK), the bus control is handed over to the external bus master, and the external bus request signal should continue to be valid at this time. When the external bus response signal of S3C4510B is valid, its memory interface is in a high-impedance state so that the external bus master can drive the external memory interface. When the S3C4510B does not control the bus, it will no longer perform DRAM refresh operations. Therefore, when the external bus master obtains bus control and it will last for a long time, it must be responsible for completing the DRAM refresh operation.

3 Software Design of the Diversified Evaluation System for Teaching Quality in Colleges and Universities

3.1 Establish a Diversified Evaluation Model for Teaching Quality

The mathematical model of fuzzy comprehensive evaluation is composed of index set T, judgment set P and judgment matrix R. Establish a hypothetical set of known indicators:

$$T = \{t_1, t_2, ...t_m\} \tag{1}$$

Among them, $\{t_1, t_2, ..t_m\}$ represents the composition of known indicators and m is the number of known indicators.

Judgment set:

$$P = \{p_1, p_2, ...p_m\} \tag{2}$$

Among them, $\{p_1, p_2, ...p_m\}$ represents the composition of the evaluation index data. The weight of each indicator is the fuzzy subset Q on T:

$$Q = (q_1,\ q_2, ...q_m) \tag{3}$$

Under the traditional teaching method, the assessment method of students' ability is mainly through the "examination + usual" mode. "Examination" is based on the final exam of each semester, and an exam is used to assess the degree of mastery of a certain course. "Usually" is mainly based on the teacher's subjective impression evaluation of the students' learning process during a semester. This kind of evaluation is highly subjective and arbitrary, and cannot objectively evaluate the students' learning process. In order to enhance the objectivity of "normal grades", many teachers will subdivide their grades, adding subdivision grades such as "homework", "attendance", and "experiment". There are also many shortcomings in the way of subdividing the grades, such as the inability to confirm whether the homework and experiment are completed independently, and so on. Based on the above situation, q_i in formula (3) is the weight corresponding to i indicators, then:

$$\sum_{i=0}^{m} q_i = \frac{Q}{P} \tag{4}$$

Suppose the evaluation of the i index is the fuzzy relationship from T to P:

$$R_i = (r_{i1}, r_{i2}..., r_{im}) \tag{5}$$

When the evaluation model is established, it is integrated into the evaluation model. The mining requirements are random and usually have no special requirements. The output of data mining may be hidden and possibly related information; Data mining has certain prediction function. By mining the information in the database, we can find the possible accidental events and predict the accidental events; Fast response to data changes. Because the changes of information and demand are relatively rapid, data mining needs to respond quickly to these needs and changes and respond in time. Data mining is more about maintaining and updating rules and requirements; The accuracy of data mining depends on a large amount of data. Only after analyzing a sufficient amount of data, the results are scientific and the laws are credible. The steps of data mining in the evaluation model are:

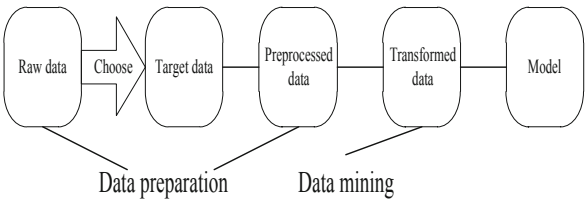

Fig. 2. Steps of data mining

In Fig. 2, in the data mining of the evaluation model, first select the original data, then determine the key data to be mined, preprocess according to the determined data, and transform the transformed data into patterns to complete the in-depth data mining.

Data preparation is similar to requirements analysis in the software development process. First, determine the source of the data, and preprocess the data so that the system can identify and operate, and then the data needs to be transformed and subtracted. Data selection refers to selecting useful data to be processed from a large amount of data stored in the database. In this step, the selected data will be processed preliminarily, so that these data can be recognized and manipulated by the data mining system. The main operation in this step is to check for deficiencies and delete data that does not meet the requirements. The evaluation matrix of m indicators is established as:

$$R = \bigcup_{i=1}^{\mathrm{m}} R_i = \begin{bmatrix} r_{11}, r_{12}, \ldots r_{1n} \\ r_{21}, r_{22}, \ldots r_{2n} \\ \ldots \\ r_{m1}, r_{m2}, \ldots r_{mn} \end{bmatrix} \tag{6}$$

Therefore, the result of comprehensive evaluation is the synthesis of Q and R

$$E = Q^{\circ}R = (e_1, e_2, \ldots e_n) \tag{7}$$

It is a matrix with m rows and n columns, which is a fuzzy subset of P. After computer simulation and comparison, the combined operation of the teaching quality evaluation in the system adopts the weighted average type. If the system is more complex, there are many indicators to consider, and there are levels of division between the indicators, then you can also use the indicator set T to comprehensively evaluate each category in some way, and then perform the evaluation results. The high-level comprehensive evaluation between "classes" is the so-called multi-level comprehensive evaluation. At this time, in the indicator set T, t consists of k sub-indicators:

$$t = \{t_{11}, t_{12}, \ldots, t_{1k}\} \tag{8}$$

t2 consists of j sub-indicators:

$$t_2 = \{t_{21}, t_{22}, \ldots, t_{2j}\} \tag{9}$$

By analogy, we can get:

$$t_m = \{t_{m1}, t_{m2}, \ldots, t_{ml}\} \tag{10}$$

In the formula, k, j, 1 etc. can be taken as $1, 2 \ldots$, etc. according to the actual situation. Therefore, according to the relationship between each indicator, an indicator relationship table can be divided and constructed, as shown in Table 2 (in the Table 2 indicators and 2 layers are taken as an example), where qi and qij respectively represent the weight of each main indicator and sub-indicator:

This step is the main step of data mining and the embodiment of the core technology of data mining. At this stage, the processed data are mined, and the result is to find

Table 2. The relationship table of the divided structure index

Second floor			Level one		
Serial number	Evaluation index	Weights	Serial number	Evaluation index	Weights
One	t1	q1	1	t11	q11
			2	t12	q11
Two	t2	q2	1	t21	q21
			2	t22	q22
			3	t23	q23
			4	t24	q24
			5	t25	q25

the hidden rules in the data. In the data mining stage, there are also the following steps: determine the specific methods of data mining: different data formats and types, different methods; Different methods are adopted for different results. Therefore, at this stage, the method selection should be made for different data. Select mining algorithm: for different formats of data and different needs, different mining algorithms should be selected. Different algorithms have different accuracy and different mining results. Mining implementation: use appropriate methods and algorithms to mine data on data sets.

3.2 Design Evaluation Model Database

The target objects of this system are mainly students, teachers and administrators. The target objects of this system are mainly students, teachers and administrators. After students log in to the system, they can complete the following operations on the corresponding interface. Viewing personal information: Students can enter this page to view personal information. Online teaching function: students can enter this interface to perform related operations such as course selection and evaluation. Others: students can perform account-related operations such as login and logout. The school's teaching quality evaluation system has its own unique features. After summary analysis, it mainly includes: There are three main types of users of the system: students, teachers, and administrators of the evaluation system; in the actual operation of the school, the relationship between teachers, students and courses It is a one-to-many relationship. The system will be recorded in this system. Since there are three main types of users, these three types of users correspond to three entities: students, teachers, and administrator entities, which are mainly related to courses, etc. In addition, it is also necessary to record the information of students and teachers. Course information.

After the physical structure design of the database is completed, these physical designs need to be transformed into logical designs. Scientific database design can effectively organize data, save storage space, ensure data integrity and improve data access speed.

In the teaching quality evaluation system, users are divided into teachers, students and administrators. Among them, the relationship between teachers, students and courses is one to many. A teacher can teach multiple courses, and students can also choose multiple courses. At the same time, students need to score a course and its corresponding teachers. Teachers can view the student scores of the courses they teach. According to the above analysis, the data tables to be created include:

(1) Student information table: The fields in this table include basic information such as student ID, name, password and class department, among which the student ID is the main key, and the rest of the fields cannot be empty.
(2) Teacher information table: The fields of this table include personal information such as the teacher's number, name, etc., as well as information such as the course department, and the teacher's number is the primary key.
(3) Administrator table: The fields of this table include personal information such as the administrator number. The number is the primary key.
(4) Course table: The fields of this table include information such as course number, name, teacher, and teaching time and place.
(5) Course selection record table, including data items: course number, course name, student number.
(6) Student evaluation record table: The fields of this table include information such as student number, teacher number, course number, and evaluation score.
(7) Teacher score record table: The fields contained in this table include information such as the teacher's number, name, course number, and score.
(8) Message form: number, message, teacher number, teacher name. According to the above data table, when the actual database design is carried out, it is necessary to restrict the fields in the data table and the relationship between the table and the table, so as to ensure that the database design conforms to the standard paradigm. The structure of each data table in the database is shown in Table 3, 4 and Table 5:

Table 3. Teacher number table

Serial number	Field name	Type	Illustrate
1	T_number	Char(8) not null	Teacher ID
2	T_name	Varchar(8)	Teacher's name
3	T_tech	Varchar(2)	Teacher title
4	T_major	Varchar(20)	Teacher professional direction
5	Deptnumber	Varchar(8)	Faculty number of the teacher

The user's model is independent of any kind of data model and any specific database management system (DBMS). Therefore, it is necessary to convert the conceptual model to a data model supported by a specific DBMS, and then establish the database that the user needs. This system uses SQLServer2020 as the database management system to establish the evaluation system database (teaching).

Table 4. Student table

Serial number	Field name	Type	Illustrate
1	S_number	Char(8) not null	Student ID
2	S_name	Varchar(8)	Student name
3	S_sex	Varchar(2)	Student gender
4	deptnumber	Varchar(20)	Student's department number
5	S_pawd	Varchar(8)	System login password

Table 5. Evaluation index data table

Serial number	Field name	Type	Illustrate
1	Deptnumber	Varchar(8) not null	Department number
2	Tarnumber	Char(4) not null	Evaluation index number
3	Tarname	Varchar(12)	Evaluation index name
4	tarkind	Varchar(8)	Evaluation index category (theory, experiment, sports)
5	tardate	Varchar(9)	Semester of the school year using evaluation indicators

4 Test Experiment

In order to verify the practicability of the system designed in this paper, the system test experiment is designed. Software test is the key step to ensure software quality. It is the final review of software specification, design and coding. The purpose of software testing is the process of executing the program in order to find the errors in the program. A good test scheme is a test scheme that is very likely to find the errors that have not been found so far.

4.1 Test Preparation

In order to make the evaluation results of teaching quality universal, the courses with a large number of students are selected as the test objects, including advanced mathematics, College English, college physics, computer foundation and program design. In order to analyze the performance of the university teaching quality evaluation system integrated with neural network, the simulation test is carried out. The parameter settings of the simulation test environment are shown in Table 6:

Under the above experimental environment setting conditions, the experimental analysis is carried out. In the experiment, the English Majors of a certain school are selected as the sample data, and the student quality of 100 students of the major in the first half

Table 6. Test environment

Environment type	Parameter	Parameter value setting
Hardware	CPU	Intel Core i510500
	RAM	Kefu DDR4 2666 8 GB
	Motherboard	MSI B450M MORTAR
	Hard disk	Western Digital Blue Disk 1TB64MB
Software	Programming tools	Java
	Operating system	Linux

of the semester is analyzed for research and analysis. The number of experimental iterations is 120, and the evaluation accuracy of the experimental sample is analyzed through iteration. The specific sample teaching scenario is shown in Fig. 3:

Fig. 3. Specific sample teaching scenario.

Choose RBF neural network, BP neural network, this paper design college teaching quality evaluation system to conduct comparative experiments, and use college teaching quality evaluation correct rate as the result evaluation index. Randomly select 1000 sample data from the sample data in Table 2 to form the verification sample set, and the others are used as the training sample set to obtain the correct rate of college teaching quality evaluation of various systems as shown in Fig. 4:

The test results are shown in Fig. 4. The evaluation accuracy of the evaluation system designed in this paper is more than 95%, which is higher than the evaluation coefficient of the other two methods.

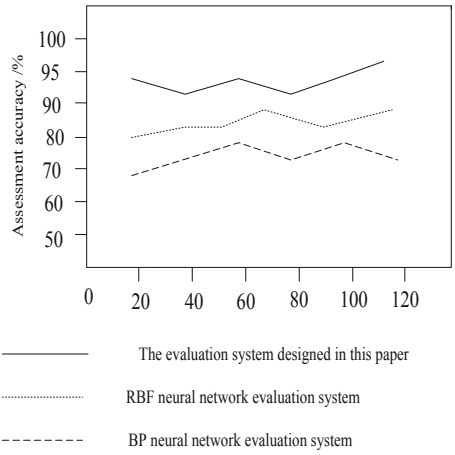

Fig. 4. Test results

The experiment analyzes RBF neural network, BP neural network and the university teaching quality evaluation system designed in this paper to compare the evaluation time. The results are shown in Fig. 5:

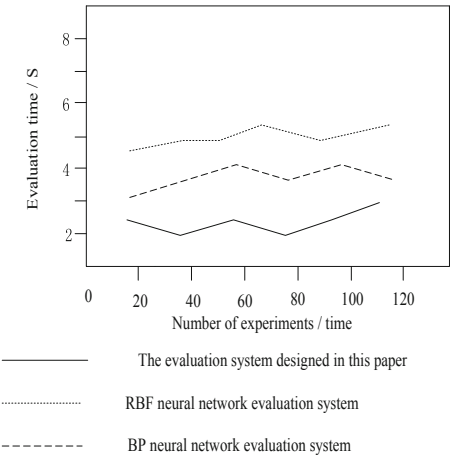

Fig. 5. Time consuming analysis of teaching quality evaluation system in Colleges and universities with different methods

By analyzing the experimental results in Fig. 5, it can be seen that there are some differences in the results obtained by comparing the evaluation time using RBF neural network, BP neural network and the college teaching quality evaluation system designed in this paper. Among them, the evaluation using RBF neural network and BP neural network takes a long time, and the evaluation using the university teaching quality evaluation

system designed in this paper takes a short time, which verifies the effectiveness of the proposed method.

5 Conclusion

This paper proposes to design a diversified evaluation system of teaching quality in Colleges and Universities Based on data mining technology. In the hardware design of the diversified evaluation system of teaching quality in Colleges and universities, the ARM microprocessor based on diversified evaluation and the data manager based on data mining are designed. In the software design of the diversified evaluation system of teaching quality in Colleges and universities, the diversified evaluation model of teaching quality is established and the evaluation model database is designed. Realize the design of diversified evaluation system of teaching quality in Colleges and universities, find these potential relationships and summarize the laws according to the association rule technology in data mining, so as to better support the management of teaching quality. The test shows that the evaluation accuracy coefficient of the system is more than 95, which is much higher than the traditional two systems. Although the existing method research at this stage is feasible, there are some deficiencies in determining the key degree of indicators in the selection of quality evaluation indicators, which need to be improved.

Fund Project. 1. Demonstration Project of Grass-roots Teaching Organization (Teaching and Research Office): Teaching and Research Office of Basic Principles of Marxism; No.: (2020JCJS01)

2. University-level undergraduate engineering project: "Introduction to Basic Principles of Marxism" first-class course of social practice; No: (2020SHSJ03)

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