A Regulated Sensing Solution Based on a Self-reference Principle for PCM + OTS Memory Array

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Abstract. Phase change memory (PCM) device associated with Ovonic Threshold Switch (OTS) selector is a proven solution to fill the gap between DRAM and mass storage. This technology also has the potential to be embedded in a high-end microcontroller. However, programming and reading phases efficiency is directly linked to the selector's leakage current and the sneak-path management. To tackle this challenge, we propose in this paper, a new sense amplifier able to generate an auto-reference taking into account leakage current of unselected cells, including a regulation loop to compensate voltage drop due to reading current sensing. This auto-referenced sense, built on the charge-sharing principle, is designed on a 28 nm FDSOI technology and validated through extensive Monte-Carlo and corner cases simulations. Layout and post-layout simulation results are also provided. From the simulation results, our sense amplifier is demonstrated to be robust for an ultra-large range of sneak-path current and consequently for a large range of memory array size, suitable for embedded memory in high-end microcontroller.

Keywords: PCM · OTS · Non-volatile memory sensing · Sneak-path compensation

1 Introduction

The evolution of edge computing, with AI and data-intensive treatment, exacerbates the requirement in terms of performances and memory capacity on edge devices, such as the high-end Micro Controller Unit (MCU) [1–5]. In this context, high-density memory based on emerging concept could replace current solutions such as 1.5T NOR Flash memory or 1T1R Phase Change Memory (PCM) [6–12]. In this context, to decrease drastically the bit cell footprint, a back-end selector solution could be adopted. Doing so, this new embedded solution could rely on the most mature back-end memory solution namely Phase Change Memory. The PCM which material phase modifications directly affect its resistance (1R) value can be associated with Ovonic Threshold Switch (OTS)

Published by Springer Nature Switzerland AG 2022
V. Grimblatt et al. (Eds.): VLSI-SoC 2021, IFIP AICT 661, pp. 225–243, 2022.
https://doi.org/10.1007/978-3-031-16818-5_11

selector (1S) [13–18], in order to form an 1S1R bit cell. However, due to process compatibility in an embedded context, OTS may require specific adjustments [19]. Beyond the well-known feature of PCM cells already demonstrated in the literature, i.e. a large resistance ratio of 10^3, a low variability thanks to a bulk phase change (crystalline and amorphous state) compared to the filamentary resistive memory, a mature process, and a large endurance 10^9 [9–12], the performances of memory with OTS as selector is mainly driven by the OTS selectivity. Regarding the OTS selectivity feature, numerous papers have reported very different performances [14, 20, 21], with selectivity ranging from 10^3 to 10^7.

The impact of the selectivity of the OTS at array level is characterized by the level of the leakage current sum due to the unselected cells during the programming and the reading operations. Thus to compensate for the impact of this leakage, defined also as sneak-path current, some circuits design techniques have been already proposed:

- The first technique proposed to limit the sneak-path current impact is based on well-chosen biasing conditions applied on the unselected row and column in the memory array. These techniques are namely *V/2* and *V/3* biasing solutions [22, 23];
- The second technique is based on sneak-path current measurement during a first pre-programming or pre-reading phase in order to adapt the biasing voltage to compensate for the amount of sneak current [24, 25];
- The third technique consists in collecting a mean sneak current coming from a compensation port and add it from a reference [26] during the operation.

As shown, compensation schemes are must-have solutions when dealing with crossbar array, but to the best of our knowledge, sensing circuit solution with auto-compensation of the leaky current and autoregulation of the row and column biasing has never been proposed at circuit level targeting a large range of OTS selectivity. In this context, the main contributions of this paper are as follows:

- we introduce, for the first time, an auto-referenced sense amplifier for PCM associated with OTS, where sensing reference is self-adapted to the leakage level. (Sects. 2 & 3);
- we also introduce a regulation loop to dynamically change the biasing conditions of the lines in the array depending on the sneak-path current but also on the reading current through the selected cell. (Sects. 2 & 3);
- we carry out functional (Sect. 3) and extensive Monte-Carlo simulations taking into account global and local variability, as well as corner cases of process, voltage and temperature (PVT), to demonstrate the robustness of our solution for a large range of OTS selectivity (Sect. 4);
- we evaluate the circuit area on a 28 nm FDSOI technology from STMicroelectronics and propose a layout of the solution together with post-layout simulations in order to assess the robustness of the solution against parasitic elements (Sect. 5).

Compared to our previous publication [27], the area estimation of the solution in an advanced 28 nm FDSOI node is given together with post-layout simulation results. We

point out that the area of the proposed solution is dominated by the regulation loop, that is constrained by middle voltage, large load and fast response time.

2 Proposed Sensing Solution Overview

In array consisting of 1S1R bit cell, as presented in the introduction, using a half bias (*V/2*) strategy during a read operation, the cells sharing the same column and the same row as the accessed cell are half biased, inducing sneak-path currents. The consequence is twofold:

- The column sneak-current adds an extra-current to the one crossing the accessed cell with the risk of blurring the cell read current;
- The row sneak-current uses extra-current than the one needed to read the cell with a risk of drop-out of the read voltage *V*.

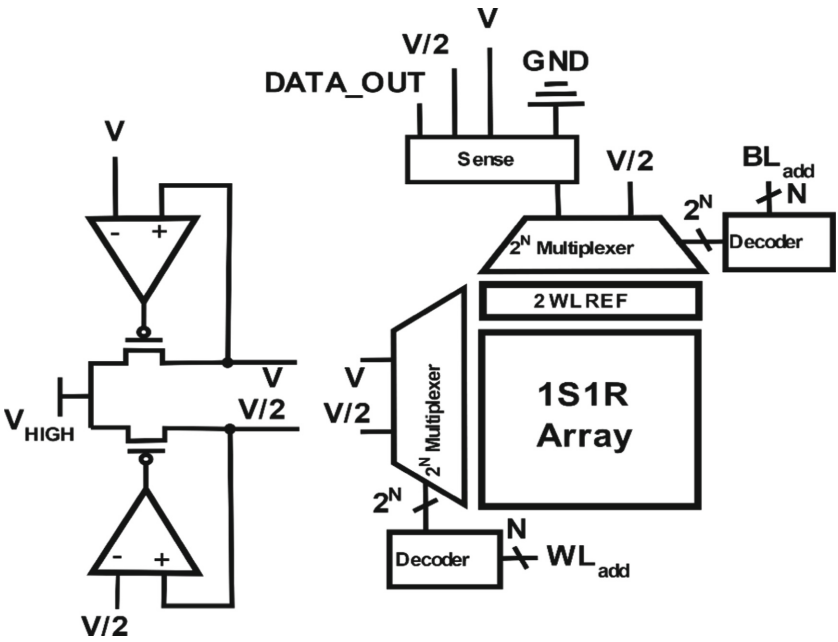


Fig. 1. Global architecture scheme, including LDO to generate V and V/2 voltages regulated from our sense amplifier regulation loop

Both sneak-path currents of course depend on OTS selectivity as well as array size, these two parameters are being linked. Consequently, any sensing solution developed for 1S1R array should be able to:

- Compensate the sneak-path current to solely isolate the contribution of the read current crossing the accessed cell;

- Regulate the applied read voltage *V* on the selected lines and *V/2* on the unselected lines to compensate for large read current due to sneak-path and read current above the OTS selector's hold current [24].

Our proposition follows these two requirements. First of all, as illustrated in Fig. 1, knowing the read voltage to be applied on the array, we use a regulator loop inside the sense amplifier solution to compensate the read voltage drop due to the current sensing, which is dependent on the accessed PCM cell state (HRS or LRS) but also of the sneak-path current amplitude. The principle is to add to the read voltage V_{READ} and respectively $V_{READ}/2$, the voltage drop in the sense amplifier in order to have constant voltage, *V* and respectively *V/2,* applied to the array.

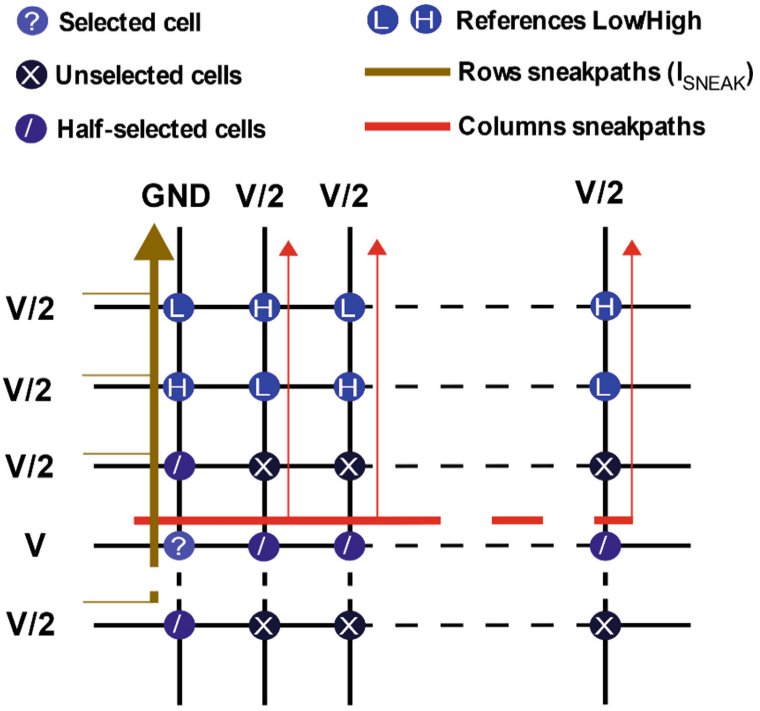


Fig. 2. 1S1R array with 2 references rows, illustrating also row sneak path and column sneak path during bit cell selection.

In a second time, we also introduce two references rows as depicted in Fig. 2. The two reference rows exhibit 1S1R cells with for each column a PCM in HRS and one in LRS. The main idea is to sense, prior to the selected cell of a given column, both references cells sharing the selected column. Doing so, we preserve the sneak-path current context, and we are able to generate a voltage reference that cancels the sneak-path current.

The reference generation is built using the charge sharing principle, in three functional phases. During the first phase, the sense input capacitor is charged using the LRS

1S1R reference cell resulting in a capacitor-voltage given in (1).

$$V_{IN} = \frac{(I_{LRS} + I_{sneak}) * T}{C} \tag{1}$$

With T the charging time, C the sense input capacitor, I_{LRS} the current through the LRS 1S1R cell reference, and I_{sneak} the sneak path current of the selected column.

During the second phase, the input capacitor is further charged using the HRS 1S1R reference cell, resulting in a new capacitor-voltage given by:

$$V_{IN} = \frac{(I_{LRS} + I_{sneak} + I_{HRS} + I_{sneak}) * T}{C} \tag{2}$$

With I_{HRS} the current through the HRS 1S1R cell reference.

In the third phase, a charge sharing process occurs, using a reference capacitor equal to the input capacitor C. Doing so, the reference voltage is given by:

$$V_{REF} = \frac{(\frac{I_{LRS}+I_{HRS}}{2} + I_{sneak}) * T}{C} \tag{3}$$

Thus when reading the selected cell, the input capacitor voltage is determined by:

$$V_{IN} = \frac{(I_{CELL} + I_{sneak}) * T}{C} \tag{4}$$

And knowing that C and T are the same in (3) and (4), it is straightforward to see, that the sneak current is compensated and that I_{CELL} (the selected cell current) is compared solely to $\frac{I_{LRS}+I_{HRS}}{2}$.

It is also important to note that any temperature drift in the 1S1R cell might be compensated by this self-reference generation.

3 Sense Amplifier Circuit Description

3.1 Circuit Description

The full scheme of our new self-referenced sensing solution is illustrated in Fig. 3. It is composed mainly of three blocks:

- The regulation block (Fig. 3a), which is mainly composed of two current mirrors generating the reference voltages V and $V/2$, used as input for the LDOs biasing the array rows and columns, from respectively the inputs V_{READ} and $V_{READ}/2$;
- The capacitor block (Fig. 3b), which exhibits the input capacitor C_{IN} and the reference capacitor C_{REF} both equal to the same value C. They are used for auto-reference generation through charge-sharing;
- The comparator block (Fig. 3c), which is built with a StrongARM comparator [28] followed by an RS latch to produce the sense output *DATA_OUT*.

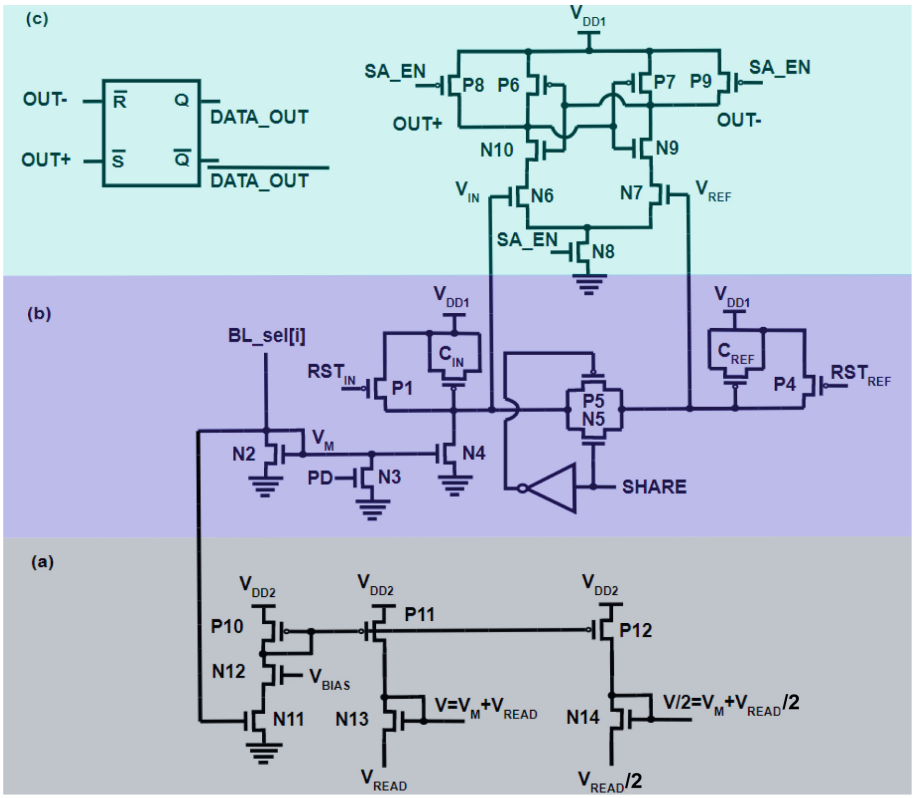


Fig. 3. Schematic of the proposed sense circuit with three main blocks: (a) the regulation block, (b) the capacitor block and (c) the comparator block.

Regulation block: Ideal biasing voltages for a read operation, that should be applied to the selected cell and unselected rows and columns are noted respectively V_{READ} and $V_{READ}/2$ on the Fig. 3.c. However, to ensure a constant read voltage and a constant inhibition, these voltages (V_{READ} and $V_{READ}/2$) have to be regulated depending on the amount of current flowing into the input branch of the sense amplifier during a read operation. Indeed, depending on the selected cell state and the sneak path contribution, the potential V_M is more or less increasing, reducing the applied potential on the selected cell to V_{READ}-V_M and on unselected rows and columns to $V_{READ}/2$-V_M. It is thus mandatory to add the corresponding potential V_M to the ideal biasing voltages V_{READ} and $V_{READ}/2$. In doing so, the LDOs reference voltages (see Fig. 1) are respectively set to $V = V_M + V_{READ}$ and $V/2 = V_M + V_{READ}/2$. Consequently, the resulting potential differences on the selected cell and on the unselected rows and columns, become respectively $V_M + V_{READ}$-$V_M = V_{READ}$ and $V_M + V_{READ}/2$-$V_M = V_{READ}/2$. To achieve this task, a copy of the V_M potential is performed through current mirrors composed of transistors P10, P11, and P12. N13, and N14 act as active charges to add respectively V_M to V_{READ} and $V_{READ}/2$. Please note, that N12 safeguards N11 from high swing voltage and needs adequate biasing for quick regulation.

Capacitors block: The principle of current acquisition is based on the voltage discharge of the input capacitor C_{IN} through a current mirror composed of N2 and N4. Thus, prior to any current acquisition, C_{IN} is charged to V_{DD1} through P1 by pooling down signal RST_{IN}. In a similar way, before any reference voltage generation, through sharing activation (signal $SHARE = $ '1'), C_{REF} is charged to V_{DD1} through P4 by pooling down signal RST_{REF}. A pull-down transistor N3 is added to ensure that N4 is cut-off during two current acquisition phases in order to do not disturb the voltage stored on C_{IN}. The sharing between C_{IN} and C_{REF} is ensured by an analog switch (N5, P5) controlled by the signal *SHARE* (active high).

Comparator block: The comparator block is designed with a StrongARM comparator followed by an RS latch. This block compares the two input voltages V_{CIN} and V_{CREF} to generate the digital output. This comparator works in two distinct phases. In the first phase, all the internal nodes of the structure are pre-charged to V_{DD1} through P8 and P9 when the signal *SA_EN* is grounded. During a second phase (signal $SA_EN = $ '1'), the pre-charge transistors are inhibited and the foot transistor is activated. Depending on the voltages V_{CIN} and V_{CREF} the StrongARM internal latch capture either a '0' or a '1'. This digital output, available on $OUT+$ and its complement *OUT-*, is then memorized in the RS latch.

3.2 Functional Validation

The proposed solution has been designed using a 28 nm FDSOI technology from STMicroelectronics, using two different supply voltages: low V_{DD1} equal to 1.0 V and middle voltage V_{DD2} equal to 5.5 V.

Figure 4 illustrates the self-reference generation followed by a read operation on an HRS cell and a read operation on an LRS cell. The self-reference generation takes three phases, whereas any successive read operations take two phases each. Please note, that to ease the representation all addressing changes, row selection, and column multiplexer activation, have been set here to 1 ns as for the sense circuit internal signal change. Of course, addressing timing varies accordingly to the array size and the memory controller feature, when the sense amplifier is embedded in a full memory chip. It is also important to note that; even if the reference generation principle remains similar to the one presented in Sect. 2, we proceed with capacitor discharge and not charge to minimize current copy circuitry.

Self-reference generation: During the 1st phase, the sense amplifier is disconnected from the memory array, accordingly the signal *PD* is activated and the reset signals (RST_{IN} and RST_{REF}) are activated with a low value to charge both capacitors to V_{DD1}, doing so both capacitor voltages are initialized and $V_{IN} = V_{REF} = V_{DD1}$. Please note that the signal *PD* is activated, whenever the sense circuit is disconnected from the array. After this 1st phase, the self-reference generation process starts with the selection of first the LRS cell reference and after with the selection of the HRS cell reference, during this complete process, the signal *SHARE* is activated, thus the discharge occurs simultaneously on both C_{IN} and C_{REF}. With this strategy, the charge sharing between both capacitors is realized during the acquisition. Thus, during the 2nd phase, the sense amplifier is connected to the memory array (*PD* is disabled) and both capacitors are

discharged following (5):

$$V_{IN} = V_{REF} = V_{DD1} - \frac{(I_{LRS} + I_{sneak}) * T}{2.C} \tag{5}$$

It is also important to notice that since the read current I_{LRS} plus the sneak-path current *Isneak* are absorbed by the structure, the potential V_M rises and has to be added to the regulated voltages *V* and *V/2*. After the second phase, the sense is first disconnected from the array, the HRS cell reference is addressed, and when the signals are stabilized in the memory array, the sense amplifier is again connected, here also with the *SHARE* signal activated. During this 3rd phase, here also with regulated loop activated, both capacitors are again discharged, thus the resulting voltages on the capacitors can be expressed following (6):

$$V_{IN} = V_{REF} = V_{DD1} - \frac{(I_{LRS} + I_{HRS} + 2.I_{sneak}) * T}{2.C} \tag{6}$$

This process, similarly to the principle described in Sect. 2, creates a reference voltage image of the mean of the I_{LRS} and I_{HRS} including the sneak path current of the acceded column I_{sneak}. It is interesting to note that the self-reference generation takes three phases, after that, only the input capacitor will have to be charged to V_{DD1} and discharge accordingly to the state of the cell to be read, in two phases. Another advantage of this self-referencing scheme is that after a reference generation and until the leakage current of the MOS (P4, P5, N7, and N5) degrades the voltage reference V_{REF}, numerous reading phases can be performed on the cells of the same column in burst mode, before refreshing the reference voltage.

Read operation: Before any read operation, it is mandatory to disable the *SHARE* signal and to reset the input capacitor by activating the RST_{IN} signal. Doing so during the *1st phase* of a read operation the voltage V_{IN} is again initialized to V_{DD1}. In the *2nd phase* of the read operation, the sense amplifier is connected to the memory array and the input capacitor is discharged by the read current, accordingly to the state of the addressed cell, while considering the sneak path current I_{sneak}. Depending on the state of the addressed cell, the voltage V_{IN} is above (HRS) or below (LRS) the voltage reference V_{REF}. The comparator is then activated latching the output on the two internal nodes *OUT* + and *OUT*-. Please note, that the regulation process is also active during the read operation *2nd phase*.

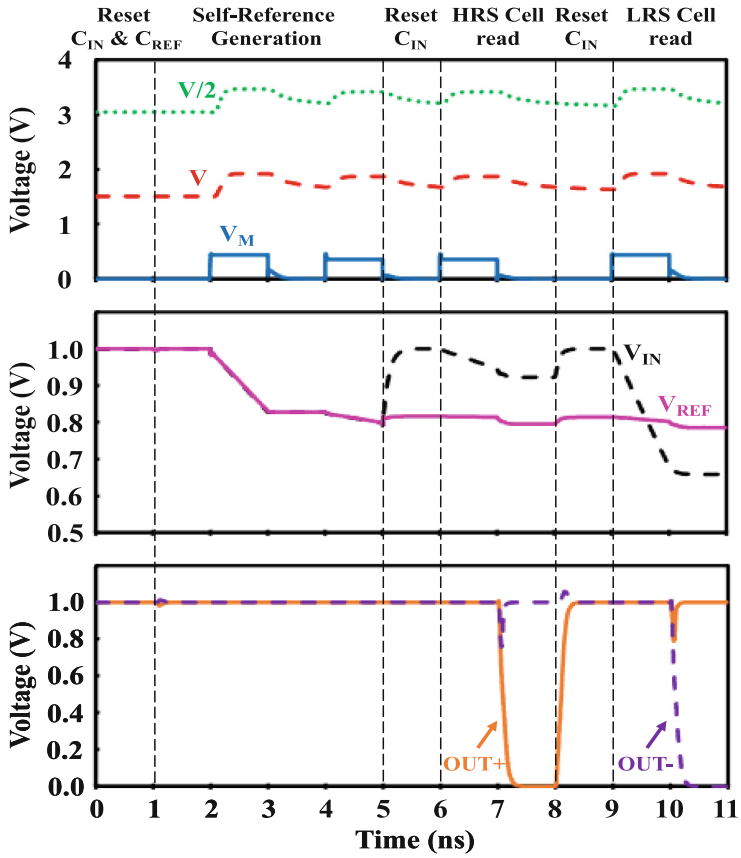
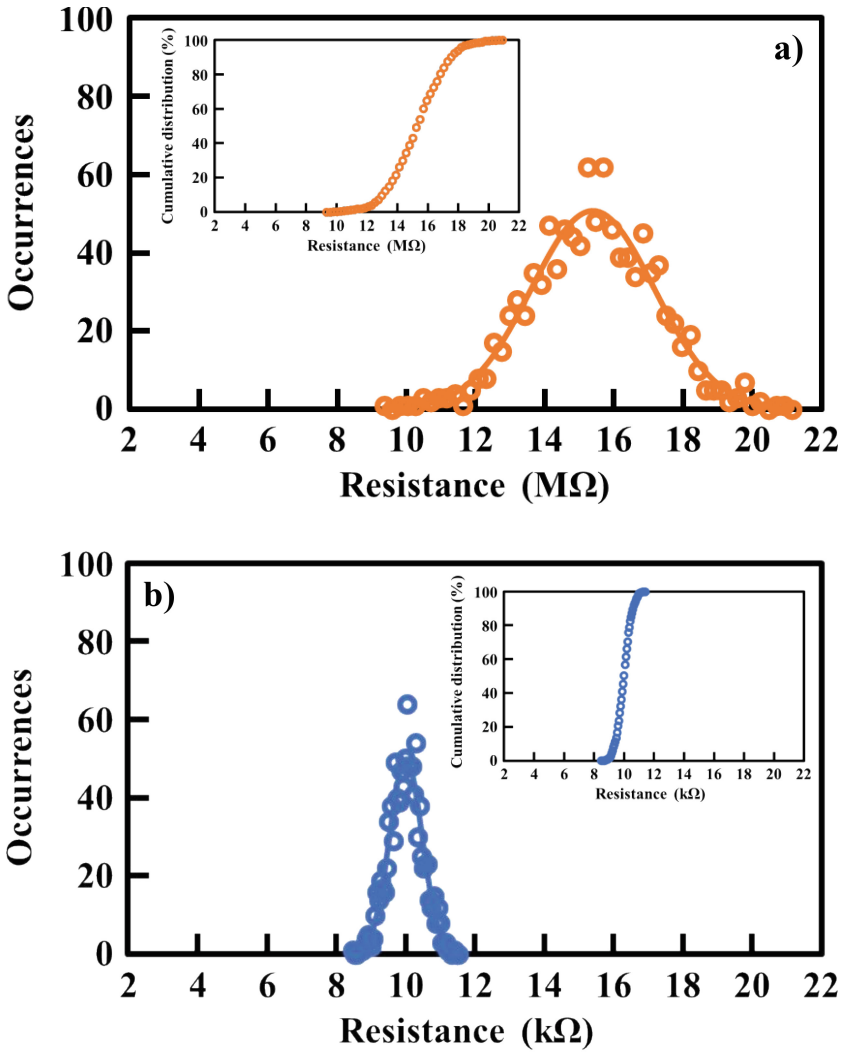


Fig. 4. Simulation of the proposed sense operation, with the self-reference generation (Reset both capacitors & reference generation), followed by the sensing of a cell in a HRS (reset in and read) $V_{IN} > V_{REF}$ and $OUT+ = 0$ and respectively of a LRS cell (reset in and read) $V_{IN} < V_{REF}$ and $OUT+ = 1.0$ V. Regulated signal are also represented during all phases.

4 Sense Amplifier Validation

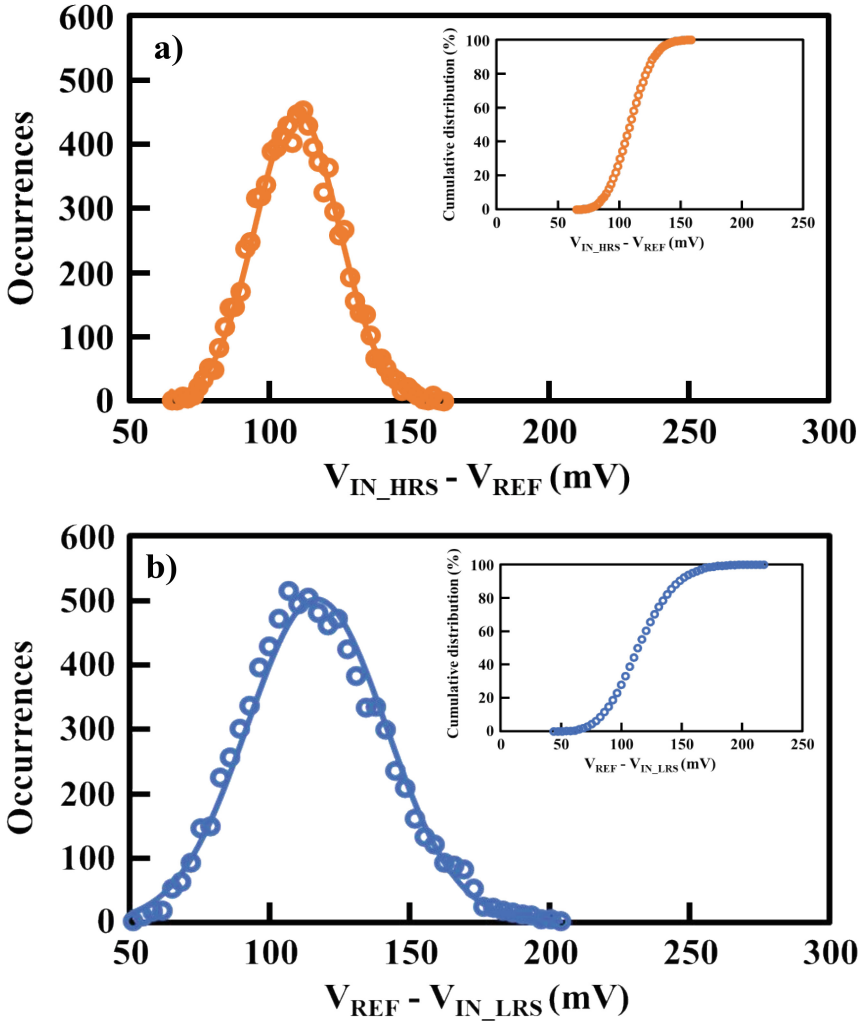
4.1 Sense Robustness Versus Variability

The sizing of our new sense amplifier is defined to target, 10 μA of sneak path current, corresponding to the OTS characteristics reported in [29] and considering a 1Mb array. The simulation timings are the ones presented in Fig. 4. First of all, the energy consumption of the sense amplifier has been extracted from simulations in nominal case, per block and per operation (self-reference generation, HRS, and LRS cell read), as shown in Table 1. As expected, since a large current is involved during reference generation and LRS read, these operations are the most consuming. The regulation loop is the main contributor, whereas the consumption of the two other blocks remains below the tens of fJ.



	Median (Ω)	σ (Ω)	Min (Ω)	Max (Ω)
HRS	$15.3 \cdot 10^6$	$1.8 \cdot 10^6$	$9.3 \cdot 10^6$	$20.9 \cdot 10^6$
LRS	$9.9 \cdot 10^3$	$0.47 \cdot 10^3$	$8.5 \cdot 10^3$	$11.4 \cdot 10^3$

Fig. 5. Equivalent resistance distribution and gaussian fit, used to simulate OTS and PCM variability with (a) OTS in off state during the read operation of a PCM in HRS state and, (b) OTS in on state during the read operation of a PCM in LRS state



	Median (mV)	σ (mV)	Min (mV)	Max (mV)
V_{IN_HRS} - V_{REF}	109	14.9	65	158
V_{REF} - V_{IN_LRS}	115	25	44	218

Fig. 6. Margin window distribution including gaussian fit, with (a) V_{IN_HRS} - V_{REF} for a read operation on a PCM HRS and (b) V_{REF} - V_{IN_LRS} for a read operation on a PCM LRS.

Then, to analyze the robustness of our sense solution, we first run an extensive set of simulations to take into account Process – Voltage – Temperature variations. Voltage variations are classically set to –10%, nominal, and + 10% of the *VDD1* defining 3 corner cases: 0.9 V, 1 V, and 1.1 V. The operating temperature variations are also defined with 3 corner cases: –55° C, 27° C, and 125° C. So, the validation of our sense solution

Table 1. Sense amplifier energy consumption

Blocks	Operations		
	Ref. Generation	HRS cell read	LRS cell read
Regulation	1.465 *pJ*	384 *fJ*	1.28 *pJ*
Capacitors	16.6 *fJ*	1.05 *fJ*	15.2 *fJ*
Comparator	0.052 *fJ*	0.3 *fJ*	*0.68 fJ*
Total	1.48 *pJ*	385.4 *fJ*	1.3 *pJ*

is performed against this set of 9 corner cases. For the process variations, we consider global as well as the local source of variability at –3σ/ + 3σ, including mismatch on the typical process corner, considering the implementation of common centroid and inter-digitized layout in order to reduce the mismatch between capacitor and StrongArm comparator. For all simulated voltage and temperature corners, 1000 runs are performed to take into account the process variations. Regarding the OTS and PCM variability [30], we have extracted dispersion reported in [29] for the OTS and in [31] for the PCM respectively. From these extractions and knowing that during a read operation on a PCM in LRS with OTS-on and a PCM in HRS with OTS-off, we have considered a Gaussian distribution whose mean value is 9.93 kΩ and standard deviation is equal to 470 Ω and another Gaussian distribution whose mean value is 15 MΩ and standard deviation is equal to 1.78 MΩ, respectively (Fig. 5).

Figure 6.a reports the margin window ($V_{IN} - V_{REF}$) between the input capacitor voltage V_{IN} and the reference capacitor voltage V_{REF}, considering our 9 Voltage-Temperature corners and with 1000 Monte Carlo runs for each corner, in the case of a read operation on a PCM HRS (noted V_{IN_HRS}). Respectively, Fig. 6b reports the margin window ($V_{REF} - V_{IN}$) in the same conditions, but for a read operation on a PCM LRS (noted V_{IN_LRS}). Both margin windows exhibit a positive value of 65 mV and 44 mV, validating the robustness of our sense solution. This robustness strongly relies on the auto-reference generation, compensating even worst-case variations.

4.2 Sense Robustness Versus OTS Characteristics and Array Size

Keeping the same sizing and timing constraints, the proposed sense solution is evaluated versus different levels of sneak-path current to assess the robustness of the design with different OTS selector characteristics and different array sizes. The evaluated conditions are reported in Table 2 with for each pair of OTS selector characteristic/array size, the corresponding theoretical sneak-path current.

Please note, that sneak-path currents above 1 mA are discarded as non-realistic values in memory chip design-space exploration (noted NA in Table 2). The sneak path current is calculated as follow:

$$\mathrm{I_{sneak}} = \sum_{row=0}^{n-1} I_{sneak[i]} \tag{7}$$

with *Isneak[i]* a single cell sneak-current when the OTS is biased at *V/2* and *n* is the number of rows in the array.

Table 2. Sneak Path Current I_{SNEAK}

$I_{sneak[i]}$ (A) at V/2	n×n array size			
	10 kb	1 Mb	100 Mb	3.2 Gb
OTS from [20]: 10 pA	10 nA	100 nA	1μ A	6 μA
OTS from [28]: 1 nA	1 μA	10 μA	100 μA	600 μA
OTS from [21]: 50 nA	50 μA	500 μA	NA	NA

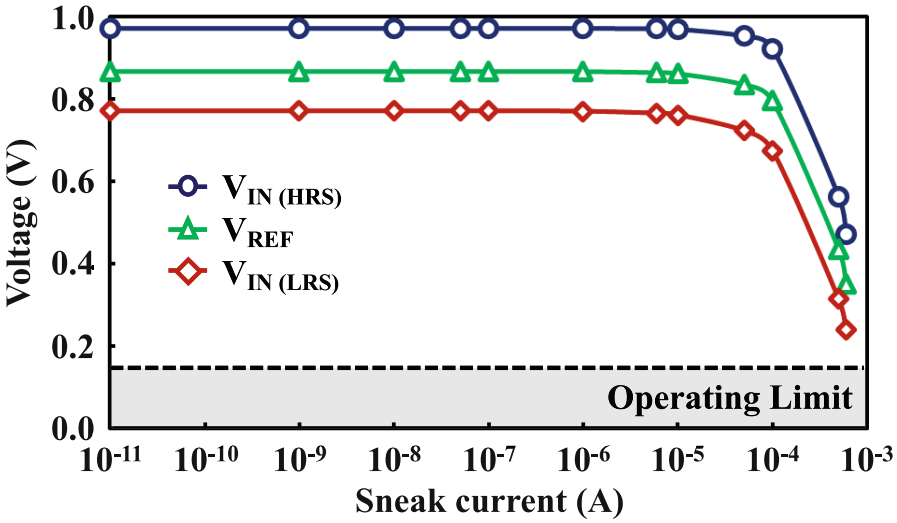


Fig. 7. Input voltage V_{IN} (corresponding to the read of a PCM HRS and respectively a PCM LRS) and voltage reference V_{REF} evolution versus the identified conditions given Table 2 for various OTS selector characteristic and array size.

The simulation results for a typical case are reported in Fig. 7 with the *VIN* voltage for a read operation on a PCM in HRS (noted V_{IN_HRS}), respectively on a PCM in LRS (noted V_{IN_LRS}), and the V_{REF} voltage versus the sneak-path current given Table 2. One can first notice that the auto-reference generation technique is efficient for a broad range of sneak-path current. Actually, for sneak-path current ranging up to 600 μA, the reference voltage level is well balanced in between the LRS voltage level and the HRS voltage level. However, due to the sizing of the capacitor block (Fig. 3.b), when the input current overcomes a given limit (around a few hundreds of μA), one can observe two effects. The first one is a too large potential capacitor-discharge, with possibly V_{IN} and V_{REF} close to the NMOS threshold voltages (noted as operating limit in Fig. 7), with a direct impact on the comparator response time and an over-sensibility to mismatch. The second effect is a nonlinear discharge of the capacitor due to the polarization regime change of the transistor N4, however since the reference is auto-generated, this effect remains partially compensated. Thus depending on selector characteristics as well as array size, careful

sizing of the capacitors C_{IN} and C_{REF}. Has to be adopted. Finally, it is worth noting, that using body bias options, the threshold of the MOS at the inputs of the comparator can be trimmed to enhance the sense robustness to large sneak-path current for a given sizing.

	Global & Local variations with Mismatch (1000 Monte Carlos runs)									Process
	0.9 V			1.0 V			1.1 V			Voltage
sneak current	-55 °C	27 °C	125 °C	-55 °C	27 °C	125 °C	-55 °C	27 °C	125 °C	Temperature
1 nA	0	0	0	0	0	0	0	0	0	
1 µA	0	0	0	0	0	0	0	0	0	
10 µA	0	0	0	0	0	0	0	0	0	
100 µA	0	0	0	0	0	0	0	0	0	
200 µA	0	0	0	0	0	0	0	0	0	
400 µA	17	4	1,6	1,2	0,3	0	0	0	0	
600 µA	98	66	71	72	62	15	39	8	1	

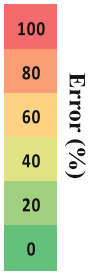


Fig. 8. Fail results (shmoo plot) of the PVT simulation of the proposed sensing circuit for various sneak-path currents.

4.3 Overall Sense Robustness

Finally, our sense amplifier is benchmarked on various sneak-path current for the 9 predefined corners with Monte Carlo simulations (1000 runs) to include process variations. Figure 8 presents a shmoo plot of the pass/fail sensing results considering the corners cases and the process variation versus different sneak path current values. The first errors occur for a sneak-path current of 400 µA for the most severe voltage corner case. The errors are mainly due to the low voltage corner (0.9 V) since this corner reduces the dynamic across the capacitor, leading to 17% of reading errors. For extreme sneak-path current the solution exhibits errors, whatever the corner, meaning that the C_{IN} and C_{REF} sizing is not sufficient to deal with the extreme amount of sneak-path current. Besides, for this high sneak path, the errors are mainly due to voltage corner (0.9 V) together with low temperature corner. For all other cases representing a large range of sneak-currents including the targeted one (10 µA), due to the auto-reference generation, our new sensing solution has clearly demonstrated its robustness.

5 Sense Amplifier - Layout Evaluation

Figure 9 represents the full layout of the complete solution, including two blocks designed with thin transistors, namely the capacitor block and the comparator block, and a middle voltage block for regulation, designed with thick transistors. The overall area is 28.1 µm by 65.2 µm, whereas if we do not consider the middle voltage regulation block, the area is limited to 7.78 µm by 9.67 µm.

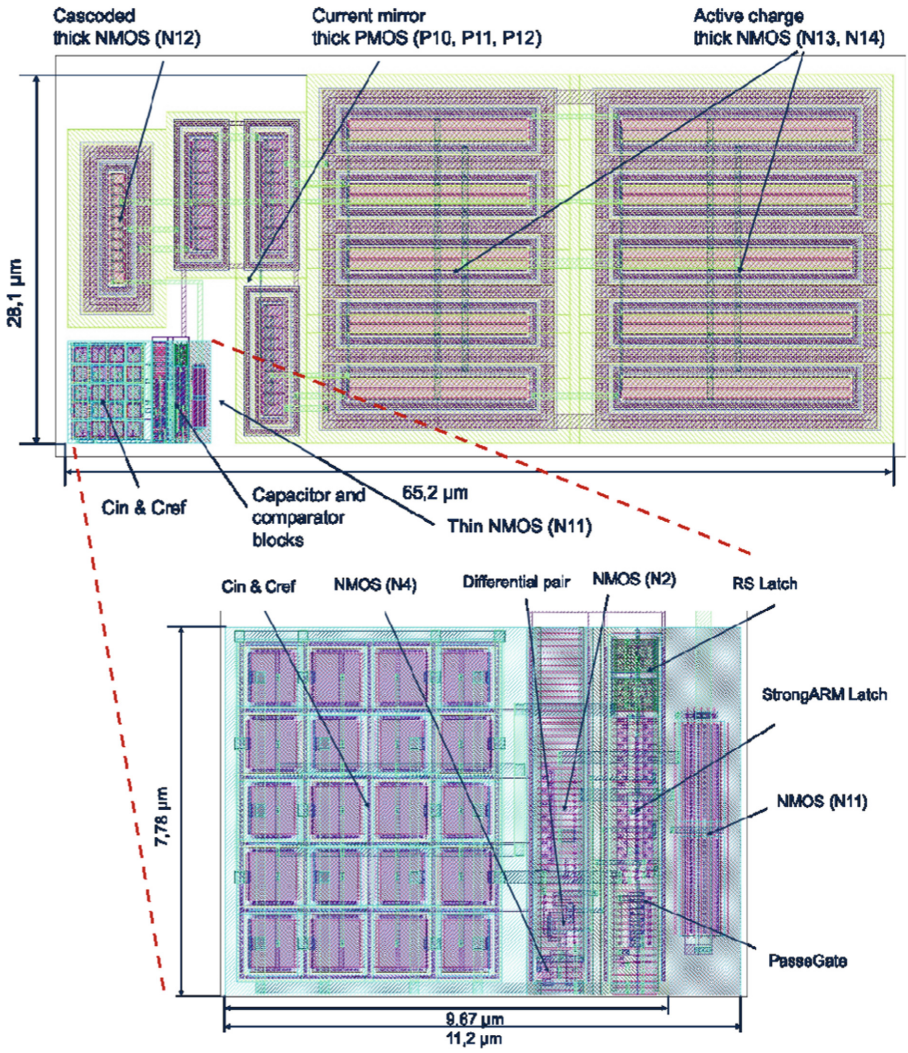


Fig. 9. Layout of the proposed sense solution, with a detailed view of the capacitor and comparator blocks. The regulation block dominates the overall area due to required fast response time and middle voltage devices.

Thus, it appears that the regulation block dominates the area of the solution, with 94.5% of the complete area. The sizing of the regulation block is constrained by middle voltage compatibility, together with important output load and fast response time (ns range). The remaining 5.5% are mainly dominated by CIN and CREF sizing, that account for 4.6% of the total area. The layout of CIN and CREF is realized with a common-centroid approach since both capacitors have to be strictly equivalent [32] to avoid any offset at the input of the comparator.

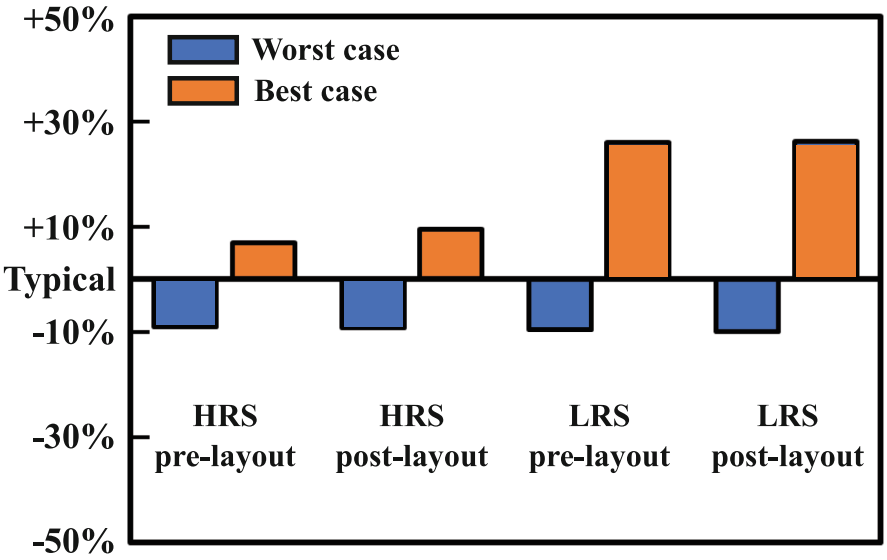


Fig. 10. Post-Layout simulation results for the best and worst corner-cases, normalized to the typical corner-case for ideal scheme (pre-layout) and extracted netlist (post-layout), when reading a LRS cell and a HRS cell

To further assess the robustness of the proposed sensing solution, post-layout simulations are realized. The sizing of the entire circuit is performed to be fully compliant with a leakage current of 10 µA. Thus, post-layout simulations have been performed for such a current, considering three corner-cases as reported Table 3.

Table 3. Post-Layout simulation for a leakage current of 10 µA – corner-cases definition

Corner-cases	Simulation conditions		
	Process	Temperature (°C)	Voltage (V)
Worst	TT	-55	0.9
Typical	TT	27	1.0
Best	TT	125	1.1

The simulation results are given for the three corner-cases, comparing the ideal (pre-layout) and post-layout simulations. The Fig. 10 presents the percentage of variation, normalized versus the typical case, for the worst and best cases, considering ideal and post-layout simulation results. The results are expressed considering the read margin variation in percent (difference between V_{IN} and V_{REF}) for a read operation on a LRS cell and respectively on a HRS cell. As depicted Fig. 10, the percent of read margin reduction is around 9% considering the worst corner-case, whatever the resistance state (HRS or LRS) for ideal and post-layout simulation. For the best corner-case, here also

ideal and post-layout simulation results show the same trend with an increase of the read margin versus the typical case, of 7% (ideal) and 9% (post-layout) considering the HRS cell and of 26% for both considering the LRS cell. To summarize, similar results are obtained for ideal and post-layout simulation, assessing the robustness of our layouted sensing solution versus corner cases study.

6 Conclusion

In this work, we propose for the first time a sense amplifier suitable for OTS selector and PCM memory. The main advantage of our sensing solution, is to generate, just when necessary, a self-reference that takes into account the sneak-path current. Thanks to this self-reference generation, the leakage current during the read operation of a 1S1R cell is fully compensated. Moreover, we also introduce a regulation loop to apply a constant reading voltage on the selected cell whatever the sensing current. It is worth to note that this regulation loop is the main contributor (94,5%) of the overall area. Finally, we have demonstrated the exceptional robustness of our approach through extensive corner cases and Monte-Carlo simulations, including post-layout simulations, and thus for a broad range of sneak path current, corresponding to various OTS features and/or memory array size. This new sensing solution opens the way to a robust OTS selector and PCM memory reading operation in high-end microcontroller products.

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