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Ultra-low Voltage Circuit Techniques for Energy Harvesting

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Rafael Luciano Radin would like to dedicate this work to his parents.
Marcio Bender Machado would like to dedicate this work to his wife and son.

Preface

The Internet of Things (IoT) is a pervasive technology that connects everyday objects with many applications in human life. IoT has been enabled by advances in microelectronics, which have led to a remarkable reduction in both the size and consumption of computational devices. The multitude of new IoT applications to promote quality of life and health and provide entertainment is closely accompanied by an ever-growing number of connected objects, where energy harvesting has become a pivotal solution to power such devices. Energy harvesting is an indispensable tool for applications such as the continuous monitoring of a patient's health and the powering of implantable biomedical devices.

The demand for miniaturization and energy autonomy of connected devices imposes a challenge in which the power consumption of the devices plays an essential role. Energy autonomy is achieved through the harvesting of ambient energy, which is available in different forms, including heat, illumination, and radiofrequency signals. Transducers such as thermoelectric generators, photovoltaic cells, and antennas are commonly employed to convert the ambient energy into usable electric signals. However, due to the low levels of ambient power, typically in the range of microwatts to milliwatts, the output voltage provided by these transducers varies between tens to hundreds of millivolts, and voltage boosting is needed to power connected devices.

The voltage converters employed to perform step-up conversion in an energy harvesting interface need to cope with low input voltages provided by the transducers, leading to challenging design trade-offs to deal with both efficient conversion and startup from ultra-low voltages. Therefore, to enable the further development of energy harvesting converters and related IoT applications, the low voltage capabilities of a low-cost technology such as CMOS should be fully exploited. In this regard, models suitable for CMOS circuits operating with ultra-low voltages are indispensable.

In the past decade, low-voltage energy harvesting has been the main research theme of several groups worldwide. However, design techniques directed toward extremely low voltages are still lacking. This book intends to fill this gap, providing

IC designers with techniques appropriate for realizing the main building blocks of energy harvesters, such as oscillators, rectifiers, and inductor-based converters. Herein, we address the design of energy harvesters operating from ultra-low voltages, enabling autonomous operation of connected devices driven by human or ambient energy.

This book is organized as follows. Chapter 1 presents the fundamental concepts of ultra-low-voltage energy harvesting. A brief introduction to energy harvesting approaches and the models for some standard transducers are provided. Next, an overview of biomedical and IoT applications is presented, followed by a review of state-of-the-art energy harvesting converters. At the end of the chapter, a physics-based MOSFET model to help with the design of ultra-low-voltage converters is provided.

Chapter 2 addresses the analysis, design, and realization of oscillators that operate with reduced supply voltage. Special attention is given to LC oscillators, such as the cross-coupled oscillator, the enhanced-swing cross-coupled oscillator, and the enhanced-swing Colpitts oscillator. These oscillators can operate from supply voltages well below 100 mV while providing oscillation amplitudes higher than the supply rails. Design examples and experimental results are presented to validate the theoretical analysis.

Chapter 3 describes the analysis of rectifier circuits valid for ultra-low-voltage (ULV) operation. Expressions for the output voltage, power conversion efficiency, and input resistance for the Dickson charge pump and the voltage multiplier are given in terms of the diode parameters and the load current.

Design methodologies and experimental results for voltage converters employing rectifier circuits, namely the Dickson charge pump and the voltage multiplier, are presented in Chap. 4. Both DC-DC converters based on ultra-low-voltage oscillators and rectifiers and RF-DC converters are explored. Several experiments with ultra-low-voltage oscillators and rectifiers show their feasibility for energy harvesting.

The analysis and modeling of inductive boost converters for ultra-low-voltage operation are detailed in Chap. 5. Design parameters for the maximization of the power extraction and conversion efficiency are presented for the employment of the boost converter in typical energy harvesting applications. After an analysis of the converter losses, the boost switches are sized to maximize the power efficiency of the converter.

Chapter 6 addresses the design, implementation, and measurements of a DC-DC voltage converter for energy harvesting applications. The converter prototype starts up from input voltages as low as 11 mV. After its initialization, the converter can operate with input voltages in the range of 7.3–140 mV. The prototype presents end-to-end efficiencies higher than 50% for input voltages above 10.5 mV and peak end-to-end efficiency of 85% at 140 mV.

This book can be used as a reference for analog IC designers and to both undergraduate and graduate students. It can act as supplementary material in undergraduate and graduate analog electronics courses, requiring a background on basic electronics and semiconductor devices.

We would like to thank all those who contributed to producing this book. In particular, we want to express our gratitude to our former students and colleagues Lucas Pereira Luiz, Franciele Nörnberg, Arun Kumar Sinha, Lucas Goulart de Carli, Daniel Lucas Novack, Pedro Fleury, and Adilson Jair Cardoso, who made important contributions to the research on ultra-low-voltage energy harvesting. We also thank Laurent Mouden for support with the prototypes. We wish to acknowledge CNPq and CAPES, Brazilian agencies for scientific development, for their research support and CMC microsystems and MOSIS for the integration of the prototypes. We acknowledge Franciele Nörnberg for the source code of the optimization routine detailed in Sect. 4.3.2 as well as for the production of Figs. 4.16 and 4.17. Last but not least, we would like to acknowledge Siobhan Wiese for the outstanding revision of the manuscript.

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Chapter 1
Introduction to Ultra-Low-Voltage Energy Harvesting

1.1 Introduction

During the past century, advances in electronics have allowed the development of new consumer products, which have had a significant impact on the development of modern society as we know it today. Communication mechanisms, forms of entertainment, and the sharing of knowledge have been significantly modified with the availability of broadcast systems, notably radio, television, and the Internet. The introduction of several new types of biomedical equipment has enabled new approaches to diagnosis and treatments, contributing to the fast development of medicine. The industry has also evolved with the adoption of control systems and robotics, which allow faster production and the development of more complex products.

Similarly, more recent developments in electronics continue to alter diverse aspects of human life, with new applications that lead to the ever-growing computational capacity of devices. In the Internet-of-Things (IoT) scenario, connected devices, such as smart sensors, allow the acquisition of large amounts of data, which can be processed using machine learning techniques to perform more complex tasks [1].

The acquisition of data and intelligent decision-making capabilities have enabled several new approaches in the development of smart cities, such as the deployment of a smart grid, which can reduce energy consumption and allow distributed generation, intelligent management of waste, pollution monitoring, management of traffic congestion, smart parking, lighting control, etc. [2]. Homes and buildings can also benefit from IoT devices, which can help with reducing energy consumption, expanding entertainment options and quality-of-life applications, promoting intelligent automation, etc. Furthermore, the human body has a strong potential for several

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IoT applications to promote better life quality and health, such as aids for sports training, wearable health-monitoring devices, ambient assisted living, and real-time streaming [3].

With several applications in everyday life, the number of connected devices has been steadily increasing, and by 2010, it had already surpassed the human population [4]. An essential requirement for the connected devices is an autonomous energy supply for operation, which allows the device to be independent of any wiring needs or batteries, decreasing both maintenance needs and chemical waste generation and increasing device portability. In this context, energy harvesting has become a necessary solution to allow connected devices to better fit the requirements of uninterrupted autonomous operation [5], being a feasible solution for powering sensor nodes [6] while meeting the requirements of performance and lifetime for such devices.

Although the available power (P_{AV}) harvested by compact transducers is generally low, of the order of mW or less, it enables several autonomous low-power applications. From an application perspective, appropriate low-power design is essential to maximize the use of such restricted power levels. Circuit techniques such as V_{DD} scaling and power cycling are essential strategies to reduce power consumption and are suitable for many applications that do not require a fast and "always-on" response.

Along with the available power of common energy harvesters being low, the voltage provided by them is also low, typically being of the order of hundreds or tens of mV. Because, in general, this voltage is not sufficient to supply electronic circuits of current technologies, a step-up (boost) voltage converter is required to power the application circuit.

From the step-up converter design perspective, the ultra-low-power (ULP) and ultra-low-voltage (ULV) levels of energy-harvesting transducers impose challenging design constraints. To minimize the impact of such constraints, we have analyzed and modeled different types of voltage converters using physics-based MOSFET and diode models, which enable appropriate designs to be obtained for ULV converters.

1.2 Common Methods for Low-Power Energy Harvesting

In the energy scavenging scenario, the ambient energy can be exploited as a source to power electronic devices. Figure 1.1 shows a simplified energy-harvesting interface, where a transducer is employed to convert the ambient energy to electricity, enabling the powering of a load. Due to the ULV levels generated by the transducers, a converter is commonly employed between the transducer and the load to provide step-up voltage conversion and stabilization of the output voltage.

The most common sources for energy harvesting, the amount of ambient power, and the power typically collected by the transducers are detailed in Table 1.1. As can be seen, the harvested power is generally a very small fraction of the source power

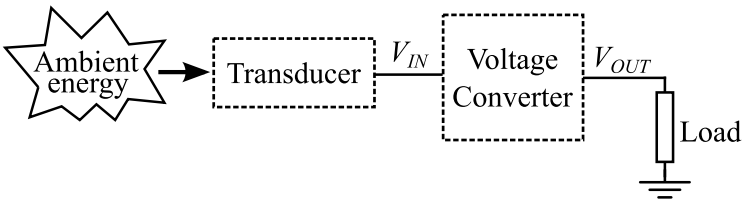

Fig. 1.1 A simplified representation of an energy-harvesting interface

Table 1.1 Energy-harvesting approaches and associated power levels [7]

Source	Source power	Harvested power
Ambient light—indoor	0.1 mW/cm^2	10 μW/cm^2
Ambient light—outdoor	100 mW/cm^2	10 mW/cm^2
Vibration/motion—human	0.5 mW/cm^2	4 μW/cm^2
Thermal energy—human	20 mW/cm^2	30 μW/cm^2
Radiofrequency	0.3 μW/cm^2	0.1 μW/cm^2

due to the low efficiency of the transducer. In this section, we analyze the most common methods for energy harvesting and provide information on the transducers used in each approach. The equivalent electric circuit presented for each type of transducer aids in the search for different techniques for maximum power point tracking (MPPT).

1.2.1 Thermal Energy Harvesting

Thermal energy harvesting is a feasible approach to power on-body devices using human thermal energy. A thermoelectric generator (TEG) is employed to convert a temperature difference into electricity through a physical process known as the Seebeck effect, which occurs in both semiconductor and conductor materials. The basic structure of a TEG is a thermocouple (Fig. 1.2), which is comprised of two different semiconductor materials, a p-type material with a positive Seebeck coefficient (S_P) and an n-type material with a negative Seebeck coefficient (S_N). To realize a TEG, the thermocouples are joined by an electrically conductive material and sandwiched between two electrically insulated and thermally conductive plates, which form the cold and hot sides of the device [8].

Once a thermal gradient is applied between the hot and cold sides of the device, diffusion of charge carriers from the hot side (higher thermal energy) to the cold side (lower thermal energy) occurs, generating an electric field due to the gradient of charge carriers. Once the circuit is closed, the flow of electrical current is established.

The open-circuit voltage generated by a thermocouple (V_{TC}), which is proportional to the temperature difference between plates, is given by

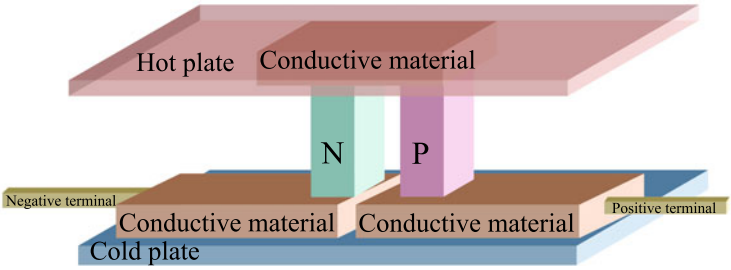

Fig. 1.2 The basic structure of a thermocouple

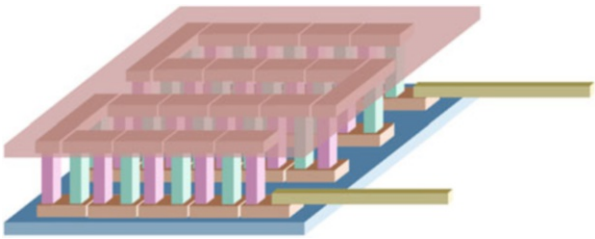

Fig. 1.3 Common TEG construction using thermocouples in series

$$V_{TC} = S\Delta T = (S_P - S_N)\Delta T. \tag{1.1}$$

Due to the low value of the Seebeck coefficient (S), TEGs are generally built with a series of thermocouples to increase the voltage (Fig. 1.3).

Although higher voltages can be achieved with the series connection of thermocouples, the increase in the number of devices connected in series also causes the electrical resistance of the TEG and the total TEG area to increase. Standard commercial TEG devices of a few cm^2 (Tellurex, Kryotherm, Marlow, and TEGPro) deliver around 30–60 mV/K under the open-load condition and have a resistance of around 1 to 10 Ω. More recent thin-film technologies achieve a higher Seebeck coefficient for the same TEG area, although the electrical resistance is also increased to the range of some hundreds of ohms.

The electrical model of a TEG is comprised of a voltage source in series with a resistance, as shown in Fig. 1.4. To maximize the power that can be extracted from a TEG, the input impedance of the converter should be matched to the internal resistance of the TEG (R_S). Under this condition, the voltage obtained at the TEG terminals is one-half of the TEG open-circuit voltage (V_S), as represented in Fig. 1.4. Therefore, the power delivered to the converter (P_{IN}) equals the available power, which is given by

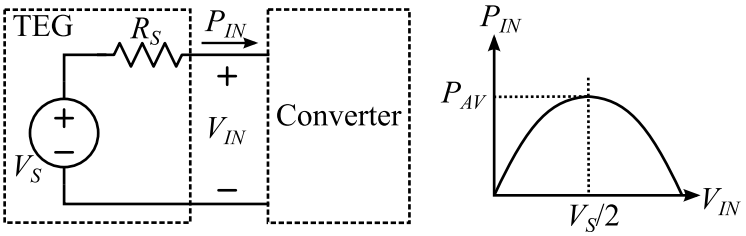

Fig. 1.4 The equivalent electrical circuit of a TEG connected to a step-up voltage converter and the condition for maximizing the extraction of the available power

Fig. 1.5 Equivalent thermal circuit of a TEG on the human body

$$P_{AV} = \frac{V_S^2}{4R_S}. \tag{1.2}$$

1.2.1.1 Harvesting Thermal Energy from the Human Body

The voltage level of each thermocouple is a function of the temperature gradient between the hot and cold sides of the device (1.1). When scavenging thermal energy from the human body, this gradient is always lower than the difference between the ambient temperature and the human body temperature. As represented in the thermal circuit of Fig. 1.5 [9], the temperature gradient across the TEG is limited by the thermal resistance between the human body and the TEG as well as between the TEG and the air. The air resistance is dependent on the air flow, which is affected by wind conditions, body movement, etc., while the resistance of the human body can be reduced by choosing contact areas with lower thermal resistance, such as the chest, head, and wrist [10]. As demonstrated in [11], the integration of TEGs with clothes is also a feasible way to harvest energy from the human body.

1.2.2 Photovoltaic Energy Harvesting

Photovoltaic cells (Fig. 1.6) are p-n junctions that convert light radiation into electricity. Being built from a well-developed technology, photovoltaic cells are widely used as power supplies for many applications.

Typical values of harvested power densities of photovoltaic cells range from 10 mW/cm^2 outdoors to values of the order of 10 μW/cm^2 indoors [7]. Despite the reduced harvested power under low illumination, its value is of interest for several

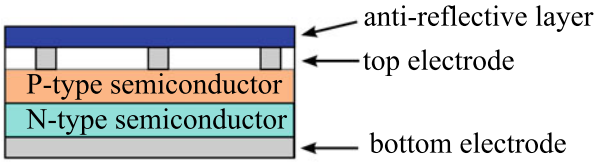

Fig. 1.6 Basic photovoltaic cell structure

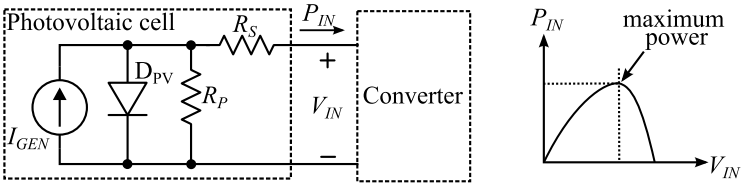

Fig. 1.7 The equivalent electrical circuit of a photovoltaic cell and the dependence of the converter input power on its input voltage [14]

ULP applications, such as sensor networks and biomedical circuits. An example of silicon-based small-area cells for a subcutaneous implant application presented in [12] operates with an efficiency of around 17%. In [13], photovoltaic cells implemented with different materials (GaAs, GaInP, and Si) were tested under low-irradiance conditions. Both GaAs and GaInP cells outperformed the more conventional Si-based photovoltaic cells. The highest measured conversion efficiency was close to 27% for the GaInP-based photovoltaic cells.

The equivalent electrical model of a photovoltaic cell is shown in Fig. 1.7 [14]. The current I_{GEN} is dependent on the light radiation. The resistances R_S and R_P model the ohmic losses and the internal leakage current, respectively, and the diode represents the p-n junction. Due to the nonlinear voltage-current relationship, an algorithm for MPPT is usually employed in the converter to maximize the extracted power.

1.2.3 Vibrational Energy Harvesting

Vibrational energy either from the human body or from the environment can be converted into electrical energy. Electrostatic, piezoelectric, and electromagnetic transducers are the most common transducer types used to harvest vibrational energy [7].

Piezoelectric transducers (Fig. 1.8) are available as several commercial products for the specific purpose of energy harvesting. These transducers are based on the piezoelectric effect, a property of some crystals and ceramics in which electrical charges are accumulated in response to an applied mechanical strain due to the change in the crystalline structure of the material.

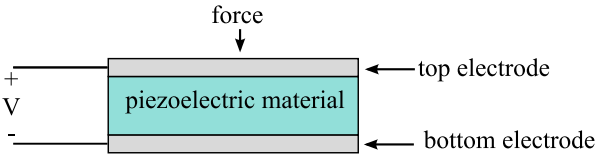

Fig. 1.8 Basic structure of a piezoelectric transducer

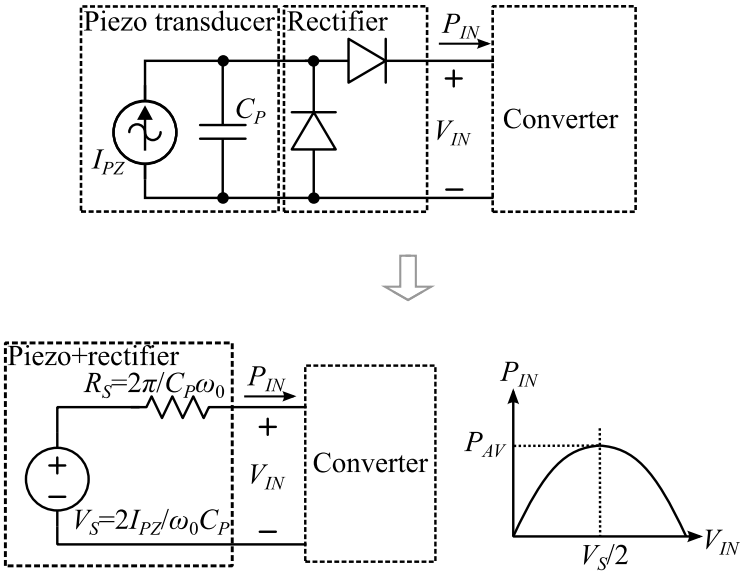

Fig. 1.9 The equivalent electric circuit of a piezoelectric transducer combined with a rectifier and the condition for extraction of the available power [14]

An equivalent electrical model of a piezoelectric transducer is shown in Fig. 1.9 [14], where I_{PZ} is the current generated when the piezoelectric material is submitted to a mechanical strain, and C_P models the capacitance between the electrodes. Assuming operation at the resonant frequency (ω_0), which is an intrinsic characteristic of the transducer, the piezoelectric transducer can be modeled by a voltage source and a series resistance, as in Fig. 1.9. Due to the nature of the vibration signals, the oscillatory output of the transducer is commonly connected to simple rectifier circuits, as shown in Fig. 1.9 [14].

1.2.4 Radiofrequency Energy Harvesting

The power density of radiofrequency (RF) signals is typically lower than that of other energy harvesters; however, it is still an attractive option, especially in densely populated areas, where wireless RF sources are widely available and can thus

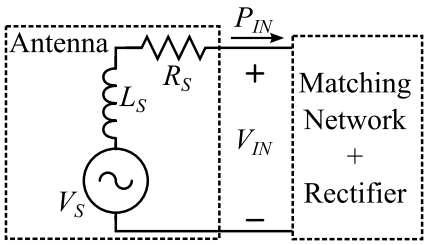

Fig. 1.10 The equivalent electrical circuit of an antenna connected to an RF/DC converter

support several autonomous applications. In such a scenario, RF energy harvesting could be used to recharge batteries in situations where a battery replacement would be impractical. RF signals from cellular networks, Wi-Fi, and other types of wireless networks can be captured by small form-factor antennas and further converted into a usable DC voltage by RF/DC converters, generally through a matching network and a rectifier [15–17].

The equivalent electrical circuit of an antenna is presented in Fig. 1.10, where V_S, R_S, and L_S are the open-circuit peak voltage, internal series resistance, and inductance of the antenna, respectively. The matching network is employed between the antenna and the rectifier to provide impedance matching and maximize the power transfer between the antenna and the rectifier. When the input impedance of the matching network equals the complex conjugate of the antenna impedance, the available power, given by

$$P_{AV} = \frac{V_S^2}{8R_S}, \tag{1.3}$$

is delivered to the input of the converter.

1.3 Ultra-low-voltage Energy-Harvesting Applications

Energy harvesting is a feasible technology to power sensor networks [18] and IoT devices for several biomedical and quality-of-life applications. Due to the low power typically harvested, appropriate design techniques and efficient communication protocols must be employed to operate the connected devices.

For the communication between on-body devices, protocol standards such as the IEEE 802.15.6 have been developed, allowing the deployment of short-range wireless body area networks (WBANs) [3], for which low power consumption is an essential requirement. Furthermore, for the operation of sensor networks, new communication standards, such as ZigBee with the Green Power feature, have been developed, targeting the use of harvesters as a power source.

Several recent papers report the powering of sensor nodes from energy scavengers. In [10], a complete sensor node solution powered from a TEG connected to a human wrist was able to measure and transmit data every 2 s, with an average power

consumption of 50–75 μW. A complete sensor node supplied by a photovoltaic cell is described in [19]. The complete prototype, designed with stacked integrated circuits and including the photovoltaic cell, occupies a total volume of only 1.0 mm^3.

Small sensor nodes allow several quality-of-life and biomedical applications. The circuits described in [20] are specifically designed to be implanted in the anterior chamber of the eye, enabling both the measurement of the eye pressure and wireless communication to send the measurement results. The circuits are designed to occupy a total volume of 1.5 mm^3, including a photovoltaic cell and a thin-film lithium battery. Targeting a subcutaneous implant, the system powered by the photovoltaic cell presented in [21] consists of a power management unit, a temperature sensor, a Bluetooth Low Energy (BLE) module, and a 7-mAh rechargeable battery. The long-term operation of the subcutaneous implant can be verified using ex-vivo experimental results. A wearable sensor node that measures body temperature and the heartbeat is described in [22]. The sensor node powered by a flexible photovoltaic transducer can perform autonomous 24-h operation. The sensor nodes use the BLE protocol for communication, enabling the implementation of an autonomous WBAN. In a study reported in [23], a body sensor node that acquires and transmits electrocardiogram, electromyogram, and electroencephalogram data was developed. The system is powered by a 30-mV input from a TEG and uses an RF kick-start.

Energy harvesting using ultrasound (US) [24, 25] and inductive links [26] is also a feasible approach for implantable devices, where an external source of energy is placed in a very close location to power the implantable device. A monolithic device that occupies a total volume of 0.065 mm^3 is reported in [24]. The device is powered by an external US probe and uses an on-chip piezoelectric transducer to harvest the ultrasound waves. The system is employed as a temperature sensor and to transmit temperature data through acoustic backscattering. The implantable system described in [25] uses a piezoelectric transducer to harvest energy from an external US transceiver. The same piezoelectric transducer is used for the US data uplink. The system is designed to measure pressure through the adoption of a resistive bridge pressure transducer and is comprised of an analog-to-digital converter, a finite-state machine, and a power-management unit.

1.4 Ultra-low-voltage Energy-Harvesting Converters

The voltage level generated by miniature transducers is low and varies widely with the power in the environment. Voltage converters between the transducer (antenna, thermoelectric generator, solar panel, etc.) and the device being powered are required to provide a stable and appropriate voltage level under several conditions of available power. Hence, voltage converters capable of operation with ULV inputs are needed to enable harvesting from the environment even when the available ambient energy is low, as is the case of thermoelectric generators (TEG) operating under low temperature gradients or weak radiofrequency signals captured by small antennas. The most relevant figures of merit for such converters are as follows:

- Input voltage range—A wide range of input voltages is required to provide a stable and adequate output voltage when the level of the ambient power oscillates.
- End-to-end efficiency—The converter should be designed to maximize the extraction of the available power and provide high conversion efficiency.
- Startup voltage—Low startup voltages allow the converter startup and power cycling at typical low levels of ambient power.
- Device size—A compact form factor using a minimum number of off-chip components and chip area is desirable, increasing device portability and reducing implementation costs.

The most common types of converters used to achieve voltage boosting in energy-harvesting interfaces are the switched-inductor and switched-capacitor converters.

1.4.1 Switched-Capacitor Converters

Switched-capacitor converters [27–31] can be fully integrated, with minimal area requirements, although the minimum input voltage for operation of this type of converter is high (100 mV in [27]). Also, the efficiency is low compared with switched-inductor converters, especially at low input voltages (only 33% at 100 mV [27]).

1.4.2 Switched-Inductor Converters

Switched-inductor converters are largely employed as an efficient means of DC-DC conversion in energy-harvesting interfaces [32–34]. This type of converter provides high end-to-end efficiency (90.8% reported in [35]), but it is generally comprised of an off-chip inductor and two off-chip capacitors, as will be explained in Chap. 5. Also, this type of converter cannot self-start at low input voltages, requiring auxiliary cold-starter circuits, which can be fully integrated, or rely on off-chip components of large values and high-quality factors (Q). A converter topology including a cold starter and a main converter is shown in Fig. 1.11.

1.4.2.1 On-Chip Startup Mechanisms

The startup voltages reported in [36, 37] are of the same order of magnitude achieved by switched-capacitor converters and are thus not appropriate when the aim is ULV startup. Several circuit techniques have been proposed for startup to find a trade-off between low-voltage startup and the device size and cost [38–41].

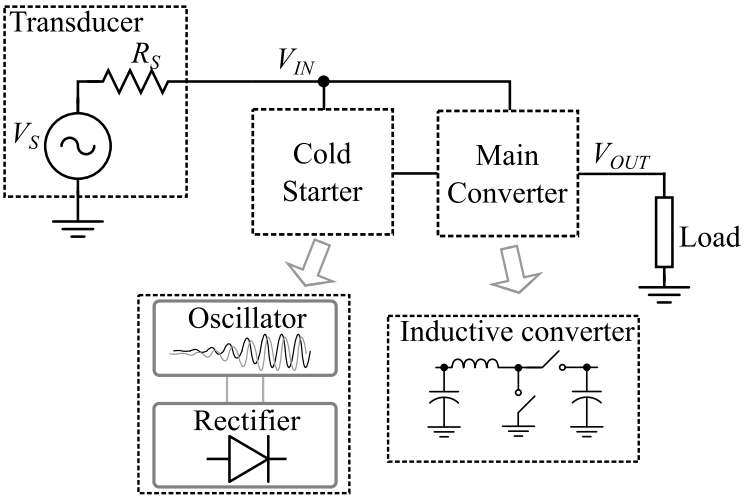

Fig. 1.11 An energy-harvesting interface comprised of a cold starter, the main inductive boost converter, and the load

In [38], an oscillator comprised of Schmitt-trigger stages and a cross-coupled rectifier was used, starting up the converter from an input voltage of 70 mV. By means of a cross-coupled oscillator (XCO) with on-chip inductors and an 8-stage charge pump, the work reported in [39] achieved startup with an input voltage of 65 mV at the cost of 0.65 mm^2 of silicon area for the inductors. Using stacked inverters to implement an on-chip oscillator and cross-coupled complementary charge pumps, the circuit described in [40] achieves startup for voltages as low as 57 mV.

1.4.2.2 Off-Chip Startup Mechanisms

The minimum voltage for a system startup can be lowered by using off-chip components, such as inductors, capacitors, and/or transformers, rather than on-chip components. A common approach to designing a cold starter is the use of a transformer in an LC oscillator, which is reused in the boost converter topology as the main inductor, as reported in [42, 43] and implemented in off-the-shelf products [44, 45]. The startup voltages of this type of cold starter are very low (21 mV in [43]), but a complex optimization of the transformer is required to achieve low-voltage startup and high efficiency. To provide startup at low input voltages and, simultaneously, high efficiency during steady state, the work reported in [46] uses a purpose-built transformer with a third coil, providing independent optimization of the startup and efficiency. A three-stage voltage converter is described in [34, 47], where an additional auxiliary stage between the steady-state boost converter and the cold starter is introduced, aiming to reduce the loading effects on the

cold starter at the cost of increased number of off-chip components and circuit complexity. In [48], a dual-stage converter is described, where the inductor used in the cold-starter Colpitts oscillator is reused by the boost converter in a steady state, achieving startup voltages lower than those of on-chip designs but still higher than those provided by transformer-based oscillators. In [33], an enhanced-swing cross-coupled oscillator (ES-XCO) and a Dickson charge pump (DCP) provide startup for voltage levels as low as 11 mV at the expense of four external inductors for the ES-XCO. In [49], the circuit achieves startup at 50 mV using a one-shot cold-start technique. Although no additional off-chip components are required, the startup circuit relies on an off-chip boost inductor.

1.5 MOS Transistor Modeling for Ultra-Low-Voltage Design

This section provides a concise model of the MOS transistor for the analysis and design of CMOS circuits that operate from reduced supply voltages of the order of some hundreds of mV or even less. The model provides a description of the current versus voltage characteristics of the MOS transistor from weak inversion to strong inversion, but emphasis will be placed on the former, since this is the most common region of operation of MOS circuits supplied by ULV sources.

1.5.1 DC Model of the MOS Transistor

In this subsection, we describe a MOS transistor model suitable for integrated circuit design. In this model, named the unified current control model (UICM), the drain current of the MOSFET is decomposed into its forward (I_F) and reverse (I_R) components [50–52]. In the UICM, I_F is dependent on both the gate (V_G) and source (V_S) voltages, while I_R is dependent on both the gate and drain (V_D) voltages, or, algebraically,

$$I_D = I_F - I_R = I(V_G, V_S) - I(V_G, V_D). \tag{1.4}$$

The voltages in (1.4), seen in Fig. 1.12, are referred to the substrate (B). Note that for a long-channel device, I_F is independent of the drain voltage, while I_R is independent of the source voltage.

The forward and reverse currents can be expressed in terms of the normalized forward (i_f) and reverse (i_r) components of the drain current [50–52] as

$$I_{F(R)} = I_S i_{f(r)}, \tag{1.5}$$

where

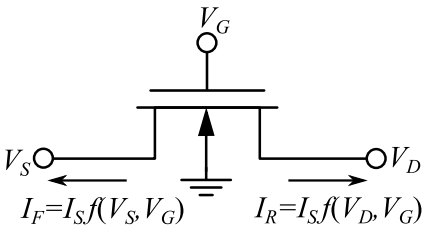

Fig. 1.12 NMOS transistor symbol. The drain current is the algebraic sum of the forward and reverse currents

$$I_S = I_{SH}\frac{W}{L} \tag{1.6}$$

is the specific (normalization) current, whereas W and L are the gate width and length, respectively, and

$$I_{SH} = \mu C_{ox} n \frac{\phi_t^2}{2} \tag{1.7}$$

is the sheet specific current, μ is the carrier mobility, C_{ox} is the oxide capacitance per unit area, n is the slope factor, and ϕ_t is the thermal voltage. For a given technology, I_{SH} is slightly dependent on the gate voltage but, for first-order calculations, can be assumed to be independent of bias.

The dependences of the normalized forward (i_f) and reverse (i_r) currents in terms of the applied voltages are given by the UICM [50–52] as

$$V_P - V_{S(D)} = \phi_t\left[\sqrt{1+i_{f(r)}} - 2 + \ln\left(\sqrt{1+i_{f(r)}} - 1\right)\right], \tag{1.8}$$

where V_P, the pinch-off voltage, is

$$V_P \cong \frac{V_G - V_{T0}}{n}, \tag{1.9}$$

and V_{T0} is the equilibrium threshold voltage [50–52].

In Fig. 1.13, the drain current of a long-channel MOSFET is plotted in terms of the drain voltage, for constant gate and source voltages. In the region generally referred to as saturation, the drain current is almost independent of V_D. This means that in saturation, $I(V_G, V_D) \ll I(V_G, V_S)$ or, equivalently, $i_f \gg i_r$. Therefore, $I(V_G, V_S)$ can be interpreted as the drain current in forward saturation. Similarly, in reverse saturation, I_D is independent of the source voltage. Even though the long-channel DC model is not accurate, it is a good approximation for first-order calculation of the DC current of any MOS transistor.

Let us now show the simplified results for operation of the transistor either in strong inversion or in weak inversion. Roughly speaking, weak inversion (WI) is a condition for which both inversion levels i_f and i_r are much less than unity, say 0.1 or less. In this case, the drain current is approximated as

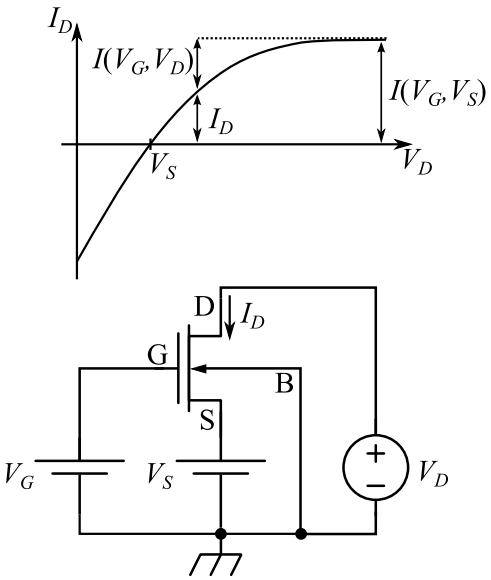

Fig. 1.13 Output characteristics of a long-channel NMOS transistor for constant V_S and V_G

$$I_D = I_X \left[e^{\frac{(V_P - V_{SB})}{\phi_t}} - e^{\frac{(V_P - V_{DB})}{\phi_t}} \right] = I_X e^{(V_P - V_{SB})/\phi_t} \left[1 - e^{-V_{DS}/\phi_t} \right], \tag{1.10}$$

where

$$I_X = \mu C_{ox} n \phi_t^2 e^1 \frac{W}{L}. \tag{1.11}$$

Note that for WI, we have $V_P - V_{S(D)} \ll -\phi_t$. From (1.10), we can see that the current saturates for $V_{DS} > 4\phi_t$ at a value equal to

$$I_D = I_X e^{(V_P - V_{SB})/\phi_t} \cong I_X e^{\frac{(V_{GB} - V_{T0})}{n\phi_t}} e^{-\frac{V_{SB}}{\phi_t}}. \tag{1.12}$$

Figure 1.14 shows the WI characteristics of a long-channel MOSFET [53]. The drain current increases one decade per $2.3n\phi_t$ of increase in the gate voltage and decreases one decade per $2.3\phi_t$ (around 60 mV at 20 °C) increase in the source voltage. The output characteristics in weak inversion saturate for a drain-to-source voltage of around $4\phi_t$, or around 100 mV at 20 °C.

For strong inversion (SI), $V_P - V_{S(D)} \gg \phi_t$. Thus, the drain current becomes approximately

$$I_D = \mu C_{ox} n \frac{W}{2L} \left[(V_P - V_S)^2 - (V_P - V_D)^2 \right], \tag{1.13}$$

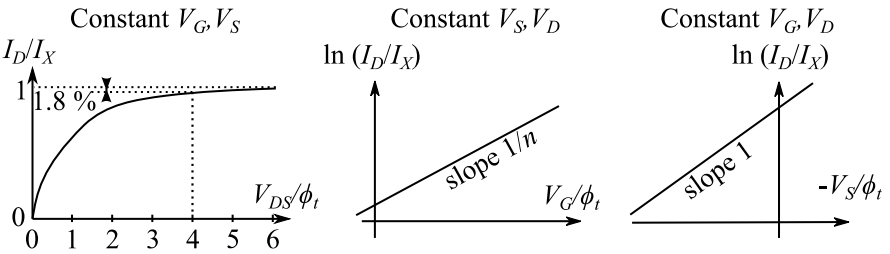

Fig. 1.14 Forward characteristics in weak inversion. (Adapted from [53])

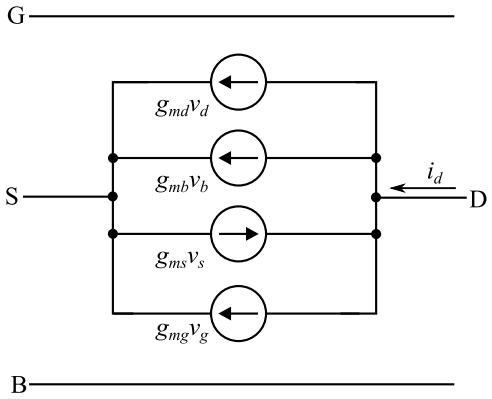

Fig. 1.15 Low-frequency small-signal model of the MOSFET

which for $n = 1$ (negligible body effect) coincides with the usual formula of the current of MOSFETs given in classical textbooks [5] and reproduced below:

$$I_D = \mu C_{ox} \frac{W}{2L} \left[(V_{GS} - V_{T0})^2 - (V_{GD} - V_{T0})^2 \right]. \tag{1.14}$$

In this book, we place greater emphasis on the weak inversion region, because for low supply voltages, the MOSFETs will generally operate in this region.

1.5.2 *Low-Frequency Small-Signal Model of the MOS Transistor*

At low frequencies, the small-signal model of the MOSFET is characterized by four transconductances, as shown in Fig. 1.15.

The gate, source, drain, and bulk transconductances are given by

$$g_{mg} = \frac{\partial I_D}{\partial V_G}, \quad g_{ms} = -\frac{\partial I_D}{\partial V_S}, \quad g_{md} = \frac{\partial I_D}{\partial V_D}, \quad g_{mb} = \frac{\partial I_D}{\partial V_B}. \tag{1.15}$$

Using the UICM of expression (1.8), the source and drain transconductances can be expressed as

$$g_{ms(d)} = \frac{2I_S}{\phi_t}\left(\sqrt{1 + i_{f(r)}} - 1\right). \tag{1.16}$$

Equation (1.16) for the transconductance is a universal expression that allows the source and drain transconductances of a long-channel MOSFET to be computed in terms of the inversion level $i_{f(r)}$.

The gate transconductance can be written as

$$g_{mg} = \frac{g_{ms} - g_{md}}{n}. \tag{1.17}$$

For a long-channel MOSFET in saturation, $i_r \ll i_f$, and consequently $g_{mg} \cong g_{ms}/n$. Lastly, the bulk transconductance g_{mb} can be calculated from

$$g_{ms} = g_{md} + g_{mg} + g_{mb}. \tag{1.18}$$

The small-signal transconductances, along with their dependence on the inversion levels, are instrumental for designing low-voltage oscillators, as we will see in Chap. 2.

1.5.3 Medium-Frequency Small-Signal Model of the MOS Transistor

A medium-frequency small-signal model of the MOSFET model, such as the one shown in the schematic in Fig. 1.16 [51, 52, 54], is suitable for the ULV applications covered in this book. Figure 1.16 includes five intrinsic capacitances, each of them defined as follows:

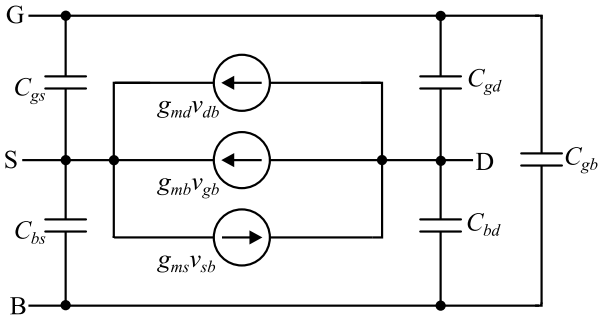

Fig. 1.16 Intrinsic small-signal MOSFET model. The complete small-signal model must include the extrinsic capacitances

$$C_{jk} = -\frac{\partial Q_j}{\partial V_k}, \tag{1.19}$$

where Q_j is the electrical charge associated with terminal j. The dependence of the capacitances on the operating point can be found in [51, 52, 54].

In addition to the intrinsic capacitances, the charge storage in the extrinsic parts of the MOS transistor must be incorporated into the model of Fig. 1.16. The overlap between the gate and the source and drain diffusions originates the overlap capacitances. In parallel with the overlap capacitance, the outer fringing and top capacitances must be included. The substrate-source and substrate-drain junctions must also be modeled by the nonlinear diode capacitances. Lastly, the extrinsic gate-to-bulk capacitance must be incorporated into the medium-frequency model [52, 54].

1.5.4 Diode-Connected MOS Transistors

Diodes are essential components for application in rectifier and charge-pump circuits. In this subsection, we examine some possible realizations of diodes.

We start with the Shockley equation of the p-n junction diode, which expresses the current I_D through the diode in terms of the diode voltage V_D as

$$I_D = I_{SAT}\left(e^{\frac{V_D}{n\phi_t}} - 1\right), \tag{1.20}$$

where I_{SAT} is the saturation current and n is the ideality factor, typically a number between 1 and 2. The p-n junction diodes of CMOS technologies are, in general, not appropriate for ULV applications due to the extremely low value of the saturation current per unit area along with its strong dependence on the temperature. However, for ULV applications, we can configure MOS transistors to operate as diodes, as we will see next.

Figure 1.17 shows two possible topologies for the MOS transistor connected as a diode. Note that the current through the device is composed of the transistor channel current plus the current through the p-n junction diode. The disadvantage of the MOS transistor in the usual connection, with the substrate (B) connected to the source (S) (Fig. 1.17a), is that the MOS diode and the p-n junction diode are connected in antiparallel. Consequently, when the MOS diode is reverse-biased, the p-n junction is forward-biased. As a result, we have a current that increases exponentially with the reverse voltage. To avoid the antiparallel connection of the MOS diode and the p-n junction, the dynamic threshold voltage MOSFET (DTMOS) configuration shown in Fig. 1.17b can be used. In this case, the channel and junction diodes are in parallel. The DTMOS can be used for p-channel transistors in an n-well process or for n-channel transistors in a p-well process or in triple-well processes. To model the MOS diodes, let us use, for simplicity, the WI model.

According to (1.10), the drain current for the MOS diode in Fig. 1.17a is

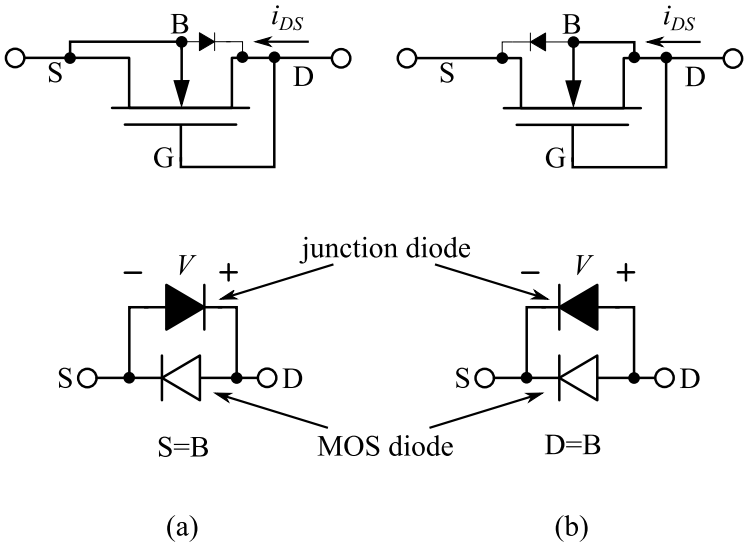

Fig. 1.17 MOSFET connections as a diode: (**a**) MOS transistor with the bulk connected to the source and (**b**) MOS transistor with the bulk connected to the gate and drain terminals

$$I_{DS} = I_X e^{-\frac{V_{T0}}{n\phi_t}} \left[e^{\frac{V}{n\phi_t}} - e^{\frac{-(n-1)V}{n\phi_t}} \right]. \tag{1.21}$$

Equation (1.21) shows that the reverse current of the MOS diode increases exponentially with the reverse voltage applied to the device. Note that the extrinsic p-n junction also contributes to the increase in the reverse current.

For the DTMOS connection, using Eq. (1.10) with $V_{GB} = 0$, $-V_{SB} = -V$, and $V_{DB} = 0$ yields

$$I_{DS} = I_X e^{-\frac{V_{T0}}{n\phi_t}} \left[e^{\frac{V}{\phi_t}} - 1 \right]. \tag{1.22}$$

As Eq. (1.22) shows, the DTMOS diode behaves as an ideal diode with ideality factor $n = 1$ for low-voltage operation (weak inversion). As is clear from Eqs. (1.21) and (1.22), the requirements for a high saturation current of the DTMOS are a low V_{T0} and a high aspect ratio.

1.6 Transistor Selection and Characterization

Selecting an appropriate technology is of utmost importance for ULV circuits. Enhancement-mode devices, such as MOS transistors with threshold voltage in the range of 0.3–0.5 V, operate with very low current density for supply voltages below

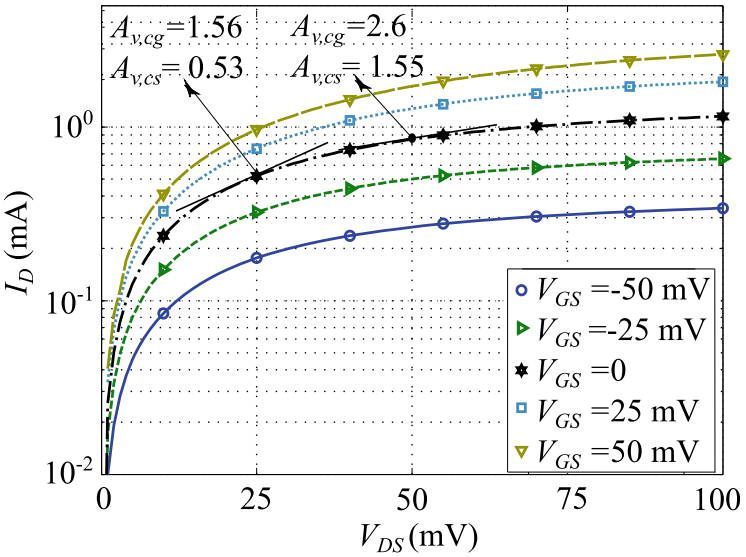

Fig. 1.18 Output characteristics of a zero-VT transistor with W/L = 2500 μm/420 nm

100 mV and are, thus, of very limited practical utility [55]. MOS transistors with low or near-zero threshold voltages are particularly suitable for ULV circuits due to their current drive capability and sufficient voltage gain at very low supply voltages. As can be seen in the experimental plot of I_D vs. V_{DS} for the zero-VT transistor in Fig. 1.18, the device presents a current capability of some hundreds of micro-amperes, for low or negative values of V_{GS}.

The intrinsic voltage gains of the common-gate and common-source amplifiers, *Av,cg* and *Av,cs*, respectively, of a zero-VT transistor are shown in Fig. 1.18. Assuming the operation of the transistor in weak inversion in the triode region [55], we have

$$Av, cg = \frac{g_{ms}}{g_{md}} = e^{\frac{V_{DS}}{\phi_t}}, \tag{1.23}$$

and

$$Av, cs = \frac{g_m}{g_{md}} = \frac{g_{ms} - g_{md}}{n g_{md}} = \frac{e^{\frac{V_{DS}}{\phi_t}} - 1}{n}. \tag{1.24}$$

For the common-source amplifier, the voltage gain equals unity for $V_{DS} = (kT/q)$ $\ln(1 + n)$. On the other hand, the common-gate amplifier provides a voltage gain of greater than unity for $V_{DS} > 0$. This property of the common-gate amplifier is very useful for lowering the supply voltage limit for the operation of oscillators.

1.6.1 Extraction of the Main MOSFET Parameters

The main parameters of the MOS transistor (V_T, I_S, and n) used in calculations throughout this book were extracted using a procedure based on the transconductance-to-current ratio (g_m/I_D) [50]. Briefly, V_T, I_S, and n are extracted from $I_D - V_G$ measurements in the circuit shown in the lower part of Fig. 1.19. For $V_{DS} = \phi_t/2$, V_T is the gate voltage at which the condition $g_m/I_D = 0.53.(g_m/I_D)_{max}$ holds. Also, the specific current $I_S = 1.63I_D^*$, I_D^* being the drain current determined when $V_G = V_T$. Because $(g_m/I_D)_{max} = 1/n\phi_t$, the slope factor n is easily extracted from the peak of the g_m/I_D curve and the temperature. Even though n decreases slightly with the increasing gate voltage, it is assumed to be independent of V_G for the calculations in this book.

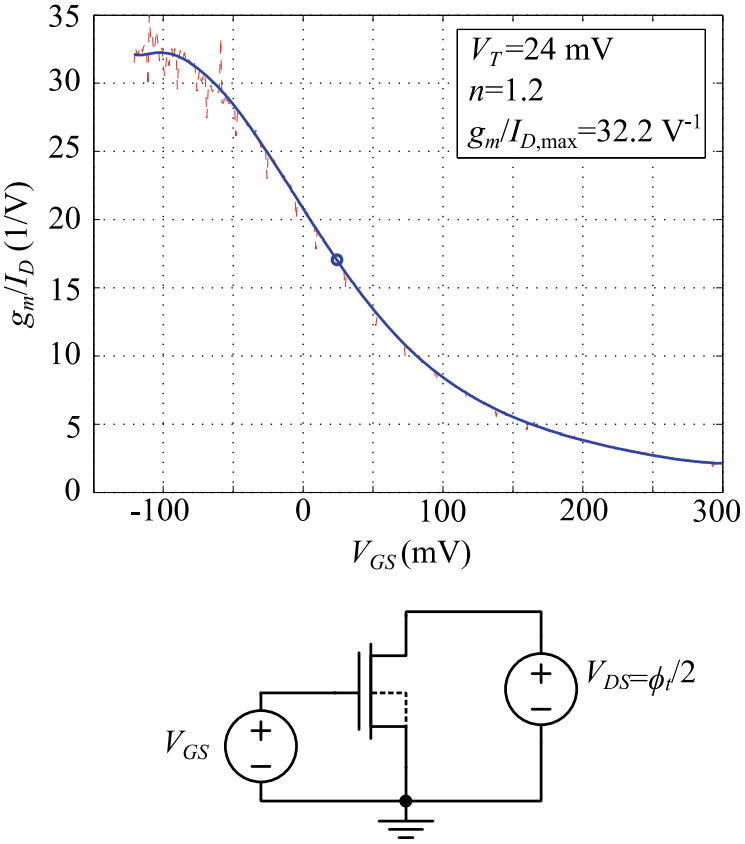

Fig. 1.19 Experimental g_m/I_D curve of a zero-VT transistor with W/L = 1500 µm/420 nm and the circuit configuration for extracting the main static MOSFET parameters

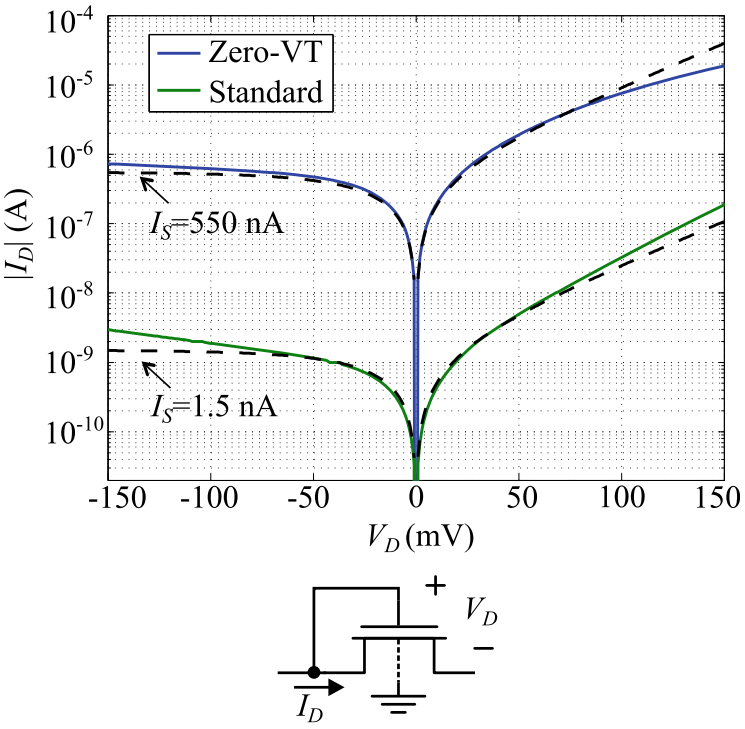

Fig. 1.20 Simulated I_D vs. V_D characteristics of the standard and zero-VT transistors available in the 130-nm technology, both connected as diodes with $W/L = 4.2$ μm/420 nm. The dashed line represents the ideal Shockley behavior given by (1.20) with $n = 1.4$ for both devices

1.6.2 Comparison Between Zero-VT and Standard Transistors Operating as Diodes

A comparison between the zero-VT and the standard transistors, both connected as diodes, is shown in Fig. 1.20. As can be seen in the graphs, for low V_D, the zero-VT MOSFET presents a saturation current more than two orders of magnitude higher than that of a conventional transistor of the same area available in a 130-nm process.

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Chapter 2
Ultra-Low-Voltage Oscillators

2.1 Introduction to Ultra-Low-Voltage Oscillators for Energy Harvesting

Ultra-low-voltage (ULV) oscillators are important building blocks for energy-harvesting converters due to their ability to self-start at extremely low supply voltages. This characteristic makes them a feasible means for starting up voltage converters operating from the low voltage levels provided by energy-harvesting transducers.

In recent years, some authors have presented complementary metal-oxide-semiconductor (CMOS) oscillators able to operate from ultra-low DC voltages, typically smaller than 100 mV. Back in the 1990s, a CMOS ring oscillator operating from V_{DD} of 100 mV was presented in [1]. To reduce V_{DD} to a minimum, the circuit in [1] employed transistors with threshold voltages close to zero that were tuned using back bias. More recently, different CMOS-based ring oscillator topologies have been explored. A VT-tuned CMOS oscillator with hot-carrier injection, described in [2], achieved startup for supply voltages as low as 80 mV. A further reduction in the supply voltage of CMOS oscillators was demonstrated in [3], using a stacked inverter topology, and in [4, 5], using Schmitt trigger cells.

Targeting a more aggressive reduction in the minimum supply voltage for the achievement of oscillations, LC-based ULV oscillators have been widely adopted in energy-harvesting applications. Employing native transistors and external inductors and capacitors, recent publications report the operation of classical topologies, such as the Colpitts oscillator, from DC voltages lower than 20 mV [6–8]. A further reduction in V_{DD} is achieved using the enhanced-swing ring oscillator [9]. Employing native transistors, the topology in [9] can operate from voltages as low as 30 mV and 5 mV, with fully integrated and off-the-shelf inductors, respectively.

R. L. Radin et al., *Ultra-low Voltage Circuit Techniques for Energy Harvesting*,
Analog Circuits and Signal Processing, https://doi.org/10.1007/978-3-031-04492-2_2

The adoption of LC oscillators in energy-harvesting circuits allows the startup and operation of DC-DC converters from voltages well below 100 mV, as reported by several authors [10–15] in the past decade. Therefore, due to the important characteristics of ULV startup, herein we focus on the analysis, design, and implementation of three LC-based oscillator topologies, namely, the cross-coupled oscillator (XCO), the enhanced-swing cross-coupled oscillator (ES-XCO), and the enhanced-swing Colpitts oscillator (ESCO).

2.2 The Cross-Coupled LC Oscillator

In the inductive ring oscillator shown in Fig. 2.1 [9], an inductor replaces the PMOS transistor of the classical CMOS inverter. In this configuration, the oscillator can operate from lower supply voltages than the classical CMOS inverter and boost the amplitude of the oscillations beyond the supply voltage. When the number of stages is equal to 2, the inductive ring oscillator is reduced to the cross-coupled LC oscillator (XCO), shown in Fig. 2.2, which is widely used in energy-harvesting applications.

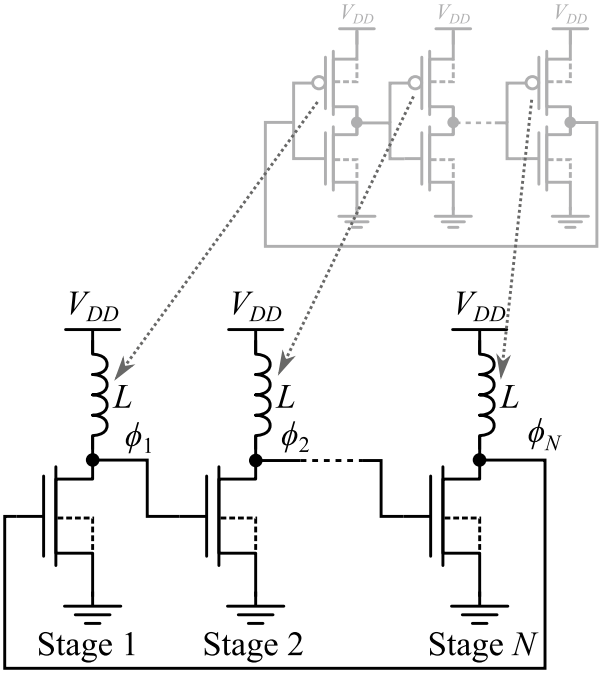


Fig. 2.1 Schematic of an *N*-stage inductive ring oscillator

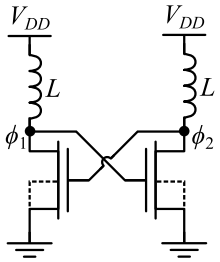


Fig. 2.2 Schematic of the cross-coupled LC oscillator

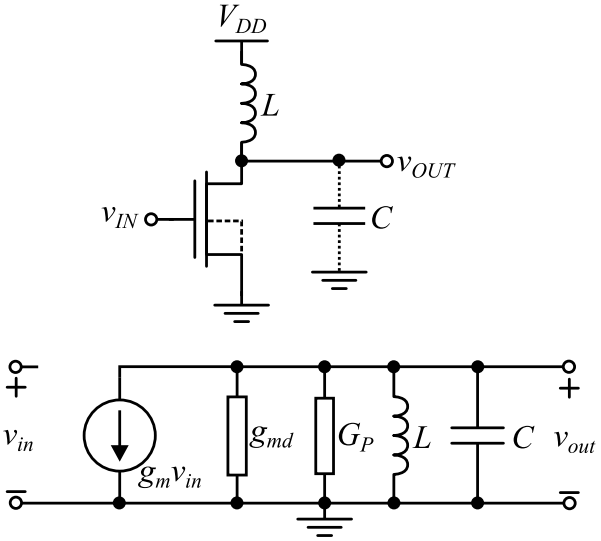


Fig. 2.3 Schematic and the simplified small-signal model of a single stage of the XCO

2.2.1 Analysis of the Cross-Coupled LC Oscillator

The analysis of the XCO is based on the simplified small-signal equivalent circuit of a single stage of the XCO shown in Fig. 2.3 [9, 16], where g_m and g_{md} are the gate and drain transconductances, respectively, C is the sum of all parasitic capacitances between the drain node and the AC ground, and G_P models the inductor losses. For the sake of simplicity, it is assumed that the drain-to-gate capacitance C_{gd} is negligible. The transfer function of the single stage in Fig. 2.3 is given by

$$\frac{v_{out}}{v_{in}} = -\frac{g_m}{g_{md}+G_P}\frac{1}{1-j\tan\phi}, \tag{2.1}$$

where ϕ, the phase shift between the output and the input, is given by

$$\phi = \tan^{-1}\left(\frac{1-LC\omega^2}{\omega L(g_{md}+G_P)}\right). \tag{2.2}$$

2.2.1.1 Oscillation Frequency of the Cross-Coupled Oscillator

The Barkhausen criterion states that the phase shift around the loop should be equal to zero or an integer multiple of 2π for the achievement of oscillations, thus requiring the phase shift introduced by each stage of the XCO to be equal to π. Therefore, from (2.2), the oscillation frequency ω_o is

$$\omega_o = \frac{1}{\sqrt{LC}}\,. \tag{2.3}$$

2.2.1.2 Minimum Supply Voltage for Oscillation Startup of the Cross-Coupled Oscillator

Once the Barkhausen criterion for phase has been satisfied at ω_o, the loop gain calculated from (2.1) is given by

$$H(j\omega) = \left(-\frac{g_m}{g_{md} + G_P}\right)^2. \tag{2.4}$$

From (2.4), the requirement of greater than unity gain for the starting up of oscillations is satisfied if

$$\frac{g_m}{g_{md}}\,\frac{1}{1+\frac{G_P}{g_{md}}} > 1. \tag{2.5}$$

Because the relation between source, drain, and gate transconductances (g_{ms}, g_{md}, and g_m, respectively) is $g_m = (g_{ms} - g_{md})/n$ (Chap. 1), the minimum transistor gain g_{ms}/g_{md} required for oscillation, calculated from (2.5), is

$$\frac{g_{ms}}{g_{md}} > 1 + n\left(1 + \frac{G_P}{g_{md}}\right), \tag{2.6}$$

where n is the transistor slope factor.

The minimum supply voltage required to start up the oscillator ($V_{DD,min}$) can be calculated using (2.6) and the expression for the drain-source voltage (V_{DS}) provided by the MOSFET model described in Chap. 1 given by

$$\frac{V_{DS}}{\phi_t} = \frac{\phi_t}{2I_S}\,g_{md}\left(\frac{g_{ms}}{g_{md}} - 1\right) + \ln\frac{g_{ms}}{g_{md}}. \tag{2.7}$$

For each transistor in Fig. 2.1, the DC voltages are $V_S = V_B = 0$ and $V_G = V_D = V_{DD}$. Because V_{DS} ($= V_{DD}$), given by (2.7), is a monotonic function of

the g_{ms}/g_{md} ratio, the minimum supply voltage required to start up the oscillator is calculated by substituting (2.6) into (2.7), yielding

$$V_{DD,min} = \frac{\phi_t^2}{2I_S} n g_{md} \left(1 + \frac{G_P}{g_{md}}\right) + \phi_t \ln\left[1 + n\left(1 + \frac{G_P}{g_{md}}\right)\right]. \tag{2.8}$$

The limit value for minimum supply voltage required to start up the oscillator ($V_{DD,lim}$) is obtained when the transistor operates in weak inversion and the inductor losses are negligible. Thus,

$$V_{DD,lim} = \phi_t \ln[1 + n]. \tag{2.9}$$

If $n = 1$, the limit given by (2.9) is around 18 mV at room temperature. This limit shows that the circuit can theoretically operate with one-half the value of the Meindl limit [17] of digital circuits, which for a CMOS inverter is 36 mV at room temperature. This result was expected since the oscillation condition of the cross-coupled oscillator (loaded with an infinite-Q tank) is that the voltage gain of the transistor equals unity. The unity gain of a transistor operating in weak inversion is obtained for a supply voltage of 18 mV at room temperature [6].

2.2.2 *Cross-Coupled Oscillator Design and Experimental Results*

Experimental results for the oscillator topology in Fig. 2.2, operating from DC voltages below 100 mV, have been reported in the technical literature for different realizations [16, 18]. For energy-harvesting applications, the oscillator design should consider the reduction of $V_{DD,min}$, form factor, and power consumption. In this section, we focus on the design and experimental results of a fully integrated cross-coupled oscillator [16].

2.2.2.1 Design of a Fully Integrated Cross-Coupled Oscillator

Based on the analysis presented in Sect. 2.1, an XCO that operates from supply voltages lower than 50 mV was designed. From (2.8), one can see that the minimum supply voltage has a strong dependence on the inductor losses. Thus, inductors with a high-quality factor at the oscillation frequency ($Q \approx 8$ at 500 Mhz) were chosen. It is then possible to calculate (or determine through simulation) the W/L ratio of the zero-VT transistor to achieve the required capacitance for the specified oscillation frequency (f_{osc}), which should be lower than the self-resonant frequency (SRF) of the inductors. The characteristics of the integrated transistors and inductors are

Table 2.1 Summary of the device characteristics and the main simulated and experimental results of the fully integrated two-stage XCO [16]

Device characteristics		Results	
Transistor	Inductor	Simulated	Experimental
$W/L = 30 \times 6\mu m/0.42\ \mu m$	$L = 108$ nH	$V_{DD,min} = 38$ mV	$V_{DD,min} = 45.3$ mV
$V_T = 53$ mV	$Q = 7.9$	$f_{osc} = 467$ MHz	$f_{osc} = 410$ MHz
$I_S = 75\ \mu A$	SRF = 1.1 GHz	$I_{DC} = 0.14$ mA	$I_{DC} = 0.26$ mA
$g_{md} = 2.06$ mA/V			

[a] g_{md} and I_{DC} were determined at $V_{DD} = 30$ mV and 50 mV, respectively
[b] L was simulated at 460 MHz

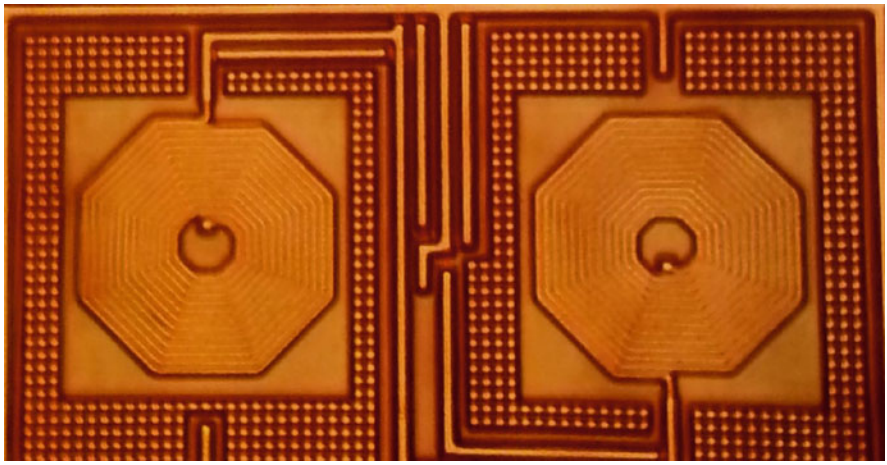


Fig. 2.4 Micrograph of the two-stage XCO in the 130-nm technology

summarized in Table 2.1. Differences between the simulated and experimental values of the DC current (I_{DC}) at $V_{DD} = 50$ mV are mainly attributed to the differences between the nominal and practical values of the threshold voltage.

A micrograph of the fully integrated XCO in a 130-nm technology can be seen in Fig. 2.4. Measurements were taken in both the time and frequency domains. The experimental waveforms shown in Fig. 2.5a for each output of a voltage buffer, which has as inputs the two phases of the inductive ring oscillator, were measured using an oscilloscope (Tektronix DSA 70804C). The measured oscillation frequency is around 410 MHz for $V_{DD} = V_{DD,min} = 45.3$ mV. The spectrum of the signal generated by the XCO for $V_{DD} = 50$ mV, which is shown in Fig. 2.5b, was taken using the spectrum analyzer Agilent MXA 9020A.

The oscillation amplitude and frequency of the XCO were measured as functions of the supply voltage, as shown in Fig. 2.6. The peak-to-peak oscillation amplitude (V_{PP}) is around 68 mV at $V_{DD} = 50$ mV.

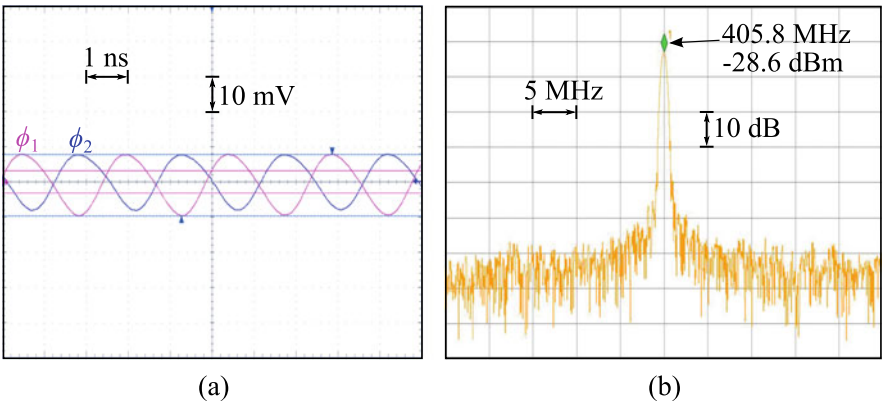
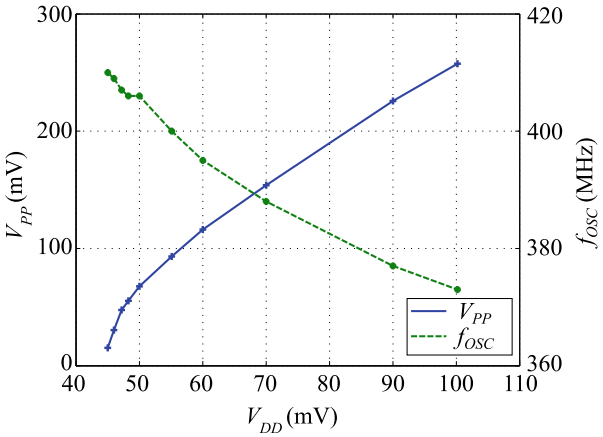


Fig. 2.5 (**a**) Experimental waveforms at the buffer outputs for $V_{DD} = 45.3$ mV and (**b**) spectral diagram of the cross-coupled oscillator signal for $V_{DD} = 50$ mV

Fig. 2.6 Experimental peak-to-peak output voltage and oscillation frequency of the XCO versus V_{DD}



The deviations of the minimum supply voltage, oscillation frequency, and DC power consumption (measured at $V_{DD} = V_{DD,min}$) were determined from the measurements taken for five samples. The slight variation of the oscillation frequency with V_{DD} is due to the nonlinear capacitances of the MOSFET. The maximum deviation of $V_{DD,min}$ between the samples was 2 mV, whereas the frequency deviation between the fastest and the slowest sample was less than 1%. The power consumption of the oscillator was below 20 µW for all five samples.

The main simulated and experimental results of the XCO are summarized in Table 2.1. Since the main goal of this design is to obtain an oscillator for energy-harvesting applications that provides startup at ultra-low supply voltages, the accuracy of the oscillation frequency is not of major concern.

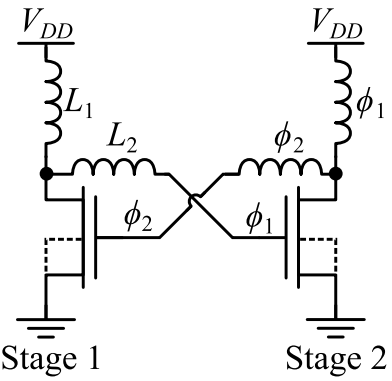


Fig. 2.7 Schematic diagram of a two-stage ES-XCO

2.3 The Enhanced-Swing Cross-Coupled Oscillator

The enhanced-swing cross-coupled oscillator (ES-XCO), shown in Fig. 2.7, is a variation of the XCO that uses an additional inductor between adjacent stages of the oscillator to further reduce $V_{DD,min}$ and increase the oscillation amplitude [19, 20].

2.3.1 Analysis of the Enhanced-Swing Cross-Coupled Oscillator

The simplified small-signal equivalent circuit of a single stage of the ES-XCO is shown in Fig. 2.8, where R_{S2} is the series resistance of inductor L_2, G_{P1} is the parallel conductance of L_1, and the other symbols have the same meaning as in Fig. 2.3. To simplify the analysis, the transistor capacitance C_{gd} was not taken into account.

The transfer function of the single stage in Fig. 2.8 is

$$\frac{v_{out}}{v_{in}} = -\frac{j\omega g_m L_1}{j\omega(g_{md}+G_{P1})L_1\left[1-\omega^2 L_2 C+\frac{R_{S2}C/L_1}{(g_{md}+G_{P1})}\right]-\omega^2 L_1 C[1+(g_{md}+G_{P1})R_{S2}+L_2/L_1]+1} \tag{2.10}$$

The condition of loop phase shift equal to a multiple of 2π for oscillation requires the phase shift between the two stages of the circuit in Fig. 2.7 to be equal to π, similar to the XCO.

2.3.1.1 Oscillation Frequency of the Enhanced-Swing Cross-Coupled Oscillator

The condition for a phase shift equal to π between v_{out} and v_{in} is that the imaginary part of (2.10) equals zero. Therefore,

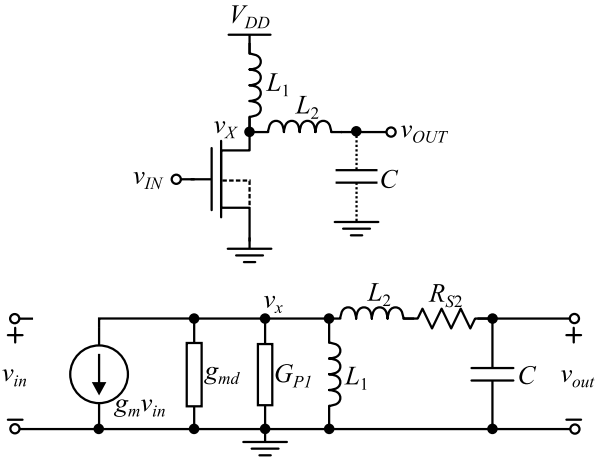


Fig. 2.8 Schematic and simplified small-signal model of a single stage of the ES-XCO

$$\omega_o = \frac{1}{\sqrt{L_1 C[1 + L_2/L_1 + R_{S2}(g_{md} + G_{P1})]}}, \tag{2.11}$$

which, for lossless inductors, reduces to

$$\omega_o = \frac{1}{\sqrt{(L_1 + L_2)C}}\ . \tag{2.12}$$

2.3.1.2 Enhanced-Swing Cross-Coupled Oscillator Minimum Supply Voltage for Oscillation Startup

From (2.10), the greater-than-unity gain required to start up oscillations is achieved for

$$g_m > \left[(g_{md} + G_{P1})\left(1 - L_2 C\omega_o^2\right) + \frac{R_{S2}C}{L_1}\right]. \tag{2.13}$$

Because $g_m = (g_{ms} - g_{md})/n$ (see Chap. 1), (2.13) can be rewritten as

$$\frac{g_{ms}}{g_{md}} > 1 + n\left[\left(1 + \frac{G_{P1}}{g_{md}}\right)\left(1 - L_2 C\omega_o^2\right) + \frac{R_{S2}C}{L_1 g_{md}}\right]. \tag{2.14}$$

Assuming that the inductors are lossless and the oscillation frequency is given by (2.12), the transistor gain required for oscillation in (2.14) can be rewritten as

$$\frac{g_{ms}}{g_{md}} > 1 + n\left[\frac{L_1}{L_1 + L_2}\right]. \tag{2.15}$$

We follow the same procedure used for the XCO to calculate the minimum supply voltage. For each oscillator transistor, we have the DC values $V_S = V_B = 0$ and $V_G = V_D = V_{DD}$. For a fixed g_{md}, the minimum V_{DS} ($= V_{DD}$) is reached combining the equation for the minimum g_{ms}/g_{md} ratio given in (2.14) and the expression for the drain-source voltage (V_{DS}) in Chap. 1. Thus, for operation in weak inversion, the limit value for the minimum supply voltage is given by

$$V_{DD,lim} = \phi_t \ln\left(1 + n\frac{L_1}{L_1 + L_2}\right). \tag{2.16}$$

If $L_2 \gg L_1$, the voltage gain of the transistor can be (much) lower than unity. Thus, for high values of L_2/L_1, the ES-XCO is capable of oscillating at supply voltages well below the thermal voltage, as experimentally verified in Sect. 2.2.2.

2.3.1.3 The Effect of the Load on the Oscillating Frequency and Minimum Transistor Gain

For energy-harvesting applications, the output of the oscillator is typically loaded by an AC-DC converter, such as a charge-pump circuit. Thus, we analyze the effect of the output load on the behavior of the ES-XCO shown in Fig. 2.9a. Using the equivalent small-signal circuit of a single stage, as shown in Fig. 2.9b, the transfer function of a single stage is

$$\frac{v_{out}}{v_{in}} = -\frac{g_m}{\left(g_{md} + G_{P1} + \frac{1}{sL_1}\right)[(sC + G_o)(sL_2 + R_{S2}) + 1] + sC + G_o}. \tag{2.17}$$

where G_o represents the load at the oscillator output.

Following the same procedure adopted for calculating the oscillation frequency of the unloaded ES-XCO, the oscillation frequency for the loaded oscillator is given by

$$\omega_o = \sqrt{\frac{G_o R_{S2} + 1}{(L_1 + L_2)C + L_1(R_{S2}C + L_2 G_o)(g_{md} + G_{P1})}}, \tag{2.18}$$

which reduces to

$$\omega_o = \frac{1}{\sqrt{(L_1 + L_2)C + L_1 L_2 G_o g_{md}}} \tag{2.19}$$

for negligible inductor losses. The greater-than-unity gain required for oscillations is achieved for

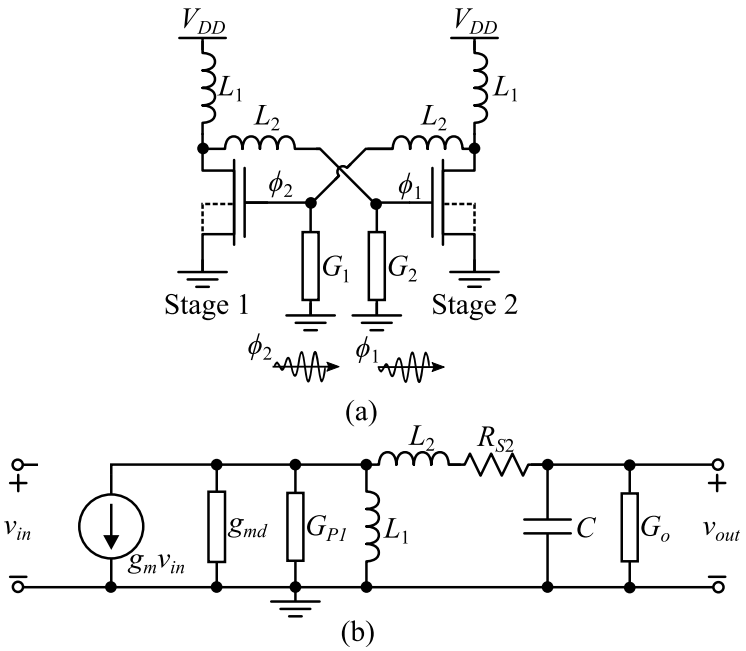


Fig. 2.9 (**a**) Schematic diagram of the two-stage ES-XCO and (**b**) simplified small-signal model of a single stage of the ES-XCO

$$g_m > g_{md}\left(1 - L_2 C\omega_o^2 +\right) + G_o\left(1 + \frac{L_2}{L_1}\right), \tag{2.20}$$

which can be written in terms of g_{ms} and g_{md} as

$$\frac{g_{ms}}{g_{md}} > 1 + \frac{n}{g_{md}}\left[g_{md}\left(1 - L_2 C\omega_o^2\right) + G_o\left(1 + \frac{L_2}{L_1}\right)\right]. \tag{2.21}$$

Finally, disregarding the inductor losses, assuming $n = 1$ and substituting (2.19) into (2.21), the minimum transistor gain required for oscillation can be written as

$$\frac{g_{ms}}{g_{md}} > 2 - \frac{L_2 C}{(L_1 + L_2)C + L_1 L_2 G_o g_{md}} + \frac{G_o}{g_{md}}\left(1 + \frac{L_2}{L_1}\right). \tag{2.22}$$

The effect of G_o on both the oscillation frequency (2.19) and the minimum transistor gain (2.22) is shown in Fig. 2.10. The effect of G_o on the minimum transistor gain required for oscillation can be reduced by increasing g_{md} through transistor widening.

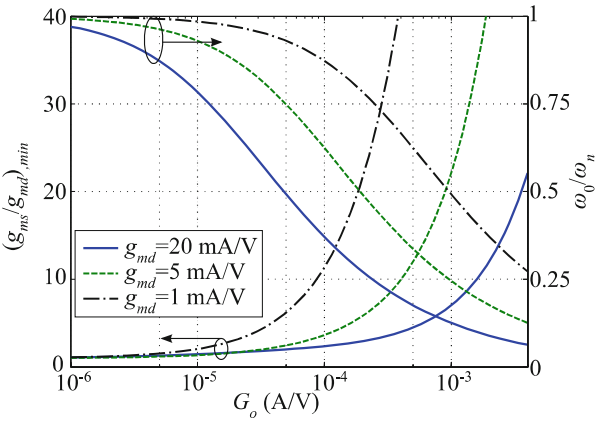


Fig. 2.10 Calculated oscillation frequency normalized to $\omega_n = 1/\sqrt{(L_1 + L_2)C}$ and minimum transistor gain as a function of the output conductance. $L_1 = 9.5$ µH, $L_2 = 950$ µH (both with $Q = 80$) and $C = 3$ pF

2.3.2 *Enhanced-Swing Cross-Coupled Oscillator Design and Experimental Results*

To demonstrate the capability of the ES-XCO to operate from ultra-low supply voltages and to boost the oscillation amplitude beyond the supply rails, the design and the experimental results of two ES-XCOs are described in this section. The first ES-XCO was built with off-the-shelf inductors while the second ES-XCO with fully integrated inductors. The ES-XCOs demonstrated operation at supply voltages as low as 3.5 mV and 30 mV, respectively.

2.3.2.1 Design of an Enhanced-Swing Cross-Coupled Oscillator Using Off-the-Shelf Components

A prototype of an ES-XCO was realized using off-the-shelf inductors and native transistors with an aspect ratio of $W/L = 1500$ µm/420 nm in a 130-nm CMOS process [9]. The transistors, which were designed to provide enough drive capability to compensate for the inductor losses, were built as a parallel association of 300 × 5 µm-width transistors with minimum channel length. The oscillator circuit, along with the values for the inductor parameters characterized at 1 MHz, are shown in Fig. 2.11.

The voltages at the oscillator outputs are shown in Fig. 2.12a, b for supply voltages of 3.7 mV and 4.7 mV, respectively. The measured oscillation frequency is around 1.1 MHz. Note that the amplitude of the output voltage greatly exceeds the supply voltage. The difference in the magnitudes is a consequence of mismatches between inductors and between transistors.

The oscillation amplitude in terms of the supply voltage is shown in Fig. 2.13. The measured values are very close to those obtained from simulations using

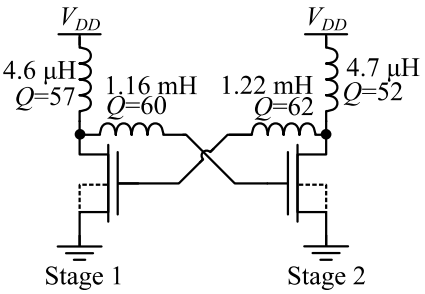


Fig. 2.11 The ES-XCO with off-the-shelf inductors

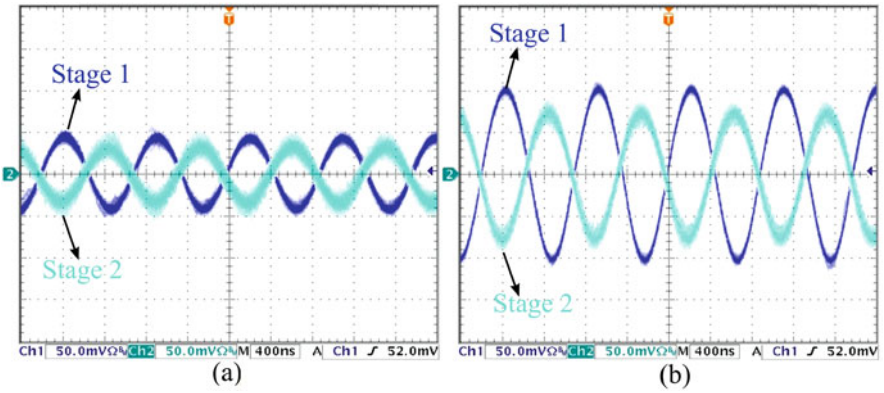


Fig. 2.12 Experimental gate voltages of the ES-XCO for (**a**) $V_{DD} = 3.7$ mV and (**b**) $V_{DD} = 4.7$ mV

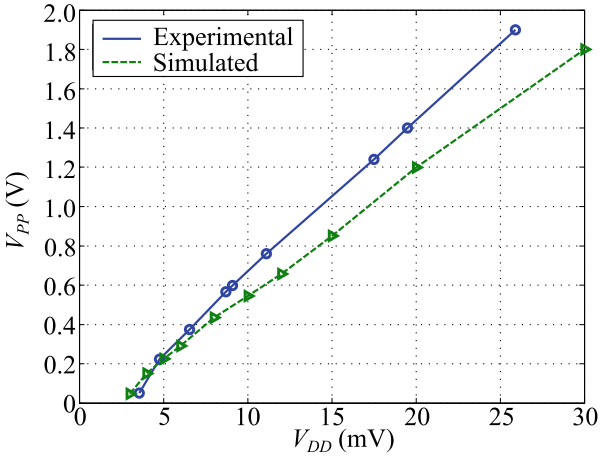


Fig. 2.13 Simulated and experimental peak-to-peak gate voltage vs. supply voltage of the ES-XCO

Cadence Spectre. The photograph in Fig. 2.14 indicates the discrete prototype of the ES-XCO, along with the measurement equipment. In this experiment, in which the minimum supply voltage for oscillation was around 3.5 mV, each oscillator output was loaded by an oscilloscope probe of $R = 1$ MΩ and $C = 2$ pF.

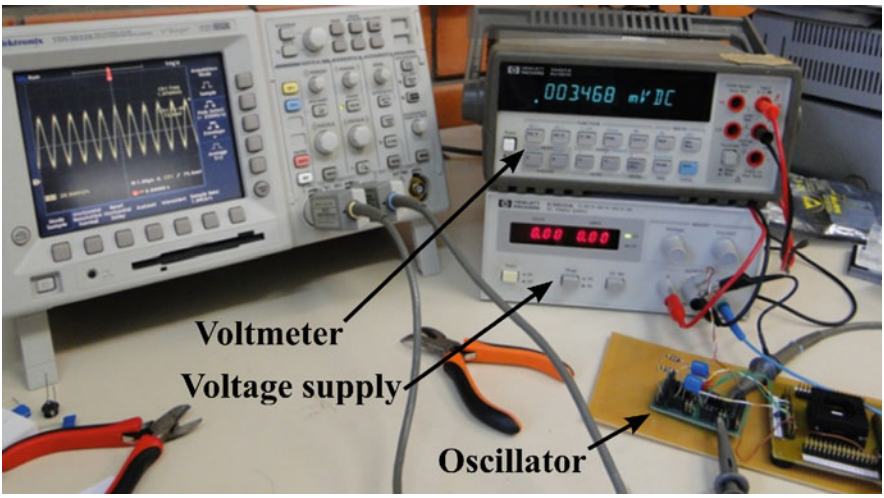


Fig. 2.14 Picture of the discrete prototype of the ES-XCO and test equipment

2.3.2.2 Design of a Fully Integrated Enhanced-Swing Cross-Coupled Oscillator

A prototype of a fully integrated ES-XCO was implemented in the 130-nm CMOS process [16]. The inductors were designed to achieve a relatively high $K_L = L_2/L_1$ ratio (around 4) targeting the reduction of g_{ms}/g_{md} and, consequently, the reduction of $V_{DD,min}$. Both inductors have a relatively high Q (around 8 at 400 MHz), which is close to the maximum value of Q for the technology under consideration.

The oscillator transistor was sized with minimum length, while the width was sized to achieve a gate capacitance of the order of 1.6 pF, which would result in an oscillation frequency of approximately 400 MHz. Due to the additional parasitic elements introduced by the physical layout, we resorted to some fine-tuning through simulation to determine the transistor width, which was found to be 25 × 20 μm for starting up oscillations at the lowest supply voltage.

A summary of the characteristics of the components of the ES-XCO is given in Table 2.2. As can be seen, the measurements and the simulated results of the ES-XCO match approximately. Figure 2.15 shows a micrograph of the ES-XCO circuit integrated in a 130-nm technology.

The same setup used to measure the fully integrated XCO was employed to characterize the fully integrated ES-XCO. Voltage buffers were employed to measure the two oscillator phases shown in Fig. 2.16a. A remarkable feature of this circuit is that it oscillates from a supply voltage of as low as 30 mV, despite the different amplitudes of the waveforms. The oscillation frequency is around 340 MHz. The spectrum of the signal generated by the fully integrated ES-XCO for $V_{DD} = 30$ mV can be seen in Fig. 2.16b.

Table 2.2 Summary of device characteristics and the main simulated and experimental results for the fully integrated ES-XCO design [16]

Device characteristics			Results	
Transistor	Inductor L_1	Inductor L_2	Simulated	Experimental
$W/L = 25 \times 20\mu m/0.42\ \mu m$	$L = 19$ nH	$L = 80$ nH	$V_{DD,min} = 29$ mV	$V_{DD,min} = 30$ mV
$V_T = 46$ mV	$Q = 8.7$	$Q = 7.9$	$f_{osc} = 410$ MHz	$f_{osc} = 340$ MHz
$I_S = 225\ \mu A$	SRF = 6.2 GHz	SRF = 1.2 GHz	$I_{DC} = 0.72$ mA	$I_{DC} = 0.86$ mA
$g_{md} = 7$ mA/V				

[a] *gmd* and *IDC* were obtained at *VDD* = 30 mV and 50 mV, respectively
[b] L_1 and L_2 were simulated at 460 MHz

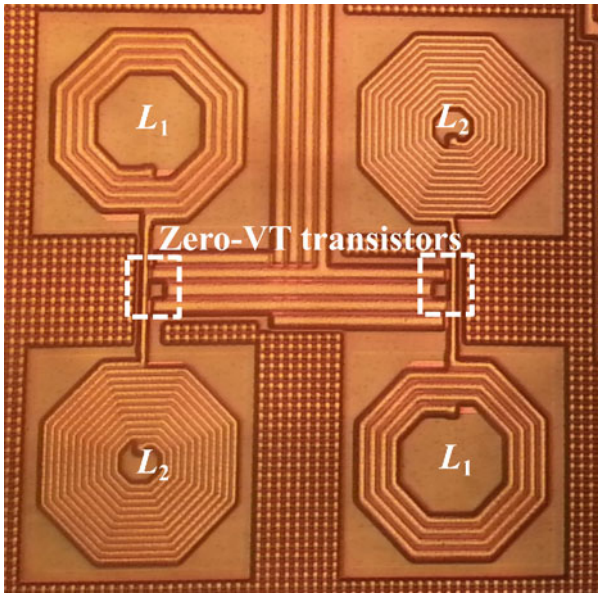


Fig. 2.15 Micrograph of the two-stage ES-XCO in the 130-nm technology

The dependence of both the amplitude and frequency of the ES-XCO on the supply voltage V_{DD} can be seen in Fig. 2.17. For $V_{DD} = 50$ mV, the peak-to-peak amplitude is around 290 mV. The minimum supply voltage for starting up oscillations is 30 mV at room temperature.

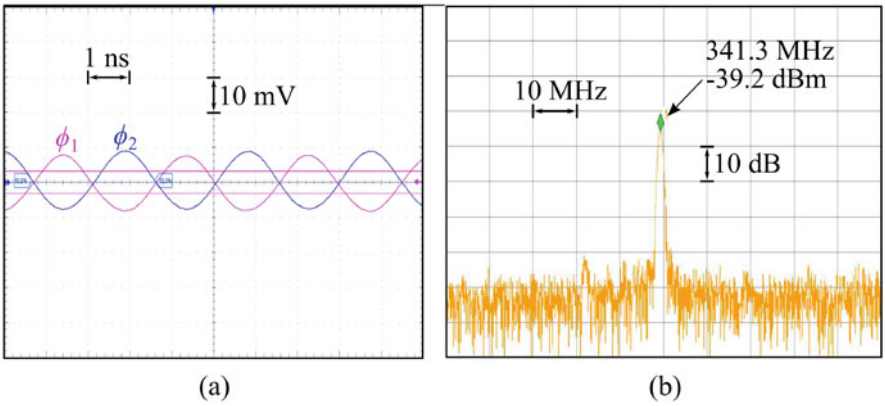


Fig. 2.16 (**a**) Waveforms at the output of the voltage buffers for $V_{DD} = 32$ mV and (**b**) spectral diagram for the ES-XCO with $V_{DD} = 30$ mV

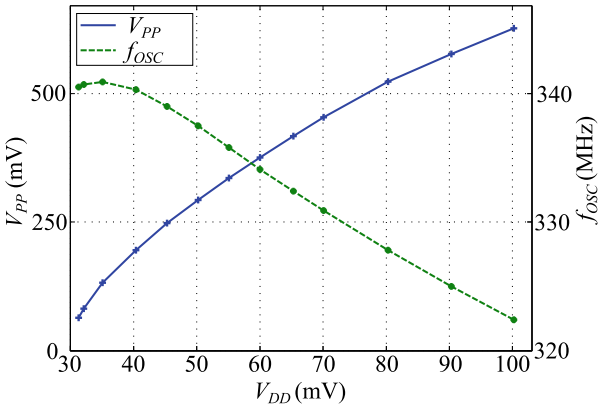


Fig. 2.17 Experimental peak-to-peak output voltage and frequency of the ES-XCO as a function of V_{DD}

2.4 The Ultra-low-Voltage Enhanced-Swing Colpitts Oscillator

For ULV applications, the conventional Colpitts oscillator illustrated in Fig. 2.18 presents some limitations, which will be discussed before analyzing the enhanced-swing Colpitts oscillator (ESCO).

When the voltage swing is large, the current source enters the triode region for a fraction of the period, leading to a close-to-zero voltage drop across the current source. Thus, the minimum voltage at the source and drain is limited to around zero volts (ground level). Consequently, the maximum sinusoidal peak-to-peak voltage swing at the drain cannot exceed $2V_{DD}$ (supply-limited region), which is an important drawback of the Colpitts oscillator in Fig. 2.18.

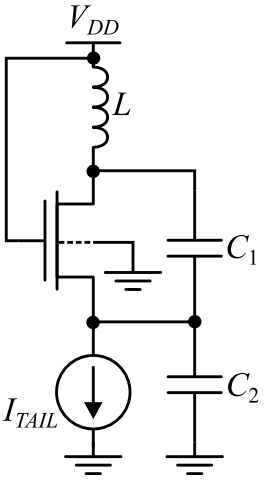


Fig. 2.18 Conventional Colpitts oscillator

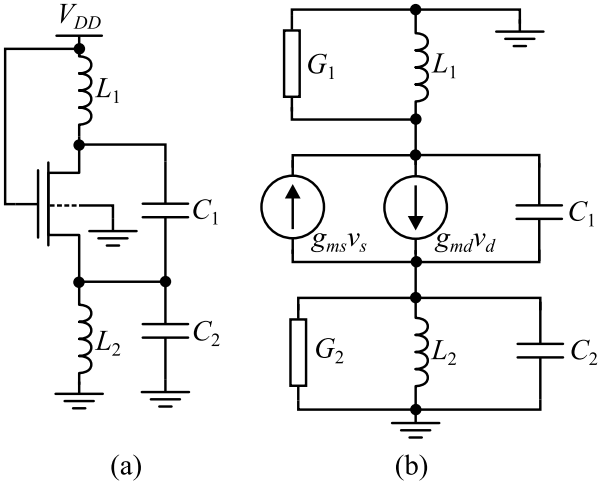


Fig. 2.19 (**a**) Schematic of the ESCO and (**b**) its small-signal model

In order to increase the voltage swing of the oscillations, the current source in Fig. 2.18 can be replaced by an inductor [7, 21–23], as shown in Fig. 2.19a. This topology can boost the oscillation amplitude beyond the supply rails. In [24], in addition to the inclusion of a second inductor, substrate bias is used to reduce the minimum V_{DD} required for oscillations.

2.4.1 Analysis of the Enhanced-Swing Colpitts Oscillator

The small-signal model of the ESCO is shown in Fig. 2.19b. The transistor capacitances at the source node are absorbed into C_2. G_1 and G_2 model the losses of inductors L_1 and L_2, respectively.

2.4.1.1 Oscillation Frequency of the Enhanced-Swing Colpitts Oscillator

For the sake of simplicity, let us assume that the ESCO oscillation frequency is independent of both the losses and the transistor parameters. The oscillation frequency can be calculated as the resonance frequency of the equivalent LC tank (Fig. 2.19b) composed of the inductor L_1 and an equivalent capacitance C_{eq} given by

$$C_{eq} = \frac{C_1 C_2'}{C_1 + C_2'}, \tag{2.23}$$

where

$$C_2' = C_2 - \frac{1}{\omega_o^2 L_2} \tag{2.24}$$

is the equivalent capacitance of the L_2C_2-tank at the oscillation frequency ω_o, which can be determined from

$$\omega_o^2 L_1 C_{eq} = 1. \tag{2.25}$$

The value of the equivalent capacitance C_{eq} is found from (2.23), (2.24), and (2.25), yielding

$$C_{eq} = \frac{(C_1 + C_2)k_L + C_1 - \sqrt{[(C_1 + C_2)k_L - C_1]^2 + 4k_L C_1^2}}{2}, \tag{2.26}$$

where $k_L = L_2/L_1$.

2.4.1.2 Minimum Transistor Gain for Oscillation Startup

To find the requirements with regard to the transistor parameters to achieve oscillation, firstly, the voltage gain from drain to source must be calculated. Using the small-signal equivalent circuit of Fig. 2.19b and assuming that the Q values of the LC tanks are high at the oscillation frequency ω_o, the relationship between the source and drain voltages is

$$\frac{v_d}{v_s} = a \cong -\frac{L_1}{L_2}\left(1 - \omega_o^2 L_2 C_2\right) = \frac{C_2}{C_{eq}} - \frac{L_1}{L_2}, \tag{2.27}$$

where v_d and v_s are the small-signal voltages at the source and drain, respectively. The value of a, calculated from (2.26) and (2.27), is given by

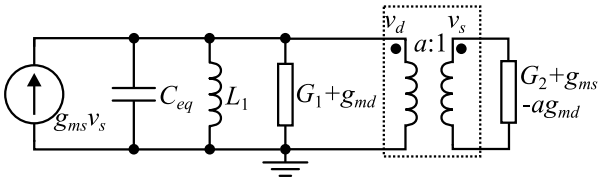


Fig. 2.20 ESCO with capacitive divider modeled as a transformer

$$a = u + \sqrt{u^2 + \frac{L_1}{L_2}}, \tag{2.28}$$

where

$$u = \frac{1}{2}\left(1 + \frac{C_2}{C_1} - \frac{L_1}{L_2}\right). \tag{2.29}$$

To achieve high swing with low supply voltages, the value of a must be relatively close to unity, i.e., $C_2/C_1 \ll 1$. In this case, (2.28) can be approximated as

$$a_{C_2 \ll C_1} = 1 + \frac{C_2/C_1}{1 + L_1/L_2}. \tag{2.30}$$

Using the calculated value of a, the capacitive divider is modeled as a transformer [25], as represented in the small-signal equivalent circuit of the ESCO shown in Fig. 2.20. To achieve oscillations, the transistor must compensate for the losses of the passive components. Reflecting the conductance connected to the secondary winding to the primary winding (Fig. 2.20), the requirement for oscillation is written as.

$$\frac{g_{ms}}{g_{md}} > a + \frac{a^2}{(a-1)}\frac{G_1}{g_{md}} + \frac{1}{(a-1)}\frac{G_2}{g_{md}}. \tag{2.31}$$

The curves in Fig. 2.21 represent the minimum gain g_{ms}/g_{md} calculated from (2.31) for the case in which $G_1 = G_2 = G$.

As is clear from Fig. 2.21, there is an optimum value for the voltage gain a that minimizes the transconductance required for oscillation. The value a_{opt} that minimizes the right-hand side of (2.31) is

$$a_{opt} = 1 + \sqrt{\frac{G_1 + G_2}{G_1 + g_{md}}}. \tag{2.32}$$

From (2.30) and (2.32), after selecting g_{md}, L_1, and L_2, and assuming that the quality factors of the inductors are equal, i.e., $G_1/G_2 = L_2/L_1$, the C_2/C_1 ratio that minimizes the voltage gain required for oscillation is given by

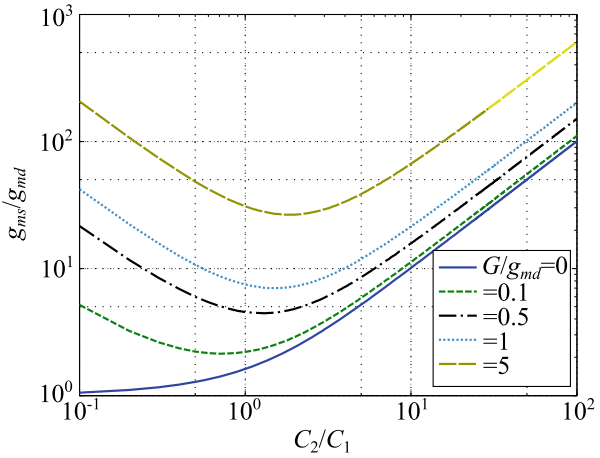


Fig. 2.21 Minimum transistor intrinsic gain to start up oscillations versus C_2/C_1 ratio for $L_1 = L_2$, with G/g_{md} as a parameter

$$\left.\frac{C_2}{C_1}\right|_{opt} = \left(1+\frac{L_1}{L_2}\right)^{3/2}\sqrt{\frac{G_1/g_{md}}{1+G_1/g_{md}}}. \tag{2.33}$$

The substitution of (2.32) into (2.31) yields the optimized minimum value for the intrinsic gain

$$\frac{g_{ms}}{g_{md}} > 1+2\frac{G_1}{g_{md}}+2\sqrt{\left(1+\frac{L_1}{L_2}\right)\left(1+\frac{G_1}{g_{md}}\right)\frac{G_1}{g_{md}}}. \tag{2.34}$$

2.4.1.3 Minimum Supply Voltage for Oscillation Startup

The DC values of the MOSFET terminal voltages are $V_S = V_B = 0$ and $V_G = V_D = V_{DD}$. For a fixed g_{md}, the minimum V_{DS} $(= V_{DD})$ is reached by combining the equation of the minimum transistor gain and the expression for the drain-source voltage (V_{DS}) provided in Chap. 1, which, along with $G_1/G_2 = L_2/L_1$, yields

$$\begin{aligned} V_{DD,min} = {} & \frac{\phi_t^2}{2I_S}g_{md}\left[2\frac{G_1}{g_{md}}+2\sqrt{\left(1+\frac{L_1}{L_2}\right)\left(1+\frac{G_1}{g_{md}}\right)\frac{G_1}{g_{md}}}\right] \\ & +\phi_t\ \ln\left[1+2\frac{G_1}{g_{md}}+2\sqrt{\left(1+\frac{L_1}{L_2}\right)\left(1+\frac{G_1}{g_{md}}\right)\frac{G_1}{g_{md}}}\right]. \end{aligned} \tag{2.35}$$

For $C_2/C_1 \ll 1$, the MOSFET operation in the subthreshold region and negligible losses in the inductors, (2.30) and (2.35) can be combined to obtain the limit for the minimum supply voltage of the ESCO as

$$V_{DD,lim} = \phi_t \ln(a) = \phi_t \ln\left(1 + \frac{C_2/C_1}{1 + L_1/L_2}\right). \tag{2.36}$$

Theoretically, as (2.36) shows, the ESCO can oscillate at ultra-low supply voltages. In practice, however, the unavoidable losses, parasitic capacitance of the drain node, and operation of the transistor in moderate or strong inversion will contribute to increasing the value of V_{DD} given by (2.36). Some simulated and experimental results for the minimum supply voltage, including losses and considering the transistor operation in moderate inversion, will be given in Sect. 2.3.2.

2.4.2 Enhanced-Swing Colpitts Ocillator Design and Experimental Results

To demonstrate the feasibility of the operation of the ESCO for supply voltages under 100 mV, two designs are presented, one using off-the-shelf devices with high-quality inductors and capacitors and the other with fully integrated components.

2.4.2.1 Design of an Enhanced-Swing Colpitts Oscillator with Off-the-Shelf Components

The ESCO prototype shown in Fig. 2.22a was built with off-the-shelf inductors and capacitors and a zero-VT transistor of the 130-nm CMOS technology [9]. The main transistor parameters are shown in Table 2.4. The oscillator circuit, together with the values for the components employed in the experiment, are shown in Fig. 2.22b. Inductors with nominal inductance of 10 mH and a quality factor of around 90 were chosen. Using Eq. (2.26), for $C_1 \gg C_2$, the approximate value for C_2 was found ($\approx$ 440 pF), which provides an oscillation frequency of around 110 kHz. For the experiment, we employed nominal values of 3.6, 2.0, 1.8, and 1.54 nF for C_1. Transistor capacitances, measured for $V_G = V_D = 20$ mV and $V_S = 0$, are negligible in comparison with C_1 and C_2. The quality factors of the capacitors are around 2000. Passive devices were characterized at 100 kHz, and their values, along with the parasitic losses, are given in Fig. 2.22.

With $C_1 = 1.54$ nF, the prototype shown in Fig. 2.22 oscillates at around 108 kHz. The experimental waveform of the drain voltage is shown in Fig. 2.23 for $V_{DD} = 15$ mV.

The simulation results for the minimum supply voltage required for the achievement of oscillations are reported in Fig. 2.24. Note that the losses of the passive components do not play an important role in this case, except for very low C_2/C_1

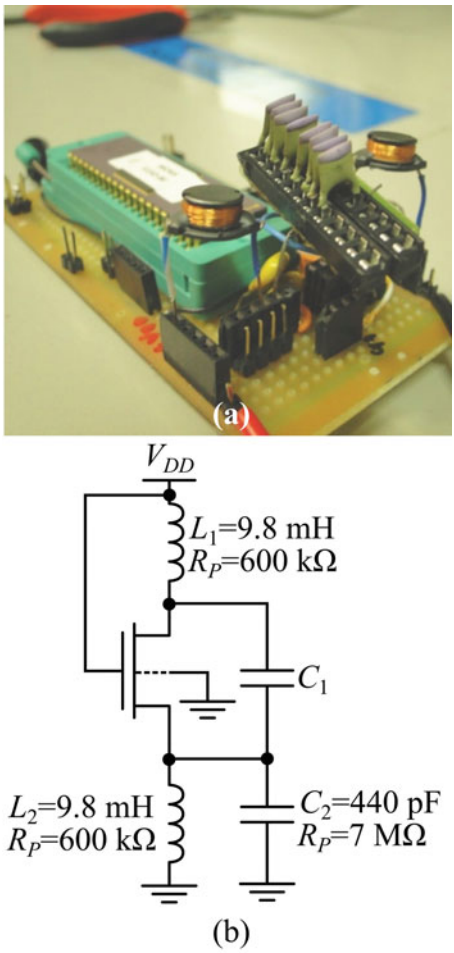


Fig. 2.22 (**a**) Photograph of the ESCO prototype with zero-VT transistor in the 130-nm technology and (**b**) schematic of the ESCO with values for the passive components characterized at 100 kHz. Values for C_1 are given in the text

ratios (i.e., below approximately 10^{-2}). Four experimental values, $C_2/C_1 = 0.12$, 0.22, 0.25, and 0.29, represented by the triangles, show acceptable agreement with the simulation results. For $C_2/C_1 = 0.12$, the prototype sustained oscillations at a supply voltage of only 15 mV, whereas the simulation indicated a supply voltage of 8 mV. The dotted line indicates the theoretical limit for operation in weak inversion.

Figure 2.25 shows the oscillation amplitude as a function of the supply voltage. The curves represent the simulated values, whereas the symbols indicate the experimental results.

2.4.2.2 Design of a Fully Integrated Enhanced-Swing Colpitts Oscillator

Based on the analysis presented in Sect. 2.3.1, a fully integrated Colpitts oscillator was designed for operation at 800 MHz [8]. The oscillator employs a wide zero-VT

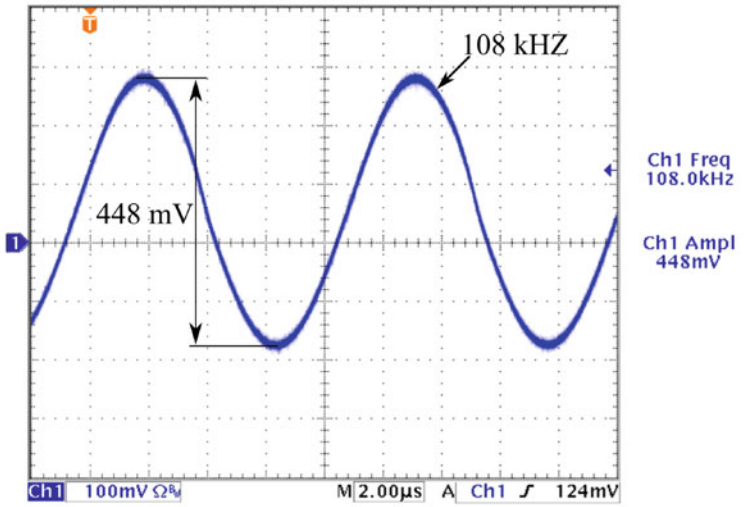


Fig. 2.23 Drain voltage waveform for $V_{DD} = 15$ mV, $C_1 = 1.54$ nF, $C_2 = 0.44$ nF, and temperature of around 23 °C

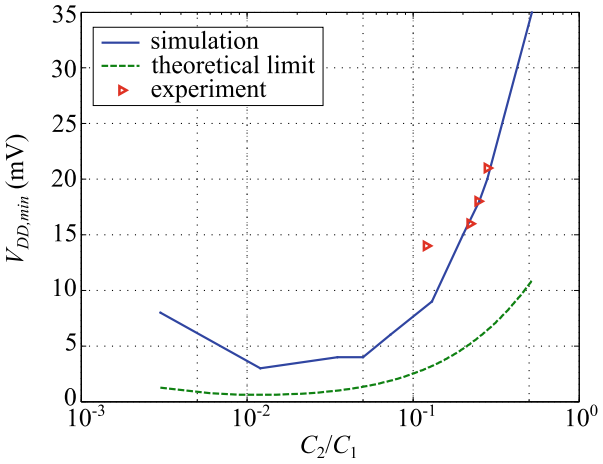


Fig. 2.24 $V_{DD,min}$ versus C_2/C_1 for the ESCO in Fig. 2.22. Details for the values of C_1 and C_2 are given in the text

transistor ($W/L = 300 \times 5$ µm/420 nm) to provide enough drive capability to compensate for the inductor losses.

Once the inductors and transistor parameters are known, the capacitive feedback can be readily determined from (2.33), which, in this design, yields an optimum capacitive ratio of approximately 0.7. From (2.25) and (2.26), after some adjustments to account for the parasitic capacitances of the layout, the values of C_1 and C_2 were set to 6 pF and 3.5 pF, respectively.

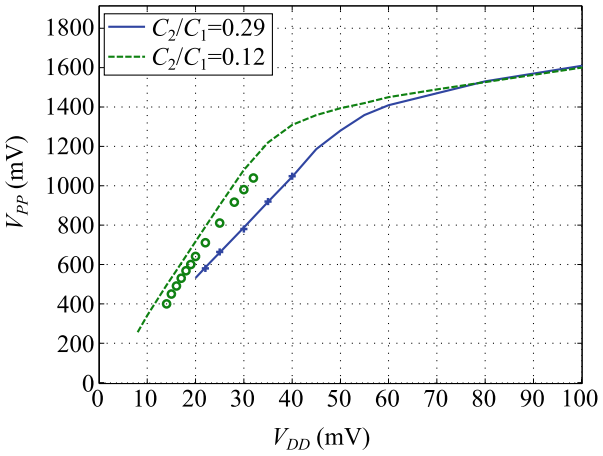


Fig. 2.25 Simulated (curves) and experimental (symbols) peak-to-peak oscillation amplitude at the drain versus supply voltage for $C_2/C_1 = 0.29$ and 0.12

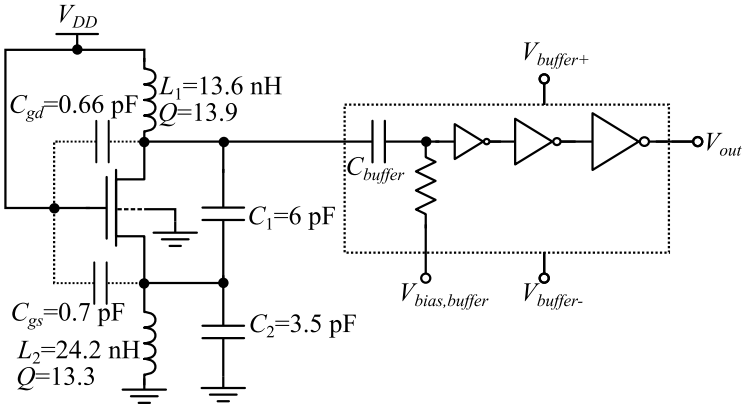


Fig. 2.26 Schematic diagram of the fully integrated ESCO and the voltage buffer

A schematic diagram of the oscillator and the voltage buffer is shown in Fig. 2.26. A tapered inverter chain was chosen for the buffer, minimizing the capacitive load at the oscillator output. The inductor parameters, simulated at 800 MHz, and the MOSFET capacitances, extracted from Cadence EDA tools, are indicated in Fig. 2.26. The micrograph of the chip in the IBM 130-nm technology is shown in Fig. 2.27.

The setup used for the measurements is shown in Fig. 2.28. The fully integrated ESCO was able to oscillate from supply voltages of around 86 mV, while the calculation based on (2.35) gives a minimum supply voltage of 56 mV. The calculated values were taken from the simulated parameters detailed in Fig. 2.26, without taking into account the parasitic elements introduced by the layout.

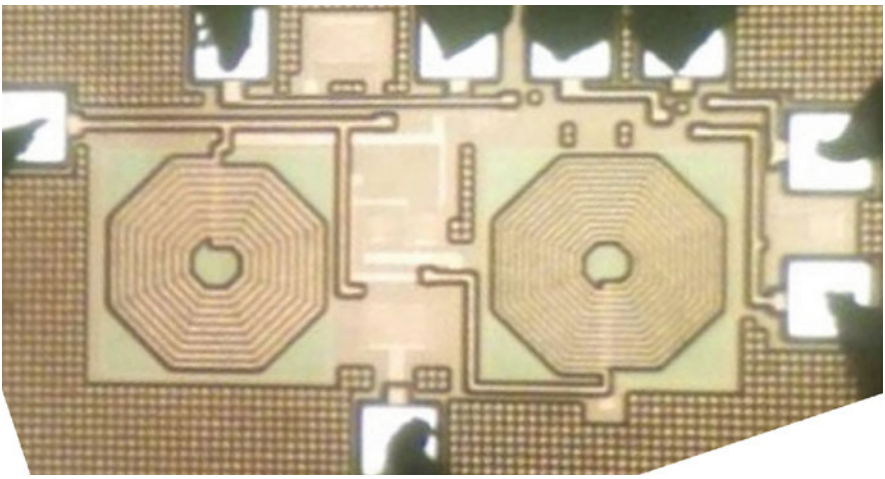


Fig. 2.27 Micrograph of the fully integrated ESCO built in the IBM 130-nm technology

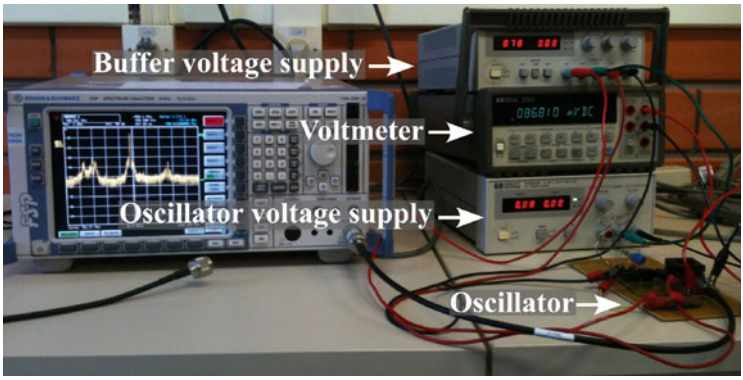


Fig. 2.28 Setup used for the measurements of the fully integrated ESCO, operating with $V_{DD} = 86$ mV

2.5 Comparison Between the Circuits

This chapter presented an analysis of three oscillator topologies appropriate for ultra-low-voltage operation. The main results as well as some design characteristics are summarized in Table 2.3. Two of the topologies described, the ESCO and the ES-XCO, can operate from supply voltages below the thermal voltage. On the other hand, the inductive ring oscillator is a very convenient topology for applications that require minimum supply voltages of the order of $2kT/q$ (two times the thermal voltage) and fewer components.

Table 2.3 Comparison between the XCO, ES-XCO, and ESCO topologies

	XCO	ES-XCO	ESCO
$V_{DD,lim}/\phi_t$	$\ln(1+n)$	$\ln\left(1+\frac{nL_1}{L_1+L_2}\right)$	$\ln\left(1+\frac{C_2/C_1}{1+L_1/L_2}\right)$
ω_o	$1/\sqrt{LC}$	$1/\sqrt{C(L_1+L_2)}$	$1/\sqrt{C_{eq}L_1}$
Design	Easiest: "ratio-less" design	Intermediate: L_1/L_2 ratio	Hardest: L_1/L_2 and C_2/C_1 ratios
Area	Intermediate, at least two inductors	Large, at least four inductors	Intermediate, two inductors and two capacitors

Table 2.4 Comparison between the ULV oscillators designed in this study

	Devices		Experimental
Fully integrated XCO	$W/L = 30 \times 6\mu m/0.42\ \mu m$		$V_{DD,min} = 46$ mV
	$L = 108$ nH	$Q = 7.9$	$V_{PP} = 68$ mV
			$f_{osc} = 410$ MHz
			$I_{DC} = 0.26$ mA
	*L simul. at 460 MHz; V_{PP}, I_{DC} meas. at $V_{DD} = 50$ mV		
Fully integrated ES-XCO	$W/L = 25 \times 20\mu m/0.42\ \mu m$		$V_{DD,min} = 30$ mV
	$L_1 = 19$ nH	$L_2 = 80$ nH	$V_{PP} = 290$ mV
	$Q_1 = 8.7$	$Q_2 = 7.9$	$f_{osc} = 340$ MHz
			$I_{DC} = 0.86$ mA
	*L simul. at 400 MHz; V_{PP}, I_{DC} meas. at $V_{DD} = 50$ mV		
ES-XCO off-the-shelf	$W/L = 300 \times 5\mu m/0.42\ \mu m$		$V_{DD,min} = 3.5$ mV
	$L_1 = 4.6\ \mu$H	$L_2 = 1.2$ mH	$V_{PP} = 1.44$ V
	$Q_1 = 55$	$Q_2 = 60$	$f_{osc} = 1.1$ MHz
	*L simul. at 1 MHz; V_{PP}, meas. at $V_{DD} = 20$ mV		
Fully integrated ESCO	$W/L = 300 \times 5\mu m/0.42\ \mu m$		$V_{DD,min} = 86$ mV
	$L_1 = 13.6$ nH	$L_2 = 24.2$ nH	$f_{osc} = 706$ MHz
	$Q_1 = 13.9$	$Q_2 = 13.3$	$I_{DC} = 3$ mA
	$C_1 = 6$ pF	$C_2 = 3.5$ pF	
	*L simul. at 800 MHz; I_{DC} meas. at $V_{DD} = 100$ mV		
ESCO off-the-shelf	$W/L = 500 \times 5\mu m/0.42\ \mu m$		$V_{DD,min} = 15$ mV
	$L_1 = 9.8$ mH	$L_2 = 9.8$ nH	$V_{PP} = 640$ mV
	$Q_1 = 90$	$Q_2 = 90$	$f_{osc} = 110$ kHz
	$C_1 = 1.54$ nF	$C_2 = 440$ pF	
	*L simul. at 100 kHz; V_{PP}, meas. at $V_{DD} = 20$ mV		

Table 2.4 summarizes the main characteristics and experimental results of the different realizations. It should be noted that for both ES-XCO and the ESCO, high ratios between the values of the energy storage devices can lead to very low $V_{DD,min}$, which is feasible with discrete components but can be hard to achieve in integrated implementations.

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Chapter 3
Rectifier Analysis for Ultra-Low-Voltage Operation

3.1 Introduction to Ultra-Low-Voltage Rectifiers

Rectifiers are commonly used together with ultra-low-voltage (ULV) oscillators [1, 2], such as those analyzed in Chap. 2, to build step-up voltage converters that can boost voltages as low as the thermal voltage kT/q to the higher levels ($V_{DD} > 500$ mV) required to supply electronic devices. Although this type of converter is usually associated with low efficiency, it can be fully integrated and can start up from ultra-low voltages, making it a feasible option to provide cold startup in a complete energy-harvesting interface [3].

In the context of this work, the voltage levels can be far lower than 100 mV; thus, the approximation of constant forward voltage of the diode, usually taken as some tens of mV for silicon diodes, is not appropriate. In this chapter, we use a physics-based (Shockley) diode model valid for extremely low voltages [4, 5] to analyze the main characteristics of rectifiers, such as the Dickson charge pump (DCP) and the voltage multiplier. Expressions for the output voltage, power conversion efficiency, and input resistance are derived, allowing the design and optimization of rectifiers based on the diode parameters and specifications, such as the signal amplitude and the load current. These models can be used in the co-design of oscillators and rectifiers, as described in Chap. 4, to minimize the startup voltages of voltage converters.

3.1.1 The Basic Half-Wave Rectifier

Before introducing the ULV rectifier model, we analyze the basic half-wave rectifier shown in Fig. 3.1, which forms the basis for the more complex rectifiers described in the following sections. To simplify the analysis, we assume that:

R. L. Radin et al., *Ultra-low Voltage Circuit Techniques for Energy Harvesting*,
Analog Circuits and Signal Processing, https://doi.org/10.1007/978-3-031-04492-2_3

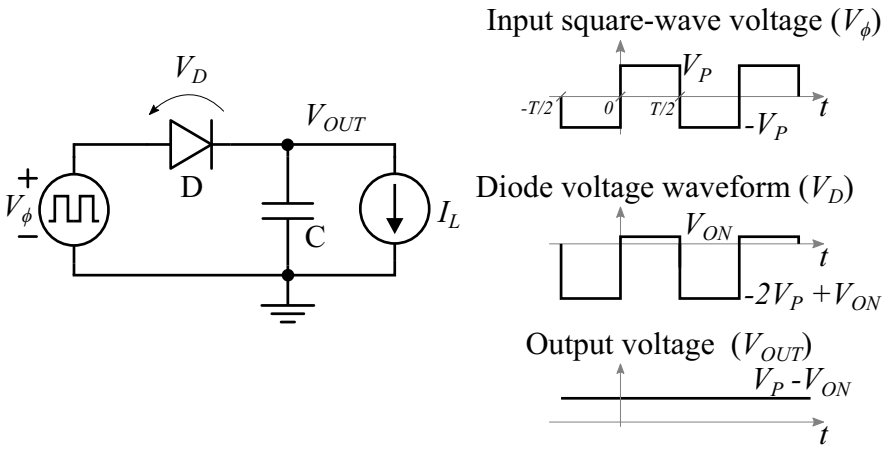

Fig. 3.1 Basic half-wave rectifier along with the voltage waveforms

(i) the circuits operate in a steady state;
(ii) the capacitors have an infinite quality factor and are large enough to ensure that the AC voltage across them is much smaller than the thermal voltage;
(iii) the stray capacitances to ground are much smaller than the coupling capacitances;
(iv) the load current is constant.

For the sake of simplicity, we first assume that the input voltage is a square wave.

In this analysis, the diode $I \times V$ relation is modeled by the Shockley equation given by

$$I_D = I_{SAT}\left(e^{V_D/n\phi_t} - 1\right), \tag{3.1}$$

where I_{SAT} is the diode saturation current, n is the diode ideality factor, ϕ_t is the thermal voltage, and V_D is the voltage across the diode.

Under steady-state operation, the average diode current in Fig. 3.1 over a complete cycle of the oscillation is equal to the load current I_L [4], i.e.,

$$I_L = \frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} I_D dt. \tag{3.2}$$

Assuming that the rectifier is connected to a square-wave voltage generator, as in Fig. 3.1, the voltage across the diode D can be calculated using the Kirchhoff Voltage Law (KVL), resulting in the waveform also presented in Fig. 3.1. Therefore, expression (3.2) can be written as

$$\left(1+\frac{I_L}{I_{SAT}}\right)T=\int_{-\frac{T}{2}}^{0}e^{\left(\frac{V_{ON}-2V_P}{n\phi_t}\right)}dt+\int_{0}^{\frac{T}{2}}e^{\left(\frac{V_{ON}}{n\phi_t}\right)}dt. \tag{3.3}$$

From (3.3), the diode forward voltage drop can be expressed as

$$V_{ON}=V_P-n\phi_t\ln\left[\frac{\cosh\left(V_P/n\phi_t\right)}{1+I_L/I_{SAT}}\right]. \tag{3.4}$$

As can be seen in expression (3.4), the diode forward voltage drop is a function of the peak amplitude of the signal applied to the rectifier, the load current, and the diode parameters (n and I_{SAT}). For the case of $V_P/n\phi_t \gg 1$, Eq. (3.4) can be simplified to

$$V_{ON}\cong n\phi_t\ln 2(1+I_L/I_{SAT}). \tag{3.5}$$

Therefore, the half-wave rectifier circuit acts as a peak detector with a usually small error given by (3.5).

Once the diode forward voltage drop is found, the output voltage of the half-wave rectifier can be calculated as

$$V_{OUT}=V_P-V_{ON}=n\phi_t\ln\left[\frac{\cosh\left(V_P/n\phi_t\right)}{1+I_L/I_{SAT}}\right]. \tag{3.6}$$

The curves of the normalized output voltage of the half-wave rectifier are plotted in Fig. 3.2 using expression (3.6).

Expression (3.4), used to determine the diode forward voltage drop, can be applied to calculate the characteristics of other types of rectifiers such as the DCP and the voltage multiplier, which are described in the next chapter.

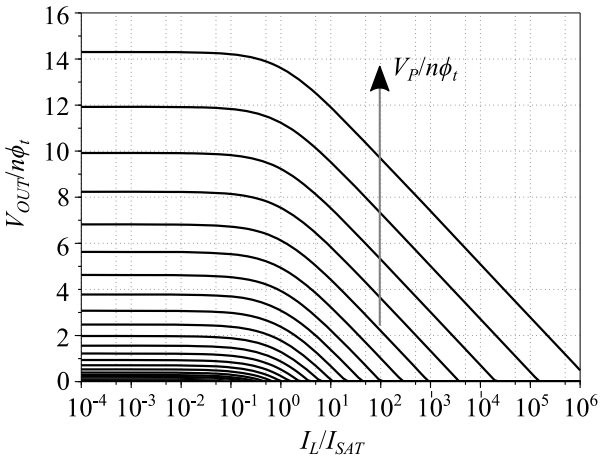

Fig. 3.2 Theoretical curves of the half-wave rectifier output voltage ($V_P/n\phi_t$ is a logarithmically spaced vector ranging from 0.1 to 15)

3.1.1.1 The Ripple of the Half-Wave Rectifier

Let us now assume a finite capacitor for calculation of the voltage ripple. For the capacitor discharge, the current calculated by the Kirchhoff Current Law (KCL) is given by

$$I_C \cong -(I_L + I_{SAT}), \tag{3.7}$$

where I_{SAT} stands for the diode current leakage. The approximation of (3.7) is valid for $V_P/n\phi_t \gg 1$. In the time interval from $-T/2$ to 0, the voltage variation ΔV across the capacitor is calculated as

$$\Delta V = -\frac{1}{C}\int_{-\frac{T}{2}}^{0}(I_L + I_{SAT})dt = -\frac{(I_L + I_{SAT})T}{2C}. \tag{3.8}$$

The percentage ripple voltage at the output is

$$\frac{\Delta V}{V_{OUT}} = 100\frac{(I_L + I_{SAT})T}{2CV_{OUT}}. \tag{3.9}$$

For a given specification of the percentage ripple of the half-wave rectifier, expression can be used to calculate the output capacitance.

3.2 The Dickson Charge Pump

The basic operation of a charge pump can be understood with the help of the basic voltage doubler shown in Fig. 3.3. The switches S_1 and S_2 are controlled by a clock signal that sets two alternating phases of operation. During phase ϕ_1, S_1 is closed and S_2 is open; thus, the capacitor C_1 is charged with C_1V_{DD}. During phase ϕ_2, only S_2 is closed, and charge redistribution between C_1 and C_2, which are now in series, occurs. For the ideal and unloaded circuit of Fig. 3.3 and assuming that $V_{OUT}(0) = 0$, after the first clock cycle, $V_{OUT} = 2V_{DD}C_1/(C_1 + C_2)$. After a few clock cycles, the system reaches a steady state, and V_{OUT} tends towards $2V_{DD}$.

The Dickson charge pump shown in Fig. 3.4 has the same principle of operation as the voltage doubler, in which capacitors are used to transfer charges to the output, providing voltage boosting. Assuming initially that the forward voltage drop across each diode is the same, the DCP output voltage in a steady state is given [6, 7] by

$$V_{OUT} = V_{IN} + 4V_P - 3V_{ON}, \tag{3.10}$$

where V_{ON} is the diode forward voltage drop, and V_P is the peak voltage of the clock signal.

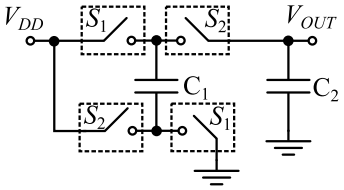

Fig. 3.3 Basic voltage doubler

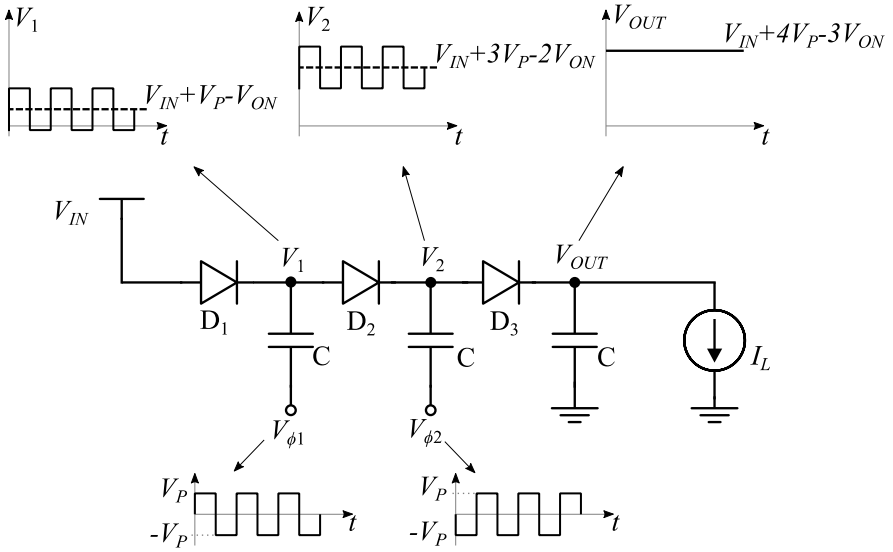

Fig. 3.4 Dickson charge pump along with an indication of the nodal voltages

Although the result obtained in (3.10) gives us some idea regarding the output voltage of the DCP, the conventional approach assuming a constant forward voltage drop over the diodes is not applicable for ULV operation because it does not take into account the dependence of V_{ON} on both the diode parameters and the load current. Thus, to analyze the DCP for input voltages down to the order of the thermal voltage kT/q or even less, a converter model, which includes both the load current and the more realistic exponential current-voltage characteristic of the diode, is derived [8–10].

3.2.1 *Analysis of the Dickson Charge Pump*

A schematic of the DCP with the voltage waveforms across the diodes for steady-state operation is shown in Fig. 3.5. The voltage waveforms across D_1 and D_N differ from those across the intermediate diodes because one of the terminals of both the

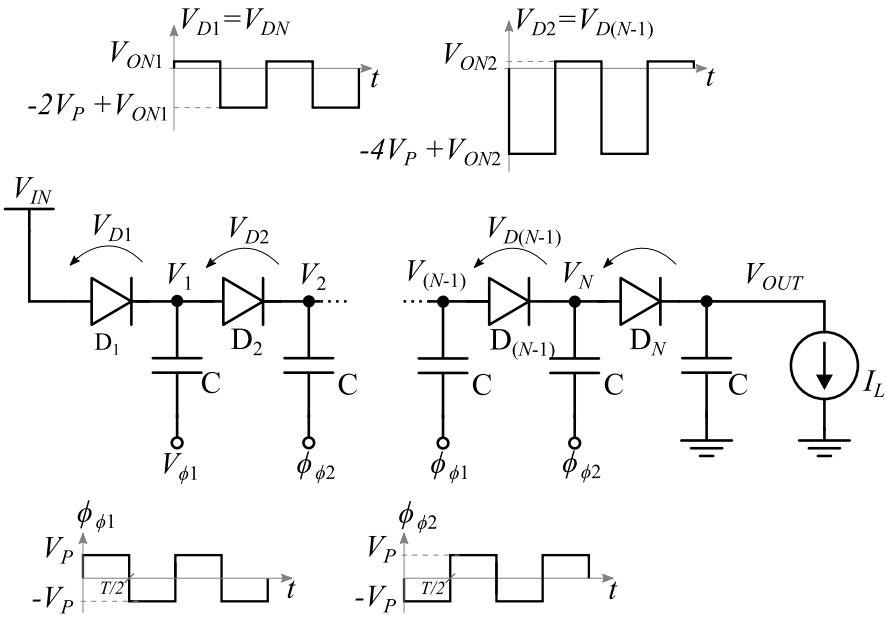

Fig. 3.5 Dickson charge pump and voltage waveforms across the diodes

leftmost and rightmost diodes is connected to the DC nodes (V_{IN} and V_{OUT}, respectively). For this reason, the forward voltage drops across D_1 and D_N are the same ($V_{ON1} = V_{ON,N}$). For the other diodes, the forward voltage drop across them will be the same ($V_{ON2} = \ldots = V_{ON,N-1}$). Thus, the DC output voltage of the DCP [8] is

$$V_{OUT} = V_{IN} + (N-1)2V_P - 2V_{ON1} - (N-2)V_{ON2}, \tag{3.11}$$

where N is the number of diodes.

To calculate the forward voltage across the diodes, V_{ON1} and V_{ON2}, we apply the same method used to find (3.4). Because the average value of the diode current over an oscillation cycle is equal to I_L (see Eq. 3.2), the forward voltage drops V_{ON1} and V_{ON2} across D_1 and D_2 (Fig. 3.5) are calculated, respectively, by

$$\left(1+\frac{I_L}{I_{SAT}}\right)T = \int_{-\frac{T}{2}}^{0} e^{\left(\frac{V_{ON1}}{n\phi_t}\right)}dt + \int_{0}^{\frac{T}{2}} e^{\left(\frac{V_{ON1}-2V_P}{n\phi_t}\right)}dt, \tag{3.12}$$

$$\left(1+\frac{I_L}{I_{SAT}}\right)T = \int_{-\frac{T}{2}}^{0} e^{\left(\frac{V_{ON2}}{n\phi_t}\right)}dt + \int_{0}^{\frac{T}{2}} e^{\left(\frac{V_{ON2}-4V_P}{n\phi_t}\right)}dt, \tag{3.13}$$

resulting in

$$V_{ON1} = V_P - n\phi_t \ln\left[\frac{\cosh\left(V_P/n\phi_t\right)}{1 + I_L/I_{SAT}}\right], \tag{3.14}$$

$$V_{ON2} = 2V_P - n\phi_t \ln\left[\frac{\cosh\left(2V_P/n\phi_t\right)}{1 + I_L/I_{SAT}}\right]. \tag{3.15}$$

Substituting (3.14) and (3.15) into (3.11) yields

$$V_{OUT} = V_{IN} + 2n\phi_t \ln\left[\frac{\cosh\left(V_P/n\phi_t\right)}{1 + I_L/I_{SAT}}\right] + (N-2)n\phi_t \ln\left[\frac{\cosh\left(2V_P/n\phi_t\right)}{1 + I_L/I_{SAT}}\right]. \tag{3.16}$$

For the case of $V_P/n\phi_t \gg 1$, Eq. (3.16) can be simplified to

$$V_{OUT} = V_{IN} + 2V_P(N-1) - Nn\phi_t \ln 2(1 + I_L/I_{SAT}). \tag{3.17}$$

The output voltage calculated with (3.16) is plotted in Fig. 3.6 as a function of the normalized load current I_L/I_{SAT}, with the number of stages as a parameter, for a peak-to-peak input voltage equal to 180 mV. In this figure, $V_{IN} = 30$ mV and $n\phi_t = 25.7$ mV.

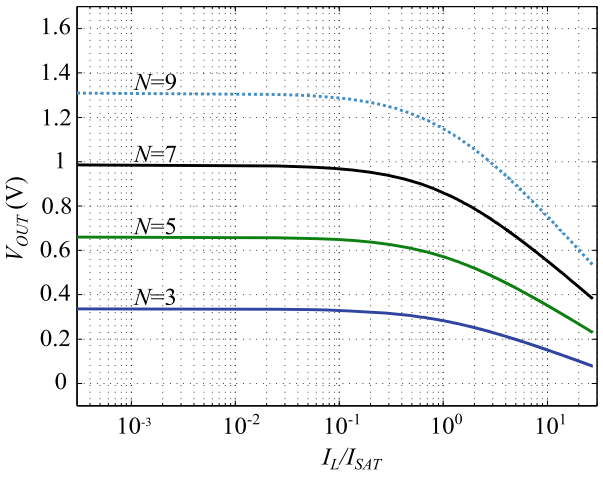

Fig. 3.6 Output voltage (V_{OUT}) vs. the load current normalized to the saturation current (I_L/I_{SAT}) (N ranges from 3 to 9, $V_{IN} = 30$ mV and $V_P = 90$ mV)

3.2.2 Dickson Charge Pump Power Conversion Efficiency

The power conversion efficiency is defined as

$$\eta_{CONV} = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}}. \tag{3.18}$$

Recalling that the voltage waveforms across D_1 and D_N differ from those across the intermediate diodes (see Fig. 3.5), the power loss (P_{LOSS}) of the DCP is given by

$$P_{LOSS} = 2P_{D1} + (N-2)P_{D2}, \tag{3.19}$$

where P_{D1} stands for the power losses of D_1 and D_N, and P_{D2} represents the power losses of the intermediate diodes. The detailed analysis provided in the Appendix gives the following results for P_{D1} and P_{D2}

$$P_{D1} = (I_{SAT} + I_L)V_P \tanh\left(\frac{V_P}{n\phi_t}\right) - I_L n\phi_t \ln\left[\frac{\cosh(V_P/n\phi_t)}{1 + I_L/I_{SAT}}\right], \tag{3.20}$$

$$P_{D2} = (I_{SAT} + I_L)2V_P \tanh\left(\frac{2V_P}{n\phi_t}\right) - I_L n\phi_t \ln\left[\frac{\cosh(2V_P/n\phi_t)}{1 + I_L/I_{SAT}}\right]. \tag{3.21}$$

Because $P_{OUT} = V_{OUT} I_L$, the input power of an N-stage DCP can be calculated using (3.20) and (3.21), yielding

$$P_{IN} = I_L V_{IN} + (I_{SAT} + I_L)2V_P\left[\tanh\left(\frac{V_P}{n\phi_t}\right) + (N-2)\tanh\left(\frac{2V_P}{n\phi_t}\right)\right]. \tag{3.22}$$

The power conversion efficiency (PCE) of the N-stage DCP can be calculated as

$$\eta_{CONV} = \frac{V_{IN} + 2n\phi_t \ln\left[\frac{\cosh(V_P/n\phi_t)}{1+I_L/I_{SAT}}\right] + (N-2)n\phi_t \ln\left[\frac{\cosh(2V_P/n\phi_t)}{1+I_L/I_{SAT}}\right]}{V_{IN} + \left(1 + \frac{I_{SAT}}{I_L}\right)2V_P\left[\tanh\left(\frac{V_P}{n\phi_t}\right) + (N-2)\tanh\left(\frac{2V_P}{n\phi_t}\right)\right]}. \tag{3.23}$$

For the case of $V_P/n\phi_t \gg 1$, and $V_{IN} = 0$, expression (3.23) can be written as

$$\eta_{CONV} \cong \frac{(N-1) - \frac{Nn\phi_t}{V_P}\ln 2(1 + I_L/I_{SAT})}{(N-1)\left(1 + \frac{I_{SAT}}{I_L}\right)}. \tag{3.24}$$

Figure 3.7 shows the theoretical PCE (3.23) as a function of the normalized load current I_L/I_{SAT}. As can be seen, the PCE is strongly dependent on the load current.

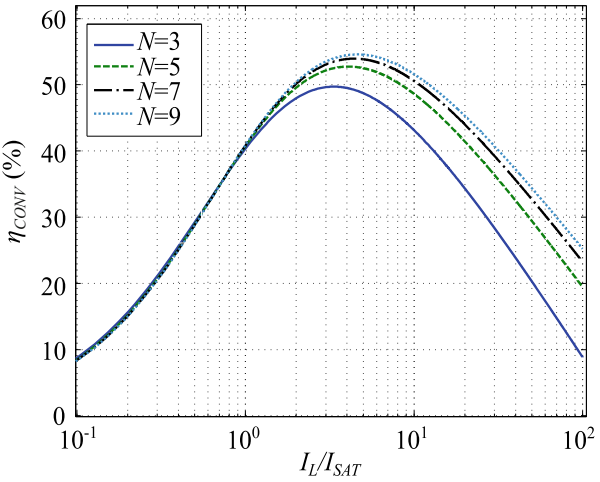

Fig. 3.7 Theoretical power conversion efficiency vs I_L/I_{SAT} ($V_{IN} = 50$ mV, $V_P = 2V_{IN}$, $n\phi_t = 25.7$ mV)

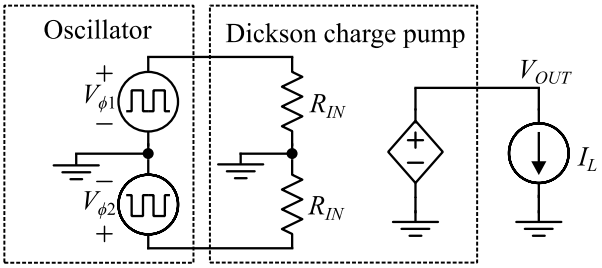

Fig. 3.8 Equivalent electrical circuit of the DCP including the resistance seen by the oscillator

Also, for a given I_L and V_P, there is an optimum value for the diode saturation current that maximizes the power conversion efficiency, which is given [8] by

$$I_{SAT,opt} = I_L \frac{Nn\phi_t}{V_{OUT}}. \tag{3.25}$$

Expression (3.25) was derived assuming $V_{IN} = 0$ V. This is a reasonable approximation, since in general $V_{IN} \ll V_{OUT}$, and the contribution of V_{IN} to the output voltage, as given by expression (3.16), is generally low.

3.2.3 Dickson Charge Pump Input Resistance

In energy-harvesting applications, the DCP is generally connected to a ULV oscillator to realize the voltage conversion, as shown in Fig. 3.8. In this configuration, the input of the DCP loads the oscillator, affecting both the oscillation amplitude and the converter output voltage. For the equivalent circuit of Fig. 3.8, the input resistance of the DCP is given by.

$$R_{IN} = \frac{V_P^2}{P_{IN}/2}. \tag{3.26}$$

Substituting (3.22) into (3.26) and disregarding the term related to the DC input voltage ($V_{IN} = 0$) yield

$$R_{IN} = \frac{V_P}{(I_{SAT} + I_L)\left[\tanh\left(\frac{V_P}{n\phi_t}\right) + (N-2)\tanh\left(\frac{2V_P}{n\phi_t}\right)\right]}. \tag{3.27}$$

For $V_P/n\phi_t \gg 1$, we can simplify (3.27) to

$$R_{IN} = \frac{V_P}{(I_{SAT} + I_L)(N-1)}. \tag{3.28}$$

The expressions for V_{OUT}, PCE and R_{IN} of the Dickson charge pump for a sine wave signal are presented in Sect. 3.4.

3.3 The Voltage Multiplier

Voltage multipliers are useful AC-DC converters employed to boost the low voltage levels provided by AC sources. A single stage of the basic half-wave multiplier, known as voltage doubler, is shown in Fig. 3.9. Note that this circuit is composed of a clamper circuit followed by a half-wave rectifier.

In steady state, the average current through the capacitors is null; thus, the average current through the diodes is equal to the load current (I_L). For identical diodes, the output voltage of the circuit can be written as $V_{OUT} = 2V_P - 2V_{ON}$. The voltage drop V_{ON} across the diodes can be calculated using a similar method to that used for the derivation of (3.4), which allows the output voltage to be written as

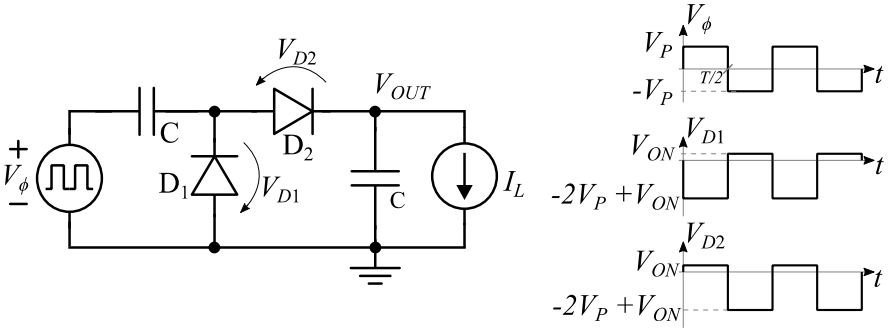

Fig. 3.9 Schematic of a single-stage voltage doubler and the voltage waveform across the devices

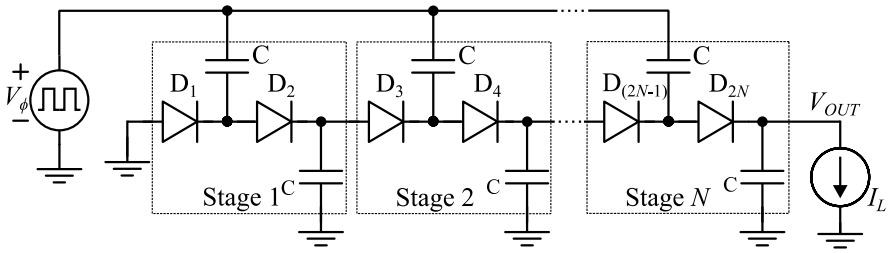

Fig. 3.10 Schematic of N-stage voltage multiplier

$$V_{OUT} = 2n\phi_t \ln\left[\frac{\cosh\left(V_P/n\phi_t\right)}{1 + I_L/I_{SAT}}\right]. \tag{3.29}$$

Expression (3.29) can be extrapolated to the N-stage voltage multiplier shown in Fig. 3.10 [4], yielding

$$V_{OUT} = 2Nn\phi_t \ln\left[\frac{\cosh\left(V_P/n\phi_t\right)}{1 + I_L/I_{SAT}}\right], \tag{3.30}$$

which, for $V_P/n\phi_t \gg 1$, becomes

$$V_{OUT} = 2N[V_P - n\phi_t \ln 2(1 + I_L/I_{SAT})],$$

3.3.1 Power Conversion Efficiency of the Voltage Multiplier

Because all diodes of the voltage multiplier have the same voltage waveform across them (Fig. 3.9) and the average current through each diode is equal to I_L, the power loss in each diode (P_D) is the same. Thus, the power conversion efficiency of the voltage multiplier is given by

$$\eta_{CONV} = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + 2NP_D}. \tag{3.31}$$

Following the procedure detailed in the Appendix, the power loss in each diode of the voltage multiplier is given by

$$P_D = (I_{SAT} + I_L)V_P \tanh\left(\frac{V_P}{n\phi_t}\right) - I_L n\phi_t \ln\left[\frac{\cosh\left(V_P/n\phi_t\right)}{1 + I_L/I_{SAT}}\right]. \tag{3.32}$$

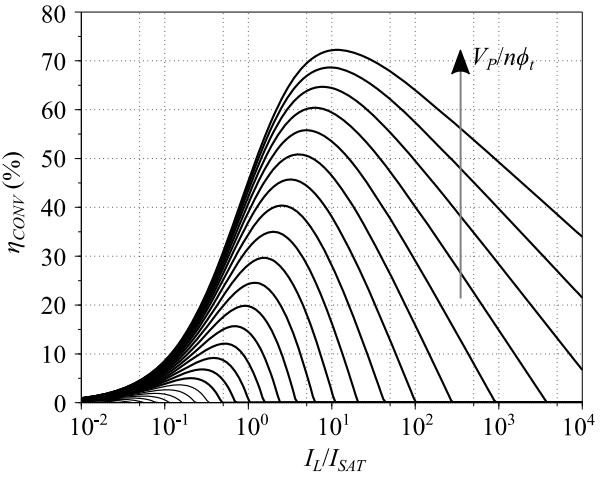

Fig. 3.11 Theoretical power conversion efficiency curves of the *N*-stage voltage multiplier in terms of I_L/I_{SAT} ($V_P/n\phi_t$ is a logarithmically spaced vector ranging from 0.1 to 15)

Therefore, using (3.30) and (3.32), η_{CONV} can be expressed as

$$\eta_{CONV} = \frac{n\phi_t/V_P}{\left(1+\frac{I_{SAT}}{I_L}\right)\tanh\left(\frac{V_P}{n\phi_t}\right)} \ln\left[\frac{\cosh\left(V_P/n\phi_t\right)}{1+I_L/I_{SAT}}\right]. \tag{3.33}$$

Figure 3.11 presents the behavior of the η_{conv} values in terms of I_L/I_{SAT} with $V_P/n\phi_t$ as a parameter. As can be seen, for a given peak amplitude, there is an I_L/I_{SAT} value that maximizes the PCE. The best I_{SAT} value is given [4] by (3.34).

$$I_{SAT,opt} = I_L \frac{2Nn\phi_t}{V_{OUT}}. \tag{3.34}$$

3.3.2 The Voltage Multiplier Input Resistance

The input resistance of the *N*-stage voltage multiplier represented in Fig. 3.12 is expressed as

$$R_{IN} = \frac{V_P^2}{P_{IN}} = \frac{V_P^2}{P_{OUT} + 2NP_D}. \tag{3.35}$$

The substitution of (3.32) into (3.35) yields

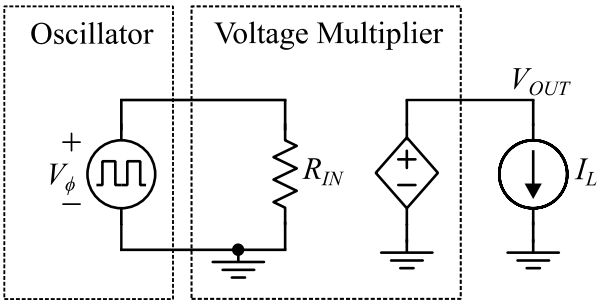

Fig. 3.12 Equivalent electrical circuit of the voltage multiplier including the resistance seen by the oscillator

$$R_{IN} = \frac{V_P}{2N(I_{SAT} + I_L)\tanh\left(\frac{V_P}{n\phi_t}\right)}. \tag{3.36}$$

The design equations of the voltage multiplier for a sine wave are shown in Table 3.1.

3.3.3 *Analysis of the Full-Wave Voltage Multiplier*

The full-wave voltage multiplier shown in Fig. 3.13 is a variation of the half-wave rectifier that can perform voltage conversion from complementary oscillatory signals. This useful variation provides symmetrical loading when connected to an oscillator with complementary outputs, such as the cross-coupled oscillator and the enhanced-swing cross-coupled oscillator analyzed in Chap. 2.

In this configuration, the average current through the diodes is equal to $I_L/2$. Therefore, following the same procedure adopted to find (3.4), we can express the forward voltage drop across the diodes of Fig. 3.13 as

$$V_{ON} = V_P - n\phi_t \ln\left[\frac{\cosh\left(V_P/n\phi_t\right)}{1 + I_L/2I_{SAT}}\right]. \tag{3.37}$$

Because $V_{OUT} = 2V_P - 2V_{ON}$, from (3.37), the output voltage of the single-stage full-wave multiplier of Fig. 3.13 is given by

$$V_{OUT} = 2n\phi_t \ln\left[\frac{\cosh\left(V_P/n\phi_t\right)}{1 + I_L/2I_{SAT}}\right], \tag{3.38}$$

and the output voltage of a full-wave voltage multiplier with multiple stages, obtained by the extrapolation of (3.38), can be expressed as

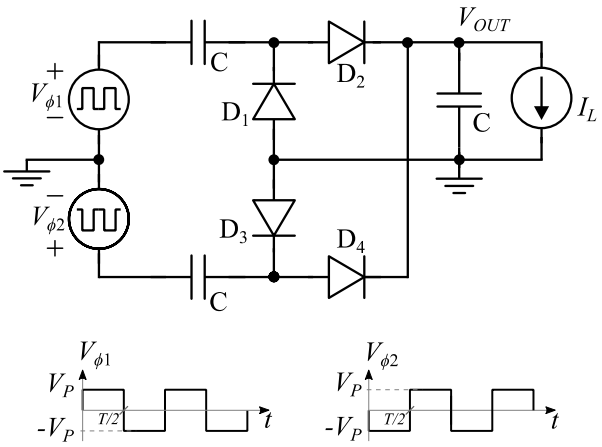

Fig. 3.13 Schematic of the single-stage full-wave voltage multiplier

$$V_{OUT} = 2Nn\phi_t \ln\left[\frac{\cosh\left(V_P/n\phi_t\right)}{1 + I_L/2I_{SAT}}\right]. \tag{3.39}$$

Expressions for the output voltage, efficiency, and input resistance of the full-wave multiplier, considering sine wave signals at the input, are shown in Table 3.1.

3.4 The Equivalence Between Square and Sine-Wave Signals

In the context of this study, where the converters are commonly connected to an LC oscillator, it is convenient to adapt the models previously developed for square-wave inputs for sine-wave inputs. Using the equivalence between square-wave signals of magnitude V_P and sine-wave signals of amplitude V_A demonstrated in [4], we have

$$I_0(V_A/n\phi_t) \rightarrow \cosh\left(V_P/n\phi_t\right) \tag{3.40}$$

and

$$\frac{I_1(V_A/n\phi_t)}{I_0(V_A/n\phi_t)} \rightarrow \tanh\left(V_P/n\phi_t\right), \tag{3.41}$$

where $I_0(z)$ and $I_1(z)$ are the modified Bessel functions of the first kind of order zero and one, respectively. Using (3.40) and (3.41), we can rewrite the equations derived in this chapter for sine-wave signals, as summarized in Table 3.1, where $v_a = V_A/n\phi_t$.

Table 3.1 Main design expressions for the half-wave rectifier, DCP, half-wave voltage multiplier, and full-wave voltage multiplier

Half-wave rectifier	V_{OUT} =	$n\phi_t \ln\left[\frac{I_0(v_a)}{1+I_L/I_{sat}}\right]$
	η_{CONV} =	$\frac{n\phi_t/V_A}{\left(1+\frac{I_{sat}}{I_L}\right)\left[\frac{I_1(v_a)}{I_0(v_a)}\right]} \ln\left[\frac{I_0(v_a)}{1+I_L/I_{sat}}\right]$
	R_{IN} =	$\frac{\left(V_A/\sqrt{2}\right)^2}{P_{in}} = \frac{V_A}{2(I_{sat}+I_L)}\left[\frac{I_0(v_a)}{I_1(v_a)}\right]$
	Optimization	$I_{sat,opt} = I_L \frac{n\phi_t}{V_{OUT}}$
Dickson charge pump	V_{OUT} =	$V_{IN} + 2n\phi_t \ln\left[\frac{I_0(v_a)}{1+I_L/I_{sat}}\right] + (N-2)n\phi_t \ln\left[\frac{I_0(2v_a)}{1+I_L/I_{sat}}\right]$
	η_{CONV} =	$\frac{V_{in}+2n\phi_t \ln\left[\frac{I_0(v_a)}{1+I_L/I_{sat}}\right]+(N-2)n\phi_t \ln\left[\frac{I_0(2v_a)}{1+I_L/I_{sat}}\right]}{V_{in}+\left(1+\frac{I_{sat}}{I_L}\right)2V_A\left[\frac{I_1(v_a)}{I_0(v_a)}+(N-2)\frac{I_1(2v_a)}{I_0(2v_a)}\right]}$
	R_{IN} =	$\frac{\left(V_A/\sqrt{2}\right)^2}{P_{in}/2} = \frac{V_A}{2(I_{sat}+I_L)\left[\frac{I_1(v_a)}{I_0(v_a)}+(N-2)\frac{I_1(2v_a)}{I_0(2v_a)}\right]}$
	Optimization	$I_{sat,opt} = I_L \frac{Nn\phi_t}{V_{OUT}}$
Half-wave voltage multiplier	V_{OUT} =	$2Nn\phi_t \, ln\left[\frac{I_0(v_a)}{1+I_L/I_{sat}}\right]$
	η_{CONV} =	$\frac{n\phi_t/V_A}{\left(1+\frac{I_{sat}}{I_L}\right)\left[\frac{I_1(v_a)}{I_0(v_a)}\right]} \ln\left[\frac{I_0(v_a)}{1+I_L/I_{sat}}\right]$
	R_{IN} =	$\frac{\left(V_A/\sqrt{2}\right)^2}{P_{in}} = \frac{V_A}{4N(I_{sat}+I_L)}\left[\frac{I_0(v_a)}{I_1(v_a)}\right]$
	Optimization	$I_{sat,opt} = I_L \frac{2Nn\phi_t}{V_{OUT}}$
Full-wave voltage multiplier	V_{OUT} =	$2Nn\phi_t \ln\left[\frac{I_0(v_a)}{1+I_L/2I_{sat}}\right]$
	η_{CONV} =	$\frac{n\phi_t/V_A}{\left(1+\frac{2I_{sat}}{I_L}\right)\left[\frac{I_1(v_a)}{I_0(v_a)}\right]} \ln\left[\frac{I_0(v_a)}{1+I_L/2I_{sat}}\right]$
	R_{IN} =	$\frac{\left(V_A/\sqrt{2}\right)^2}{P_{in}/2} = \frac{V_A}{4N(I_{sat}+I_L/2)}\left[\frac{I_0(v_a)}{I_1(v_a)}\right]$

Appendix: Dickson Charge-Pump Diode Power Losses

The power dissipated in the leftmost and rightmost diodes are equal and can be given by

$$P_{D1} = \frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} V_{D1} I_{D1} dt = \frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} V_{D1} I_{SAT}\left(e^{V_{D1}/n\phi_t} - 1\right) dt \tag{3.42}$$

For the voltage waveform of V_{D1} presented in Fig. 3.5, (3.42) can be written as

$$P_{D1} = \frac{1}{T}\int_{-\frac{T}{2}}^{0} V_{ON1} I_{SAT}\left(e^{\frac{V_{ON1}}{n\phi_t}} - 1\right)dt + \frac{1}{T}\int_{0}^{\frac{T}{2}} (V_{ON1} - 2V_P) I_{SAT}\left(e^{\frac{V_{ON1}-2V_P}{n\phi_t}} - 1\right)dt \quad . \tag{3.43}$$

Using (3.14), after some algebra, the value of P_{D1} can be rewritten as

$$P_{D1} = I_L(V_{ON1} - V_P) + (I_{SAT} + I_L)V_P \tanh\left(\frac{V_P}{n\phi_t}\right). \tag{3.44}$$

Finally, combining (3.14) with (3.44) results in the expression of the power loss of D_1 given in (3.20).

To calculate the power dissipated in the intermediate diodes (P_{D2}), the same procedure used to calculate P_{D1} can be followed for the voltage waveform across D_2 in Fig. 3.5.

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Chapter 4
Rectifier Design

4.1 Introduction to Application-Oriented Rectifier Design

Rectifiers are commonly employed in energy-harvesting converters to generate a DC output voltage from AC signals of very low amplitude. Although rectifiers do not have any startup requirements, the output voltage is not regulated, and the conversion efficiency is a function of the amplitude of the input AC signals, which can be very low in typical energy-harvesting applications. Due to these characteristics, rectifiers are commonly used in conjunction with ultra-low-voltage (ULV) oscillators to realize an auxiliary DC-DC converter (cold starter) responsible for generating a temporary V_{DD} (V_{DDCS}) for the startup of the main converter in energy-harvesting interfaces, as represented in Fig. 4.1 [1]. The main converter, which is usually an inductive boost converter, can operate and provide high conversion efficiency even at low input voltage levels, despite not being capable of self-start at low voltage levels. Therefore, an auxiliary cold starter is an indispensable complement to the main converter in a hybrid converter topology such as that shown in Fig. 4.1.

Another common application of rectifiers involves the AC-DC conversion of RF signals of very low amplitude harvested from the environment by small form-factor antennas. In such an application, a matching network is commonly inserted between the antenna and the rectifier to match the impedance of the antenna and the rectifier, as shown in the RF harvester of Fig. 4.2. Besides matching the rectifier and the antenna impedances, a matching network can also provide passive voltage boosting of the RF signals [2], making the AC-DC conversion more efficient.

In this chapter, we describe application-oriented design methodologies of the rectifier for energy-harvesting converters. Section 4.1 provides experimental results for DC-DC converters using ULV oscillators and rectifiers and validates the models derived in the previous chapters. Section 4.2 presents the design methodologies for

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Analog Circuits and Signal Processing, https://doi.org/10.1007/978-3-031-04492-2_4

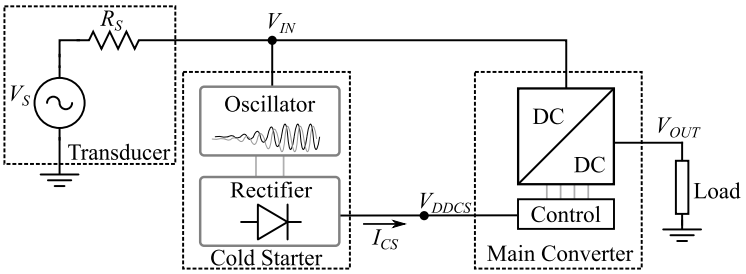

Fig. 4.1 Hybrid DC-DC converter configuration comprised of a cold starter and an efficient main converter

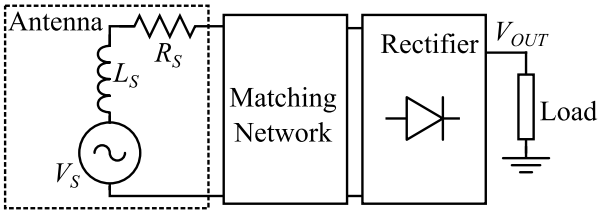

Fig. 4.2 Block diagram of an RF energy harvester

cold starters using a computer-aided routine. In Sect. 4.3, a design methodology for RF energy harvesters that includes some results of Chap. 3 and the passive voltage boosting of the matching network is presented.

4.2 DC-DC Converter Prototypes

In this section, we describe three DC-DC converter prototypes composed of the enhanced-swing cross-coupled oscillator (ES-XCO) and the Dickson charge pump (DCP). The goal of developing different prototypes is to demonstrate the feasibility of the converter for extremely low voltages with different realizations. Also, we show that the minimum V_{IN} required to start up the circuit is strongly dependent on the technology and, particularly, on the quality factor of the inductors.

The converters in this study should generate, from a very small DC input voltage, a DC output of 1 V. The ES-XCO [3, 4] presented in Chap. 2, was chosen to provide the AC signals required for the operation of the DCP. Diode-connected native transistors with high drive capability or Schottky diodes were employed in the prototypes.

The prototypes were experimentally characterized with the setup shown in Fig. 4.3. The input voltage was emulated by the Keithley 2450 source meter, which delivers an accurate voltage and measures the DC current. The output voltage was measured using a high-impedance voltmeter. To emulate the load current, a Keithley 6221 current source was employed.

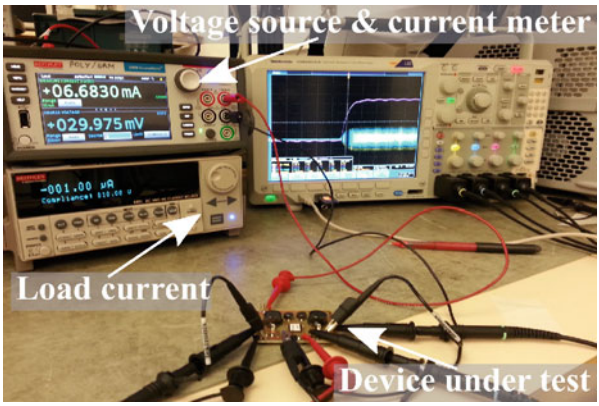

Fig. 4.3 Setup used to characterize the cold-starter converters

4.2.1 Off-the-Shelf Converter Prototype

To show the operation of DC-DC converters from extremely low voltages, a prototype using off-the-shelf devices, apart from the transistors, was designed. The schematic diagram of the circuit presented in [5] is shown in Fig. 4.4. Using native transistors of the 130-nm technology with $W/L = 1500$ µm/420 nm for the ES-XCO, off-the-shelf inductors, and Schottky diodes, the circuit started up from $V_{IN} = 3.8$ mV while providing a DC output voltage of 150 mV. A photograph of the prototype assembled with passive surface mount devices (SMDs) is shown in Fig. 4.4b. High-Q inductors (L_1 and L_2) were used to boost the oscillator output voltage. The inductor parameters characterized at 600 kHz are $L_1 = 9.5$ µH; $Q_{L1} = 80$; $L_2 = 950$ µH; and $Q_{L2} = 80$.

The three-stage ($N = 3$) DCP was built using off-the-shelf Schottky diodes and capacitances $C = 2.2$ nF. The values of the diode saturation current (I_{SAT}) and the slope factor (n) were experimentally obtained as 90 nA and 1, respectively. The converter output reaches 1 V for an oscillation amplitude of 300 mV and a load current of 9 nA or, equivalently, $I_L/I_S = 0.1$.

The transient characteristic of the converter is illustrated in Fig. 4.5a, for $V_{IN} = 25$ mV and $I_L = 120$ nA. The DC output voltage is around 2.2 V. Figure 4.5b shows the waveforms of the converter for $V_{IN} = 11$ mV and $I_L = 10$ nA. The DC output voltage is around 1 V. Due to the loading of the oscillator output nodes by the oscilloscope probe, the results shown in Fig. 4.5 deviate slightly from those shown in Fig. 4.6.

Figure 4.6 presents the converter output voltage (V_{OUT}), output power (P_{OUT}), and power conversion efficiency (η_{CONV}) as a function of the input voltage (V_{IN}). In the graphs, the data were obtained experimentally using the prototype shown in Fig. 4.4b, for load currents ranging from 10 nA to 8 µA. It can be observed that the converter can reach $V_{OUT} = 1$ V at $V_{IN} = 10$ mV and $I_L = 100$ nA. For the case in which the load current is 1 µA, the capability to drive a load of 1 µW is reached for $V_{IN} = 25$ mV.

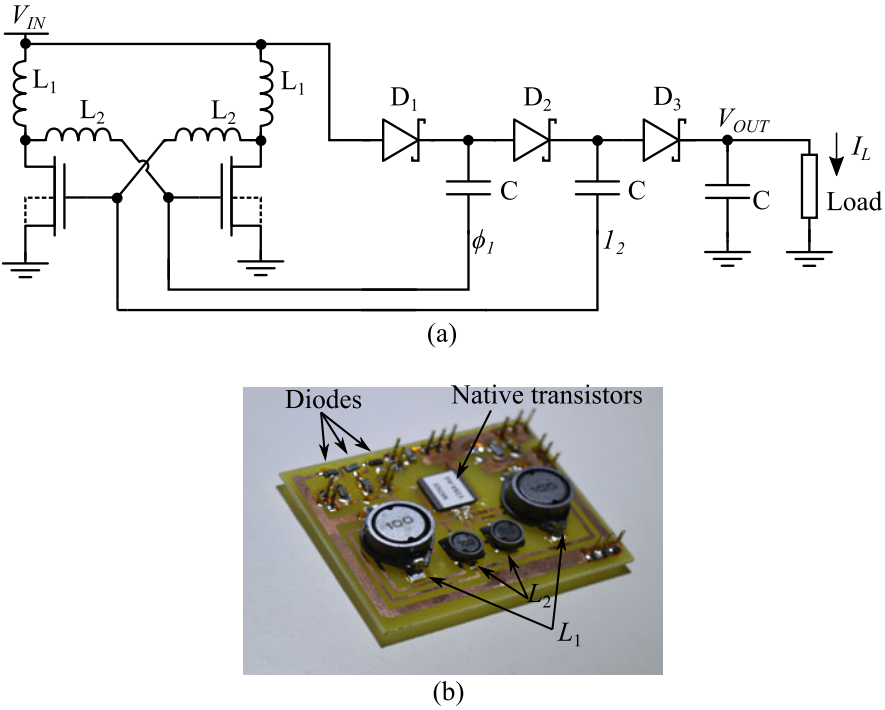

Fig. 4.4 (**a**) Schematic diagram and (**b**) photograph of the cold-starter converter prototype assembled with native transistors of the 130-nm CMOS process and off-the-shelf inductors

4.2.2 A Wire-Bonded Converter Prototype

To increase the output power capability and the conversion efficiency of the circuit shown in Fig. 4.4a, aiming at a startup voltage lower than the thermal voltage kT/q, a second DC-DC converter was designed [6]. Using an integrated DCP and external inductors with quality factors of around 60, the prototype started up for $V_{IN} = 16$ mV and a load current of 10 nA. To reduce the losses associated with the connections between the chip and the external inductors and decrease the minimum startup voltage, the chip was directly wire-bonded to the board substrate. Figure 4.7 presents a photograph of the board employed to test the chip. The areas of inductors L_1 and L_2 are 2.5 mm × 2 mm and 3.4 mm × 1.6 mm, respectively.

The schematic diagram of the wire-bonded converter is shown in Fig. 4.8. For an ES-XCO with an inductive ratio ($K_L = L_2/L_1$) of around 3 ($L_1 = 220$ nH, $L_2 = 595$ nH, $Q \cong 60$ at 50 MHz), the aspect ratio of the native transistor was chosen as 400 × 5 µm/0.42 µm. After the oscillator parameters had been obtained, the DCP parameters were determined. Based on the specifications of $V_{OUT} = 1$ V and $I_L = 1$ µA and employing Eq. (3.16) for the output voltage and Eq. (3.25) for the maximum power conversion efficiency, the number of stages N and the load current normalized

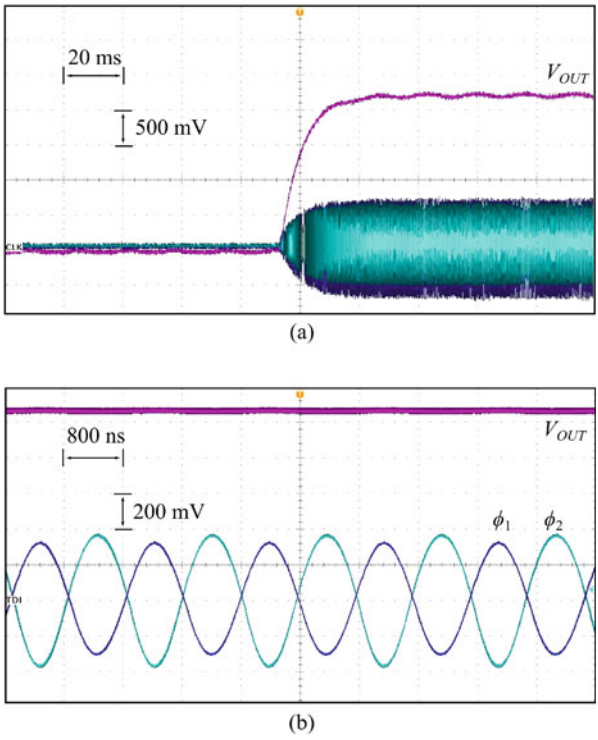

Fig. 4.5 Oscillator and DCP outputs for the off-the-shelf design: (**a**) transient waveforms for $V_{IN} = 25$ mV and $I_L = 120$ nA; (**b**) steady-state waveforms for $V_{IN} = 11$ mV and $I_L = 110$ nA

by the I_L/I_S ratio selected were around 11 and 2.5, respectively. After some tuning through simulation, the requirements for the output voltage and load current were achieved using diode-connected native transistors for the DCP, with $W/L = 4.2$ μm/0.42 μm, which results in a diode saturation current $I_{SAT} = 550$ nA.

The transient of the circuit startup for $V_{IN} = 40$ mV and $I_L = 3$ μA is shown in Fig. 4.9a. It can be observed that the circuit takes less than 2 ms to stabilize at around $V_{OUT} = 1.1$ V. The voltages at the two complementary oscillator outputs and at the converter output for $V_{IN} = 30$ mV and $I_L = 1$ μA are shown in Fig. 4.9b. Due to the oscilloscope probe impedance, the results shown in Fig. 4.9 deviate slightly from those shown in Fig. 4.10.

For the prototype shown in Fig. 4.7, the experimental curves for V_{OUT}, P_{OUT}, and conversion efficiency as a function of the supply voltage are shown in Fig. 4.10. Note that the circuit starts up for $V_{IN} = 16$ mV at $I_L = 10$ nA. The condition $I_L = 1$ μA and $V_{OUT} = 1$ V is obtained at $V_{IN} = 23$ mV, while with $V_{IN} = 37.7$ mV, the circuit can supply a load current of 5 μA at $V_{OUT} = 1$ V. Due to the low amplitude of the oscillatory signals provided by the oscillator in this prototype, the converter efficiency is limited to around 10% for an output voltage of 1 V. The peak efficiency is obtained for $I_L = 4$ μA, corresponding to $I_L/I_{SAT} = 7.3$.

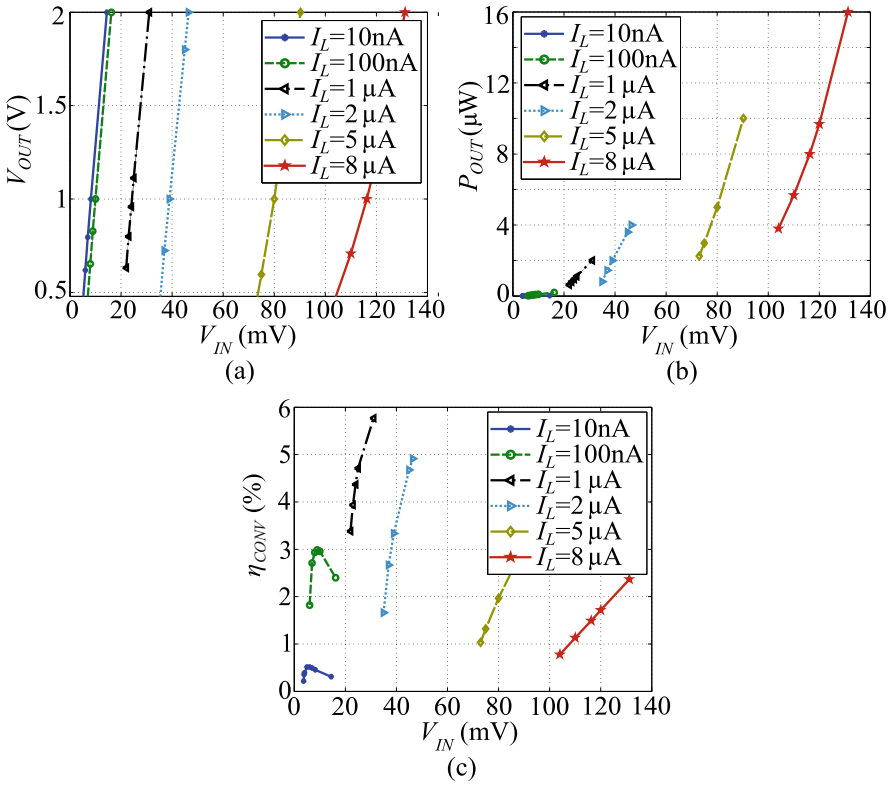

Fig. 4.6 Experimental values of (**a**) output voltage, (**b**) output power, and (**c**) power conversion efficiency of the off-the-shelf converter for load currents ranging from 10 nA to 8 μA, as a function of the input voltage

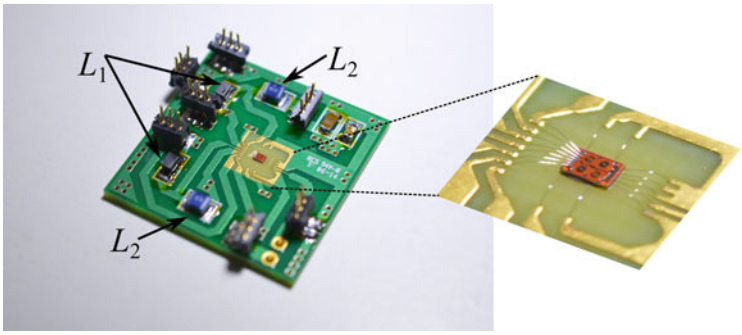

Fig. 4.7 Photograph of the wire-bonded prototype

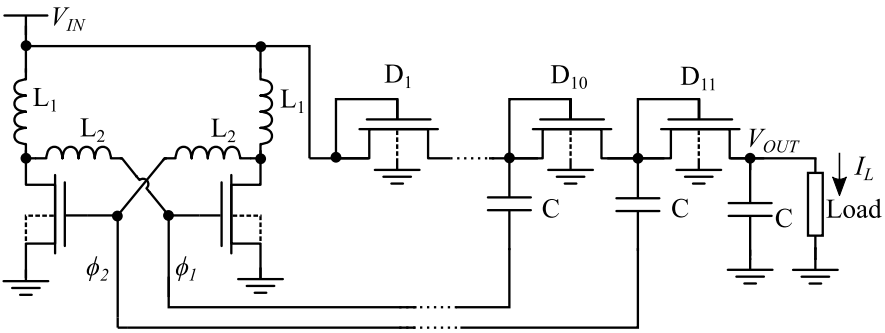

Fig. 4.8 Schematic diagram of the wire-bonded prototype

4.2.3 A Fully Integrated Prototype

The fully integrated cold-starter converter shown in Fig. 4.8 was designed [7] in a 130-nm CMOS technology. The main design goal was to reach the output specification ($V_{OUT} = 1$ V and $I_L = 1$ μA) with the minimum input DC voltage.

In the case of the ES-XCO design, the inductors were chosen for an inductive ratio ($K_L = L_2/L_1$) of around 3.5. Both inductors have a quality factor Q of around 8 at 500 MHz, which is close to the maximum value achievable for the specified frequency in the technology under consideration. After some tuning through simulation, a *W/L* ratio of 500 μm/0.42 μm for the oscillator transistors was found to reach the minimum startup voltage.

The micrograph of the chip containing the fully integrated design integrated in a 130-nm CMOS technology is shown in Fig. 4.11. Wide metal lines were used to reduce the ohmic losses. Along with the converter, a voltage buffer was implemented to measure the oscillator outputs, and a voltage limiter was included to protect the diodes of the converter.

For the fully integrated prototype, the dependence of V_{OUT}, P_{OUT}, and power conversion efficiency on the input voltage was experimentally determined for load currents ranging from 10 nA to 5 μA, as shown in Fig. 4.12. Operating at a frequency of around 550 MHz, the fully integrated prototype can start up from $V_{IN} = 73$ mV, generating around 400 mV at the output. The target specification of 1 V of output voltage and 1 μA of load current is obtained at $V_{IN} = 86$ mV. The integrated step-up converter can supply 5 μW at the output for an input voltage of around 108 mV.

4.3 Design Methodology for Cold Starters

The DC-DC converters described in the previous section provide peak efficiencies much lower than those of switched inductor converters, limiting their application as an efficient main converter. The efficiency is not an essential parameter of a cold

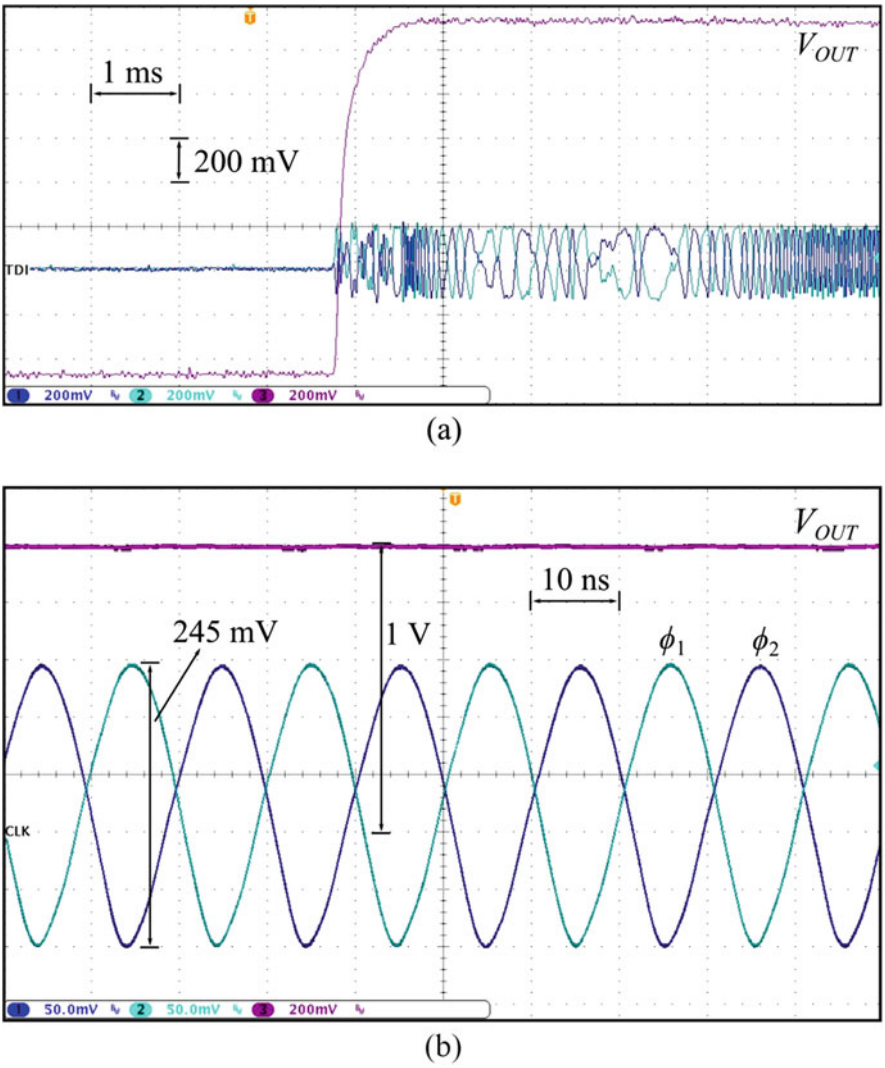

Fig. 4.9 Oscilloscope waveforms of the wire-bonded DC-DC converter: (**a**) startup for $V_{IN} = 40$ mV and $I_L = 3$ μA and (**b**) steady-state operation for $V_{IN} = 30$ mV and $I_L = 1$ μA

starter because its main objective is to self-start at ultra-low-input voltages, providing the startup of the main converter. Therefore, due to the ability to self-start at ultra-low voltages without additional requirements, a structure comprised of a ULV oscillator and a rectifier is commonly adopted as a cold starter in an energy-harvesting interface [1, 8, 9].

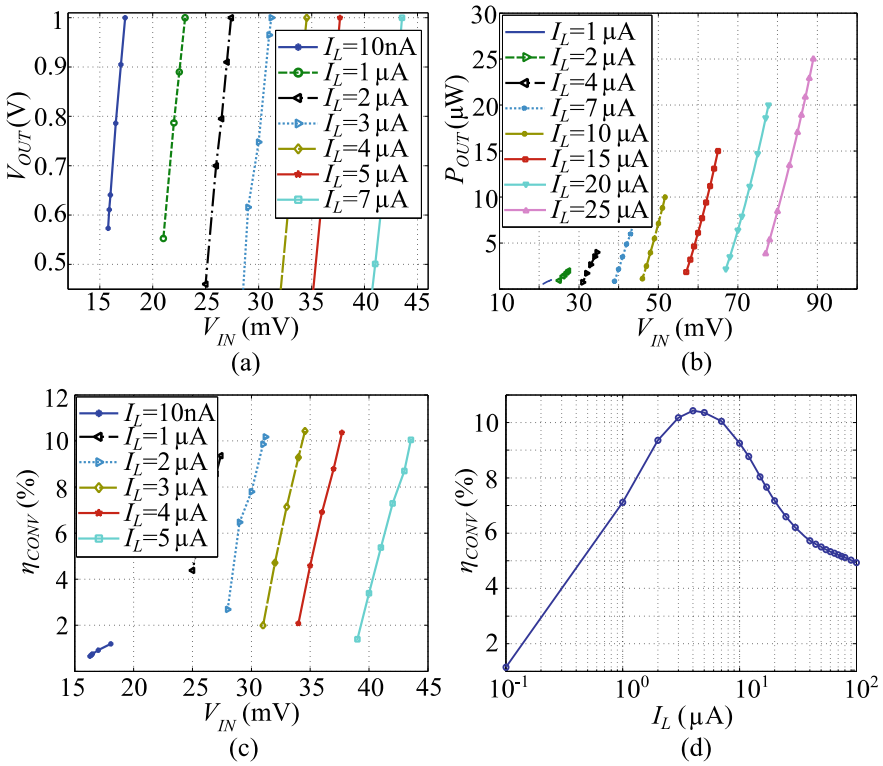

Fig. 4.10 Experimental results for the wire-bonded converter: (**a**) DC output voltage, (**b**) output power, and (**c**) power conversion efficiency as a function of the supply voltage. (**d**) Power conversion efficiency as a function of I_L, for $V_{OUT} = 1$ V

In this section, we describe a design methodology for fully-on-chip cold starters where the expressions of the minimum input voltage of ULV oscillators derived in Chap. 2 and the expressions of the rectifiers provided in Chap. 3 are exploited to reduce the startup voltage of the main converter.

4.3.1 Selecting the Oscillator

Ultra-low-voltage LC oscillators such as those analyzed in Chap. 2 are employed in cold starters to generate AC voltage levels much higher than the DC voltage delivered by the transducer. To choose an appropriate LC oscillator topology for a cold starter, in this section we compare the performances of the cross-coupled oscillator (XCO) and the enhanced swing XCO (ES-XCO) considering both the inductor quality factor (Q) and the load imposed by the rectifier. Using the simplified

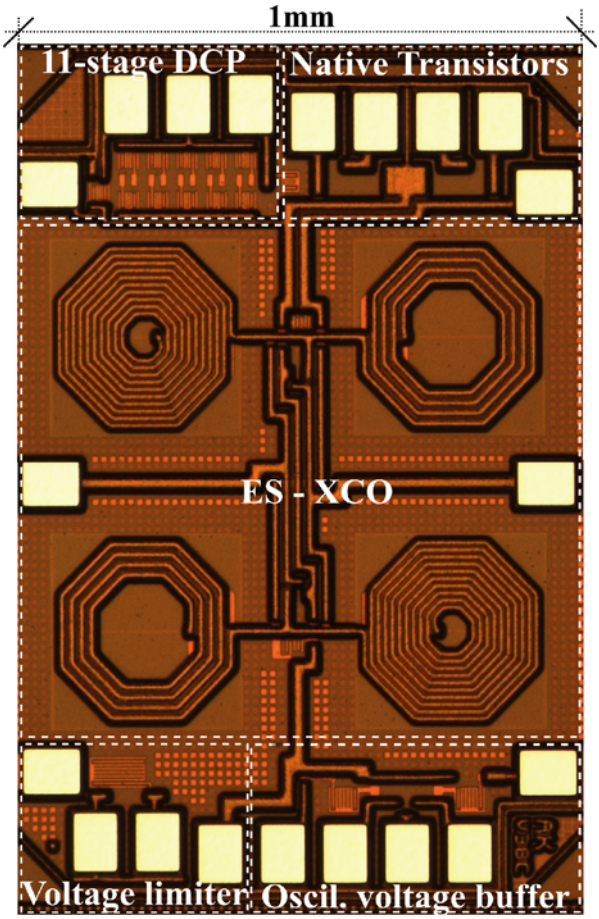

Fig. 4.11 Micrograph of the cold-starter converter integrated in the 130-nm technology

small-signal equivalent circuits of a single stage of the XCO (Fig. 2.3) and the ES-XCO (Fig. 2.8), assuming weak inversion operation, a load equal to G_O at each oscillator output, and a slope factor $n = 1$, the minimum V_{IN} for achieving oscillations with the XCO and with the ES-XCO are approximated by (4.1) and (4.2), respectively

$$V_{IN,min} \approx \phi_t \ln\left[2 + \frac{G_{EQ,XCO}}{g_{md}}\right], \tag{4.1}$$

$$V_{IN,min} \approx \phi_t \ln\left[1 + \frac{1}{1+K_L} + \frac{G_{EQ,ESXCO}}{g_{md}}\right]. \tag{4.2}$$

where

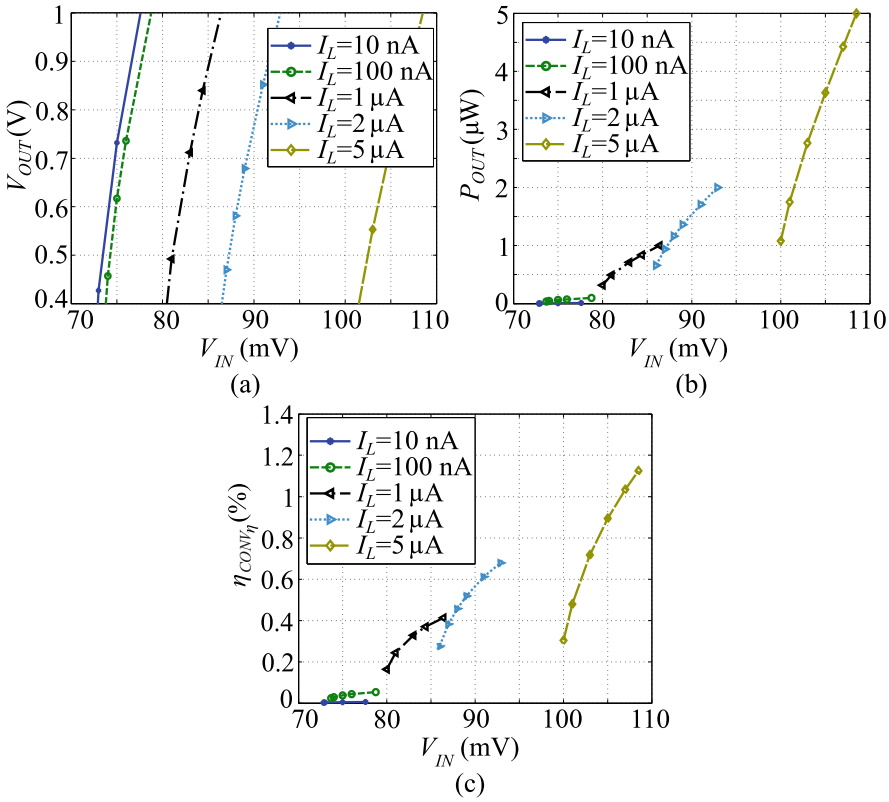

Fig. 4.12 Experimental values of (**a**) output voltage, (**b**) output power, and (**c**) power conversion efficiency of the fully integrated converter for a load current ranging from 10 nA to 5 µA as a function of the input voltage

$$G_{EQ,XCO} = \frac{\sqrt{\frac{C_T}{L}}}{Q} + G_0, \tag{4.3}$$

and

$$G_{EQ,ESXCO} = \frac{\sqrt{\frac{C_T}{L_2}}}{Q} + \sqrt{K_L(1+K_L)} + G_0(1+K_L). \tag{4.4}$$

In weak inversion, with the aid of (1.10) and (1.15), we can approximate $g_m \approx I_X/\phi_t$. Thus, Fig. 4.13 shows the minimum V_{IN} obtained with the XCO and with the ES-XCO for different values of $K_L = L_2/L_1$ using (4.1), (4.2), (4.3) and (4.4). Practical values for the maximum L and Q available in the 180-nm technology are assumed in Fig. 4.13. To plot the curves, C_T and I_X were determined by the extracted parameters of the transistor of the oscillator, which is explained in Sect. 4.3.2.

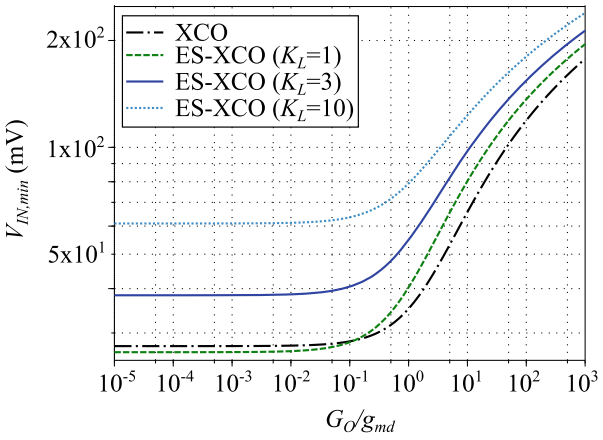

Fig. 4.13 Minimum V_{IN} obtained with the XCO and with the ES-XCO ($I_X = 106$ µA, $C_T = 21$ pF, $\phi_t = 25$ mV, $Q = 8.8$, $L = L_2 = 18.8$ nH)

Although the adoption of the ES-XCO with off-chip inductors of high-Q can provide ultra-low startup voltages [1], in this simulation, the XCO provides better results due to the low Q and limited L of on-chip inductors in the 180-nm technology; thus, the XCO was the preferred choice over the ES-XCO for the realization of the ULV oscillator.

4.3.2 Cold-Starter Design

In the cold-starter design, many degrees of freedom need to be considered due to the various parameters involved in the design of inductors, and transistors, along with the type of rectifier, number of stages, and size of the rectifier devices. Due to both the mutual dependence between oscillation amplitude and rectifier input resistance, and the lack of an analytical expression for the oscillation amplitude, we developed an algorithm to calculate the time domain response of the cold starter. Using this algorithm, we generate a plot of the converter output voltage as a function of both the number of stages and I_{SAT}, enabling the sizing of the rectifier devices [10].

The voltage and current at the cold-starter output (V_{DDCS} and I_{CS} indicated in Fig. 4.1) should be specified to provide the proper powering of the control circuit of the main converter, enabling its startup. For the converter described in Chap. 6 [1, 11], $V_{DDCS} = 0.5$ V and $I_{CS} = 100$ nA fulfill the conditions for the main converter startup.

The design procedure of a completely on-chip cold starter is shown in the flowchart of Fig. 4.14. Initially, the inductor and transistor parameters of the XCO can be determined through simulation using a resistive load connected at the oscillator outputs. This resistive load should be iteratively adjusted to dissipate the specified output power multiplied by a factor k_R higher than the unity to account for the rectifier losses ($k_R \times V_{DDCS} \times I_{CS}$). A factor of two, which emulates a rectifier with 50% efficiency, would be a good starting point.

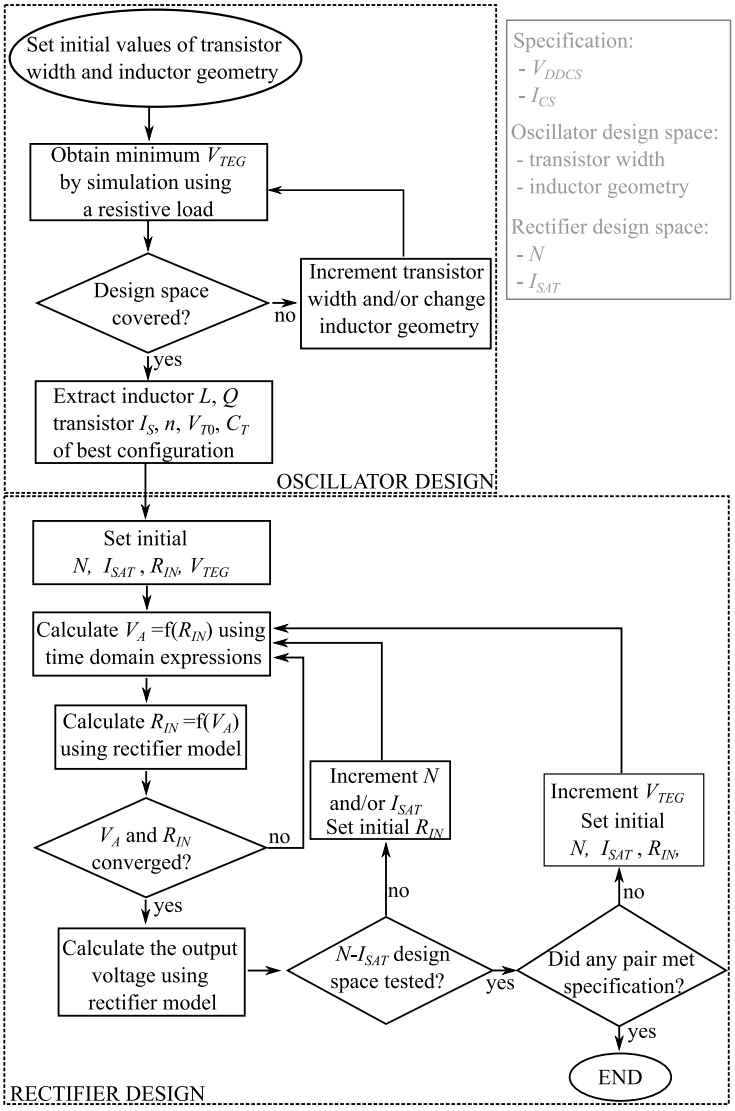

Fig. 4.14 Flowchart detailing the proposed optimization routine

The value of the transistor aspect ratio should be chosen to minimize the V_{TEG} required to obtain the specified output specification (V_{DDCS}, I_{CS}); therefore, several combinations of inductors and transistors are evaluated by parametrical analysis to choose the values of inductance and transistor width that minimize the input voltage required for achieving oscillations. After the determination of the inductor and transistor of the oscillator, the main parameters of the chosen inductor and the transistor are extracted by the EDA tool. These parameters are introduced into the

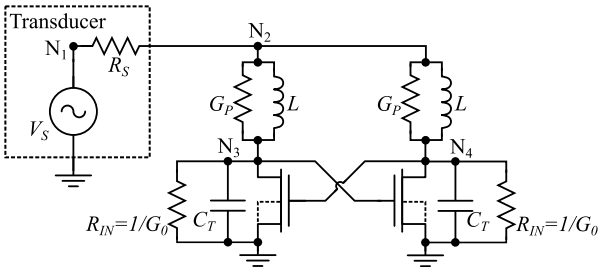

Fig. 4.15 Schematic of the circuit used for the optimization routine

optimization routine, which calculates the time domain response of the circuit in Fig. 4.15 and the amplitude of oscillation. For this, the KCL is applied to the four circuit nodes ($N_{1–4}$), with the capacitors, inductors, and resistors represented by their current-voltage linear relationships. The transistor drain current is calculated using the model provided in Chap. 1.

Once the values of the DC voltage V_{TEG}, the inductance, and the transistor channel length and width have been determined for the oscillator, the optimization routine is started. To initiate the routine, we set an arbitrary value of $R_{IN}\left(G_0^{-1}\right)$ and a value of V_{TEG} lower than the one obtained in the previous step, when a resistive load was connected to the oscillator output. We calculate the oscillation amplitude V_A for a given pair (N, I_{SAT}). Based on the V_A value obtained, a new R_{IN} value is calculated using the expression of R_{IN} for the type of rectifier employed (Table 3.1). With the new value of R_{IN}, the system recalculates and updates the oscillator amplitude (V_A). This cycle should be repeated until V_A and R_{IN} reach convergence within pre-specified limits, allowing V_{DDCS} to be calculated for the given N and I_{SAT}. This procedure should then be repeated for other values of N and I_{SAT}, covering the specified design space. If no N-I_{SAT} pair meets the output specification, V_{TEG} is increased, and the routine is repeated until an N-I_{SAT} pair successfully meets the specification.

Using this methodology, we calculate the minimum voltage that delivers the specified output characteristics ($V_{DDCS} = 500$ mV and $I_{CS} = 100$ nA). The output voltage of the DCP and the full-wave voltage multiplier as a function of N and I_{SAT} are shown in Figs. 4.16 and 4.17, respectively, in the form of level curves [10]. The output level curves are plotted for $V_{TEG} = 46.5$ mV for the DCP and $V_{TEG} = 49$ mV for the voltage multiplier. The target specification can be fulfilled using a DCP with 34 to 70 stages and diodes with I_{SAT} ranging from 300 to 640 nA (N and I_{SAT} points inside the level curve for $V_{DDCS} = 500$ mV).

4.4 Design Methodology for RF Energy Harvesters

In a typical RF energy-harvesting application, an antenna collects the RF signal of very low power, which is converted into a DC voltage by rectifiers [2, 12, 13]. Due to the difference between the antenna impedance and the input impedance of the rectifier, a matching network is adopted (Fig. 4.2) to avoid the reflection of power,

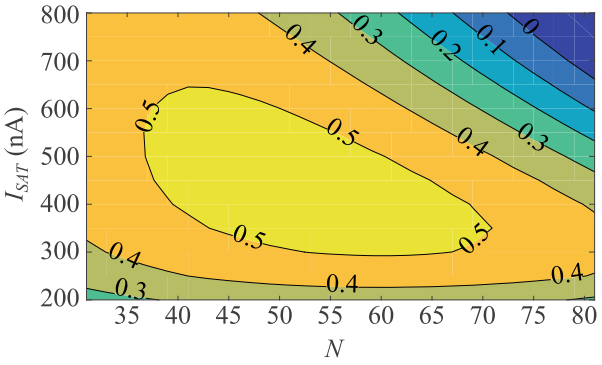

Fig. 4.16 Output voltage level curves obtained using the DCP ($V_{TEG} = 46.5$ mV and $I_{CS} = 0.1$ μA)

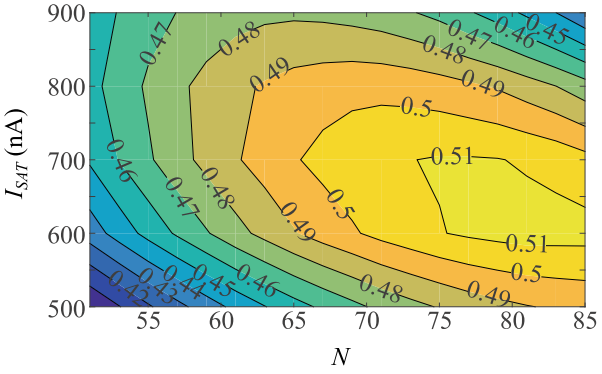

Fig. 4.17 Output voltage level curves obtained using the full-wave voltage multiplier ($V_{TEG} = 49$ mV and $I_{CS} = 0.1$ μA)

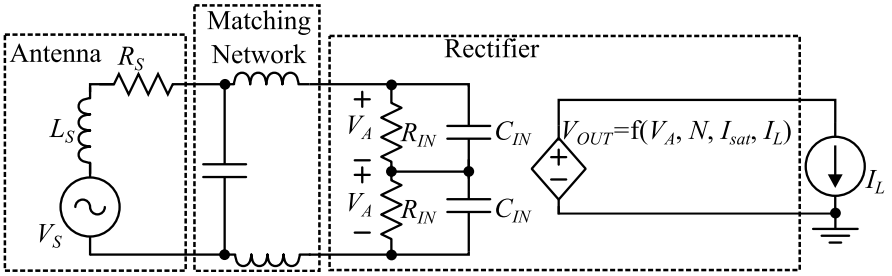

Fig. 4.18 Simplified electrical equivalent circuit of the RF energy harvester comprised of an antenna, an L matching network, and a rectifier

thus, maximizing the power transfer. Another benefit of the matching network can be a voltage boosting, which increases the amplitude of the signal at the rectifier input, thus providing a more efficient operation of the rectifier.

A simplified electrical equivalent circuit of the RF energy-harvesting conversion chain is presented in Fig. 4.18, where V_S, R_S, and L_S are the source (antenna) open-circuit voltage, internal resistance, and inductance, respectively.

4.4.1 Matching-Network Gain

To maximize the power transfer from the antenna to the rectifier, the matching network input impedance should be equal to the complex conjugate of the source impedance, and the output impedance of the matching network should be equal to the complex conjugate of the load impedance (rectifier). For details about the design of the matching network, the reader is referred to [14].

Assuming that these requirements are fulfilled and that matching network is lossless, all the power collected by the antenna is delivered to the rectifier, and the gain of the matching network can be expressed as [2]

$$A_{MN} = \frac{V_A}{\frac{V_S}{2}} = \sqrt{\frac{R_{IN}}{2R_S}} \tag{4.5}$$

The voltage provided by the antenna and the voltage at the input of the rectifier are given, respectively, by

$$V_S = \sqrt{8 \times R_S \times P_{AV}} \tag{4.6}$$

$$V_A = \sqrt{R_{IN} P_{AV}} \tag{4.7}$$

Therefore, the matching network can ideally provide passive voltage boosting ($2V_A > V_S$) when $R_{IN} > 2R_S$. In this section, we assume an ideal matching network to simplify the analysis. It is important to note that further losses in a non-ideal matching network will reduce the voltage calculated using (4.7).

4.4.2 Design Optimization

The design of an energy harvester commonly targets the maximization of both the conversion efficiency and the output voltage, a wide range of input power, and high sensitivity. The designer has many degrees of freedom to consider in the configuration of the harvester, such as the type of rectifier and matching network, number of stages, and sizes of devices. In this section, we initially employ the full-wave voltage multiplier for the harvester, although any type of rectifier can be designed following the same approach. As previously detailed in Chap. 3, the output voltage, conversion efficiency, and input resistance of the full-wave voltage multiplier are given, respectively, by

$$V_{OUT} = \frac{N}{2} n\phi_t \ln\left[\frac{I_0(v_a)}{1 + I_L/2I_{SAT}}\right] \tag{4.8}$$

$$\eta_{CONV} = \frac{n\phi_t/V_A}{\left(1 + \frac{2I_{SAT}}{I_L}\right)\left[\frac{I_1(v_a)}{I_0(v_a)}\right]} \ln\left[\frac{I_0(v_a)}{1 + I_L/2I_{SAT}}\right] \tag{4.9}$$

$$R_{IN} = \frac{2V_A}{N(2I_{SAT} + I_L)}\left[\frac{I_0(v_a)}{I_1(v_a)}\right] \tag{4.10}$$

Using expressions (4.7), (4.8), (4.9), and (4.10), a design methodology for RF energy harvesters similar to those presented in [2, 15] can be employed to optimize the rectifier. In this methodology, the design space (N, I_{SAT}) should be evaluated to find the optimum values of N and I_{SAT} for a given specification. Assuming all the available power is delivered at the input of the rectifier, we combine (4.7) and (4.10), yielding

$$P_{AV} = \frac{NV_A(2I_{SAT} + I_L)}{2}\left[\frac{I_1(v_a)}{I_0(v_a)}\right]. \tag{4.11}$$

Due to the difficulty in obtaining an expression for V_A as an explicit function of P_{AV}, we solve (4.11) numerically using a computer-aided optimization method to find the solution of V_A for a given P_{AV}, enabling the optimization of the rectifier for maximum sensitivity, output voltage, or conversion efficiency. The design methodology provides a set of N and I_{SAT} design points that comply with the specification.

4.4.2.1 Maximizing Sensitivity

The sensitivity of the RF energy harvester is defined as the minimum level of available power that can fulfill the output specification (V_{OUT}, I_L). Following the flowchart given in Fig. 4.19, the sensitivity of the rectifier can be maximized. This optimization procedure specifies the load current and the output voltage. To maximize the sensitivity, N and I_{SAT} pairs that meet the specification for the lowest P_{AV} should be chosen. Therefore, for a given level of P_{AV}, (4.11) should be solved numerically to find the value of V_A for each N-I_{SAT} pair of the design space. With the values obtained for V_A, V_{OUT} is calculated using (4.8). If any pair successfully meets the specification of V_{OUT} and I_L, the value of P_{AV} can be decreased, and the process can be repeated for lower levels of P_{AV}.

Using this design methodology, the level curves showing the N-I_{SAT} pairs that meet the output specification for different levels of P_{AV} are shown in Fig. 4.20 for the full-wave voltage multiplier. The same procedure is also repeated for the Dickson

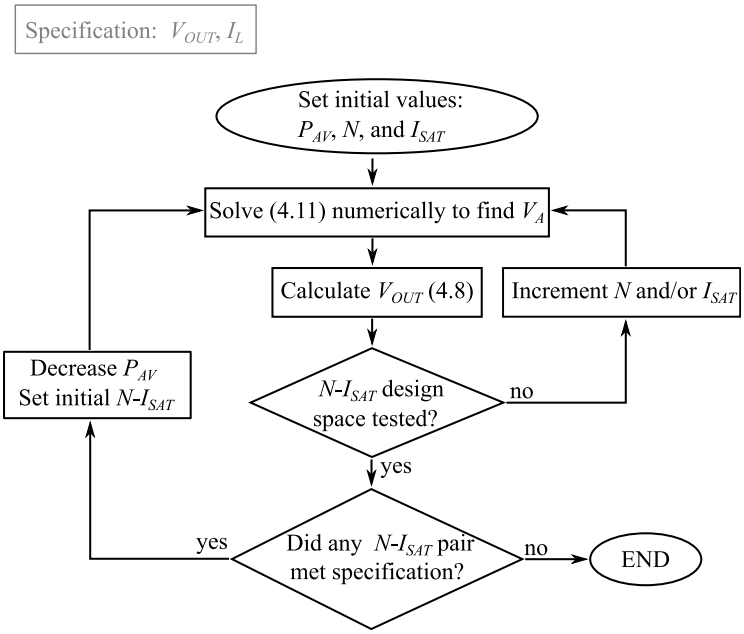

Fig. 4.19 Flowchart detailing the optimization procedure to maximize sensitivity

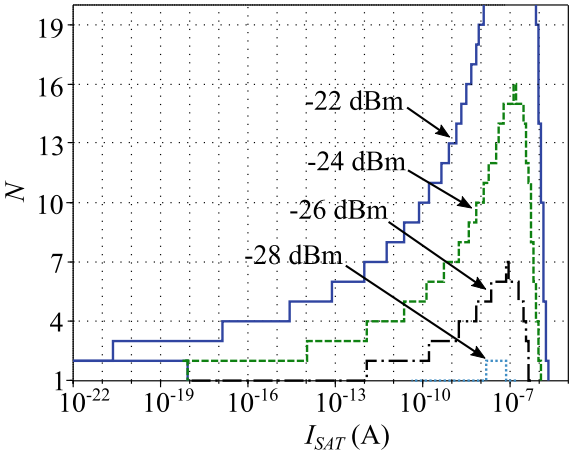

Fig. 4.20 Level curves for P_{AV} for the specification of $V_{OUT} = 1$ V and $I_L = 1$ µA using the full-wave voltage multiplier

charge pump using the expressions derived in Chap. 3, with the corresponding results given in Fig. 4.21. It can be noted that for the specifications of $V_{OUT} = 1$ V and $I_L = 1$ µA, an N-I_{SAT} pair enclosed by the level curve of $P_{AV} = -28$ dBm should be chosen to maximize the sensitivity of a full-wave voltage multiplier or the DCP.

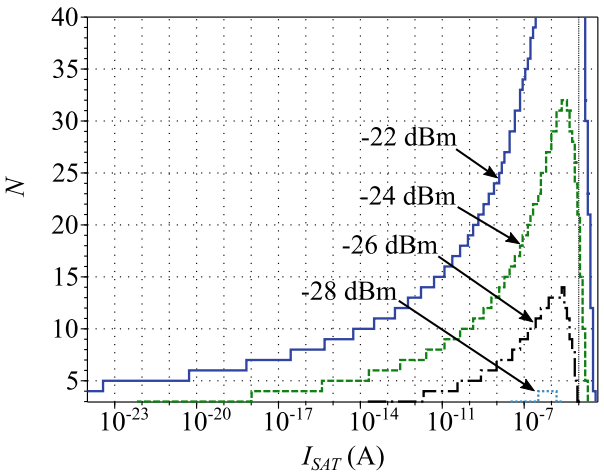

Fig. 4.21 Level curves for P_{AV} for the specification of $V_{OUT} = 1$ V and $I_L = 1$ µA using the DCP

After choosing the N-I_{SAT} pair, the input resistance can be calculated using (4.10), enabling the design of the matching network. However, the input resistance of the rectifier is a (nonlinear) function of the dynamic variables I_L and V_A. Therefore, the system is only matched for the specified values of I_L and V_A and operates slightly unmatched for different operational conditions. In such cases, the reflected power will decrease the power transfer to the rectifier, thus decreasing the harvesting efficiency.

4.4.2.2 Maximizing the Output Voltage and Efficiency

The output voltage and conversion efficiency of the rectifier can be maximized following the steps shown in the flowchart given in Fig. 4.22. In this optimization procedure, the load current and the available power are specified, and (4.11) should be solved numerically to find the value of V_A for each N-I_{SAT} pair of the design space. The V_{OUT} and η_{CONV} values are then calculated with the results obtained for V_A using (4.8) and (4.9), respectively.

The level curves for V_{OUT}/η_{CONV} are shown in Fig. 4.23, for the full-wave voltage multiplier. The same procedure is repeated for the Dickson charge pump using the expressions derived in Chap. 3, with the results presented in Fig. 4.24. Note that for the specifications of $P_{AV} = -27$ dBm and $I_L = 1$ µA, both the full-wave voltage multiplier and the DCP can deliver around 1.4 V at the output with a peak efficiency of 70%.

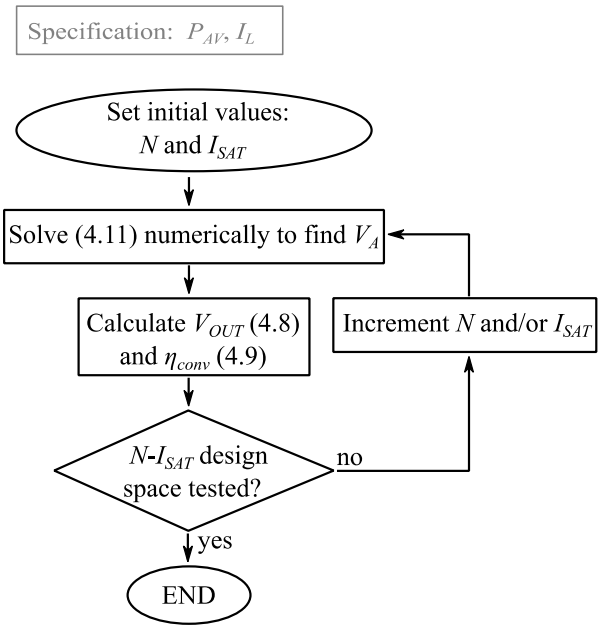

Fig. 4.22 Flowchart detailing the optimization procedure to maximize the output voltage and efficiency

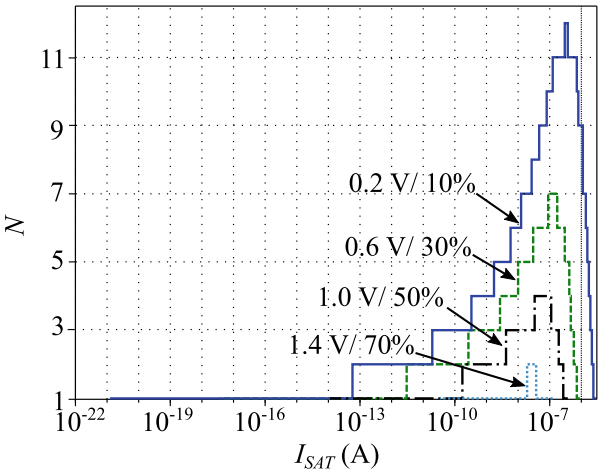

Fig. 4.23 Level curves for V_{OUT} and η_{CONV} as a function of N and I_{SAT} using the full-wave voltage multiplier

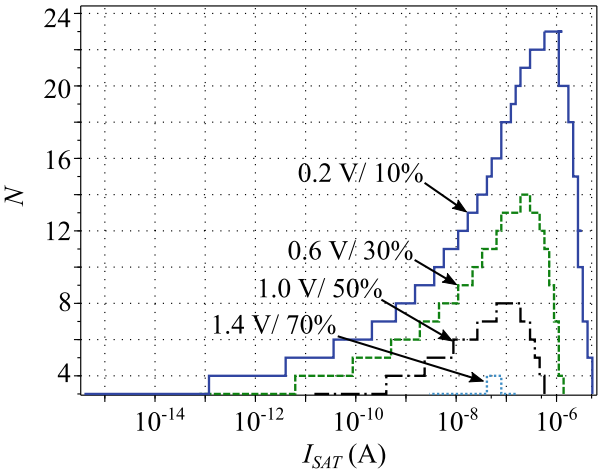

Fig. 4.24 Level curves for V_{OUT} and η_{CONV} as a function of N and I_{SAT} using the DCP

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Chapter 5
Analysis of the Inductive Boost Converter for Ultra-Low-Voltage Operation

5.1 Introduction to Inductive Boost Converters

Inductive boost converters are commonly used for DC-DC conversion in energy-harvesting applications. The converter employed in such applications needs to cope with the restricted levels of available power and ultra-low input voltages delivered by conventional transducers and to provide efficient voltage conversion. The fulfillment of these requirements makes the inductive boost converter a feasible choice for energy-harvesting interfaces, because it can provide high conversion efficiency under a wide range of input voltages and regulate the output voltage. Nevertheless, inductive boost converters suffer from drawbacks such as the need for external off-chip components and auxiliary circuits to provide low-voltage startup.

5.2 The Converter Conduction Mode

A simplified architecture of an inductive boost converter is presented in Fig. 5.1. The conventional inductive boost converter is comprised of an inductor (L), an output capacitor (C_{OUT}), and two switches, namely, the low-side switch (LSS) and the high-side switch (HSS), employed to control the charging and discharging phases of the inductor, respectively.

Inductive boost converters can be operated in either continuous conduction mode (CCM) or discontinuous conduction mode (DCM). In CCM, the inductor current is always greater than zero. Under steady-state operation, each period (T) of the converter is divided into two phases, as shown in Fig. 5.2, with

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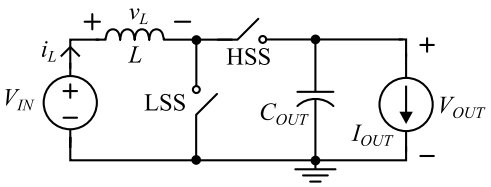

Fig. 5.1 Simplified schematic of the inductive boost converter

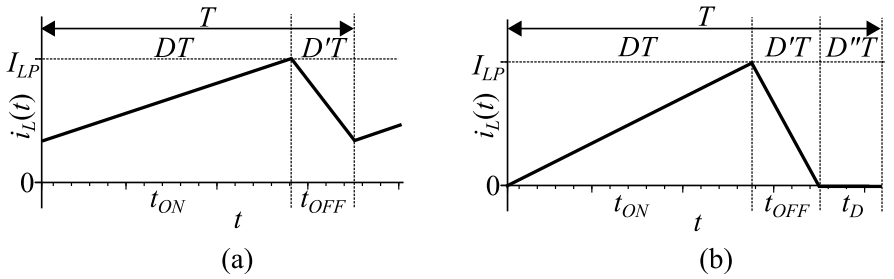

Fig. 5.2 Inductor current for the (**a**) CCM and (**b**) DCM operation

$$t_{ON} = DT, \tag{5.1}$$

$$t_{OFF} = D'T. \tag{5.2}$$

During the charging phase (t_{ON}), the LSS is closed and the HSS is open. Thus, the inductor is charged by the input voltage source (V_{IN}), while the load current is supplied by the capacitor. During the discharging phase (t_{OFF}), the LSS is open and the HSS is closed; therefore, a fraction of the inductor energy is used to both supply the load and recharge the capacitor. In CCM, the inductor continuously alternates between the charging and discharging phases. In DCM operation (Fig. 5.2b), there is an additional idle phase (t_D), when both switches are open, and the inductor current is equal to zero.

$$t_D = D''T. \tag{5.3}$$

To compare the efficiency of DCM with CCM, we analyze the inductor charging efficiency [1] using the circuit shown in Fig. 5.3. In this configuration, the inductor voltage and current, respectively, are given by

$$v_L(t) = (V_S - Ri_L(0))e^{-t\frac{R}{L}}, \tag{5.4}$$

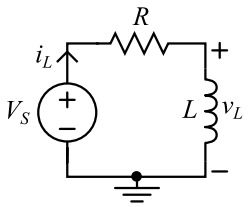

Fig. 5.3 Circuit used for the analysis of the inductor charging efficiency

$$i_L(t) = \frac{V_S}{R} + \left(i_L(0) - \frac{V_S}{R}\right)e^{-t\frac{R}{L}}. \tag{5.5}$$

where V_S is the power supply voltage, L is the inductance, and R is the total path resistance.

For any given charging time, the inductor charging efficiency can be written as the ratio between the energy transferred to the inductor (E_L) and the energy delivered by the power supply (E_S):

$$\eta_L(t) = \frac{E_L(t)}{E_S(t)}, \tag{5.6}$$

where

$$E_S(t) = \int_0^t V_S i_L(t)dt = \int_0^t V_S\left[\frac{V_S}{R} + \left(i_L(0) - \frac{V_S}{R}\right)e^{-t\frac{R}{L}}\right]dt \tag{5.7}$$

and

$$E_L(t) = \int_0^t \left[(V_S - Ri_L(0))e^{-t\frac{R}{L}}\right]\left[\frac{V_S}{R} - \frac{1}{R}(V_S - Ri_L(0))e^{-t\frac{R}{L}}\right]dt. \tag{5.8}$$

Using (5.6), the inductor charging efficiency is plotted as a function of the normalized $i_L(0)$ for different normalized charging times (tR/L) in Fig. 5.4.

As can be seen, for fixed circuit parameters, low values of $i_L(0)$ provide higher efficiencies. Thus, the charging of the inductor starting at $i_L(0) = 0$ is always the point of highest efficiency. Therefore, the DCM has an intrinsic advantage over CCM for maximizing the energy transfer from the source to the inductor. An additional benefit of DCM operation is the maximization of the extraction of the available power by means of a simple relation between the switching frequency and the inductance, as will be explained later in this chapter. Hence, the DCM operation of the inductive boost converter is a common solution for DC-DC conversion for energy-harvesting applications.

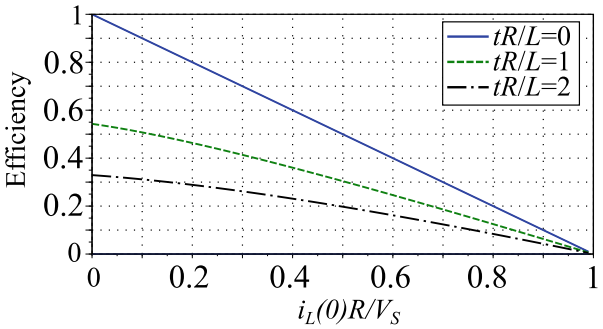

Fig. 5.4 Plot of the inductor charging efficiency

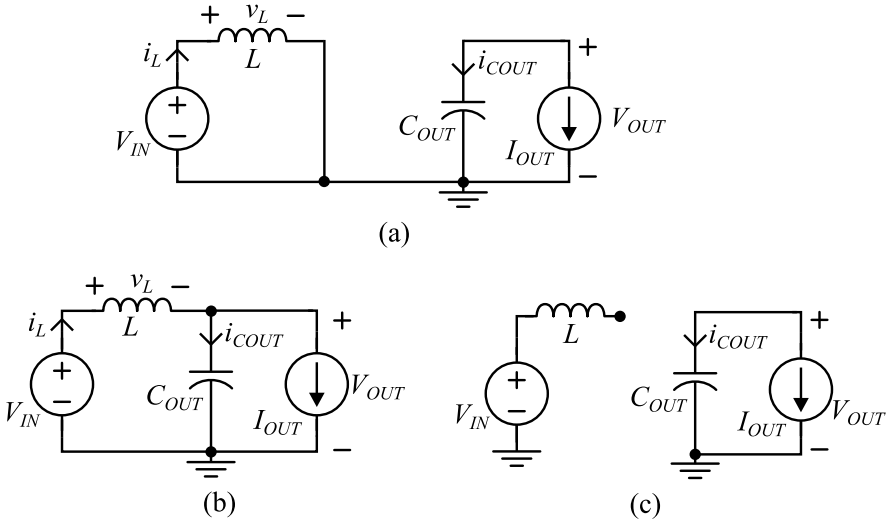

Fig. 5.5 Equivalent circuit of the inductive boost converter during (**a**) t_{ON}, (**b**) t_{OFF}, and (**c**) t_D

5.3 The Ideal Boost Converter in Discontinuous Conduction Mode

For a first-order analysis, let us assume that the power supply is modeled as an ideal voltage source and a lossless inductor. During the inductor charging phase, the circuit shown in Fig. 5.1 is equivalent to that presented in Fig. 5.5a. During this phase, the inductor is charged by the input voltage, and the output capacitor delivers the load current. The inductor current is given [2] by

$$i_L(t) = \frac{V_{IN}}{L}t; \tag{5.9}$$

thus, the peak inductor current is given by

$$I_{LP} = \frac{V_{IN}}{L} t_{ON} = \frac{V_{IN}}{L} DT. \tag{5.10}$$

During the discharging phase (Fig. 5.5b), the inductor energy is transferred to both the output capacitor and the load. The inductor current is given by

$$i_L(t) = \frac{V_{IN}}{L} t_{ON} + \left(\frac{V_{OUT} - V_{IN}}{L}\right)(t_{ON} - t). \tag{5.11}$$

During the idle phase, the circuit reduces to that shown in Fig. 5.5c, and $i_L(t) = 0$. Hence, using (5.9) and (5.11), the average inductor current for a full conversion period (T) is given by

$$\bar{i_L} = \frac{I_{LP}(t_{ON} + t_{OFF})}{2T} = \frac{V_{IN} DT(D + D')}{2L}. \tag{5.12}$$

Applying the charge balance to the lossless output capacitor, the total charge delivered by the inductor during the inductor discharging phase is consumed in the load over period T. Therefore,

$$I_{OUT} = \frac{I_{LP} t_{OFF}}{2T} = \frac{V_{IN} DD'T}{2L}. \tag{5.13}$$

5.4 The Ideal Gain Factor

The voltage gain, or the gain factor, of the boost converter is

$$M = \frac{V_{OUT}}{V_{IN}}. \tag{5.14}$$

Applying the volt-second balance for the lossless inductor yields

$$\int_0^T v_L(t)dt = V_{IN} t_{ON} + (V_{IN} - V_{OUT})(t_{OFF}) = 0. \tag{5.15}$$

Hence,

$$M = \frac{V_{OUT}}{V_{IN}} = 1 + \frac{t_{ON}}{t_{OFF}} = 1 + \frac{D}{D'}. \tag{5.16}$$

Substituting D' given by (5.13) into (5.16), we obtain an expression for the gain factor of the boost converter in DCM as follows:

$$M = 1 + \frac{D^2 T V_{IN}}{2 L I_{OUT}} = 1 + \frac{D^2 V_{IN}}{2 L f_{SW} I_{OUT}}, \tag{5.17}$$

where $f_{SW} = 1/T$. For low-voltage energy-harvesting applications in which $V_{IN} \ll V_{OUT}$, we approximate (5.17) by

$$M \cong \frac{D^2 V_{IN}}{2 L f_{SW} I_{OUT}}. \tag{5.18}$$

5.5 Efficiency in Energy-Harvesting Boost Converters

Let us now define the extraction, conversion, and end-to-end efficiencies of a typical energy-chain using the boost converter shown in Fig. 5.6. A resistance was included in series with the voltage supply to model an energy source with limited available power.

The available power is the maximum power that can be extracted from the energy-harvesting transducer. For transducers modeled by a voltage source in series with an internal resistance, e.g., a thermoelectric generator (TEG), the available power is given by

$$P_{AV} = \frac{V_S^2}{4 R_S}. \tag{5.19}$$

The extraction efficiency indicates how efficiently the available power is delivered to the converter. It is defined as the ratio of the converter input power (P_{IN}) to the available power

$$\eta_{EXTR} = \frac{P_{IN}}{P_{AV}}. \tag{5.20}$$

The conversion efficiency, which is a common figure of merit for voltage converters, is defined as the ratio of the converter output power (P_{OUT}) to the converter input power

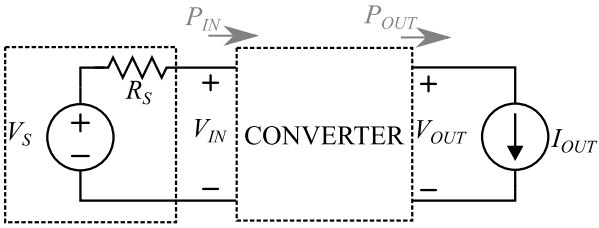

Fig. 5.6 Simplified energy-harvesting conversion chain

$$\eta_{CONV} = \frac{P_{OUT}}{P_{IN}}. \tag{5.21}$$

From (5.20) and (5.21), the end-to-end efficiency can be calculated as

$$\eta_{END\text{-}TO\text{-}END} = \eta_{EXTR}\eta_{CONV} = \frac{P_{OUT}}{P_{AV}}. \tag{5.22}$$

The end-to-end efficiency is a useful figure of merit of an energy harvester since it represents the fraction of the available power that is delivered to the load.

5.6 Extraction Efficiency of Ultra-Low-Voltage Boost Converters

Usually, the available power of energy-harvesting transducers is very low. Hence, the converter should be designed to exploit, as much as possible, the available power. The maximization of the extraction efficiency is an important requirement of an energy-harvesting converter, since it increases the range of applications that can be powered.

To maximize the extraction efficiency, the conventional circuit of the inductive boost converter needs to be modified and some design parameters properly set to allow the maximum power transfer from the transducer to the converter.

5.6.1 Harvesting from Known Available Power

If the open circuit voltage (V_S) is constant in the circuit of Fig. 5.7, the input power of the converter is

$$P_{IN} = \frac{1}{T}\int_0^T p_{IN}(t)dt = \frac{1}{T}\int_0^T [V_S - R_S i_S(t)]i_L(t)dt. \tag{5.23}$$

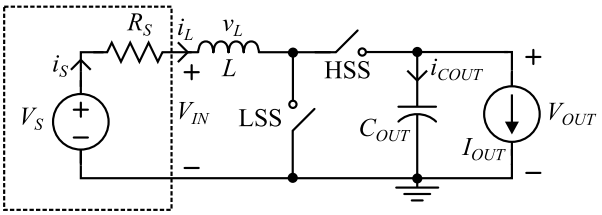

Fig. 5.7 Conventional inductive boost converter

Since the power supply current is equal to the inductor current, using expressions (5.9), (5.10), (5.11), and (5.23), we obtain

$$P_{IN} = \left(\frac{t_{ON} + t_{OFF}}{T}\right)\left(\frac{V_S I_{LP}}{2} - R_S \frac{I_{LP}^2}{3}\right). \tag{5.24}$$

The substitution of (5.24) into (5.20) yields

$$\eta_{extr} = \frac{\left(\frac{t_{ON}+t_{OFF}}{T}\right)\left(\frac{V_S I_{LP}}{2} - R_S \frac{I_{LP}^2}{3}\right)}{\frac{V_S{}^2}{4R_S}}. \tag{5.25}$$

The peak inductor current (I_{LP}) that delivers the maximum extraction efficiency, calculated for $\partial \eta_{extr}/\partial I_{LP} = 0$, gives

$$I_{LP,MAX} = \frac{3}{4}\frac{V_S}{R_S}. \tag{5.26}$$

Substituting (5.26) into (5.25) yields

$$\eta_{extr} = \left(\frac{t_{ON} + t_{OFF}}{T}\right)\left(\frac{3}{4}\right). \tag{5.27}$$

Therefore, when the dead time is zero ($t_D = 0 \rightarrow t_{ON} + t_{OFF} = T$), the circuit in Fig. 5.7 reaches the maximum extraction efficiency of 75%.

5.6.1.1 Insertion of an Input Capacitor

With the inclusion of an input capacitor (C_{IN}), as shown in Fig. 5.8, the input ripple caused by the inductor current through R_S can be made negligible and the extraction of power maximized. In general, C_{IN} is a high-value off-chip capacitance due to the requirements of ripple and frequency.

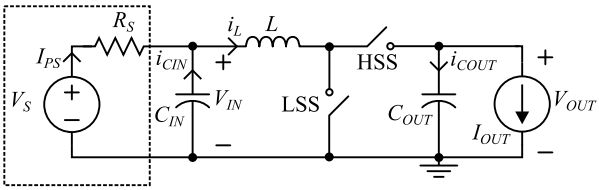

Fig. 5.8 Inductive boost converter using an input capacitor

In this configuration, the supply current can be assumed to be constant (I_{PS}) and equal to the average inductor current. Therefore, the extraction efficiency is given by

$$\eta_{EXTR} = \frac{\frac{V_S I_{LP}(t_{ON}+t_{OFF})}{2T} - R_S \frac{I_{LP}^2 (t_{ON}+t_{OFF})^2}{4T^2}}{\frac{V_S^2}{4R_S}}. \tag{5.28}$$

The peak inductor current that leads to maximum efficiency is

$$I_{LP,MAX} = \frac{V_S T}{R_S(t_{ON} + t_{OFF})}. \tag{5.29}$$

Substituting (5.29) into (5.28) gives a maximum extraction efficiency of 100%. Therefore, an input capacitor can be used for the maximization of the extraction efficiency. Section 5.8 provides expressions for calculating the value of the input capacitor for a specified input ripple.

5.6.2 *Maximum Power Point Tracking*

Maximum power point tracking (MPPT) techniques are employed in boost converters to ensure that the available power is delivered at the input of the converter. The control of the peak current according to (5.29) requires a complex circuit solution; hence, the most common approaches for the maximization of the extraction efficiency are the proper regulation of the input impedance of the converter [3, 4] or control of the converter input voltage level [5].

5.6.2.1 Converter Input Impedance

For energy-harvesting transducers modeled by a voltage supply in series with an internal resistance, a feasible solution to perform the MPPT is to match the input impedance of the converter to the internal resistance of the power supply ($R_{IN} = R_S$). Under this condition, we have

$$V_{IN} = \frac{V_S}{2}. \tag{5.30}$$

In this case, the input impedance of the converter is given by

$$R_{IN} = \frac{V_{IN}}{I_{PS}}, \tag{5.31}$$

The supply current is equal to the average inductor current, and thus, for a high gain factor ($t_{ON} \gg t_{OFF}$), the supply current calculated using (5.9) is

$$I_{PS} = \frac{I_{LP}}{2} D = \frac{V_{IN} D^2}{2 L f_{SW}}. \tag{5.32}$$

Hence, (5.31) can be rewritten as

$$R_{IN} = \frac{2 L f_{SW}}{D^2}. \tag{5.33}$$

To track the maximum power point, R_{IN} must be equal to R_S. Thus, (5.33) can be rewritten as

$$L f_{SW} = \frac{D^2 R_S}{2}. \tag{5.34}$$

Therefore, to track the maximum power point, the converter should be designed to set the Lf_{SW} product as given by (5.34). In a typical case where the series resistance of the energy-harvesting transducer is nearly constant over a specified range of P_{AV}, setting the design parameters to comply with (5.34) is a feasible way to carry out the MPPT. It should be noted that, under the condition of MPPT, the gain factor (5.18) reduces to

$$M \cong \sqrt{\frac{V_{OUT}}{I_{OUT} R_S}}. \tag{5.35}$$

5.6.2.2 Controlling the Converter Input Voltage

Besides setting fixed design parameters L and f_{SW} to comply with (5.34), another approach for the realization of MPPT is the use of control circuits that adjust the input voltage to one-half of the transducer open-circuit voltage. This can be achieved by controlling D and/or f_{SW} dynamically. This method requires the periodic disconnection of the power supply for the measurement of the open-circuit voltage and comparison with the input voltage. Based on the result obtained, D and/or f_{SW} can be controlled to ensure the MPPT. This approach provides a more precise MPPT with the drawback of the additional consumption of the control circuit used for this purpose, as well as an increase in circuit complexity.

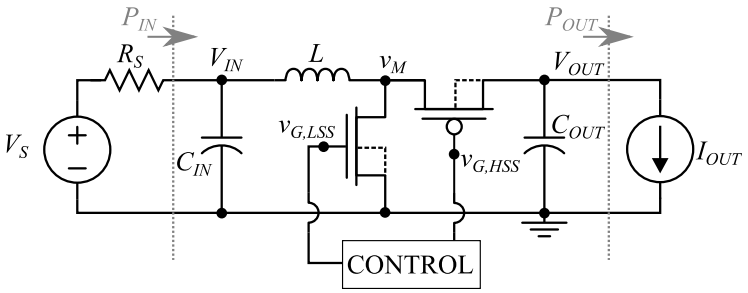

Fig. 5.9 Simplified inductive boost converter in CMOS technology

5.7 Conversion Efficiency

A simplified representation of the inductive boost converter implemented in the CMOS technology is shown in Fig. 5.9. The LSS and the HSS are commonly realized by NMOS and PMOS transistors, respectively, controlled by an on-chip circuit. Signals $v_{G,LSS}$ and $v_{G,HSS}$ control the opening and closing of the LSS and HSS for the charging, discharging, and idle phases.

For the circuit shown in Fig. 5.9, the conversion efficiency is given by

$$\eta_{CONV} = \frac{P_{IN} - P_{LOSS}}{P_{IN}}, \tag{5.36}$$

where P_{LOSS} is the total of the converter losses. The conversion efficiency is dependent on design parameters, such as the boost switches sizes, the frequency of operation, and the duty cycle. There are optimal values for the design parameters that minimize the converter losses. In the following subsections, we analyze the relevant sources of losses of the inductive boost converter under low-voltage operation, namely, the conduction losses (P_{COND}), the dynamic losses (P_{DYN}), the leakage losses (P_{LEAK}), and the power consumption of the control block (P_{CTL}), as shown in (5.37).

$$P_{LOSS} = P_{COND} + P_{LEAK} + P_{DYN} + P_{CTL}. \tag{5.37}$$

5.7.1 Conduction Losses

The conduction losses are due to ohmic losses in the switches, inductor, and metal tracks. Figure 5.10 shows the equivalent circuit of the boost converter including the main parasitic resistances during t_{ON} (top) and t_{OFF} (bottom). The idle phase is not represented because the inductor current is zero during this phase.

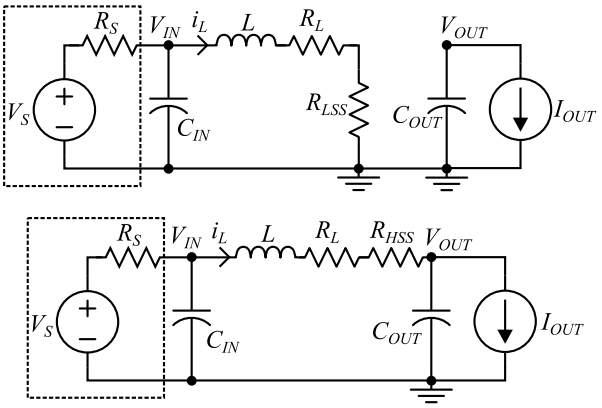

Fig. 5.10 Equivalent circuit of the boost converter including the inductor and switches resistances during t_{ON} (top) and t_{OFF} (bottom)

Using the equivalent circuits shown in Fig. 5.10, we can simplify the total conduction losses as

$$P_{COND} \approx P_{CL} + P_{CLSS} + P_{CHSS}, \tag{5.38}$$

where P_{CL} is the conduction loss in the equivalent series resistance (R_L) of the inductor, P_{CLSS} is the conduction loss in the LSS resistance (R_{LSS}), and P_{CHSS} is the conduction loss in the HSS resistance (R_{HSS}). Assuming that t_{ON} and t_{OFF} are much shorter than the time constant $L/(R_L + R_{LSS})$, we use the time domain expressions of the ideal boost converter to approximate

$$P_{CL} = \frac{1}{T}\int_0^T R_L i_L(t)^2 dt \approx \frac{R_L {I_{LP}}^2 (D + D')}{3}. \tag{5.39}$$

The substitution of (5.10) into (5.39) and the assumptions that the Lf_{SW} product complies with (5.34) and the converter operates under high gain give

$$P_{CL} \approx \frac{2\sqrt{2}}{3} \frac{R_L V_{IN}^2}{\sqrt{{R_S}^3 L f_{SW}}}. \tag{5.40}$$

Using the same method employed to calculate the conduction losses in the inductor series resistance, we obtain the conduction losses in the switches and rewrite (5.38) as

$$P_{COND} \approx \frac{2\sqrt{2}}{3} \frac{V_{IN}^2}{\sqrt{{R_S}^3 L f_{SW}}} \left(R_L + \frac{R_{S,LSS} L_{LSS}}{W_{LSS}} + \frac{R_{S,HSS} L_{HSS} V_{IN}}{W_{HSS} V_{OUT}} \right). \tag{5.41}$$

$L_{L(H)SS}$ and $W_{L(H)SS}$ are the channel length and width, respectively, of the low (high) side switch. The sheet resistances of the switches ($R_{S,L(H)SS}$) can be calculated using the MOSFET model [6] in strong inversion presented in Chap. 1. Assuming

that the logic-low and logic-high control signals applied to the gates ($v_{G,LSS}$ and $v_{G,HSS}$) of the LSS and HSS are, respectively, zero and V_{OUT}, we have

$$R_{S,L(H)SS} \approx \frac{1}{\mu_{n(p)} C_{ox}\left(V_{OUT} - \left|V_{T0,n(p)}\right|\right)}. \tag{5.42}$$

where $\mu_{n(p)}$ is the electron (hole) mobility, C_{ox} is the gate oxide capacitance per unit area, and $V_{T0,n(p)}$ is the equilibrium threshold voltage of the N(P)MOS device used for the switch.

5.7.2 Leakage Losses

The leakage losses are due to the leakage currents in MOS switches when they are open. The leakage currents are represented in the equivalent circuits of Fig. 5.11.

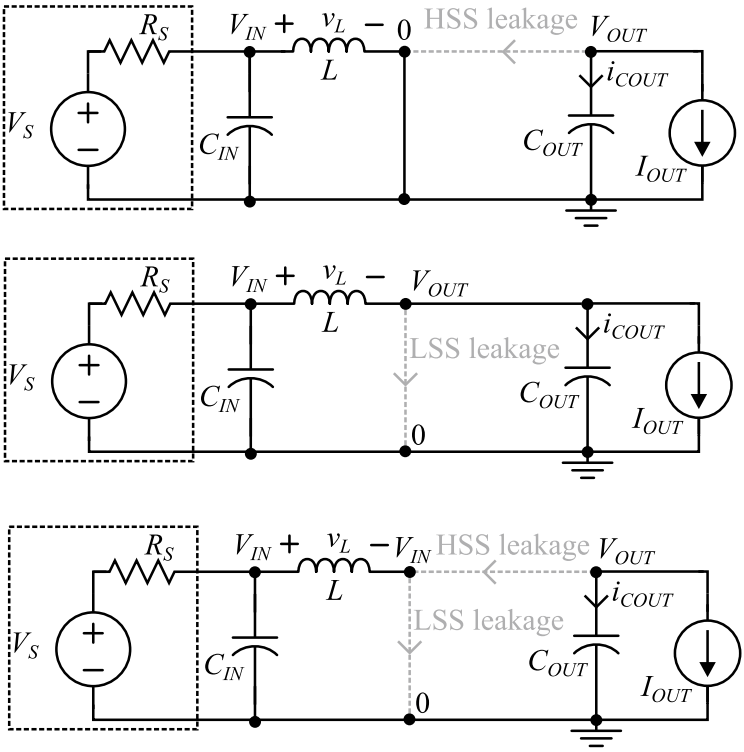

Fig. 5.11 Simplified equivalent circuit of the inductive boost converter during t_{ON} (top), t_{OFF} (middle), and t_D (bottom) including the leakage paths of the MOS switches

The total leakage losses are given by the sum of the leakage losses in the LSS (P_{LLSS}) and in the HSS (P_{LHSS}) during the three phases of operation. Assuming high-gain operation and that the transistors are in saturation, we approximate the leakage losses by

$$P_{LEAK} = P_{LHSS} + P_{LLSS} \approx I_{XQ,n} \frac{W_{LSS}}{L_{LSS}} V_{IN} + I_{XQ,p} \frac{W_{HSS}}{L_{HSS}} V_{OUT} \tag{5.43}$$

$I_{XQ,n(p)}$ in (5.43), which is calculated from the extrapolated saturation current (I_X) [6] defined in Chap. 1, is given by

$$I_{XQ,n(p)} = \mu_{n(p)} n C_{ox} \phi_t^2 e^1 e^{-\frac{\left|V_{TO,n(p)}\right|}{n\phi_t}}, \tag{5.44}$$

where n is the slope factor, and ϕ_t is the thermal voltage.

5.7.3 Dynamic Losses

The dynamic losses are due to the charging and discharging of capacitive nodes. The most relevant nodes for the dynamic losses are the gates of the LSS and HSS and the parasitic capacitance (C_{PAR}) of the intermediate node v_M (Fig. 5.9). The total dynamic losses, composed of three terms, the first due to the LSS (P_{DHSS}), the second due to the HSS (P_{DHSS}), and the third due to the parasitic capacitance (P_{DPAR}), can be approximated as

$$\begin{aligned} P_{DYN} &\approx P_{DLSS} + P_{DHSS} + P_{DPAR} \\ &\approx \frac{f_{SW} V_{OUT}^2}{2} (C_{ox} W_{LSS} L_{LSS} + C_{ox} W_{HSS} L_{HSS} + C_{PAR}). \end{aligned} \tag{5.45}$$

5.7.4 Losses in the Control Block

The losses in control block (P_{CTL}) account for the power consumption of circuits such as comparators, logic circuits, reference circuits, clock circuit, etc. Careful design and application of each of the building blocks should be carried out to keep these losses to a small fraction of the minimum specified P_{AV}.

5.7.5 *Maximizing the Conversion Efficiency*

To maximize the conversion efficiency, optimum values for the switches width, switching frequency, and duty cycle must be found.

5.7.5.1 Switches Sizing

The lengths of the switches ($L_{L(H)SS}$) are set to the minimum, since the losses are minimized for aspect ratios higher than the unity and minimum gate areas. The switches widths must be chosen to minimize the total losses of each switch. Both the leakage and dynamic losses are proportional to the transistor width, whereas the conduction losses are inversely proportional to the width. Hence, the optimum switch width is that which makes the sum of the leakage and dynamic losses equal to the conduction losses, yielding

$$W_{LSS,opt} = \left(\frac{2^{\frac{3}{2}}}{3} \frac{R_{S,LSS}}{\left(\frac{C_{ox} f_{SW} V_{OUT}^2}{2V_{IN}^2} + \frac{I_{XQ,n}}{V_{IN} L_{LSS}^2} \right) \left(R_S^3 L f_{SW} \right)^{\frac{1}{2}}} \right)^{\frac{1}{2}}, \tag{5.46}$$

$$W_{HSS,opt} = \left(\frac{2^{\frac{3}{2}}}{3} \frac{R_{S,HSS}}{\left(\frac{C_{ox} f_{SW} V_{OUT}^3}{2V_{IN}^3} + \frac{I_{XQ,p} V_{OUT}^2}{L_{HSS}^2 V_{IN}^3} \right) \left(R_S^3 L f_{SW} \right)^{\frac{1}{2}}} \right)^{\frac{1}{2}}. \tag{5.47}$$

With the aid of (5.46) and (5.47), the optimum switches widths can be calculated as a function of f_{SW}, as shown in Fig. 5.12. The dynamic, leakage and conduction losses of the switches, also presented in Fig. 5.12, were then calculated using the optimum values given by (5.46) and (5.47). For these calculations, we used parameters of the 130-nm technology and assumed $R_S = 100\ \Omega$, $V_{OUT} = 1$ V, and $V_{IN} = 50$ mV. The inductance was set to 1 μH. Higher inductance values allow for a reduction in f_{SW} (5.34) and, consequently, a reduction in the dynamic losses. However, to comply with practical values of inductance available in small form-factor inductors, a maximum value for the inductance should be defined by the designer.

Based on the results in Fig. 5.12, it is possible to determine the optimum value of f_{SW} that minimizes the losses in each of the switches. It can be observed that the f_{SW} values that minimize the losses of the LSS and the HSS differ. Hence, a complete analysis that takes into account the overall converter losses (P_{LOSS}) should be performed to determine the optimum f_{SW} for the design.

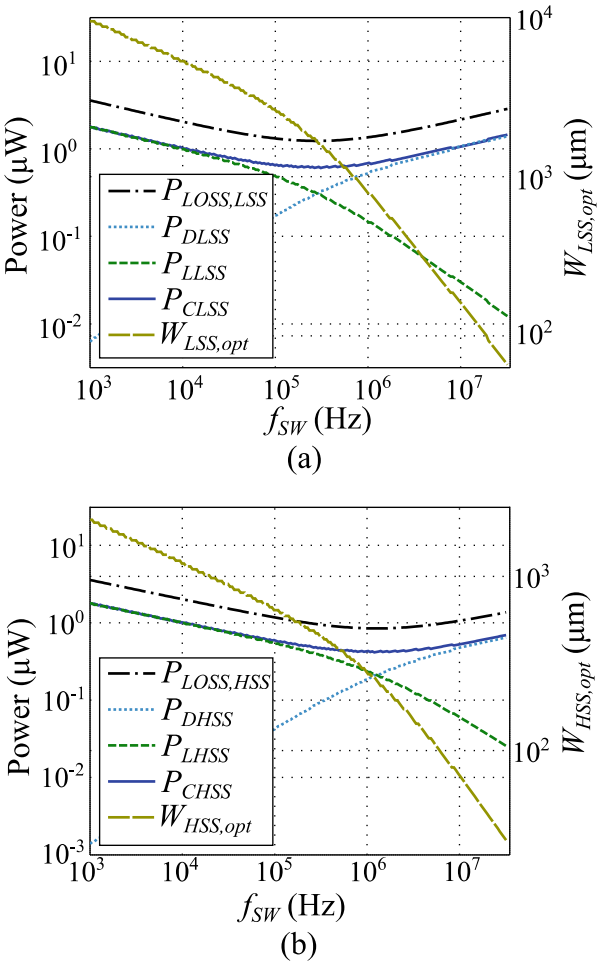

Fig. 5.12 Power losses and optimum width of the (**a**) LSS and (**b**) HSS vs f_{SW} ($\phi_t = 25$ mV, $n = 1.2$, $L_{HSS} = L_{LSS} = 0.12$ μm, $\mu_n = 0.05928.10^{12}$ μm^2/Vs, $\mu_p = 0.0134.10^{12}$ μm^2/Vs, $V_{T0,n(p)} = 200$ mV, $C_{ox} = 11.10^{-15}$ F/μm^2)

5.7.5.2 Switching Frequency and Duty Cycle

Optimum values of f_{SW} and D should be chosen for the minimization of P_{LOSS}. For the same design specifications used in Fig. 5.12, and assuming $R_L = 0.1\ \Omega$ (obtained from the known value of Q at the switching frequency), $C_{PAR} = 10$ pF and $P_{CTL} = 100$ nW, the power losses versus f_{SW} are shown in Fig. 5.13. From these results, the conversion efficiency can be calculated as a function of f_{SW}, thus allowing the determination of the optimum f_{SW}. The optimum switches widths that minimize P_{LOSS} can then be calculated by (5.46) and (5.47) using the optimum value of f_{SW}. Also, for the optimum f_{SW}, there is a corresponding D value calculated by (5.34) that maximizes the conversion and extraction efficiency. Figure 5.14 shows the conversion efficiency, the switches widths, and the duty cycle D in terms of f_{SW}.

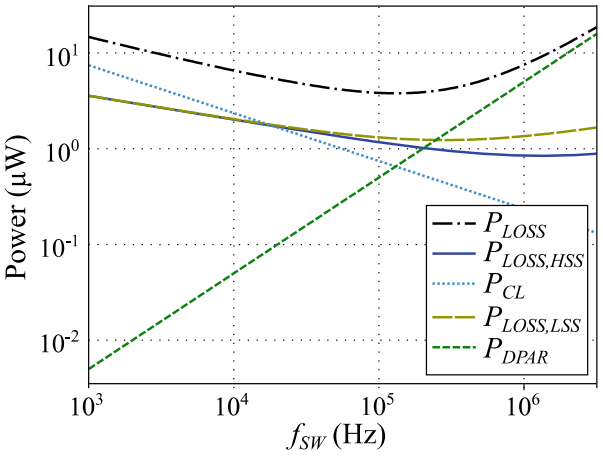

Fig. 5.13 Power losses versus f_{SW}

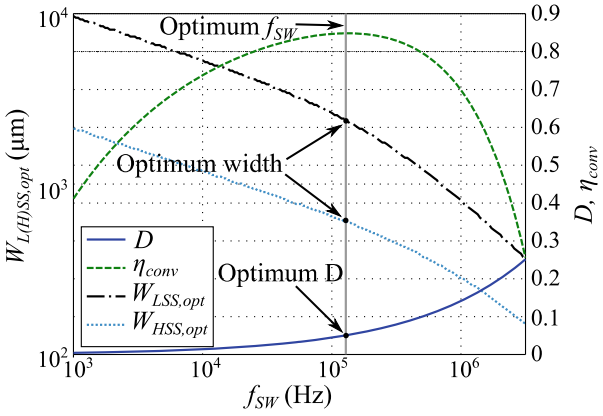

Fig. 5.14 Conversion efficiency, duty cycle, and switches widths versus f_{SW}

5.7.6 *Zero-Current Switching Schemes*

In a practical implementation of the boost converter, the LSS is generally controlled by a pulse signal that sets f_{SW} and t_{ON} (or, equivalently, D). The control of the HSS requires a more complex solution since the inductor discharging time is a function of the input voltage, which is a dynamic parameter in a typical energy-harvesting application. Hence, in DCM, the control circuit needs to sense the inductor current, detect the zero-current crossing, and instantly open the HSS. The delayed opening of the HSS leads to a negative current that drains charges from the output capacitor. Also, a premature opening of the HSS impedes the energy stored in the inductor to be fully transferred to the output. These two mechanisms of efficiency reduction are designated as synchronization losses (P_{SYNC}), because they are dependent on the correct timing of the opening of the HSS and further affect the conversion efficiency beyond the losses considered in (5.37).

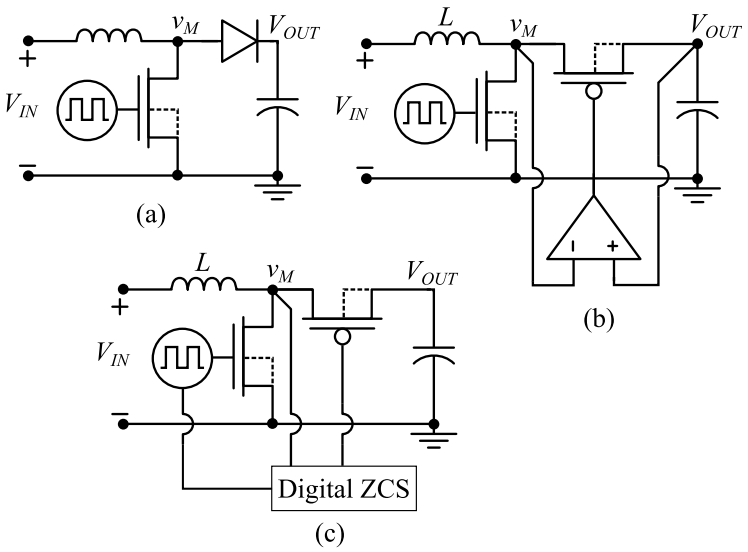

Fig. 5.15 Simplified schematics of ZCS approaches including (**a**) a diode as the HSS, (**b**) a MOS switch controlled by a comparator, and (**c**) a MOS switch controlled by a digital ZCS scheme

The simplest approach to zero-current switching (ZCS) is the use of a diode as the HSS (Fig. 5.15a) [7–10]. However, this strategy is not appropriate for Ultra-Low-Voltage applications due to tradeoffs involving the diode leakage current and forward voltage drop. A MOS switch controlled by ZCS schemes is usually employed as the HSS, since this can improve the conversion efficiency when compared with the solution employing a diode. The ZCS circuits used in this type of solution should detect the zero-current crossing and open the HSS of the boost converter at an instant close to the zero crossing of the inductor current.

Some designs use voltage comparators [5] to sense the voltage drop across the HSS to detect the zero-current crossing (Fig. 5.15b). However, since the HSS resistance is low when the switch is closed, the voltage drop across the HSS when the current is close to zero is also very low, making this type of solution inherently prone to error. Also, the consumption of comparators can impair the conversion efficiency, especially at low P_{AV}.

Another common approach to realizing the ZCS involves the use of digital schemes to detect the zero-current crossing through an indirect variable, which is the voltage v_M (Fig. 5.15c) [3, 11–15]. Due to the adoption of a digital solution, the static power consumption of the ZCS scheme is reduced. The main design challenges associated with this solution are the prevention of the high detection error that usually occurs at low V_{IN} and the setting of the appropriate time for the measurement of v_M.

To open the HSS close to the zero-crossing of the current, the ZCS circuit proposed in [4, 13] improves the detection accuracy by adopting both an appropriate timing for the measurement of v_M and a nonlinear division of the t_{OFF} (and V_{IN})

range, which increases the detection accuracy at low V_{IN}. This solution is analyzed in Chap. 6, where the expressions for the synchronization losses are presented for this approach.

5.8 Output Capacitor and Ripple

In a complete energy-harvesting interface, the output of the converter can be connected to energy reservoirs, such as batteries or supercapacitors, used to store energy when the connected load is not consuming the available power. For this type of solution, the output voltage is generally regulated by additional conversion stages (buck converter, LDO, etc.). When the boost converter directly supplies the output load without the use of energy reservoirs, the value of the output capacitor should be properly set to keep the output ripple within acceptable limits.

To define the value of the output capacitor based on ripple specifications, observe that $I_{OUT} = -I_{COUT}$ during t_{ON} and t_D. Therefore, assuming the converter is operating under high gain, the output ripple is given by

$$\Delta V_{OUT} = \frac{I_{OUT}(t_{ON} + t_D)}{C_{OUT}} \approx \frac{I_{OUT}(T)}{C_{OUT}}. \tag{5.48}$$

Using (5.13) and (5.16), and assuming that the Lf_{SW} product should comply with (5.34), we rewrite (5.48) as

$$\Delta V_{OUT} = \frac{V_{OUT}}{R_S f_{SW} M^2 C_{OUT}}. \tag{5.49}$$

Thus, one can determine the output capacitance from

$$C_{OUT} = \frac{1}{R_S f_{SW} M^2 \frac{\Delta V_{OUT}}{V_{OUT}}}. \tag{5.50}$$

To calculate C_{OUT} for the worst condition, M should be the minimum value of the gain factor, which can be estimated from the maximum input voltage specified for the converter.

5.9 Input Capacitor and Ripple

The input ripple is calculated using the input-capacitor current i_{CIN} shown in Fig. 5.16a, which is obtained by applying the KCL at the input node. For this analysis, we assume high-gain operation ($t_{ON} \gg t_{OFF}$) and approximate the input-

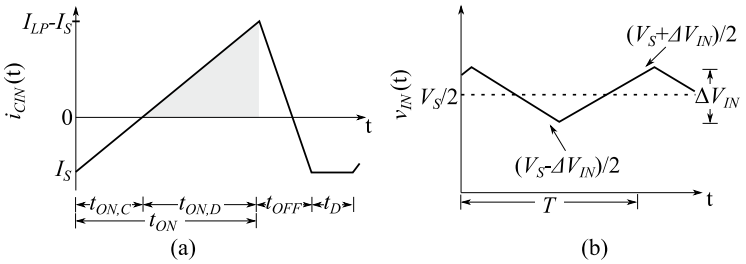

Fig. 5.16 (**a**) Input capacitor current and (**b**) representation of the ripple at the input of the boost converter

capacitor discharging time by $t_{ON,D}$, which can be calculated by a simple trigonometric relation, given in Fig. 5.16a, yielding

$$t_{ON,D} = t_{ON}\left(\frac{I_{LP} - I_S}{I_{LP}}\right). \tag{5.51}$$

Thus, the input voltage ripple can be obtained from the voltage-current relationship at the input capacitor

$$\Delta V_{IN} = \frac{1}{C_{IN}}\int_{t_{ON,C}}^{t_{ON}} i_{CIN}(t)\partial t = \frac{1}{C_{IN}}\left(\frac{I_{LP} - I_S}{2}\right)t_{ON,D} = \frac{t_{ON}}{2I_{LP}C_{IN}}(I_{LP} - I_S)^2. \tag{5.52}$$

Using (5.32), (5.52) can be rewritten as

$$\Delta V_{IN} = \frac{D^2 V_{IN}}{2C_{IN}L{f_{SW}}^2}\left(1 - \frac{D}{2}\right)^2. \tag{5.53}$$

Therefore, assuming that the input impedance is matched for MPPT according to (5.34), it is possible to define the input capacitor value based on the percentage ripple at the input, yielding

$$C_{IN} = \frac{1}{\left(\frac{\Delta V_{IN}}{V_{IN}}\right)R_S f_{SW}}\left(1 - \sqrt{\frac{Lf_{SW}}{2R_S}}\right)^2 = \frac{1}{\left(\frac{\Delta V_{IN}}{V_{IN}}\right)R_S f_{SW}}\left(1 - \frac{D}{2}\right)^2. \tag{5.54}$$

To obtain the appropriate value for C_{IN}, we investigate the effect of the input ripple on the extraction efficiency, which is given by

$$n_{extr} = \frac{1}{P_{AV}}\frac{1}{T}\int_0^T v_{IN}(t)[i_S(t) - i_C(t)]\partial t \cong 2 - \frac{4}{{V_S}^2}V_{IN,RMS}^2 \tag{5.55}$$

The approximation in (5.56) is valid for small-percentage ripple. Assuming the charging and discharging of the input capacitor to be linear, as represented in Fig. 5.16b, we have

$$V_{IN,RMS}^2 = \left(\frac{V_s}{2}\right)^2 + \left(\frac{\frac{\Delta V_{IN}}{2}}{\sqrt{3}}\right)^2 \tag{5.56}$$

Substituting (5.56) into (5.55) yields

$$n_{extr} = 1 - \frac{1}{12}\left(\frac{\Delta V_{IN}}{V_{IN}}\right)^2. \tag{5.57}$$

Hence, once an acceptable value for the extraction efficiency is specified, the proportional input ripple is calculated using (5.57), allowing the value of the input capacitor to be determined with (5.54).

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Chapter 6
Ultra-Low-Voltage Boost Converter for Energy-Harvesting Applications

6.1 Introduction

Recent developments in energy harvesting have been focused on ultra-low-voltage (ULV) operation using switched-inductor converters as an efficient means of DC-DC conversion [1–8]. Although switched-capacitor converters [9–11] have the advantage of a fully integrated implementation, the minimum input voltage for operation of this type of converter is generally high (typically above 100 mV), and the efficiency is low when compared with switched-inductor converters, especially at low input voltages, being inappropriate for ULV operation.

Inductive converters can provide efficient operation with input voltages well below 100 mV, but an off-chip inductor and capacitors are required. Since inductive converters are not able to self-start at low input voltages, auxiliary cold-starter circuits are used to provide the startup, which can be achieved at ultra-low voltages when off-chip components with a high-quality factor (Q) are employed [1, 2, 12–14].

In this chapter, an ultra-low-voltage converter, which uses an efficient inductive converter for steady-state operation and an ultra-low-voltage cold starter for system startup, was designed to fulfill the following requirements:

- Achieve startup and operate efficiently at low-input-voltage levels, typically provided when harvesting thermal energy from the human body or solar energy in indoor environments.
- Operate efficiently from different types of transducers, accommodating a wide range of input voltages and internal resistances (R_S), and provide a stable and adequate output voltage under several input conditions;
- Provide an output voltage level of around 0.7 to 1 V, which is high enough to supply low-power Internet-of-Things (IoT) devices;
- Provide high end-to-end efficiency for an available power (P_{AV}) in the range of μW to mW, which is the common range required by low-power IoT devices.

R. L. Radin et al., *Ultra-low Voltage Circuit Techniques for Energy Harvesting*,
Analog Circuits and Signal Processing, https://doi.org/10.1007/978-3-031-04492-2_6

6.2 Converter Architecture

Targeting the startup and operation from very-low input voltages, a step-up converter for ULV energy-harvesting applications was designed and integrated in a 130-nm CMOS technology. A block diagram of the converter architecture is shown in Fig. 6.1.

The converter is comprised of the cold starter, the main boost converter, and the control circuit. The cold starter is used to establish a temporary supply voltage (V_{DDCS}) at the beginning of the converter operation to power the control circuit, thus enabling the startup of the inductive boost converter. The main goal of the cold starter is to provide a V_{DDCS} of approximately 500 mV and a current of 100 nA, which are sufficient to supply the control circuit for the switching of the boost converter. The implemented cold starter is detailed in Sect. 6.4.

The inductive boost converter is employed to perform efficient voltage conversion in a steady sate. In the architecture of Fig. 6.1, the boost converter is implemented with two low-side switches (LSSs), $\mathrm{LSS_{AB}}$ and $\mathrm{LSS_C}$, which are employed during the boost converter startup and in steady state, respectively.

The control block was designed to perform three main roles: (i) to control the states of the high-side switch (HSS) and of the LSSs of the boost converter within each operation cycle through the adoption of a clock circuit and a zero-current-switching (ZCS) circuit; (ii) to coordinate the V_{DD} buildup during the startup sequence; and (iii) to limit the output voltage to around 1 V.

The types and sizes of the transistors used as the converter switches are shown in Table 6.1.

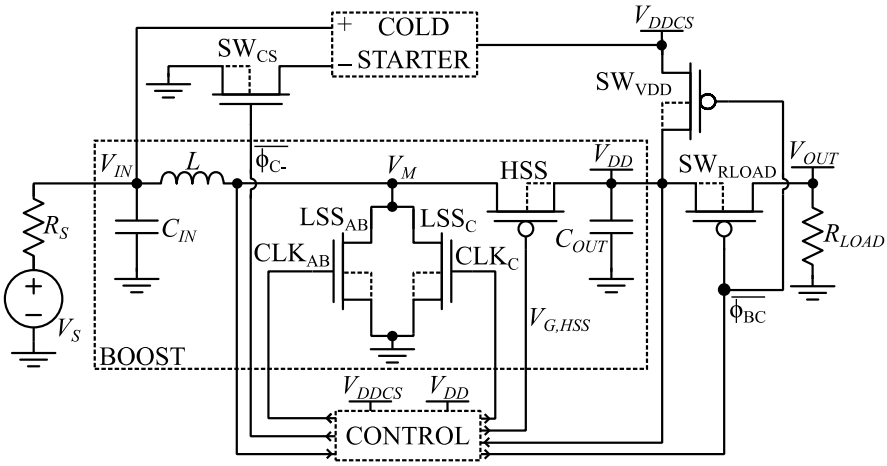

Fig. 6.1 Schematic showing the converter architecture

Table 6.1 Transistors of the converter switches

Device	Type	m × W (μm)[a]	L (nm)
LSS_{AB}	Low-V_T (LVT) NMOS	60 × 20	120
LSS_C	LVT NMOS	150 × 20	120
HSS	Standard PMOS	120 × 20	120
SW_{CS}	Zero-V_T (ZVT) NMOS	100 × 20	420
SW_{VDD}	Standard PMOS	60 × 20	120
SW_{RLOAD}	Standard PMOS	150 × 20	120

[a]m is the number of transistors in parallel

6.3 V_{DD} Buildup

Once the converter starts up, it commutes between three distinct phases of operation, building up the V_{DD} voltage from zero volts to the steady-state value. The buildup sequence allows different circuit configurations to minimize low-voltage startup and maximize the steady-state efficiency.

6.3.1 Phase A

When the primary source (V_S) is connected to the converter input, the cold starter turns on, establishing the voltage V_{DDCS} that powers the control circuit, hence providing the switching of the boost converter and giving rise to the buildup of node V_{DD}. During this phase, node V_{DDCS} powers only the part of the control circuit responsible for the clock generation and for keeping SW_{RLOAD} and SW_{VDD} in the open state. A simplified equivalent circuit of the converter in phase A is shown in Fig. 6.2.

In this phase, the load is disconnected from the output to avoid unnecessary consumption during startup and therefore $V_{OUT} = 0$ V. To reduce the dynamic losses, a small switch (LSS_{AB}), with an area close to a third that of LSS_C, is used during startup. The dynamic losses of the LSS, which impose a significant load at the cold starter output node (V_{DDCS}), should be minimized to achieve a low startup voltage. A narrower switch increases the conduction losses, but this is not of concern regarding the inefficient cold starter since these losses are supplied directly by the transducer. During this phase, the ZCS circuit is bypassed and $V_{G,HSS}=V_{DD}$; thus, the HSS is equivalent to a diode-connected MOSFET.

6.3.2 Phase B

When V_{DD} reaches approximately 530 mV, the converter commutes to phase B. During this phase, node V_{DDCS} is connected to node V_{DD}, which is now responsible

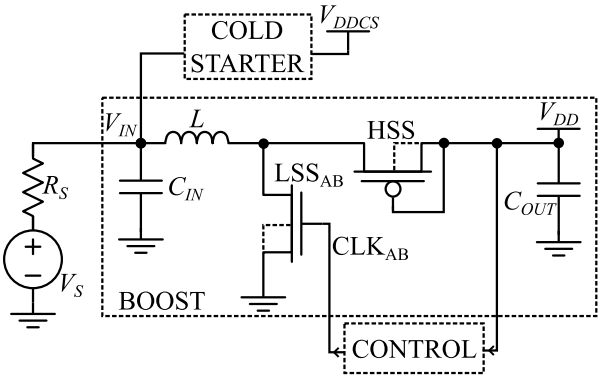

Fig. 6.2 Simplified equivalent circuit of the converter during phase A

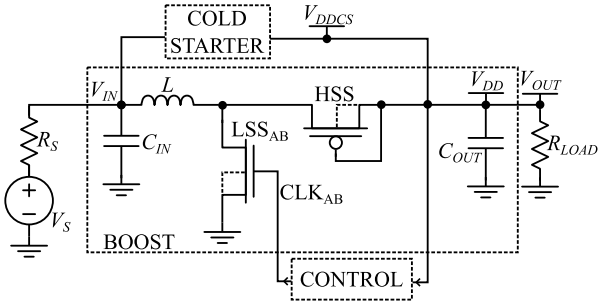

Fig. 6.3 Simplified equivalent circuit of the converter during phase B

for powering the whole circuit, as represented in Fig. 6.3. The load is connected to the output, and thus, $V_{OUT} = V_{DD}$=V_{DDCS}.

6.3.3 *Phase C*

When V_{DD} equals 660 mV, the cold starter is turned off to avoid unnecessary power consumption, and the ZCS circuit starts to operate. LSS_{AB} is replaced by a wider switch, LSS_C, which is sized to minimize the overall losses. During phase C, the circuit reaches the steady state, and the equivalent circuit in this phase is shown in Fig. 6.4.

When the boost converter operates in discontinuous conduction mode (DCM) under high conversion gain, the output voltage can be determined using expression (5.18), repeated as follows:

$$V_{OUT} \cong \frac{D^2 {V_{IN}}^2}{2Lf_{SW}I_{OUT}}, \tag{6.1}$$

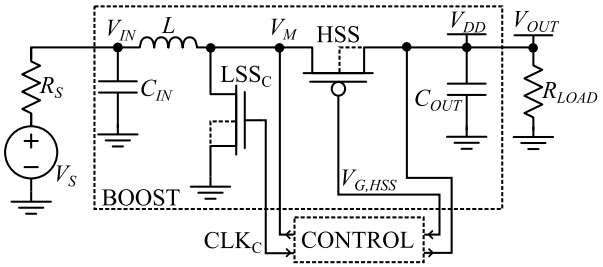

Fig. 6.4 Converter equivalent circuit during phase C

In our design, the switching frequency (f_{SW}), boost inductance (L), and duty cycle (D) are fixed parameters; therefore, during circuit operation, the output voltage is dependent only on V_{IN} and I_{OUT}. To avoid an increase in the output voltage under the condition of low output current and/or high input voltage, the control circuit temporarily disables the clock, interrupting the boost operation for a certain amount of time, to limit the output voltage to around 1 V. The control mechanism responsible for the limiting of V_{OUT} is explained in Sect. 6.3. Thus, in steady-state operation, the converter can operate in two distinct ways, namely, with non-limited or limited V_{OUT}, as described next.

- Non-limited V_{OUT} – when V_{IN} and I_{OUT} lead to V_{OUT} between 0.6 and 1.0 V, the boost operation is continuously maintained. The output ripple for non-limited V_{OUT} is a function of C_{OUT}, for which the value was determined in Sect. 5.8. The maximum power point tracking (MPPT) is given by (5.34), which sets the value of the Lf_{SW}.
- Limited V_{OUT} – when V_{IN} and/or I_{OUT} lead to a value of V_{OUT}, which tends to be above 1 V, the limiting of V_{OUT} to 1 V takes place. The converter alternates between active (clock is on) and inactive (clock is off) states, with durations t_{AS} and t_{IS}, respectively. During the inactive state, in which the clock is disabled, the output capacitor provides the load current, and the harvesting ceases. Simulations of V_{OUT} limiting as well as of the clock voltage are shown in Fig. 6.5. For limited V_{OUT}, the output ripple, which can be observed in Fig. 6.6, is dependent on the hysteresis width set by the comparator that enables or disables the clock.

6.4 Control Circuit

The control block shown in Fig. 6.7 is comprised of a five-stage current-starved ring oscillator (CSRO) responsible for generating the clock signal, switch drivers, a V_{DD} sensing circuit, a voltage reference circuit, a negative voltage generator, hysteretic comparators, and the fully digital ZCS circuit used to guarantee an efficient DCM operation for both low and high input voltages. V_M is used to indirectly sense the zero crossing of the inductor current, as will be explained later. The instances inside the control block are powered by node V_{DDCS}, unless otherwise indicated in Fig. 6.7.

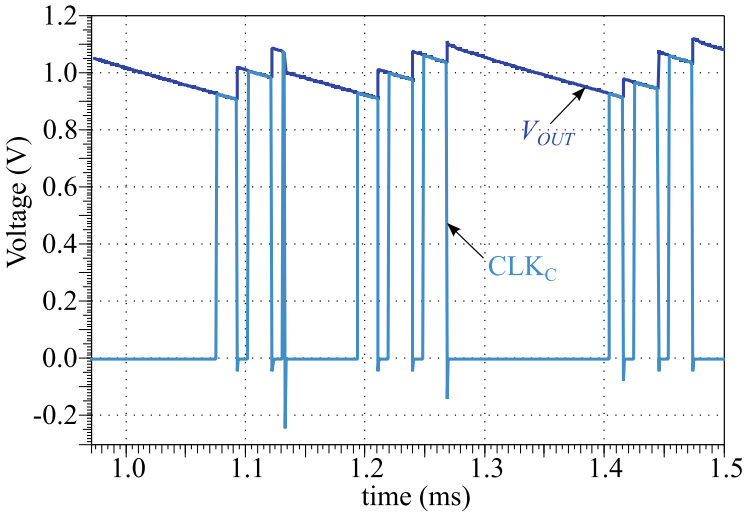

Fig. 6.5 Simulation of V_{OUT} limiting

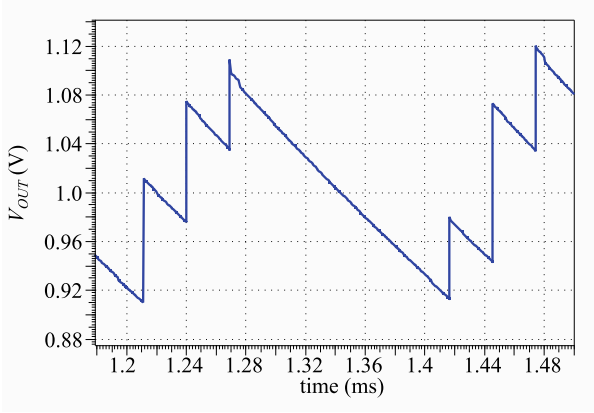

Fig. 6.6 Output ripple for V_{OUT} limited to approximately 1 V

During startup, V_{DD} is the main input variable of the control block, which is sensed and compared with a reference voltage. The comparators output the control signals used to open and close the switches of the converter, enabling different circuit configurations for each of the phases. Figure 6.8 shows the simulation results for the control signals generated in the control block during V_{DD} buildup.

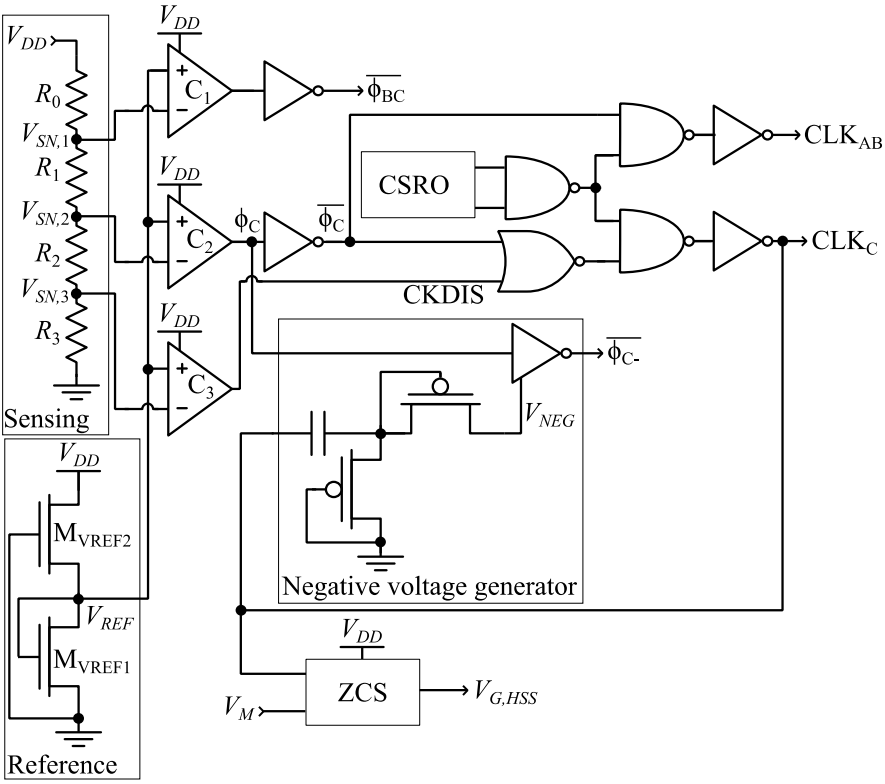

Fig. 6.7 Simplified schematic of the control circuit

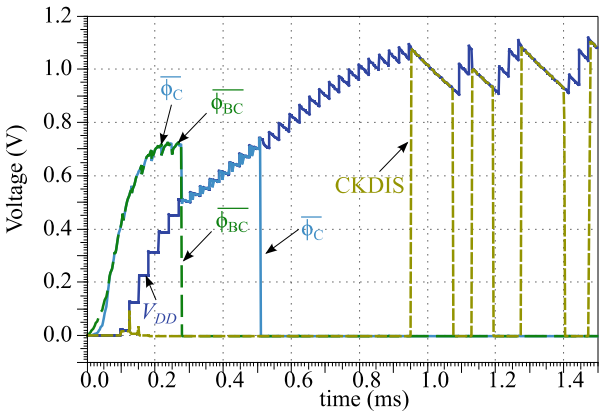

Fig. 6.8 Simulation results for the control signals

6.4.1 Voltage Reference

The voltage reference generator in Fig. 6.7, which uses two transistors, sets the voltage reference (V_{REF}) of the control circuit. The principle of operation of this circuit is detailed in [15]. For the proper functioning of the circuit, devices with different threshold voltages should be employed. Transistor M_{VREF1} is a standard-V_T thick-oxide device, and M_{VREF2} is a ZVT thick-oxide device. Using the transistor model described in Chap. 1, and assuming both transistors operate in weak inversion and have equal drain currents, we have

$$V_{REF} = \frac{1}{1+n_1}\left(n_1\phi_t \ln\left(\frac{\mu_{n,2}n_2\frac{W_2}{L_2}}{\mu_{n,1}n_1\frac{W_1}{L_1}}\right) + \left(V_{T0,1} - \frac{n_1}{n_2}V_{T0,2}\right)\right), \tag{6.2}$$

where n is the slope factor; $W_{1(2)}$ and $L_{1(2)}$ are the MOSFET channel width and length of $M_{VREF1(2)}$, respectively; $V_{T0,1(2)}$ is the equilibrium threshold voltage of $M_{VREF1(2)}$; $\mu_{n,1(2)}$ is the electron mobility of $M_{VREF1(2)}$; and ϕ_t is the thermal voltage.

The first term in parenthesis of the V_{REF} expression is proportional to the absolute temperature, whereas the second term is complementary to the absolute temperature. Therefore, the transistors can be sized to minimize the dependence of V_{REF} on the temperature. Figure 6.9a shows the dependence of V_{REF} on the temperature for several M_{VREF1} width values. A width of 28 µm was selected, because this value provided the best performance regarding temperature stability. For the chosen dimensions, the variation in V_{REF} is around 0.048% for a temperature range of −10 to 80 °C.

The circuit was also simulated to verify its stability against V_{DD} and process variations. The results are shown in Fig. 6.10. For $V_{DD} > 0.4$ V, V_{REF} varies 0.2% for V_{DD} varying from 0.4 to 1.2 V in the TT corner. For the SS and FF corners, a variation in V_{REF} of 3.2% was observed.

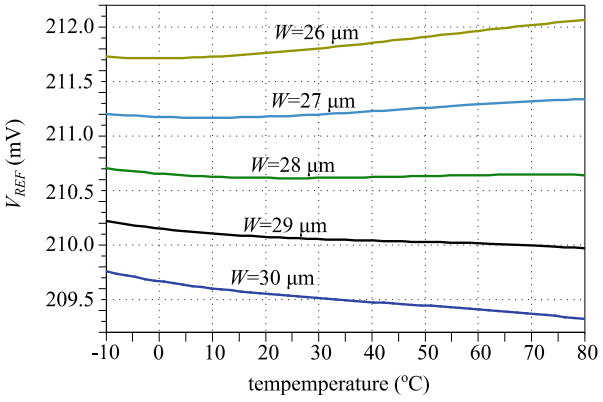

Fig. 6.9 V_{REF} vs temperature for different M_{VREF1} widths

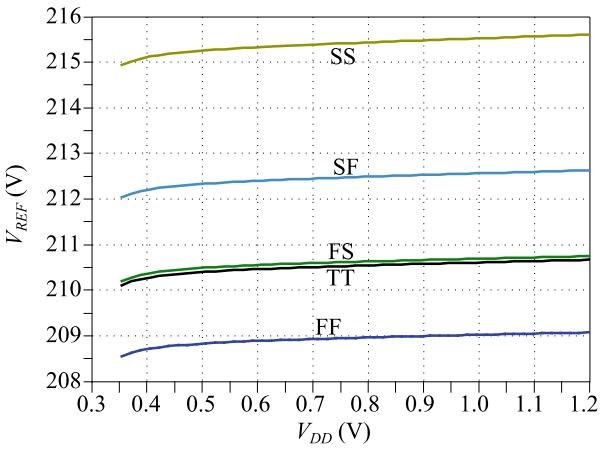

Fig. 6.10 V_{REF} vs V_{DD} for different corners

Table 6.2 Sizing of the reference generator transistors

Transistor	*W/L*	Type
M_{VREF1}	28 µm/30 µm	Thick-oxide NMOS
M_{VREF2}	33 µm/30 µm	Thick-oxide ZVT NMOS

The simulated results for V_{REF} show that the circuit stability against process, voltage, and temperature (PVT) variations is suitable for the requirements of this application, since the tolerance of V_{DD} levels for transition between phases is higher than the variations observed in simulations. The transistor sizes are shown in Table 6.2.

6.4.2 *Sensing Circuit*

The V_{DD} level is sensed by the resistive voltage divider in accordance with $V_{SN,i} = k_i V_{DD}$, where k_i is the attenuation of the voltage divider at node k_i. Hence, when comparing V_{REF} with the sensed voltages ($V_{SN,i}$), a change in the comparator state occurs for

$$V_{SN,i} = V_{REF} \pm \frac{V_{HYS}}{2}. \tag{6.3}$$

V_{HYS} is the hysteresis width, intentionally introduced in the comparator to avoid improper triggering. Thus, transitions occur for

Table 6.3 Parameters related to the sensing circuit

i	R_i (MΩ)	k_i	V_{DD} transition (V)
0	7	–	–
1	1	0.4	0.53 ± 0.038
2	1.25	0.32	0.66 ± 0.046
3	2.5	0.21	1.0 ± 0.07

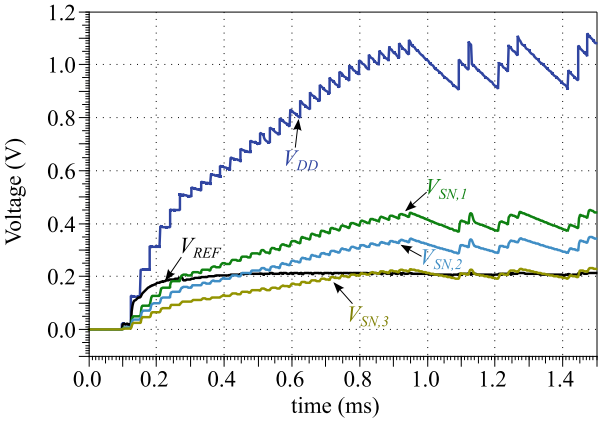

Fig. 6.11 Sensed voltages and V_{REF} during V_{DD} buildup

$$V_{DD} = \frac{V_{REF} \pm V_{HYS}/2}{k_i}. \tag{6.4}$$

Table 6.3 shows the values for the resistors of the voltage divider, the attenuation ratio k_i, and the V_{DD} values for the transition between phases. The simulation results for the voltages generated by the sensing circuit during the V_{DD} buildup are shown in Fig. 6.11.

6.4.3 Hysteretic Comparators

The comparators are used to control the state of switches SW_{RLOAD}, SW_{CS}, and SW_{VDD} and to activate/deactivate CLK_{AB} and CLK_C. Comparator C_1, responsible for the transition between phase A and phase B, controls the state of SW_{RLOAD} and SW_{VDD}. Comparator C_2 controls the transition from phase B to phase C, activating CLK_C, deactivating CLK_{AB}, and setting a control signal used by a negative voltage doubler to turn off the cold starter. C_3 is responsible for activating/deactivating CLK_C when V_{OUT} is being limited.

To avoid undesirable transitions at the output, the comparators were implemented with hysteresis [16]. The comparators are composed of three stages (Fig. 6.12): the preamplifier stage, the decision stage, and the output stage (Fig. 6.12). In the

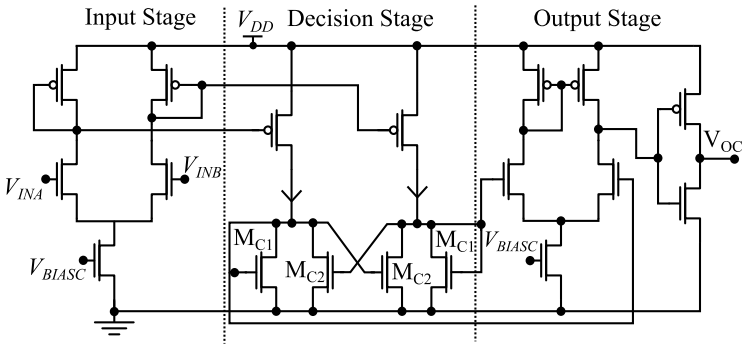

Fig. 6.12 Schematic of the comparator

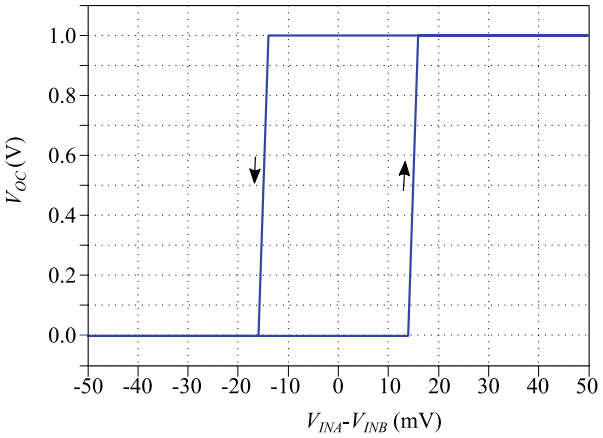

Fig. 6.13 DC transfer curve for the comparator showing the hysteretic behavior

decision stage, the difference in the transistor sizes directly affects the switching point ($M_{C1} \neq M_{C2}$) and sets the hysteresis width.

Figure 6.13 presents the DC transfer curve for the comparator. Since $V_{REF} \approx 211$ mV, the hysteresis of approximately ± 15 mV around V_{REF}, which is obtained for $M_{C2}/M_{C1} = 5$, translates into a hysteresis of ± 38 mV around V_{DD} for C_1, ± 46 mV for C_2 and $\pm$ 70 mV for C_3, as shown in Table 6.3.

The transition time of the comparator can be relatively high, due to the slowness of the signals being controlled (V_{DD} signal ramps up slowly, in the ms range). A transient analysis of the comparator is presented in Fig. 6.14, where the DC level of both V_{INA} and V_{INB} is equal to $V_{DD}/2$ and a sinusoidal signal is applied to V_{INA}. The average consumption of each comparator is around 55 nW for $V_{DD} = 1$ V, which is adequate for the targeted range of P_{AV}. The settling time for a load capacitance of 100 fF is around 1 µs.

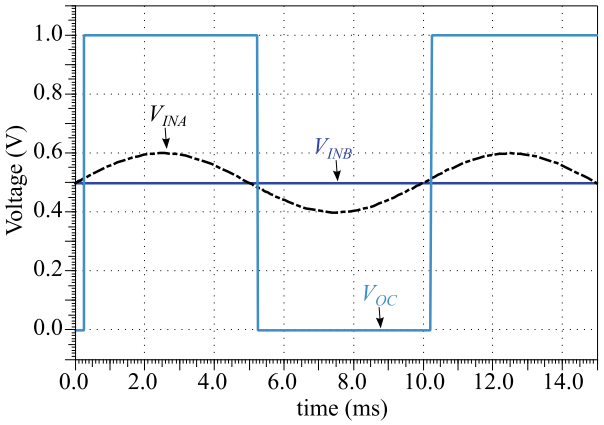

Fig. 6.14 Transient response of the comparator

6.4.4 Negative Voltage Generator

The consumption of the cold starter is around 115 μW for $V_{IN} = 80$ mV ($R_S = 5\ \Omega$), and thus, it should be turned off after V_{DDCS} has reached 660 mV to improve the system efficiency. In this work, the cold starter is comprised of a ULV oscillator and a charge pump. Therefore, a ZVT NMOS transistor (SW_{CS}) is used as a switch to interrupt the ULV oscillator connection to ground in phase C, effectively interrupting the operation of the cold starter. Due to the ZVT characteristics, a negative voltage needs to be generated to effectively turn off the cold starter.

Using the CLK_C signal, we implemented a negative voltage doubler (Fig. 6.7) with the conventional topology of a clamp followed by a peak detector to generate a negative voltage (V_{NEG}). The output capacitor of the voltage doubler is the input capacitance of SW_{CS}, and the ZVT transistor should thus be sized considering three distinct aspects: firstly, the ON series resistance should not significantly affect the minimum V_{IN} for startup; secondly, the switch should effectively turn off the oscillator in steady state; and thirdly, the gate capacitance of the switch should provide an acceptable ripple level.

For the oscillator shutdown in phase C, we use an inverter for which V_{DDCS} and V_{NEG} are the supply rails (Fig. 6.7). Therefore, during phases A and B, the inverter outputs V_{DDCS}, while during phase C, the inverter outputs V_{NEG}. Figure 6.15 shows the transient simulation of the control signal that turns off the ULV oscillator of the cold starter when the converter commutes from phase B to phase C.

6.4.5 Clock Source

The clock circuit (Fig. 6.16) provides the signal for switching the LSS. It is also used for both the timing of the ZCS circuit and as the oscillatory signal used in the negative voltage doubler.

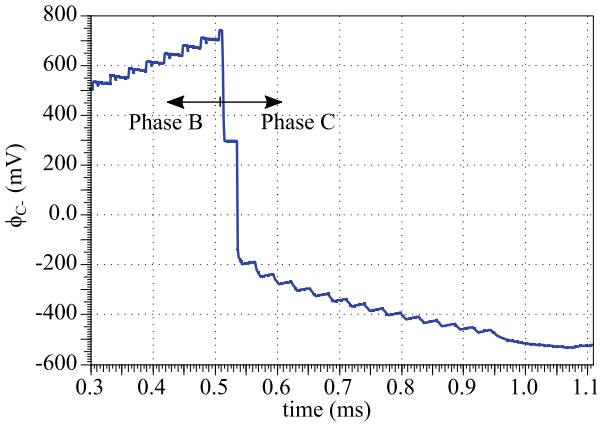

Fig. 6.15 Transient simulation of control signal used for the shutdown of the cold starter

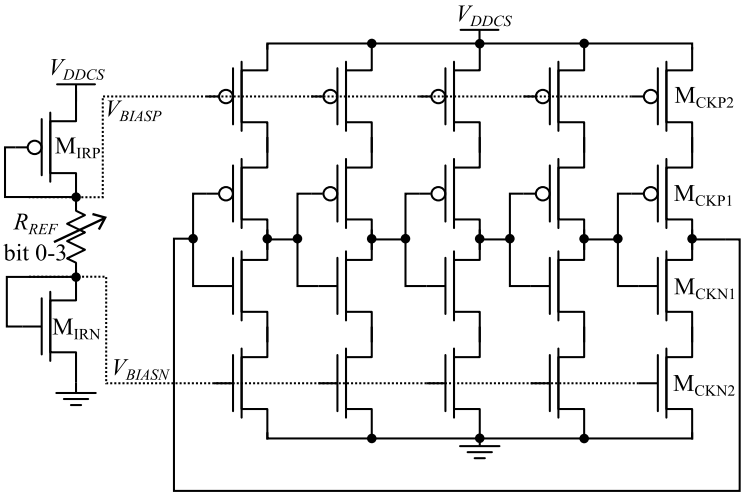

Fig. 6.16 Schematic of the clock and bias circuits

The clock is a five-stage CSRO in which the frequency can be fine-tuned by four external trimming bits to maintain V_{IN}=V_S/2. The switching frequency is set to around 30–40 kHz. The external trim bits enable the value of R_{REF} to be adjusted from 16 MΩ to 22 MΩ, which allows a variation of around 33% in f_{SW}. The f_{SW} variation can be used to compensate for tolerances of off-the-shelf inductors and process variations. The sizes of the transistors of the CSRO are given in Table 6.4. The simulation of the CSRO for the different corners resulted in a variation of 5.3% (FF), −0.8% (FS), −1.5% (SF), and + 0.36% (SS) in the oscillation frequency.

At the output of the CSRO, two signals from different stages are used by a NAND gate to generate an asymmetrical waveform with a duty cycle close to 0.7. This value allows a minimum voltage gain of 3.3 or, equivalently, the maximum input voltage

Table 6.4 Sizes of the clock circuit transistors

Transistor	*W/L*	Type
M_{CKP1}	2.5 µm/1 µm	Standard PMOS
M_{CKP2}	2 µm/2 µm	Standard PMOS
M_{IRP}	8 µm/2 µm	Standard PMOS
M_{CKN1}	700 nm/1 µm	Standard NMOS
M_{CKN2}	1 µm/2 µm	Standard NMOS
M_{IRN}	4 µm/2 µm	Standard NMOS

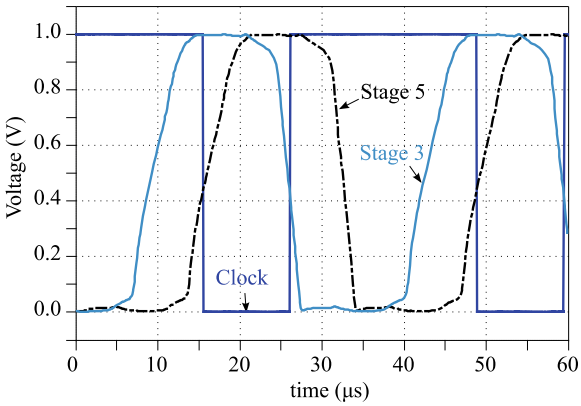

Fig. 6.17 Simulated signals of the third and fifth stages of the CSRO and the asymmetrical clock at the NAND output

of around 300 mV for $V_{OUT} = 1$ V under DCM operation, which are appropriate values for the given application. The results of post layout simulations of the outputs of the third and fifth stages as well as the asymmetrical clock signal after the NAND gate can be observed in Fig. 6.17.

After the generation of the asymmetrical clock, logic gates are used to enable and disable the signals CLK_{AB} and CLK_C during the different phases of operation. During phases A and B, CLKAB is enabled and CLK_C is disabled. In phase C, CLK_{AB} is always disabled, and CLK_C is enabled if the converter is active and disabled if it is inactive (limited V_{OUT}). Figure 6.18 presents the simulation of CLK_{AB} and CLK_C during V_{DD} buildup and in a steady state for a case in which V_{OUT} is limited after reaching Phase C.

6.4.6 *Zero-Current Switching*

The ZCS circuit shown in Fig. 6.19 [17] was designed to allow efficient DCM operation of the boost converter. The operation of our circuit is similar to those described in [7, 8, 18, 19], but the detection accuracy is improved, especially at low V_{IN}.

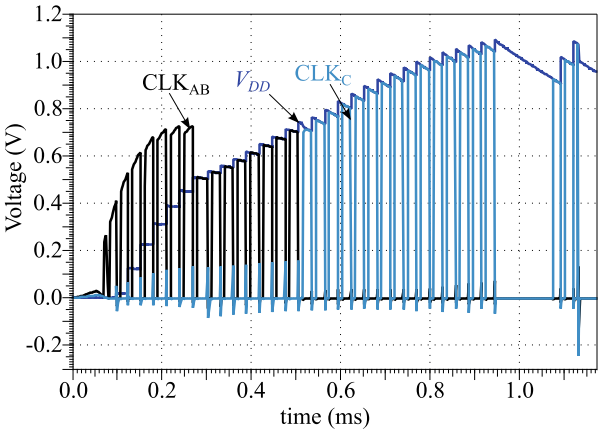

Fig. 6.18 Simulation of CLK_{AB} and CLK_C during V_{DD} buildup

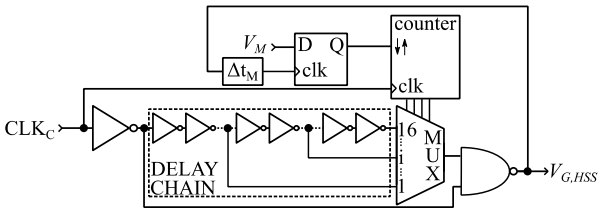

Fig. 6.19 Implemented ZCS circuit

The pulse signal generated by the ZCS circuit ($V_{G,HSS}$) controls the state of the HSS of the converter, keeping it closed during the inductor discharging time (t_{OFF}) and open during inductor idle (t_D) and charging (t_{ON}) times. Through the relation given by (5.16), each value of t_{OFF} fits a specific input voltage level, and when the converter operates under high voltage gain, this relation is nearly linear. Since V_{IN} is a dynamic variable, the pulse signal generated by the ZCS circuit has an adjustable width (t_{PW}), which ideally is very close to t_{OFF} of the corresponding V_{IN}. For this purpose, we adopted a four-bit system, allowing 16 different values of pulse width to cover the range of t_{OFF} and, consequently, the range of V_{IN}.

The ZCS circuit is comprised of a delay chain with 16 stages implemented with current-starved inverters to generate a pulse with variable width, the sensing flip-flop, the measurement delay (Δt_M) block, and the pulse selection circuit (multiplex +4-bit counter). The whole ZCS block is supplied with V_{DD}, since this block is used only after the converter has started up and reached phase C.

6.4.6.1 Operation Principle

The ZCS circuit senses the node V_M, which indirectly provides information about the late and early opening of the HSS, and based on the sensing results, it adjusts t_{PW} to best fit t_{OFF}. A D-type flip-flop is employed to sense the voltage V_M a certain time

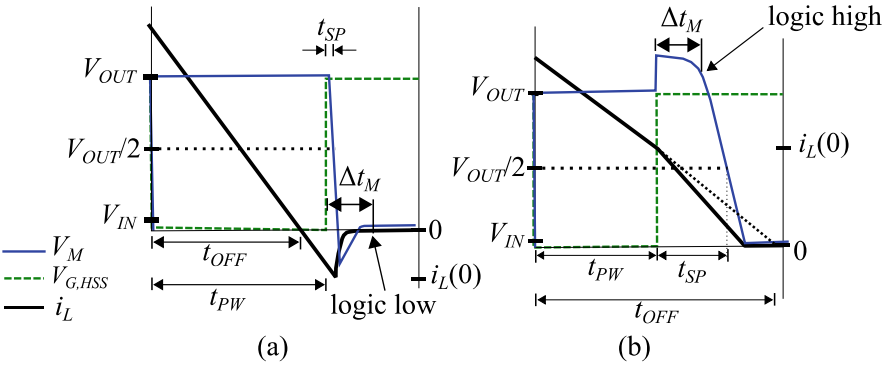

Fig. 6.20 i_L, $V_{G,HSS}$, and V_M for (**a**) late opening and (**b**) early opening

after the opening of the HSS (Δt_M). If the HSS opens after the zero-current crossing, the inductor current at the instant the HSS opens ($i_L(0)$) is negative, and V_M will rapidly shift from V_{OUT} to zero. On the other hand, if the HSS opens before the zero-current crossing ($i_L(0) > 0$), the inductor will still discharge through the HSS, which is now a high-resistance path, causing an overshoot at V_M, as represented in Fig. 6.20. Thus, if V_M is still higher than a specified switching point (logic high) a short time (Δt_M) after the opening of the HSS, early opening is detected. If V_M is lower than the switching point (logic low), late opening is detected by the sensing flip-flop.

Based on the result that is sensed by the flip-flop, the counter is then incremented or decremented, and the current pulse width applied to the gate of the HSS is increased or decreased, respectively. The counter controls a multiplexer, which selects one of the outputs of the delay chain and connects it to the pulse generation circuit, setting the pulse width. If t_{PW} is slightly narrower than t_{OFF}, early opening is detected, and t_{PW} is increased. On the other hand, if t_{PW} is wider than t_{OFF}, late opening is detected, and t_{PW} is decreased. After the system reaches convergence, t_{PW} will alternate around t_{OFF}.

6.4.6.2 The Measurement Delay and t_{SP}

The discrimination between low and high logic levels of V_M is performed by the sensing flip-flop. The measurement of V_M is taken at a certain time (Δt_M) after the opening of the HSS. A V_M value above the flip-flop switching point ($V_M > V_{OUT}/2$) indicates early opening, and a value lower than the switching point ($V_M < V_{OUT}/2$) is a sign of late opening. The time interval between the opening of the HSS and the crossing of V_M through the switching point of the sensing flip-flop ($V_{OUT}/2$) is defined as t_{SP}, as represented in Fig. 6.20. The value of t_{SP} is a function of both the circuit parameters and the initial conditions at the opening of the HSS.

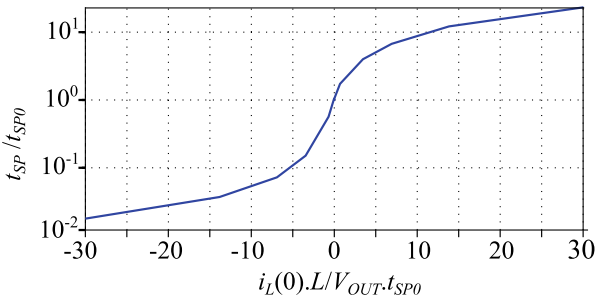

Fig. 6.21 Post-layout results for normalized t_{SP} vs $i_L(0)$, where t_{SP0} is the value of t_{SP} for $i_L(0) = 0$

The appropriate time to sense node V_M, which is critical for the accuracy of the ZCS scheme, is set by the measurement delay block comprised of two logic inverters. If Δt_M is set at a much lower value than t_{SP}, late opening can be wrongly interpreted as early opening. On the other hand, if Δt_M is set at a much higher value than t_{SP}, early opening can be wrongly interpreted as late opening.

The dependence of t_{SP} on the inductor current at the opening of the HSS ($i_L(0)$) was analyzed by simulation for $L = 33$ μH and $L = 220$ μH, where the initial condition for the inductor current was used as a parameter, and t_{SP} was measured by transient simulation. The results for normalized $i_L(0)$ are shown in Fig. 6.21.

As can be observed in Fig. 6.21, because t_{SP} is a monotonic function of $i_L(0)$, Δt_M should be set to a higher value than the t_{SP} of negative $i_L(0)$ to allow V_M to reach the switching point, thus providing the correct detection of late openings of the HSS. Also, Δt_M should be set to a lower value than the t_{SP} of positive $i_L(0)$, to prevent v_M from reaching the switching point, thus providing the correction detection of early openings of the HSS. Therefore, when Δt_M is calibrated to the value of t_{SP} for $i_L(0) = 0$ (t_{SP0}), early and late opening of the HSS are correctly discriminated. For a boost inductor of 33 μH, the simulated value of t_{SP0} was 13 ns, and for 220 μH, it was 33 ns.

If Δt_M is properly set to t_{SP0}, the pulse width values alternate around t_{OFF}, which causes alternating late and early opening of the HSS, and $i_L(0)$ continues to alternate around zero. However, inappropriate values of Δt_M might lead to an alternation around a different value of $i_L(0)$, and only early or only late opening could be generated, increasing the detection error and reducing the conversion efficiency. Figure 6.22 shows how the incorrect choice of the measurement delay affects the readings of logic levels.

6.4.6.3 Analytical Determination of t_{SP0}

To obtain an analytical expression for t_{SP0}, we analyze the time response of the second-order system comprised of the capacitance at node V_M (C_{MPAR}), inductance (L), and the parasitic resistance of the switches (Fig. 6.23) for $i_L(0) = 0$. Applying the Kirchhoff Current Law at node V_M [20], we have

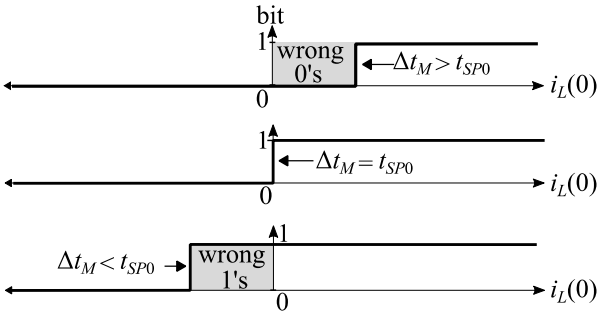

Fig. 6.22 Representation of the logic levels sensed for different Δt_M values

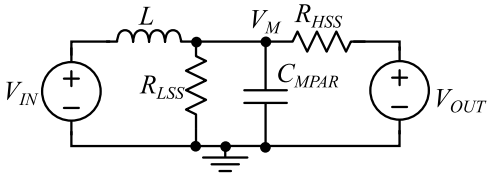

Fig. 6.23 Equivalent circuit for time response calculations

$$\frac{d^2V_M(t)}{dt^2} + 2\alpha\frac{dV_M(t)}{dt} + \omega_0^2 V_M(t) = \omega_0^2 V_{IN} \tag{6.5}$$

where

$$\omega_0 = \frac{1}{\sqrt{LC_{MPAR}}}, \alpha = \frac{1}{2(R_{LSS}//R_{HSS})C_{MPAR}}. \tag{6.6}$$

To obtain the time-domain expression for t_{SP}, the type of damping that occurs after the opening of the HSS should be firstly evaluated. Therefore, the values for the switch resistances and C_{MPAR} were obtained through post-layout simulations. When V_M ranges from V_{OUT} to $V_{OUT}/2$, the measured value of R_{LSS}/R_{HSS} ranges from 55 to 100 kΩ, and the measured value of C_{MPAR} is 4.6 pF. Thus, for the highest value of the boost inductance considered in this research ($L = 220$ μH when $R_S = 40$ Ω), we have $\omega_0 = 3.14 \times 10^7$ and $1.09 \times 10^6 \leq \alpha \leq 1.97 \times 10^6$. As a result, for the whole range of switch resistances and boost inductance values, we have a highly underdamped system ($\alpha \ll \omega_0$), and the time response follows the expression

$$V_M(t) = V_{IN} + (B_1 \cos(\omega_D t) + B_2 \sin(\omega_D t))e^{-\alpha t}, \tag{6.7}$$

where $\omega_D = \sqrt{\omega_0^2 - \alpha^2} \approx \omega_0$. Because $\alpha \ll \omega_0$, the V_M shift from V_{OUT} (when $t = 0$) to $V_{OUT}/2$ (when $t = t_{SP0}$) is associated with the sinusoidal terms; thus, the attenuation term imposed by α can be neglected. Also, assuming high gain operation ($V_{IN} \ll V_{OUT}$) and that $V_M = V_{OUT}$ for $t = 0$, for $i_L(0) = 0$, we approximate (6.7) as

$$V_M(t) = V_{OUT} \cos(\omega_D t) \tag{6.8}$$

Considering that V_M is equal to $V_{OUT}/2$ at the switching point ($t = t_{SP0}$), using (6.8), we have

$$t_{SP0} = \sqrt{LC_{MPAR}} \arccos 0.5 \approx 1.05\sqrt{LC_{MPAR}} \tag{6.9}$$

Hence, setting Δt_M equal to t_{SP0} given by expression (6.9) minimizes the detection error. The result obtained with (6.9) is in close agreement with the simulation results.

6.4.6.4 Pulse Scaling

To make t_{PW} as close as possible to t_{OFF}, we first define the zero-current detection error (ZCDE) for a given t_{OFF} and t_{PW} as

$$ZCDE = \frac{|t_{PW} - t_{OFF}|}{t_{OFF}} \tag{6.10}$$

Since in steady state the system alternates between two values of t_{PW}, one slightly narrower and one slightly wider than t_{OFF}, the overall ZCDE for the given t_{OFF} is the average of the ZCDE for the two alternating t_{PW} values. Using (6.10), the ZCDE was plotted as a function of V_{IN} in Fig. 6.24 for different bit resolutions, with a linear division of the t_{PW} range.

As can be seen, the ZCDE is increased for low input voltages, since the step size in this range is greater when compared with the respective t_{OFF}. To overcome this problem without resorting to a large number of bits, we propose the use of geometric scaling of the t_{OFF} range, in other words, decreasing the step size for low t_{PW}. The scaling factor (SF) and the pulse width generated by each of the delay outputs ($t_{PW}(i)$) are therefore given by

$$SF = \left(\frac{V_{IN,MAX}}{V_{IN,MIN}}\right)^{\frac{1}{n_{DS}-1}} \tag{6.11}$$

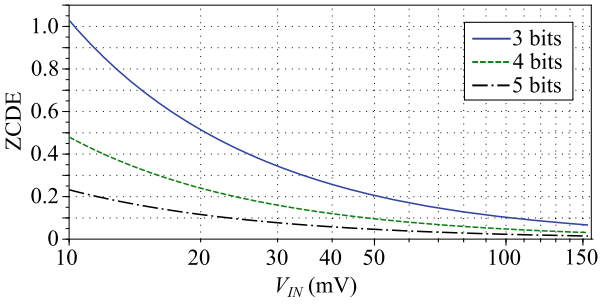

Fig. 6.24 Detection error for different bit resolutions

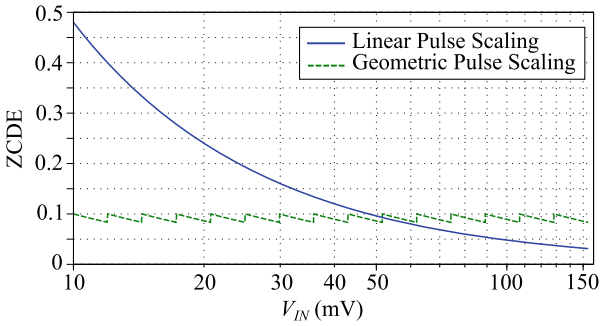

Fig. 6.25 Detection error for geometric and linear pulse scaling

$$t_{PW}(i) = SF^{i-1} t_{PW}(1) \tag{6.12}$$

where $V_{IN,MIN}$ and $V_{IN,MAX}$ are the specified minimum and maximum values of V_{IN}, respectively, and $n_{DS} = 2^b$ is the number of delay stages for a number of bits equal to b. The value of $t_{PW}(1)$ is equal to t_{OFF} for the case of V_{IN}=$V_{IN,MIN}$ and can be determined by the boost gain expression (5.16), since $V_{OUT} = 1$ V and t_{ON} is fixed. The detection error for geometric scaling is plotted in Fig. 6.25 along with the linear scaling of t_{PW} for a 4-bit resolution.

The geometric scaling equalizes the ZCDE across the whole V_{IN} range, mitigating the problems of detection accuracy in the low V_{IN} range, which results in a loss in the conversion efficiency. For early opening, some energy is lost in the HSS series resistance during the remaining discharging period of the inductor. On the other hand, late opening generates a reverse energy flow that partially discharges the output capacitor. Thus, with the aid of Fig. 6.20, we define the ZCS conversion efficiency (η_{ZCS}) as the ratio of the energy transferred to the load for a given t_{PW} (E_{TPW}) to the energy transferred to the load for the case of ideal ZCS (E_{ZCS}), which is obtained when $t_{PW} = t_{OFF}$, leading to

$$\eta_{ZCS} = \frac{E_{TPW}}{E_{ZCS}} = 1 - \frac{k_L (t_{OFF} - t_{PW})^2}{t_{OFF}{}^2} \tag{6.13}$$

For the case of $i_L(0) < 0$ (late opening), k_L has no meaning and is equal to 1. For the case of $i_L(0) > 0$ (early opening), k_L represents the fraction of the energy stored in the inductor at the opening of the HSS that is lost in the HSS. The k_L value is a function of the HSS off-resistance, and it can be estimated by simulation once the size of the HSS is defined.

Since, t_{PW} alternates between two values in steady state, the efficiency of the proposed ZCS scheme is given by the average of the efficiency given by (6.13) for the two alternating values of t_{PW}. Using (6.13), η_{ZCS} is plotted for the case of linear and geometric pulse scaling for a 4-bit system in Fig. 6.26.

Using the proposed scaling strategy, the current-starved inverters (Fig. 6.27) can be sized to generate a pulse width and delay in accordance with the values shown in Table 6.5. The final sizing of the delay chain devices, determined by simulation, is also presented in Table 6.5.

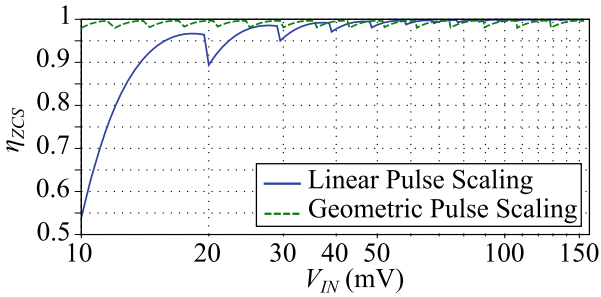

Fig. 6.26 Values of η_{ZCS} for geometric and linear pulse scaling ($k_L = 0.3$)

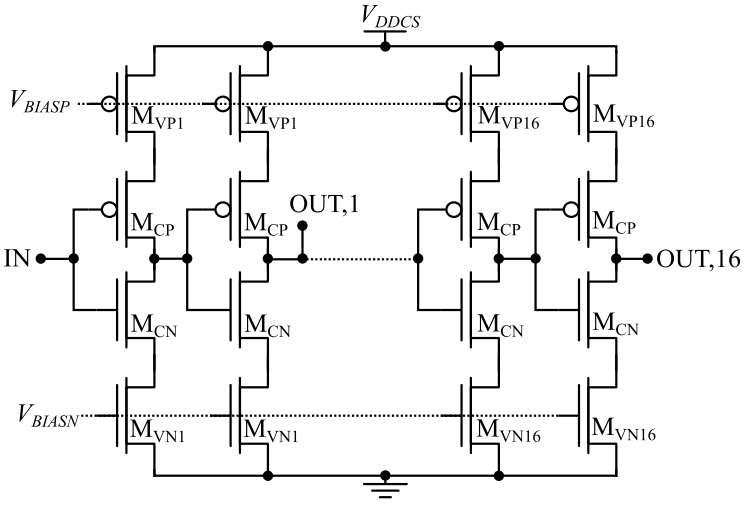

Fig. 6.27 Delay chain using current-starved inverters

Figure 6.28 shows the simulation results for the pulse width obtained for each stage [21] and the proportional deviation of each of the corners.

To evaluate the effect of Δt_M on the ZCDE and η_{ZCS}, we use the relation given in Fig. 6.21 and (5.11) to determine the two alternating values of t_{PW} for any given Δt_M and V_{IN}, enabling (6.10) and (6.13) to be calculated for the geometric pulse scaling. Considering our design parameters ($L = 220$ µH, $V_{IN,MIN} = 10$ mV, $V_{IN,MAX} = 154$ mV, $SF = 1.2$ and $n_{DS} = 16$), we plot ZCDE and η_{ZCS} vs V_{IN} for different values of Δt_M in Figs. 6.29 and 6.30, respectively.

As can be observed, setting Δt_M according to (6.9) maximizes the efficiency, which can be significantly impaired as Δt_M deviates from t_{SP0}. It should be noted that when Δt_M is properly set by (6.9), the results are equal to those in Figs. 6.25 and 6.26 for the geometric scaling, as expected.

Table 6.5 Sizing of current-starved inverters, pulse width, and delay time of each stage

Stage	Device	Width	Pulse width	Delay
1	$M_{VN(P)1}$	5.5 µm[a]	250 ns	250 ns
2	$M_{VN(P)2}$	6.83 µm	300 ns	50 ns
3	$M_{VN(P)3}$	5.9 µm	360 ns	60 ns
4	$M_{VN(P)4}$	5.4 µm	432 ns	72 ns
5	$M_{VN(P)5}$	4.85 µm	518 ns	86 ns
6	$M_{VN(P)6}$	4.15 µm	622 ns	104 ns
7	$M_{VN(P)7}$	3.5 µm	746 ns	124 ns
8	$M_{VN(P)8}$	3.05 µm	895 ns	149 ns
9	$M_{VN(P)9}$	2.6 µm	1.07 µs	179 ns
10	$M_{VN(P)10}$	1.87 µm	1.29 µs	215 ns
11	$M_{VN(P)11}$	1.54 µm	1.55 µs	258 ns
12	$M_{VN(P)12}$	1.35 µm	1.86 µs	310 ns
13	$M_{VN(P)13}$	1.17 µm	2.23 µs	372 ns
14	$M_{VN(P)14}$	1 µm	2.68 µs	446 ns
15	$M_{VN(P)15}$	850 nm	3.21 µs	535 ns
16	$M_{VN(P)16}$	720 nm	3.85 µs	642 ns

[a]The first stage is comprised of five cascaded stages, each calibrated for a 50-ns delay. The length of all transistors is 1.2 µm

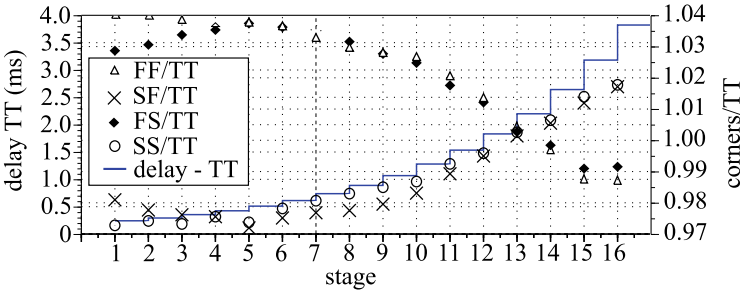

Fig. 6.28 Pulse width and corner deviation of each delay chain stage

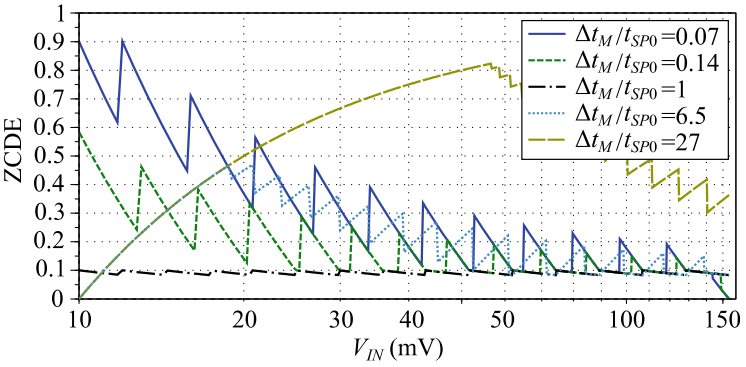

Fig. 6.29 ZCDE vs V_{IN} for different Δt_M values using geometric pulse scaling

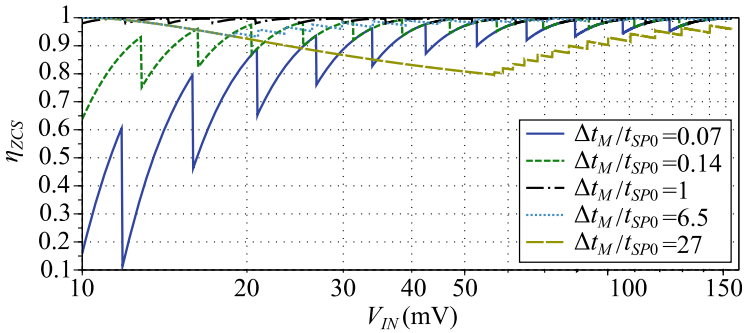

Fig. 6.30 Plot of η_{ZCS} vs V_{IN} for different Δt_M values using geometric pulse scaling ($k_L = 0.3$)

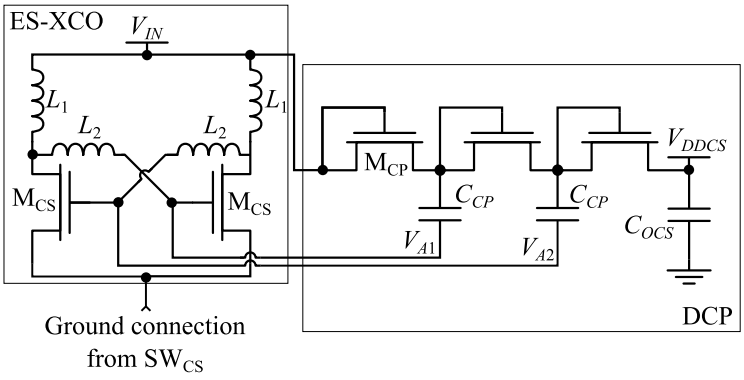

Fig. 6.31 Schematic of the implemented cold starter

Table 6.6 On-chip devices of the cold starter

Device	Value or size
M_{CS}	ZVT − (90 × 20) µm/420 nm
M_{CP}	8 µm/120 nm
C_{OCS}	12.8 pF
C_{CP}	1.41 pF

6.5 Cold Starter

A cold starter employing off-chip inductors was designed through parametrical analysis in Cadence Virtuoso EDA tools, targeting a reduction in the startup voltage. For a complete design methodology of a fully-on-chip cold starter, the reader is referred to Sect. 4.3. Figure 6.31 shows a schematic of the cold starter, which is comprised of an enhanced-swing cross-coupled oscillator (ES-XCO) [22] and a 3-stage Dickson charge pump (DCP).

Table 6.6 presents the component values and sizes of the on-chip devices used in the cold starter. In post-layout corner simulations, the startup of the boost converter

was achieved for 9.8 mV (TT), 9.2 mV (FS), 12.3 mV (SF), 9.2 mV (FF), and 12.3 mV (SS). According to (2.16), a high L_2/L_1 ratio reduces the supply voltage required for oscillation. Thus, we set $L_1 = 1$ µH and $L_2 = 100$ µH, both modeled with $Q = 100$ at 1 MHz for the off-chip inductors of the ES-XCO.

6.6 Experimental Results

The DC-DC converter [1] was integrated in the Global Foundries 130-nm CMOS technology supported by Cadence EDA tools in the design phase. The availability of ZVT transistors used in the ES-XCO is an important requirement when determining the technology. The off-chip components are the boost inductor L, C_{IN}, and C_{OUT} and the four ES-XCO inductors.

Figure 6.32 shows a micrograph of the active area (0.35 mm^2) of the chip. For the measurements, V_S was emulated by a variable power supply (Keithley 2401), and R_S was set with resistors of either 6 Ω or 40 Ω, combined with an off-the-shelf inductor of 33 µH or 220 µH, respectively, setting the MPPT as defined in (5.34). The input and output capacitors are determined from (5.54) and (5.50), respectively, keeping the proportional ripple lower than 10% for $L = 33$ µH, which leads to values of $C_{IN} = 22$ µF and $C_{OUT} = 2.2$ µF. A photograph of the test bench setup is shown in Fig. 6.33.

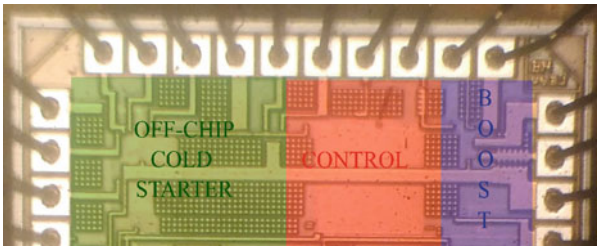

Fig. 6.32 Micrograph showing the active area of the fabricated chip

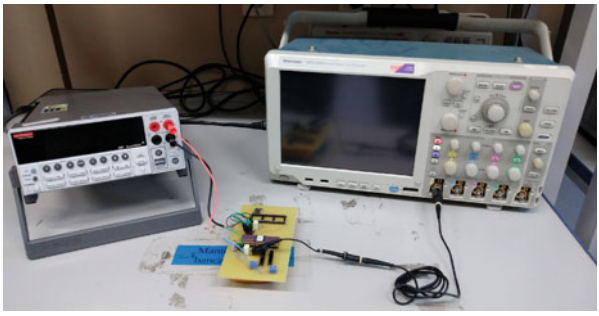

Fig. 6.33 Test bench setup used for the measurements

6.6.1 Startup

For the ES-XCO using off-the-shelf inductors, several combinations of inductors L_1 and L_2 were tested to find the values that start up the converter at the lowest input voltage, as shown in Table 6.7. The startup voltage is defined as the minimum input voltage, which allows the boost converter to reach steady-state operation (phase C).

According to (2.14) and (2.22), the oscillation condition is a function of not only the ratio L_1/L_2 but also the losses in the inductors and the charge-pump input conductance (G_o). The combination of off-the-shelf inductors that led to the minimum supply voltage to start up the boost converter was $L_1 = 1$ μH ($Q = 40$ @1 MHz) and $L_2 = 100$ μH ($Q = 100$ @1 MHz). On applying these values, the ES-XCO started to oscillate for an input voltage of 3.3 mV, which provided a voltage of 63.4 mV at node V_{DDCS}. However, this is not high enough to power the clock circuit. As the input voltage increases, the V_{DDCS} also increases, making it possible to start up the boost converter.

Figure 6.34 shows the voltage at node V_{DDCS} against V_{IN}. The boost converter can start up and achieve steady-state operation (phase C) for $V_{IN} \cong 11$ mV, when V_{DDCS} is high enough (≈420 mV) to allow efficient switching of the LSS. It should be noted

Table 6.7 Startup voltages for several ES-XCO inductor combinations

L_1 (μH)	L_2 (μH)	Startup (mV)
4.7	33	28
4.7	1000	26
10	100	20
4.7	220	20
4.7	330	20
4.7	470	19
4.7	100	15
1	100	11

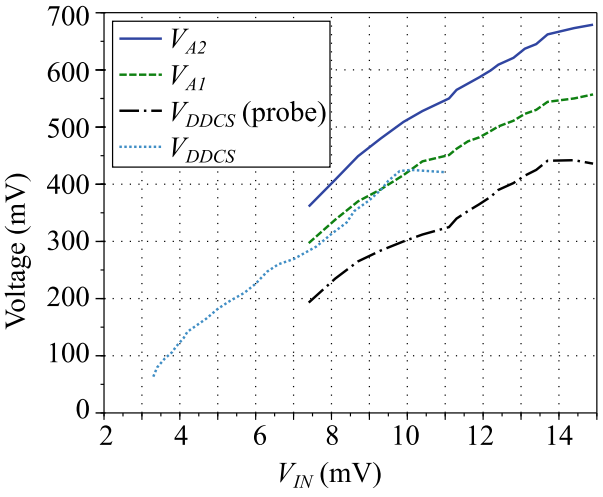

Fig. 6.34 Measured V_{DDCS}, V_{A1}, and V_{A2} vs V_{IN} for $R_S = 6\ \Omega$

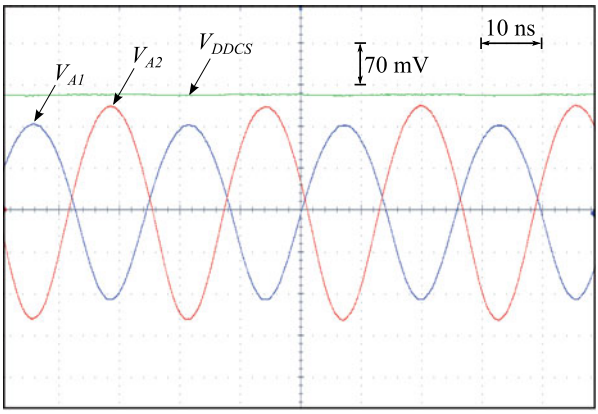

Fig. 6.35 Measured V_{DDCS}, V_{A1}, and V_{A2} waveforms for $V_{IN} = 7.4$ mV ($R_S = 6\ \Omega$)

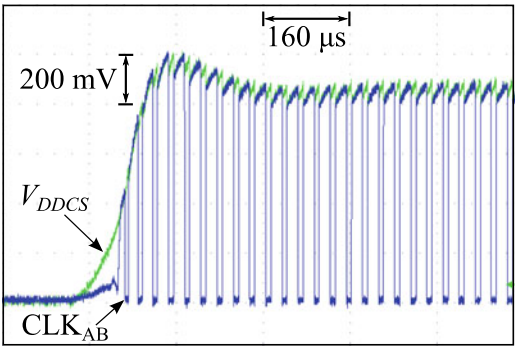

Fig. 6.36 Measured V_{DDCS} and CLK_{AB} during startup

that the oscilloscope probe imposes a relevant load (10 MΩ) at node V_{DDCS}. Another cold starter test, in which nodes V_{A1}, V_{A2}, and V_{DDCS} were simultaneously measured against V_{IN}, is also shown in Fig. 6.34. The effect of loading the ES-XCO output nodes using the probes of 10 MΩ and 3.8 pF clearly impairs the startup performance, as can be noted by the difference in V_{DDCS} when V_{A1} and V_{A2} are not being measured.

The waveforms of V_{A1}, V_{A2}, and V_{DDCS} are plotted against time in Fig. 6.35 for an input voltage of 7.4 mV, which is the minimum V_{IN} required to start up the ES-XCO when nodes V_{A1} and V_{A2} are loaded by the oscilloscope probes. The measured oscillation frequency is around 3.9 MHz for the values of $L_1 = 1$ µH and $L_2 = 100$ µH.

6.6.2 V_{DD} *Buildup*

Figure 6.36 shows V_{DDCS} and CLK_{AB} during startup for $V_{IN} = 20$ mV. As can be seen, after the cold starter has established the voltage V_{DDCS}, the CSRO starts to oscillate. Every time the CSRO switches the transistor NM_{1AB}, V_{DDCS} drops a little

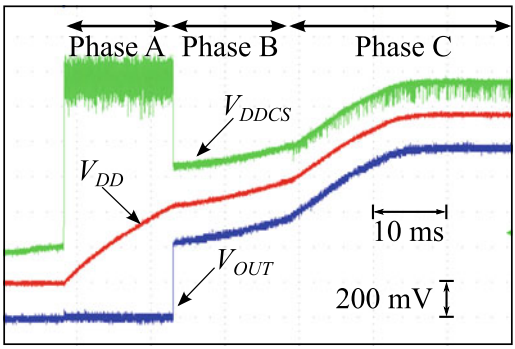

Fig. 6.37 Measured V_{DDCS}, V_{DD}, and V_{OUT} buildup

due to the switching of a high-capacitance node. A larger-area switch would lead to a higher voltage drop at the V_{DDCS} node, thus increasing the V_{IN} required for a given V_{DDCS} level. Hence, the dual-switching scheme using a specific switch with smaller dimensions during startup is an important strategy for reducing the minimum startup voltage of the converter.

After CLK_{AB} has started up, the boost operation begins, and node V_{DD} builds up. The complete buildup of V_{DD}, V_{DDCS}, and V_{OUT} is shown in Fig. 6.37 for $V_{IN} = 30$ mV. When V_{DD} reaches approximately 420 mV, nodes V_{DDCS}, V_{DD}, and V_{OUT} are connected to each other, and once V_{DD} reaches approximately 600 mV, switch $\text{NM}_{1\text{C}}$ replaces switch $\text{NM}_{1\text{AB}}$, the ZCS scheme starts to operate, and the ES-XCO is disabled. Due to the gain in the efficiency delivered by the ZCS scheme, V_{DD} starts to increase at a faster rate, reaching a steady state for V_{DD} close to 1 V. The transition between phases occurred at voltage levels lower than those designed in Sect. 6.3.2, but no significant effect was observed in terms of the system performance.

6.6.3 *Zero-Current Switching*

In order to evaluate the performance of the ZCS scheme, V_M and $V_{G,HSS}$ were measured. Since the capacitance of the oscilloscope is of the same order of magnitude as the capacitance of both nodes, some degradation is introduced by the measurement equipment. Figure 6.38 shows the steady-state waveform of $V_{G,HSS}$. Figure 6.39 shows the waveform of V_M, where it is possible to see the alternation between early and late openings of the HSS. As can be noted, the early opening of the HSS generates a glitch in the waveform of V_M, whereas late opening does not. Figure 6.40 shows the V_M waveform in detail for early and late openings.

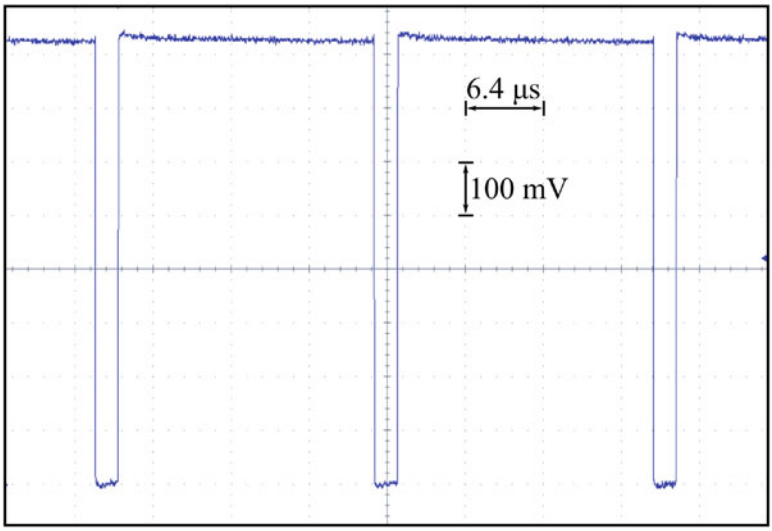

Fig. 6.38 $V_{G,HSS}$ waveform during steady-state operation

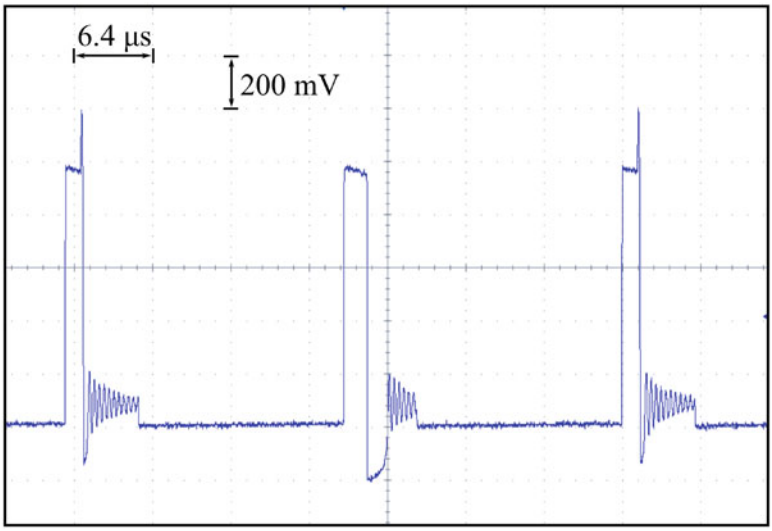

Fig. 6.39 V_M waveform during steady-state operation

6.6.4 Clock Frequency

As explained in Sect. 6.4.5, four external bits are used to control f_{SW} to maximize the harvesting efficiency. Figure 6.41 shows the measured waveform of the CLK_C signal for maximum (word 1111) and minimum (word 0000) settings.

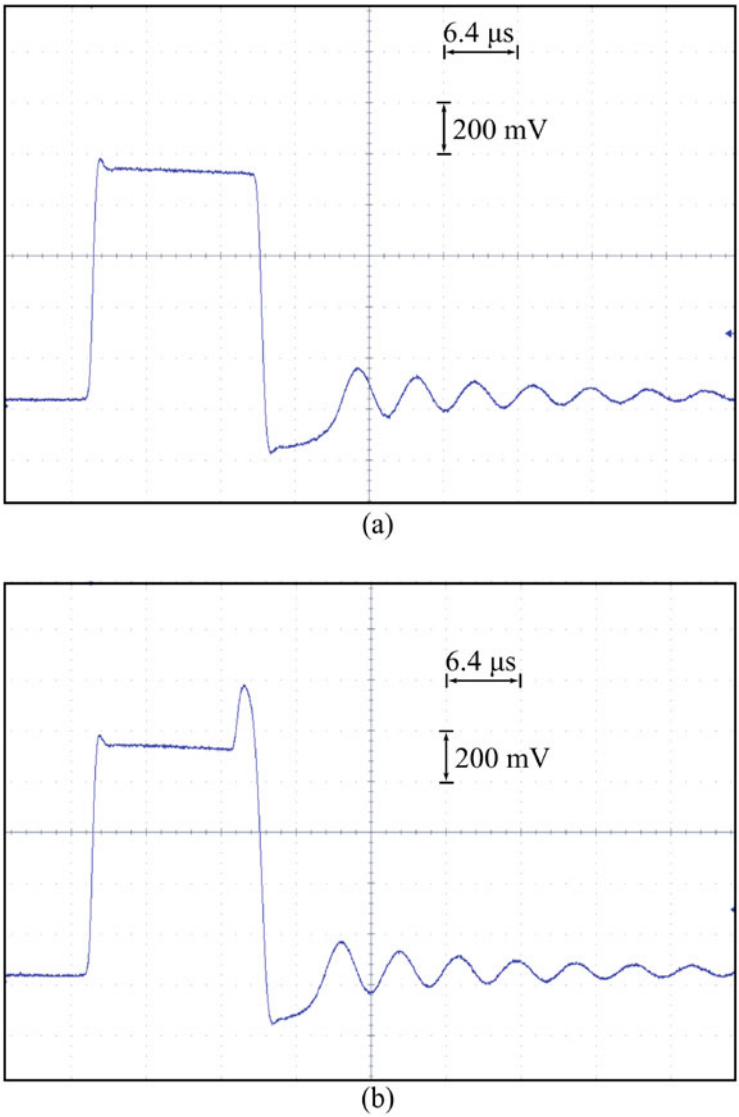

Fig. 6.40 V_M waveform for (**a**) early opening and (**b**) late opening of the HSS

6.6.5 Efficiency

The extraction and end-to-end efficiencies were measured for different R_S and input voltages, as shown in Fig. 6.42. A resistive load was varied at the output to perform the measurements. The minimum input voltage capable of sustaining steady-state operation during phase C was around 7.3 mV, for a 10 MΩ load (oscilloscope load)

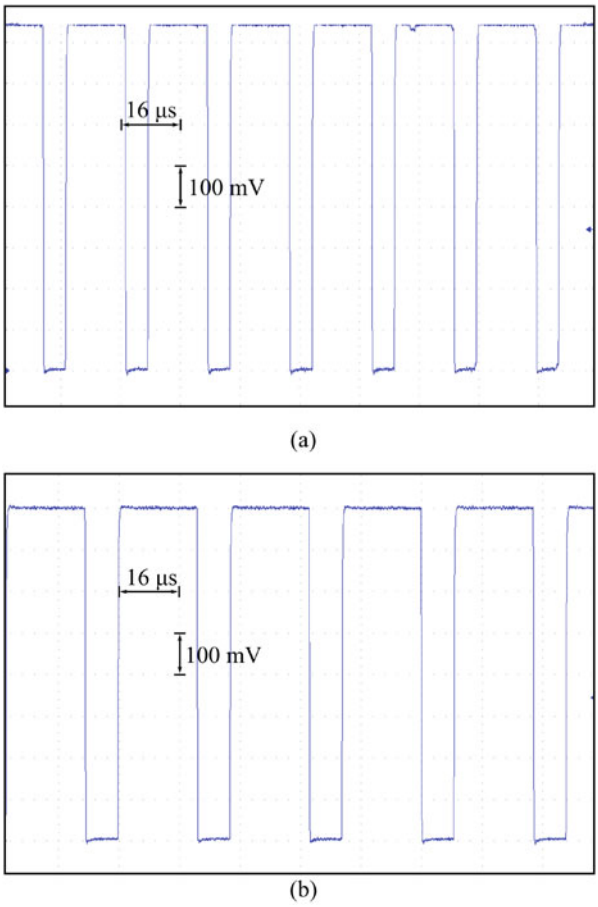

Fig. 6.41 CLK_C signal for (**a**) maximum (45.44 kHz) and (**b**) minimum (33.71 kHz) frequency settings

connected at the output. For this condition, the output voltage is 690 mV, and $\eta_{end\text{-}to\text{-}end}$ is 2.4%.

The system delivers better efficiencies for $R_S = 40\ \Omega$ as compared with $R_S = 6\ \Omega$. For $V_{IN} > 42$ mV, $\eta_{end\text{-}to\text{-}end}$ reaches a plateau with a value of the order of 83%, with a peak $\eta_{end\text{-}to\text{-}end}$ of 85% for $V_{IN} = 140$ mV. The minimum input voltage required to achieve a 50% end-to-end efficiency is approximately 10.5 mV. The extraction efficiency is higher than 95% for the whole range of V_{IN}, validating the MPPT approach. The maximum output power was 2.8 mW for $V_{IN} = 132$ mV and $R_S = 6\ \Omega$.

Keeping V_S fixed, the efficiency was measured for different load conditions. Since for light load conditions V_{OUT} is kept constant (at around 1 V), a decrease in both end-to-end and extraction efficiencies is expected when the load current decreases. Figure 6.43 presents the variation in the end-to-end efficiency with the load current for four values of V_S with $R_S = 40\ \Omega$. Two specific regions can be

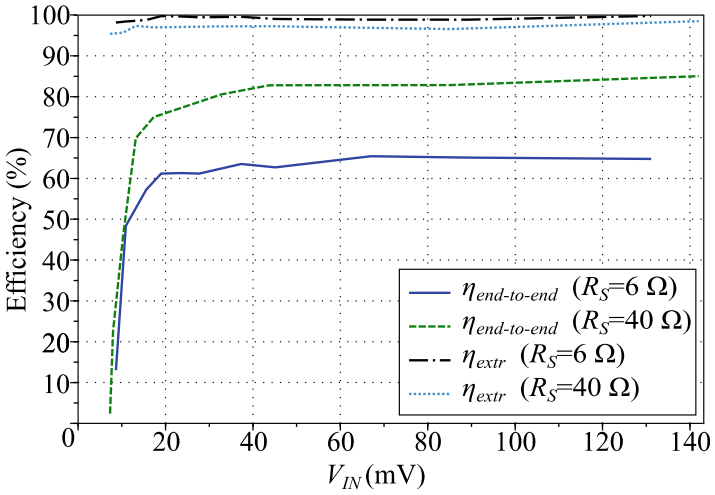

Fig. 6.42 Maximum end-to-end and extraction efficiencies vs V_{IN} for different R_S values

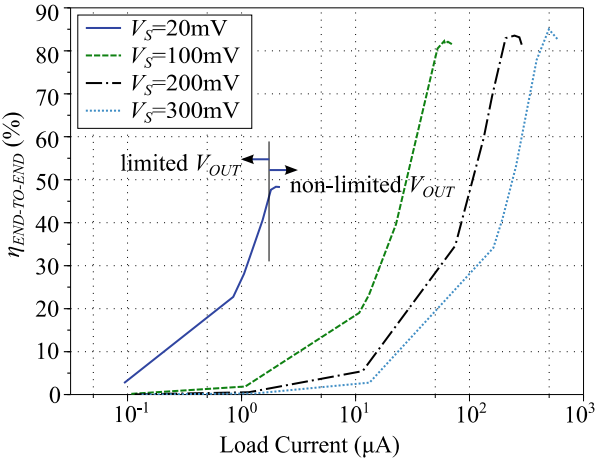

Fig. 6.43 End-to-end efficiency vs load current for different V_S values ($R_S = 40\ \Omega$)

observed. In one region, V_{OUT} is limited to 1 V, and the efficiency is proportional to the load current. In the other region, V_{OUT} is not limited, and thus, the system maximizes the extraction efficiency. The threshold between the two regions is indicated for $V_S = 20$ mV.

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