Chapter 3
Off-Chip/On-Foil Passive and Active Components

HySiF concept gains its strength from mixing and matching different flexible electronic technology directions in a way that optimizes the utilization of its integrated components. Towards the realization of a mature and reliable HySiF based on the CFP process, different off-chip/on-foil passive and active components are implemented. In this chapter, six case studies are designed to highlight key HySiF challenges and present a practical methodology to address these challenges. The chapter starts with introducing three ultra-thin environmental sensors, namely one temperature and two relative humidity sensors. Here, the CFP compatibility with different sensing materials is investigated. Furthermore, on-foil spiral inductors are implemented to study the challenges associated with integrating wireless communication and energy harvesting functionality into HySiF. Finally, a low-voltage digital library for Organic Thin-Film Transistors (OTFTs) is characterized on the CFP flexible substrate. The digital library is then used to implement an addressing circuit for distributed large-area sensor arrays.

3.1 On-Foil Resistive Temperature Detector

Figure 3.1 shows a conceptual schematic of one HySiF variant in which an off-chip/on-foil temperature sensor and UTC are integrated into the CFP flexible package [1]. In general, small and constant thermal contact resistance is required between the temperature sensing element and the surface or object that its temperature is measured (cf. thermal interface A in Fig. 3.1). Modern silicon-based integrated temperature sensors are compact, power-efficient and highly accurate [2]. However, the thermal insulation of the die plastic packaging, including the CFP, increases the thermal resistance between the sensing chip and the package surface, in addition to non-linearities in the sensor response. Albeit, on-chip temperature sensors can be used to monitor the chip self-heating and in-package thermal behavior in

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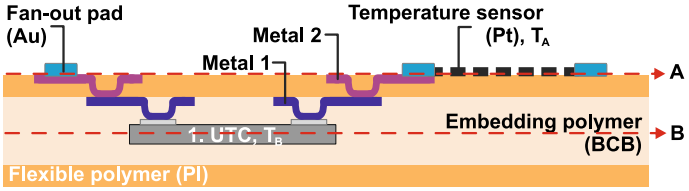


Fig. 3.1 Cross-section of one variant of the CFP process in which embedded UTC and off-chip/on-foil temperature sensor are integrated into/on a flexible polymeric substrate [1]

high-frequency communication or high-power switching applications (cf. thermal interface B in Fig. 3.1) [3, 4].

To resolve this issue, off-chip/on-foil thin-film temperature sensors are implemented in this work. The typical ultra-thin form factor and low thermal mass (i.e. small form factor) of thin-film Resistive Temperature Detectors (RTDs) allow them to draw negligible heat from the measured object or surface. Even when the thin-film RTD is encapsulated and its area increases much larger than that of the on-chip sensors, the thermal resistance between the thin-film RTD and the package surface would still be small. These thermal characteristics when combined with the thin and adaptive form factor of the CFP package, enables the realization of precision bendable smart temperature sensors.

Different flexible temperature sensing elements have been reported (e.g. flexible amorphous silicon [5], carbon black and nickel oxide mixture [6] and printed graphene oxide [7]). Here, thin-film platinum (Pt) RTDs are chosen due to their well-defined temperature response and inherent compatibility with standard microelectronics fabrication processes that are used during UTC embedding in the CFP process.

Sensor Design

As shown in Fig. 3.2, the RTDs use the serpentine and horseshoe layouts. The former is used when a compact sensor area is needed and the latter is used when stress compensation, mechanical compliance and stretchability are crucial. The serpentine metal linewidth and spacing are both about 10 µm, which is limited by the photolithography processing step. Large contact pads ($250\,\mu m \times 250\,\mu m$) are used to allow enough space for 4-point probing during the sensor characterization.

For the choice of the optimal horseshoe shape under different material and dimension constraints, the decision criteria from [8] is followed. Figure 3.2d shows the different design parameters of the horseshoe layout, where R is the radius of the arc median line, w is the linewidth, α is the arc angle, L is the arm length and S is the end-to-end distance of the unit horseshoe cell. Horseshoe layouts with narrower linewidth w are more compliant and stretchable [8], which is why the minimum linewidth of 10 µm is chosen. A compact sensor layout is also targeted, hence the arm length L is minimized. Three unknowns α, w/R and L/R are solved as in [8], under several constraints (e.g. the distance between the two nearest horseshoe ribbons,

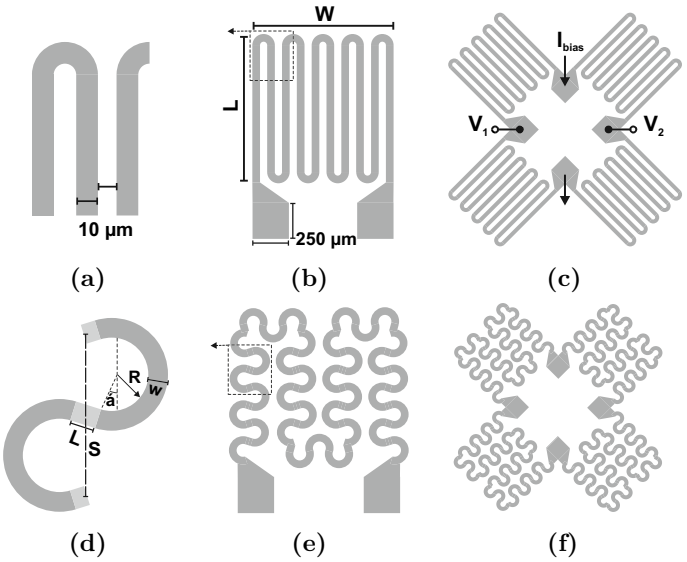


Fig. 3.2 Temperature sensor design. **a**–**c** Serpentine and **d**–**f** horseshoe RTD layouts where minimum linewidth and spacing are 10 µm. Wheatstone bridge configuration using (**c**) serpentine and (**e**) horseshoe unit RTDs in which the resistance mismatch R_{offset}, $\Omega = (V_1 - V_2)/I_{Bias}$ is extracted

surface area and minimizing the effective applied strain). The parameters α, R, L and S are chosen to be about 30 °, 50 µm, 5 µm and 140 µm, respectively.

Figure 3.2c, f show the RTDs when used as unit elements in Wheatstone bridge configuration. The purpose of this design is to directly quantify the resistance mismatch, which results from fabrication non-idealities in addition to testing possible fully differential instrumentation. Note, that evaporated thin-film metal lines show elevated gauge factors than those for bulk metals (gauge factors upto 20 for thin-film vs. 2 for bulk metals) [9, 10], which calls for system-level cancellation of common-mode disturbance, such as mechanical stress, by employing differential signaling. Here, the resistance mismatch is extracted using R_{offset}, $\Omega = (V_1 - V_2)/I_{Bias}$, where V_1 and V_2 are the bridge outputs and I_{Bias} is the bridge constant biasing current.

Sensor Fabrication

Figure. 3.3 shows three different fabrication setups that are used to characterize the on-foil RTDs [1]. In the first setup and using a 150-mm silicon wafer, 50-nm Pt is evaporated on top of 10-nm titanium (Ti) thin-film layer, which acts as adhesion promoter. For the second and third setups, the same sensor stack is evaporated on a layer of 1-µm-thick BCB, which is spin-coated on a silicon wafer. A standard lift-off process is performed for the three setups. For the third setup, an additional layer of 1-µm-thick BCB is used to encapsulate the Ti/Pt sensor stack and the BCB is finally etched to open larger contact pads.

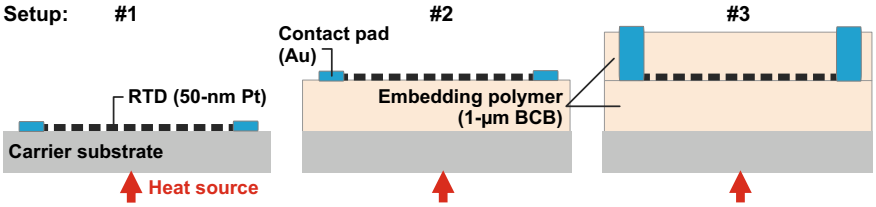


Fig. 3.3 Cross-section of three setups used to electrically and thermally characterize the thin-film Pt RTD [1]. Not drawn to scale

Sensor Characterization

The RTD wafers are placed on a thermo-chuck, which is used as a heat source and its temperature is varied starting from 40 till 120 °C in 20°C steps. At room temperature (about 20 °C), an extra data point is measured. The substrate surface temperature (in setup #1 SiO_2, in #2 and #3 BCB) is monitored using a reference thin-film Pt100 foil sensor from which the worst-case inaccuracy in the quasi steady state temperature measurement equals to ±0.75 °C.

Different RTDs with various surface areas are measured and the nominal resistance at room temperature (about 20 °C) ranges from 80 to 50 kΩ for surface areas from 0.06 to 2.5 mm^2. Figure 3.4a shows the static characterization of three RTDs with similar dimensions and horseshoe layouts but from different setups (cf. Fig. 3.3) [1]. The variation in the base resistance value originates from the different substrate material and surface topography. The extracted sensitivities ($\Delta R/R_{20\,°C}$) of 18 different sensors are plotted in Fig. 3.4b, reflecting temperature coefficients ranging from 2 to 3 mΩ/mΩ/°C depending on the substrate composition.

Although the surface temperature in setup #2 is less than that in setup #1 due to the thermal barrier introduced by the BCB layer, setup #2 clearly exhibits better sensor sensitivity. This is attributed to a higher quality of the Pt metal film when fabricated on the smoother BCB surface [11] against the silicon oxide surface [12] of setup #1. Sensors in setup #3 show the highest effective sensitivity due to the presence of an additional BCB thin thermal barrier layer between the RTD and air, thus lowering the heat loss to ambient air by convection.

Figure 3.4c shows the bridge offset resistance value R_{offset} for the horseshoe- and serpentine-based Wheatstone bridges. Although both bridges have the same surface area ($4 \times 2.5\ mm^2$), the horseshoe-based Wheatstone bridge showed superior matching to that of the serpentine-based bridge. This is regarded to better randomization of the fabrication process non-idealities for the horseshoe layout. For instance, the laser direct writer scans the wafer in one direction only, which leads to either better or less matching between the structures fabricated parallel or perpendicular to each other, respectively.

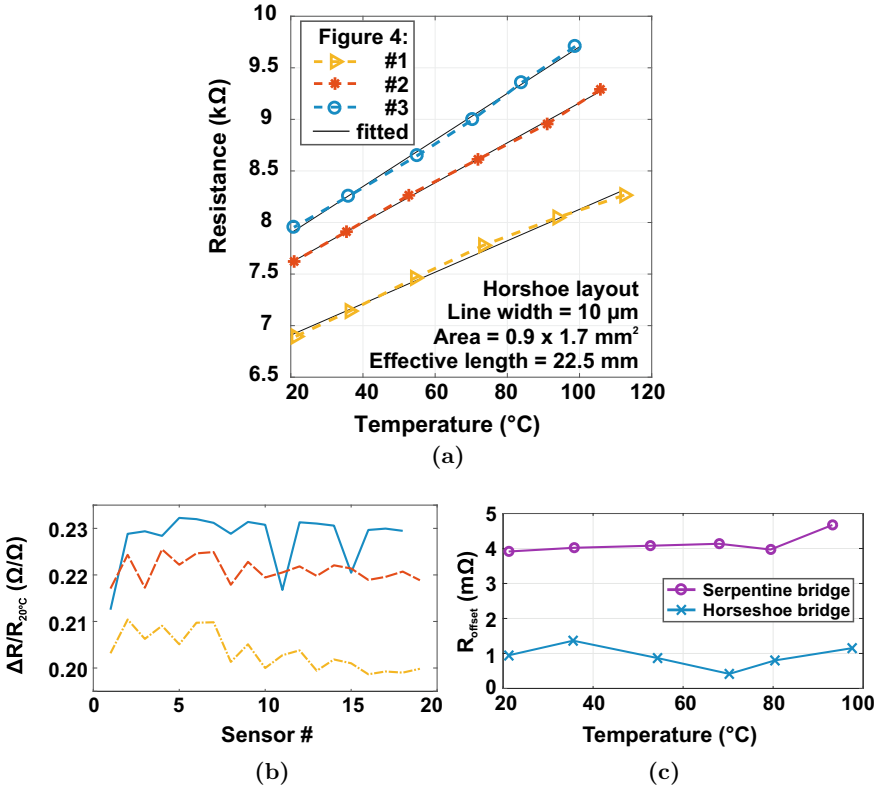


Fig. 3.4 **a**Measured resistance of three RTDs with similar dimensions from three different setups. **b** Measured sensitivity of multiple RTDs from the three different setups shown in Fig. 3.3. **c** Bridge offset resistance R_{offset} plotted for Wheatstone bridge RTDs designed using serpentine and horseshoe layouts

3.2 Ultra-Thin Humidity Sensors

Capacitive polymeric Relative Humidity (RH) sensors are currently dominating the market [13, 14]. Other developing resistive or electrochemical-based RH sensors, such as graphene oxide (GO) [15, 16], nanosheets [17, 18] and high-surface-to-volume ratio materials, such as carbon nanotubes and nanowires [19, 20], have the potential to achieve faster response time and higher sensitivities. Here, two variants of RH sensors are presented, namely electrochemical and capacitive sensors, which have proven to be compatible with the CFP flexible package [21].

3.2.1 Electrochemical Humidity Sensor

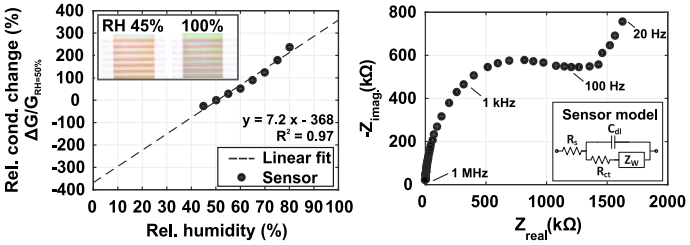
Previously, nanosheets composed of phosphatoantimonic acid $H_3Sb_3P_2O_{14}$ were spin-coated on rigid glass substrates [17] achieving huge sensitivity (5 orders of magnitude from 0 to 100% RH) and response time of $\approx$ 2 s. Upon moisture absorption, water molecules get intercalated in between the nanosheets, which increases the film thickness. This leads to an increase in the proton conductance and a simultaneous shift in the refractive index, which enables the implementation of electrical as well as optical readouts.

Here, sputtered AlSiCu electrodes on BCB/PI substrate define the sensor length and width as 0.5mm and 4mm, respectively. These values were chosen to keep the sensor base resistance below 1 MΩ (cf. [17]) for simpler sensor readout. Afterwards, the same nanosheets ($H_3Sb_3P_2O_{14}$ [17]) are spin-coated on the BCB/PI polymeric substrate at a speed of 2000rpm for 90seconds.

For sensor characterization, the electrochemical sensor is assembled using double-sided foam adhesive on a flexible carrier PCB, where pin headers are soldered to predefined copper contact pads. The electrical connections from the sensor to the carrier PCB are made using silver glue (EPO-TEK H20E). The sensor is then placed in a controlled climate chamber (Vötsch VCL 0010) and the RH is varied from 45 to 80% with 5% steps at a constant temperature of 30 °C. The chamber sensors are used as reference sensors with an inaccuracy of 0.58 K and 1.7% for temperature and RH, respectively. The RH sensor is then connected to an LCR meter (HP4284A, input amplitude and frequency of 300 mVpp and 800 Hz) using 4-point Kelvin connection for electrical impedance characterization. Note that a higher amplitude of the AC excitation signal can permanently ionize, and, thus, destroy the nanosheets.

Figure 3.5 shows the characterization results of the electrochemical RH sensor. The relative conductance change $\Delta G/G_{RH=50\%}$ is plotted against the RH data from the reference sensor in the RH range from 45 to 80%. A linear fit is also plotted with a coefficient of determination ($R^2 = 0.9724$). The extrapolated fit indicates an expected maximum $\Delta G/G_{RH=50\%}$ of about ±368% for the full RH range. The measured sensor performance matches well with the previous realization of the same sensing material on rigid glass. This indicates that the BCB surface of the CFP package is smooth enough on the nanoscale level for the proper fabrication and operation of the nanosheets. The inset of Fig. 3.5a shows the change in the film optical thickness (surface color from red to green) at RH of 45 and 100%. Figure 3.5b shows the Nyquist plot of the electrochemical sensor at RH of about 60%. The measurement results indicate that the sensor electrical behavior can be modeled using Randles equivalent circuit [22] that is shown in the inset of Fig. 3.5b. The extracted proton conductivity is about 15 mS/cm at RH of about 55%.

Although the implemented electrochemical sensor provides huge sensitivity and optical readout, it still requires AC excitation and complex impedance readout techniques for integration into HySiF. Due to the reactive electrochemical nature of the nanosheets, a protective vent can be assembled onto the sensing active region in order to reduce condensation and contamination [23].



(a) (b)

Fig. 3.5 **a** Measurement results of the electrochemical sensor relative conductance change $\Delta G/G_{RH=50\%}$ against relative humidity. A linear fit is also plotted with a coefficient of determination (R^2 = 0.9724). The inset of this figure shows the change in the film optical thickness (surface color from reddish to green) at RH of 45 and 100%. **b** Nyquist plot of the electrochemical sensor at RH of about 60%. The measurement results indicate that the sensor electrical behavior can be modeled using Randles equivalent circuit [22], which is shown in the figure inset. The model consists of the electrolyte resistance R_s, charge transfer resistance R_{ct}, specific electrochemical element of diffusion Z_w and double-layer capacitance C_{dl}

3.2.2 Capacitive Humidity Sensor

Driven by the well-established plastics industry, polymers have been widely employed as dielectric material in integrated interdigitated and parallel plate capacitive RH sensors [13, 14, 24–26]. They currently dominate the RH sensor market due to their linear response, CMOS-compatibility, stable operation over long periods and potential high power efficiency due to the fact that no static power is consumed to operate the sensors [24, 27–30]. Thanks to the automotive and consumer electronics applications, environmental monitoring sensors, RH sensors in particular, are directed towards miniaturization and compactness as the polymer sensing material is typically spin-coated on the top metal layer of the CMOS readout chip. Consequently, wire-bonding between the sensor and readout circuit is eliminated. A one-chip solution is achieved where short circuit interconnections result in low parasitic capacitance, which enables compact, ultra-low power and precision sensor readout [29]. However, this technique is not economic for flexible and large-area electronic applications (area of more than tens of mm^2, e.g. touchless motion tracking), that's why an inherently CFP-compatible off-chip/on-foil polymeric capacitive RH sensor for HySiF integration is developed in this work.

Sensor Design

The RH sensor implemented in this work uses the variations in the dielectric constant ε_r of PI material (Durimide manufactured by the company Fujifilm [31]) upon moisture absorption and desorption [21]. The sensing material is inherently compatible with the CFP UTC-embedding process as it has been used as a reinforcing polymer in one variant of the CFP flexible package [32].

Besides, most integrated capacitance-to-digital converters (CDCs) implementations use an insensitive and stable reference capacitor to construct a half or full

bridge, which enables fully differential readout and cancellation of the sensor base capacitance [24, 27–29]. The reference capacitor is integrated on-chip only when the value of the sensor base capacitance is low enough (less than a few pF). In contrast, the need for an off-chip reference capacitor grows when the value of sensor base capacitance is high, which is true in this case as a nominal sensor base capacitance in the tens of pF range is targeted. Note, that slight variations of the capacitor nominal value, resulting from modeling inaccuracy or fabrication non-idealities, is mostly tolerated in CDCs that incorporate a reference capacitor. However, CDCs that directly digitize the sensor base capacitance along with the RH capacitive variations suffer from degraded input dynamic ranges upon variations in the value of the sensor base capacitance.

The capacitance ratio of the wet (RH=100%) and dry (RH=0%) PI is given in first approximation by the following relation [33]:

$$\frac{C_{wet}}{C_{dry}} = \frac{\varepsilon_{wet}}{\varepsilon_{dry}}. \tag{3.1}$$

Using the empirical Looyenga formula [34], we can calculate ε_{wet} for different fractional volume γ of absorbed water in our PI film as follows [33]:

$$\varepsilon_{wet} = \left\{ \gamma \left(\varepsilon_{water}^{1/3} - \varepsilon_{dry}^{1/3} \right) + \varepsilon_{dry}^{1/3} \right\}^3, \tag{3.2}$$

where $\varepsilon_{water} = 78$. Given that the capacitance value of the fringe capacitor is a linear function of its dielectric constant ε_r to the first approximation [24, 33, 35] and that for our PI, ε_r changes from 3.5 to 3.8 when RH changes from 4 to 50% (curing temperature of 350 °C for 2 h, cf. manufacturer's datasheet [31]), an ideal relative sensitivity $S = \Delta C/C_{RH=50\%}$ of about ±8% is expected.

To contain all the fringing electric field lines of the planar capacitor, the PI thickness should be at least equal to the sum of the finger width and spacing [33]. Here, the minimum resolution is limited by the lithography to about 10μm that in turn requires a PI thickness of 20 μm. Consequently, more than 6 spin-coating and curing cycles are required to achieve this PI thickness. As proven in [36], the thickness of PI must be minimized for faster sensor response. In this work, we have used two PI thicknesses, namely 3 and 1 μm, in order to achieve fast response time and a simpler fabrication process.

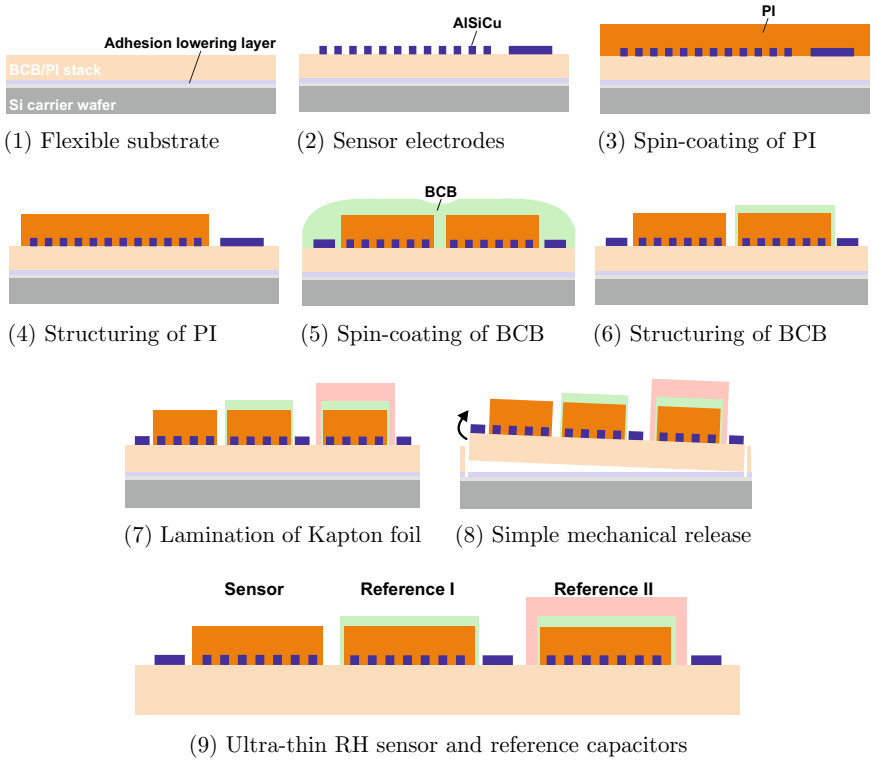
Using the analytical model presented in [35], a capacitance per unit area value of 1.16 pF/mm^2 is calculated for a fringe capacitor with finger width and spacing of 10 μm, PI layer thickness of 3 μm and ε_r of 3.8. Finite Element Method (FEM) is also used to calculate the nominal value of the sensor base capacitance where the low-frequency solver of the CST studio suite is used. A capacitance per unit area value of 1.57 pF/mm^2 is simulated for the same previously mentioned dimensions and material properties.

Measurements, using LCR meter and 4-point connection, show a close value of 1.28 and 1.02 pF/mm^2 for sensors (finger width and spacing of 10 μm) with 3- and

1-µm-thick PI sensing layers, measured at RH of 55% and temperature of 25 °C. Here, the sense and reference capacitors use the interdigitated electrode design for achieving a simple planar fringe capacitor. Different finger width and spacing are designed ranging from 5 to 20 µm in a fixed area of $5 \times 5\,\text{mm}^2$

Sensor Fabrication

Figure 3.6 shows the cross-section of the BCB/PI flexible substrate on which the RH sensor and two reference capacitor variants are fabricated. Following the CFP process [32], the substrate is an alternate stack of BCB and PI layers spin-coated on a 150-mm carrier wafer. The metal electrodes are fabricated using sputtered AlSiCu that is structured using standard lithography step (laser direct writing, VPG400 HIMT, followed by dry etching). This optical lithography step, along with other process non-idealities, such as the BCB/PI surface topography, determines the minimum electrode spacing and consequently the maximum capacitance per unit area.



(1) Flexible substrate (2) Sensor electrodes (3) Spin-coating of PI

(4) Structuring of PI (5) Spin-coating of BCB (6) Structuring of BCB

(7) Lamination of Kapton foil (8) Simple mechanical release

(9) Ultra-thin RH sensor and reference capacitors

Fig. 3.6 Fabrication process steps for the ultra-thin RH sensor, reference I and reference II. The sensing material is PI, which is isolated using BCB to fabricate reference I and an additional Kapton lamination to fabricate reference II. The foil is detached (cf. Fig. 3.7) from the carrier wafer for characterization

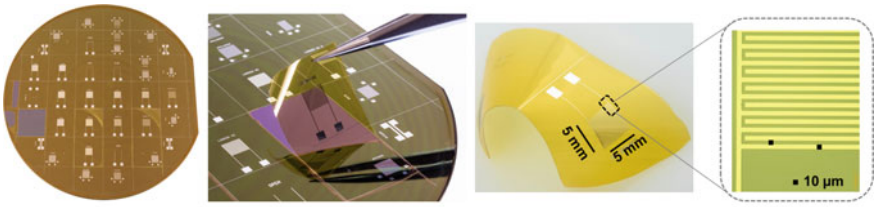


Fig. 3.7 **a** RH sensors on 150-mm carrier wafer. Illustration of the RH sensor **b** during and **c** after the simple mechanical release or detachment from the carrier wafer

The PI sensing material is then spin-coated at 1500 rpm and cured at a temperature of 250 °C achieving a PI thickness of about 3 µm, which is etched down to achieve a PI thickness of 1 µm for a faster sensor response time. The fabrication of references I and II in Fig. 3.6 follows the exact processing steps of the RH sensor and an additional 1-µm thick BCB layer is spin-coated on the PI layer to shield it from any moisture uptake. For reference II, a 25-µm-thick Kapton foil is laminated on top of the thin BCB layer.

Since the RH sensor is fabricated on the surface of BCB/PI substrate, the fringing field that passes through the CFP package causes a humidity-insensitive parasitic capacitance in parallel to the humidity sensitive capacitor. An alternative approach would be to first spin-coat the PI sensing layer, followed by electrodes fabrication and then another layer of PI, thus a fully RH sensitive planar capacitor can be achieved.

Sensor Characterization

In this section, the dynamic behavior of the RH sensor is discussed, while the static characterization is presented later in section 4.1. Figure 3.8 shows the dynamic characterization of 41 ultra-thin RH sensors having a PI sensing layer thickness of 1µm and finger width and spacing of 10µm. Figure 3.8a plots the sensors' response upon forced moisture adsorption with air having a high concentration of water vapor in order to saturate the sensors, thereby reaching RH level of 100%. Figure 3.8b plots the sensors' recovery during the spontaneous desorption that occurs shortly after the air flow is discontinued. An asymmetry is observed between the adsorption and desorption events which traces primary to the different diffusion triggering mechanisms (forced adsorption vs. spontaneous desorption) and secondary to the moisture-dependent diffusion coefficient [36].

Using the measured dynamic response, rise and fall times and relative sensitivity are extracted for all the sensors and the corresponding histograms are plotted in Fig. 3.8c–e. The relative sensitivity (cf. Fig. 3.8d) is calculated using $(C_{max} - C_{min})/C_{min}$, where C_{max} and C_{min} are the maximum and minimum capacitance values at 100% RH and 55% RH, respectively. The average rise and fall times and relative sensitivity are 54, 750 ms and ±21.85%, respectively. Furthermore, the measured relative sensitivity is about 2.73x more than the analytically predicted relative sensitivity (±8%) in spite of using thinner PI sensing layers. Using lower

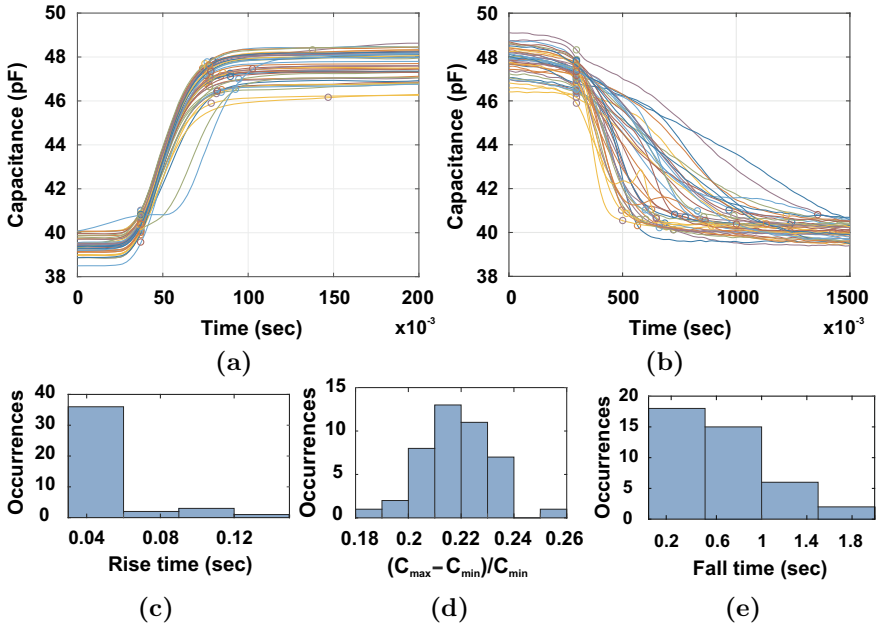


Fig. 3.8 Dynamic characterization of RH sensors where 41 sensors are measured by **a** forced adsorption of water vapor, thus saturating the sensor dielectric with 100% RH. Rise times are extracted and a histogram is plotted in (**c**) with mean time of 54 ms. **b** Sensors' recovery by spontaneous desorption. **d** Histogram of the relative sensitivity (calculated using $(C_{max} - C_{min})/C_{min}$), where C_{max} and C_{min} are the maximum and minimum capacitance values at 100% RH and 55% RH, respectively. Fall times are extracted and a histogram is plotted in (**e**) with mean time of 750 ms

curing temperature than that mentioned in the PI datasheet, might be a reason for the improved sensitivity.

Figure 3.9 compares the dynamic response of the RH sensor with reference I and II, where Fig. 3.9a, b plots the response and recovery times. By extracting the relative sensitivity of reference I ($\pm 2.71\%$), the additional 1-µm-thick BCB layer desensitized the sense capacitor by a factor of $8\times$ achieving a good reference capacitor while maintaining the same value of the base capacitance. A thicker BCB layer could completely desensitize the reference capacitor. The 25-µm-thick Kapton foil achieved complete desensitization for reference II, with a slightly higher capacitance value. Minor level variations in the measured response of reference II are observed that are triggered by the adsorption and desorption events, which are related to variations in temperature, pressure and contact resistance.

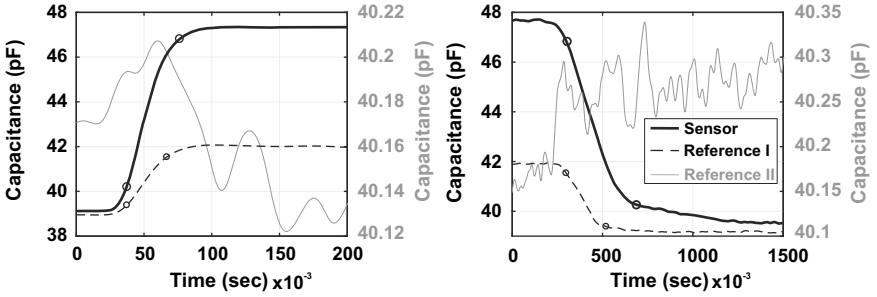


Fig. 3.9 Comparison between the measured dynamic response of RH capacitive sensor, reference I and reference II of Fig. 3.6. **a** Adsoption and rise time, **b** spontaneous desorption and fall time of RH sensor, reference I and reference II. The value of reference II capacitance is near-stable and plotted on the scaled y-axis on the right-hand side

3.2.3 Benchmarking

Table 3.1 benchmarks the RH sensors presented in this work against recent thin and ultra-thin RH sensors. Different sensing materials, with thicknesses ranging from few tens of nm to less than a mm, have been used, such as ceramics materials (e.g. Al_2O_3, TiO_2 and SiO_2) [20], polymers (e.g. Polyimides, Poly(ethyleneterephthalate) (PETT), Poly(methyl methacrylate) (PMMA) and Kapton) [25, 26] and inorganic materials (e.g. graphene oxide (GO), tungsten-based 2D semiconductors WO_3/WS_2/WS_3, 1D materials: nanofibers, nanowires, nanotubes) [15, 16, 19, 38, 40–42].

A wide range of RH detection techniques has been employed including those techniques, which are based on changes in the dielectric constant (capacitive), proton or ionic conduction (electrochemical, resistive or capacitive) and refractive index (optical). Sensor sensitivity or dynamic range vs. response time is typically optimized according to the target application. Few RH sensors have achieved response and recovery times in the ms range (e.g. GO-based [39], optical sensors [44] and thin-film polymer-based [45]) as most of the reported sensors have shown few tens of seconds response time.

3.3 Printed Strain Gauge

In this section, a resistive strain gauge, which is printed using silver-ink, is designed and characterized. In the next chapter (section 4.2), the presented strain gauge is combined with a readout UTC demonstrating a HySiF, which has been developed for robotic e-skin applications.

Table 3.1 Ultra-thin RH sensors performance summary and comparison against the state-of-the-art

Reference	Transduction	Sensing material	Thickness	Fabrication	Substrate	Electrode material	Sensitivity	Response time (s)	Recovery Time (s)	Measured range (%)
This work	EIS, R	nanosheets $H_3Sb_3P_2O_{14}$	0.2	Spin- coating	BCB/PI	AlSiCu/Au	±369%	2	2	45-80
This work	C	PI	1-3	Spin-coating	BCB/PI	AlSiCu/Au	±21%-90%	0.05-1	0.7-2.5	45-80
[26]	C	PI	4.6	Spin-coating	Glass	Au/Cu	15.2fF/%RH	18	31	5-85
[25]	C	Kapton	75	Inkjet Printing	Kapton	Ag-ink	0.5fF / $\%RH.mm^2$	350		20-90
[37]	C	PEG/PEDOT:PSS	250	Spin-coating	PDMS	PEDOT:PSS	0.0085/%RH	2		10-90
[18]	R	PANI/PEDOT:PSS	100	Inkjet Printing	Paper	PEDOT:PSS	200%	420		16-98
[16]	EIS, R	GO	12	Spray-coating	Si/SiO_2	Au/Ti	4.7 M-0.6 kΩ	0.5		25-95
[15]	R	GO	0.0025	Drop-casting	Si/SiO_2	Au	1200x	5		25-88
[38]	C	GO	-	Drop-casting	Si/SiO_2	Au	37800%	10.5	40	15-95
[39]	EIS, R	GO	1-0.015	Spray-casting	PEN	Ag	$10_{-7} - 10_{-6}$	0.02	0.03	30-80
[40]	R	WS_2	0.0021+55	W +Sulfur-ization	PDMS	Graphene	2357x	5	6	20-90
[41]	EIS, R	WS_3	171	Spin-coating	Ceramic	Ag-Pd	277%	4	63	11-95
[42]	R	BP/Graphene	-	Electro-spraying	Si/SiO_2	Au	43%	9		15-70
[19]	R	nanofibers	0.02	Drop-coating	Glass	Au	45000x	2.2	1.05	5-80
[43]	EIS,C	IESM	19	Natural	IESM	Ag-ink	5 – 0.5 MΩ32 – 60pF	2		0-90
[44]	Optical	Nafion	1	Drop-coating	PDMS	-	1.4%/%RH	0.21	0.25	30-100

IESM: Inner Egg Shell Membrane, BP: Black Phosphorus, EIS: Electrochemical Impedance Spectroscopy, PDMS: Polydimethylsiloxane, PEN: Polyethylene naphthalate

Sensor Design

Generally, a wire's electrical resistance R is related to its length L and cross-section area A using the following relation:

$$\mathrm{R} = \frac{\rho \cdot \mathrm{L}}{\mathrm{A}}, \tag{3.3}$$

where ρ is the material resistivity. As the wire stretches, its length increases and its cross-section area decreases by a certain ratio called Poisson ratio υ. The relative change in the electrical resistance is related to the mechanical strain ϵ by the gauge factor (GF) in the following relation:

$$\mathrm{GF} = \frac{\Delta \mathrm{R}/\mathrm{R}}{\epsilon} = \frac{\Delta\rho/\rho}{\epsilon} + 1 + 2\upsilon, \tag{3.4}$$

where ΔR is the change in the electrical resistance. The bending strain at a distance y from the neutral surface of a bending plate is given by the following relation:

$$\epsilon = \frac{\mathrm{y}}{\mathrm{r}}, \tag{3.5}$$

where r is the bending radius of the neutral surface and 1/r is the bending curvature. We conclude from the relations (3.3)–(3.5) that bending the strain gauge with a certain radius results in a mechanical strain on its surface, which affects the geometric dimensions (macroscopic) and electrical resistivity (microscopic) resulting in variations of the strain gauge electrical resistance. Furthermore, the microscopic coefficient of piezoresistivity in metals is very small and can be neglected in most cases (but can not be neglected in thin-film metal [9, 10]) leaving only the macroscopic geometry variation factor to be evaluated.

The Wheatstone bridge circuit is a network of four series-parallel resistors as shown in Fig. 3.10a. It has two output terminals V_1 and V_2, which have equal voltage levels when the bridge is balanced. The bridge is balanced when the ratio of the two resistors in one branch is equal to the ratio of the two resistors in the other branch.

In order to achieve high bridge sensitivity and linear operation, full bridge topology is adopted in which two strain-sensitive resistors $\mathrm{R_V}$, are printed vertically (cf. Fig. 3.10b) and the other two, ideally strain insensitive, resistors $\mathrm{R_H}$ are printed horizontally in the direction perpendicular to the bending strain. Equation (3.6) relates the bridge individual resistance values to the voltage difference between the output terminals $\mathrm{V_{out}}$, given constant biasing current $\mathrm{I_B}$:

$$\mathrm{V_{out}} = \mathrm{V_1} - \mathrm{V_2} = \mathrm{I_B} \cdot \frac{\mathrm{R_{V,1}R_{V,2}} - \mathrm{R_{H,1}R_{H,2}}}{\mathrm{R_{V,1}} + \mathrm{R_{V,2}} + \mathrm{R_{H,1}} + \mathrm{R_{H,2}}}. \tag{3.6}$$

It is important to note that the stability of the biasing current is crucial for the sensor readout accuracy, as any change in the biasing current is misinterpreted by

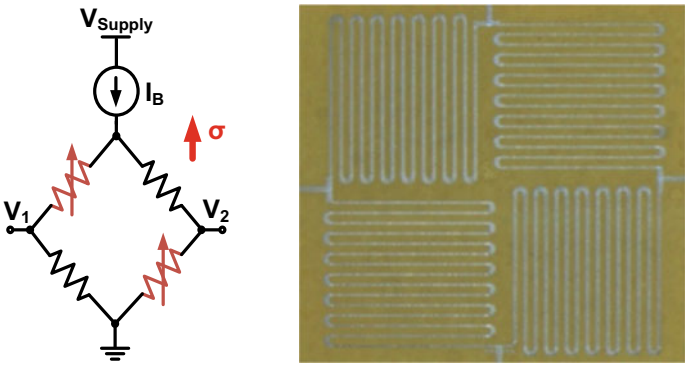


Fig. 3.10 **a** Wheatstone bridge circuit, which has four resistors arrange in a diamond shape, biased using constant current source. **b** Photograph of serpentine-shaped strain gauge printed using silver ink on BCB/PI substrate. The linewidth is 20µm, the total dimension of the bridge circuit is 5 x 5mm^2 and nominal resistance of 800Ω. The direction of expected bending (i.e. mechanical stress σ) of the robotic gripper is indicated

the bridge circuit as a change in the resistance of the active elements. The linear transfer characteristics of the bridge output voltage with the change in resistance ΔR can be shown using $R_V + \Delta R_V = R_{V,1} = R_{V,2}$ and assuming that the strain-insensitive resistors are equal ($R_H = R_{H,1} = R_{H,2}$) and using Eq. (3.6), this results in the following relation:

$$V_{out} = \frac{I_B}{2} \cdot \Delta R_V + V_{offset}, \tag{3.7}$$

where the offset voltage V_{offset} corresponds to the mismatch between the two printing directions and is given by $V_{offset} = \frac{I_B}{2}(R_V - R_H)$. Using Eqs. (3.4), (3.5) and (3.7) the end-to-end relation linking the bridge output voltage to the bending curvature is as follows:

$$V_{out} = \frac{I_B}{2} \cdot GF \cdot R_V \cdot \frac{y}{r} + V_{offset}. \tag{3.8}$$

Sensor Fabrication

Aerosol Jet printing technique, also known as maskless mesoscale material deposition (M^{3}D) [46], is utilized in this work to print the strain gauges on the BCB/PI substrate (cf. Fig. 3.10b) [47–49]. The high-velocity silver-ink jet is capable of creating a compact and high resolution printing with a minimum feature size of 10 µm. The printed structures are cured at a temperature of 150°C.

One of the shortcomings of this printing technique is the mismatched horizontal and vertical printing. This traces back to the accumulation of minor impurities near the nozzle tip during the printing process. Consequently, a mismatch between the resistance values of the vertically and horizontally printed serpentine-shaped structures (R_V and R_H) is observed, which introduces an offset voltage V_{offset} between the two output voltages of the strain gauge bridge circuit (cf. the resistance mismatch of the on-foil RTDs in Sect. 3.1). Selective printing is used to lower the resistance mismatch by following a print-measure-print routine.

Sensor Characterization

After the printing and curing processes are finished, the strain gauges' foil can be released from the rigid carrier wafer. The sensors are then assembled on double-sided foam adhesive that is mounted on a 3D printed plastic material for robotic applications [47–49]. A column with a movable rod is used to incrementally bend the strain gauges. Using a high-resolution camera, side-view images are captured, which are then used to estimate the bending curvature of the strain gauges.

Figure 3.11a shows the measured strain gauge differential output voltage $V_1 - V_2$ with the bending curvature [47–49]. The bridge output voltage is increasing monotonically with increasing the bending curvature (the relationship is ideally linear, cf. Eq. (3.8)). The measured output voltage is about 5mV at a bending radius of 38mm and using 1mA as a biasing current. At no bending, a non-zero output voltage is observed, which traces back to the resistance mismatch between the bridge resistors. As shown in Fig. 3.11b, the memory effect in both the 3D printed plastic material and foam adhesive materials causes the variation of the offset voltage after each bending cycle. This memory effect can be reset if the strain gauge is forced to the no-bending position or left without bending activities for long periods.

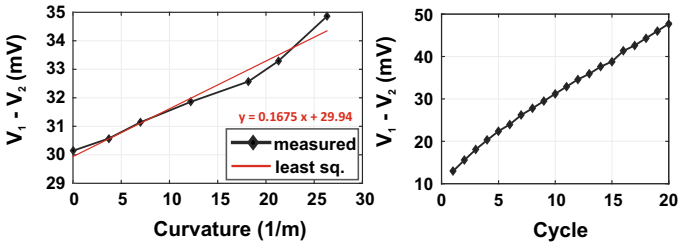


Fig. 3.11 (a) Measurements show a monotonic increase of strain gauge output voltage with increasing the bending curvature [47–49]. (b) Bridge offset voltage increases after each bending cycle, until the memory effect is reset

3.4 On-Foil Spiral Inductors

Flexible sensor systems increasingly require wireless power and data transmission systems, which partly incorporate antennas that are mechanically and electrically tolerant to high levels of bending and stretching. The performance of flexible antennas (e.g. an inkjet-printed 1.2-3.4 GHz multiband antenna [50], 915-MHz antenna fabricated using conductive fibers in PDMS substrate [51] and 5.5-GHz antenna on BCB/PI with embedded transceiver UTC [52, 53]) is steadily approaching those fabricated on conventional rigid substrates.

In this section, off-chip/on-foil spiral inductors are designed, fabricated and characterized that are compatible with the CFP process. Here, the design targets HySiF integration as a part of a flexible NFC sub-system in a multistandard high-performance smart label. However, the approach presented here applies to other HySiF integration scenarios that incorporate spiral inductors. Bendable NFC transceivers [54], energy harvesting systems [55–58], LC wireless sensor readout [59], magnetic resonance imaging (MRI) [60] and proximity sensing [61] are some examples where conventional off-chip planar spiral inductors are needed.

Spiral Inductor Design

Unlike most high-frequency antennas that transmit and receive electromagnetic wave signals, NFC antennas rely mainly on the magnetic field of conductor loops. According to classical electromagnetism, the electric current in a conductor results in a surrounding magnetic field that forms concentric circles of field lines, which decay with increasing the distance from the conductor. The opposite is also true as described by the Maxwell-Faradays' law, as when a time-varying magnetic field induces an electric field. In RFID systems, both scenarios take place as the transmitter coil generates a strong magnetic field that is capable of reaching nearby coil(s) of the passive receiver(s). The transmitter and receiver coils are now inductively coupled, and the mutual magnetic field modulates a voltage difference on a resistor in the receiver circuitry. This voltage is usually rectified to serve as a power supply for the passive NFC tag. It is also used to communicate between the transmitter and receiver in a so-called load-modulation.

NFC systems uses the world-wide ISM-band (industrial, scientific and medical) of 13.56MHz but for short-range secure payments or in cases of multiple tag stacking, the NFC system can be detuned to 14.5 MHz, or even higher frequencies of 17-19MHz [63, 64]. International NFC standards (e.g. ISO/IEC 13157, 14443, 180092, 21481, etc.) define the tag physical characteristics (i.e. antenna size), communication parameters (e.g. modulation and channel coding schemes), the card activation sequences and the digital protocol [65]. In this work, the NFC antenna dimensions, defined by the ISO/IEC 14443, are used from which classes 1 and 3 (Fig. 3.12) are chosen as these classes are most suitable for smart tablets and smart phones.

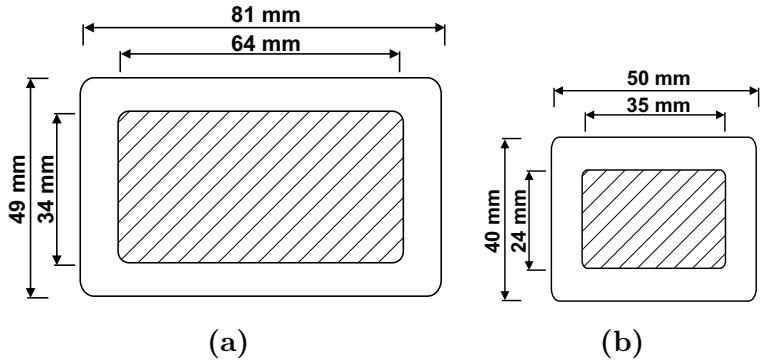


Fig. 3.12 NFC antenna design based on ISO/IEC 14443 for (a) class 1 and (b) class 3 [62]

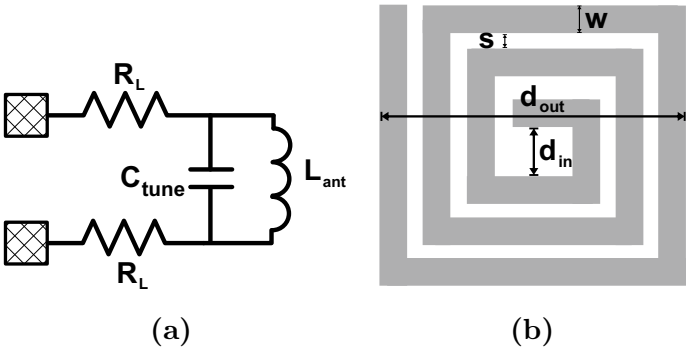


Fig. 3.13 **a** NFC antenna circuit model. **b** Planar spiral inductor design paramters [66]

Depending on the used NFC tag IC and its output impedance, the antenna matching circuit is constructed. In this work, a NFC IC from the company em microelectronics, which is later back-thinned to a thickness of 30µm, is utilized [63]. It is optimized for an operating nominal resonant frequency of 14.5MHz supporting data rates from 106 kbps up to 848 kbps. In addition, it includes an on-chip resonant capacitor of 14pF and its evaluation board includes an off-chip tuning capacitor of 33pF. As shown in Fig. 3.13a, the antenna is modeled using a RLC circuit. If a fixed antenna design is used, the off-chip tuning capacitor C_{tune} adjusts the LC resonance frequency to the nominal operating frequency using the following relation:

$$C_{tune} = \frac{1}{(2 \cdot \pi \cdot f_0)^2 L_{ant}} - C_{chip}, \tag{3.9}$$

where f_0 is the NFC operating frequency, L_{ant} is the antenna inductance and C_{chip} is the on-chip resonant capacitor.

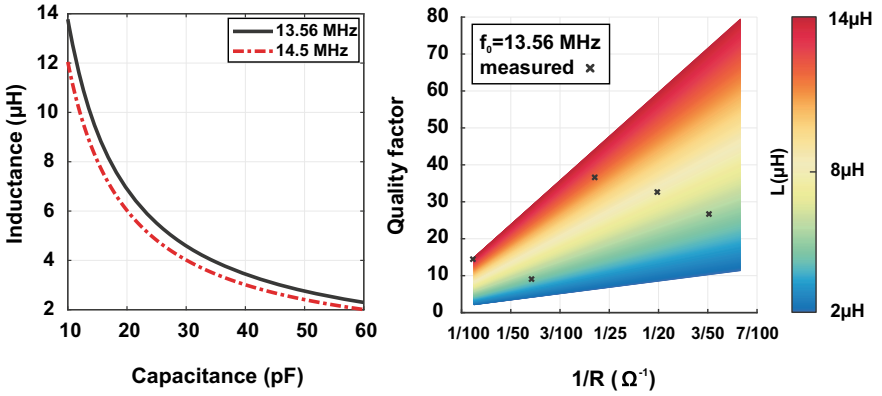


Fig. 3.14 **a** Inductance value plotted against the required total capacitance for two NFC operating frequencies using equation 3.9. **b** Quality factor plane plotted against the loop equivalent conductance for different inductance values using equation 3.10 and some measured on-foil inductors are plotted

In this work, the total capacitance value is limited to a few tens of pF, which originates from the capability of achieving off-chip/on-foil capacitors in this range (cf. Sect. 3.2.2). In order to estimate the inductance of the NFC antenna, equation (3.9) is plotted in Fig.3.14a, where the total capacitance value is swept from 10 to 60 pF for two operating frequencies of 13.56 and 14.5 MHz. Inductance values in the range of 2–14 µH are calculated and these inductance values are used to design planar spiral inductors.

In general, the operating bandwidth (BW) is inversely proportional to the quality factor ($Q = f_0/BW$). Therefore, the Q factor is chosen not too high (< 40 [65]) so it limits the transmission data rate and not too low so the antenna requires more current to be driven by the NFC IC. In general, the Q factor of inductors is limited by the resistive losses in the spiral coil and by the substrate losses [67]. Here, the substrate losses are negligible compared to the resistive loses as the spiral coil is fabricated on BCB polymer, which have low loss tangent of 0.0008 at 1GHz [68]. The Q factor can be calculated using the following relation:

$$Q = \frac{\mathrm{im}(Z)}{\mathrm{re}(Z)} = \frac{2 \cdot \pi \cdot f_0 \cdot L_{ant}}{R_L}, \tag{3.10}$$

where Z is the coil impedance, R_L is the total series resistance of the coil conductor in addition to any additional circuit interconnections. A widely used and best-practiced R_L range is from 20 to 80 Ω [65]. Figure 3.14b plots the inverse resistance in the previously mentioned range against the Q factor for different inductance values that result from Fig. 3.14a.

Table 3.2 Spiral inductors measured performance summary [69]

Inductance (μH)	Resistance (Ω)	Size (mm_2)	Turns	s, w (μm)
3.6	9.2	41 × 55	5	600, 300
5.2	16.6	41 × 71	5	400, 400
3.3	10.5	35 × 40	5	400, 200
4.4	41.3	25 × 35	5	100, 100
13.8	81.3	25 × 35	10	100, 100
7.7	20.1	35 × 40	10	400, 200
11.6	27	35 × 40	15	400, 200

Figure 3.13b shows the different geometric parameters such that the number of turns n, turn width w, turn spacing s, outer diameter d_{out}, inner diameter d_{in}, average diameter $d_{avg} = 0.5(d_{out} + d_{in})$, fill ratio $\rho = (d_{out} - d_{in})/(d_{out} + d_{in})$ are defined. The planar spiral inductance values are calculated using the modified Wheeler empirical formula [66] as follows:

$$L = K_1 \mu_0 \frac{n^2 \cdot d_{avg}}{1 + K_2 \cdot \rho}, \tag{3.11}$$

where the coefficients K_1 and K_2 equals to 2.34 and 2.75 for spiral coils with square layout and μ_0 is the electrical permeability, which is defined as $4\pi \cdot 10^{-7}$ H/m. The metal sheet resistance together with the desired resistance and inductance determine the number of turns n and turn width w and the capacitive coupling between each turn limits the turn spacing s. Different spiral coils are designed and their parameters and characterization results are listed in Table 3.2.

Spiral Inductor Fabrication

Here, spiral inductors are fabricated on BCB/PI substrate that is similar to the CFP package stack [69]. Figure 3.15 shows the 150-mm wafer with the fabricated spiral inductors, the structure of which follows the ISO/IEC 14443 standard for NFC antennas [62]. Following the CFP process, a BCB layer is spin-coated, which has a thickness of 5 μm and cured at 250°. An underpass is then fabricated using AlSiCu sputtering having a thickness of 1 μm. Note, that for lower parasitic resistance, a double-layer spiral inductor can be fabricated where the first layer is fabricated in the same processing step as the underpass.

After the fist metalization step, another 1-3-μm thick layer of BCB is spin-coated and cured. Using standard lithography, array of multiple CFP-standard vias (size = 30 μm × 30 μm) is opened to connect the underpass with the inductor main loop of the top metal. Another AlSiCu metalization step is done for achieving the top

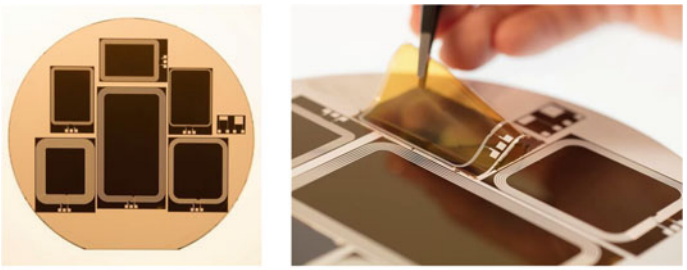


Fig. 3.15 (a) Photograph of a test wafer for the fabricated on-foil spiral inductors using BCB/PI substrate [69]. (b) Photograph demonstrating the mechanical detachment of a spiral inductor from the carrier wafer

metal and main inductor loop with a thickness of 2 μm. The inductors are then released from the carrier wafer as illustrated in Fig. 3.15b. Note, that as the metal trace density increases, the stress induced on the flexible substrate increases, which leads to warpage and difficulties during the foil release [69].

Spiral Inductor Characterization

Table 3.2 summarizes the electrical characterization results of the on-foil planar spiral inductors [69] and Q factor is previously plotted in Fig. 3.14b. The electrical characterization is performed by connecting the inductor under test to LCR meter (MFIA Impedance Analyzer) using four-point connection.

Figure 3.16b shows the measured inductance of a spiral inductor (25×25 mm^2, 10 turns, $w = s = 100\mu m$) [69]. The tensile uniaxial tensile strain acting on the inductor increases with increasing the bending radii. As a result, the spiral loop average diameter d_{avg} increases, which increases the inductance values (cf. Eq. (3.11) and [70]). The average diameter, calculated as $d_{avg} = 0.5(d_{out} + d_{in})$, increases since the inductor traces expand upon tensile uniaxial strain and with small Poisson ratio for metals, both d_{out} and d_{in} increases.

3.5 Thin-Film Organic Electronics

Previous work has demonstrated in-depth device modeling [71] and the realization of OTFT-based complex circuits, such as shift registers [72], ADCs [73], DACs [74] and digital processor [75]. However, such circuits usually require high voltages to operate in the range of 10–20 V.

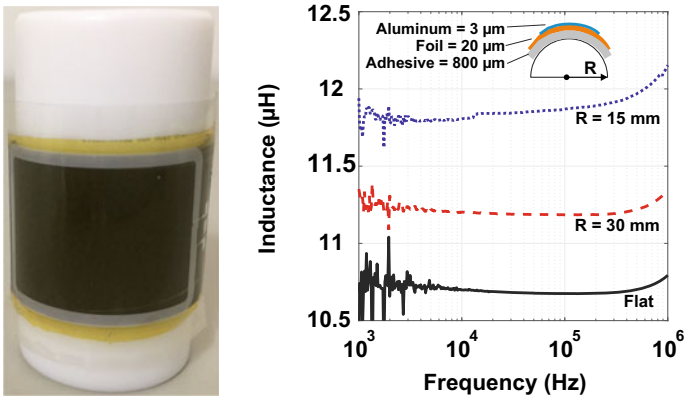


Fig. 3.16 (a) Photograph of the spiral inductor during bending [69]. (b) Characterization of the spiral inductor for different bending radii

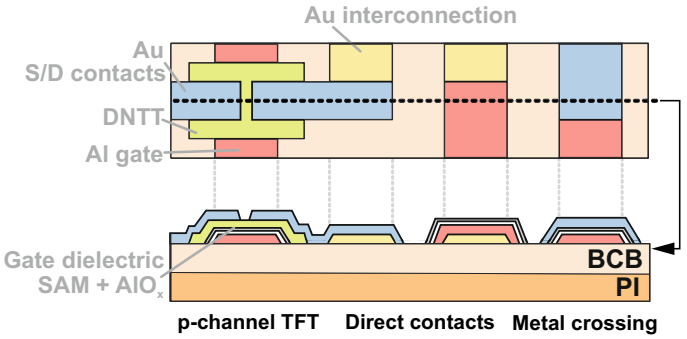


Fig. 3.17 Top and cross-sectional views of the OTFTs on the flexible BCB/PI substrate [76]

Fabrication

Using high-resolution silicon stencil masks, the inverted staggered OTFTs are fabricated on the flexible BCB/PI substrate [71, 76]. As shown in Fig. 3.17, the organic transistors use the p-channel organic semiconductor dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) and have channel lengths as short as 5 µm and gate-to-contact overlaps of 20µm. The gate electrodes and circuit interconnects of the first layer are fabricated first using a 30-nm-thick of Al by thermal evaporation in vacuum. The gate dielectric is a stack of 3.6-nm thick AlO_x layer and 1.7-nm-thick solution-processed tetradecylphophonic acid self-assembled monolayer (SAM). The capacitance of the hybrid gate dielectric is about 700 nF/cm^2 [77] that allows for low-voltage operation (3.3–2 V). A 25-nm-thick layer of the small-molecule organic semiconductor DNTT is then deposited. In order to fabricate the source/drain contacts and circuit interconnects of the second layer, a 25-nm-thick Au is evaporated.

Table 3.3 Extracted OTFT parameters [76]

Parameter	Value
Threshold voltage V_{th}	-1 V
Mobility μ_0	1.3 cm^2 /(Vs)
Contact resistance R_c	0.2 kΩcm
Sheet resistance R_{sh}	666 kΩ/□
On/off current ratio	10^6

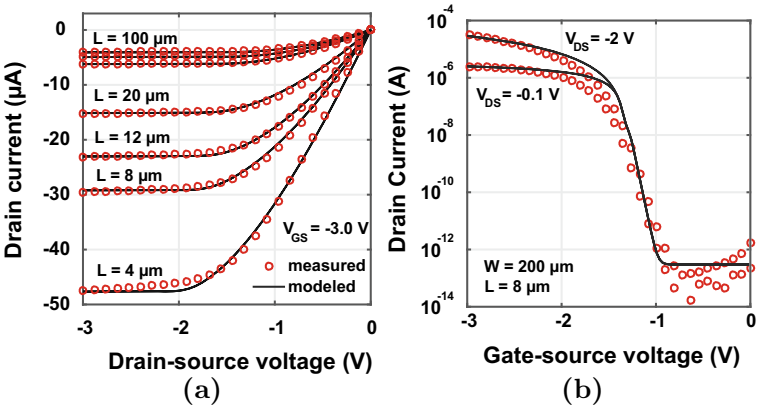


Fig. 3.18 Measured and modeled static output and transfer characteristics of OTFTs

Characterization and Modeling

The OTFTs are fabricated on the smooth BCB surface and their static output and transfer characteristics are measured. The transmission line method (TLM) is used to extract the threshold voltage V_{th}, intrinsic channel mobility μ_0 and contact and sheet resistances R_c and R_{th} [71]. Table 3.3 summarizes the extracted values [76].

Using the static characterization results and the extracted transistor parameters, a SPICE model is developed for proper design and simulation of OTFT-based circuits [78]. The industry standard Berkeley short-channel IGFET model (BSIM3) is chosen to develop a simple and fast model for our OTFTs. Figure 3.18 shows the static output and transfer characterization results plotted against the simulated data using the customized BSIM3 model [76, 78].

3.5.1 Flexible Low-Voltage OTFT Digital Library

Logic design based on p-channel OTFTs is used here instead of the generally preferred complementary logic design since the performance and stability of organic

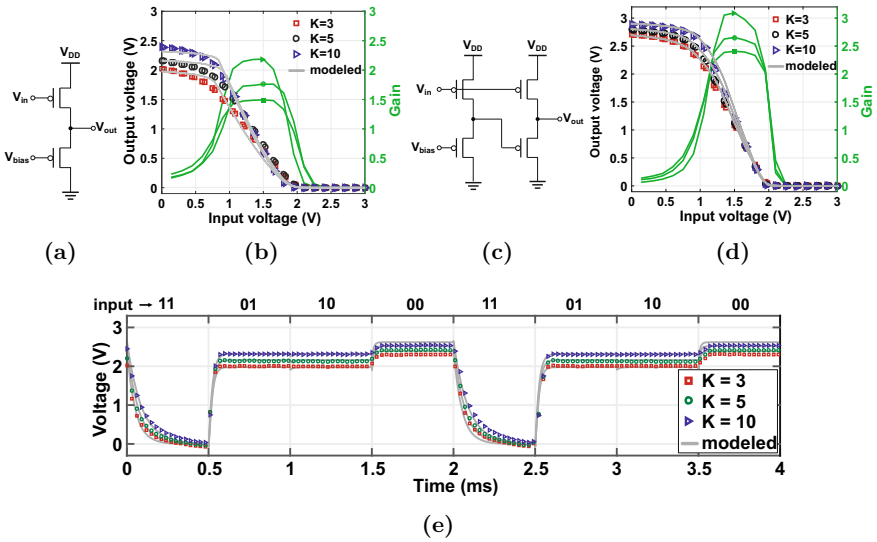


Fig. 3.19 Schematics and measured vs. modeled voltage transfer characteristics of OTFT-based (a), (b) biased-load and (c), (d) pseudo-E inverters [76]. (e) Transient modeling and measurements of 2-input NAND gates based on biased-load inverter design. All OTFTs have a channel length of $5 textmm$

Table 3.4 Extracted static and dynamic parameters of the organic inverters [76]

Parameter	Zero-VGS	Biased-load	Pseudo-D	Pseudo-E
NMH (V)	1.3	0.4	1.3	1.1
NML (V)	1.4	0.4	1.5	0.3
Gain	81	2	100	3
Rise time (µs)	43	29	53	61
Fall time (µs)	368	144	345	147

n-channel TFTs is still inferior. Four different logic designs are investigated, namely zero-VGS, biased-load, pseudo-D and pseudo-E [76]. Figure 3.19a–d shows the schematics and the measured and modeled static voltage transfer characteristics (VTC) of biased-load and pseudo-E inverter designs. Table 3.4 summarizes the extracted static and dynamic performance parameters of the organic inverters for the zero-VGS, biased-load and pseudo-CMOS logic designs [76]. The noise margin high (NMH) and low (NML) are calculated using a graphical approach [79].

In the biased-load inverter design, the load transistor is always-on, using the external bias voltage V_{bias}, so that it provides a rapid discharging of the output node (cf. Fig. 3.19a). When the input voltage is low, the driver transistor pulls up the output voltage but a finite voltage drop across the conducting load transistor is inevitable. The non-rail-to-rail operation of the biased-load inverter is observed

in the measured VTC in Fig. 3.19b. Consequently, the driver transistor is typically designed with a larger channel width compared to load transistor (K > 1, where K is the ratio between the driver and load transistors' channel width. Figure 3.19e shows the transient measured and modeled behavior of a 2-input NAND gate based on the biased-load designs for an input signal frequency of 1 kHz. Here, the fall time decreases as K increases from 3 to 10 since the sizing of the load transistor is different for the three designs (33 µm, 20 µm, 10 µm). On the contrary, the rise time is independent of K, which traces back to the identical sizing of the driver transistors for all three designs (100 µm).

In the pseudo-E inverter design, a rail-to-rail output swing is possible at the expense of a larger transistor count [80]. The pseudo-E design first stage is a biased-load inverter, while its second stage driver transistor connects its gate to the same input signal and the load transistor is biased using the output voltage of the first stage (cf. Fig. 3.19c). When the input voltage is low, the output of the first stage is high, which turns off the load transistor of the second stage, thereby preventing any direct current flow from the supply to the ground similar to the CMOS action. The rail-to-rail operation of the pseudo-E inverter is observed in the measured VTC in Fig. 3.19d.

3.5.2 *On-Foil Sensor Addressing Circuit*

Based on the previously developed combinational digital blocks, sequential digital circuits, such as flip-flops and shift registers, are implemented [47, 76]. Fig. 3.20a shows the schematic of a sensor addressing circuit incorporating a 3-stage shift register and analog OTFT switches. Using the shifted versions (i.e. D_{bit1}, D_{bit2} and D_{bit3}) of the input waveform D_{in}, the OTFT analog switches are time-multiplexed.

Figure 3.20b shows the schematic of a 1-stage shift register, which is based on a dynamic positive-edge-triggered master-slave flip-flop using the biased-load inverter design and operating using low-voltage (3.3–2 V). The flip-flop consists of two latches and each latch includes 3 biased-load inverters and two pass transistors.

Conventionally, when the clock signal CLK is zero, the p-channel pass transistors are not able to pass a logic low signal. Therefore, the design here consists of two parallel paths so that the signal can pass directly through the primary path, whereas in the secondary path, the signal is inverted first then passed through the pass transistor and then inverted back again. All OTFTs have a channel length of 20µm and K ratio of 5.

Figure 3.20c, d show photographs of a 1-stage shift register based on the biased-load design (cf. Fig. 3.20b) and the flexible BCB/PI substrate with the organic shift registers during its mechanical release from the rigid carrier wafer [47, 76].

Figure 3.21a shows the transient measurement and modeling results of the 3-stage shift register where an input clock frequency of 100 Hz and a bias voltage of −1 V are used. As shown in Fig. 3.21b, the dynamic flip-flop operates at a maximum frequency of 3 kHz where it consumes about 233 µW. In principle, the presented

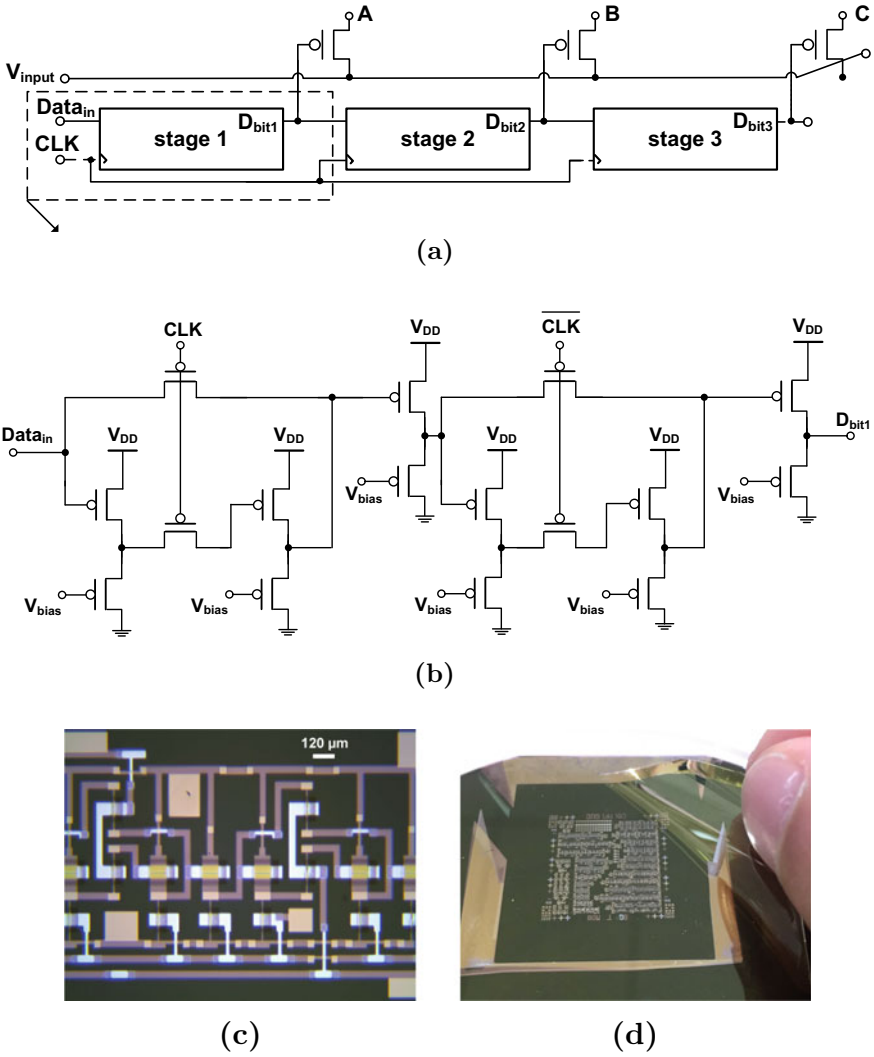
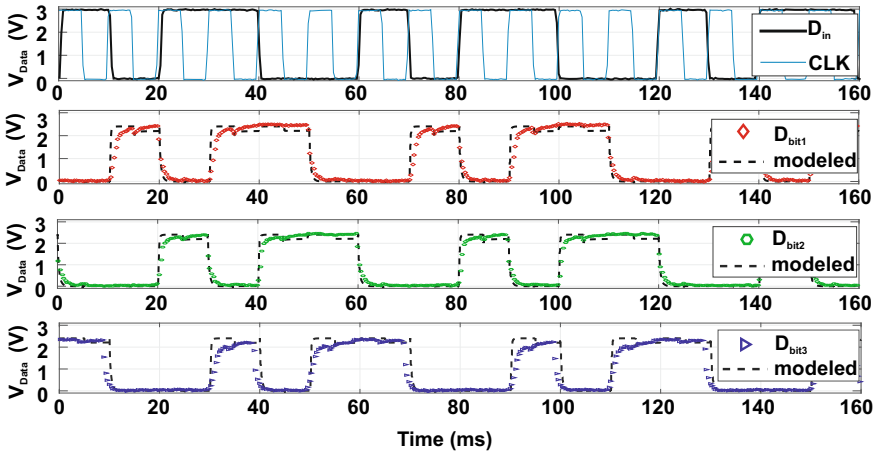
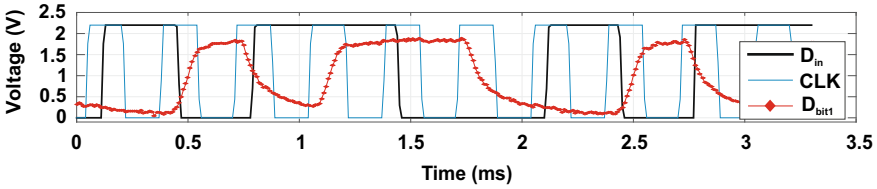


Fig. 3.20 **a** Schematic of 3-stage shift register, where **b** is the schematic and **c** is the photograph of a 1-stage shift-register using dynamic positive-edge-triggered master-slave flip-flop using biased-load inverters [47, 76, 81]. All OTFTs hve channel length of 20 µm. (d) Photograph of the flexible BCB/PI substrate with organic circuits during the mechanic release from the carrier wafer

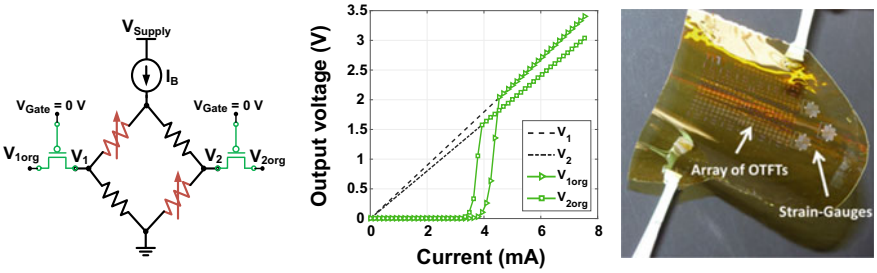


(a)



(b)

Fig. 3.21 **a** Measurement and modeling of a 3-stage shift register operated using a supply voltage of 3V, bias voltage of -1V and clock frequency of 100 Hz. **b** Measurements of 1-stage shift register operated using supply voltage of 2.2 V, bias voltage of −1 V and clock frequency of 3 kHz



(a) (b) (c)

Fig. 3.22 **a** Schematic of one strain gauge biased using current source and connect to a pair of OTFT analog switches. **b** Static measurements showing the performance of the OTFT analog switches in the off/on states. **c** OTFTs and printed strain gauges fabricated on the surface of the BCB/PI substrate [82]

flip-flop will also operate with a bias voltage of 0 V, albeit with larger signal delay and smaller noise margins [76]. Note, that the minimum load at the output node is the oscilloscope input impedance, which is in our case 1MΩ in parallel with 16 pF. In fact, the shifting frequency is higher when the shift register drives the gates of OTFT analog switches, in order to successively address the off-chip/on-foil sensors.

Figure 3.22a shows the schematic of a pair of OTFT analog switches, which is connected to a printed strain gauge (previously discussed in Sect. 3.3, here the gauge resistance equals about 400 Ω) [49]. As shown in Fig. 3.22b, the OTFT acts as a proper switch when its gate-source voltage V_{GS} is higher than the threshold voltage V_{th}. Figure 3.22c shows the released BCB/PI substrate including 3 strain gauges and an array of OTFT switches [82].

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