Chapter 28
Experiencing Layout Design Techniques from Highly Skilled IC Design Engineers

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Abstract Our silicon industries are giving indicator that they are having shortage of expertise in IC design especially from local graduates. On top of that the employed graduates are also lacking of skills. IC design involves with wide topics due to wide application. Specialization is normally related to application such as RF design, memory design, analog design, and digital design. Expertise may end up with specializing in one or two applications only due to long effort to capture the whole skill and knowledge. It is known that the process to build up expertise in this field is hard and challenging. The degree structure needs to equip with high-end software, experience staff, and fund for fabrication. Most programs aim is to produce high level of graduate with good competitive skills that would help the silicon industries to employ them without retrain issue. Hence, in this article, a compilation of teaching process is shared which involves a highly skill mentor who is guiding the trainee on the design process. The sample results concluded that teaching advanced technology in IC design requires sophisticated facilities as well as experienced trainers.

Keywords Teaching · IC design · Specialization · Graduate and Industries

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28.1 Introduction

Layout design is a process of translating circuits into silicon structures. The process of making the whole silicon chip involves huge efforts from the specialization team. The team must be led by a project engineer who has vast knowledge and experience. The team members should also have very good background in CAD simulation and silicon knowledge. Layout is a set of geometric patterns (typically in the form of polygons) which specifies the size and location of silicon layers, polysilicon, and metals to create all sorts of nano sized components. In fabrication process, the layout is used as mask the template for photolithographic process. The polygons in IC layout must satisfy the wafer fabrication's set of design rules. These rules must be applied to ensure the fab machine can fabricate accordingly against its minimum limitation.

Errors are not tolerable, therefore, all the geometric features must be precisely calculated. The impact of errors is failure. Failures are a huge topic in IC design. It can come from wrong geometric design, wrong techniques design, and wrong fabrication process. However, in this article, we are focusing on good design techniques which can safeguard on functional aspect of the silicon devices for increasing end yield.

An example of layout design has been identified and is used as a model in investigating all the proposed techniques from the expert. The layout model is the battery switchover IC (BSIC) [1–4] which consists of several functional blocks. In layout environment, there are two layout domains, analog, and digital which require different strategies in achieving a workable silicon structure. Some techniques and strategies are hardly written in any literature due to confidential issues. Despite the limitation, through guidance from an experience IC engineer, the work is still achievable. Therefore, BSIC is used as a platform to explore the implementation of good techniques under supervision of an IC engineer. After one year of hard work, BSIC is successfully designed and fabricated. The results in the last section show good justification for all the blocks within BSIC. It is evident that the knowledge and skill in IC design are well translated through guidance from experience engineer who has good knowledge in layout design and vast experience working in fabrication process. Without one of the two aspects, the works are potentially falling in failure mode.

28.2 Project Methodology

The aim of this project is to build up skill of IC making from layout until silicon prototype. The development of this project is carried out by a master student under guidance of an experienced IC engineer. It took one year to accomplish the whole design process. The team managed to complete the layout and submitted the design for fabrication. The end part of this study is to evaluate the successful rate or yield of 20 fabricated silicon dies. The results justify all the guidance from the engineer are well translated. Having this experience, the trainee gains very valuable knowledge and skills which are good for our future silicon industries.

In the design process, this article emphasizes on tips and guidance from the IC engineer. Other issues pertaining to design process such as simulation of CAD, silicon knowledge, and circuit operation is not elaborated due to content limitation by the conference organizer. The following section unfolds some of the good tips that make the investigation of layout making it a very successful story.

28.3 The Full Custom Layout Design Flow

The full custom design approach is the best option for a designer to obtain the most robust layout in terms of speed and power. The advantage of this approach is that designers have the ability to customize their own standard cells specific to their design project. This includes the gates positioning, the size, and shape of the circuit component as well as the connection paths among them. A typical full custom IC layout design process flow is illustrated in Fig. 28.1.

This process usually begins once a schematic design that fulfills all its design specification is fully functional at its system level. The next step is to define the floorplan which will take into consideration the special design requirements such as power grids, signal for critical area, symmetrical layout cells, noise, and latch-up protection as well as approximate total chip size. The important step during floorplanning is to decide the design for appropriate cells. Cells can vary from a single transistor to a cluster of combined transistors. Understanding the floorplan beforehand can help a designer to create a more effective cell library such that it will be easier for the designer to work on the top level design of the layout.

In layout design stage, there are three verification tools. Design rules check (DRC) is a tool to check the minimum dimension of components on its sizing, wires, connectors, etc., must be met. This setting must comply with the machines in fab process. The second tool is electrical rules check (ERC). ERC is a tool to verify the size of wire to avoid wire stress or known as electromigration. Wires which are thin but carry heavy current will make the wire stressed. This causes disconnection when the layout is under full testing procedure. The worst is when the wires intermittently failure after few months on operation. The third step is the layout versus schematic (LVS). The verification is carried out by comparing the netlist extraction from the schematic design with the layout drawing. This step is to ensure that the layout drawing is connected correctly corresponding to the schematic design as its reference. If the layout design does not match with the schematic, then the layout drawing has to be modified and later checked again until it matches perfectly with the schematic. Once the layout has completely passed with no errors for these three checking, the chip is now ready for tape-out and ready for the fabrication. The layout file is converted to graphic data system II (GDSII) format for vendor submission.

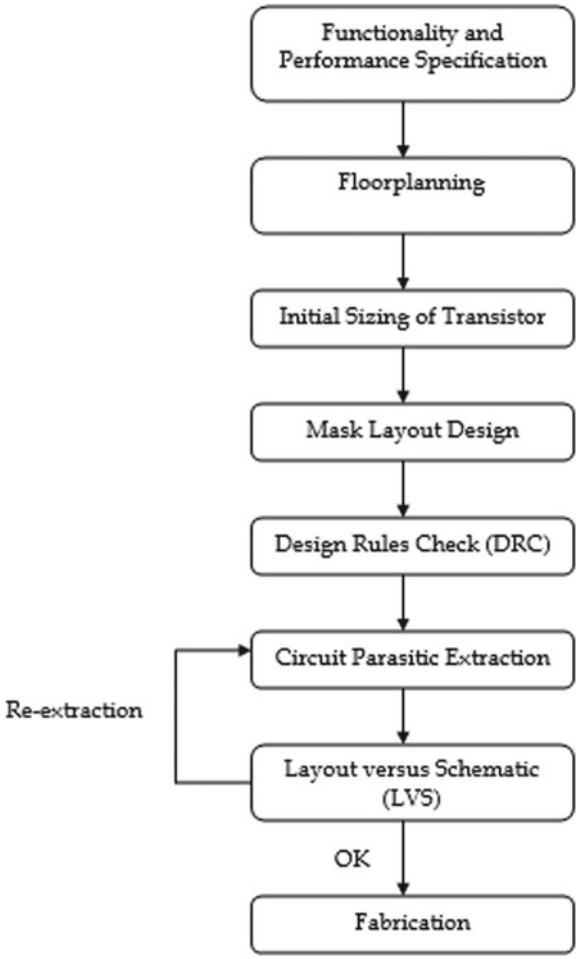

Fig. 28.1 SIC design flow

28.4 Layout Design Stages and Issues

IC design process is a game of war. It must be well planned and executed. A project leader who has very deep knowledge will lead the team. Team members are assigned to build up the block based on his capacity and skills. The work must accomplish within the time frame before tape-out dateline. The ultimate goal toward the end is the complete design must be functional, compact, and optimizing space intelligently.

28.4.1 Floorplanning

Floorplan is a draft of block placement associated with the total size of the silicon area. In certain circumstances, the total size of the floorplan could be in different shape depending on the silicon area allocated by the project manager. In this exercise, BSIC is the target of implementation. There are six blocks in BSIC and each block should occupy the space in different shape. Figure 28.2 shows the initial floorplan for BSIC. The six blocks are ring oscillator (ROSC), power on reset (POR), resistor divider, manual reset, power fail, and watchdog (WD).

The first decision to be considered in placing the block is the potential block that actively transits signals. The most active transition that occurs is the oscillator circuit. Oscillation causes active transition between two logics. This transition could transmit interference to other block due to the fact that all blocks are sharing the same substrate in silicon structure [5, 6]. The next decision is to identify block that responds to the interference. In confirming the theory and the advice of the expert to run away

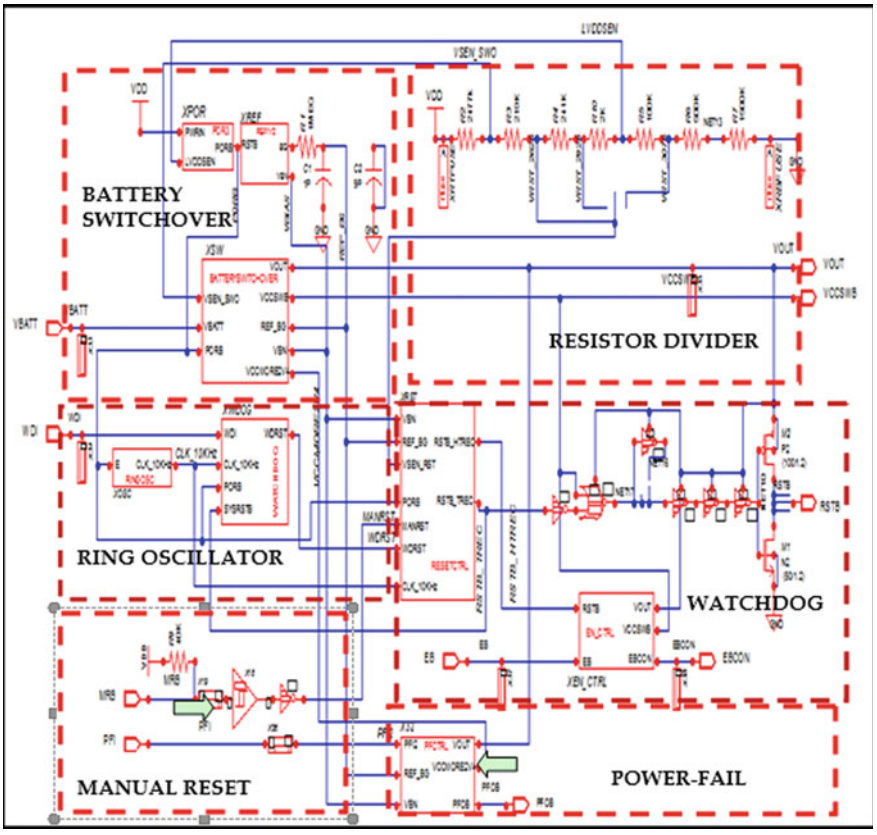

Fig. 28.2 Floorplan for BSIC

with this situation, the digital block must be separated with the analog block [7, 8]. Hence, the active block is the ring oscillator while the sensitive block is the battery switchover. Both must be separated with significant distance to avoid the transition of ring oscillator effecting the waiting signal mode of the battery switchover block.

28.4.2 Wire Size for Power Grid

Power issues in silicon need to be addressed efficiently with regards to simple concept the higher the number of transistor the bigger the wire. The most common issues in wiring is electromigration, whereby the wire is under stress when high current flows in the wire. According to the expert, the power grids should be the first issue that needs to be solved after floorplanning [5, 6]. Power supply lines and ground (VCC and GND) are large since both carry high amount of current, therefore they must be sized appropriately. Calculating the amount of current that flows in the power line will give easy estimation of size for the wire. The power lines are surrounding the entire blocks for easy access to each block. Each power line is set with 10 μm widths to compensate the total current consumption of 5 mA.

28.4.3 Wire Direction

Interconnecting technique becomes significantly important to avoid the issue of crosstalk. Overlapping wires between top and bottom layers could cause crosstalk. The overlapping area can behave as capacitor that is capable of storing charge. Charge is kept in that particular structure giving low impedance during resonant frequency. Therefore, crosstalk will occur. The best solution for this is by minimizing the cross over area between wires. The size of wire for single interconnect should be small. One of the best option as per expert say, all wires in one layer should emphasize with the same direction either horizontally or vertically. For example, if metal 2 is kept its direction horizontally, the adjacent layer (metal 1 and metal 2) should be placed vertically [9, 10]. Any cross area between the adjacent layers causes small parasitic value of capacitor. The small value of parasitic capacitor will give impact for crosstalk to happen. As shown in Fig. 28.3, metal1 layer is in vertical direction and metal2 layer is in horizontal direction.

28.4.4 Bond Pad Placement

Bond pads are metal “slabs” that are used to connect the external pins of the chip to the silicon layout. Generally, bond pads are located on the periphery of the chip as shown in Fig. 28.6. They are electrically connected to the devices within the

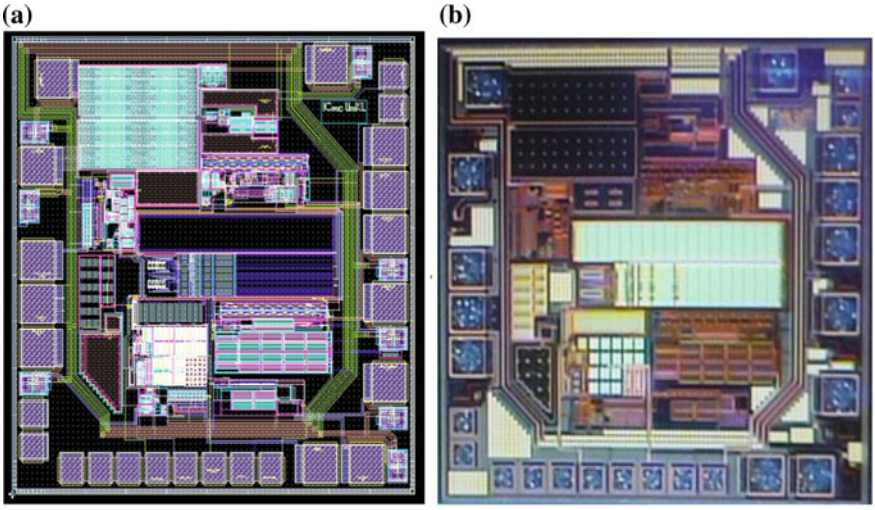

Fig. 28.3 **a** Layout from cadence. **b** Fabricated layout

ICs through buffers and electrically conducting interconnects. In the pad, a static discharge circuit is placed known as the electro-static discharge (ESD). The size for a bond pad for this chip is 80 μm × 80 μm.

Another pad known as probe pad is placed for testing purposes. A probe pad is placed when the node is not assessable and highly important to check the circuit's functional. In this case, ROSC output is one of the nodes to test its output for determining the frequency response. Probe pad size is much smaller; 50 μm × 50 μm.

28.4.5 Metal Density

Uniform metal layer is an important requirement for high yield in the fabrication process. Any empty space in metal layer should be filled up by dummy metal so that the total fill up area must be at the range of 30–70% [9, 10]. In BSIC structure, a set of dummy metal fills has been added to achieve minimum metal density as shown in Fig. 28.5.

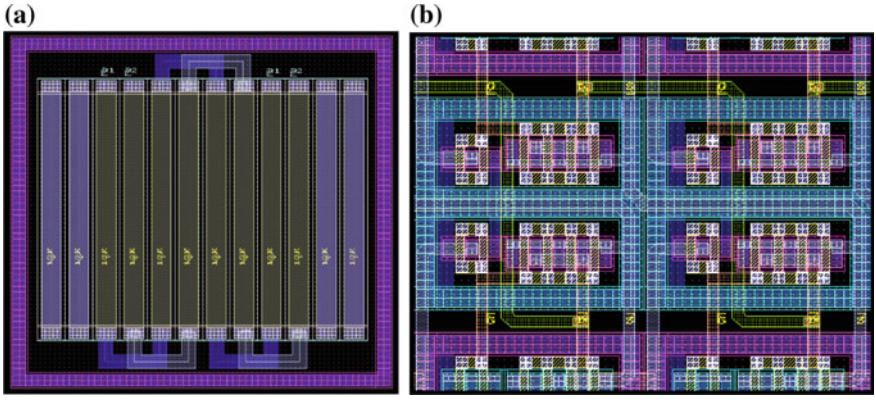

Fig. 28.4 **a** Dummy resistor 2 strip L/R **b** Polarization for p-substrate and n-well

28.4.6 Matching

In structuring devices on a chip, two identical resistors may not give the same performance. They are electrically different in term of carrier concentration. The neighboring components may also influence the performance due to parasitic element such as capacitor and resistor. In this case, a good solution is creating dummy devices. Dummy devices have identical structure with the devices under test. According to the expert, this can minimize the effect of process variations during fabrication. Figure 28.4 shows an example of resistor with twelve strips. Eight strips are used as resistor while two strips on left and right are functioned as dummy. The dummy strips are protecting the resistor from interference from neighboring components.

28.4.7 Transistor Arrangement

Polarization contact to substrate is a technique to eliminate latch-up effect in CMOS. The two transistors PMOS and NMOS are exposed to latch-up effect which causes damage when short circuit occurred. A solution is by shorting NWELL substrate for PMOS to VDD while P-substrate for NMOS is shorted to GND. This will secure the polarity of the substrate to permanently high and low. In addition to this, a maximum number of contacts depending on the space is recommended. Figure 28.4b shows the structure of transistor in the layout with four contacts for PMOS and NMOS, respectively.

28.4.8 Fingering

Fingering technique is used for creating large transistors. The finger structure is referring to the length of the polysilicon. Polysilicon is not a good conductor. It must be short to reduce the gate internal resistance. Therefore, for large transistor, the long polysilicon is chunk into number of fingers and each of them performs as a single transistor. All chunk transistors are connected in parallels for functioning as a single large transistor. There are two types of fingering technique; which are for wider W and larger L. PMOS with W = 60 μm/L = 0.6 μm and NMOS W = 30 μm/L = 0.6 μm as depicted in Fig. 28.6a, b shows the structure for width fingering. 12 fingers are applied to PMOS and NMOS.

While for larger L instead of polysilicon as fingering structure, diffusion is used as fingering element. Figure 28.6b shows the CMOS with the same size of NMOS and PMOS (W = 3 μm/L = 192 μm). The polysilicon size covering the diffusion fingers at the bottom. All the diffusion fingers are connected in series using METAL 1 and contact [9, 10].

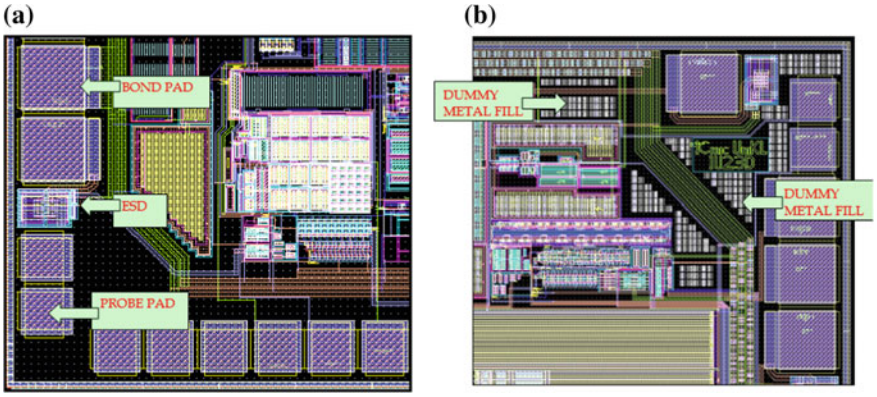

Fig. 28.5 **a** Bond and probe pad insertion. **b** Dummy fill up

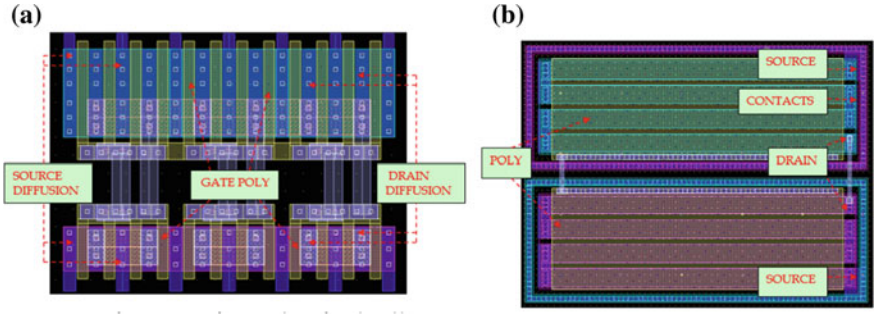

Fig. 28.6 **a** Fingering for width. **b** Fingering for length

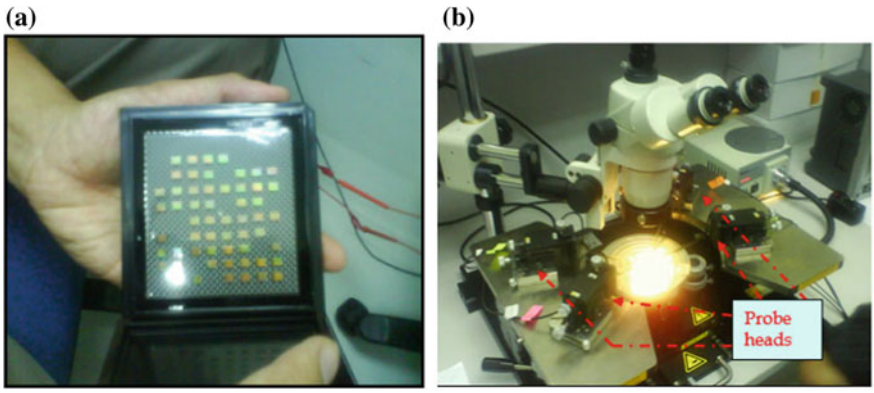

Fig. 28.7 **a** 20 Samples of silicon dies **b** Test bench and equipment

28.5 Layout of Battery Switchover IC (BSIC) Chip

The complete BSIC chip layout has been designed and fabricated. The silicon layout is shown in Fig. 28.2b. The total transistors that have been fabricated has 1091 transistors with the prototype die size of 1.0 mm × 1.0 mm. The prototype is manually tested to examine the performance of all the blocks using the wafer probing system (SUSS EP6 manual probe station, Fig. 28.7). Figure 28.8 shows three samples of waveform which are captured using the digital oscilloscope. All the waveform verifies that the silicon structure is performing accordingly against the specification.

28.6 Conclusion

Out of the 20 chips that have been tested, 70% are functioning as expected. The testing procedure using the manual probe station is targeting block for POR, ROSC, and WD. The testing results as shown in Fig. 28.8 verify the reset system is functioning accordingly and meets the specification at room temperature. However, there are some minor malfunctions for a few chips due to handling error during testing procedure such as chips contamination and scratched chips.

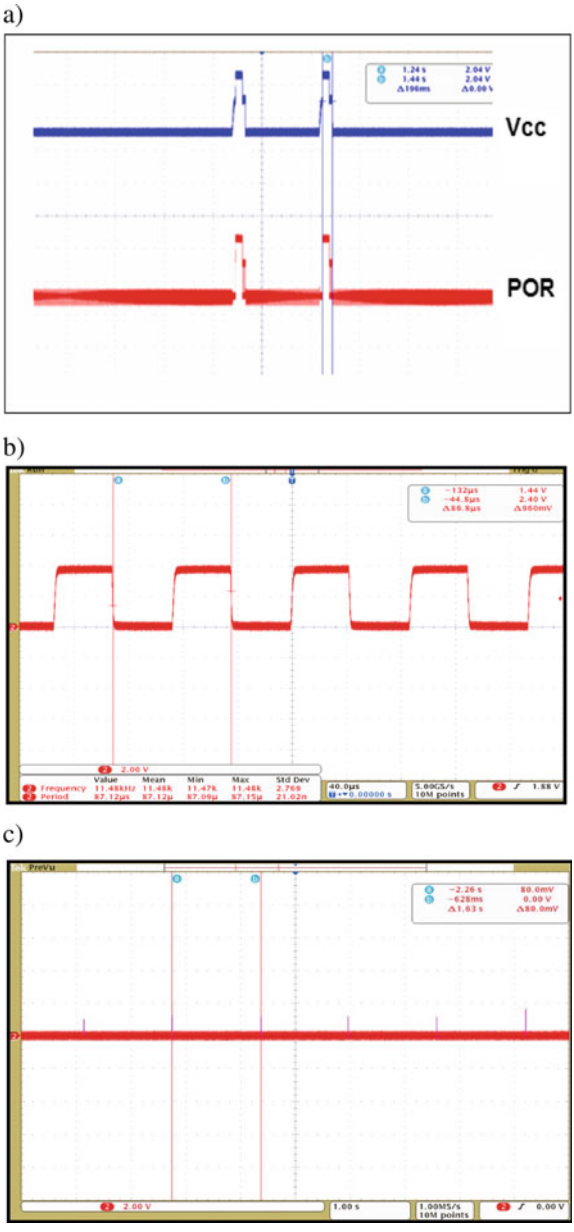

Fig. 28.8 **a** Battery switchover response **b** Ring oscillator output **c** Watchdog timer pulse trigger

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