Salt-Assisted Chemical Vapor Deposition Synthesis of 2D WSe_2 and Its Integration in High Performance Field-Effect Transistors

Anupama B. Kaul and Avra S. Bandyopadhyay

Abstract The synthesis of two-dimensional (2D) transitional metal dichalcogenides (TMDCs), including in the monolayer limit with control on crystallinity, is an important factor for their integration into a number of device platforms. Monolayer tungsten diselenide (WSe_2) has recently attracted a great deal of interest because of its tunable charge transport behavior, making it attractive for a variety of electronic and optoelectronic devices. However, the controlled and efficient synthesis of WSe_2 using chemical vapor deposition (CVD) is often challenging because of the high temperatures required to generate a steady flux of tungsten atoms in the vapor phase from the oxide precursors. Here, we use a salt (NaCl)-assisted process within the CVD furnace to reduce the growth temperature to ~750 °C, which is lower than the typical temperatures needed with conventional CVD for realizing monolayer WSe_2. The role of substrates also play an important role in the CVD growth process and we found that sapphire improves the optical and crystalline quality of both CVD-grown and mechanically exfoliated WSe_2 when compared with SiO_2/Si substrates. Finally, we fabricated WSe_2-based field-effect transistors using metal contacts of varying work functions and analyzed the interface properties in metal-2D WSe_2 junctions by extracting the interface state trap density, showing their promise for state-of-the-art electronic, optoelectronic, and quantum-optoelectronic devices using scalable synthesis routes.

Keywords Chemical vapor deposition · Tungsten diselenide · Raman and PL spectroscopy · Interface state density

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TMS 2022 151st Annual Meeting & Exhibition Supplemental Proceedings, The Minerals, Metals & Materials Series,
https://doi.org/10.1007/978-3-030-92381-5_48

Introduction

Two-dimensional (2D) materials, such as graphene and transition metal dichalcogenides (TMDCs), recently have attracted significant attention due to their unique properties and are widely used for fabricating electronics, optoelectronics, flexible and sensing devices [1–13]. Amongst the TMDCs, MoS_2 [7, 10] has been widely explored, but studies on WSe_2 are still in the relatively early stages. Moreover, WSe_2 offers unique attributes such as ultra-broadband detection spectral range, a high photoluminescence (PL) quantum yield (nearly unity), a strong spin–orbit coupling, all of which make it intriguing for high performance optoelectronic device applications such as photodetectors, light emitting diodes, and quantum-optoelectronics devices [4, 8, 14]. At the same time, practical device possibilities for WSe_2 rely on breakthroughs in the controlled and efficient growth of large-area films. Controlled CVD growth of WSe_2 is often challenging in comparison with MoS_2 since the metal oxide precursors employed for nucleating WSe_2, such as WO_3 is significantly more difficult to vaporize, that consequently yields a lower vapor pressure P for WO_3, compared to the MoO_3 precursor used for MoS_2 synthesis [8].

In this work, we have conducted experiments to optimize the synthesis of 1L and bi-layer (2L) WSe_2 by using a halide-assisted low-pressure CVD process, where NaCl was the halide of our choice which helps activate the tungsten from the oxide precursor to a lower growth temperature. Growth parameters of interest in our study included the NaCl concentration and growth T, where the role of these parameters on the properties of the *as-grown* WSe_2 crystals was examined. The choice of substrate is also an important parameter in CVD growth, as it directly impacts the crystalline quality of the material synthesized. We used two different substrates, SiO_2/Si and sapphire (Al_2O_3), for this study and the crystalline quality of WSe_2 was found to improve on sapphire. We have also analyzed the phonon lifetime τ in CVD grown and mechanically exfoliated WSe_2 and found that τ increases on sapphire substrates, suggestive of its higher crystalline quality due to a more pristine interface on sapphire when compared to SiO_2.

At the same time, interfaces play an important role to determine device performance figures-of-merit. Compared to traditional semiconducting materials such as silicon, Ge, or III−V materials, the 2D materials, including TMDCs, exhibit pristine surfaces with minimal dangling bonds which should facilitate the realization of interface states with low-interface trap density. This is particularly pertinent at metal–semiconductor hetero-junctions where a high interface trap density can often degrade device performance. In the second part of this work, we discuss the fabrication of WSe_2 field-effect-transistors (FETs) using metals with different work functions, where we have analyzed the metal-2D WSe_2 interface properties. The conductivity of WSe_2 was found to be *p*-type, ambipolar, and *n*-type with Au (with Ti as adhesion layer), Mo, and Al metal contacts, respectively. The interface state properties in the metal-2D WSe_2 junctions were also investigated using capacitance-frequency measurements.

Experimental

In this study, WSe_2 nanosheets were grown using a halide-assisted CVD method and the details of the synthesis process is described in our previous work [8]. In short, a CVD furnace with a three-foot quartz reaction tube was used for the WSe_2 synthesis on either SiO_2/Si (270 nm) or C-plane (0001) sapphire substrates. The optical image of the setup is shown in Fig. 1a. Selenium powder was placed upstream at a position that yielded a $T \sim 270$ °C during the growth, while a mixture of $WO_{2.9}$ and NaCl was placed at the center of the furnace. The substrates were placed downstream and face-down, while a mixture of Ar and H_2 was introduced as the carrier gas. The center of the furnace was ramped to 750 °C at a ramp rate of 10 °C/min for the growth phase. When the center heating zone reached 750 °C, this translated to a $T \sim 700$ °C at the substrate location. During the growth process, the flow rate of Ar/H_2 was kept at 120/30 sccm, and the chamber P was ~ 6 Torr throughout the growth run. The WSe_2 nanosheets were also mechanically exfoliated on top of SiO_2/Si ($t_{ox} \sim 270$ nm) and sapphire substrates using the scotch tape method [1]. The samples were characterized using Raman and PL spectroscopy using a LabRAM HR Evolution NIR microscope equipped with a 532 nm laser for excitation. The WSe_2-based FETs were fabricated using a standard e-beam lithography process using the JEOL JSM-7001F SEM and XENOS XPG 2 EBL pattern writer. The electrical measurements were conducted using a state-of-the-art Lakeshore probe stage (CRX-4 K) interfaced to an ultra-low noise semiconductor parameter analyzer (Keysight B1500A).

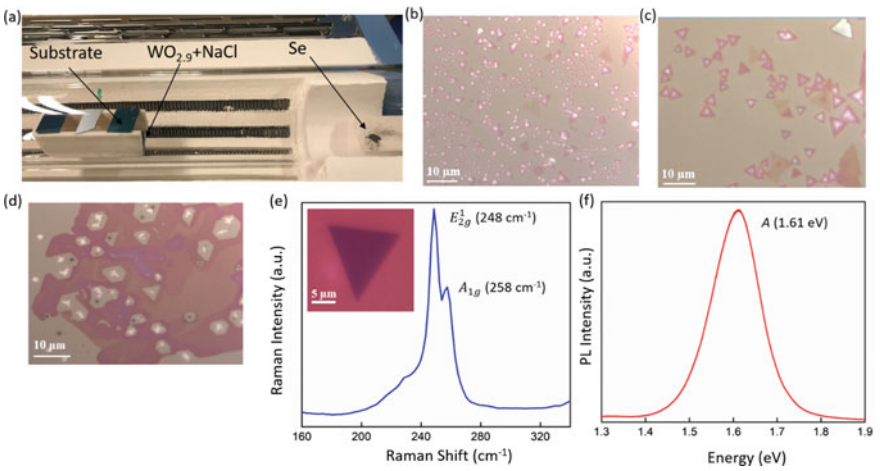

Fig. 1 **a** The optical image of the CVD furnace for the growth of WSe_2. **b–d** The optical images of the WSe_2 nanocrystallites grown due to incomplete nucleation. The **e** Raman and **f** PL spectra of monolayer WSe_2. Inset of (**e**) shows the optical image of monolayer WSe_2

Results and Discussion

CVD Growth Analysis of WSe_2

In this study we implemented a salt-assisted CVD method to synthesize WSe_2 nanosheets. In particular, NaCl was used to reduce the growth T of WSe_2 with the formation of volatile tungsten oxyhalides [15]. Several important CVD growth parameters were systematically varied in order to optimize crystalline quality. Among these parameters, the amount of precursors used, such as Se, $WO_{2.9}$, and NaCl, were found to be the two variables that appeared to have a significant influence on the growth of our WSe_2 crystallites. Figure 1b–d shows the optical images of the WSe_2 nanosheets due to incomplete nucleation of the WSe_2 seeds, attributed to the low amount of NaCl used in the mixture. For example, Fig. 1b shows the WSe_2 nanosheets grown using CVD where the amount of Se, $WO_{2.9}$, and NaCl used were 15.9 mg, 22 mg, and 4 mg, respectively, while Fig. 1d shows the WSe_2 nanosheets grown using CVD where the amount of Se, $WO_{2.9}$, and NaCl used were 15 mg, 22.3 mg, and 5 mg, respectively. However, with careful optimization of the growth parameters, we were successfully able to synthesize WSe_2 nanosheets at a growth T of ~750 °C where the ratio of $WO_{2.9}$ and NaCl was tuned to be in the 7:3 ratio.

Thereafter, Raman and PL spectroscopy were used to evaluate the quality of our synthesized WSe_2 crystals. The Raman spectra of monolayer WSe_2 is shown in Fig. 1e at room T, where the two characteristic peaks for WSe_2 at 248 cm^{-1}, assigned to the in-plane E^1_{2g} vibrational mode, and at 258 cm^{-1}, assigned to the A_{1g} out-plane vibrational mode, are observed [16, 17]. The inset of Fig. 1e shows the optical image of the *as-grown* monolayer WSe_2 nanosheets. Figure 1f depicts a typical PL spectra of monolayer WSe_2 nanosheets which exhibits a strong emission at ~1.61 eV and the single, symmetric PL *A*-peak suggests the direct band gap nature of monolayer WSe_2, which is in excellent agreement with other recent PL reports for monolayer WSe_2 [8, 16, 18].

To study the impact of the halide content, the ratio of $WO_{2.9}$ and NaCl was varied from 7:1 to 7:4, while the growth T was fixed at 750 °C, and the full-width-half-maxima (FWHM) of the PL *A*-peak for 1L WSe_2 is shown in Fig. 2a. The lowest value of the FWHM in the PL *A*-peak was also found to be ~0.13 eV when the mixing ratio was 7:3, as shown in Fig. 2a. Additionally, the ratio of the PL and Raman intensity (I_{Lum}/I_{Raman}) has been utilized as a metric to gauge optical quality of TMDCs to determine the intrinsic luminescence quantum efficiency [8, 19]. In our study, I_{Lum} and I_{Raman} represent the intensities of the PL *A*-peak and the Raman E^1_{2g} peak, respectively, and the secondary y-axis of Fig. 2a shows I_{Lum}/I_{Raman} as the oxide-to-halide ratio is varied. It was found that the I_{Lum}/I_{Raman} was maximized at ~ 0.30 when the mixing ratio was 7:3. The PL spectra for 1L WSe_2 at various oxide-to-halide ratios are also shown in Fig. 2b, from which it can be inferred that the lowest full-width-half-maximum (FWHM) was ~0.13 eV obtained when the ratio is 7:3.

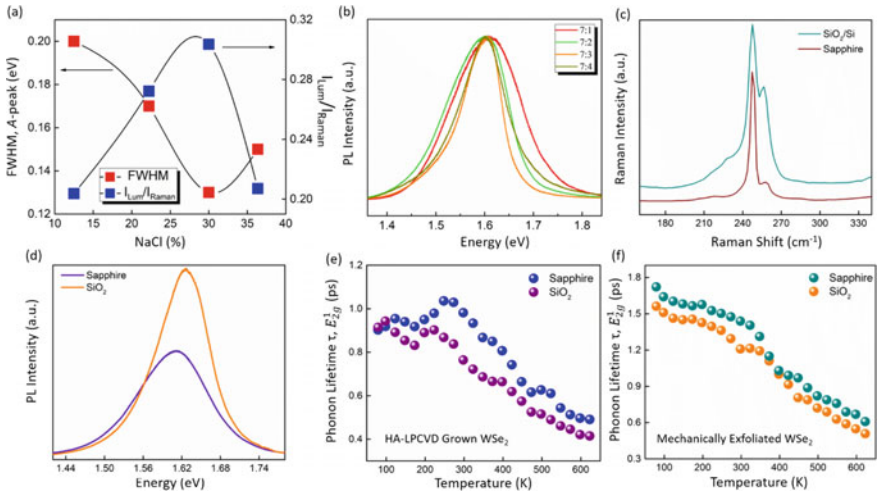

Fig. 2 **a** The dependence of the FWHM of the PL *A*-peak and I_{Lum}/I_{Raman} ratio as a function of the halide ratio for 1L WSe_2 at $T = 750$ °C. **b** PL spectroscopy of monolayer WSe_2 grown using varying oxide-to-halide ratios. **c** Raman and **d** PL spectra of monolayer WSe_2 grown on SiO_2/Si and sapphire substrates. Comparative analysis of T-dependency of phonon lifetime in **e** CVD grown and **f** mechanically exfoliated WSe_2 on SiO_2/Si and sapphire substrates

Role of Substrate in WSe_2 Nanocrystallites

Next, we move to analyze the role of substrates in influencing the crystalline quality of CVD grown WSe_2. Figure 2c and d shows a comparative analysis of the Raman and PL spectra, respectively, of monolayer WSe_2 grown on sapphire and SiO_2/Si substrates under the optimized metal oxide-to-halide ratio of 7:3 and a growth T of ~750 °C, as discussed earlier. The intensity of the *A*-peak PL emission on sapphire was nearly ~2 × higher when compared to SiO_2/Si substrates, as is evident in Fig. 2d.

Additionally, $I_{\text{Lum}}/I_{\text{Raman}}$ was found to be 0.76 for sapphire while it was calculated to be ~0.30 at the most optimal conditions for SiO_2/Si substrates; this data is clear evidence for the improved optical quality of 1L WSe_2 grown on sapphire. A further gauge of crystalline quality is the PL FWHM, where the FWHM of the *A*-peak seen Fig. 2d was narrower for WSe_2 on sapphire (~0.08 eV), compared to ~0.13 eV for SiO_2/Si.

Phonon lifetime τ is an important parameter to analyze the optical quality in the crystal and it is calculated using the energy uncertainty relationship, with the phonon linewidth Γ as given by Eq. (1) below [20, 21],

$$\tau = \frac{\hbar}{\Gamma} \tag{1}$$

where τ is in picoseconds, and $\hbar$ is Planck's constant (~5.3 ps-cm^{-1}). The value of τ for CVD grown monolayer WSe_2 on SiO_2/Si and sapphire for the E^1_{2g} mode at $T = 298$ K was found to be ~ 0.76 ps and 0.98 ps, respectively. Figure 2e and f show τ for CVD grown and mechanically exfoliated monolayer WSe_2, respectively, on SiO_2/Si and sapphire substrates, where the mechanical exfoliation is conducted using the scotch tape approach, details of which are provided in the Experimental Section. The lifetime τ was found to decrease at higher T due to the higher probability for *phonon–phonon* and *electron–phonon* interactions leading to dissipation, as was reported in our earlier works [8, 21]. As seen from Fig. 2e and f, τ is higher for WSe_2 on sapphire which is attributed to the superior quality of monolayer WSe_2 on sapphire for both CVD-grown and mechanically exfoliated samples.

Role of Metal Contacts in Electrical and Interface State Properties in WSe_2-based FETs

In the second part of our work, we report here, WSe_2 FETs fabricated using metals with different work functions ϕ_m, such as Au (ϕ_m ~ 5.47 eV), Mo (ϕ_m ~ 4.53 eV), and Al (ϕ_m ~ 4.08 eV). The conductivity of WSe_2 was found to be *p*-type, ambipolar, and *n*-type with Au, Mo, and Al metal, respectively, which is in accordance with our previous work [10] and other reports [21]. The gate leakage currents for the Au/Ti/WSe_2, Mo/WSe_2, and Al/WSe_2 FETs are shown in Fig. 3a–c. The Au/Ti/WSe_2, Mo/WSe_2, and Al/WSe_2 FETs were also annealed in vacuum conditions and the mobilities were found to increase post-annealing treatment.

Frequency-dependent conductance G_p measurements have been carried out to investigate the interface properties between the metal and 2D WSe_2 as it is very important to determine the effects of the interface trap states in the metal–semiconductor (MS) junction. It is possible to calculate the interface trap density, i.e., D_{it} by investigating the MS Schottky junction at different frequencies f as the filling and refilling of the trap states cause a measurable change in the capacitance of the junction. The values of D_{it} can be obtained from the G_p/ω- ω plot which is shown in Fig. 4a–c for Au/Ti/WSe_2, Mo/WSe_2, and Al/WSe_2 junctions, respectively.

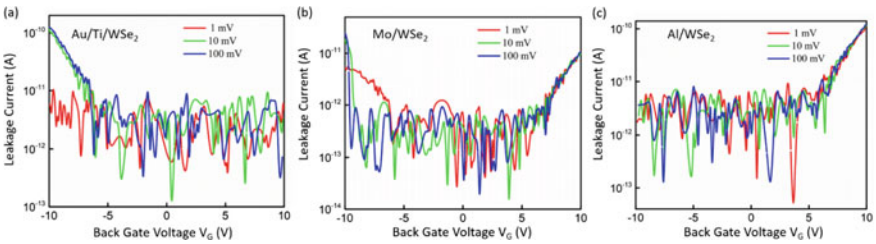

Fig. 3 The gate leakage currents in **a** Au/Ti/WSe_2, **b** Mo/WSe_2, and **c** Al/WSe_2 FETs. The leakage currents were found to stay mostly at the noise-floor (~10-10 A-10-14 A)

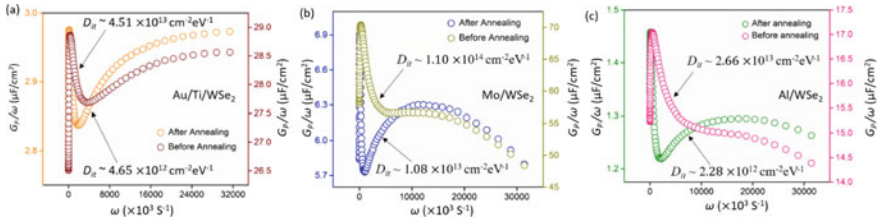

Fig. 4 The normalized conductance vs angular frequency G_p/ω- ω plots for **a** Au/WSe_2, **b** Mo/WSe_2, and **c** Al/WSe_2 MS junctions before and after annealing

The normalized conductance is expressed as [22, 23],

$$\frac{G_P}{\omega} = \frac{q D_{it}}{2\omega\tau_{it}} \ln\left[1 + (\omega\tau_{it})^2\right] \tag{2}$$

where τ_{it} and ω are the interface trap time constant and angular frequency ($\omega = 2\pi f$), respectively.

For the maximum value of the peak, the first derivative of Eq. (2) was taken, and the density of interface states and the interface trap time constant were expressed as,

$$D_{it} = \frac{2.5}{q}\left(\frac{G_P}{\omega}\right)_{max} \tag{3}$$

The values of D_{it} were calculated to be ~4.51 × 10^{13} cm^{-2} eV^{-1}, 1.11 × 10^{14} cm^{-2} eV^{-1}, and 2.66 × 10^{13} cm^{-2} eV^{-1} for Au/Ti/WSe_2, Mo/WSe_2, and Al/WSe_2 junctions, respectively, at room temperature which shows that the D_{it} is the lowest for Au/Ti/WSe_2 FET. It was also found that the value of D_{it} decreases by an order of magnitude with post-annealing treatment for Au/Ti/WSe_2, Mo/WSe_2, and Al/WSe_2 devices, which are lower than the previously reported values for D_{it} in WSe_2-based devices [24]. These results confirm the role of annealing to improve interface properties in metal-2D WSe_2 junctions.

Conclusions

In conclusion, we have synthesized WSe_2 using a salt-assisted CVD method, where NaCl was added to $WO_{2.9}$ to lower the growth T to ~750 °C at an optimized 7:3 metal oxide-to-halide ratio. The role of substrates on WSe_2 crystallites was also studied and it was found that the optical and crystalline quality of WSe_2 improved when sapphire was used as the substrate. Moreover, the value of τ was found to be ~0.78 ps and 0.98 psfor our CVD grown monolayer WSe_2 on SiO_2/Si and sapphire substrates,

respectively, indicating the superior quality of WSe_2 on sapphire. Finally, we fabricated WSe_2-based FETs using Au/Ti, Mo, and Al as the metal contacts and the conductivities of WSe_2 were found to be *p*-type, ambipolar, and *n*-type, respectively. The interface state density D_{it} was also extracted to be ~4.51×10^{13} cm^{-2} eV^{-1}, 1.11×10^{14} cm^{-2} eV^{-1}, and 2.66×10^{13} cm^{-2} eV^{-1} for Au/Ti/WSe_2, Mo/WSe_2, and Al/WSe_2 junctions, respectively. Our results validate the potential of 2D WSe_2 as a promising 2D semiconductor for electronics, optoelectronics, and quantum-scale systems.

Acknowledgements We are extremely grateful to the Air Force Office of Scientific Research (grant number FA9550-15-1-0200) and the National Science Foundation (grant number NSF ECCS 1753933) who provided funding support that enabled us to pursue this work. A.B.K. also acknowledges support from the PACCAR Technology Institute and the Endowed Professorship support at the University of North Texas.

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