Design of Sports Dance Online Interactive Teaching System Based on Intelligent Terminal

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Abstract. This research designs an online interactive teaching system of sports dance based on intelligent terminal. In the hardware part of the system, the processor, memory and storage circuit, wireless transceiver circuit, power circuit, liquid crystal display module and circuit module are designed; In the software part of the system, the data in the system are mainly processed, and the corresponding database is designed. The experimental results show that the sports dance online interactive teaching system based on intelligent terminal not only improves the storage capacity of the system, shortens the response time of the system, but also improves the maximum concurrent number of the system, which shows that it has high practical significance and can effectively realize the online teaching of sports dance.

Keywords: Intelligent terminal · Sports dance · Online interaction · Teaching system

1 Introduction

Sports dance is a dance of international social activities, which plays an important role in enriching human life and improving human self-cultivation. However, due to the limitation of time and space in traditional dance teaching, it is difficult for the majority of fans to arrange time to study reasonably [1].

With the continuous development and maturity of computer network technology and communication technology, online teaching has become a reality. The use of online video teaching can make up for the limitations of traditional sports dance teaching, so that people do not have to learn sports dance at a designated time and place, which can increase the interest of dance lovers and improve dance.

Generally speaking, the sports dance video teaching system uses the combination of sports dance and computer technology, uses the recorded dance teaching video to express the teaching content of the course in a digital form, and uses the establishment of a database to compare the various teaching resources in the teaching system and Student and teacher information is stored and managed. It can not only effectively manage teaching resources, but also provide learning opportunities for fans more clearly and conveniently through video teaching. At present, the commonly used teaching systems

mainly include online interactive teaching system of sports dance based on VEM framework and online interactive teaching system of sports dance based on VEM framework of Leap Motion Motion controller. However, it is found in practical application that the above-mentioned traditional system has some shortcomings such as poor storage capacity and long response time.

Smart terminals are also called mobile smart terminals, mainly including mobile phones, tablets, laptops, vehicle-mounted smart terminals, PDA smart terminals, wearable devices, etc. In our country, students, no matter in primary and secondary schools, generally have mobile phones. This creates conditions for the development of teaching based on intelligent terminals. Therefore, in view of the shortcomings of the traditional system, this research is based on the intelligent terminal to design the online interactive teaching system of sports dance.

2 Hardware Design of Sports Dance Online Interactive Teaching System

The hardware structure of Sports Dance online interactive teaching system is shown in Fig. 1.

In Fig. 1, the data layer mainly stores teaching data in the form of XML database. The data layer takes knowledge points as the core; the intermediate agent layer mainly interacts with the system after the learners log in to the system and returns to the information base according to the learners' learning results; the realization layer mainly accepts the user's request and returns the generated formatted data to the page.

2.1 Processor Design

ARM's Cortex-M3 processor is the latest generation of embedded ARM processors. It provides a low-cost platform, reduced pin count, reduced system power consumption, and excellent computing performance for the needs of MCU. And advanced interrupt system response. In addition, ARM's Cortex-M3 processor is a 32-bit RISC processor, which provides additional code efficiency and exerts the high performance of the ARM core in the storage space of the usual 8-bit and 16-bit systems [2, 3].

Stm32f103zet6 is a high-performance arm Cortex-M3 32-bit RISC microcontroller produced by stm32f103zet6. Therefore, it is compatible with all arm development tools and software. Stm32f103xx is a complete series, its members are completely foot to foot compatible, software and function are also compatible. In the reference manual, stm32f103x4 and stm32f103x6 are classified as small capacity products, stm32f103x8 and stm32f103x B are classified as medium capacity products, and stm32f103x C, stm32f103x D and stm32f103x e are classified as large capacity products. Small capacity products have smaller flash memory, RAM space and fewer timers and peripherals. The high-capacity products have larger flash memory, RAM space and more on-chip peripherals, such as SDIO, FSMC, I2S and DAC, while maintaining compatibility with other products of the same series.

STM32F103ZET6 is mainly equipped with 3 12-bit analog-to-digital converters, 1us conversion time, up to 21 input channels; 2-channel 12-bit digital-analog converter;
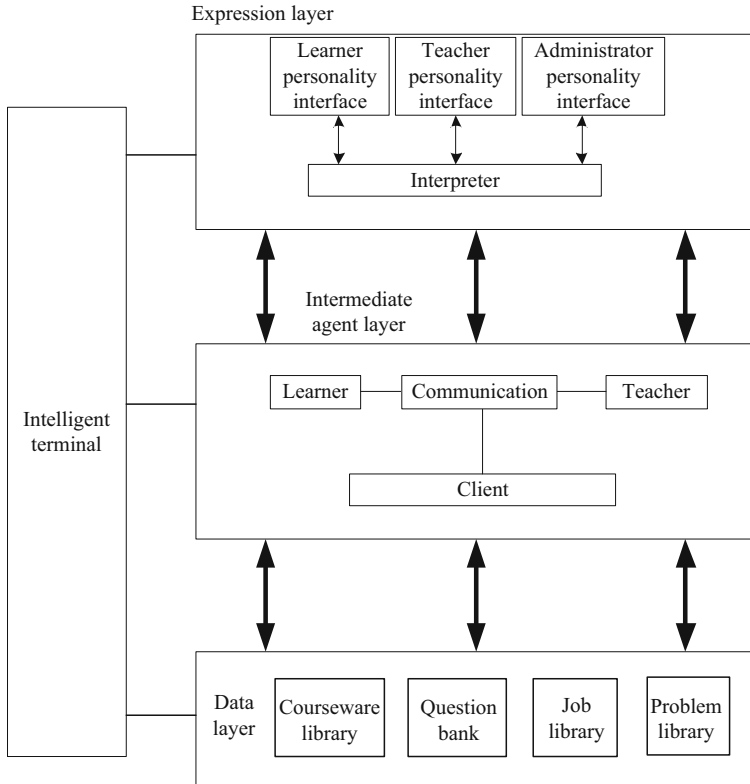
Expression layer

Fig. 1. Hardware structure of online interactive teaching system of sports dance

12-channel DMA controller; up to 11 timer, Are 4 16-bit timers, each timer has up to 4 channels for input capture, output comparison, PWM or pulse counting and incremental encoder input [4, 5]; 2 16-bits with dead zone Control and emergency braking, PWM advanced control timer for motor control; 2 watchdog timers (independent and window type); 2 16-bit basic timers for driving DAC; 1 system time timer: 24-bit self-decreasing counter; up to 13 communication interfaces, respectively 2 I2C interfaces; 5 USART interfaces; 3 SPI interfaces, 2 of which can be reused as I2S interfaces; Controller area network CAN interface (2.0B Active); USB 2.0 full-speed host/slave/OTG interface; up to 112 users can operate general-purpose I/O pins; debug mode has a serial single-wire JTAG debug port.

2.2 Design of Memory and Storage Circuit

SRAM is a kind of static random access memory. SRAM uses registers to store information, and it can save the internal data without refreshing the circuit. Therefore, SRAM has high performance, and the speed of SRAM is very fast, so it is the fastest read-write storage device at present [6–8]. SRAM needs four to six transistors and some other parts, while DRAM only needs one transistor and a small capacitor for the same memory cell.

Therefore, for SRAM and DRAM with the same capacity, the cost of SRAM is much more expensive than DRAM, and the chip area is also larger.

Therefore, this system chooses 256K × 16bit SRAM, the model is IS61WV25616BLL-10TLI, it is a high-speed asynchronous CMOS performance SRAM produced by ISSI company, the operating frequency can be up to 125 MHz, the operating voltage is 3.3 V, and the operating power consumption The maximum is 85 mW, the static power consumption is 7 mW, with three-state output, the data read and write control is divided into high byte and low byte, and the address line and data line operate independently [9].

In SRAM, the decoder and interface circuit with external signal are around the array of memory cells arranged in matrix form. Memory cells are usually in the form of square or matrix to reduce the area of the whole chip and facilitate data access. A0-a17 is the address input, I/o0-i/O15 is the data input and output, and /CE is the chip enabling end. The low level is effective. When the driving level is low, the device is enabled. /OE is the data output enable end, low level valid, / we is the write enable end, low level valid, /Ub and /lb are the high and low byte control end, low level valid respectively. SRAM operation is divided into read operation and write operation. When the address of MCU /lb /CE is low, the data can be read from MCU /lb /CE Write data. The function of high and low byte control terminals /Ub and /lb is to facilitate users to write or read only one byte of data at a time [10].

2.3 Wireless Transceiver Circuit Design

The RF wireless transceiver module is also the core module of the system. This research uses CC1101RF transceiver to design RF wireless transceiver module. The CC1101RF transceiver is a sub-1 GHz high-performance radio frequency transceiver launched by Texas Instruments. It is Chipcon's Smart RF 04 technology based on a 0.18 micron CMOS crystal and is designed for extremely low power RF applications. The CC1101RF transceiver integrates a highly configurable modem. This modem supports different modulation formats, and its data transfer rate can reach 500 kbps. By turning on the forward error correction option integrated on the modem, performance can be improved. In addition, the CC1101RF transceiver provides extensive hardware support for data packet processing, data buffering, burst data transmission, clear channel assessment, connection quality indication and electromagnetic wave excitation.

Cc1101rf transceiver can provide a wide range of hardware support for packet processing, data buffering, burst transmission, received signal strength indication (RSSI), idle channel assessment (CCA), link quality indication and wireless wake-up (wor). Cc1101rf transceiver is compatible with CC1100 in code, package and external pin. It can be used in the most commonly used open RF design with frequency lower than 1 GHz in the world. The main characteristics of cc1107 transceiver are as follows:

- Small size (QLP 4 × 4mm package, 20 pins);
- Real single chip UHF RF transceiver;
- Frequency bands: 300–348 MHz, 400–464 MHz and 800–928 MHz;
- High sensitivity (- 110D BM at 1.2 kbps, 1% packet error rate);
- The programmable data transmission rate can reach 500 kbps;

- Low current consumption (15.6 m a, 2.4 kbps, 433 MHz in Rx);
- The output power of programmable control can reach + 10d BM for all supporting frequencies;
- Need few external components: on chip frequency synthesizer, no external filter or RF conversion;
- The programmable baseband modem supports 2-fsk, GFSK, MSK and ook;
- Optional forward error correction with interleaving;
- Separate 64 byte RX and TX data FIFO;
- Efficient SPI interface: all registers can be controlled by a "burst" converter.

The working principle of CC1101RF transceiver is as follows: CC1101RF transceiver chip has multiple functional modules, mainly including low noise amplifier (LNA), power amplifier (PA), analog-to-digital converter (ADC), multiplier, 90-degree phase shifter, Baseband modem and frequency synthesizer, etc. When receiving data, the CC1101RF transceiver can be used as an IF (Intermediate Frequency) receiver. The received RF signal first passes through a low-noise amplifier (LNA) to amplify the useful signal and suppress noise, and then down-convert to an intermediate frequency (IF) through a mixer. At the intermediate frequency, two orthogonal components he signals I and Q are respectively converted into digital signals through two analog-to-digital converters (ADC) [11, 12]. After the two digital signals are controlled by forward error correction, they are packed and stored in the 64Byte receive buffer (RXFIFO). Wait for the microcontroller to read the data. The transmitted data of CC1101 is based on the direct synthesis of RF frequency. Its internal frequency synthesizer includes a complete LC voltage-controlled oscillator (VCO) and a 90-channel signal generated by the down-conversion mixer in the receiving mode. Degree phase shift network. The transmitted data is first stored in the 64Byte transmission buffer, and then the data is packaged and modulated. The modulated signal is directly generated by the frequency synthesizer and then passed through the phase shift network and power amplifier (PA), and finally transmitted through the antenna.

2.4 Design of Power Supply Circuit

The battery panel uses 36 ah, 12 V maintenance free lead-acid battery as the energy storage element, that is, the output voltage of the battery is 12 V. When selecting the power conversion chip for 5 V voltage conversion circuit, it is necessary to have an overall evaluation of the overall power consumption of the system. In order to make the power conversion chip meet the maximum load requirements of the system and leave a certain margin, at the same time, it is necessary to consider the efficiency of chip conversion. 5 V power supply is mainly for LED The display power consumption is relatively large, and the maximum power consumption can reach several watts. Considering the above factors, in this system, the 5 V voltage conversion chip selects the Synchronous Step-Down Switching Regulator lm2576-5.0v of national semiconductor company, which can provide various functions of the step-down switching regulator, and can drive 3 A at most It contains a frequency compensator and a fixed frequency oscillator of 52 kHz, which can reduce the number of external components to the minimum and make the designer more convenient.

2.5 LCD Module Design

Syg128641 LCD module is adopted, which is a 128×64 dot matrix LED backlight STN LCD with blue background and white characters. With negative pressure conversion function, its connection principle is shown in Fig. 2.
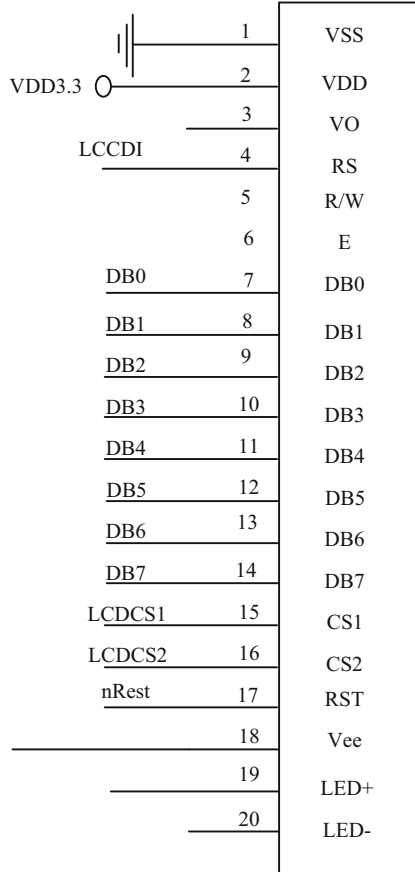

Fig. 2. Partial connection diagram of LCD module

In Fig. 2, DB0–DB7 represent data line 0~data line 7, VOUT represents voltage output, LEDA represents backlight input, RD represents read signal, CE represents chip select signal, and C/D represents command/data selection.

2.6 Liquid Crystal Display Module Circuit Design

The integrated LCD controller of OMAP-L138 includes two independent controllers, one raster controller and one LCD display interface display driver (Lido) controller. Each controller operates independently and only one controller can be effective at the

same time. Grating controller is used to process synchronous LCD interface [13], which provides clock and data for continuous graphic refresh of passive display; Lido controller supports asynchronous LCD interface, which provides programmable control signal and output data. The maximum resolution supported by LCD controller is 1024×1024 pixels, and the maximum frame rate is determined by image size and clock frequency. LCD controller supports two kinds of LCD, STN (super twisted nematic) LCD and TFT (thin film transistor) LCD.

This research uses POWERTIP's TFT LCD PH320240T-005-IQ, which has a resolution of 320×240 pixels, supports 24bit RGB (red, green, and blue) color mode, uses 3.3 V power supply, and its operating current is generally 75 mA. The dot clock frequency is 6.4 MHz. The internal LCD controller of OMAP-L138 only provides 16 data lines, while the selected LCD screen PH320240T-005-I-Q has a total of 24 data lines. In this design, the excess 8 data lines are directly pulled up. The LCD_AC_ENB_CSn signal is used here as the LCD controller data output enable signal, that is, the DE signal. In order to ensure the high quality of the liquid crystal display, this design adds a resistance of 33 Ω to the data line, clock line and control line to do impedance matching processing to eliminate signal reflection and ensure signal integrity [14, 15].

3   Software Design of Online Interactive Teaching System for Sports Dance

3.1   Teaching Data Processing

Based on the hardware design of the above-mentioned sports dance online interactive teaching system, the software design of the sports dance online interactive teaching system. Under the intelligent terminal, the software development of the sports dance online interactive teaching system is mainly composed of teaching resources, bulletin boards, resource downloads, student communication and management systems, in order to meet the functions of downloading and sharing learning resources of students, and understanding the latest learning trends. Teachers can also use the software to publish news and carry out teaching to complete classroom teaching and experimental analysis.

The software designed this time mainly includes news updates, bulletin boards, download centers, communication areas, system management, course introduction, teaching methods, syllabus, teaching plans, bibliography, electronic courseware, stereo and answers, case addition and deletion functions. In order to avoid conflicts between various functions in the system, a resource database is constructed, and the port of the sports dance online classroom teaching system is connected to the database to ensure that the data transmission speed is increased when resources are requested to download. In addition, set the user authentication function in the system software, because there are more users using the software, if there are more users accessing a project at the same time, there will be a stuck phenomenon, so set the user authentication function. According to the different identities of teachers and students, access to different system resources. So as to improve the use of the online classroom teaching system. The user authentication link needs to mobilize the database to complete, so it is necessary to enter the relevant information of teachers and students in the online classroom teaching

software to improve the response speed of the system. The implementation steps are as follows:

First, user requirements are abstracted as information structure, which is also the basis of database design;

Second, construct the result tree, add any structure through filtering and reordering, and judge the data attributes. The calculation formula is as follows:

$$|G| = \frac{v \in t}{\int V \times K_i} \tag{1}$$

In formula (1), $|G|$ is the data in the database, $\int V$ is the data attribute, K_i is the attribute determination factor, and $v \in t$ represents the attribute of the data v is t.

Third, the attributes of the data are obtained through the above calculations, and the result tree is constructed according to the attributes of the data;

Fourth, format the system data and use the following formula to achieve:

$$G \log = \sqrt{\frac{p_{bv}}{Z \times v}} \tag{2}$$

In formula (2), $G \log$ stands for formatting factor, Z stands for data entity attributes, v stands for configuration data, and p_{bv} stands for data hierarchy logic.

Fifth, the formatted vocabulary specified in the XML document is implemented to construct the result tree. Each type of data in the database corresponds to a formatted object class. Mapping process is shown in Fig. 3.
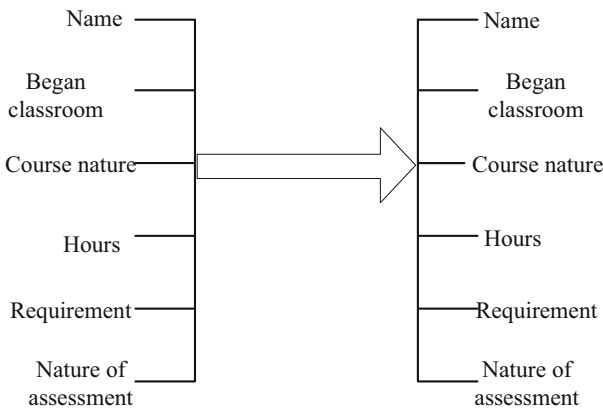

Fig. 3. Data mapping process

When an attribute of a data in the system database has the same attribute value in multiple object instances, all the system name information is stored in a single database table to avoid data redundancy;

Sixth, create a course group. In the process of creating, if the service nature of assessment encounters an access request, it first executes the data segment. Because the

amount of data mapped to the library table is large, which affects the query efficiency, it creates a course group, stores the same kind of data information in the unified curriculum table, and then returns the execution result to the system together with the JSP file;

Seventh, test function, which is the core part of the distance teaching management system, separates the generation and display of the content in the system. According to the result of separation, the level of students is distinguished. The degree of discrimination of each test question in the system is determined in advance by an experienced teacher, and is continuously adjusted according to the test takers' scores. The mathematical expression of the overall degree of discrimination is:

$$Q_n = \left(\sum_x j \times W_j \right) / M \tag{3}$$

In formula (3), Q_n is the discrimination degree of question n, W_j is the full score of question j, $\sum_x j$ is the full score of the whole paper, and M is the test taker's score.

The calculation process and results are stored in the database, so that the system can continuously improve the database structure according to the level of students.

3.2 Database Design

The data after the above processing is stored, and the relevant information of the relationship table between the main entities in the database is shown in Table 1.

Table 1. The relationship table between the main entities in the database

Entity 1	Entity 2	Relationship type
Student	Class	an: 1
Class	Profession	an: 1
Forum message	Leave a feedback	1: an
Student	Forum message	1: an
Student	leave a feedback	1: an
Student	Q & A	1: an
System users	Operating	1: an
Test questions	Chapter	an: 1
Test questions	Error	1: 1

Based on the above analysis, the software flow is designed as follows:

1) Connect the system database with the system hardware;
2) Check whether the hardware connection is successful. If successful, access the relevant information. If unsuccessful, send an error report and return to the login page;

3) Through the output - Edit - Review - modify - delete and other steps to complete the software operation.

The structure of class table is shown in Table 2.

Table 2. Class table structure

Serial number	Field name	Types of	length	meaning
1	Classid	Integer	256	Welder id
2	Institutename	Character type	30	College name
3	Majorname	Character type	30	Professional title
4	Classcode	Character type	8	Class number
5	Classname	Character type	20	Class name

According to the above process, the data is stored to complete the research on the online interactive teaching system of sports dance based on the intelligent terminal.

4   Experimental Comparison

In order to verify the effectiveness of the design of Sports Dance online interactive teaching system based on intelligent terminal, experimental analysis is carried out, and in order to ensure the preciseness of the experiment, the performance of this research system is compared with the traditional system.

4.1   Comparison of System Storage Capacity

The storage capacity comparison between the online interactive teaching system of sports dance based on intelligent terminal and the traditional system is shown in Fig. 4.

Analyzing Fig. 4, we can see that in the first phase of testing, the data storage capacity of the research system is similar to that of the traditional system. The data storage capacity of the research system is on the rise throughout the entire time period, and the data storage capacity is relatively high. The overall data storage capacity is higher than that of the traditional system. It can be proved that this research can achieve the system design goal in data storage capacity, and there is no storage slack, and the storage capacity is superior.
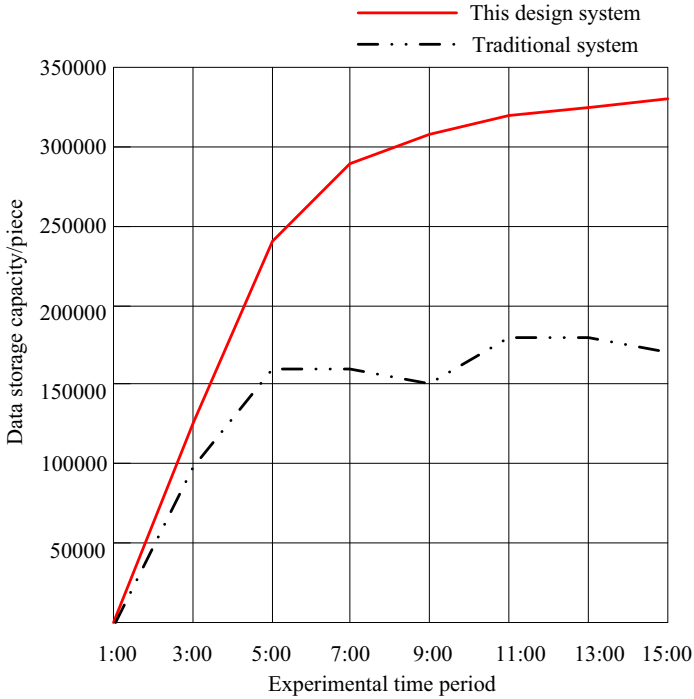
Fig. 4. System storage capacity comparison

4.2 Comparison of Response Time of Different Requests

Compare the response time of this research system and the traditional system under different requests. The main test contents include the response time of teacher assignment, user login operation, online classroom operation and homework operation. The comparison results are shown in Fig. 5.

Analyzing Fig. 5, we can see that the transmission rate of different systems is different under different user operations. By comparison, it can be seen that the response time of the four operations of this research system is relatively short, and it can respond to user operations in a short time. However, the traditional system has a longer response time in user login operation time response, online classroom operation time response, and homework exercise operation, and the response time is much longer than this research system.
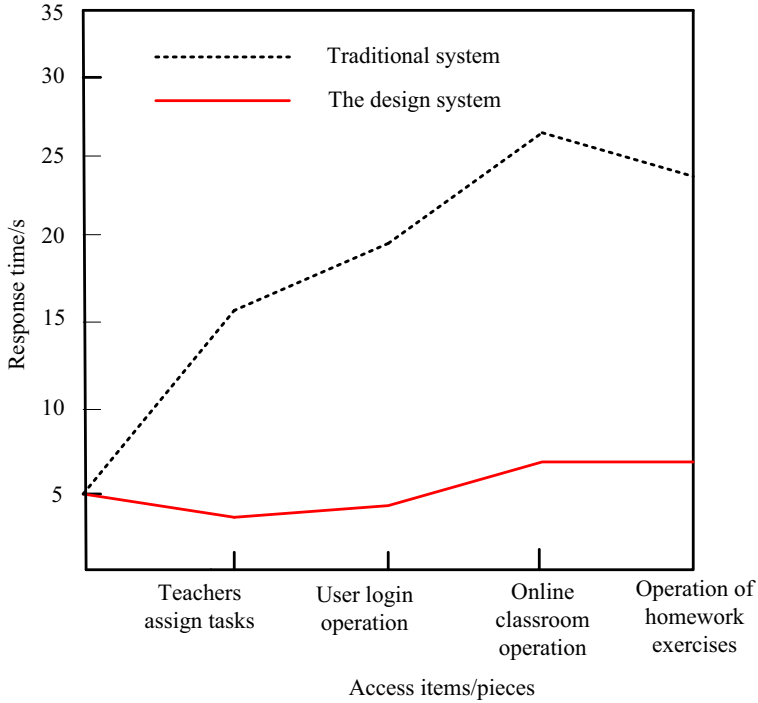
Fig. 5. Comparison of response time of different requests

4.3   Comparison of the Maximum Number of Concurrent Systems

Figure 6 shows the comparison result of the maximum concurrency between the research system and the traditional system.

Analyzing Fig. 6 we can see that when the number of concurrent data of the research system and the traditional system accomplish the same goal, the system time shows a gradual upward trend. Careful analysis shows that the research system takes less time than traditional systems to complete the maximum concurrency.
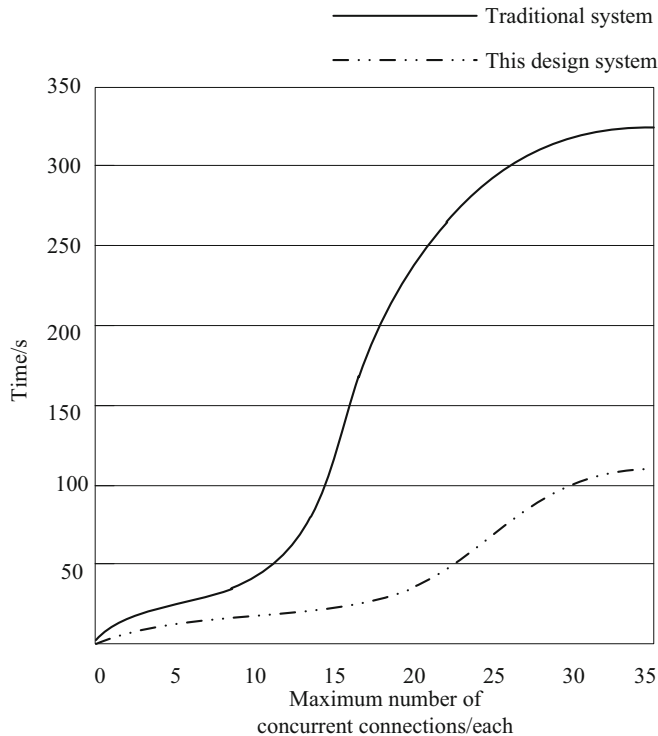
Fig. 6. Comparison of the maximum number of concurrent systems

5   Conclusion

This study designed an online interactive teaching system of sports dance based on intelligent terminal. The functions of the system include user login and authentication, information management, course management and database design. This system can not only realize the sharing of teaching resources, but also create network courses. The system reduces the limitation of communication between teachers and students, students can ask questions on the message board, teachers reply students can check, the design of other network classroom teaching software development system is also of reference significance. However, due to the limitation of research time, the system still has some deficiencies. In the following research, the system will be further optimized from the perspective of teaching resource oriented mining.

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