

Chapter 50

CPU-Based FPGA Algorithm Model of Fiber Optic Current Sensor Demodulator



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Abstract There is a far distance between computer simulation and hardware implementation of fast inline processing algorithms. This gets even harder when applying such an advanced technology as FPGA, with its benefits of speed and reliability but also caveats like unfamiliar development approaches, integer math and even hours of compilation time. We managed to bypass the complexity of tools by using LabVIEW FPGA and National Instruments hardware platform to rapidly implement control and demodulation functionality into a mock-up of a Fiber Optic Current Sensor. It was a great leap to get an alpha-prototype working in the lab with its parameters exceeding the best industry solutions. However, this implementation needed a plenty of work ahead to implement our ideas, debug and polish algorithms and ensure reliability. And that was the point where we got stuck with minor changes in the code and then hours of compilation to find out that we did wrong. Due to the rapidness of the process in fiber-optic scheme no other implementation could handle real-time processing so we were ought to put up with the delays. Finally, we convinced that this was the dead end. So, we put our efforts to create a reliable simulation model of the optical scheme of current sensor with the same LabVIEW tools. Succeeding in it, we applied our FPGA integer and fixed-point math to the desktop environment. This worked simply great, so we were able to run plenty of experiments, making changes and trying new ideas in real time in the form, that could be seamlessly moved to hardware FPGA-based platform. The article discloses several of our experiment results with the computer simulation correlated to the real-world measurements acquired with the mock-up.

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50.1 Introduction

Several years of sequential research [1, 2] in fiber-optic current sensing (FOCS) technology performed by authors resulted in functional lab mock-up of FOCS design. This mock-up implemented several new ideas, approaches and algorithms, and showed the remarkable measurement accuracy in different environment conditions.

We have made several improvements to a well-known scheme [3] replacing a piezoceramic modulator with an electrooptic one. This allowed to vary the modulation frequency flexibly, even moving to ten times higher frequencies, and exposed a much wider dynamic range than a resonance-based piezoceramic modulator. Moreover, we could apply modulation frequencies equal to power of 2, that required much fewer FPGA resources for inline processing. Moving to higher frequency disclosed an additional economical effect. The higher the modulation frequency is, the shorter delay line is required for operation [4]. This line is represented with hundreds of meters (in its legacy implementation about a kilometer) of expensive bow-tie optical fiber. With a reciprocal length to frequency dependency a 10 times higher frequency of modulation requires a 10 times shorter delay line, resulting 10 times savings on this costly component.

In brief the FOCS scheme being researched functions as following: light radiation from source propagates through the fiber-optic coupler, polarizer and phase modulator oriented 45° to the polarizer [5]. The output represented with two orthogonal modes passes through a bow-tie fiber delay line to a quarter-wave fiber plate turning into circularly polarized and then to a magnetic field sensitive part made of spun fiber. At the end, the light reflects at the mirror and propagates backwards with an opposite polarization direction and returns to a photosensor interfering with the onward wave [6–8].

The enabling element of implemented optical scheme is a fiber quarter-wave plate, that transforms orthogonally polarized modes into circularly polarized ones and vice versa. This plate is a noticeably short (about 1–2 mm depending on the fiber used) piece of fiber, that is extremely sensitive on length errors, bending and environment temperature. We have made our efforts to engineer a method of making this component with accuracy enough for proper operation of overall optical scheme.

It is well-known that the accuracy and stability of operation of this scheme is strictly dependent on quarter-wave plate conditions, especially its temperature [9]. We equipped the mock-up with a thermal chamber around the plate and run several experiments with temperature control. In temperature limits between 15 and 55 °C the accuracy of electric current measurements drop achieved 5% that is unacceptable for industrial implementation. Then we implemented authors' algorithms of

temperature error compensation that reduced the error to 0,2% without any hardware improvements.

50.2 The Problem

Though the mock-up with developed compensation algorithms represented a good stability in variable temperature and current levels, we faced unexpected artifacts sometimes causing the scheme to denial of operation. It was a sudden process appearing in different circumstances which were difficult to determine intuitively. The research of the cause of this trouble appeared to be much more difficult because of hardware FPGA-based implementation of control and processing algorithms, but no other platform than FPGA could provide a nanosecond synchronization [10, 11] of modulation control and measurements with inline demodulation and error processing. With all this benefits, FPGA required a careful handling of fixed-point and integer datatypes avoiding saturation and data loss and took about two hours of compilation time on every change made to the code.

This forced us to develop an adequate computer model of the FOCS scheme to discover the limitations of algorithms in simulation instead of physical object [12]. As the mock-up software was implemented in LabVIEW programming environment the decision was made to develop a model using the same tools. It should give a possibility of re-use FPGA code with simulated signals without any significant change and then after applying new patches on it to move it back to FPGA seamlessly.

The simulation model was implemented using LabVIEW primitives basing on the Jones matrices formalism. Every subsequent element represented with its integral matrix form and merged. The model is described in detail in [13].

50.3 The Experiment

The simulation ran on 8 generation Core i7 mobile processor, with a time step of $1/2.56E6$ s (1/10 of modulation frequency selected), at a speed of approximately 3.5 s per 0.02 s of simulated process which is 1 period of 50 Hz industrial current. It is not a real time, but extremely more efficient than 2 h of FPGA code compilation. But what is the best for choosing LabVIEW for modeling is that we did move the algorithms from FPGA code to execute on host processor keeping the code “as is” with integer and fixed-point variables resolution as shown in Fig. 50.1. Unlike the compiled FPGA instance, the same code running on CPU is fully traceable, every wire data value can be monitored, plotted or saved to file.

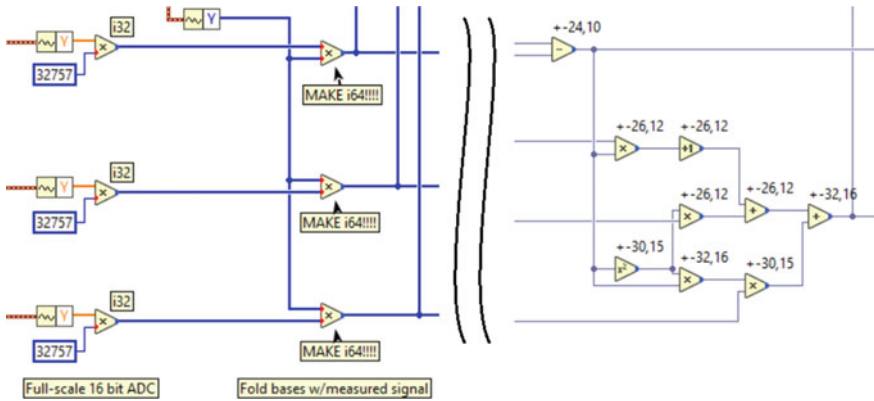


Fig. 50.1 Int32/Int64 and FXP FPGA code in simulation

The demodulation algorithm worked with simulation model exactly like we observed it to operate on physical mock-up. That was the approval of simulation model fidelity over its physical twin. We were able to run a plenty of tests, achieving the best performance over resources needed for demodulation [14, 15]. Skipping the iterative process of algorithms polishing we found out the limitations of phase signal demodulation.

A difference between two setups can be seen in Fig. 50.2: 2π current amplitude with 20% of noise and with 21% of noise in measured current signal. It is noticeable that in the first case the signal is noisy but is a sine waveform of 50 Hz. And even more, the noise is far less than 20% of signal, because of averaging in processing algorithm. Next one more percent of noise does not make the demodulated signal worse. The algorithm completely fails! There can be seen significant phase wraps that are unrecoverable with unwrap algorithm included in processing code. Injecting more noise in source signal destroys the output totally, making no sine waveform discoverable.

The behavior described above is universal for this algorithm, but the threshold of 20% noise is applicable only to the current amplitude of 2π . There should be a dependency over current vs noise to demodulation potency of algorithm.

Thus, we automated the discovery process, sending to model matrix of current amplitudes and noise percentage. The resulting SNR surface distribution and its' projection are represented in Figs. 50.3 and 50.4.

The behavior discussed above is seen on these images. There is a threshold, a limit of algorithm's robustness, where a minor disturbance makes the method all inapplicable.

The projection in Fig. 50.4 discloses the threshold trends. The higher is the measured signal, the less robust is the algorithm against noise. The future experiments sowed that at the levels below $\pi/2$ the demodulation processing recovers the signal with 100% of noise, and at above 10π amplitude the unwrapping of demodulated signal returns errors on 0.5% noise. This overall threshold line appears

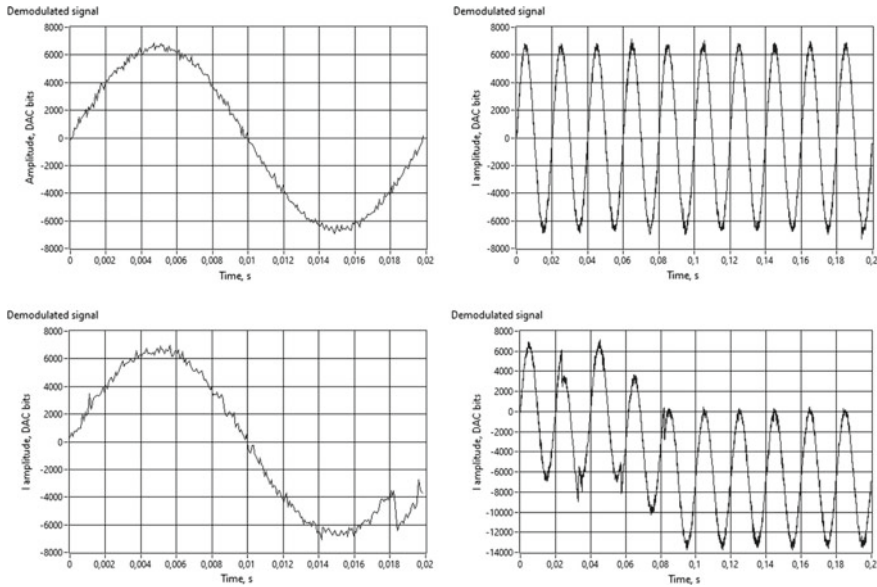


Fig. 50.2 Demodulated current signal vs time. Top left to bottom right: current signal of 6.28 radians, 20% noise 1 period, 10 periods, 21% noise 1 period, 10 periods

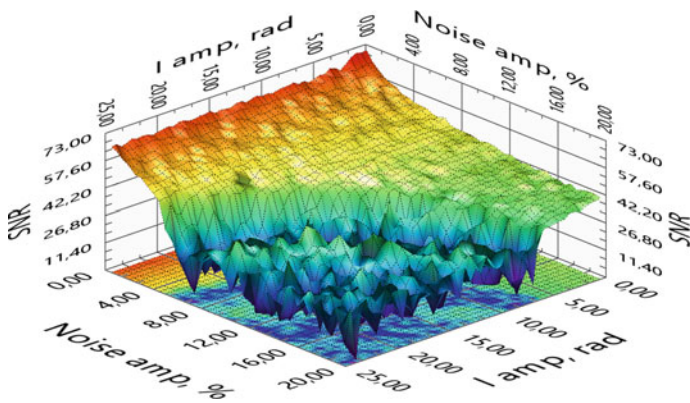


Fig. 50.3 Measured signal SNR vs. signal amplitude vs. source signal noise

a logarithmic graph with approximately 32 rad of X axis intersection and, in theory, asymptotically approaching Y axis, which is limited in real setup with ADC LSB value. Fortunately, in real-world operation the higher the current signal is, the lower noise percentage it contains. And the tolerance of the algorithm growth as the signal lowers.

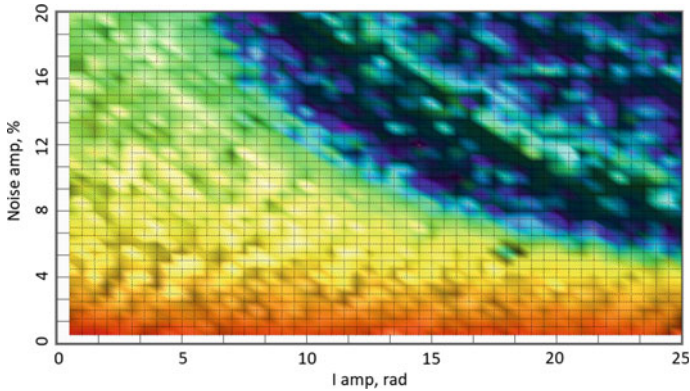


Fig. 50.4 Signal amplitude vs noise % accuracy distribution

50.4 Conclusions

The research on the FPGA algorithm of signal processing for Fiber-Optic Current Sensor made a great impact on future research. The caveats and limitations are now visible, so they can be avoidable. Similarly, the perfect operation conditions with the widest dynamic range and best stability are now easily determinable to achieve best accuracy and robustness of FOCS for industry.

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