Electrothermal Characterization of Double-Sided Cooling Si Power Module

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Abstract This paper presents an electrothermal characterization of a prototype double-sided cooling power module. The junction temperature T_j is an important parameter of power devices. Different methods exist for junction temperature measurement. In this work, an electrical method based on temperature sensitive electrical parameter (TSEP) is conducted to estimate the junction temperature of the power module. A 3D thermal model was built to better comprehend thermal behavior within the module. A comparison between simulation and measurement results is performed and analyzed. Results have shown that 3D numerical modeling help understanding several manufacturing defects (soldering, sintering, die defaults, etc.).

1 Introduction

Nowadays, most applications like electric drive transportation require higher and higher power densities and efficiency for power electronics. In the case of power modules, there is a trend towards higher switching frequencies and power levels, while decreasing the total volume. The increased power densities demand an

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improved thermal management of power modules. By the way, the junction temperature (T_j) has a large impact on performance and reliability of power devices. This parameter is really important for thermal characterizations (thermal resistance R_{th} and thermal impedance Z_{th}) or for offline/online monitoring of power modules. Optical, physical contact or electrical methods are several technical solutions to measure the temperature of power modules [1, 2].

Optical methods, such as IR camera, photo-luminescence, Raman effect, thermo-reflectance, and refraction index, require direct visual access of power chips [2–4]. In most cases, these measurement methods are not used.

Physical contact methods, e.g., thermocouple, scanning thermal microscopy, liquid crystals, or optical fibers [5, 6], not only need to have physical access to the module, but also might be intrusive.

Electrical methods allow us to have an indirect estimation of the junction temperature without having access inside the power module. However, a drawback of this method is that the measured temperature is only an average temperature of the die. Some electrical methods give the possibility of online temperature measurement monitoring of transistors. For example, if the converter encountered a problem, an immediate temperature measurement would give an indication about the relationship between the fault and the junction temperature. These methods might be employed, for example, in aeronautical and automotive applications for fault detection.

Hence, electrical methods are based on the temperature dependence of electrical parameters (voltage, current) of power devices. By measuring the temperature sensitive electrical parameter (TSEP) and using a known temperature dependence of this parameter, the junction temperature can be estimated. Different TSEPs are investigated for temperature measurements of Si devices [1, 2]. The forward voltage V_F of a diode under low current (10–100 mA) is widely used to measure junction temperature [7]. For IGBTs temperature measurement, different TSEPs can be used: saturation voltage V_{CESAT}, threshold voltage V_{TH}, gate-emitter voltage V_{GE}, saturation current I_{SAT}, or gate current I_G [4].

The content of this work consists in applying an electrothermal characterization applied to a prototype double-sided cooling Si power module. One of the goals is to be able to identify manufacturing defects by means of numerical modeling performed by 6SigmaET software. In the first part, the prototype power module is presented (physical and numerical modeling). Then, a non-intrusive T_j measurement method and its associated test bench are detailed. Experimental and numerical results about junction temperature and thermal resistance are compared and discussed.

2 Wire-Bondless, Double-Sided Cooling Power Module

2.1 Overview of the Power Module

The device under test (DUT) used in this work is a double-sided cooling power module.

As already demonstrated by many authors, cooling power modules on both sides of the active switching devices reduce the operational junction temperature compared to conventional single-sided cooling [8]. The outstanding facts are the increased current carrying capabilities by 100–200% and an improvement around 50% of the equivalent thermal resistance by using double-sided cooling embedded Si power packages.

The DUT is a Si IGBT/Diode power module (600 V–400 A) designed by aPSI^{3D} and IRT Saint-Exupery. It is composed of both upper and lower switches. Each switch includes a Si IGBT and an anti-parallel Si diode (see Fig. 1b). As one can see in Fig. 1a, gate driver connections are implemented within the module. The module plastic case is designed so that numerous modules can be mechanically connected in series.

Instead of using conventional wire-bonding, copper bumps are used to interconnect the dice. This technology will help reduce parasite inductances within the

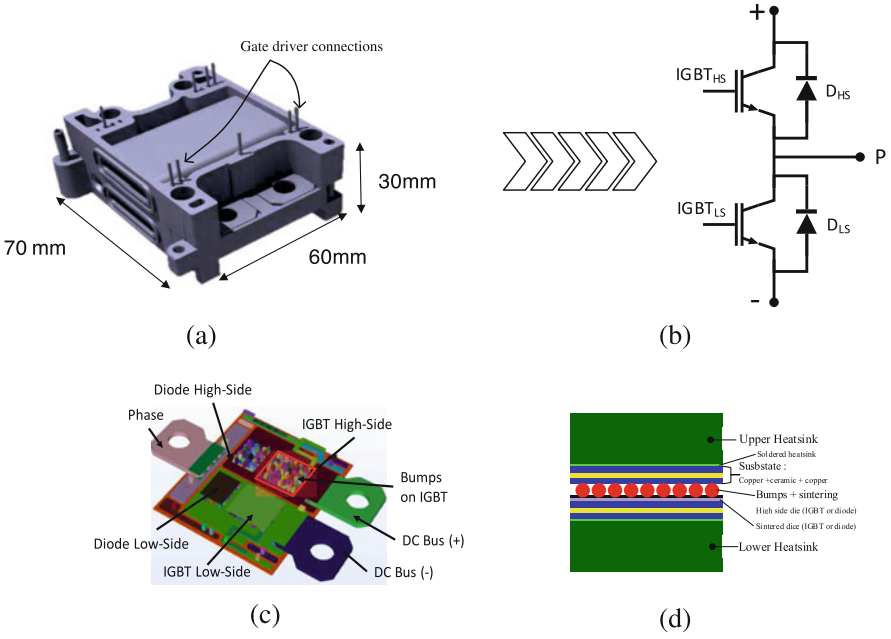


Fig. 1 DUT: double-sided cooling Si IGBT/diodes power module. (**a**) 3D view. (**b**) Electrical circuit. (**c**) Inside. (**d**) Cross section die assembly

module. The upper switch dice are directly mounted on the lower Active Metal Brazed (AMB) substrate. The front side of these dies is connected to the upper AMB substrate through copper bumps. Inversely, the lower switch dice are mounted directly on the upper AMB substrate and connected through copper bumps to the lower AMB substrate. These interconnections within the power module are presented in Fig. 1c, d. Hence, the first advantage of this wire-bondless module is that a double-sided cooling can be performed. The second one is to reduce parasitic inductance within the module by eliminating wire-bonding. Other simulations and measurement showed good values of module inductances (under 8 nH) [9].

Afterwards, an optimized heatsink, leads reducing the pressure losses and increasing the thermal capability at constant flow rate, are soldered on both sides of the power module. Several geometry parameters were optimized, such as base plate thickness, cooling fin shape, heatsink position, and symmetry. To illustrate these facts, computational fluid dynamics (CFD) simulations and experimental tests were performed to optimize the pressure losses of the heatsink (test bench presented in Sect. 4). Figure 2 shows that the optimized heatsinks allow lower pressure losses compared to classical solutions (heatsink cooling fins) at several water cooling temperatures. The gain gap between 0 and 60 °C is due to the liquid cooling viscosity, which decreases with increasing temperature.

The whole module is packaged inside a plastic case which allows liquid cooling.

2.2 Numerical Modeling

A numerical modeling, performed by 6SigmaET software, was set up to analyze the thermo-fluidic behavior of the Si IGBT power modules. 6SigmaET is really suitable for electronics applications and it brings a good compromise between accuracy and quick simulations. The whole power module is covered in our simulations (packaging, substrate, die, bumps, etc.). More than 700 elements were included. A regular unstructured meshing was implemented, finer for smaller dimensions, including 31 millions of cells.

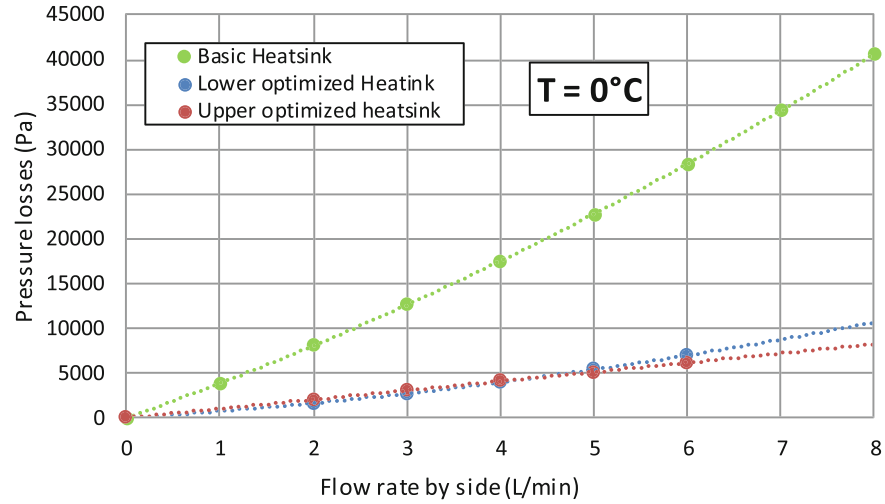
Thermo-fluidic coupling was taken into account by means of a simplified model (wall laws, turbulence model k–ε, etc.). Coolant was used as a cooling fluid in double-sided cooling configurations.

All simulations are treated by an Eulerian approach in stationary steady-state [10], with a k–ε turbulence model at constant density [11].

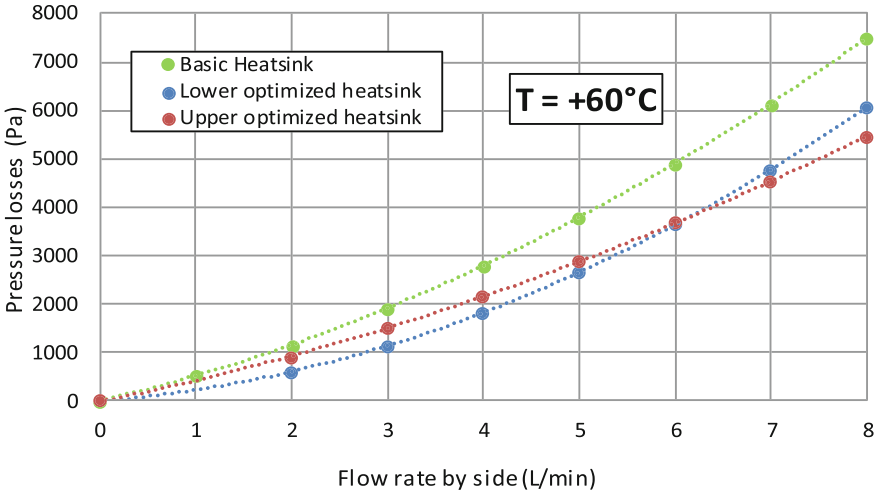
The turbulent kinetic energy k [$m^2\,s^{-2}$] is mainly carried by large structures, with any interaction of fluid viscosity: formation vortices.

The dissipation ε [$m^2\,s^{-3}$] is mainly due to the small structures, which are destroyed by the fluid viscosity effect, corresponding to speed of large vortices destruction.

Eulerian phase around the module at T_a was carried out in the air environment. The T_j was evaluated by volume average temperature of the die. Table 1 summarizes fluid and simulation parameters.



(a)



(b)

Fig. 2 Experimental results of pressure drop at different fluid temperature. (**a**) At 0 °C. (**b**) At 60 °C

Figure 3 shows several surface temperature fields of the power module for biased high side Si IGBT. Three fluidic configurations were taken into account: double side cooling, upper or lower single side cooling. During double side cooling, a vertical distribution of the heat flow is clearly illustrated. Heat extraction is around

Table 1 Simulation parameters (fluidic and electric considerations)

Parameters	Values
Fluid temperature T_{fluid}	65 °C
Ambient temperature T_a	20 °C
Fluid density ρ_f	1045 kg/m^3
Fluid dynamic viscosity	1.4 mPa s
Thermal conductivity λ	0.42 W/m K
Flow rate $\dot{m}$	6 L/min
Dissipated power by die P	100 W

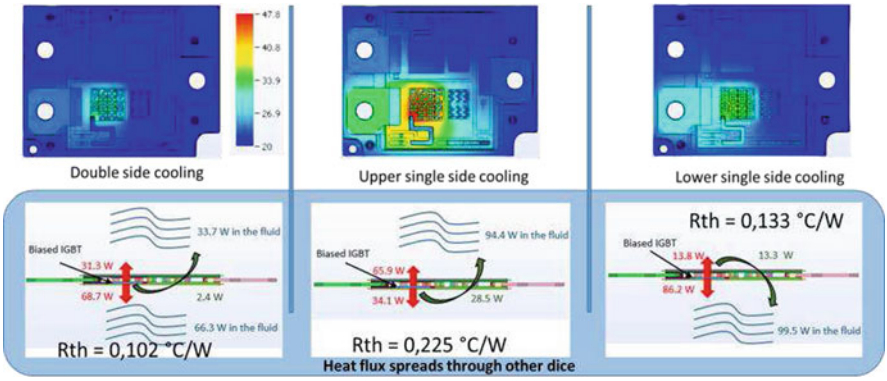


Fig. 3 Surface temperature fields of the power module for biased high side Si IGBT

2/3 through the die back side and 1/3 through the front side by means of copper bumps.

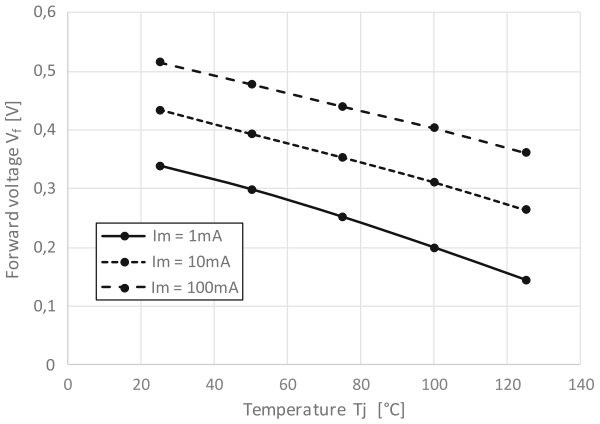
Heat extraction is more efficient through the back-side joint than through the bumps on the front side of the die. Based on a surface average temperature, the thermal resistance was estimated at 0.102 K/W.

A comparison between simulations and experimental results concerning equivalent thermal resistance is presented in Sect. 4.

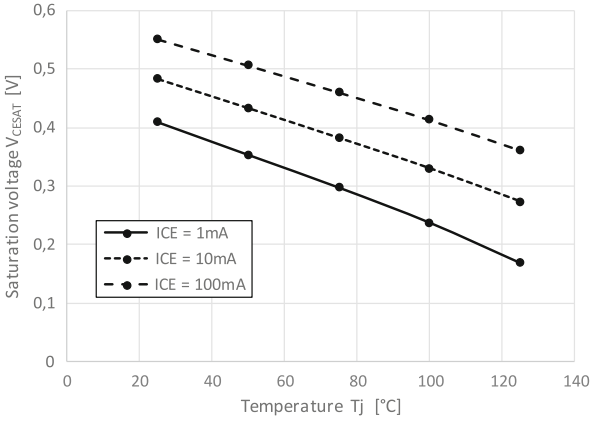
3 Non-intrusive T_j Measurement

3.1 Principle

As presented above, several methods are known to measure the junction temperature of power modules. In our study, an electrical method using a TSEP was chosen and applied to IGBT/diode half bridge (forward voltage V_F and saturation voltage V_{CESAT}, respectively, to the diode and the IGBT). The TSEP is used to indirectly estimate junction temperature of the power module and to benefit from a precise and linear thermometric parameter (around −2 mV/°C), an easy implementation of



(a)



(b)

Fig. 4 Law of variation between the TSEP and the temperature under a weak current. (**a**) $V_f = f(T°)$. (**b**) $Vce = f(T°)$

the simple measurement as well as a calibration. It was shown [12] that estimated temperatures with V_F or V_{CESAT} are close to average junction temperatures of the power module.

Basically, there are two different steps. The first step, which is a calibration step, consists in establishing a law of variation between the TSEP and the temperature at low current (below 100 mA) of excitation, in order not to produce conduction losses. Figure 4 shows the TSEP evolution under DC-biased current while power modules are located inside a controlled oven.

Once the TSEP evolution at low current is reached, an electrical method is carried out. Figure 5 shows its measurement principle. It consists in injecting a power current (I_P) flowing through the DUT until it reaches the thermal steady-state. Power current is then replaced by measurement current I_m used in previous calibrations (see Fig. 4). Cooling curve of the DUT is recorded through voltage

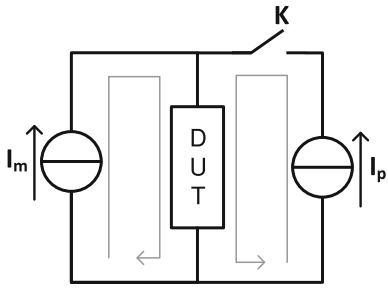


Fig. 5 Schematic of the junction temperature measurement method

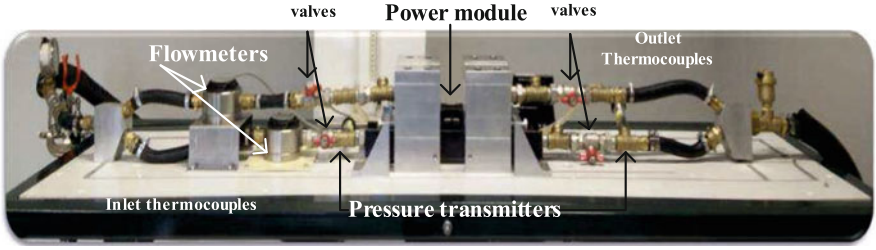


Fig. 6 Overview of the hydraulic system

drop variations. The initial temperature T_{j0} at the end of power current injection is then calculated using square root time based extrapolation on the linear part of the cooling curve. Authors in [13] showed that the strong dynamics observed during short times (close to 40 µs) do not correspond to a thermal response but correspond to electrical effects due to parasitic capacitive and inductive elements of the measuring circuit.

Therefore, the estimated junction temperature allows us to calculate the average thermal resistance of the DUT:

$$R_{th} = \frac{T_j - T_{amb}}{P}. \tag{1}$$

In this formula, P is the power absorbed by the DUT, corresponding to the conduction losses and T_{amb} is the inlet coolant temperature.

The method described and its associated test bench (see Sect. 3.2) shall be extended to a transient thermal impedance measurement, based on pulsed heating curve technique [14].

3.2 Test Bench

In order to estimate the thermal resistance, a complete electrothermal fluidic bench was developed, as shown in Fig. 6.

3.2.1 Hydraulic Parts

The coolant circuit is divided into two parallel channels in order to supply the coolant to both faces of the module. DUT is located in the middle of the coolant circuit. A cryostat is used in order to control the coolant temperature. Several valves are located in the upper and lower coolant circuit to regulate the flow rate.

In addition, different measurements are provided at the inlet and the outlet of each module:

- Two volumetric flowmeters (MACNAUGH, model MX12, accuracy of $\pm 0.5\%$, repeatability $< 0.03\%$) are used to measure the coolant flow rate flowing into each module face. The measuring range is between 1 and 16 L/min, for coolant temperature from -30 to $+90\,^{\circ}\mathrm{C}$.
- Four high accuracy pressure transmitters (WIKA, S20, accuracy of ± 1.25 mbar). It allows us to measure the pressure drop of each module side, in the range of coolant flow rate from 1 to 8 L/min, for temperatures from -20 to $+80\,^{\circ}\mathrm{C}$.
- Four type T thermocouples (accuracy of $\pm 0.5\,^{\circ}\mathrm{C}$), in the widest operating temperature range: -30 to $+90\,^{\circ}\mathrm{C}$. They quantify the impact of the module heating on the coolant temperature. Other thermocouples of type K (accuracy of $\pm 1\,^{\circ}\mathrm{C}$) are used to measure, respectively, the reference outside ambient temperature, the power terminal, and the casing surface module.

Several studies have been conducted to validate the very low pressure losses of the cooling circuit and the DUT [9] by means of experimental and CFD simulations.

3.2.2 Electric Parts

Figure 7 shows the electrical circuit of the I_m and I_p currents control.

High current pulses I_P are created by storing energy in an inductor (L). Two MOSFET transistors (T1 and T2) are used to drive the current into the DUT. The injected power current is measured using a current probe with a large bandwidth. A TSEP current (I_M), adjusted by a low current source, is injected permanently into the DUT and checked by using a shunt resistor (R_m). The Schottky diode

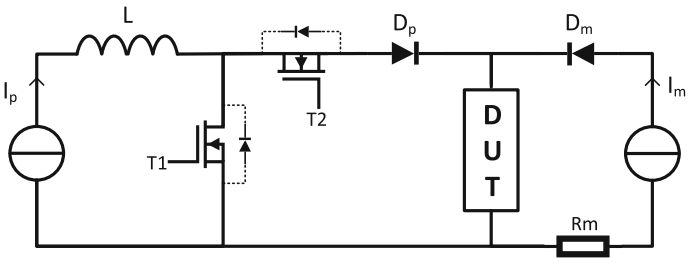


Fig. 7 Electrical current switcher

D_p prevents the current I_M from passing through the MOS2 body diode and MOS1 during the indirect junction temperature measurement of the DUT by voltage acquisition under low current. The diode D_m prevents from the influence of current I_P on the I_M current source. In our case, the current I_M is set to 10 mA, which is low enough to avoid self-heating during the temperature measurements and high enough to get a good sensitivity on the whole temperature range from 0 °C up to 150 °C, as shown in Fig. 4.

4 Experimental and Numerical Results: Comparison of Thermal Resistance R_{th}

In this section, the thermal resistance R_{th} of the power module IGBT is measured under certain conditions:

- Liquid temperature: (20 °C)
- Flow rate: 6 L/min/channel
- Dissipated power 65 W up to 160 W
- cooling configurations: double-sided cooling, single high-sided cooling, single low-sided cooling
- DC-biased current I_M: 10 mA

Figure 8 demonstrates the evolution of junction temperature of high side IGBT under varying dissipated power and different types of cooling. The junction temperature increases linearly with the dissipated power of the die.

Figure 9 shows that thermal resistance of high side IGBT is invariant with different dissipated power. It is evident that double-sided cooling results have a lowest thermal resistance. Thermal resistance of the IGBT under single low sided

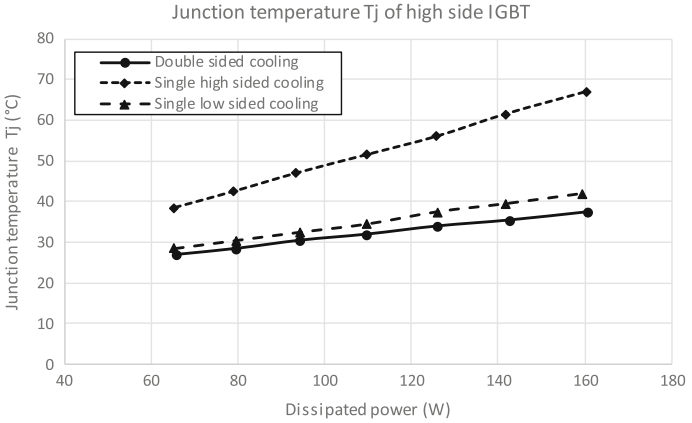


Fig. 8 Variation of junction temperature of high side IGBT with varying dissipated power

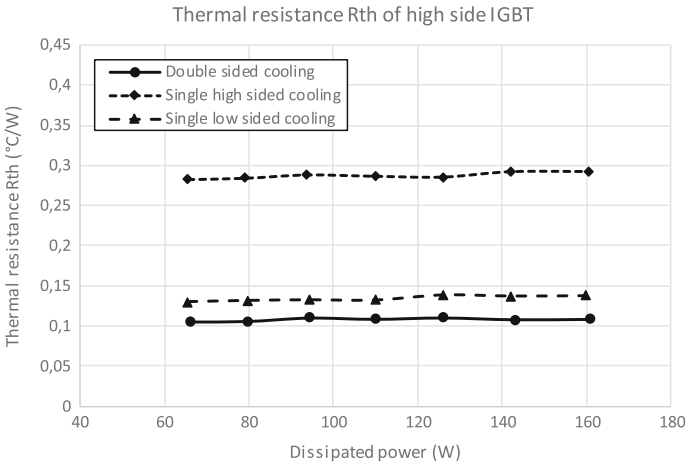


Fig. 9 Thermal resistance of high side IGBT with varying dissipated power

Table 2 Simulated and measured thermal resistance R_{th} of the power module's IGBT under double and single-sided cooling

Cooling	Simulation	Measurement	Difference
Double-sided cooling	0.106	0.108	2%
Single high-sided cooling	0.220	0.288	31%
Single low-sided cooling	0.130	0.134	3%

cooling (heat transfers through under side of the die) is much lower than the one under single high-sided cooling.

Table 2 summarizes measured (average value) and simulated thermal resistances of the IGBT and the relative difference between these values.

As mentioned, under double-sided cooling, the measured thermal resistance is very close to the simulated one (only 2% difference). The measured and simulated thermal resistances under single low sided cooling (heat is cooled through back side of the die) are also only 3% difference. However, the measured thermal resistance under single high-sided cooling is 31% higher than the simulated one. This means the heat transfer through front sides (and so through copper bumps) is not as good as expected on the basis of the numerical results.

5 Conclusions

An electrothermal characterization of a double-sided cooling Si power module using an electrical method is presented in this paper. In addition, a numerical model helps to have a thermal performance reference for the power module. Experimental results show good thermal performance of the power module under double-sided cooling

and single back-sided cooling. However, a difference of 30% is found between experimental and simulated thermal resistance under single front-sided cooling. It is important to notice that the value of the thermal resistance under single-sided cooling dramatically depends on the contact between the bumps and the sintering layers. The difference between computer-aided design (CAD) modeling and real module may explain such differences. Further work are being conducted in order to explain these facts and improve the assembly technology of the power module and in using MOSFET SiC technology.

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