Hardware-in-the-Loop Simulation of High-Power Modular Converters and Drives

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Abstract This paper explains several industrial cases involving the HIL simulation of MW-range drives and inverters using CPU cores with FPGAs to compute model equations. The use of HIL simulators is common today in the industry to accelerate design cycles, mitigate financial and human risks and support software updates throughout the product life cycle.

The first case presented is a 2-level inverter scheme in which increasing power specifications are met by adding parallel IGBT-modules. The second case is a multi-level motor drive with low harmonic injection on the AC-side. The third case is a modular multi-level converter in a grid application. We also discuss a new T-type inverter model that uses an industry PV-to-grid power converter.

In each case, all power system modelling was done using Simulink and SimPowerSystems in conjunction with the SSN solver from the ARTEMiS blockset in addition to code generation for CPU execution at time steps in the 20–50 μs range, with an exception for MMC models on FPGA. In all cases the firing accuracy of the IGBTs remains in the nanosecond range using time-stamping techniques and an FPGA board. In the case of the parallel 2-level inverters, there is significant difficulty regarding the small firing delays (typically <500 ns) between modules that create circulating currents. These circulating currents are rendered correctly on the HIL bench.

Also discussed in the paper are the various optimisations, solvers and methods that enable these performances.

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1 Introduction

Real-time simulation is an important part of power system and industrial drive development as it enables engineers to test system controllers in the lab before field commissioning. This helps to reduce overall costs by providing early detection of issues during the design process. After deployment, the real-time simulator continues to be used to test controller software updates before release in the laboratory, at safe power levels, without the need to maintain a real drive.

This paper presents some of the most challenging HIL simulation cases for drives and converters undertaken by Opal-RT, as of 2019. HIL simulation of these drives and converters is made possible through constant advancements in the field of multi-core CPU and FPGA technologies combined with clever algorithms and simulation methods.

2 Some Requirements for HIL Simulation of Drives

The main objective of the HIL test system is to verify the functionality of the real system in controlled laboratory conditions and at low power levels, before actual release, including software upgrades and commissioning.

In particular, the HIL test system must:

- Check the drive start-up and shutdown sequences. Models must be able to output truly null currents before the starting sequence for this to be checked correctly in HIL mode. Otherwise an error occurs and the controller goes into safe mode.
- Check the circulating currents between IGBT inverter modules in parallel configurations. Small circulating currents are normal in the real system and are due to variations in firing caused by wiring and element tolerances. The drive closely monitors these currents and shuts them down if they exceed a pre-determined level, which is an indication of system malfunction.
- The HIL system must be able to adequately reproduce the PWM inverter characteristics on a CPU-based simulator running the model within a 25–50 μs range. This is achieved using the time-stamping technique [1] and special inverter models called Time-Stamped Bridges or TSB. Direct connection of controller PWM pulses to the HIL simulator is mandatory (i.e., use of averaged models is not possible).
- These TSBs must be able to work correctly in natural rectifying mode; this is especially important for drives with Active-Front-End rectifiers.

3 Some MW Converter Topologies Simulated in HIL

3.1 Two-Level Parallel IGBT Modular Motor Drive and Active-Front-End Rectifier

This topology comes from the Rockwell PowerFlex 750-Series products for the Low-Voltage market (from 160 to 6000 kW) and is depicted in Fig. 1 This topology provides a scalable power level by using parallel 2-level IGBT modules up to 6 MW. More details can be found in [2].[1]

An OPAL-RT Hardware-In-the-loop (HIL) system was chosen to perform a wide variety of product software and hardware verification and validation during the product design phase and will be used for regression testing over the life of the product. As with any simulation, fidelity and accuracy of the simulation must adequately match the product itself to guarantee usefulness and confidence in any testing and verification. This section shows the PowerFlex 755TM Common Bus Inverter. The inverter PWM frequency is 1.33 kHz and the complete model runs at 50 μs in HIL mode. In HIL tests, close to 2000 I/Os were required in the simulator to interface and test the actual controllers in the real-time simulated drive system, with up to ten converters at any given time during operation.

IGBT modules are connected together through interphase reactance to smooth out any small difference of voltage output between the parallel inverters.

The drive controller closely monitors this current difference between the same phases of parallel inverters and puts the system in fault mode if it rises above a certain threshold.

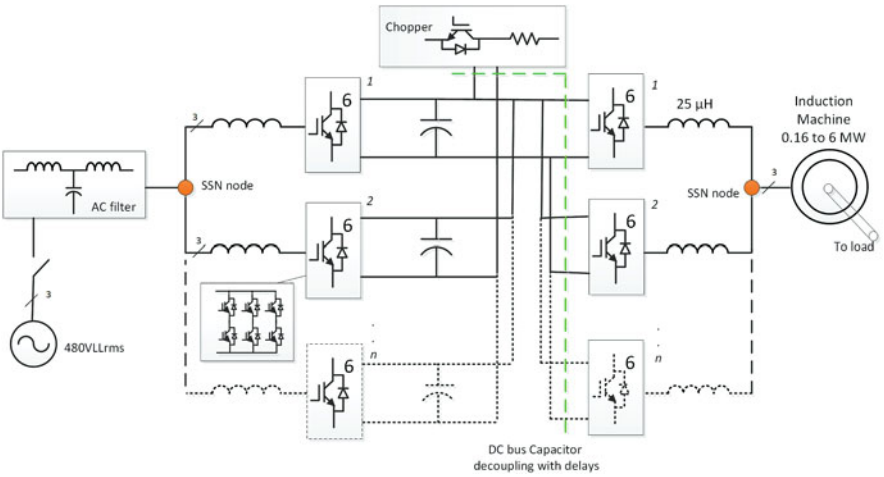


Fig. 1 Parallel 2-level IGBTs drive with AFE rectifier

[1]The authors acknowledge the re-use of some of their own verbatim of this reference.

3.1.1 Modelling Techniques

This inverter topology poses several difficulties, such as the accurate computation of inter module currents and the need for accurate current levels at low power. Furthermore, the model must be decoupled in small parts, running on different cores of the CPU to maintain the simulation time step within an acceptable range.

The system has a large DC-link, which makes the separation of the model into separate parts easier. DC-bus voltages and currents can be transmitted between separated parts with an inserted delay, with negligible errors.

The model uses modified interpolating inverter models (Time-Stamped Bridge, TSB); these inverter models are able to incorporate I/O gating signal time-stamps and to interpolate voltage outputs, resulting in very accurate simulation, mainly limited by the simulator FPGA sampling rate (in this instance, 5 ns).

Of special interest is the treatment of cases in which dead-time occurs near zero-crossing. In this case, the standard TSB model may actually output opposite voltages on different modules of the same phase.

For example, for a DC voltage of 640 V and an interphase inductance of 25 μH, the circulating current rises at the rate of $640/(2 \times 25e{-}6) \times \tau$ (for two parallel IGBT inverters), where τ is the firing delay between parallel IGBTs. For a 500 ns delay, the current would rise to about 7 A, within the controller's tolerance level.

As a simple test, we ran the model offline at 50 μs, in a simple motor start-up sequence with two parallel IGBT modules, with a high-resolution PWM modulator and variable inserted delay between the parallel IGBTs. The result is depicted in Fig. 2 and is consistent with the theory.

The requirement for null current during blocked modes, as well as accurate natural rectification modes, led us to model the diode as binary switches. This in turn caused the total number of connected diodes to be very high (60 diodes for ten parallel modules), dramatically increasing the total number of possible electric modes and permutations of state-space equations (possibly 2^{60}). By using SSN, each TSB module, containing six binary diodes each, was set into a different SSN group, solving this potential issue for real-time calculation.

Finally, the induction motor model used was an SSN, meaning that no minimum load or stabilisation snubber was required to run the model stably, even at very low power levels [3].

3.2 Multi-level Motor Drive with Low Input Harmonic

The multi-level motor drive depicted in Fig. 3 is designed to provide low harmonic AC-voltage to the load, as well as low input current harmonic to the feeding grid. This is achieved by arranging the multiple diode rectifiers with zig-zag transformers with varying phase shifts. The system runs in HIL with attached industrial controller under test at a time step of 25 μs.

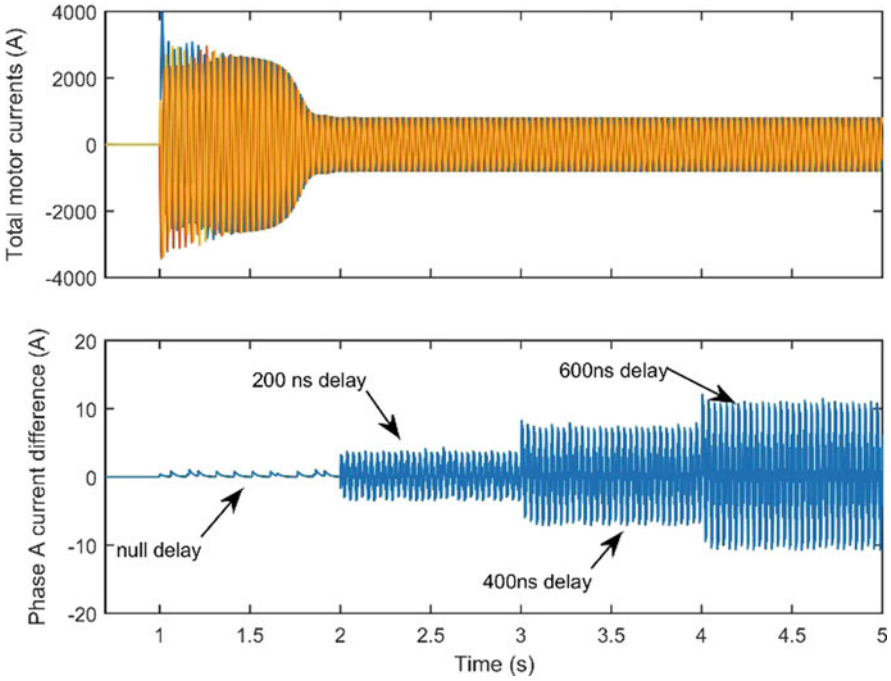


Fig. 2 Motor start-up with variable firing delay between two IGBT modules. Top: motor current; bottom: current difference between the parallel inverters

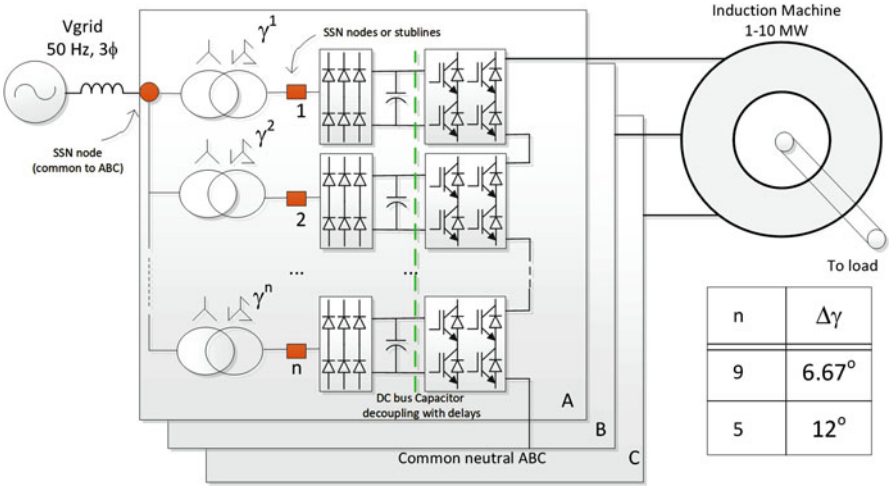


Fig. 3 Multi-level motor drive with low input harmonic

3.2.1 Modelling Techniques

This inverter topology presents several difficulties for HIL simulation. One of these is the common inductive connection of all zig-zag transformer primary windings; the SSN solver makes it possible to break down this huge state-space system of equations into several smaller ones, *without delays*. In one version of the model, where the $3 \times n$ 6-pulse rectifier (here n is the number of inverter stages) was separated using SSN nodes, SSN was also required to decouple the $3 \times n$ 6 pulse rectifiers. In the final implementation, stublines were used to provide a better decoupling at the expense of slightly lower precision.

Also, the presence of a DC-bus at each 6-pulse rectifier allowed us to simulate the rectifiers and the inverters in different cores of the simulator.

The SSN node location allows for the creation of three large SSN groups, one for each phase of zig-zag transformers, which allowed us to compute these groups on different cores.

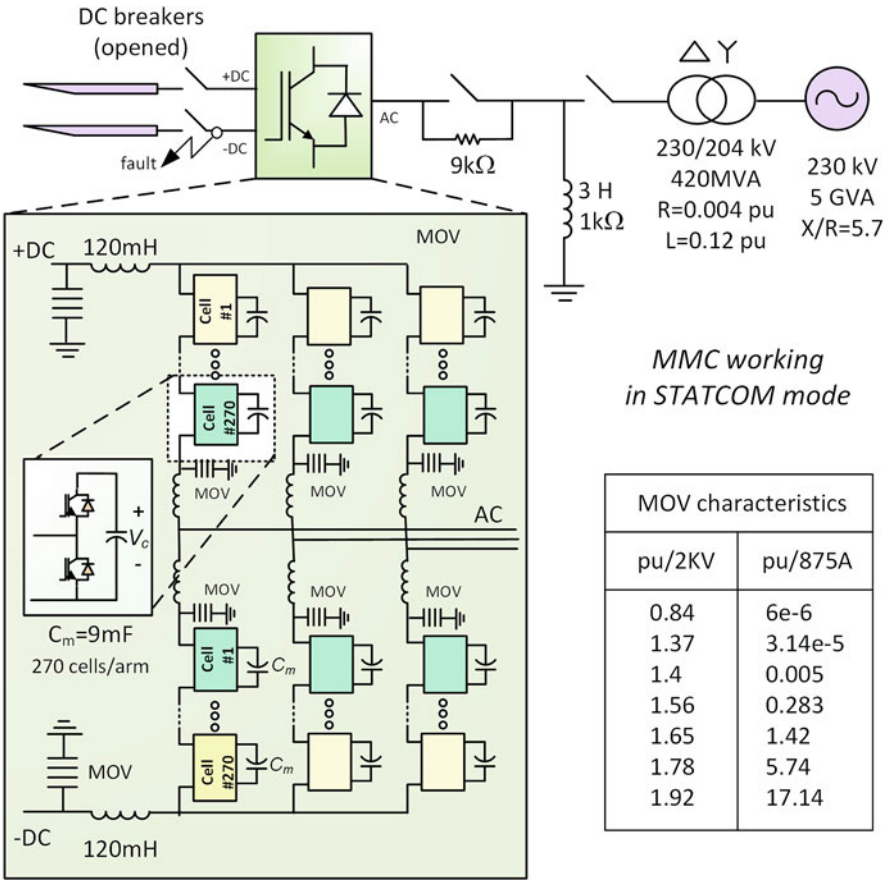
Stublines are artificial one-time-step-delay transmission lines and are used to completely decouple a circuit from one end of the stubline to the other. As they add a little capacitance to the circuit, they are less precise than SSN, which does not approximate or add delays to the simulated equations.

3.3 Multi-level Modular Converter (MMC)

Modular Multi-level Converter (MMC)-based High-Voltage Direct Current (HVDC) is a rapidly emerging technology for DC current transport and high-power converters in general. MMC, by its modular nature, has the advantage of being very reliable, easily maintainable and scalable: the inverters can continue to work correctly if a module fails, and the defective module can be replaced without completely shutting down the converter. This is an important issue with sites difficult to access, such as offshore windfarms. The converter described in this section is a 271-level MMC system in a power grid, configured for STATCOM operation, as specified for the factory acceptance test of an OPAL-RT client in the Zhoushan region of China. The MMC-STATCOM is part of a multi-terminal HVDC system and, in this case, its DC breaker is open, disconnecting the MMC station from the other stations [4, 5]. In this configuration, depicted in Fig. 4, the MMC is used as a STATCOM to stabilize the AC voltage level.

3.3.1 Modelling Techniques

To achieve HIL simulation of this MMC system with 3240 IGBTs and 1620 capacitors, the modelling approach is different from the previous cases: all IGBT switching and capacitor voltage calculations are done directly on the FPGA, and a



MOV characteristics	
pu/2KV	pu/875A
0.84	6e-6
1.37	3.14e-5
1.4	0.005
1.56	0.283
1.65	1.42
1.78	5.74
1.92	17.14

Fig. 4 MMC converter in a power grid

Thevenin equivalent is sent to the CPU for the SSN solver updates with iterative surge arresters. This model runs in HIL at a time step of 25 μs [6].

3.4 T-Type 3-Level Inverter for PV-to-Grid Converter

Among recent developments is the creation of a TSB-type model for the T-type 3-level inverter in ARTEMiS-SSN. The topology is tested in this section for a 25 kW industrial PV converter for grid, depicted in Fig. 5.

The converter's PWM switching frequency is 20 kHz. This is typical for PV inverters rated below 30 kW for residential and commercial PV applications where audible noise is not acceptable.

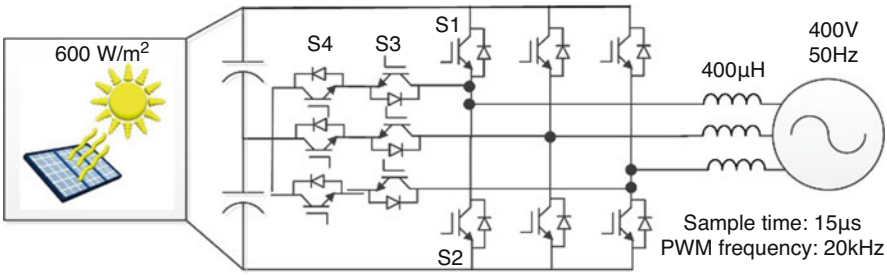


Fig. 5 T-type 3-level inverter in PV-to-grid converter

The model was simulated in a multi-rate offline model as follows: the grid and converter were simulated at 15 µs while the controller and PWM modulator were simulated at 1 µs and interfaced with the electric system using time-stamping. This time-stamping approach very closely imitates the HIL time-stamping method, described in Sect. 4.1.

This test case is one where the converter delivers 25 kW of power to the grid. Then at 0.25 s, the DC-link voltage reference is changed from 800 to 850 V. This results in a small gap in the currents; while the solar panel charges up the DC link, it does not deliver power to the grid; then at 0.26 s, the DC-link meets the commanded values and power flow to the grid is restored. The simulation result is compared with a reference model in which the entire model is run at 1 µs, depicted in Fig. 6.

The figure is zoomed in on the currents to show that the PWM component is still present in the simulation but somehow attenuated. This is normal considering the low ratio of simulation sampling frequency to PWM frequency. For $T_s = 15$ µs and $F_{PWM} = 20$ kHz, this ratio is only 3.33! Nevertheless, the current amplitudes are very accurate and free of amplitude jitter, which is sufficient to fully test the controller.

This also clears up some common confusion about TSBs: they are NOT averaged models, because the PWM component is included in the simulation. Rather, TSBs could be called 'Per time step averaging models', while standard averaged models are, by definition, 'Per fundamental period averaging models'.

4 Miscellaneous Topics

4.1 Time-Stamping Technique and Real-Time Simulators

Interpolating IGBT models are very important to obtain accurate simulation on a CPU-based computational platform. Interpolating data for power inverters is obtained by time-stamping the gate transitions on a high-frequency FPGA; logic and transition time values are then used by the interpolating model (TSB) on the

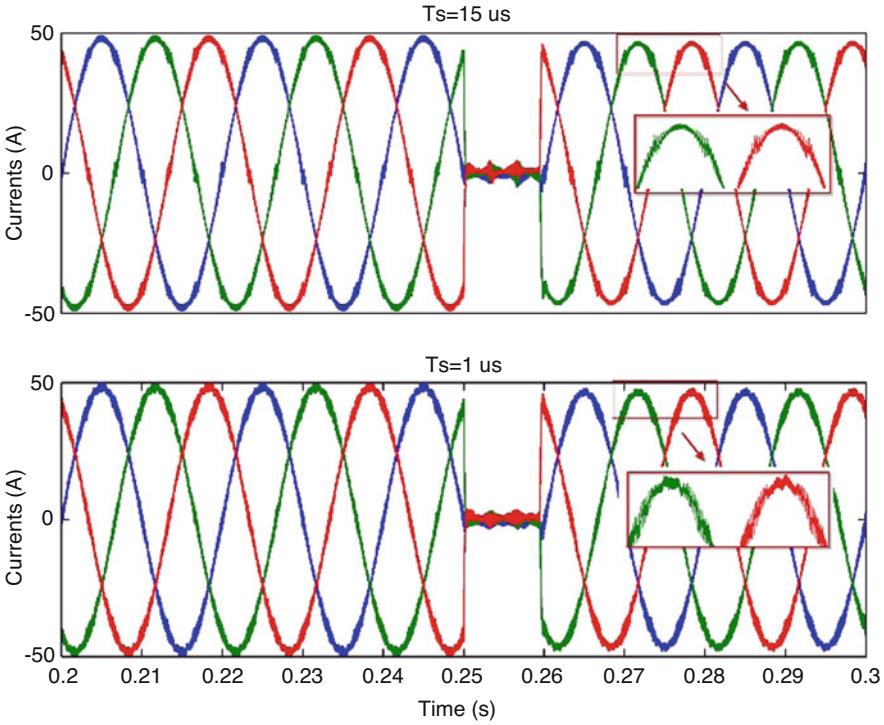


Fig. 6 Comparison of simulation at 15 μs using time-stamping method (upper) vs. reference model running at 1 μs (lower)

HIL simulator, as shown in Fig. 7 [7, 8]. A similar approach is done without I/Os by calculating the intra-step zero-crossing of PWM modulators.

In certain cases, such as MMC, some parts of the model can be computed on the FPGA.

4.2 Machine Models and SSN

All the machine models used in these models were SSN machines; that is, machine models developed using the nodal admittance method of SSN [3, 9, 10]. The main reason for this choice was to ensure stability without any parasitic loads or stabilisation snubbers at the machine terminals.

This was especially important for the Two-Level Parallel IGBT Modular Motor Drive because of the inductive connection of the motor and the interface inductor of the different modules. Standard SPS machine models use the current injection technique, which is prone to numerical instability, and is actually unstable when injected into such inductive node.

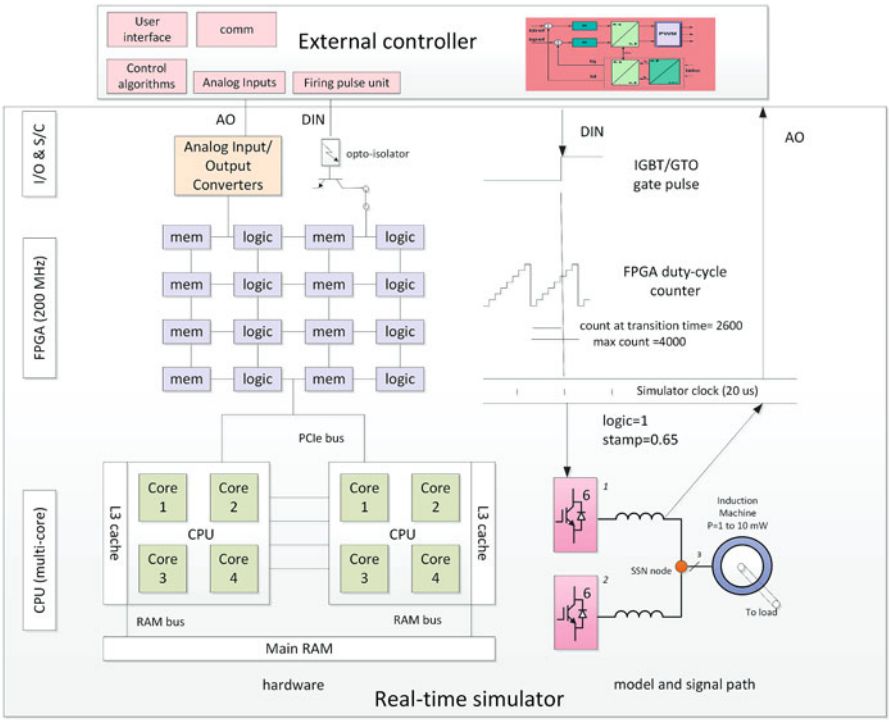


Fig. 7 RT-LAB simulator hardware structure and time-stamping

4.3 Decoupling for Power Circuits and Drives

Figure 8 summarizes the various techniques to decouple a power system or electric drive. Long transmission lines (where the transport delay is larger than the simulation time step) are the best way to decouple a power system into small parts; however this technique relates more to power systems than drives.

More common in drives and converters, DC links are also an excellent choice to decouple a drive with a delay between fractioned parts. Stublines are also a good choice when substituted for large inductor or transformer leakage inductance. As stublines are an approximation of the real circuit, this decoupling method should be validated when used.

SSN is also an excellent choice to parallelise the calculation of a grid or drive. In this case, the parallelisation is made during the calculation itself, similar to computing a 'parallel for' loop in MATLAB. For example, *SSN introduces neither approximation nor delays* into the calculation of the equations, but the parallelisation effectiveness is less than full task decoupling created by DC link delays and stublines.

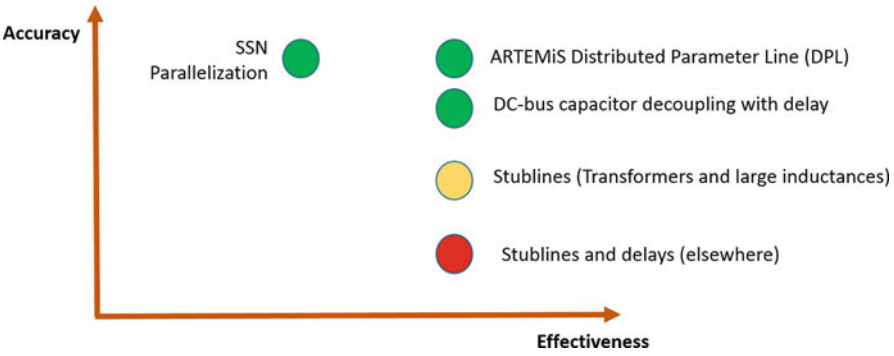


Fig. 8 Comparison of accuracy vs. effectiveness of common decoupling techniques

4.4 CPU vs. FPGA Modelling

FPGA chips can be powerful enough to compute drive equations in HIL simulators. Special advantages of FGPA include:

- Smaller time steps, which are typically under 1 μs.
- Lower input–output latency in HIL systems (considering that I/Os and models are together on the FPGA).
- A natural way to sample high-frequency PWM drives.

Recent advances in the field of electric circuit simulation on FPGA [11, 12] now enable the simulation of variable topology, variable parameter circuits, all without the need for bitstream generation, which until recently has been a powerful disincentive in FPGA technology since it can take hours to place and route (the equivalent of compiling with a CPU). Today, FPGAs are still considered as a specialist's domain with several limitations, in particular the coding of complex and flexible algorithms such as SSN. This is the main reason that CPU-based HIL simulation is still preferred today.

The best approach here is to use both technologies in a pragmatic approach: unless very low-latency (<5 μs) or PWM components are absolutely required in the simulation (e.g., resonant converters), CPUs are preferable. When the model is run on a CPU, there is a typical two-time step latency involved, caused by data transfer to and from I/Os at each time step.

The case of the MMC is particularly interesting in its pragmatism: the MMC topology is indeed better suited to FPGA simulation because of its extremely high modularity and number of devices. FPGA makes it possible to simulate this topology efficiently, using pipelining methods. It also allows for direct connectivity of thousands of I/O points. The more complex model parts of the complete MMC system, such as iterative surge arresters, are then computed on the simulator's CPU using the SSN solver.

4.5 The Case for CPU-Based High-PWM-Frequency Drives

It is worth noting that high PWM frequency is NOT always a good reason to run a model on FPGA. With the time-stamping techniques described in this paper, accuracy is excellent even at large simulation time steps. Even when the sampling frequency is close to the PWM frequency, this technique still provides good accuracy by filtering out the PWM component in the simulation. It happens that most converters are designed so that PWM components are filtered out (with some exceptions such as resonant converters); therefore this PWM filtering effect often has no impact on tests. Also, the time-stamping method has an obvious advantage over average models: in HIL mode, power electronic devices can be directly driven by the controller firing pulses.

In this paper, we have shown a good example using a 3-level T-type inverter in which the model sampling frequency was only 3.33 times higher than the PWM frequency where accuracy remains high. PWM modulation is simply a way to convert DC to AC and the PWM component is not normally tested (again, there are exceptions, such as resonant converters). So, for control testing purposes, it is often acceptable to have this PWM component damped.

The inverter used in the models of this paper are of a novel generation (called TSB-RD), a kind of hybrid between interpolated switching-functions, for the active mode (similar to older generation of TSB) and binary switches (in SimPowerSystems, these are 2-state switches with very low resistance if ON or very high resistance if OFF) for the natural rectification modes. It is worth noting that older generations of TSB, in which the rectifying modes were simulated using current-nulling feedback loops, can still be used because they are sometimes more computationally efficient than using TSB-RD with SSN. That was actually the case in the *Multi-level Motor Drive with Low Input Harmonic* (Sect. 3.2).

5 Conclusions

This paper discussed the different modelling techniques used to simulate several large motor drives and converters. All these topologies have been successfully commissioned at industrial client sites.

Here the motto of HIL simulation is ‘Make it work!’, and this motto is additionally the reason for providing all these various models, options, decoupling techniques and solvers in ARTEMiS: to meet all the demanding client objectives.

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