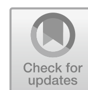
From Microelectronics to Nanoelectronics: Fifty Years of Advancements in Electronics



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Abstract Fifty years ago, when the Università Politecnica delle Marche (UnivPM) was founded, the minimum size of an electron device was about ten micrometers, today dimensions in the order of twenty nanometers can be reached by the current technologies. At that time silicon foundries were able to integrate about tens of components on a chip, after fifty years has passed, an integrated circuit (IC) might contain more than ten billion devices. As the need for increasing integrated density on chips continues and silicon technologies show their physical limits, the new era of nanotechnologies, that have the potentiality for circumventing these limits, is coming. The aim of this paper is to highlight some key aspects that determined this rapid advancement and to discuss the contributions given by UnivPM both in microelectronics and nanoelectronics during these five decades. In particular, in the context of microelectronics the paper focuses on research activity in the fields of device modeling, tolerance analysis, statistical analysis of ICs, statistical simulation and design of ICs. With regard to nanoelectronics, the recently discovered nanosize materials, such as atomic clusters, nanotubes/nanowires, and monoatomic layers, may constitute a new scalable platform for RF electronics, namely for switches, amplifiers, logic devices, frequency multipliers, rectifies, interconnects, and sensors. In this framework, the present contribution provides a view on the most recent developments in modelling and simulation of carbon based devices. Specifically, we describe rigorous multi-physics approaches for the analysis of quantum transport and electromagnetic

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S. Longhi et al. (eds.), *The First Outstanding 50 Years of "Università Politecnica delle Marche"*, https://doi.org/10.1007/978-3-030-32762-0_1

fields in nanostructured materials. In addition, we show that the low profile and size of nanomaterials make them perfect candidates as test beds for novel experiments on single electron devices and quantum transistors. Finally, the paper will give a brief excursus of the activity in progress at UnivPM, taking a look at the future development in electronics.

1 Introduction

In 1969 a paper by Y. Tarui et al. was published on IEEE Journal of Solid-State Circuits [55], that reported the analysis and characterization of a high-speed large scale integrated (LSI) memory. The memory was fabricated using n-channel enhancement metal oxide silicon (MOS) transistors that operated at a higher speed than p-channel transistors, due to higher effective carrier mobility of electrons. A photograph of the memory is reported in Fig. 1. An 114-bit (16 word $\times$ 9 bit) n-channel MOS-LSI memory was fully integrated on a chip with an area of 4.3×3.0 mm, and operated with 40-ns write cycle time.

At the same time a study on the technological reliability and performance of integrated complementary MOS (CMOS) circuits, was published on the same journal [33]. The basic building block of these circuits—the complementary pair of MOS inverter—consisted of two enhancement mode MOS transistors connected in series, with their gates connected together (Fig. 2). Due to its characteristics—very low standby power consumption, high speed, ground noise immunity—the circuit became the fundamental block of subsequent silicon technologies development.

Fifty years later (2018), in the paper [35] a system-on-chip (SoC) was presented, embedding an ARM® Cortex® $-$M0 + MCU, 2×4 SRAM, an ultra-low power frequency synthesizer, a custom power switch, and a power management enabling active and sleep modes. The device shown in Fig. 3, has been fabricated using a 28 nm fully

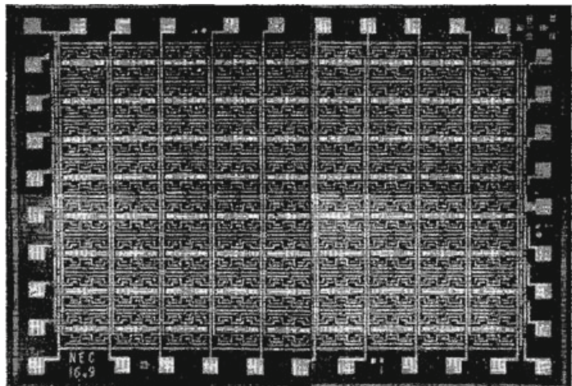

Fig. 1 The photograph of an 144-bit (16 word $\times$ 9 bit) n-channel MOS-LSI memory. The chip area is 4.3×3.0 mm [55] ©[1969] IEEE

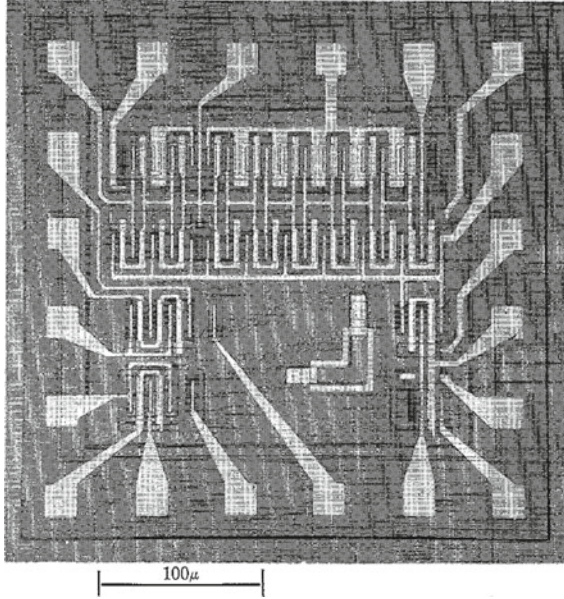

Fig. 2 Photomicrograph of the monolithic complementary pair MOS inverter test circuit [33] ©[1969] IEEE

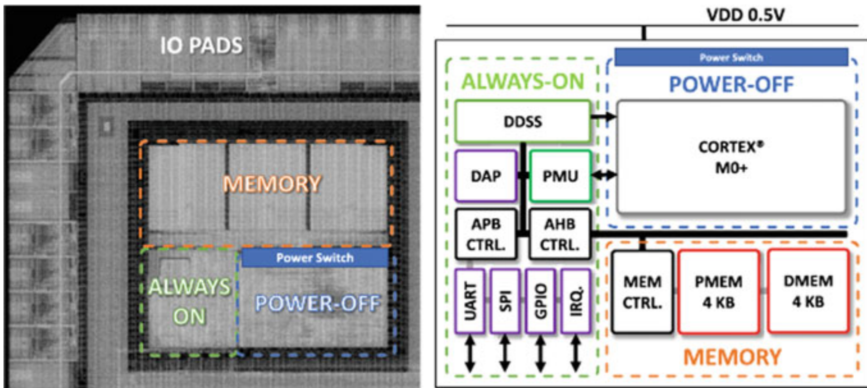

Fig. 3 28 nm FD-SOI SoC implementation and corresponding block diagram. Core area is 0.073 mm^2 [35] ©[2018] IEEE

depleted silicon-on-insulator (FD-SOI) technology, has a core area of 0.073 mm^2 and silicon measurements report an SoC's power consumption of 2.7 pJ/cycle at 16 MHz.

These three circuit examples clearly show the great advancements of silicon technology during the last fifty years. The key aspects that determined a such rapid progress are not only related to technological improvements but also to the development of design methodologies and techniques able to manage the increasing complexity of silicon circuits.

This paper is mainly addressed to this second aspect and aims to report the contributions given by UnivPM both in microelectronics and nanoelectronics during these five decades. In particular it is focused on these following subjects: (i) circuit simulation and device modeling; (ii) statistical IC design; (iii) system level and circuit design; (iv) graphene based field-effect-transistors and modelling perspective.

2 Circuit Simulation and Device Modeling

With the rapid increase of device density of integrated circuits, the development of computer aided design (CAD) techniques, became one of the key aspects in the design of large-scale (LSI) and very-large-scale (VLSI) integrated circuits. Due to their complexity, circuit simulation, that is simulation of circuit behaviour by computer, performing several analysis, i.e., DC, AC and transient analysis, was crucial for the success of CAD based design approach [50]. Circuit simulation is based on circuit analysis, that establishes general equations describing the behaviour of a circuit (f.i. modal analysis). A circuit simulator numerically computes the solutions, by using suitable algorithms, under different stimulus and initial conditions. The responses so obtained are useful to predict the real behaviour of a circuit bypassing the fabrication of samples for testing the performance, thus reducing the cost of the design. The Simulation Program with Integrated Circuit Emphasis (SPICE), written by Larry Nagel in 1972 and subsequently released as SPICE2 in 1975 [45], has been widely accepted for circuit analysis since its introduction and continues to be the framework in the more advanced circuit simulation tools.

Device modeling played a central role in VLSI circuit design because the accuracy of computer-aided circuit analysis results strongly depends on the accuracy of the device models used in the circuit simulator. As a consequence a great attention was devoted to MOS transistor modeling and a considerable effort was spent to model even smaller and more complex transistors, for several decades [68].

- A macromodel for integrated all-MOS operational amplifiers
In the eighties a great attention was devoted to fully monolithic PCM filters for telecommunication applications, and in this context the design of high-performance CMOS switched-capacitor (SC) filters was a main issue in analog ICs design. To this end a large adoption of CAD tools was required to simulate the behaviour in both the time and the frequency domain, and in particular to take into account for second-order effects such as (1) non zero resistance of the switches, (2) parasitic capacitances, (3) noise, (4) non ideal characteristics of the op amps (slew rate, settling time, gain, bandwidth, nonzero output impedance, etc.). However, as an integrated op amp was usually described at the device level and typically included about 20–40 MOS transistors, this complete description would lead to an excessive and impractical computing time for the simulation of the entire SC filter. To achieve both accurate simulations and minimum computer time, several authors [34] suggested simple linear models of the MOS op amps, taking into account only for a finite value of the

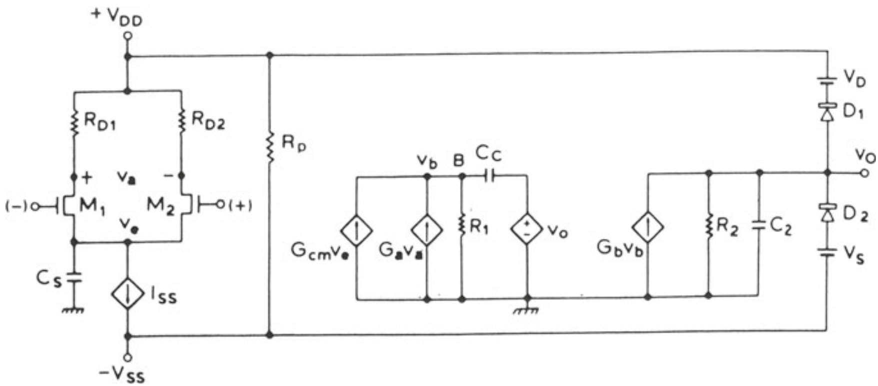

Fig. 4 The macromodel for integrated all-MOS operational amplifiers [57] ©[1983] IEEE

voltage gain, a nonzero output resistance and the presence of poles in the transfer function.

In the paper [57], C. Turchetti and G. Masetti, studied the problem of a whole and inexpensive modeling of integrated MOS op amps and presented a macromodel that met all these requirements. The macromodel, shown in Fig. 4, was able to adequately represent the main electrical performances of integrated all-MOS op amps and especially the settling time that is of particular concern for charge redistribution ICs, where only capacitive loads are considered. In the macromodel, each performance specification of the op amp is modeled separately, by a set of fifteen parameters, independently chosen each other. A large experimentation was carried out to investigate the validity of the proposed approach, with reference to the electrical characteristics of several integrated MOS op amp, available in the literature [54].

- On the small-signal behaviour of the MOS transistor in quasistatic operation

In the context of MOS analog ICs, the use of devices with aspect ratio (gate length to gate width) as large as 500–100 was often necessary to meet the performance required. In these devices the intrinsic capacitance effects can dominate the device behaviour in the frequency domain, thus requiring accurate small signal modeling to predict AC behaviour of analog circuits [43, 46, 66, 67]. However very inaccurate models were available to the designers, so that they tend to yield very conservative designs. For example, amplifiers designed with excessive stability margins, or working well above threshold (with excessive power consumption), due to the poor knowledge of capacitance effects.

The contribution of the paper by C. Turchetti, G. Masetti and Y. Tsividis [62] to this problem was twofold:

(i) it proposed a complete small-signal topology for the MOS transistor;
(ii) the small-signal capacitances and conductances in the above model were derived using a general formulation based on quasistatic assumption.

- A CAD-oriented analytical MOSFET model for high-accuracy applications
In the design of low power low voltage analog ICs there was a continuous demand for very precise and CAD-oriented MOSFET models. Although analytically models which avoid previous integral formulation [49] and able to correctly describe all the operating regimes of the device were reported [67], they were not explicitly expressed in an analytical form, thus requiring the solution of an implicit equation. The iterative procedure required for solving such an implicit equation, was the main obstacle for the implementation of those models in CAD programs.

In the paper by C. Turchetti and G. Masetti [58], an explicit formulation for the surface potential along the channel of a long-channel MOS transistor was derived, that overcomes the limitations of the previous models. On the basis of this formulation a model for the drain current which is (i) a continuous function of all the voltages applied to the device; (ii) valid in all the operating regimes of the device (weak inversion, moderate inversion and strong inversion) was established.

- Influence of diffusion current on the DC channel and AC characteristics for the Junction Field-Effect Transistor (JFET)
An advancement of analytical theory for the JFET, that usually takes into account only the drift component of the drain current, is reported in the paper by C. Turchetti and G. Masetti [60]. In this paper a precise analytical model for the JFET that includes both diffusion and drift currents, giving a natural saturation of the output characteristics, was presented. The model gives analytically an expression of the DC characteristic of a long-channel JFET valid in all the regimes of the device: linear region, pinchoff, sub-pinchoff.

- Analysis of the depletion-mode MOSFET including diffusion and drift currents
Before the development of CMOS technology, one of the main problem in obtaining high-performance circuits was the need for transistors with negative threshold. As a consequence the adoption of depletion-mode MOSFETs (DMOSFETs) in the realization of the MOS ICs was considered. However, although for the enhancement MOSFET some good physical models [56, 58, 67], valid within the framework of the gradual channel approximation scheme, were developed, for the depletion mode MOSFET the analytical models proposed until then were based on too simplified assumptions, thus leading unrealistic results [30].

The purpose of the work by C. Turchetti and G. Masetti [59] was to present an analysis of a long-channel depletion-mode MOSFET which, taking into account to both the diffusion and the drift components of the current, was able to predict the DC characteristic of the device in the linear, saturation and sub-pinchoff regimes of operation.

- A charge-sheet analysis of short-channel enhancement-mode MOSFET's
With the continuous demand for higher density ICs, a corresponding scaling of device sizes was required, thus giving rise to the so-called short-channel MOSFET devices. A detailed knowledge of the physical behaviour to determine the electrical characteristics of such devices, whose dimensions was under the micron, required

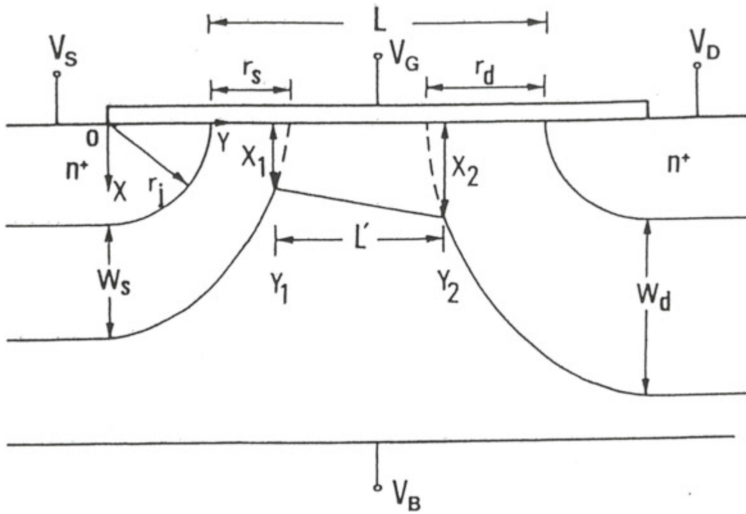

Fig. 5 Schematic cross section of a short-channel MOSFET [61] ©[1986] IEEE

the solution of two- or three- dimensional device equations, that is impractical for CAD using. This requirement was the motivation for the development of analytical and pseudo analytical short channel MOSFET models.

The purpose of paper by C. Turchetti and G. Masetti [61] was to derive a charge-sheet approach for the short channel MOSFET model, which was able to describe the device characteristics in all the operating regimes, i.e., strong inversion, weak inversion and saturation, without introducing discontinuities in the drain current and it derivatives with respect to bias voltages. With reference to the cross section of a short n-channel MOSFET shown in Fig. 5, the model was developed by coupling and solving the Poisson's equation and the continuity equation, under the charge-sheet approximation, that is assuming the free charge in the channel is concentrated in a small region close to the silicon surface [60, 67].

- A Meyer-like approach for the transient analysis of digital MOS ICs
Transient analysis of digital MOS ICs performed by simulation program such as SPICE, requires accurate modeling of intrinsic charges in a MOSFET. However one of the most widely adopted model, the so-called Meyer's model [43], did not guarantee the charge conservation in a MOSFET during transient analysis. To solve this problem the Ward's charge based model [66], that did not have this drawback, was developed. However, Ward's complete model was somewhat complex to be currently used as a standard model for the design of all MOS circuits. Besides both the Meyer and Ward models were developed under quasistatic operation, that is inadequate assumption for circuits operating at relative high speed.

The above considerations were the basic motivations for the development of a simple "Meyer-like" model presented in the paper by C. Turchetti et al. [63]. Start-

ing from the integral relationship for the gate current, after a numerical integration approach, an expression for the discretized gate current that satisfy charge conservation requirement, was derived.

- A non-quasi-static analysis of the transient behaviour of the long-channel MOS valid in all regions of operations
With the appearance of many digital, analog, and mixed digital/analog MOS ICs operating at relatively high speed, the accurate modeling of transient behaviour in MOSFET devices, became of paramount importance in the design of such circuits. In particular, the inertia in the charge transport of the carriers from source to drain and in the charge readjustment when fast turn-off or turn-on transient voltages are applied to the device terminals, were the main effects to model in such devices [46].

The purpose of the paper by P. Mancini, C. Turchetti and G. Masetti [38], was to present an analysis of the non-quasi-static behaviour of the intrinsic long-channel MOS transistor, when arbitrary voltage steps are applied to the four device terminals. The analysis was developed for a long-channel MOSFET assuming a charge-sheet formulation, thus yielding a model valid in all operating regimes of the device, i.e., strong inversion, moderate inversion, weak inversion and saturation.

3 Statistical IC Design

In the last decades, the advances in IC fabrication technology to obtain faster and more complex chips have determined a continuous reduction in the feature size of CMOS devices. As a consequence, at the decananometer geometries used in VLSI technologies, accurate modeling of statistical behavior of integrated devices has becomed essential in the design of ICs, for several reasons.

Local and global statistical fluctuations of the electrical parameters of the devices in submicron ICs severely limit the performance obtainable from both analog and digital circuits. In the design flow of high-performance ICs it is therefore of increasing importance to define statistical models that are able to predict such random variations. Thus, the research has addressed the following issues:

- Definition of a statistical MOS transistor model that links the variance and correlation of critical model parameters (BSIM3, MOS Level9) to the covariance of the process parameters affected by random variations. This model is able to predict the mismatch between devices as a function of length, width, area, orientation, and distance between devices on a chip [13].
- Definition of a methodology for estimating the statistical model parameters.
- Definition and design of test structures for evaluating both *intra-die* and *inter-die* process variations in order to (i) accurately assess the device mismatch (indispensable for the estimation of performance of more complex circuits such as digital-to-analog (D/A) converters) and take into account the effects of the geometry and the distance between the devices [17], and (ii) easily monitor the mismatch

during the production cycle with test patterns in the spaces between the dice (scribe lines) [20].

- Layout based improvement of the mismatch model in order to take into account the partitioning of the devices and their mutual positions on the chip [9, 19].
- Development and characterization of a versatile statistical model for submicron MOS transistors that allows to evaluate the effects of technological variations on circuit performance without using complex Monte Carlo simulations [25].

- Statistical IC modeling for parametric yield maximization

In order to estimate how the statistical variations of process parameters affect the circuit performance and to design ICs in such a way as to maximize the yield, the statistical analysis of electronic circuits has been studied. A methodology for carrying out the sensitivity analysis of circuit performance to the variations of device model empirical parameters has been proposed. The methodology it is based on an accurate statistical MOSFET model that takes into account the correlations between the devices as functions of device sizes and mutual distances [12, 16]. The validity of this technique has been demonstrated by implementing the mismatch model in a statistical CAD tool [18, 21]. Additionally, by modeling the mismatch of the drain current of MOSFETs, a methodology of statistical design of high performance CMOS D/A converters has been developed. The technique allows to explore different circuit architectures and to assess the effects of the layout on the performance without using standard Monte Carlo simulations [24, 26].

Finally, a technique for statistical simulation of non-linear ICs affected by device mismatch has also proposed. This simulation technique is aimed at helping designers maximize yield, since it can be orders of magnitude faster than other readily available methods, e.g. Monte Carlo. Statistical analysis is performed by modeling the electrical effects of tolerances by means of stochastic current and/or voltage sources, which depend on both device geometry and position across the die. They alter the behavior of both linear and non-linear components according to stochastic device models, which reflect the statistical properties of circuit devices up to the second order (i.e. covariance functions). DC, AC, and transient analyses are performed by means of the stochastic modified nodal analysis, using a piecewise linear stochastic technique [4, 5].

- Statistical circuit simulation

A fundamental aspect that cannot be neglected, especially in analog circuit design, is that of fabrication tolerances, that translate to parametric uncertainties in the resulting transistors. These uncertainties are usually bigger between chips produced in different fabrication lots, decrease significantly within the same lot and within the same wafer, and should be minimal for very closely spaced transistors in the same IC. Unfortunately, taking care of such uncertainties at design stage is not easy. CAD tools usually only offered a Monte Carlo simulation option, that just randomly choses the transistor model parameters within the specified tolerance range and performs a whole, and usually long, simulation for each random draw.

- SiSMA—A Tool for efficient analysis of analog CMOS integrated circuits affected by device mismatch
For many analog circuits, the dependence of the output from model parameters is not usually very strong. After all, they should be designed to be as immune as possible to these variations! With this consideration the idea of trying to linearize this dependence around the nominal solution was born. Performing a linearized simulation is much faster than performing a full nonlinear circuit simulation, and so the tool SiSMA was developed. It contains a circuit simulation engine similar to that used in SPICE for linearized simulations, but instead of sweeping the frequency of an AC source, it propagates variances from the sources of uncertainties to the circuit outputs. As shown in [1, 3], it can achieve simulation speeds orders of magnitude faster than a conventional Monte Carlo simulator.

- Piecewise linear second moment statistical simulation of ICs affected by non-linear statistical effects
Of course, most digital circuits and some analog circuits exhibit a strongly nonlinear behaviour that cannot be linearized without incurring into severe approximation errors. Yet, oftentimes a piecewise linear model can be used to better the results of a simple linear model. The tool SiSMA was hence augmented to support this additional operational mode, whereby linearization is performed across a multitude of operation points, carefully selected to allow reconstruction of the required output variances. In [5] the approach is described, and successfully applied to the simulation of the effect of the tolerances on performance indices such as propagation delay in a digital adder or harmonic distortion in an analog multiplier.

4 System Level and Circuit Design

Due to steady downscaling in CMOS device dimensions, from 2005 extremely complex systems called System-on-Chip (SoC) have been implemented. A fundamental issue has been represented by the design productivity gap: the number of available transistors grows faster than the ability to design them meaningfully and efficiently, guaranteeing a feasible time-to-market. The escalating gate count, desired system heterogeneity and trend towards increased productivity for complex SoC devices did not allowed anymore the use of traditional RTL-to-gates design methodology that was based on VHDL or VERILOG simulation. Thus, electronic system level (ESL) design methodologies have been developed on understanding the functionality of the system components, separating system design from implementation. Thus, industry has addressed SoC design by exploring the extension of an existing specification/design language, such as C/C++ or Java with hardware-oriented (memory, control, communication and synchronization) data structures.

In order to bridge the gap between technology capabilities for the implementation of SoC and electronic design automation (EDA) limitations, an environment integrating new concepts within new languages and methodologies, as well as within

a corresponding set of system-oriented EDA tools was needed. In particular these requirements had to be met:

- high degree of reuse of IP blocks, beyond the borders of intra-company reuse;
- optimal hardware and software partitioning based on a system abstraction;
- interoperability between tools from various domains, such as analog, digital, micro-electro-mechanical (MEMS) devices to support heterogeneous design;
- hardware/software co-design.

Some relevant aspects of system level design has been faced by the he research group of electronics of the Università Politecnica delle Marche aspects in the last 20 years: system level power estimation, transaction level modeling and system level modeling of heterogeneous systems.

- System level power estimation

System-level design and IP modeling is the key to fast SoC innovation with the capability to quickly try out different design alternatives, to confirm the best possible architecture, including the power consumption issue, early in the design process. At this high level of abstraction the power estimation allows:

- the evaluation of different system architectures: in this case there is not always the need for a very accurate estimation; power can be evaluated quickly if it is possible to know the design complexity and the signals activity derived by a fast functional simulation;
- the precise evaluation of the power consumption of a particular block in the system, in order to carry out accurate power values for IP qualification: in this case a low-level model of the system should be provided, often obtained through synthesis or hardware inferencing.

From 2001 the research group developed a system-level approach power estimation approach and a methodology to integrate a power model into an existing executable specification. In particular we have developed two libraries, called PKtool (Power Kernel tool) [6, 64, 65] and PowerSim [31, 32] based on SystemC 2.0, that the designer can use to efficiently create a hierarchical power model of the system under development. Particular attention has been dedicated to the definition of the user interface, the set of methods that can be used to access power functionalities; the designer only has to perform a small set of steps to integrate the power model in the system-level specification, with a very small impact on the code already written.

- Transaction level modeling

The design of complex Systems-on-Chip and multi-core systems requires the exploration of a large solution space. Multi-core system design methodologies perform architecture exploration at high level, taking into account constraints at this high level.

Transaction level modelling (TLM) has been widely used to explore the space solution at system level in a fast and efficient way. TLM enables architectural exploration, performance analysis and functional verification in the early stages of the

design with fast, data-accurate simulations using abstracted transactions between modules. The SystemC/TLM modeling methodology has been adopted for the design of the memory controller in [23] and for power estimation in [64] and in modeling of a Bluetooth standard in order to evaluate its performances in [7] and in the in modeling of the AMBA bus in [22].

- System level modeling of heterogeneous systems

The integration of heterogeneous systems in the same chip, such as digital, analog, biological and micromechanical parts brought to the necessity of their co-design and co-simulation. The necessity of simulating a continuous-time analog part can arise, for example, in the area of power switching control as in the automotive or RF domains. To this aim, it has been proposed to constitute an Open SystemC Initiative (OSCI) Working Group devoted to the development of an extension of SystemC to mixed-signal simulation: SystemC-AMS. Furthermore, SystemC must also extend to heterogeneous domains of application (i.e. electrical, mechanical, fluidic). Currently, the SystemC-AMS implementation is structured into different layers. The solver layer provides simple but efficient solvers for linear differential equations and for explicit-form transfer functions. The synchronization layer provides a simple and fast synchronization scheme that executes analog solvers before the first delta cycle of each time step, scheduling them using static data-flow. We developed an analogue mixed-signal extension to SystemC [47, 48] for the modelling and simulation of heterogeneous systems based on wave exchanges. This extension, named SystemC-wave mixed signal (WMS), allows the analogue part of the system to be modelled by a set of analogue modules, which communicate by exchanging energy waves. The approach based on wave quantities permits a total freedom of interconnection and therefore facilitates the development of reusable libraries of analogue modules. Moreover it is also better suited than SDF for analogue modelling, since it includes load effects naturally and provides more abstraction flexibility with respect to a circuit-level description.

- ICs for artificial neural networks, nonlinear dynamic fuzzy systems and RF applications

With the continuing improvement in the quality of the device models, and hence in the accuracy of computer simulation of integrated circuits, development of complex, mixed-signal analog/digital CMOS ICs has become possible and affordable. Analog processing paradigms, such as neural networks and fuzzy-logic, lend themselves to analog implementation quite easily. The activity of ICs design involved the analog implementation of approximate identities neural networks (AINNs) in 1.2 μm standard technology. Here a new stochastic learning algorithm whose parameters are stored by a multi stable circuit has been designed [10]. The architecture of a analog fuzzy control device for home appliance industry applications, has been developed. In particular, a prototype of the analog part of this device has been designed and implemented on silicon using a standard 0.8 μm CMOS technology, and for the membership functions a current-mode programmable translinear circuit has been designed [8]. Still, one major problem that was not easily solved in the analog domain

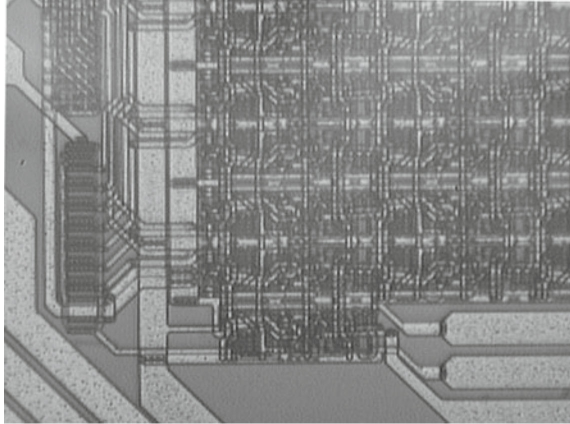

Fig. 6 Microphotography of a portion of 1998-era 800-nm CMOS IC for analog-domain storage of information. Individual transistors can be spotted to the left, while the upper-right image is a portion of a 7 × 5 matrix of storage elements

was that of (analog) parameter storage. The section dedicated to the storage of the fuzzy model parameters was thus designed, built, and tested in a standard 0.8 μm CMOS technology [14]. The purpose of the paper [2] was to further analyze the feasibility of a fully analog solution to create a multi-level memory for such storage, and evaluate the performance of such an implementation, based on nonlinear feedback circuits to create multiple attraction points and/or hysteresis. Figure 6 shows a microphotography of one of the chip built for this purpose in the late '90s. At the left side individual transistors, with a minimum gate length of 800 nm, can be spotted.

Subsequently, a new architecture has been proposed that implements the fuzzy model known as "fuzzy partition" [11, 15] and whose circuit has been designed and implemented in a standard 0.35 μm CMOS technology.

Besides, the design activity of radio frequency (RF) ICs involved the design and simulation of some circuits in C-band, in particular low-noise amplifiers (LNAs) [27, 28] and switching circuits with low losses such as the single-pole double throw (SPDT) switches [29] in order to test the cutting-edge 0.25 μm SiGe BiCMOS technology. The acquired skills have been exploited to the design of a multi-band LNA for WLAN home automation in 0.35 μm BiCMOS technology.

5 Graphene Based Field-Effect Transistors and Modelling Perspectives

The continued miniaturisation of device dimensions in ICs means that innovative solutions are demanded to overcome critical challenges in performance and reliability of future-generation electronics approaching fundamental limits due to aggressive down-scaling. Real prospects towards realization of the next-generation transistor technology are associated with high-performance devices and interconnects, that may be achieved by addressing key issues associated with applications in the areas of graphene/nanotube transistors and graphene/nanotube-based interconnects. Such

solutions promise to extend the life of digital electronics beyond the limits achievable with current silicon technology. The main hurdle preventing development in the area of graphene transistors is the absence of a band gap in graphene. Graphene only displays a quasi-band gap (vanishing of density of states), which translates into quasi-saturation, low gain and low I_{ON}/I_{OFF} for graphene transistors. Without a band gap, graphene transistors dissipate too much energy, exhibit large leakage currents and the current flow in graphene cannot be stopped to enable effective transistor switching action. In fact, the best current modulation reported to date has been about 30, measured at cryogenic temperatures. In addition, due to oxide charges and metal doping, zero band gap graphene has a finite minimum charge density despite the absence of any applied gate voltage. For that reason, as mentioned, finite current is usually measured in undoped graphene, with strong limitations in the use of as future CMOS-type logic circuits. Among the positive features of graphene-based transistor devices, we may mention (i) high mobility (up to 100 K cm^2 V^{-1} s^{-1}), (ii) low dimensional systems, few defects, (iii) high supported current ($> \mu$A/nm), (iv) planar profile. Conversely, possible limitations reside in: (i) absence of band gap, (ii) ambipolar behavior, (iii) mobility reduced by substrate effect, (iv) no saturation, (v) relatively high contact resistance.

Graphene-based materials could also play a specific role as planar interconnects, due to an intrinsically high thermal conductivity. Apart from challenges associated with scaling at the device level, interconnect systems continue to be an ever-growing challenge and are becoming one of the key components to decide IC performance due to the delay they add to critical paths, the power they dissipate and their susceptibility to electromigration that comes with progressive scaling.

Even with the limitations reported above, graphene FET (GFET) transistors have been successfully fabricated. In terms of operating speed, GFETs have already achieved a current cut-off frequency f_T above 300 GHz using conventional semiconductor manufacturing method (Table 1). Comparing graphene transistor operating speed with existing technologies (such as Si, III-V HEMTs, SiC, GaN etc.) [53] shows that graphene based devices are already comparable to conventional technology state-of-the-art. Moreover, graphene-based technologies will avoid production costs, toxicity issues and poor integrability associated with III/V materials. Differently from infinite graphene, one-dimensional carbon ribbons are theoretically expected to exhibit a band gap due to reduced dimensions electron confinement. The reduced dimensions of single-layer graphene nanoribbons (GNR), as low as 5 nm, could be exploited in transistor-like applications, whereas the performance of multi-layer and single-layer GNR with larger lateral sizes could be considered, in perspective, for on-chip interconnect applications. The expected bandgap for nanoribbons as narrow as 15 nm is 200 meV, and increases with decreasing size of the ribbon up to 0.8 eV for 5 nm wide GNR.

- Quantum transport analysis

Numerical simulation tools for the design of GFETs and interconnect applications are developed by self-consistent analysis. In general, the analysis of 2D nanodevices and nano-layered structures can be carried out by ab initio and first principles

Table 1 Comparison of graphene-FET performance with Si and III-V technologies

Technology	f_T (GHz)	f_{max} (GHz)	g_M (mS/μm)	L_g (nm)	μ ($cm^2V^{-1}s^{-1}$)	I_{DS} (mA·μm^{-1})
Exfol. graphene	300		1.27	140		3.32
CVD graphene on DLC substrate	300	42		40 and 140	3000	
Epitaxial Graphene on SiC	110	70	0.25	100	8700	>2.5
CVD graphene	23	10	0.5	110-170		1.3
Si	485		1.3	29	1400	
InP	385	1100	1.2	<50	15000	
InAs	628	331	1.62	30	13200	
GaN	225	300	0.53	30	2000	1.2

approaches, like DFT, that provide accurate calculations of the electronic structure. Other methods, based on more semi-phenomenological arguments, are commonly used to monitor the behaviour of extended systems made of a large number of atoms, which are computationally unaffordable by DFT: tight binding (TB) with DFT parametrization, and continuous models, like effective mass and $k \cdot p$ perturbation theory. A multimode scattering matrix (SM) method can be applied to model, at the electronic level, the charge transport [40–42]: this is formally equivalent to the non equilibrium Green's function (NEGF) approach, and allows easy simulation of very large structures, despite the possibly high number of electronic channels involved. It makes use of an explicit scattering matrix formalism, provided that the system under consideration is connected to the exterior world by "wave-ports", that are the terminations of semi-infinite periodic electronic waveguides. Such an analysis is applied to low dimensional systems, in their use as interconnects and channels for transistors and mixers. In addition, full-wave numerical techniques, both in frequency and time domains [51] can be applied to graphene and GNR.

Typical numerical results for the current-voltage characteristics of graphene transistor, with 600 nm channel and 200 nm gate electrode, are reported in Fig. 7. In the figure, we assume a Fermi level possibly shifted with respect to the Dirac point, mimicking a natural "doping" level for graphene, due to charge exchange with metal or substrate contacts. More refined simulations are currently under development, in order to take into account for global effects such as finite scattering length of charges, boundary effects, electrode and substrate effects.

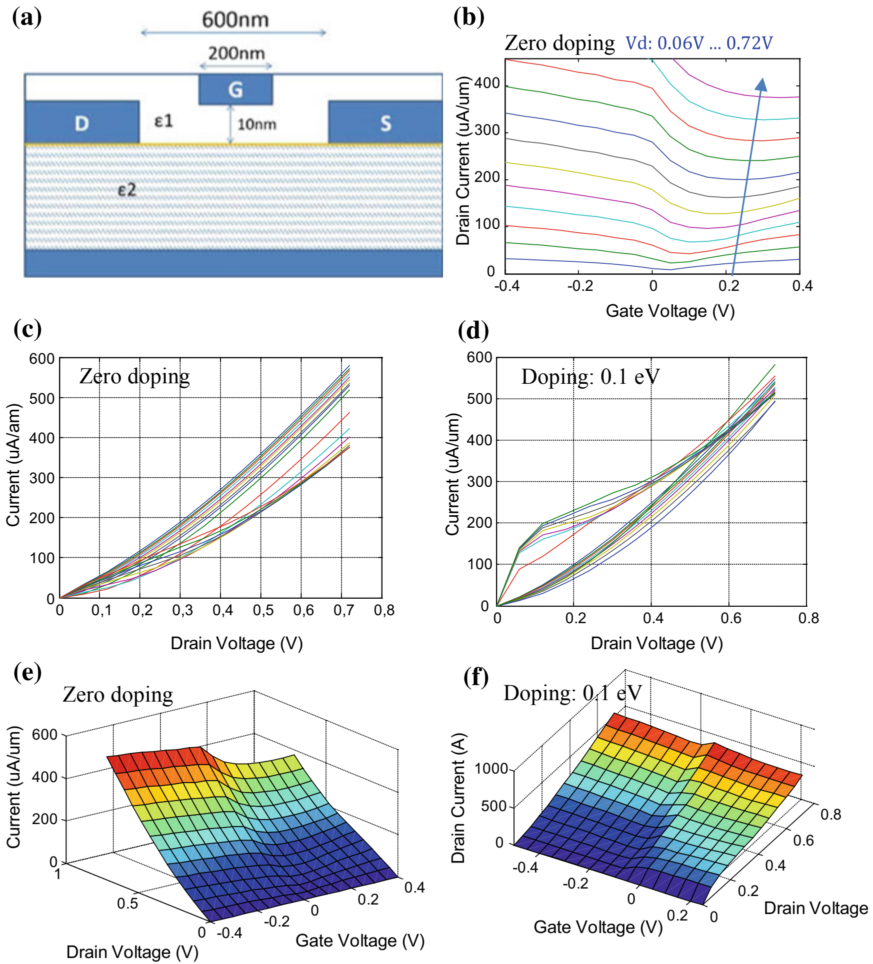

Fig. 7 Numerical simulation of current-voltage curves of graphene FET (geometry in a), showing typical poor saturation behaviour and quasi-linear slope ($b - e$). An oxide dielectric constant $\sigma_1 = 25$ is assumed, with $\sigma_2 = 4$ for the substrate. The "doping" is referred to a possible shift of the Fermi level with respect to the Dirac point [40] ©[2016] IEEE

- Computational platform

Charge-transport and electromagnetic problems are inherently multi-physics, in both usual meanings: (i) they apply the same physical model to different length and times scales, as those of quantum and electromagnetic phenomena, (ii) they link models with different underlying physics. The ambition of our activity is to deal with the above complexity at the circuit level, by developing GNR interconnects, transistor prototypes, and dedicated numerical tools. The proposed computational platform defines, on the one side, general modelling and simulation routes at both device and

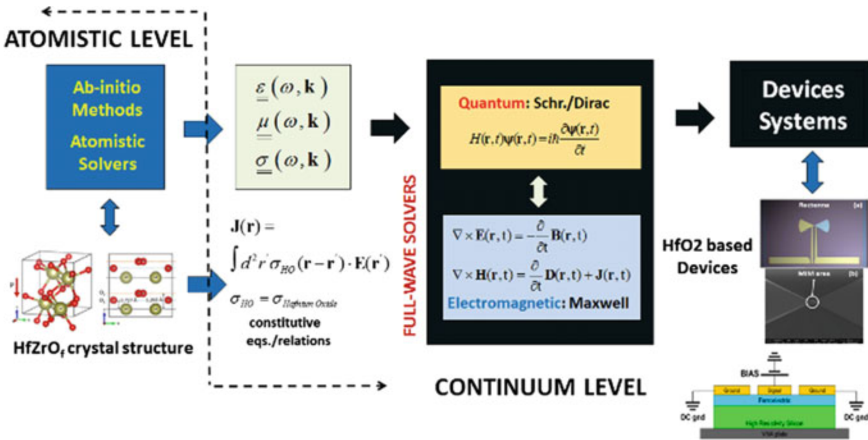

Fig. 8 Schematics of the numerical platform. *Ab-initio* simulations performed at *atomistic* level transfer/integrate the results into/with the larger scale models by constitutive equations/relations, in order to incorporate all necessary physics towards *full-wave* simulation, performed at *continuum* level. At the *continuum (device)* level, we have the simulation of the real devices/sub-modules based on nano-structured materials. At this level, the electromagnetic phenomena can be also coupled to quantum transport phenomena, described by Schrödinger/Dirac equations

sub-module level; on the other side, it provides and optimizes programs and simulations for specific issues and challenges. Particular challenges rely in dealing with the low-dimensionality of the materials and coexistence of multiphysics phenomena, e.g. electromagnetic (EM), charge propagation and quantum transport. Specifically, inherently quantum phenomena like ballistic transport, tunneling, many-body correlations, carrier confinement, and interface effects, overlap with classical physical effects. Such overlap makes traditional circuit design unsuitable to nanoelectronics. In order to overcome the above issues, we developed appropriated models based on the solution of coupled systems of equations dealing with combined electromagnetic-transport phenomena i.e. Schrödinger/Dirac, Maxwell-Boltzmann, etc. The above platform aims at accounting for the different aspect-ratio between nano-structured materials and device environment (see Fig. 8), bridging from the atomistic to the continuum scale (extreme multi-scale analysis). The key-issue is the coupling of quantum models and electromagnetic models, that acts at discrete level, but, in some case, as for ballistic regime, also at continuum level. Other physics can also be included, e.g. coupling to phonons (thermal effects).

Exploiting constitutive parameters extraction from nanoscale models may lead to a compact representation, like the one provided a by complex, temporally and spatially dispersive: (i) electric permittivity/conductivity; (ii) magnetic permeability, also in tensorial form, depending on the kind of example under analysis. These constitutive equations, that should be consistent with the Kramers-Kronig relation according to causality, are then incorporated into the full-wave simulation platform that, in turn, could consists of coupled systems of partial differential equations (PDE),

dealing with combined multi-physics phenomena, in particular: (i) electrodynamics (Maxwell); (ii) ballistic quantum transport (Schrödinger/Dirac) [51, 52]; (iii) thermal effect (acoustic wave equation, continuum mechanics). Concerning the full-wave numerical methods, it is crucial to avail both (i) frequency-domain techniques, as finite-elements/finite-difference methods (FEM, FDFD), and (ii) time-domain techniques, as finite-differences in time-domain (FDTD), and transmission line matrix (TLM) method. It is remarkable to note that the use of TLM permits, in conjunction with the implementation of system identification methods and Krylov subspace reduced order techniques: (i) to calculate the impulse response of the circuits (numerical Green's function), and (ii) to derive global (device) equivalent circuits. Standard solvers usually can simulate either quantum transport or full-wave electromagnetics, but a simultaneous solution is very hard to be achieved at a large scale. That is the reason why remark the need to link the atomistic scale up to the continuous world: separation of the micro-, meso- and macro- (bulk) scales [36] can be achieved by means of a holistic modelling framework incorporating the full-wave description at all scales, but allowing the homogenization as a subset of the of multiscale numerical procedure. Such multi-resolution approach is a representation of the underlying numerical formulation of Maxwell boundary-value problem [37, 39].

6 Conclusion

It is almost sixty years since the invention of the silicon integrated circuit and over fifty years since Gordon Moore observed that the number of components on a single chip of silicon had doubled every year since its invention [44]. However, the atomic structure of silicon will someday set limits to the further evolution of silicon technology. Nanotechnologies offer alternative materials and devices which may circumvent the limits such as resonant tunneling or single electron devices, carbon nanotubes as interconnects or transistors, and eventually complex organic molecules as memory and logic units, to name just a few. In this paper some key aspects that determined the rapid advancement of microelectronics have been reported and several recently discovered nanomaterials have been discussed.

Acknowledgements The authors would like to thank Laura Falaschetti for her comments and valuable contribution to the editing process of the paper.

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