Chapter 7
Advanced Multiphasing: Pushing the Limits of Fully Integrated Switched-Capacitor Converters

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7.1 Introduction

Over the past decades, fully integrated power management has received a lot of attention in the literature [1]. For low-power internet-of-things (IoT), sensor nodes potentially combined with energy scavenging, the reduced PCB footprint, system height, and reduction of the number of external passives that monolithic power converters provide can have a tremendous effect on the total system size and cost. On the other end, the transportation of energy onto higher power systems-on-a-chip (SoCs) has become an effective bottleneck to these systems' performance. A bottleneck that could be solved using DC–DC converters that are integrated together with the load onto the same die, as illustrated in Fig. 7.1. Using an external point-of-load (POL) converter, the SoC has a certain intake current which induces substantial voltage droops in the power delivery network (PDN). In order to guarantee correct operation, the load consequently has to be designed with a certain voltage margin in mind [2]. However, this voltage margin does lead to a higher power consumption, even when it is not needed. Moreover, thanks to the continued scaling of technology's supply voltages [3], the intake current together with the voltage margins has increased making the PDN effects effectively large loss contributors [4]. In contrast, by shifting the POL converter on-chip, as shown in Fig. 7.1b, the intake current is reduced by the converter's voltage conversion ratio (VCR), causing the voltage margins and PDN losses to be reduced by the same factor as well.

In addition, fully integrated converters are a key enabler for extensive granularization of voltage domains in today's SoCs and processors [5, 6]. The central idea

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Fig. 7.1 An example power delivery network (PDN) to an integrated load using (**a**) an external and (**b**) an on-chip DC/DC converter
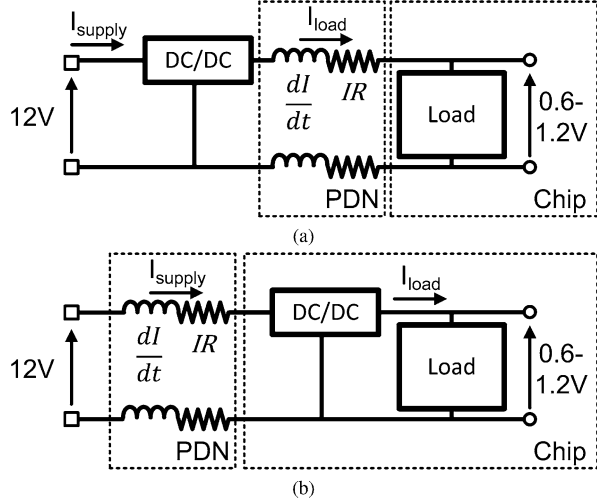
is simple: if every core or functional block of a SoC would be supplied a voltage that is just high enough to fulfill its task in a given time, independent of the rest of the SoC, then a substantial amount of energy can be saved [7]. Depending on the workload, a processor's efficiency could be increased by as much as 21% if per-core dynamic voltage and frequency scaling (DVFS) is used [8]. Because this does mean that every granular block requires its own voltage domain and thus voltage regulator, realizing a high level of granularization is impractical with external converters.

By far the most popular type of POL converter is the buck converter. However, the lack of quality of integrated inductors has posed a serious problem for their full integration. To make things worse, this quality issue appears to be tied to the inductor's small size and is thus fundamental in nature [9]. As a result, most inductive converter designs in the literature have opted for a system-in-package (SiP) rather than a SoC approach where the inductor is not integrated on the die itself, but made out of bondwires [10], extra back end of the line (BEOL) metal and/or magnetic layers [11], PCB tracks [12], or a surface-mount device (SMD), possibly mounted directly on the silicon [13].

Switched-capacitor (SC) converters, in contrast, only need switches and capacitors, both of which are readily available in modern CMOS processes. Consequently, these converters have gained popularity as a promising candidate for full integration. Nevertheless, the monolithic context does pose its own challenges that inherently constrain the design space of fully integrated SC converters. This is portrayed in Fig. 7.2. At low-power densities, the converter's efficiency is limited by the relative size of the flying capacitor's parasitic substrate coupling, C_{BP}/C_{par} and the flying capacitance, C_{fly}, itself due to a combination of charge-sharing losses in the flying capacitors and parasitic coupling, or bottom-plate (BP), losses [14, 15]. For increasingly large output powers, a clear efficiency-power-density trade-off becomes apparent due to power transistor losses gaining in importance. Here, it is
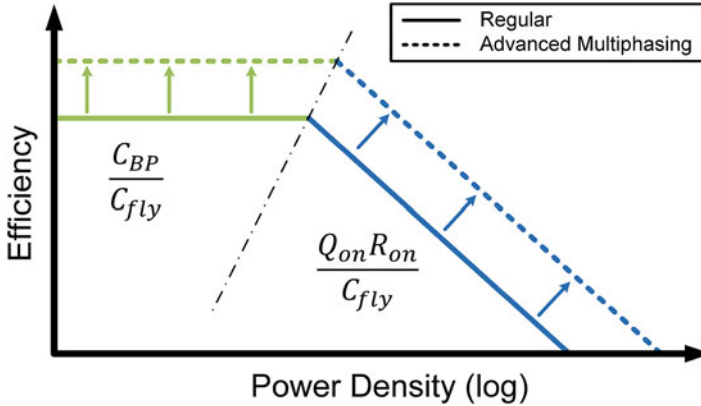
Fig. 7.2 Effect of advanced multiphasing on the monolithic SC converter design space

the ratio of the transistor $Q_{on}R_{on}$ and C_{fly} density that is the dominant factor [14]. Unfortunately, due to the planar nature of modern technology nodes, the parasitic coupling is relatively large while the flying capacitance density per unit area is small compared to external components. Thus, both at low- and high-power densities the design space is much more constrained compared with SC converters using external components.

Moreover, SC converters also have a topological issue: Due to the fact that charging capacitors with a voltage source or other capacitors inherently leads to charge-sharing losses, SC topologies have traditionally been designed to minimize the voltage swing across their capacitors' terminals [16]. With the capacitor voltages consequently being approximately constant over a full converter period, a SC converter topology has a fixed ideal voltage conversion ratio (iVCR) at which it could theoretically achieve 100% efficiency. At smaller VCRs, say when the output voltage is reduced, the efficiency drops rapidly. While multiple topologies can be combined together in a gearbox converter [17–23], this does require a lot of additional transistors to maintain a high efficiency over a wide voltage range, increases the system complexity, and ultimately reduces the efficiency and power-density for the full VCR range [24].

Multiphasing or interleaving is a popular technique in the literature where a converter is split into several converter cores that run in parallel but out of phase of each other to reduce the output voltage ripple [25, 26]. Especially in the monolithic context, where both capacitors and transistors can rather easily be split into smaller parts and where the achievable frequencies are much larger than required for a power converter, multiphasing can be implemented with very low overhead. With advanced multiphasing (AM), these out-of-phase cores are used as a resource: by having them interact with each other, the typical two-phase converter can be transformed to have many more distinct converter phases. These additional phases can then be used to boost the converter's performance or even to unlock fundamentally new types of SC converters.

This chapter is organized as follows. Section 7.2 introduces a first technique that focuses on the reduction of parasitic coupling losses in a SC converter. After, Sect. 7.3 focuses on improving the effective capacitance density on-chip, and Sect. 7.4 demonstrates a SC topology with a continuously scalable conversion ratio. Finally, Sect. 7.5 highlights the main conclusions of this chapter in a brief summary.

7.2 Scalable Parasitic Charge Redistribution

Figure 7.3a shows the main working principle of a two-phase SC converter that uses multiphasing from the point of view of its capacitor's bottom-plate node, V_{BP}.
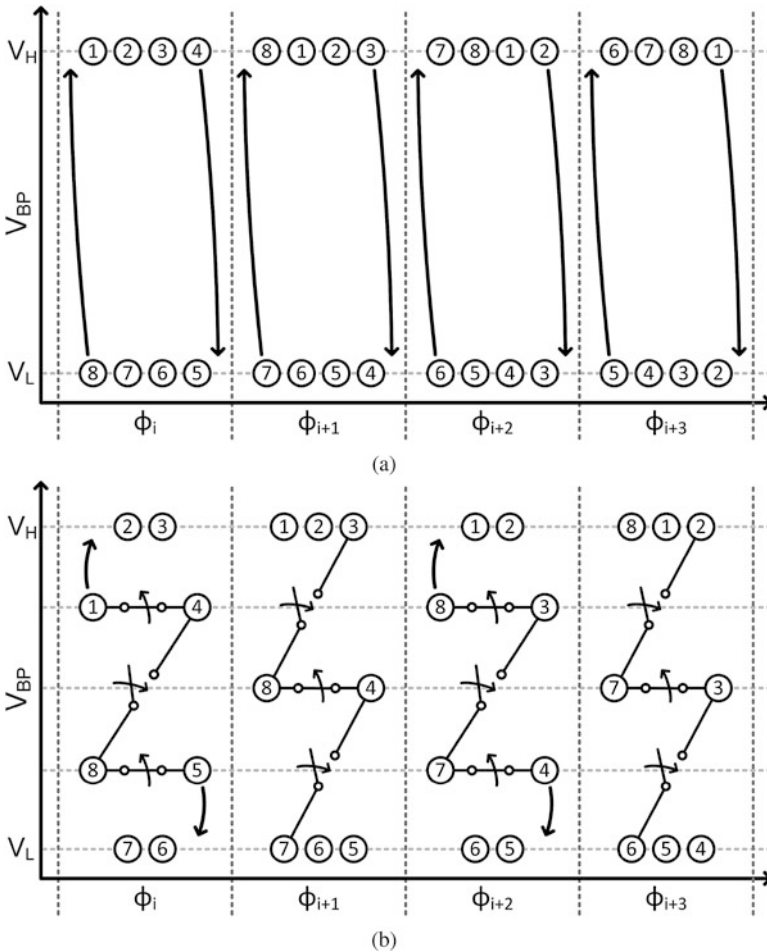

Fig. 7.3 Bottom-plate voltage, V_{BP}, versus phase diagram of (**a**) a regular multiphasing converter with 8 cores, and (**b**) a converter using SPCR with 3 charge redistribution steps. Each labeled circle represents a different converter core. Arrows represent actions during phase transition

It can be appreciated that each core can either be in a high or low voltage state, corresponding to V_H and V_L, respectively. At each switching event, the two cores that have been in the high/low state the longest transition to the next state by fully charging/discharging their V_{BP} to V_H/V_L. In the charging case, V_H needs to supply an amount of charge equal to the voltage difference between both states and the size of the parasitic coupling on the BP node.

Scalable parasitic charge redistribution (SPCR) introduces a dedicated BP charging and a dedicated BP discharging state [15, 27]. Instead of transitioning from a high state directly to a low state, cores will first enter the dedicated BP discharging state. Similarly, a core will go through the BP charging state when going from the low to the high state. Figure 7.3b illustrates an example SC converter using SPCR. Cores that are neither in the regular high nor in the regular low state are instead in the BP charging or discharging state. Here, all the regular power transistors are non-conducting and the core itself can only be at a set number of intermediate levels, chosen during design time. At every clock edge, each BP charging core is paired up with the BP discharging core which is in the closest, yet higher intermediate level. By shorting the BP nodes of each pair, their V_{BP}'s average out by transferring charge from the BP discharging to the BP charging core. This is called a charge redistribution step (CRS) and results in all paired BP charging cores going up, and all paired BP discharging cores going down one intermediate level. BP charging/discharging cores which are already at the highest/lowest intermediate level, and can consequently pair up no more, are instead pulled up/down to the high/low state. Furthermore, to keep this process going, every two phases, the two cores that have been in the high/low state for the longest time, are transferred to the BP discharging/charging state. The end result is that the low to high transition is now completed approximately adiabatically using a fixed number of CRS equal to the number of intermediate levels and that V_H only needs to supply enough charge to pull the core up to the high state, which is in general (CRS + 1) times lower than the charge without SPCR. The BP losses are consequently also reduced by the same factor.

Ultimately, the losses associated with the parasitic coupling are thus reduced in a scalable manner. Considering the fact that these losses are one of the determining factors of the maximum obtainable converter efficiency on-chip [14], the efficiency of a SC converter can be substantially improved. For larger values of CRS, though, the extra transistors that enable the charge redistribution steps to take place do add significant additional losses such as leakage that cause a new efficiency ceiling to emerge [15]. Regardless, this new ceiling is generally substantially higher compared with the situation without SPCR, depending on the ratio of the parasitic coupling to the flying capacitance, and on how leaky the transistors are. To verify the obtainable efficiencies of the SPCR technique, a fully integrated 2:1 SC converter was designed in a 40 nm process using 16 cores and 9 CRS, thus reducing the parasitic coupling losses tenfold. A system overview of the converter is shown in Fig. 7.4. Rather than connecting the cores' BP nodes directly with each other, they connect through a charge redistribution bus (CRB). Furthermore, the bus they use depends on their resulting intermediate voltage level after their V_{BP}'s average out. The end result is
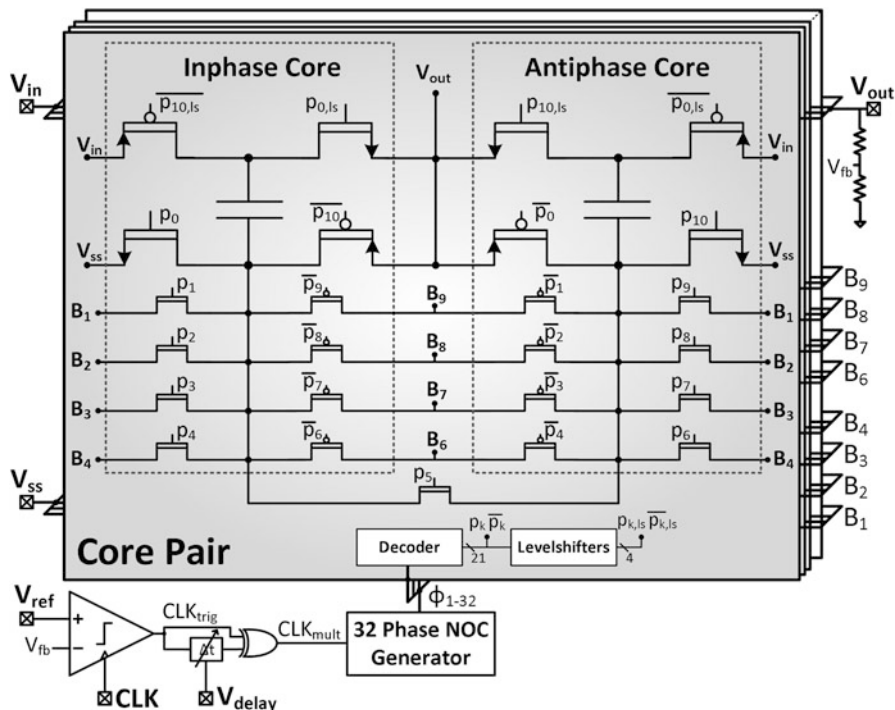
Fig. 7.4 System overview of a converter implementing SPCR, showing the controller and transistor-level implementation of the converter cores

that significantly less area overhead is needed and that the voltage swing on each CRB is approximately zero, effectively making them DC voltage rails. The CRBs can also be used to power low-power circuitry within the converter itself [28, 29], and do not require any additional start-up circuitry to converge to their DC levels: Using the regular control signals, the CRBs naturally spread evenly over the full BP node swing.

From a conceptual point of view, the CRBs also greatly facilitate the design and implementation of this technique. A core simply needs to connect to these CRBs in a certain order when charging its BP node, and in the opposite order when discharging. The number of CRBs further determines the number of CRS and subsequently by how much the parasitic coupling losses are reduced. At the converter level, there need to be enough out-of-phase cores given the number of CRBs to make sure every time a core connects to a CRB, there is another core to exchange charge with.

The bottom line is that, thanks to the presented AM technique, the realized converter achieves a higher efficiency than any other fully integrated SC regulator, including those using deep-trench capacitors which have much smaller parasitic

coupling but require extra masks [30, 31]. To this day, the achieved efficiency of 94.6% is still the highest converter efficiency demonstrated entirely on-chip.

7.3 Stage Outphasing and Multiphase Soft-Charging

Despite the success of SPCR in improving the efficiency of SC converters, its effect is reduced at higher power densities. This is simply because the parasitic coupling losses themselves are less important here. In contrast, stage outphasing (SO) and multiphase soft-charging (MSC) are two techniques that aim to improve the effective capacitance density by reducing the charge-sharing losses of the flying capacitors, thereby also having an impact at high-power densities. Although said techniques can be used for many topologies [32], they are demonstrated here using the Dickson converter [16].

In a regular N:1 Dickson converter, there are a total of N − 1 stages. If V_{out} is close to the technology's supply voltage, the top-side switches are usually implemented as two stacked transistors to avoid using less-efficient I/O devices. This also leads to the creation of intermediate nodes (k), which are topologically speaking DC nodes and can be used as voltage rails. These intermediate nodes always connect a discharging flying capacitor of a stage to a charging flying capacitor of the next stage, also portrayed in Fig. 7.5.

Note that this situation is very similar to the discharging/charging of the parasitic coupling if SPCR is used with just one CRB. Recall that with SPCR, the number of CRBs can be scaled freely, and as long as the charging and discharging capacitors connect with the CRBs in opposite order, they will spread evenly over the full range, leading to the approximate adiabatic (dis)charging of the parasitic coupling. This is also the essence of the first technique, multiphase soft-charging, shown in Fig. 7.6: simply by splitting the intermediate node (k) up into multiple nodes $(k,1)$ to (k, M) and having the charging and discharging flying capacitors connect to these in opposite order, they will spread evenly. Of course, this is assuming that the stages
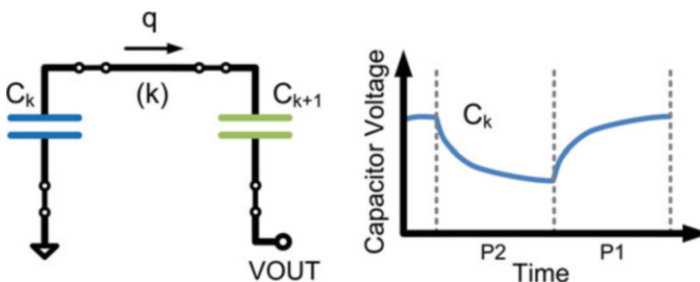

Fig. 7.5 Charge transfer between two adjacent stages of a regular Dickson converter. C_k and C_{k+1} are the flying capacitances of stages k and $k + 1$, respectively, q is the transferred charge
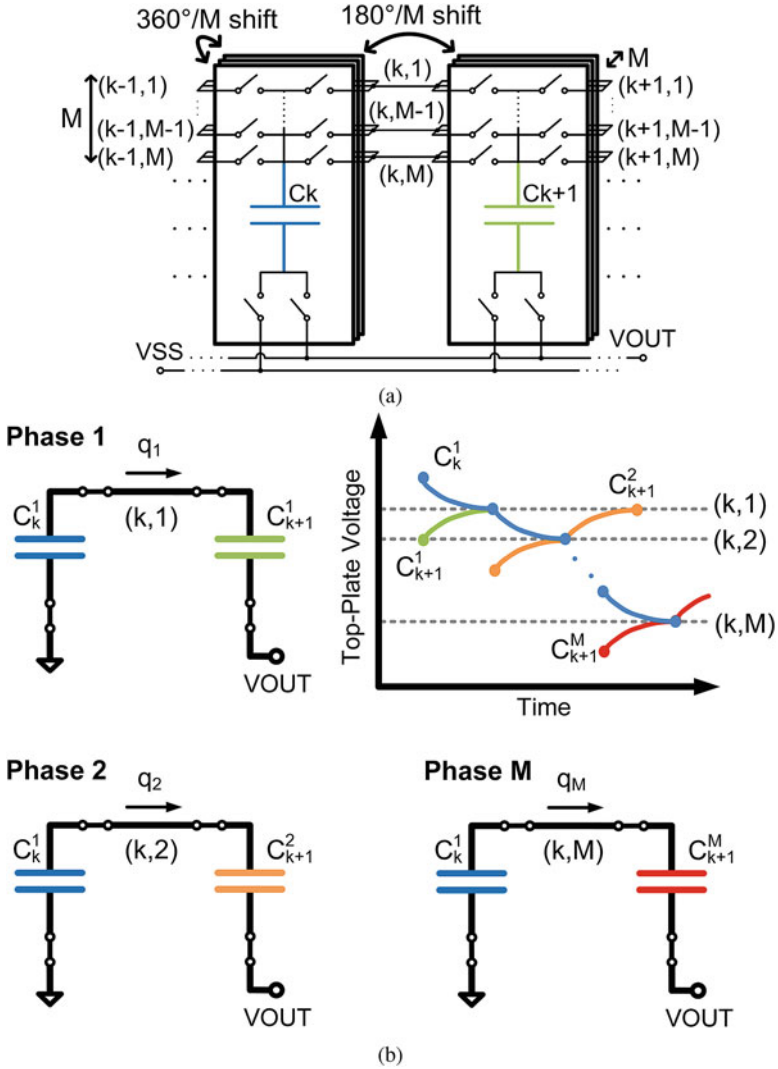
Fig. 7.6 Application of multiphase soft-charging to a Dickson converter with factor M. (**a**) a schematic overview, (**b**) the charge transfers of two adjacent stages

themselves are split up into a sufficient number of out-of-phase cores. The resulting step-wise (dis)charging reduces the charge-sharing losses by the number of steps, M, which is fully equivalent to increasing the effective capacitance density by the same factor. In other words, the effective capacitance density can be scaled freely by spreading the charge transfers between the flying capacitors out over multiple steps in what we call soft-charging. To achieve this, however, extra power transistors need to be added that connect the capacitors to the many intermediate nodes, which
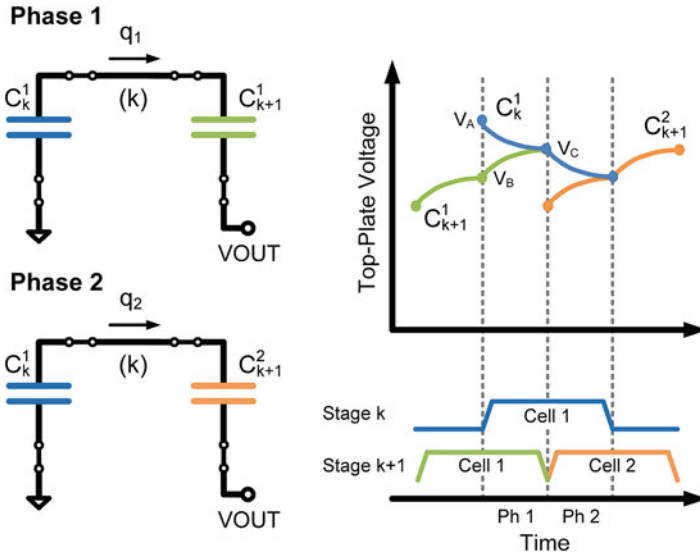
Fig. 7.7 Application of stage outphasing to a Dickson converter

will increase the total transistor-related losses. In the end, the balancing between the increase of these losses with the reduction of the charge-sharing losses will determine the optimal number of M and the overall efficiency improvement.

Stage outphasing is a second technique where adjacent stages are put out of phase with each other to, surprisingly, achieve the same effect as MSC with $M = 2$. Figure 7.7 illustrates this. Here, the discharging flying capacitor that was already connected to the intermediate node connects to the flying capacitor that has not been charged yet. In other words, the capacitor in its second discharging phase connects to the capacitor in its first charging phase. Similarly, when the converter switches again, the capacitor in the second charging phase will connect to another capacitor in its first discharging phase. In some way, the intermediate node (k) thus acts as two nodes through which the charging and discharging capacitors connect in opposite order. Unlike with MSC, though, no additional transistors have to be added, and the gain of SO consequently comes with no real cost.

Now, for a full converter there will be charge transfers that are between a capacitor and a combination of converter terminals. Because the voltage difference across these terminals is considered to be DC, these charge transfers cannot be soft-charged. Nevertheless, the Dickson converter only has two such transfers, regardless of the number of stages, which makes the use of MSC and SO more impactful as the number of stages and the VCR increases. Using a combination of SO and MSC, a fully integrated SC 3:1 DC–DC converter was made that has a 60% higher effective capacitance density [33, 34]. It is in part, thanks to these techniques, that said converter obtained 82% efficiency at a power-density of 1.1 W/mm^2

in measurements, which corresponds to $3\times$ lower losses compared with similar power-density designs, or close to $30\times$ higher power-density compared with similar efficiency designs in the literature.

7.4 Continuously Scalable Conversion Ratio

For the past decades, SC converters have been designed such that the voltage swing across their flying capacitors' terminals is minimized as shown in Fig. 7.8a, because this was considered the only way to minimize the charge-sharing losses and to obtain a high efficiency converter. Unfortunately, because the amount of charge that is transferred is proportionate to the capacitor voltage swing, this means that the output charge per cycle of these converters is minimized as well. If a higher output charge per cycle is required, the converter can only obey by increasing the voltage swing and thus lowering the efficiency, which also lowers the VCR. Consequently, a conventional SC converter's VCR, efficiency, and output charge per cycle are closely linked.

With the introduction of advanced multiphasing, however, we showed that charge-sharing losses can also be reduced by spreading the (dis)charging of flying capacitors out over multiple steps, over multiple phases. Consequently, rather than minimizing the voltage swing of the flying capacitors, and thus the output charge of the converter, the efficiency of the converter can instead be improved using soft-charging regardless of the capacitors' voltage swing. This offers the exciting opportunity to make switched-capacitor converters with large capacitor voltage swings that are soft-charged for high efficiency, as illustrated in Fig. 7.8b.

To arrive at such a converter, first a set of phases is chosen that maximizes the voltage swing on the flying capacitor while simultaneously taking into account that the transition from each phase to the next should lead to charge being transferred to and from the right converter terminals. In an efficient step-down converter, for example, charge should be transferred from the input and ground terminals to the output terminal. Figure 7.9 portrays such a set of phases, which we refer to as cornerstone phases. For a more detailed explanation on how to derive this set, the authors refer to [32, 35]. From these cornerstone phases, soft-charging can be implemented similarly to other AM techniques, by adding intermediate nodes through which charging and discharging capacitors can connect. Here, two sets of nodes are added for the top and bottom nodes of the flying capacitor, shown in Fig. 7.10. Because the charging and discharging capacitors connect to these nodes in opposite order, these nodes spread out between V_{in} and V_{out}, and V_{out} and V_{ss}, respectively.

Because the capacitor voltage does not stay approximately constant over a full clock cycle, this topology cannot be modeled using an ideal transformer with a finite
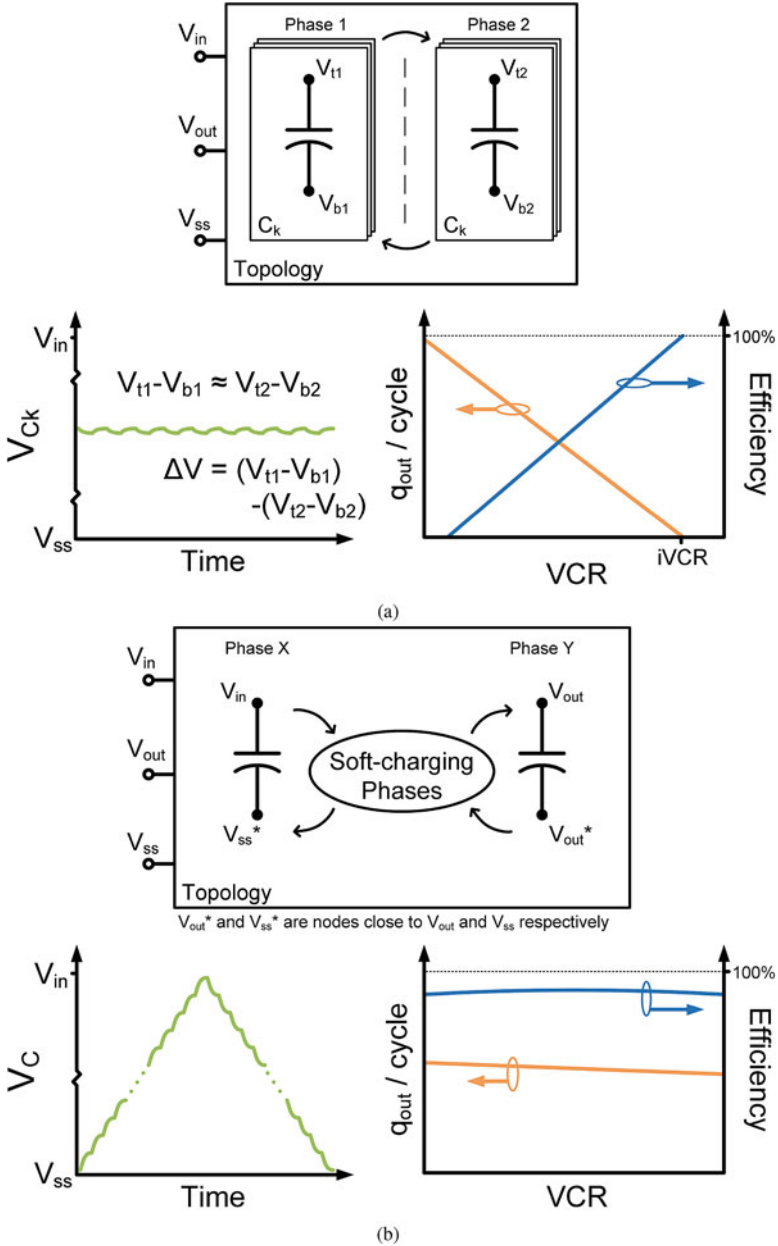
Fig. 7.8 High level concept of (**a**) a conventional two-phase switched-capacitor converter, and (**b**) a large capacitor voltage-swing switched-capacitor converter

Fig. 7.9 Cornerstone phases
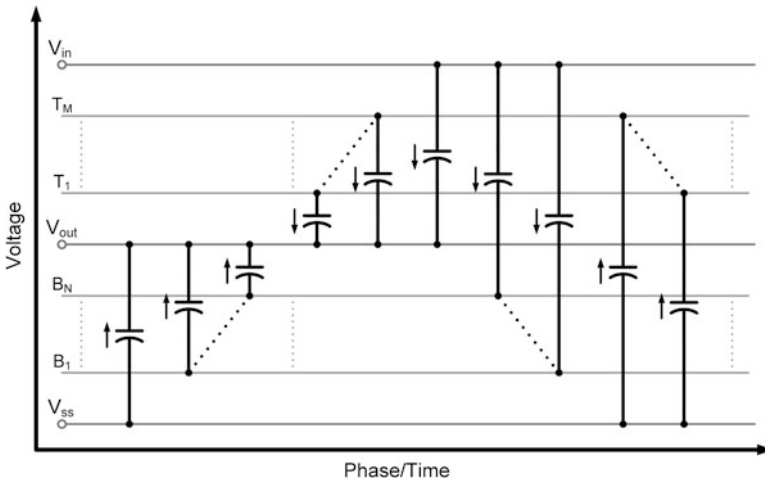of large capacitor
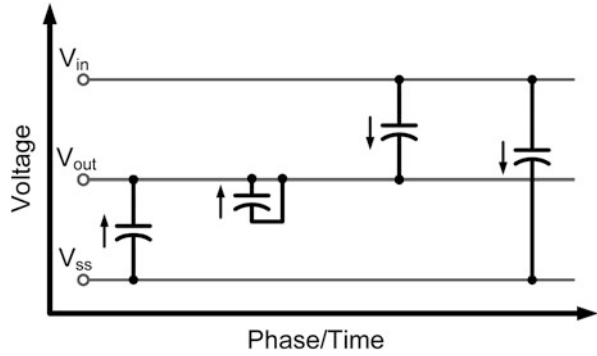voltage-swing converter

Fig. 7.10 Voltage versus phase diagram of the presented topology

output impedance like regular SC converters can [36, 37]. Instead, it can be shown that this particular topology behaves like a gyrator [32]. That is, its output current is mostly proportionate to the input voltage, and not the output voltage. Thus, with constant input voltage, the output charge per cycle is mostly independent from the conversion ratio. At the same time, the input charge per cycle scales linearly with the output voltage. Figure 7.11 compares the theoretical efficiency of this topology to a regular SC converter, and demonstrates that, as the number of intermediate nodes increases, the converter tends towards an ideal gyrator which is lossless regardless of the VCR, both step-up and step-down.

The topology is realized in a 28 nm technology using 32 intermediate nodes at both the top and bottom side [38]. The micrograph of this design is shown in Fig. 7.12, while the measured efficiency is portrayed in Fig. 7.13 for an input voltage of 2 V. It can be appreciated that the latter demonstrates the gyrator behavior of the
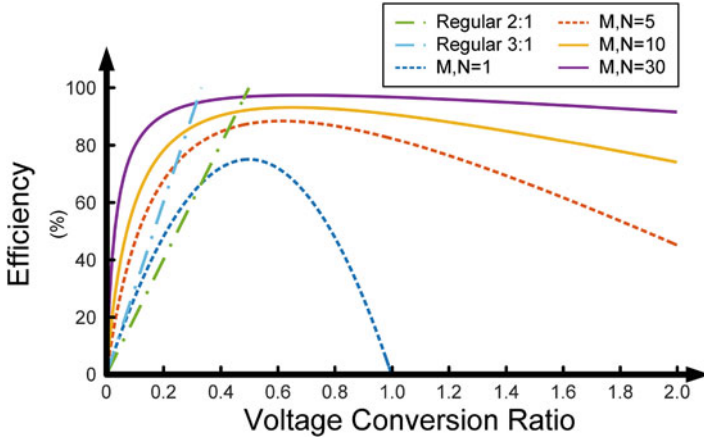
Fig. 7.11 Efficiency of presented topology for different number of top- and bottom-side soft-charging phases, M and N, compared with a regular 2:1 and 3:1 SC converter
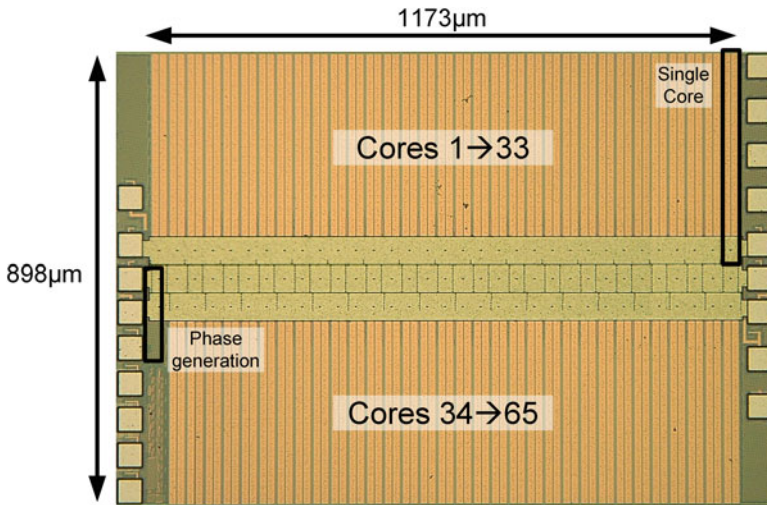

Fig. 7.12 Micrograph of the monolithic SC converter using a continuously scalable-conversion-ratio topology

topology and that the converter maintains an efficiency of more than 80% over a continuous VCR range of 0.85, which is substantially higher than designs using regular SC gearbox converters in the literature [17, 18, 23]. In addition, this design achieves a peak efficiency of 93%.
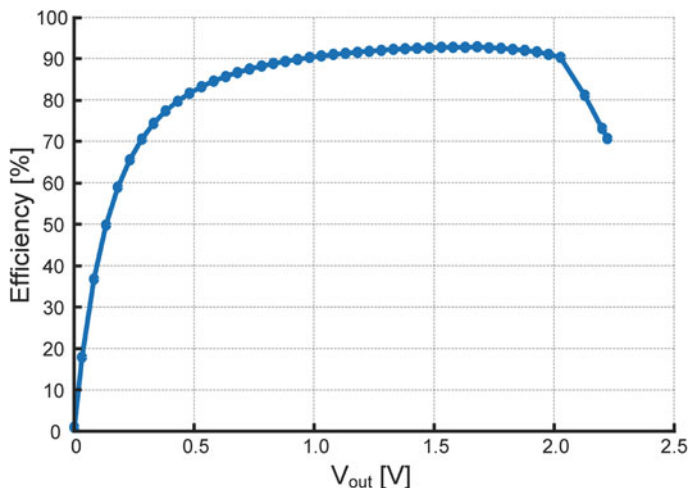
Fig. 7.13 Measured efficiency versus output voltage of the presented converter at a fixed clock frequency

7.5 Conclusions

This chapter touched upon the main factors that have sparked the interest in monolithic power conversion and why switched-capacitor converters in particular make an excellent candidate. The large parasitic coupling to the substrate, the limited capacitor density on-chip, and the inherent constrained conversion ratio range were presented as challenges to the widespread adoption of this type of converter. With advanced multiphasing, multiple out-of-phase converter cores inter- act with each other to arrive at a switched-capacitor converter with more than the typical two phases that in the end has more capabilities and/or better performance. Several advanced multiphasing techniques were discussed that focus on both high- and low-power densities, and even allow for a new type of switched-capacitor converter which has a continuously scalable conversion ratio. Measurement results demonstrated the working principles of these techniques and showed the great potential of advanced multiphasing in pushing the limits of fully integrated power conversion further.

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