Chapter 12
SOI FinFET for Computer Networks and Cyber Security Systems

Neeraj Jain and Balwinder Raj

Abstract Today, computer-based systems have become common in everyday life and these systems are used to store leverage information and people are more willing to communicate this sensitive information with the real world. So, computer networks have become the emerging domain for connecting physical devices like home appliances, vehicles, and other embedded electronics, software, actuators, and sensor-based systems, and security of these systems from cyberattacks is essential for secure communication. This results in the easy and safe communication between different entities. So, modern advanced computer systems with efficient integrated transistor technology provide the security and privacy to the computer-based real world. This chapter explores the advanced Silicon-on Insulator Fin Field Effect Transistor (SOI FinFET) technology which is the basic unit of integrated circuit used in every electronic gadget and computer hardware. In this chapter, performance analysis of device-D1 (high-*k* SOI FinFET structure) is done to implement the efficient computer hardware over a wide temperature range (200–450 K). The attempt is done to find out the ZTC (zero temperature coefficient) biased point of SOI FinFET device to have stable, reliable, and secure systems. The proposed device analysis will provide the hardware design flexibility in the electronic circuits, microprocessors, computer hardware, and thermally stable interfacing components for security applications of information technology.

The potential parameters of device-D1 like A_V (intrinsic gain), g_m (transconductance), V_{EA} (early voltage), g_d (output conductance), I_{off} (off current), I_{on} (on current), I_{on}/I_{off} ratio, C_{gs} (gate-source capacitance), C_{gd} (gate-drain capacitance), f_T (cutoff frequency), and SS (subthreshold slope) are subjected to analysis to evaluate the performance over wide temperature environment. The validation of temperature-based performance of device-D1 gives an opportunity to design numerous analog/RF and digital components in Internet cyber security infrastructure environments.

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1 Introduction

Today, SOI FinFET technology has replaced the conventional transistor technology in almost all nanoelectronic applications. From microprocessor to all system levels, electronic products are integrated with FinFET technology to have advanced functionality and thermal stability over a wide temperature environment. The requirement of low-power, high-performance, and portable consumer products has become the driving force for enhancement in transistor technology. The invention of FinFET technology drastically changes the semiconductor industry life due to 3D (dimensional) quasi-planar nature of geometry [1]. With the development of transistor technology came the advancement and protection from cyberattacks in the computing network [2].

The analog components based on FinFET technology used in sensors (temperature, motion, pressure, shock, proximity, sound, gas, infrared, etc.), amplifiers, signal processors, microcontroller, Internet of Things (IoT), and integrated chips give better technology to computer networks and cyber security applications [3–6]. Therefore, some of the world's top semiconductor chip industries like Cadence and TSMC designed FinFETs at 7-nm technology node for security and high-performance computing platforms, and other industries are further trying to enhance the performance of SOI FinFET by optimizing underlap spacer region at lower technology nodes [7–9].

The SOI high-*k* FinFET was introduced in the integrated circuits to reduce leakage current which is caused by SCEs and transistor scaling effects [10]. However, there is always a tradeoff among SCEs (short channel effects) and analog/RF performance of FinFET. Further improvement in FinFET structure has been done through SOI layer, high-*k* spacer, and source/drain engineering techniques [11–13].

According to literature, significant work already proposed with underlap high-*k* and dual-*k* spacers to enhance SCEs and analog/RF performances of SOI FinFETs [14, 15]. Similarly, [8, 16] demonstrates the asymmetric dual-k spacers and symmetrical SOI FinFET structures for high-performance application. [17, 18] also elaborated the asymmetrical dual-k spacer SOI FinFET structure for digital SRAM and low-power design applications. Some implementations of high-k SOI FinFETs like oscillators, data converters, RFID (radio frequency identification), mobile phones, and IoT devices make the human life simpler and automated [19–21].

Besides of these, some applications like automobiles, military security, and nuclear sectors require high temperature operated integrated circuits (ICs) and other like medical diagnostic systems and space applications require low temperature based operated equipment. Some industries demand for both high- and low-temperature sustainable ICs for their thermally stable environments [22–24]. FinFETs are the devices which fulfill the requirement of these ICs, and chip industries are now trying to implement the FinFET circuits in all electronic gadgets

like computer chips, mobile phones, and sensor-based high-performance security and privacy systems in varying temperature environments [25–31].

2 Reliability and Flexibility Approach of SOI FinFET Towards Security

The performance of computer networks, cyber security operating systems, and a lot of commercial electronic systems varies in different temperature environments due to variation in the performance parameters of its basic transistor parameters. So, having more stability of the mentioned systems against temperature variation, these systems are built by high-*k* SOI FinFET. The high-*k* SOI FinFET is more susceptible to temperature variation and provides a more stable analog/RF performance parameter at ZTC biased point. Analog/RF performance parameters are the basic parameters of any electronic system and are evaluated at transistor level. So, this chapter explores and analyzes the performance of high-k SOI FinFET structure and the sensitivity of this structure in temperature range 200–400 K towards analog/RF design is very crucial. So, the investigation is done for ZTC bias point over a wide temperature range through 3D simulations. ZTC bias point is an important parameter which describes the stability of a semiconductor device and shows the negligible variation in current–voltage (I-V) characteristic with temperature. The previous literature work in [32–34] has been done with ZTC bias point for MOSFET stability analysis.

As compared to conventional transistor structure, the high-k SOI FinFET gives better temperature performance at sub-20-nm technology node and enhances the analog and RF performance of complex integrated circuits without increasing the effective chip area. The performance of high-k SOI FinFET is analyzed in terms of I_{on}, I_{off}, I_{on}/I_{off}, SS (subthreshold slope), A_V (intrinsic gain), g_m (transconductance), V_{EA} (early voltage), g_d (output conductance), C_{gs} (gate-source capacitance), C_{gd} (gate-drain capacitance), and f_T (cutoff frequency) performance parameters. Starting with the introduction, Sect. 2 describes reliability and flexibility approach of high-*k* SOI FinFET. Section 3 gives a detailed design consideration of SOI FinFET structure along with all its structural dimensions, doping concentration, materials involved, and models considered in the 3D simulation process. Section 4 introduces the performance exploration and investigation part of high-k SOI FinFET over a wide temperature range. Section 5 describes the practical aspects of SOI FinFET technology and Sect. 6 presents the conclusion.

3 SOI FinFET Design Consideration and Simulation Setup

The schematic diagram and cross-section view of high-*k* SOI FinFET structure used for simulation work are shown in Fig. 12.1a, b, respectively. The 3D simulation process is done for 20-nm channel length with high-k spacer region for a given SOI

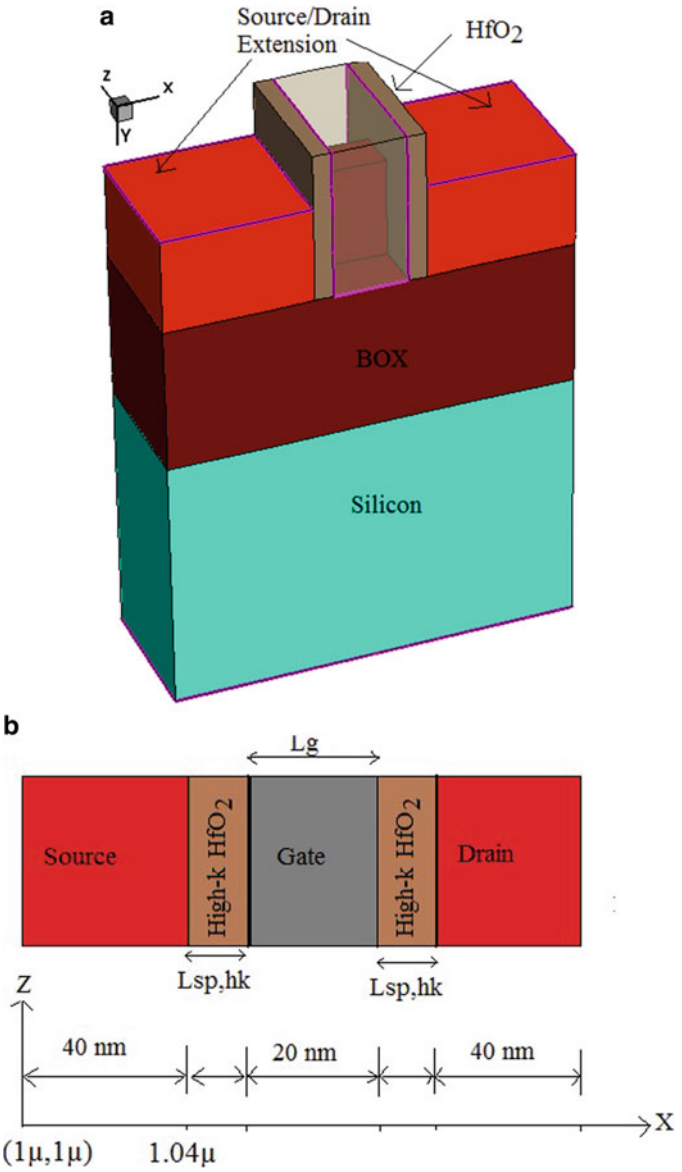

Fig. 12.1 (**a**) Device-D1 (high-k SOI FinFET) and (**b**) cross-section of device-D1

FinFET structure, and the source/drain region of this structure is heavily doped as n-type 1×10^{20} cm^{-3} and a lightly doped impurity p-type 1×10^{15} cm^{-3} is used for the channel region. The heavily doped impurities are used for the source/drain region to overcome the mobility degradation which is due to the coulomb charge scattering effect. The $W = (2H_{Fin} + W_{Fin})$ is the total effective width considered

Table 12.1 Dimensional parameters taken for 3D simulation of this work

Parameters	Descriptions (nm)	Device-D1 (nm)
W_{Fin}	Fin width	10
L_g	Gate channel length	20
H_{Fin}	Fin height	26
t_{ox}	Oxide thickness	0.9
BOX	Buried oxide thickness	40
L	Total length of device	110
Lsp,hk	High-k (HfO_2, k = 22) spacer length	5
$W_{s/d}$	Effective width of source/drain	40

for SOI FinFET structure because the effective current component across this width is the sum of all current components along the top surface and sidewalls of Fin at 20-nm node [35, 36]. Metal gate technology is used in SOI FinFET structure because it eliminates the poly gate depletion effect in all semiconductor devices. The length of source/drain is fixed to 40 nm with vertically placed source and drain contacts respectively. Device dimensional parameters of high-k spacer SOI FinFET considered for this 3D simulation work are given in Table 12.1.

Figure 12.1b has cross-section diagram of high-k SOI FinFET in which high-k spacer materials are used for the underlap region both at source and drain side. The use of high-k material in the underlap spacer region increases the I_{on} current or driving capability of the device by optimizing the GIBL (gate-induced barrier lowering) effect with significant reduction of off-state leakage current which results in high signal strength for communication systems. However, the device is compromised with RF performance in terms of cutoff frequency (f_T) due to increased effective gate fringing capacitances which results in slight degradation of circuit-level delay [37].

A lightly doped substrate with concentration of 1×10^{15} cm^{-3} is considered to minimize the random dopant's fluctuation effects in high-k SOI FinFET for detailed performance analysis [38].

The type of spacer and large value of an underlap region in SOI FinFET increase the distributed channel resistance or degradation in I_{on} current, facing the problem of controlling the doping profile. However, these problems are well tackled in [39–41] for MOSFETs. The high-k underlap region at drain side for MOSFETs and degradation in I_{on} can be improved further by introducing the high-k spacer in the underlap region without any significant degradation of output fringing capacitance [42]. So, proper value of high-k spacer region becomes the essential requirement of efficient SOI FinFET design.

The 3D simulation process of high-k SOI FinFET structure is done with the help of Sentaurus TCAD simulator tool [43]. Analog/RF performance of device-D1 is explored for underlap region of 5 nm [44–46] for temperature range of 200–450 K. The metal work function gate is 4.3 eV to have a desired value of threshold voltage. The equivalent oxide thickness (t_{0x}) is taken at a value of 0.9 nm [47–49] with supply voltage V_{DD} of 0.7 V and other simulation environmental

parameters are taken according to ITRS (International Technology Roadmap for Semiconductors) report [50]. The simulator validation for FinFET structure is investigated by previously reported results in the literature data of [49]. The models consideration for this reported work are velocity saturation model, field dependent and concentration-dependent mobility that consider the doping models [51]. The Lombardi mobility inversion CVT [52], Auger recombination models with Shockley–Read–Hall (SRH) [52–54], default carrier transport model, and quantum confinement are also considered in the simulation process. The smooth junction meshing and all biasing are done at wide temperature range (200–450 K) to evaluate the performance of SOI FinFET structure.

4 Performance Exploration and Investigation of SOI FinFET

In this section, performance of high-k SOI FinFET (device-D1) in terms of energy (CV^2), intrinsic delay (CV/I), energy-delay product (EDP), power dissipation (PD), subthreshold slope (SS), Q-Factor ($g_{m,max}$/SS), threshold voltage (V_{th}), maximum transconductance (g_{max}), I_{on}, I_{off}, I_{on}/I_{off} ratio, and the analog/RF performance parameters like A_V (intrinsic gain), g_m (transconductance), V_{EA} (early voltage), g_d (output conductance), C_{gs} (gate-source capacitance), C_{gd} (gate-drain capacitance), and f_T (cutoff frequency) are evaluated for various temperature ranges (200–450 K) for the low and high value of drain-source voltages, $V_{DS} = 0.05$ V and $V_{DS} = 0.7$ V, respectively. The temperature variation in the semiconductor device severely affects its electrical characteristic parameters like mobility, subthreshold slope, threshold voltage, leakage current, power dissipation, and intrinsic delay and becomes the major concern in the scaled technology design.

4.1 Electrostatic Performance Evaluation of SOI FinFET

Figure 12.2 shows some electrostatic-dependent performance characteristics of high-k SOI FinFET like SS, I_{on}, I_{off}, and I_{on}/I_{off} ratio with temperature variation at $V_{DS} = 0.05$ V and $V_{DS} = 0.7$ V. It is noticed from Fig. 12.2a that when increasing the temperature, the subthreshold performance of the device degraded due to reduction of I_{on} current both at low and high value of $V_{DS} = 0.05$ V and $V_{DS} = 0.7$ V, respectively. SS is an important parameter which describes the I_{off} leakage current and related with temperature as follows [55].

$$SS\,(mV/decade) \approx 60mV\frac{\mathrm{T}}{300K} \tag{12.1}$$

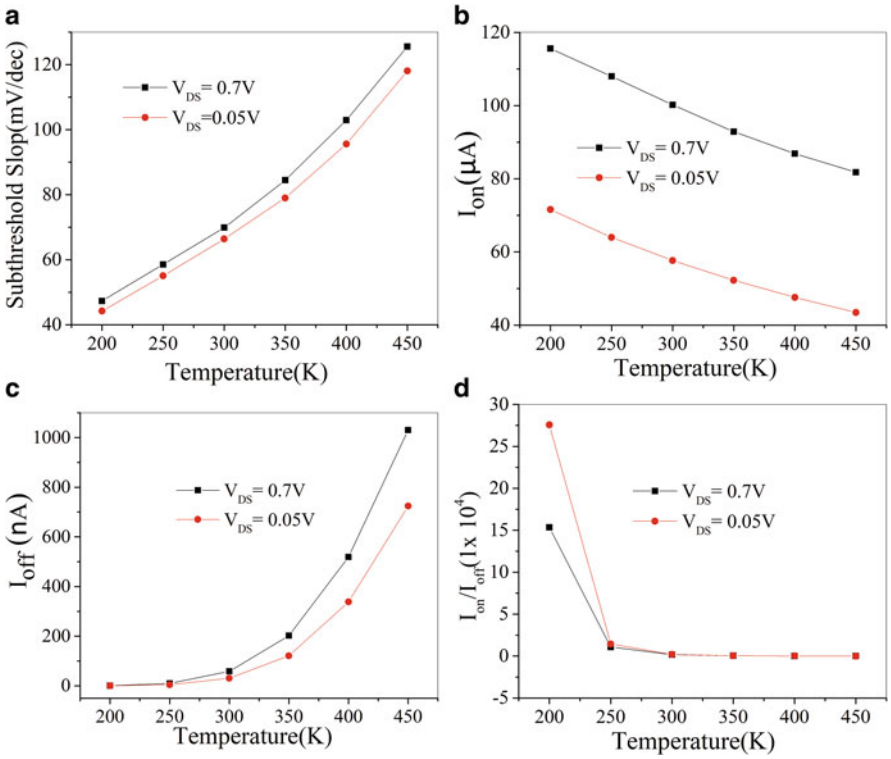

Fig. 12.2 (**a**) SS, (**b**) I_{on} current, (**c**) I_{off} current, and (**d**) I_{on}/I_{off} ratio versus temperature characteristics for high-k SOI FinFET at $V_{DS} = 0.05$ V and $V_{DS} = 0.7$ V

According to Eq. (12.1), at low-temperature range (below 250 K), there is much reduction of SS value that directly reflects the off-state leakage current of the semiconductor device and improvement in I_{off} at lower-temperature range is shown in Fig. 12.2c. So, at low temperature (below 250 K), there is big improvement in I_{on}/I_{off} ratio due to significant reduction of I_{off} current because of the low value of the subthreshold slope (SS) as shown in Fig. 12.2d. High value of I_{on}/I_{off} and low value of I_{off} are desirable for high-speed switching applications.

4.2 Analog Performance Evaluation of SOI FinFET

The I_D (drain current) and g_m (transconductance) against V_{GS} (gate-source) voltage characteristics for various values of temperature range (200–450 K) at $V_{DS} = 0.05$ V and $V_{DS} = 0.7$ V for high-k SOI FinFET are explored in Fig. 12.3a, b, respectively. The drain current as a function of mobility (μ) and threshold voltage (V_{th}) is as follows [56].

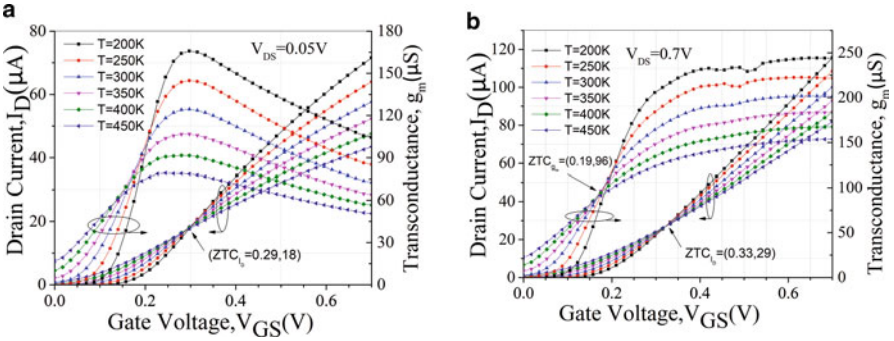

Fig. 12.3 I_D and g_m versus V_{GS} characteristics of high-k SOI FinFET with temperature variation at (**a**) $V_{DS} = 0.05$ V and (**b**) $V_{DS} = 0.7$ V

$$I_D(T) \propto \mu(T)\,[V_{GS} - V_{th}(T)] \tag{12.2}$$

The mobility term and threshold voltage both are temperature-dependent parameters. The carrier mobility follows the relationship as $\mu(T) = \mu(T_0)(T/T_0)^{-n}$ where the "n" exponent varies at 1.6–2.4 [55]. The threshold voltage of SOI devices follows the inverse temperature characteristics and decreases with increase of temperature [57]. On increasing the temperature, mobility of charge carrier also decreases for SOI FinFET due to lattice scattering effects. So, $\mu(T)$ and $[V_{GS} - V_{th}(T)]$ terms of drain current shown in Eq. (12.2) will show the inverse nature with temperature variation. Upon increasing the temperature, the $\mu(T)$ value decreases which tries to force drain current decrease while the value of $[V_{GS} - V_{th}(T)]$ term increases which tries to force drain current increases. So on increasing the gate bias point, these two effects compensated at a fixed value of the gate to the source voltage (V_{GS}) and the effect of temperature variation at this point can be neglected for evaluating the performance of the SOI device. This fixed value of V_{GS} bias is known as ZTC (zero temperature coefficient) point.

As we observe from the I_D-V_{GS} characteristics shown in Fig. 12.3 that for low and high V_{DS} value below the ZTC_{I_D} point, drain current (I_D) increases with increasing temperature, while above the ZTC_{I_D} point, the nature of drain current becomes opposite. As $V_{GS} < V_{th}$, current mainly flows by diffusion process. So, below the ZTC_{I_D} point, $[V_{GS} - V_{th}(T)]$ becomes the dominating factor as compared to $\mu(T)$ due to more degradation of threshold at high value of temperature. So, drain current increases with increase of temperature value. As $V_{GS} > V_{th}$, the dominating flow of current is by drift process. So, above the ZTC_{I_D} point, $\mu(T)$ decreases with increase of temperature due to more lattice scattering effect and becomes the dominating factor for evaluating the drain current. So, drain current decreases with increase of temperature value.

In Fig. 12.3b, at $V_{DS} = 0.7$ V, we extract the two ZTC points for drain bias and transconductance bias ZTC_{I_D} and ZTC_{g_m}, respectively. Both these ZTC points are important figures of merit for analog circuit design at various temperature values.

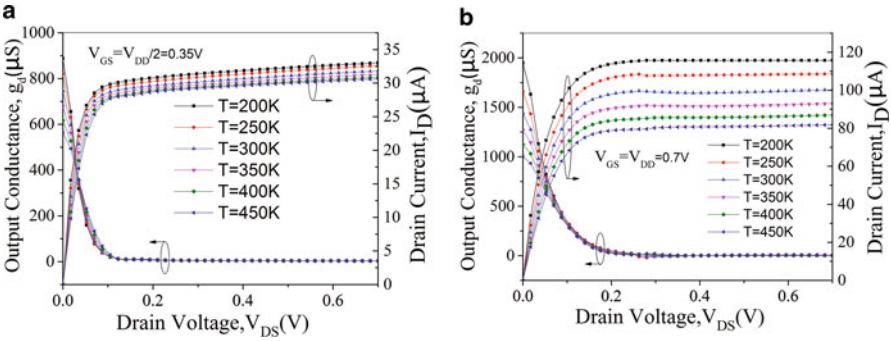

Fig. 12.4 I_D and g_d versus V_{DS} characteristics of high-*k* SOI FinFET with temperature variation at (**a**) $V_{GS} = 0.35$ V and (**b**) $V_{GS} = 0.7$ V

The ZTC_{I_D} bias point gives the information about constant DC current, while ZTC_{g_m} bias point is used to achieve stable circuit parameters for analog design. Both bias points are affected by the process variation. So, ZTC points are chosen according to the applications. It is noticed from Fig. 12.3b that the extracted value of $ZTC_{g_m} = 0.19V$ and $ZTC_{I_D} = 0.33V$ at $V_{DS} = 0.7$ V. So, below 0.19 V the transconductance (g_m) increases due to degradation of V_{th} upon increasing the temperature, while above 0.19 V the g_m decreases due to reduction of channel mobility by lattice scattering effects upon increasing the temperature.

The output performance characteristics of high-*k* SOI FinFET, I_D (drain current) and g_d (output conductance) versus V_{DS} (drain to source) voltage at $V_{GS} = 0.35$ V and $V_{GS} = 0.7$ V, are shown in Fig. 12.4a, b, respectively. It is noticed from Fig. 12.4a, b that above the ZTC_{I_D} point, drain current decreases upon increasing the temperature due to the discussed $\mu(T)$ effect with temperature and the opposite nature of the current generated below the ZTC_{I_D}. Low value of g_d is required to improve the intrinsic gain (g_m/g_d) of SOI FinFET device. Further g_d is less sensitive to temperature at $V_{GS} = 0.35$ V compared to $V_{GS} = 0.7$ V at low drain bias point and it can be analyzed from Fig. 12.4.

4.3 RF Performance Evaluation of SOI FinFET

Figure 12.5a, b shows the C_{gs} and C_{gd} capacitances versus V_{GS} characteristics for high-*k* SOI FinFET at $V_{DS} = 0.05$ V and $V_{DS} = 0.7$ V, respectively. From Fig. 12.5a, it is noticed that at $V_{DS} = 0.05$ V, ZTC for C_{gs} $\left(ZTC_{C_{gs}}\right)$ has a value of 0.192 V and 0.33 V for C_{gd} (ZTC_{Cgd}). Both C_{gs} and C_{gd} increase with increasing temperature below $ZTC_{C_{gs}}$ point, whereas the opposite nature of C_{gs} occurs above the $ZTC_{C_{gs}}$ point. At $V_{DS} = 0.7$ V, there is much variation of C_{gs} and C_{gd} characteristics with V_{GS} over the wide temperature range and no significant ZTC point generated for both C_{gs} and C_{gd} values. This much variation in C_{gs} and C_{gd} characteristics is due

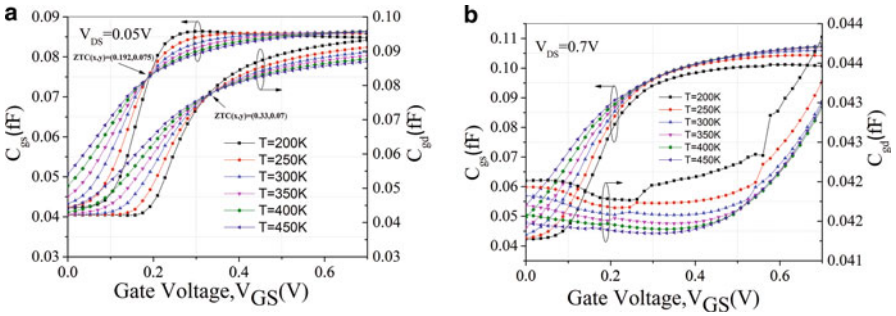

Fig. 12.5 Capacitance C_{gs} and C_{gd} characteristics of high-k SOI FinFET with temperature variation at (**a**) $V_{DS} = 0.05$ V and (**b**) $V_{DS} = 0.7$ V, respectively

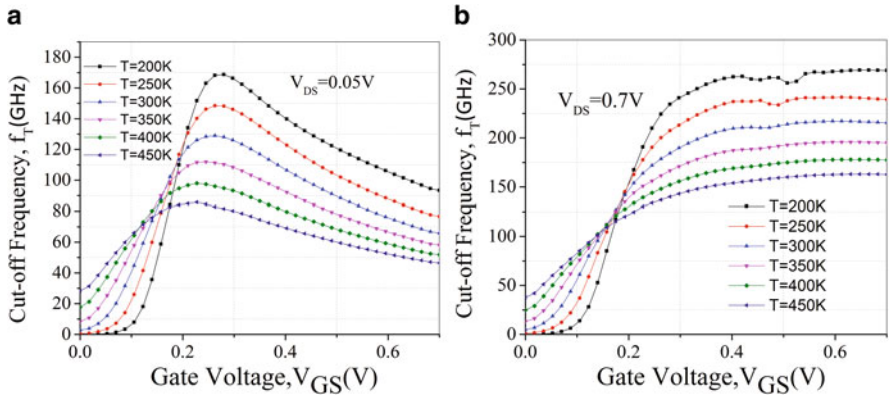

Fig. 12.6 Cutoff frequency (f_T) versus V_{GS} characteristics with temperature variation at (**a**) $V_{DS} = 0.05$ V and (**b**) $V_{DS} = 0.7$ V

to the heating effect generated at drain to source voltage, $V_{DS} = 0.7$ V. So, proper drain bias is important for high-*k* SOI FinFET to have more thermal stable systems.

Cutoff frequency $f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})}$ is a desirable parameter for evaluating the RF performance of SOI FinFET. The f_T versus V_{GS} characteristics with temperature variation at $V_{DS} = 0.05$ V and $V_{DS} = 0.7$ V are shown in Fig. 12.6a, b, respectively. It is noticed from Fig. 12.6 that in the weak inversion region, improvement in cutoff frequency (f_T) occurs on increasing the temperature, while the opposite nature of cutoff frequency (f_T) occurs in the strong inversion region. At $V_{DS} = 0.7$ V, above the ZTC point (0.175 V) of f_T, improvement in f_T occurs for low value of temperature due to steep improvement of charge carrier mobility. To have stable RF performance, SOI FinFET structure can be biased at ZTC point which has the value of $V_{GS} = 0.175$ V.

Table 12.2 shows some extracted performance parameters for high-k SOI FinFET for a wide range of temperature at $V_{DS} = 0.7$ V. From the extracted results of Table 12.2, it is noticed that there is improvement in intrinsic delay (CV/I), energy-

Table 12.2 Extracted performance metrics of high-k SOI FinFET for various temperatures at $V_{DS} = 0.7$ V

Temperature (K)	Energy (CV^2) (J) $\times 10^{-17}$	Delay (CV/I) (ps)	EDP (J) $\times 10^{-29}$	PD ($I_{off} * V_{DD}$) (nW)	SS (mV/decade)	I_{on}/I_{off}	V_{th}	$g_{m,max}$ (S) $\times 10^{-4}$	Q-factor ($g_{m,max}$/SS) $\times 10^{-6}$
200	6.80	0.840	5.71	0.528	47.318	1.53×10^5	0.226	2.44	5.16
250	6.89	0.912	6.29	7.05	58.566	1.07×10^4	0.210	2.22	3.79
300	6.91	0.985	6.80	41.0	69.891	1.71×10^3	0.203	2.02	2.89
350	6.90	1.06	7.32	141	84.465	4.60×10^2	0.193	1.83	2.17
400	6.89	1.13	7.81	364	102.959	1.67×10^2	0.181	1.67	1.62
450	6.88	1.20	8.27	721	125.584	7.94×10^1	0.168	1.54	1.23

delay product (EDP), off-state power dissipation ($PD = I_{off^*}V_{DD}$), SS value, $g_{m,max}$ (S), I_{on}/I_{off}, and Q-factor ($g_{m,max}/SS$) for low value of temperature. Q-factor and EDP are important figures of merit for circuit applications and these parameters improved due to low value of SS and intrinsic delay at low temperature. The threshold voltage can also be analyzed by extracted results and it decreases with increasing the temperature.

4.4 Extraction of Electrostatic and Analog/RF Performance Parameters

Analog/RF performance parameters like g_m, g_d, A_v ($g_m/g_{d)}$, V_{EA}, C_{gg}, C_{gs}, C_{gd}, and f_T for high-k SOI FinFET for a wide temperature range (200–450 K) are also evaluated at $V_{DS} = 0.7$ V and shown in Table 12.3. It is noticed from Table 12.3 that there is significant improvement in A_v and much improvement in f_T at lower value of temperature. This improvement is due to increased value of g_m at lower-temperature range.

5 Practical Aspects of SOI FinFET Technology

Today, the world economy directly or indirectly depends on semiconductor industries. In early days, consumer products like mobile phones, cars, watches, and even refrigerators have more power as compared to present products. Now, we are moving fast towards a more connected world, a world of computer networks, Internet of Things and cyber security applications where our consumer appliances are able to communicate each other with more efficient use of energy and other resources with less cost. This is being possible only due to improvement in basic unit (transistor) of chip industries. More numbers of transistors integrated into the chip increase the more functionality of consumer products like mobile phones, tablets, computer peripherals, industrial automation equipment, military, and security applications. More transistors on a single chip can be done with smaller-size transistor with less power consumption, and this can be done by FinFET technology. Chips can perform more and more tasks while becoming smaller at the same time, thus enabling their use in countless devices that improves our lives in multiple ways. So, with this new innovated technology, more advance featured electronic gadgets and industrial automated equipment can be implemented at lower cost in the industries which indirectly reflect the economy of a country.

Table 12.3 Extracted analog/RF performance parameters for high-k SOI FinFET for various temperature values at $V_{DS} = 0.7$ V

Analog/RF extracted performance metrics	Temperature = 200 K	Temperature = 250 K	Temperature = 300 K	Temperature = 350 K	Temperature = 400 K	Temperature = 450 K
g_m (μS)	222	201	179	160	145	132
g_d (μS)	3.25	3.50	3.33	3.17	3.05	2.97
A_V (dB)	36.67	35.18	34.60	34.06	33.51	32.94
V_{EA} (0V)	10.1	9.30	9.56	9.85	10.1	10.3
C_{gg} (aF)	139	141	141	141	141	140
C_{gs} (aF)	96.7	99.0	99.4	99.4	99.3	99.1
C_{gd} (aF)	42.0	41.7	41.6	41.5	41.4	41.4
f_T (GHz)	250	200	202	180	160	149

6 Conclusion

In this chapter, high-*k* SOI FinFET is explored in terms of performance parameters like intrinsic delay (CV/I), energy-delay product (EDP), off-state power dissipation (PD = $I_{off*}V_{DD}$), SS value, $g_{m,max}$ (S), I_{on}/I_{off}, Q-factor ($g_{m,max}/SS$), and analog/RF parameters like g_m, g_d, A_v (g_m/g_d), V_{EA}, C_{gg}, C_{gs}, C_{gd}, and f_T for a wide temperature range (200–450 K). The analysis is done on the basis of zero temperature coefficient (ZTC) for drain current and transconductance bias point for low- and high-temperature range. Above and below the ZTC point, SOI FinFET has an opposite nature. So, it is concluded that with the help of ZTC point, SOI FinFET can be biased for DC, analog, and RF applications for a wide temperature range and the effect of temperature variation on the performance of device can be minimized at ZTC bias point. So, effective use of FinFET for computer networks, integrated circuits, and cyber security applications improves the performance of chip industries which reflect the economy and business of a country.

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