Design of a 200-nW 0.8-V Voltage Reference Circuit in All-CMOS Technology

Jianhai Yu(✉) and Hui Guo

Wuzhou University, Wuzhou 543002, China
40802622@qq.com

Abstract. Based on the negative temperature characteristics of threshold voltage and positive temperature characteristics of a multiple of thermal voltage, adding them with proper weight coefficient A voltage reference circuit was proposed with a zero temperature coefficient (TC). The device consists of pure MOSFET operated in subthreshold region and uses no resistors and bipolar transistors. The triple-branch current reference structure is adopted for independence of supply voltage instead of cascade structure and embedded operational amplifier structure with the merit of chip area and power consumption. Simulation results showed that based on standard CMOS 0.18 um process, the circuit can operate at 0.75 V supply voltage with the output voltage only 563 mV. The TC of the voltage was 17.5 ppm/°C in a range from −40 °C–125 °C. The line sensitivity was 569.5 ppm/V in a supply voltage range of 1.2 V–1.8 V, and the power supply rejection ratio (PSRR) was 66.5 dB at 100 Hz. The power dissipation was only 187.4 nW.

Keywords: Low power · All-CMOS · Subthreshold · Current reference

1 Introduction

Voltage reference and current reference are the important part in analog and mixed signal integrated circuits, e.g. sensors, portable mobile devices and biomedical chip [1]. It can provide reference for other blocks so its characteristics directly affect the performance of all the system [2]. Traditional bandgap reference (BGR) circuit [3, 4] got the zero TC by weighting the negative temperature characteristics of base-emitter voltage of NPN bipolar transistor and positive temperature characteristics of thermal voltage [5], which produces a voltage that is basically independent of power supply voltage, process and temperature [6]. While the traditional circuit invoked operation amplifier structure or cascade structure to stabilize the voltage for improving the PSRR with the drawback of power dissipation and chip area, and also the noise and speed of the op-amp can affect the output voltage [7].

To solve above problems, a low power voltage reference circuit is proposed in this paper with all the MOSFETs working in the subthreshold region. To provide bias for the voltage reference a triple-branch current reference is developed with high PSRR. The circuit consists of all-CMOS devices without resistors and bipolar transistors so as to save the chip area and power consumption. Simulation results shows the benefits of the circuit.

M. Jia et al. (Eds.): WiSATS 2019, LNICST 281, pp. 120–130, 2019.
https://doi.org/10.1007/978-3-030-19156-6_12

2 A Traditional Current Source

A typical circuit for generating the bias current independent of the power voltage is shown in Fig. 1 [7]. When the circuit is powered on, M5 provides the access from VDD to the ground through M3 and M1. The M5 can be turned off after the circuit was started up in order to avoid degenerate on the condition that $V_{TH1} + V_{TH5} + |V_{TH3}| < V_{DD}$ and $V_{GS1} + V_{TH5} + |V_{GS3}| > V_{DD}$. The output current of the circuit can be expressed as

$$I_2 = \frac{2}{u_n C_{ox}(\mathrm{W/L})_n} \frac{1}{R_S} \left(1 - \frac{1}{\sqrt{K}}\right)^2 \tag{1}$$

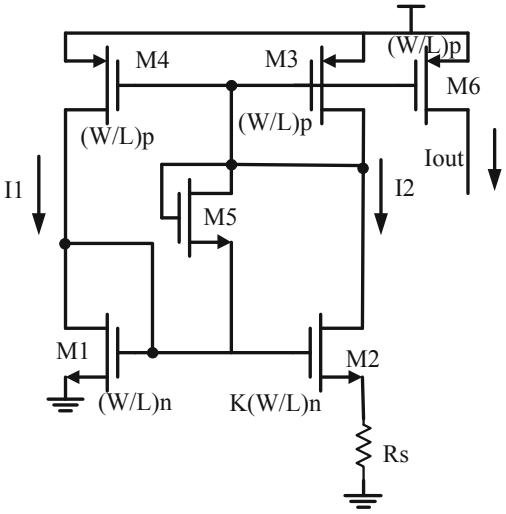


Fig. 1. Traditional supply voltage independent current source

Thus the reference current independent of the supply voltage is produced. In this block, with the fluctuating of power supply voltage, the drain voltages of M1 and M2 will change in opposite direction. So the transistors M3, M4, M1 and M2 constitute a positive feedback, and resistor Rs acts as the negative feedback of the circuit. On the whole this circuit presents a weak positive feedback loop, so the PSRR of the block will be relatively poor. In order to weaken the sensitivity of the reference current to the power supply voltage, a triple-branch current reference structure was proposed in literature [8] and [9], which constitute a negative feedback loop. In this circuit resistors was used to control the bias current, so the silicon area would be increased in order to get nanoampere current. In standard CMOS technology, not only the resistor model may be unavailable or unreliable, but also the resistors increase susceptibility of the reference to substrate noise coupling [10].

3 Improved Triple-Branch Current Reference

A novel current reference circuit which can increase the PSRR and weaken the sensitivity of the temperature is shown in Fig. 2. The triple-branch structure was adopted and the negative feedback loop was formed to restrain the variation of the power supply. When the power supply voltage V_{DD} increases, the voltage V_X decreases at the same time, and the voltage V_B increases under the operation of NM2 as common-source amplifier. For the same reason, under the action of common-source NM1, the voltage of A point drops consequently. Thus, a negative feedback loop $V_X \rightarrow V_B \rightarrow V_A \rightarrow V_X$ is formed, so the PSRR of the circuit together with linear sensitivity are relatively high. When the voltage at X point increases, the current of *I1*, *I2*, *Iout*, *Iref* decreases, $V_Y = (I1 + I2 + Iout)R_{NM5} + (I1 + I2 + Iout + Iref)R_{NM6}$ the voltage at Y point decreases rapidly, which makes the voltage at X point drop rapidly. The source of NM2 is connected with the drain of NM5 tube, which forms faster negative feedback loop. The resistor which control the magnitude of the reference current is replaced by NM5 that operates in the diode region. The NM5 gate-voltage is biased by the drain voltage of diode-connected NM4, the gate-source voltage of NM4 has a negative TC, and the drain-source voltage of NM5 has the positive TC, so the voltage of point Q which determines the current I2 can be weighted to zero TC. NM6 is used as big resistor to make the current stable. Such a structure can weaken the influence of temperature in the end.

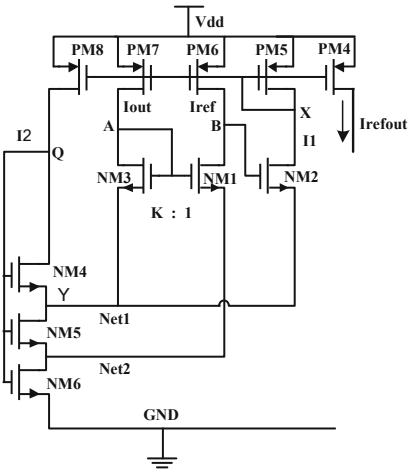


Fig. 2. Proposed current source subcircuit

In order to reduce the power consumption of the circuit, MOSFET is generally used to work in the subthreshold region in the nanoampere current reference. When $V_{GS} \approx V_{TH}$ or V_{GS} slightly smaller than V_{TH}, the current is expressed as follows [7]:

$$I_D = SI_0 \exp\left(\frac{V_{GS} - V_{TH}}{\zeta V_T}\right)\left[1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right] \tag{2}$$

S is the aspect ratio of the transistor, I_0 is the characteristic current, ξ represents the subthreshold slope factor, C_{ox} is the gate-oxide capacitance, $V_T = KT/q$ is the thermal voltage, K is the Boltzmann constant, T is the absolute temperature, q is the elementary charge *Vth* is the threshold voltage of a MOSFET [11]. For $V_{DS} > 0.1$ V, current Id is almost independent of V_{DS} and given by

$$I_D = SI_0 \exp\left(\frac{V_{GS} - V_{TH}}{\xi V_T}\right) \tag{3}$$

NM1, NM2 and NM3 operate in the subthreshold region. According to the equation above, the current of NM1 and NM3 can be obtained:

$$I_{\text{out}} = S_{NM3} I_0 \exp\left(\frac{V_{GS,NM3} - V_{\text{th}}}{\zeta V_T}\right) \tag{4}$$

$$I_{\text{ref}} = S_{NM1} I_0 \exp\left(\frac{V_{GS,NM1} - V_{\text{th}}}{\zeta V_T}\right) \tag{5}$$

PM6 and PM7 constitute a pair of current mirror structures, PM6 and PM7 have the same size, so $I_{out} = I_{ref}$, the aspect ratios of NM3 is K times that of NM1, that is $S_{\text{NM3}} = KS_{NM1}$, we get the formula:

$$I_{out} = KS_{NM1} I_0 \exp\left(\frac{V_{GS,NM3} - V_{th}}{\zeta V_T}\right) \tag{6}$$

According to the formula (4) and (6) can be obtained:

$$\ln K = \frac{V_{GS,NM1} - V_{GS,NM3}}{\zeta V_T} = \frac{I_{\text{ref}} R_{NM5}}{\zeta V_T} \tag{7}$$

transistor NM5 operates in deep-triode region, so its resistance is given by

$$R_{NM5} = \frac{1}{S_{NM5} \mu C_{OX}\left(V_{GS,NM5} - V_{\text{th}}\right)} \tag{8}$$

So the current reference can by written as

$$I_{\text{ref}} = \zeta V_T \ln(K) \bullet S_{NM5} \mu C_{OX}\left(V_{GS,NM5} - V_{\text{th}}\right) \tag{9}$$

It can be seen from the above equation the output current depends on the aspect ratio of NM5. The voltage of Q point is easy to change with the temperature, and the current of I2 will also change accordingly. It can be obtained I_{out}, the voltage I_{ref}

changes with the temperature. Only if the voltage at the Q point is stable, the current I_{ref} not change with the temperature be produced. According to the formula (6) and (7), we get:

$$I_{out} = I_{ref}\frac{S_{PM7}}{S_{PM6}} \tag{10}$$

$$V_{DS,NM5} = V_{net1} - V_{net2} = \xi V_T \ln\left(\frac{S_{NM3}}{S_{NM1}}\right) \tag{11}$$

$$V_Q = V_{GS4} + V_{DS,NM5} + V_{DS6} \tag{12}$$

$$V_Q = \xi V_T \ln\left(\frac{I_2}{S_{NM4}I_0}\right) + V_{th} + \xi V_T \ln\left(\frac{S_{NM3}}{S_{NM1}}\right) + V_{DS6} \tag{13}$$

$$V_Q = \xi V_T \ln\left(\frac{I_2 K}{S_{NM4}I_0}\right) + V_{th} + V_{DS6} \tag{14}$$

From Eq. (14) it can be seen that the first term is the multiple of the thermal voltage which has the positive TC, and the second term is the threshold voltage of MOSFET which has a negative TC. Properly weighting, the V_Q with zero TC can be derived, and the temperature effect on the reference current is weakened.

At the corner of ttssff, the output current varies versus supply voltage is shown in Fig. 3 and the temperature characteristic of output current is shown in Fig. 4. It can be seen that output current has slightly positive *TC*, and it can work normally when power supply is 0.75 V.

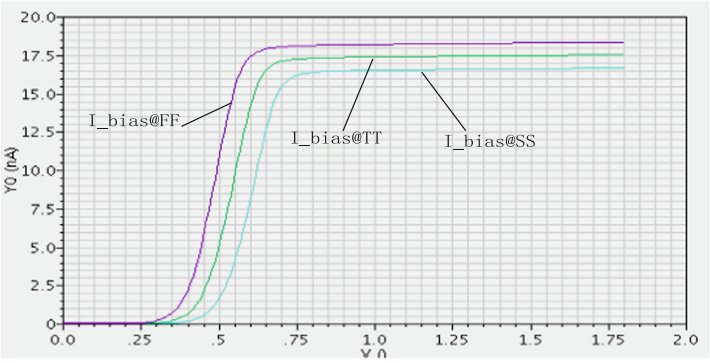


Fig. 3. Output current versus supply voltage under different corner

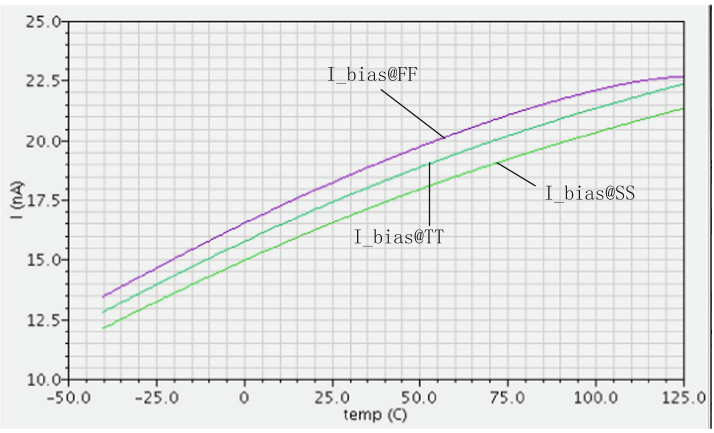


Fig. 4. Output current versus temperature under different corner

4 Voltage Reference Circuit

The bias voltage circuit is shown in Fig. 5. PM4, PM3, PM2, PM1 have the same aspect ratio and all work in saturation region in order to guarantee the same drain current (I_P) of them. It can be seen that the gate-source voltage (from V_{GS8} to V_{GS15}) of the transistors form a closed loop, and the current in M9, M11 and M13 are $4I_P$, $3I_P$ and $2I_P$ respectively. Therefore, we find that output voltage V_{REF} of the circuit is given by

$$V_{ref} = V_{GS9} - V_{GS8} + V_{GS11} - V_{GS10} + V_{GS13} - V_{GS12} + V_{GS15} \tag{15}$$

according to Eq. (3)

$$V_{GS} = V_{TH} + \xi V_T \ln\left(\frac{I_D}{SI_0}\right), \ (I_D = aIp) \tag{16}$$

And Eq. (15) can be rewritten as:

$$\begin{aligned} V_{ref} &= V_{GS9} + \xi V_T \ln\left(\frac{6S_8S_{10}S_{12}}{S_{11}S_{13}S_{15}}\right) = V_{GS9} + \xi V_T \ln(6K^3) \\ &= V_{TH} + \xi V_T \ln\left(\frac{4Ip}{S_9I_0}\right) + \xi V_T \ln\left(6K^3\right) \end{aligned} \tag{17}$$

where we assumed that the mismatch between the threshold voltage of the transistors can be ignored. Equation (17) shows that V_{REF} can be expressed as a sum of the gate-source voltage V_{GS9} and thermal voltage V_T scaled by the transistor sizes. Because V_{TH} has a negative TC and V_T has a positive TC, output voltage V_{REF} with a zero TC can be obtained by adjusting the size of the transistors.

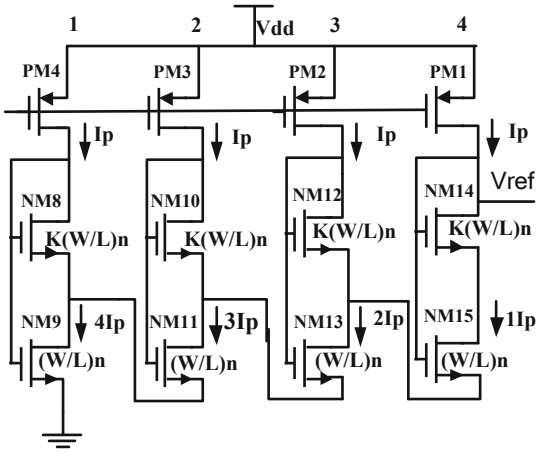


Fig. 5. The proposed zero TC voltage circuit

The entire circuit is illustrated in Fig. 6. It is composed of three blocks, which are start-up circuit, current source subcircuit and bias voltage subcircuit. A start-up circuit is used to avoid the stable state in the zero bias condition. When the power is on, PM10 works in the conducting state. *Iin* injects into the main circuit. At the same time, PM9 is on and MOS capacitor NM7 is charged, the voltage of PM10 gate increases gradually. At last PM10 cuts off and the start-up circuit separates from the main circuit.

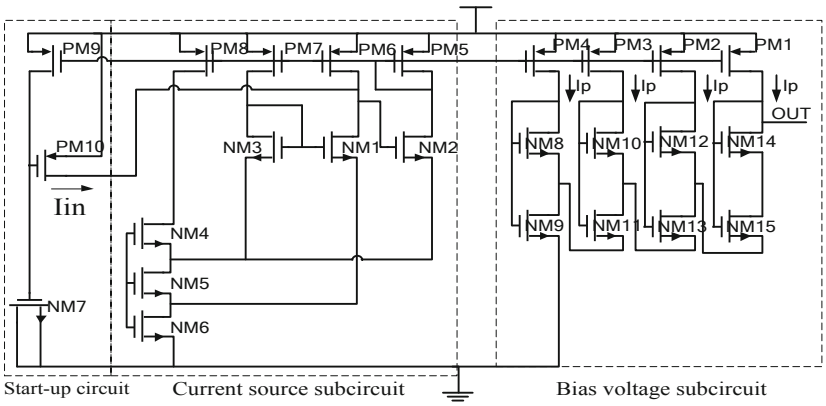
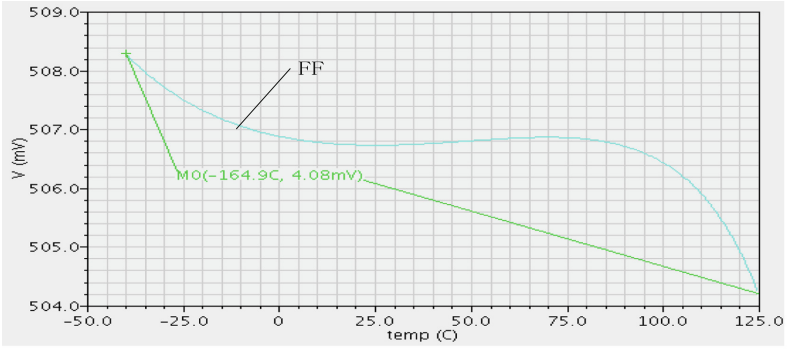


Fig. 6. The whole schematic of our voltage reference circuit

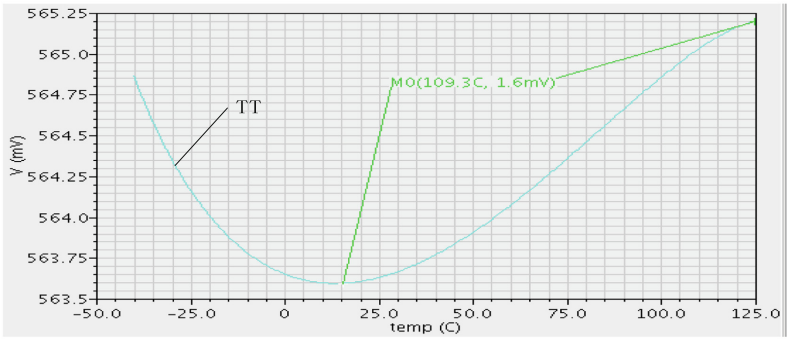
5 Simulation Results and Comparison

The performance of our proposed circuit is verified with the aid of SPECTRE simulation using a set of 0.18 um standard CMOS press with 1.8 V power supply.

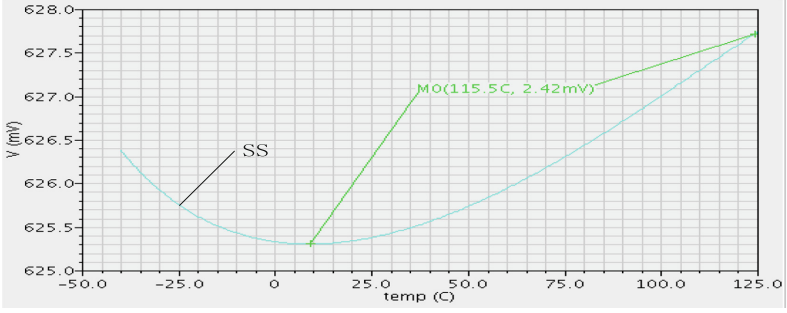
The TC of output voltage under different corner are shown in Fig. 7 respectively. It can be seen under corner of FF, the TC is 48.88 ppm/°C, with the mean output voltage 506.242 mV; under the corner of TT, the TC is 17.25 ppm/°C, with the mean output voltage 564.39 mV; under the SS corner, the TC is 23.48 ppm/°C, with the output voltage 626.516 mV. It is easy to see that output voltage varies greatly with different corner. Because the threshold voltage changes evidently under different corner, and output voltage of proposed circuit under zero TC is equal to the threshold voltage of the MOSFET at 0 K temperature. So more accurate process should be used in order to achieve excellent reference.



A FF corner



B TT corner



C SS corner

Fig. 7. Output voltage VREF as a function of temperature under various corner

The output voltage exhibits good power independence. Figure 8 shows output voltage V_{REF} at room temperature as a function of supply voltage under different corner. The circuit operates properly when supply voltage is higher than 0.75 V. The line sensitivity is 596.5 ppm/V in the power range of 1.2 V to 1.8 V under TT corner. Figure 9 shows the PSRR at room temperature with 1.8 V power supply. The PSRR is −66 dB@100 Hz, and the worst is −29 dB@63 kHz. At different corner, maximum deviation is less than 2 dB. Thus the voltage reference which is almost independent of temperature and supply voltage is achieved.

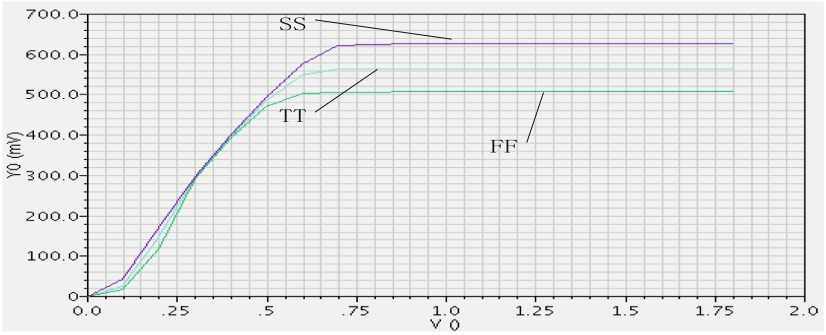


Fig. 8. Output voltage versus supply voltage

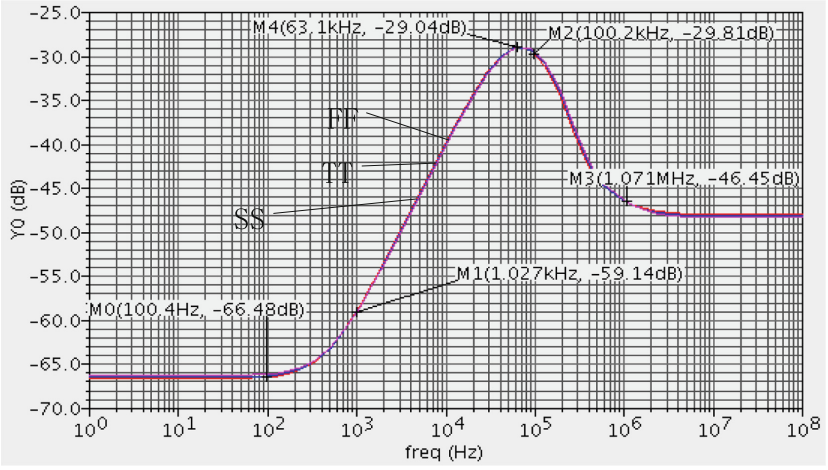


Fig. 9. PSRR of the proposed reference voltage source

The noise characteristic is shown in Fig. 10. It can be seen that the noise is relatively larger in the low frequency band, about 4 uV/sqrt(Hz)@80 Hz. The circuit noise is mainly the flicker noise of MOSFET, which can be reduced by increasing size of MOSFET. It is easy to see the noise of output voltage is not affected under different corner.

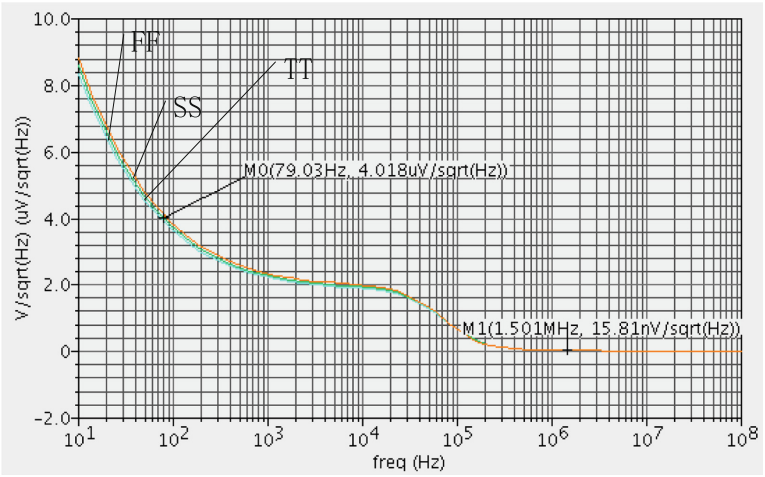


Fig. 10. Output noise versus frequency

Table 1 summarizes the characteristics of our circuit in comparison with other triple-branch structure CMOS voltage references reported in [7, 8, 12]. Our device is comparable to other circuits in PSRR, line sensitivity, and it is superior to other in TC and power consumption. Our circuit gives new improvement to the triple-branch structure circuits, so it is useful as a voltage reference for low power design.

Table 1. Comparison of reported low power CMOS voltage reference circuits

	This work	[7]	[8]	[12]
Process	0.18 um, CMOS	0.5 um, CMOS	0.18 um, CMOS	0.35 um, CMOS
Temperature range (°C)	−40–125	−40–130	−40–100	−20–80
VDD	0.75–1.8 V	2–6 V	0.7–3 V	1.4–3 V
V_{ref}	563.5 mV	1.2–3.5 V	700 mV	745 mV
Power	187.4 nW	*N.A.*	1.5 uW	0.3 uW (@.4 V)
TC (ppm/°C)	17.25	20	80	7
Line sensitivity (ppm/V)	569.5	*N.A.*	*N.A.*	20
PSRR@100 Hz	−66.5 dB	−50 dB@1 kHz	−62 dB	45 dB
Noise@80 Hz	4 uV/sqrt (Hz)	*N.A.*	4.9 uV/sqrt (Hz)	*N.A.*

6 Conclusions

A novel ultra-low power voltage reference circuit consist of all-CMOS transistors is developed in this paper. The circuit adopts improved triple-branch current reference structure instead of the traditional embedded operational amplifier and cascade structure. In addition, the circuit works at the subthreshold region in order to reduce the power consumption. The power rejection ratio and linearity of the circuit are improved while the power consumption and chip area are greatly reduced. Using a 0.18 um standard process, Simulation results show that power supply voltage can be as low as 0.75 V, the TC is about 17.5 ppm/°C, the linear sensitivity between 1.2 V to 1.8 V is 569.5 ppm/V, the output voltage is about 563.5 mV, and the PSRR is about −66.5 dB@100 Hz, the power consumption of the whole circuit is only 187.4 nW.

Acknowledgement. 1. Project supported by the National Natural Science Foundation of China (Grant No. 61562074).

2. Project supported by the Guangxi University Science and Technology Research Project (Grant No. KY2015ZD123).

3. Guangxi Innovation Driven Development Special Fund Project.

References

1. Lee, E.K.F.: Low voltage CMOS bandgap references with temperature compensated reference current output. In: IEEE International Symposium on Circuits and Systems, pp. 1643–1646. IEEE (2010)
2. Yue, M.: A 46.468 μW low-power bandgap voltage reference. In: IEEE International Conference on Computer Science and Information Technology, pp. 256–258. IEEE (2010)
3. Hua, L., Lüjian, Yadong, J.: A curvature-compensated CMOS bandgap voltage reference for high precision applications. Microelectronics **39**(1), 38–41 (2009)
4. Wang, N., Wei, L.: A low-power high PSRR OMOS bandgap voltage reference. Microelectronics **34**(3), 330–333 (2004)
5. Zhou, Q., et al.: High-PSRR high-order curvature-compensated CMOS bandgap voltage reference. J. Harbin Inst. Technol. **5**, 116–124 (2015)
6. Wadhwa, S.K., Chaudhry, N.: High accuracy, multi-output bandgap reference circuit in 16 nm FinFet. In: International Conference on VLSI Design and 2017, International Conference on Embedded Systems, pp. 259–262. IEEE (2017)
7. Razavi, B.: Design of Analog CMOS Integrated Circuits. Xi'an Jiaotong University Press (2003)
8. Yi, W., He, L., Xiaolang, A.Y.: A 30 nA temperature-independent CMOS current reference and its application in an LDO. Chin. J. Semicond. **27**(9), 1657–1662 (2006)
9. Xu, Y., Hu, W.: Design of a novel All-CMOS low power voltage reference source. Microelectronics **43**(6), 742–746 (2013)
10. Buck, A.E., et al.: A CMOS bandgap reference without resistors. IEEE J. Solid-State Circ. **37**(1), 81–83 (2002)
11. Wang, A., Calhoun, B.H., Chandrakasan, A.P.: Sub-threshold Design for Ultra Low-Power Systems. Series on Integrated Circuits & Systems. Springer, Heidelberg (2006). https://doi.org/10.1007/978-0-387-34501-7
12. Ueno, K., et al.: A 300 nW, 15 ppm/°C, 20 ppm/V CMOS voltage reference circuit consisting of subthreshold MOSFETs. IEEE J. Solid-State Circ. **44**(7), 2047–2054 (2009)