# Three Dimensional Simulation of Filling Process for Stacked-Chip Scale Packages

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**Abstract** Encapsulation is one of the key processes in electronic packaging in order to protect the integrated circuit chips from environmental and mechanical damages. The most obvious choice for the encapsulation process is transfer moulding due to its capability to mould small parts with complex features. An electronic package that employs transfer moulding is Stacked-Chip Scale Package (S-CSP). However, a computer simulation is one of the tools that could be used to simulate and predict the mould process. It is highly desirable in order to avoid the typical time-consuming procedure of mould design and process optimization by trial and error. In this paper, a fully three-dimensional analysis to predict the transfer moulding process of S-CSP encapsulation using a finite volume method (FVM) based software, FLUENT is presented. The proposed FVM simulation model is built and meshed using GAMBIT. Some simplification is done for the

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simulation model due to time consumption and the complicated geometry of the actual S-CSP model. In the analysis, the volume of fluid (VOF) technique was used to track the flow front of the encapsulation. The viscosity versus shear rate is plotted and the void formation problem is also discussed. The numerical results are compared with the previous experimental results and are in good agreement.

**Keywords** Stacked-Chip Scale Package (S-CSP) · Finite volume method (FVM) Volume of fluid (VOF) · Front tracking · Void

## 1 Introduction

Electronic packaging is defined as a package to house a silicon chip in an electronic system. The main functions of an electronic package are to protect the electronic components from adverse environmental and mechanical effects and to act as a structural support and electrical insulation [1]. It also provides heat dissipation, signal timing and power distribution [2]. In electronic packaging, one of the key processes is encapsulation. Generally, transfer moulding and liquid encapsulation are the most common encapsulation techniques. In transfer moulding, an epoxy moulding compound (EMC) is preheated before loading into the transfer port. By applying certain pressure, the heated moulding compound is transferred from the transfer port through the runners and then into the mould cavities which may consist of a single or many dies [3].

An example of electronic package using the transfer moulding process is Chip Scale Package (CSP) which is a package whose area is less than 1.2 times the area of the Integrated Chip (IC). CSP has smaller, thinner and lighter characteristics and has been developed to address the demands of modern electronics. The pace of CSP technology development is accelerating rapidly. The semiconductor industry is driven by the broad adoption of CSP in wireless handsets and handheld electronic devices. Looking into the modern life today, the market demand for thin, small, light and user friendly electronic packaging that can provide wider variety of functions is still on the increase in recent years [4–6]. The Stacked-Chip Scale Packages (S-CSP) can be the best option to meet the aforesaid demands to a remarkable extend. It integrates Application Specific Integrated Circuit (ASIC) and memories such as flash, Static Random Access Memory (SRAM), and Double Data Rate (DDR) into one package by stacking dies, interconnecting them with wire bonding and moulding all into one package based on the Joint Electronic Device Engineering Council (JEDEC) standard [7, 8]. S-CSP is adopted widely in portable multimedia devices such as cellular telephones, digital cameras, PDAs and audio players [9].

There are several factors that can affect the mould filling yields, such as die thickness (gap clearance), size and array arrangement of complicated stacking dies.

They are defined as critical factors at the initial stage of the product quality planning [10]. As the S-SCP mould is the matrix array type with thin space and wide filling area, the quality concern of the filling process becomes very significant. It involves complex non-Newtonian fluid flow, coupling heat transfer and chemical reaction. As a result, the problems like incomplete mould, void formation, unbalanced flow and wire sweeping are common. Moreover, these phenomena in the complex mould geometry make it difficult to analyze the process and further optimize the design [11].

Although transfer moulding is a mature technology, it is still difficult to optimize and the mould design is a costly and lengthy process. Prototyping often requires numerous modifications and revisions. To minimize the impact of these problems and for better mould design and optimization, numerical flow analysis during the encapsulation process is needed [12]. Turng and Wang [13], Han and Wang [14], and Nguyen et al. [15–18] are the pioneers in numerical simulation of the flow during encapsulation. Their numerical formulation was mostly based on the finite element method (FEM) coupled with the volume of fluid (VOF) technique. The Generalized Hele Shaw approximation was made for the fluid field. Basically, the Hele-Shaw cell consists of two flat plates that are parallel to each other and separated by a small distance. The Hele Shaw approximation uses gap wise-averaged mass and momentum-conservation equations ignoring the gap wise component of the flow. Moreover, the thickness of th model is relatively small as compared to its width and length, and the viscous effect dominates the flow. Thus, the inertia effect is negligible [19]. Abdullah et al. [20, 21] presented flow visualization and EMC rheology on S-CSP encapsulation studies using the finite difference method. An alternative FVM-based three-dimensional mould filling analysis using the incompressible Navier-Stokes equation is introduced in the current study. The Epoxy Moulding Compound (EMC) is modelled as a non-Newtonian fluid and the EMC is treated as a generalized Newtonian fluid (GNF). Accordingly, in our previous work [22], 3D simulation of pressurized under-filling of flip chip package has been presented. The Simulations were done with the computational fluid dynamics code FLUENT 6.3. The Volume of fluid (VOF) Technique is used to track the flow front during calculation. In the present study, we adopt the technique to investigate the flow visualization and encapsulate filling microchip encapsulation process. Numerical results of flow front profiles are compared with previous experimental results. In additional, the void formation is observed.

## 2 Numerical Model

The three-dimensional incompressible flow equation, namely the conservation of mass, Navier-Stokes equation and conservation of energy for non-isothermal, generalized Newtonian fluids (GNF) are given below:

(i) *Continuity equation*:

$$\frac{\partial u}{\partial x} + \frac{\partial v}{\partial y} + \frac{\partial w}{\partial z} = 0 \tag{1}$$

(ii) *Navier-Stokes Equation*:

*x-direction*

$$\frac{\partial u}{\partial t} + u\frac{\partial u}{\partial x} + v\frac{\partial u}{\partial y} + w\frac{\partial u}{\partial z} = -\frac{1}{\rho}\frac{\partial p}{\partial x} + \eta\left(\frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 u}{\partial y^2} + \frac{\partial^2 u}{\partial z^2}\right) \tag{2}$$

*y-direction*

$$\frac{\partial v}{\partial t} + u\frac{\partial v}{\partial x} + v\frac{\partial v}{\partial y} + w\frac{\partial v}{\partial z} = -\frac{1}{\rho}\frac{\partial p}{\partial y} + \eta\left(\frac{\partial^2 v}{\partial x^2} + \frac{\partial^2 v}{\partial y^2} + \frac{\partial^2 v}{\partial z^2}\right) \tag{3}$$

*z-direction*

$$\frac{\partial w}{\partial t} + u\frac{\partial w}{\partial x} + v\frac{\partial w}{\partial y} + w\frac{\partial w}{\partial z} = -\frac{1}{\rho}\frac{\partial p}{\partial w} + \eta\left(\frac{\partial^2 w}{\partial x^2} + \frac{\partial^2 w}{\partial y^2} + \frac{\partial^2 w}{\partial z^2}\right) \tag{4}$$

(iii) *Energy equation*:

$$\rho C_p\left(\frac{\partial T}{\partial t} + u \cdot \nabla T\right) = \nabla(k\nabla T) + \Phi \tag{5}$$

However, a modification in the conservation of energy has been made by inserting an energy source term. The energy source term is as follows:

$$\Phi = \eta\dot{\gamma} \tag{6}$$

For predicting the relationship between viscosity and the degree of polymerization that are given accordingly as:

The Cross rheology model:

$$\eta(T, \dot{\gamma}) = \frac{\eta_0(T)}{1 + \left(\frac{\eta_o \dot{\gamma}}{\tau^*}\right)}, \tag{7}$$

where

$$\eta_0(T) = B\exp\left(\frac{T_b}{T}\right) \tag{8}$$

$n$ is the power law index, $\eta_0$ is the zero shear rate viscosity, $\tau^*$ is the parameter that describes the transition region between zero shear rates and the power law region of the viscosity curve, $\dot{\gamma}$ is the shear rate, $B$ is an exponential-fitted constant and $T_b$ is a temperature fitted-constant, and $T$ is the absolute temperature.

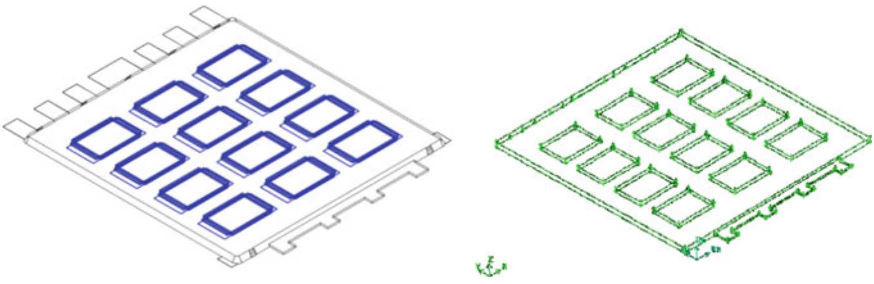
In a three-dimensional filling simulation, accurate tracking of the melt fronts as well as the representation and evolution of the complex topology are very important. In the VOF method the melt front can be tracked by solving the transport equation of the fractional volume function. The transport equation can be solved by either in the geometrical approach or the algebraic approach. The VOF equation is given as:

$$\frac{dF}{dt} = \frac{\partial F}{\partial t} + u\frac{\partial F}{\partial t} + v\frac{\partial F}{\partial t} + w\frac{\partial F}{\partial t} - \left\{\frac{\partial^2 F}{\partial x^2} + \frac{\partial^2 F}{\partial y^2} + \frac{\partial^2 F}{\partial z^2}\right\} = 0, \tag{9}$$

where $F$ is defined either as equal to one ($F = 1$) for the fluid region or equal to zero ($F = 0$) for the empty region and partially full if $F$ has value in between one and zero at the melt front ($0 < F < 1$).

## 3 Simulation Setup

The volume of fluid (VOF) model in FLUENT 6.3.26 is utilized to simulate the S-CSP mold filling process. In the VOF model, a single set of momentum equations is shared by the fluids, and the volume fraction of each of the fluids in each computational cell is tracked throughout the domain. Air and encapsulant material Hitachi CEL-9200 XU (LF) [23] are defined as the phases in the analysis and the mould temperature is set as 175 °C. Implicit solution and time dependent formulation are applied for the volume fraction in every time step. The volume fraction of the encapsulant material is defined as one and zero value for the air phase. Besides, viscosity cross model and VOF techniques are applied to track the melt front. The model is created by using GAMBIT software and a total 94196 tetrahedral elements are generated for the simulation. The simulation took about seven hours to complete for a single case. The S-CSP package model used in the present study and its simplified model and the meshed model are shown in Figs. 1 and 2, respectively. Some simplifications have been made to the actual model such as replacement of chamfered corners by 90° corners and removal of vents for the simulation model. The material properties [23] for the current study are summarized in Table 1. The boundary and initial conditions used in the calculation are as follows:



(a) Actual model (b) Simplified model

**Fig. 1** The actual and simplified S-CSP models. **a** Actual model. **b** Simplified model

**Fig. 2** 3D meshed model

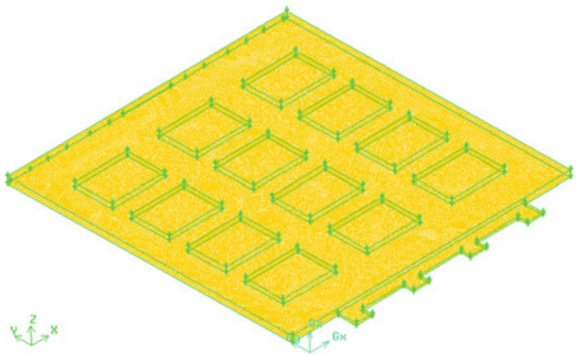


**Table 1** Material properties [23]

| Parameter | Value |
|---|---|
| $n$ | 0.7938 |
| $\tau^{*}(\mathrm{Pa})$ | 7.264E−4 |
| $B$ | 5.558E 4 |
| $T_b(\mathrm{K})$ | 7.166E3 |
| $\rho(\mathrm{kg/cm^3})$ | 2.000E3 |
| $c_p(\mathrm{J/kg^*K})$ | 1079 |
| $k(\mathrm{W/m^*K})$ | 0.97 |

(a) On the mould wall: $u = v = w = 0$; $T = T_w$; $\frac{\partial p}{\partial n} = 0$
(b) On the melt front: $p = 0$
(c) On the inlet: $u = v = w = given$; $p = p_{in}(x, y, z, t)$; $T = T_{in}$.

## 4 Results and Discussion

The experiments have been done to investigate the flow behaviour of epoxy moulding compound (EMC) inside the actual mould of Stacked-Chip Scale Package (S-CSP) with twelve arrays of six stacking dies. The EMC used in this investigation is the HITACHI CEL-9200-XU (LF). The mould temperature is set at 175 °C and the package pressure is 70 kg/cm$^2$. Short-shot results have been performed to observe the melt front advancement at different times step. The short-shot samples can be obtained by setting certain stroke length of the plunger. The package will be incomplete if the sets less then the stroke length. Thus the front profile can be attained. Figure 3 illustrates the gate, air vents, stacking dies in matrix array of 4 × 3 and the flow direction.

Figure 4 demonstrates respectively the experiment and simulation (short shot) results of melt front advancement with an inlet velocity of 4 mm/s in the S-CSP. Hitachi CEL-9200-XU (LF) is used as an encapsulant in the simulation. The encapsulation process shows a good agreement of flow front profile at 1.5 s and 2 s for experimental and simulation result. The mould compound flows around the dies and moves quickly before it starts to cover the dies. However, the flow above the dies covers more area in the experiments compared to that of the simulation. The effect of dies on the flow fronts is clearly visible. It restricted the flow along the edges and over the dies. As a result, the flow around the dies is accelerated.

However, at 2.5 s the simulation flow front profile is found more slowly in filling compared to experiments. This phenomenon is caused by the simplification of the simulation model. The simplification on the stacked chip may be a factor for affecting the encapsulant during the process. The simplified chips act as a larger obstruction to the flow and caused the encapsulant to fill the free region. At 6 s of

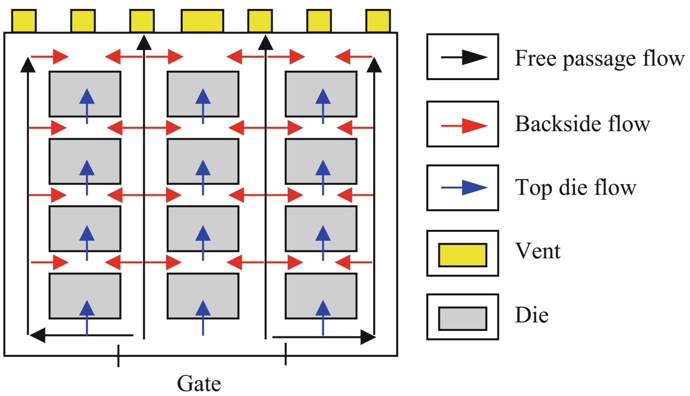



**Fig. 3** Schematic of flow in the cavity

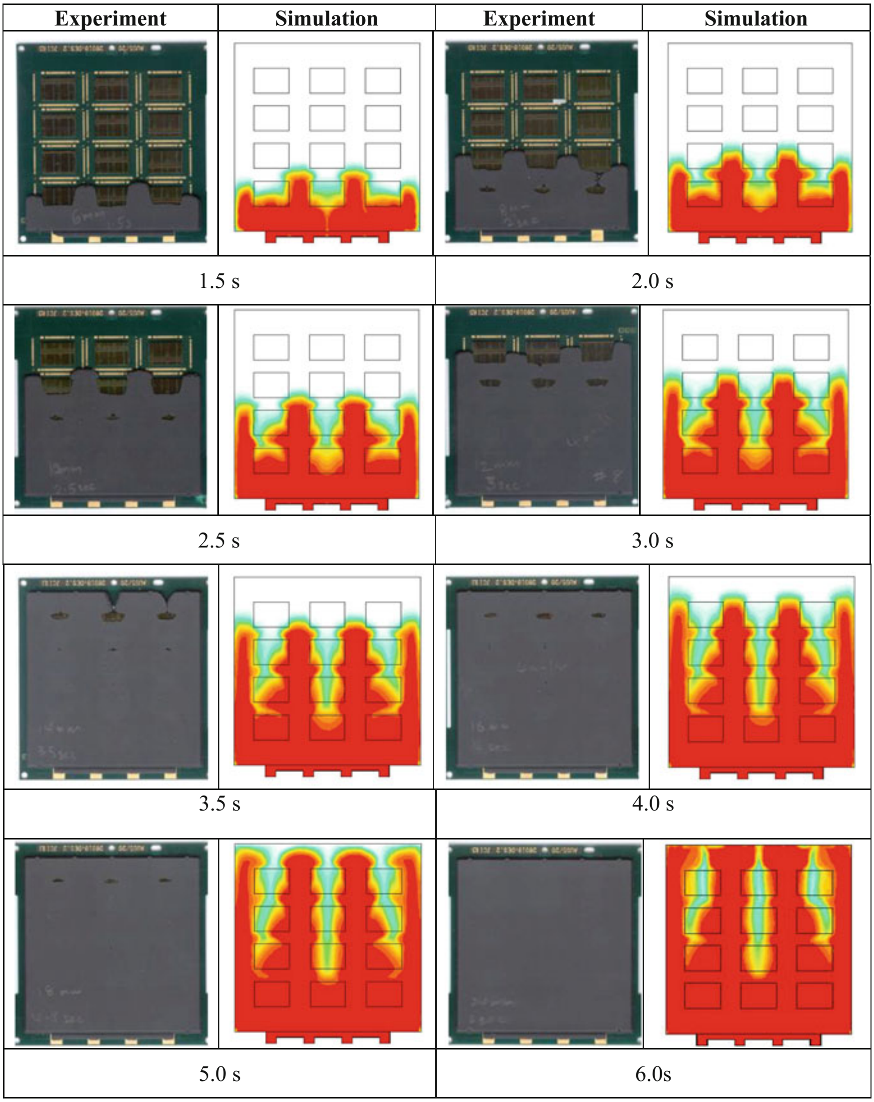



**Fig. 4** Short shot results of melt front advancement at distinct time steps with velocity inlet of 4 mm/s

the filling stage, a void is found in the mold filling process. Figure 5 shows the void formation during the S-CSP filling process.

Figure 6 shows viscosity variation versus shear rate. The curves show as a power law viscosity variation where the viscosity reduces with the shear rate.

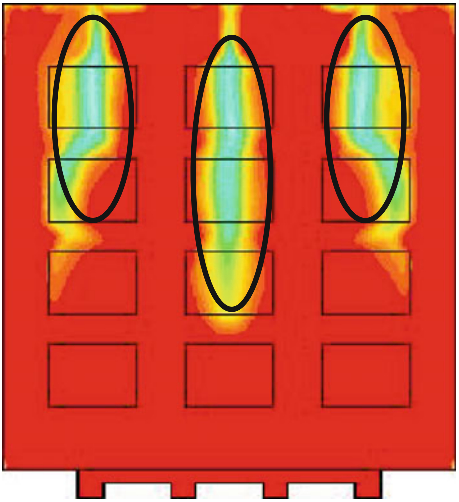


Fig. 5 Void formation at circled region

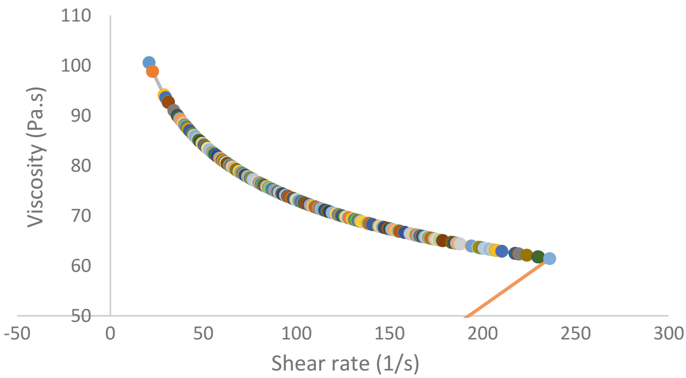



Fig. 6 Viscosity versus Shear rate

## 5 Conclusion

A three-dimensional non-isothermal incompressible analysis model based on the finite difference method (FVM) for the transfer moulding process is presented and compared with the experimental results. The three-dimensional S-CSP package is simulated to study the flow visualization in the process. The encapsulant material used is the Hitachi Chemical CEL-9200-XU (LF). Cross-viscosity model and volume of fluid (VOF) technique are used to track the flow front in the numerical simulation. Navier-Stokes equations are solved by the finite volume method and SIMPLE segregated algorithm. It is found that simulation results of melt fronts are in good agreement with the experimental results, thus proving the strength of the model and the fluent software in handling stacked chip encapsulant problems. The present study may be extended further for more actual type of stacked chip and different parameters on different S-CSP packages.

## References


1. Tummala, R.R.: Fundamentals of Microsystems Packaging, pp. 44–79. McGraw Hill, Singapore (2001)
2. Manzione, L.T.: Plastic Packaging of Microelectronic Device, pp. 1–35. Van Nostrand Reinhold, New York (1990)
3. Liang, C.W., Kulakarni, V.M., Aswatha Narayana, P.A., Seetharamu, K.N.: Parametric studies in transfer molding for Newtonian flids. J. Phys. Sci. **16**(2), 103–114 (2005)
4. Kulkarni, V.M., Seetharamu, K.N., Azid, I.A., Aswatha Narayana, P.A., Quadir, G.A.: Numerical simulation of underfill encapsulation process based on charecteristic split method. Int. J. Numer. Meth. Engng. **66**, 1658–1671 (2006)
5. Kada, M., Smith, L.: Advancements in Stacked Chip Scale Packaging (S-CSP) provides system-in-a-package functionality for wireless and handheld applications. Future Fab. Intl. **9,** 246–251 (2000)
6. Sze, M.W.H., Papageorge, M.: Encapsulation selection, characterization and reliability for fine pitch BGA (fpBGA). In: 4th Annual Flip Chip, BGA, Chip Scale Packaging '98, April 28–29, 1998, pp. 1–7 (1998)
7. Pei, C.C., Hwang, S.J.: Three-dimensional paddle shift modelling for IC packaging. Trans. ASME J. Electron. Packag. **127**, 324–334 (2005)
8. Nguyen, L., Quentin, C., Lee, W., Bayyuk, S., Bidstrup-Allen, S. A. and Wang, S.T.: Computational modeling and validation of the encapsulation of plastic packages by transfer molding. Trans. ASME J. Electron. Packag. **122**, 138–146 (2000)
9. Chang, R.-Y., Yang, W.-S., Chen, E., Lin, C., Hsu, C.-H.: On the dynamic of air trap in the encapsulation process of microelectronics package. In: Proceedings of ANTEC' 98 Conference (1998)
10. Zhou, T., Dreiza, M.: Stacked Die Package Design Guidelines. In: Proceedings of IMAPS Conference (2004)
11. Fukui, Y., Yano, Y., Juso, H., Matsune, Y., Miyata, K., Narai, A., Sota, Y., Takeda, Y., Fujita, K., Kada, M.: Triple-Chip Stacked CSP. In: IEEE 2000 International Electronic Components and Technology Conference. ISBN 0-7803-5908-9 (2000)
12. Kim, S.W., Turng, L.S.: Developments of three-dimensional computer-aided engineering simulation for injection molding. Institute of Physics Publishing. Model. Simul. Mater. Sci. Eng. **12**(2004), S151–S173 (2004)
13. Turng, L.S., Wang, V.W.: On the simulation of microelectronic encapsulation with epoxy molding compound. J. Reinf. Plastics Compos. 12, 506–519 (1993)
14. Han, S., Wang, K.K.: Flow analysis in a cavity with lead frame during semiconductor chip encapsulation. In: Advance in Electronic Packaging, ASME EEP, vol. 10–11 (1995)
15. Nguyen, L.T.: Reactive flow simulation in transfer molding of IC Packages. In: Proceedings 43rd IEEE Electronic Components and Technology Conference 1993, pp. 375–390 (1993)

## Conference Proceeding

16. Nguyen, L.: Flow simulation in IC chip encapsulation. Electronic Components and Technology Conference, Buena Vista (1994)
17. Nguyen, L., Jackson, J., Teo, C.H., Chillara, S., Asanasavest, C., Burke, T., Walberg, R., Lo, R., Weiler, P., Ho, D., Rauhut, H.: Wire Sweep Control with Mold Compound Formulation. In: 1997 Proceedings 47th Electronic Components and Technology, pp. 60–71 (1997)
18. Nguyen, L., Quentin, C.G., Lee, W.W.: Flow modeling and visualization of the transfer molding of plastic ball grid array packages. In: 1999 Electronic Components and Technology Conference, Santa Clara (1999)
19. Lee, M.M., Kim, J.Y., Yoo, M., Chung, J.Y., Lee, C.H.: Rheological characterization and full 3D mold flow simulation in multi-die stack CSP of chip array packaging. In: Electronic Components and Technology Conference, 1-4244-0152-6/06(2006)
20. Khalil Abdullah, M., Abdullah, M.Z., Mujeebu, M.A., Kamaruddin, S.: A study of effect of expoxy molding compound (EMC) rheology during encapsulation on stacked-CHIP scale packages (S-CSP). J. Reinf. Plast. Compos. 28, 2527–2538 (2008)
21. Khalil Abdullah, M., Abdullah, M.Z., Kamarudin, S., Ariff, Z.M.: Study of flow visualization in stacked-chip scale packages (S-CSP). Int. Commun. Heat Mass Transfer 34(7), 820–828 (2007)
22. Khor, C.Y., Mujeebu, M.A., Abdullah, M.Z., Che Ani, F.: Finite volume based CFD Simulation of pressurized flip chip underfill encapsulation process, microelectronics reliability. Microelectron. Reliab. 50(1), 98–105 (2010)

## Book Chapter

23. Modeling multiphase flow, FLUENT Documentation, Chapter 23