

An Extraction Method of SiC Power MOSFET Threshold Voltage

W. Jouha, A. El Oualkadi, P. Dherbécourt, E. Joubert, and M. Masmoudi

Abstract

Threshold voltage (V_{th}) is one of the most important electrical parameters in silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) design, characterization, modeling, and simulation. The reduction of the threshold voltage increases the performance in terms of switching time for the power converter. The study of the evolution of V_{th} over time must be considered by the designers of the new generations of energy conversion systems. There are several existing methods for V_{th} extraction, and the aim of this chapter is to compare the commonly used MOSFET threshold voltage extraction methods and to propose a new method based on a physical approach. The extraction method proposed in this chapter is based on the static I–V measurements and the use of the Levenberg–Marquardt optimization algorithm. The implementation of the several extraction methods is tested and discussed by applying them to commercial components in order to evaluate their performance and validity in both the linear and saturation regions. The study is carried out for two generations of power SiC-MOSFETs of CREE constructor.

1 Introduction

Recently, silicon carbide MOSFETs are of great interest in high-power applications (energy conversion, automotive industry, and aeronautics). They replace the silicon components whose performances are limited in terms of voltage blocking capability, operation temperature, and switching frequency (Raynaud et al. 2010; Bjrk et al. 2011). Wide band gap components have interesting intrinsic properties, especially a high thermal conductivity. The SiC performance makes the SiC-MOSFETs a good competitor to traditional silicon MOSFETs and IGBTs (Zhao et al. 2007; Glaser et al. 2011). However, these new components require reliability studies and physical modeling to meet the integration requirements of energy conversion systems. The threshold voltage V_{th} is a fundamental parameter for MOSFET modeling and characterization. Its extraction requires precise values (Garcia Snchez et al. 2006). The tens of millivolts errors in the threshold voltage value can no longer be neglected in the modeling of the transistor behavior. The threshold voltage has an impact in the MOSFET performance in terms of the time and energy required for switching (Simonot et al. 2010).

In the literature, various methods have been developed and used to extract the threshold voltage (V_{th}) of a MOSFET (Wong et al. 1987; Tsuno et al. 1999; DieterSchroder 2006; Bazigos et al. 2011). In this chapter, a review of the commonly used MOSFET threshold voltage extraction methods is presented and discussed. The four largely used methods are tested on two generations SiC power MOSFETs of CREE constructor. Moreover, the chapter proposes a new procedure to extract the threshold voltage based on the Levenberg–Marquardt optimization algorithm using a physical approach. The results obtained with this proposed extraction method are compared to those obtained with other methods.

This chapter is organized as follows: Sect. 2 presents a description of the studied devices. Section 3 develops usual

W. Jouha (✉) · P. Dherbécourt · E. Joubert · M. Masmoudi
Normandy University, IUT, INSA Rouen, CNRS, GPM
UMR CNRS 6634, 76000 Rouen, France
e-mail: jouhaieea@gmail.com

P. Dherbécourt
e-mail: pascal.dherbecourt@univ-rouen.fr

E. Joubert
e-mail: eric.joubert@univ-rouen.fr

M. Masmoudi
e-mail: mohamed.masmoudi@univ-rouen.fr

W. Jouha · A. El Oualkadi
LabTIC Laboratory, National School of Applied Science of
Tangier, Abdelmalek Essaadi University, Tangier, Morocco
e-mail: eloualkadi@gmail.com

threshold voltage definition for MOSFET transistors. Section 4 describes the proposed extraction procedure with four other V_{th} extraction procedures frequently used. Section 5 discusses and compares the obtained results by all these methods. Finally, the conclusion is given in Sect 6.

2 Description of the Studied Device

Two SiC-MOSFET samples for two generations of CREE constructor have been selected for this study: the second-generation SiC-MOSFET G2 (10 A, 1200 V) reference C2M0280120D and the third-generation SiC-MOSFET G3 (11 A, 900 V) reference C3M0280090D (Cree inc 2018a, b). The choice is based on the fact that both generations have close relative drain currents. Figure 1 shows the TO-247 package component and its electrical symbol.

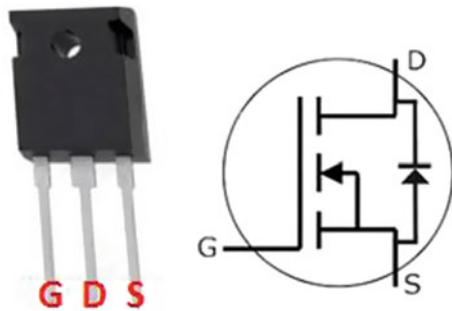


Fig. 1 The TO-247 package component (left) and its electrical symbol (right)

The constructor maintains the same planar structure for the two generations of n-channel enhancement MOSFETs. Figure 2 shows the physical structures of the two generations of SiC-MOSFETs. The performance is generally improved with the changes in the epitaxy thickness, pitch, and gate width. Indeed, the reduction in thickness of oxide for the third generation makes it possible to have a threshold voltage reduced compared to the second generation.

3 Threshold Voltage Definition

Conventionally, the threshold voltage is understood simply as the gate–source voltage (V_{gs}) at which significant drain current starts to flow, and physically the threshold voltage V_{th} is defined as the voltage applied to the metal electrode to enter the strong inversion domain of operation. When the semiconductor surface enters the strong inversion mode of operation, the surface potential (ψ_s) is equal to twice the bulk potential (ψ_B) (Ortiz-Conde et al. 1998; Baliga 2008). In this case, the V_{th} is given by

$$V_{th} = \frac{Q_S}{C_{ox}} + 2\psi_B \quad (1)$$

where C_{ox} is the specific capacitance of the oxide, and Q_S represents the total charge in the semiconductor. The bulk potential (ψ_B) can be related to the doping concentration (N_A) in the semiconductor and temperature T , and then the threshold voltage V_{th} is given by the following equation:

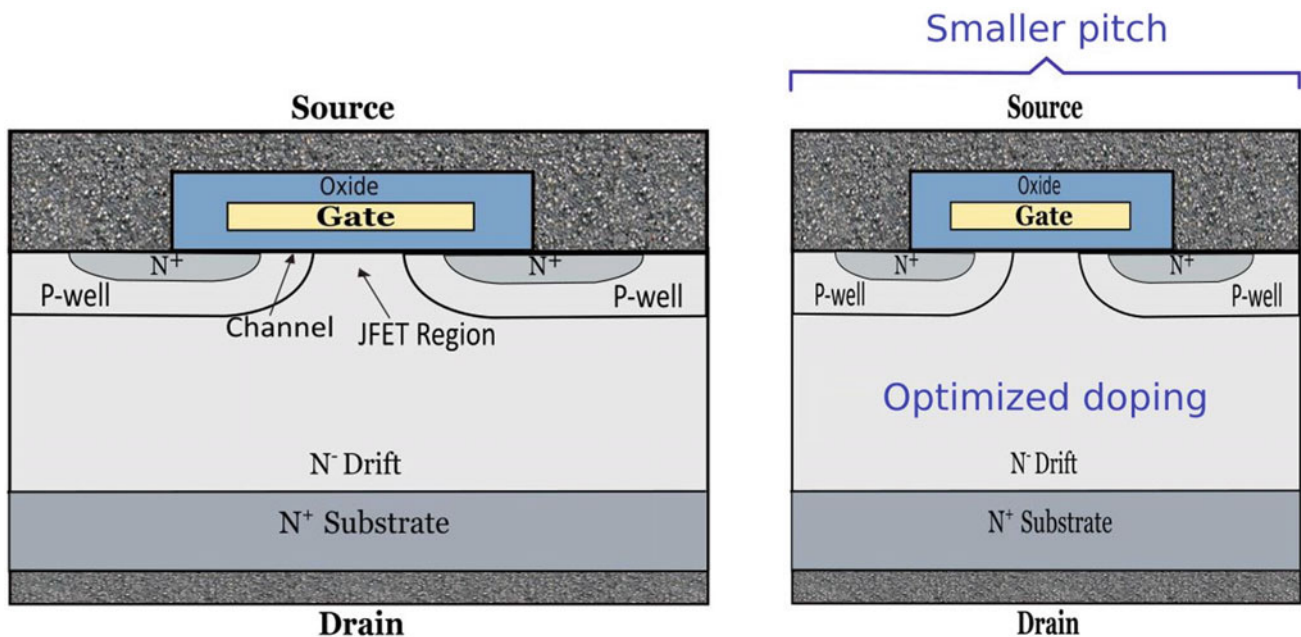


Fig. 2 MOSFET Structure of second generation (left) and third generation (right)

$$V_{th} = \frac{\sqrt{4\epsilon_{SiC}kT_jN_A \ln\left(\frac{N_A}{n_i}\right)}}{C_{ox}} + \frac{2kT_j}{q} \ln\left(\frac{N_A}{n_i}\right) - \frac{Q_{ox}}{C_{ox}} \quad (2)$$

where ϵ_{SiC} is the relative permittivity of the semiconductor, n_i is the concentration of intrinsic carriers, k is the Boltzmann constant, and Q_{ox} presents the total effective charge in the oxide. This charge is composed by the mobile ion charge, the trapped oxide charge, the fixed oxide charge, and the interface state charge after taking into account the fact that these charges are distributed throughout the oxide. The value of the threshold voltage depends on some physical parameters which characterize the MOSFET structure such as the gate material, the thickness of oxide layer t_{ox} , substrate doping concentrations N_A , and the temperature. However, this definition of V_{th} is difficult to exploit because the Q_{ox} value and the physical parameters of the component need to be defined. Various studies show that the approximate definition of V_{th} is related to the extraction method. In the following section, we present various methods usually used to define and extract the threshold voltage value.

4 Extraction Methods of Threshold Voltage

Several definitions and methods have been developed to extract the threshold voltage (Booth et al. 1987; Tsuno et al. 1998; Dobrescu et al. 2000; Terada et al. 2001; Ortiz-Conde et al. 2002; Boucart and Ionescu 2008). They include the constant current method (CC), the linear extrapolation method (LE), g_m transconductance linear extrapolation method (GMLE), and transconductance change method (TC). In this chapter, these conventional methods are

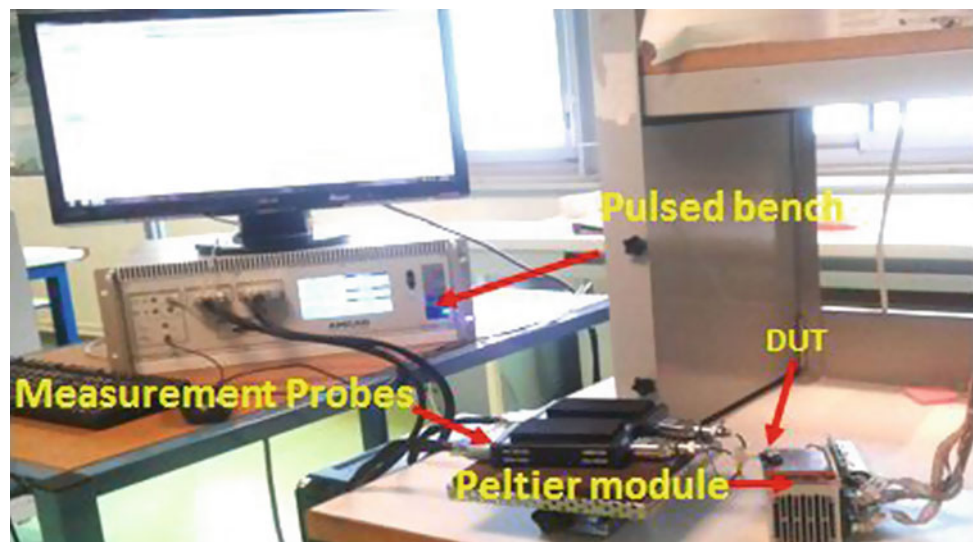
compared to a proposed method based on the current drain equation taking into account some physical parameters. For all procedures, the threshold voltage parameter is extracted directly from the static characterization (measured I-V curves) or from derived curves.

For this purpose, we have performed the I-V static characterizations using a pulsed bench presented in Fig. 3. This bench allows to avoid the self-heating of the device under test during the measurement duration by generating a pulse not exceeding 7 μ s. The temperature stabilization of the device is assured by a Peltier module.

4.1 The Constant Current Method

The constant current method (CC) is extensively exploited in industry because of its simplicity (Ortiz-Conde et al. 2002). It defines V_{th} as the value of the voltage V_{gs} corresponding to the appearance of a significant drain current for a given V_{ds} . Some studies have been examined this current equal to $(W/L) \times 10^{-7}$, where W and L are the width and length of the channel, respectively (Terada et al. 2001). However, a recent study proposes that this current should depend on the voltage V_{ds} in order to obtain a coherent V_{th} value in the saturation zone (Bazigos et al. 2011). For our study, due to lack of the values of L and W , we calculate the voltage V_{th} for MOSFET with a similar way to the datasheets for $I_{ds} = 1.25$ mA (second generation), $I_{ds} = 1.2$ mA (third generation), at the output voltage $V_{ds} = 0.1$ V in linear regime, and $V_{ds} = 20$ V in the saturation regime. The results of the extraction of V_{th} by the CC method performed on second-generation device (G2) are shown in Fig. 4 for linear regime and Fig. 5 for saturation regime.

Fig. 3 The I-V static characterizations bench



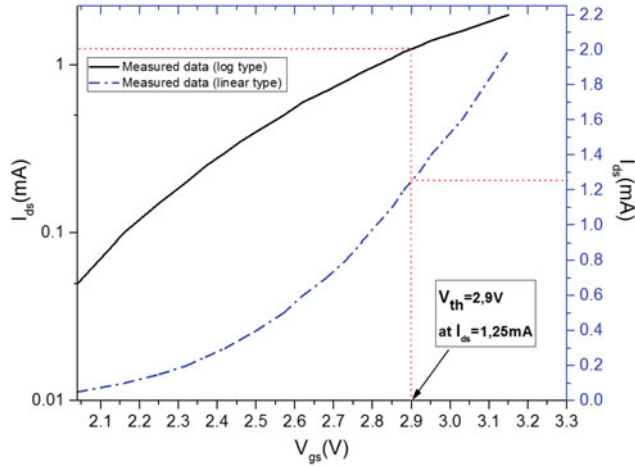


Fig. 4 Current constant method in the linear region ($V_{ds} = 0.1$ V) method implemented on the $I_{ds}V_{gs}$ measured for G2

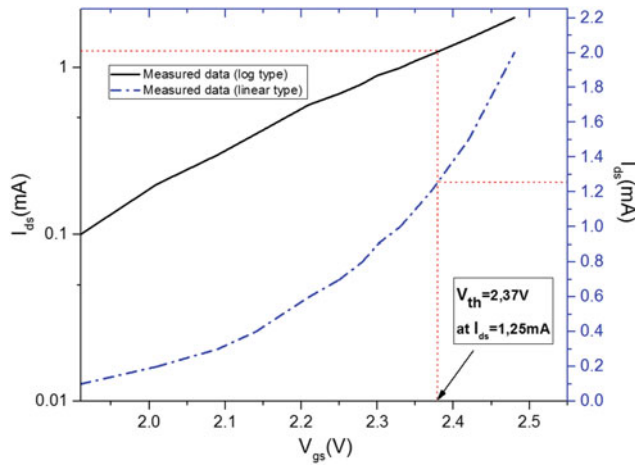


Fig. 5 Current constant method in the saturation region ($V_{ds} = 20$ V) method implemented on the $I_{ds}V_{gs}$ measured for G2

4.2 The Linear Extrapolation Method

The linear extrapolation method (LE) is most widely used. The threshold voltage is extracted directly from I–V characteristics curves. The drain current is measured as a function of the gate voltage at a low drain voltage to ensure operation in the linear MOSFET region (Dobrescu et al. 2000; DieterSchroder 2006). The threshold voltage is determined from the V_{gs} axis intercept ($I_{ds} = 0$) of the linear extrapolation of the $I_{ds}-V_{gs}$ curve at its maximum first derivative (slope) point. The threshold voltage value is founded from the extrapolated or intercept gate voltage V_{gsi} by ($V_{th} = V_{gsi} - V_{ds}/2$). Figure 6 shows the extraction of V_{th} by this method using a component of the second generation in linear region.

The threshold voltage can also be determined in the MOSFET saturation regime, and we use similar method to

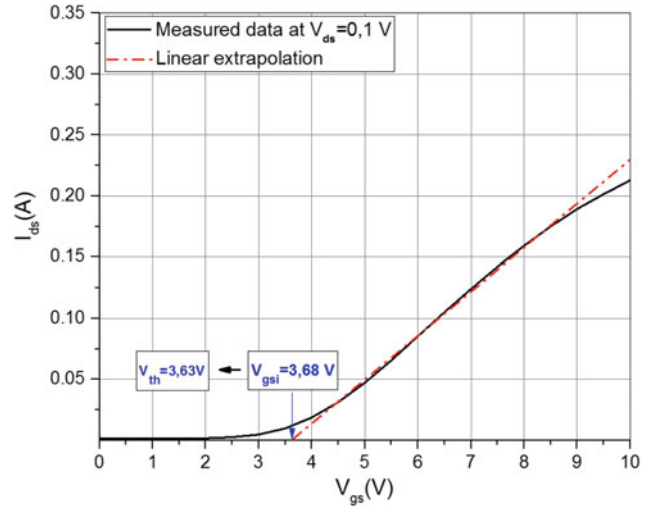


Fig. 6 Linear extrapolation method in the linear region implemented on the $I_{ds}-V_{gs}$ characteristic for G2

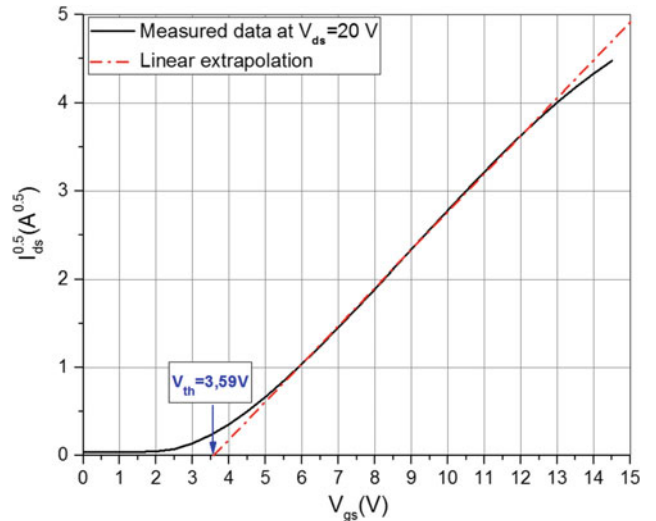


Fig. 7 Linear extrapolation method in the saturation region implemented on the $I_{ds}^{0.5}-V_{gs}$ characteristics for G2

that in the linear regime but with $I_{ds}^{0.5}-V_{gs}$ characteristic curve at a high drain voltage ($V_{ds} > V_{gs} - V_{th}$) to assure operation of MOSFET in saturation region. Figure 6 shows the obtained results with this method using a second-generation device (Fig. 7).

4.3 The Transconductance g_m Linear Extrapolation Method

The transconductance g_m linear extrapolation method (GMLE) determines V_{th} from $g_m - V_{gs}$ characteristics curves. The V_{th} is defined by extrapolating the linearity of g_m , for small V_{gs} values, to the gate voltage where

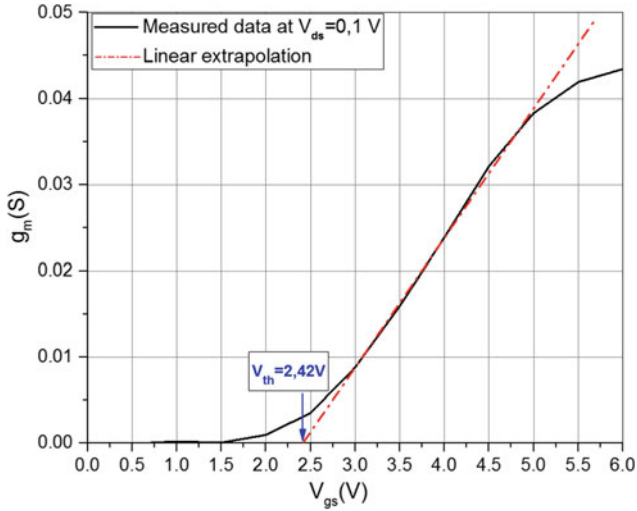


Fig. 8 g_m linear extrapolation method in the linear region implemented on the $g_m - V_{gs}$ characteristic for G2

transconductance g_m becomes equal to 0. Physically, this method uses the linear dependence of the effective carrier mobility μ_{eff} as a function of $(V_{gs} - V_{th})$. This mobility μ_{eff} is affected by the Coulomb scattering (Tsuno et al. 1998, 1999). Figure 8 shows the extraction of V_{th} based on GMLE method using a second-generation device.

In the saturation region, the same procedure is followed using $g_m^{0.5} - V_{gs}$ characteristics curves, with the measurements carried out under an output voltage included in the saturation region ($V_{ds} = 20$ V). Figure 9 shows the extraction of V_{th} using GMLE method in saturation region.

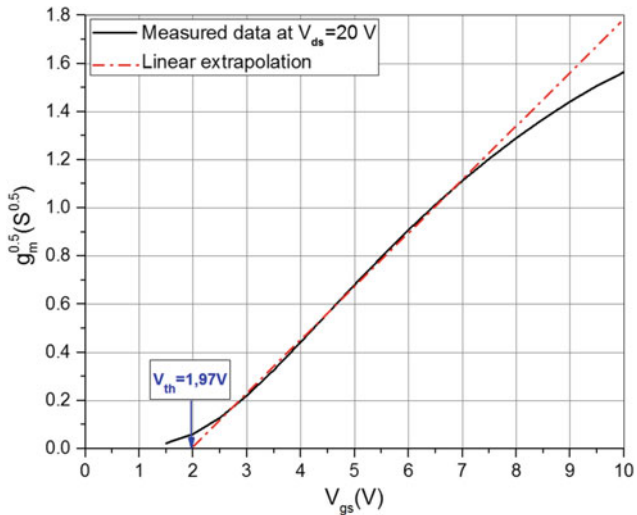


Fig. 9 g_m linear extrapolation method in the saturation region implemented on the $g_m^{0.5} - V_{gs}$ characteristic for G2

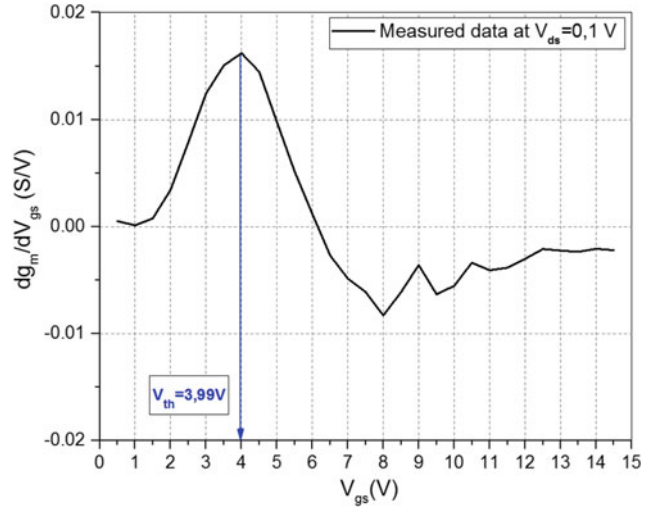


Fig. 10 Extraction of V_{th} in linear region using transconductance change method implemented on the $\frac{dg_m}{dV_{gs}} - V_{gs}$ characteristic for G2

4.4 The Transconductance Change Method

The transconductance change method (TC) uses the curve of the derivative of transconductance g_m versus V_{gs} . It determines V_{th} as the V_{gs} value at which the derivative of the transconductance is a maximum (Booth et al. 1987; Wong et al. 1987; Boucart and Ionescu 2008). Figure 10 shows the transconductance change method for extraction of V_{th} in linear region. However, Fig. 11 shows the extraction of V_{th} with the same method in saturation region implemented on the $\frac{dg_m^{0.5}}{dV_{gs}} - V_{gs}$ characteristic for the second-generation device.

4.5 New Procedure: The Optimization Levenberg–Marquardt Method

A common feature presented in the most V_{th} extraction methods based on the $I_{ds} - V_{gs}$ input characteristics is the strong influence of the channel mobility degradation on the resulting value of the extracted V_{th} . In order to take into account this situation, we present a new extraction method called Optimization Levenberg–Marquardt method (OLM) (Jouha et al. 2017). Due to the definition of the drain current (Eq. 3) (McNutt et al. 2007), this method can be used in the saturation region ($V_{ds} = 20$ V).

$$I_{ds} = \frac{K_p (V_{gs} - V_{th})^2}{2(1 + \theta(V_{gs} - V_{th}))} \quad (3)$$

where θ is a parameter that takes into account the reduction of the mobility following the increase of a transverse electric field. Note that K_p is called the transconductance exprimed

by (A/V^2) . The term transconductance is abusively used in the literature, since there is a linear relationship between K_p and g_m according to the expression ($g_m = K_p \cdot V_{ds}$) (Baliga 2008).

The extraction of the threshold voltage is based on two steps: for the first one, we used Eq. 3 of the drain current in saturation region which takes into account the influence of the channel mobility degradation (θ parameter). For the

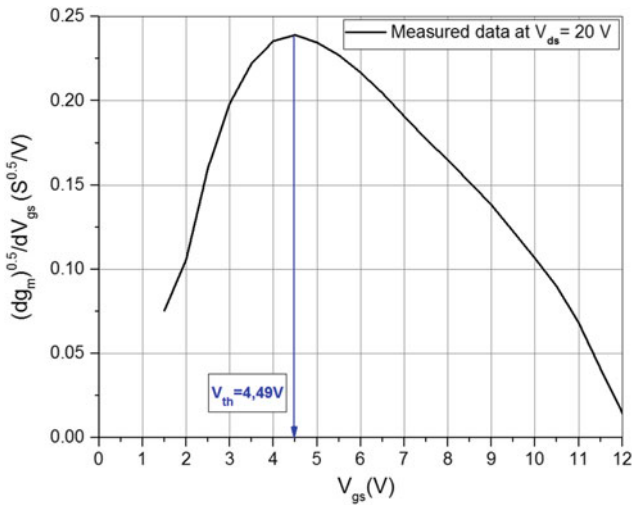


Fig. 11 Extraction of V_{th} in the saturation region using transconductance change method implemented on the $\frac{dg_m^{0.5}}{dV_{gs}} - V_{gs}$ characteristic for G2

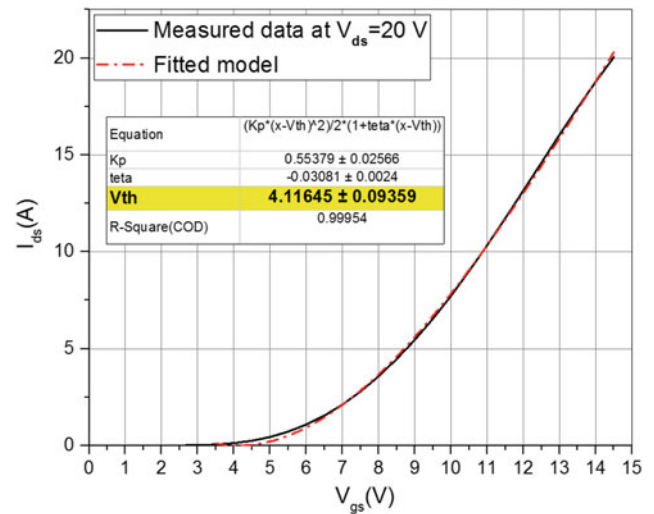


Fig. 13 Extraction of V_{th} in the saturation region using OLM method implemented on the $I_{ds} - V_{gs}$ characteristic for G2

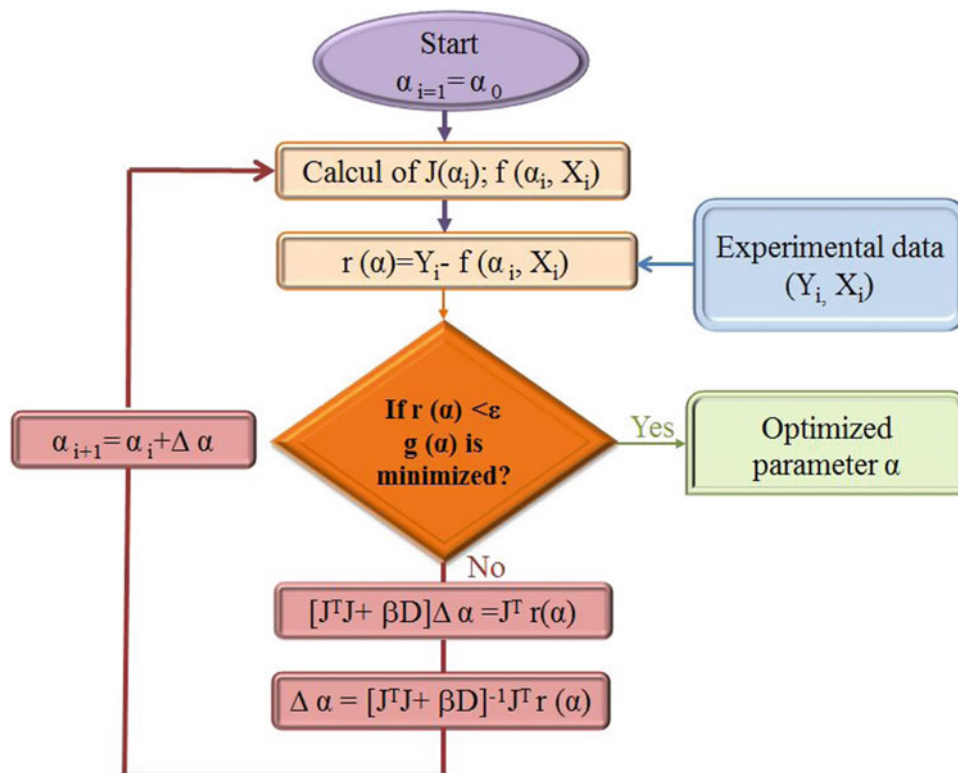


Fig. 12 Flowchart of the Levenberg–Marquardt algorithm

second step, we use the Levenberg–Marquardt (L-M) algorithm to optimize the parameters of Eq. 3 by fitting the curve of this equation with the measured I_{ds} – V_{gs} input curve. The Levenberg–Marquardt algorithm is developed by Levenberg and Marquardt (Levenberg 1944; Marquardt 1963). The flowchart of this algorithm is presented in Fig. 12.

It is an efficient iterative method for estimating nonlinear regression parameters of models. Consider the nonlinear model fit $Y_i = f(\alpha, X_i)$, where X_i (V_{gs} or Y_{ds}) and Y_i (I_{ds}) are the data extracted from the I–V measurements, α is a vector of dimension n that represents the parameters of the model (V_{th} , K_p , θ). The L-M method searches for $(\alpha_1, \alpha_2, \alpha_3, \dots, \alpha_n)$ which are the solutions of α (locally) minimizing $g(\alpha)$ defined by

$$g(\alpha) = \sum_{i=1}^m (Y_i - f(\alpha, X_i))^2 \quad (4)$$

The L-M algorithm finds the solution using

$$\alpha_{i+1} = \alpha_i - (J^T J + \beta D) J^T r(\alpha) \quad (5)$$

where $r(\alpha) = Y_i - f(\alpha, X_i)$, J is the Jacobian matrix for $f(\alpha, X_i)$, J^T is the transposed matrix of J , β is a regularization parameter, and D is the identity matrix in which its dimension is equal to that of $J^T J$ to adjust the scales factors.

The principle of this extraction parameters method is illustrated in Fig. 13 using the second-generation device, showing a correct fitting of the model with the experimental measurement data.

We have previously validated this method in order to model the static MOSFET behavior for three generations of power MOSFET, obtaining a very satisfactory fitting of I–V curves. Moreover, this method is applicable for a temperature range from 0 to 135 °C, and it allows a complete extraction of other parameters values such as K_p and θ parameter on the whole temperature range.

5 Results and Discussions

The relative performance of the presented methods is compared under the same conditions by applying them to the measured characteristics of two test devices (G2 and G3).

Table 1 Threshold voltage values obtained from four extraction methods and the proposed method for the second generation of a power SiC-MOSFETs biased in the linear and saturation region

	Linear	Saturation (V)
CC	2.9 V	2.37
LE	3.63 V	3.59
GMLE	2.42 V	1.97
TC	3.99 V	4.49
OLM	NA	4.12

Table 2 Threshold voltage values obtained from four extraction methods and the proposed method for the third generation of a power SiC-MOSFETs biased in the linear and saturation region

	Linear	Saturation (V)
CC	2.79 V	2.04
LE	3.46 V	3.12
GMLE	2.30 V	1.75
TC	3.49 V	3.99
OLM	NA	3.37

Tables 1 and 2 and Fig. 14 show the resulting threshold voltage values for these devices obtained from the presented extraction methods in two regions of operation (linear and saturation), and the proposed OLM method gives extracted values of the threshold voltage V_{th} in the saturation region.

Moreover, the value of the extracted threshold voltage depends on the used extraction method for two generations of devices. The obtained results are in agreement with those of the bibliography (Ortiz-Conde et al. 2002, 2013). The differences can be explained by the strong influence of the source and drain parasitic series resistances and the channel mobility degradation on the linearity of the I_{ds} – V_{gs} curve (Tsuno et al. 1999). However, the proposed method is very useful for an accurate evaluation of V_{th} , thanks to the excellent modeling of the output current I_{ds} in saturation region. It describes the dependence of I_{ds} to the mobility degradation, compared to other methods which are based only on the linearity of the curve versus gate–source voltage V_{gs} .

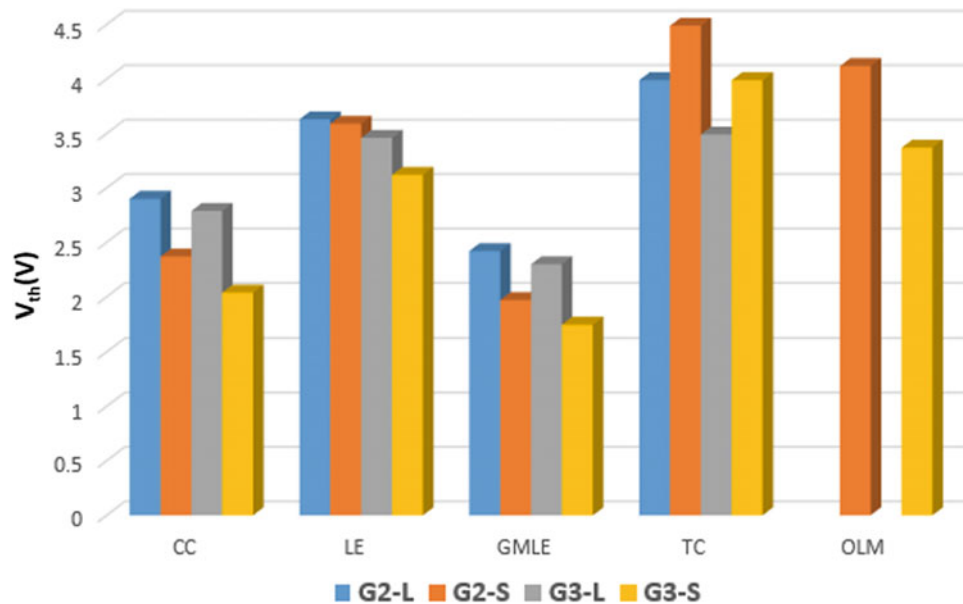


Fig. 14 Comparisons of threshold voltage values obtained for two generations of power SiC-MOSFETs (G2 & G3) biased in the linear (L) and saturation region (S)

6 Conclusion

In this chapter, we have presented, reviewed, and compared several extraction methods currently used to determine the threshold voltage value of SiC-MOSFETs from their drain current and transconductance g_m versus gate voltage characteristics measured either in linear and saturation operation regions. A new extraction method using physical approach is presented. This method is based on the measurements of input characteristics ($I_{ds}-V_{gs}$) and the optimization Levenberg–Marquardt algorithm. It is a very accurate method, thanks to the excellent modeling of the drain current in saturation operation regime of power transistor. The performance of the presented methods was compared under the same conditions by applying them to the measured characteristics of two SiC power MOSFETs generations.

The comparison of these V_{th} extraction methods shows that the proposed method is the only one that relies on the physical equations of the transistor that depends on the transconductance K_p and the channel mobility degradation μ_n . This makes the V_{th} extracted by the OLM method the best indicator for monitoring the transistor aging in operational conditions.

References

- Baliga, B. J. (2008). *Fundamentals of power semiconductor devices*. US: Springer.
- Bazigos, A., Bucher, M., Assenmacher, J., Decker, S., Grabinski, W., & Papananos, Y. (2011). An adjusted constant-current method to determine saturated and linear mode threshold voltage of MOSFETs. *IEEE Transactions on Electron Devices*, 58(11), 3751–3758.
- Bjrk, F., Treu, M., Hilsenbeck, J., Kutschak, M. A., Domes, D., & Rupp, R. (2011). *1200 V SiC JFET in cascode light configuration: Comparison versus Si and SiC based switches* (vol. 679–680, pp. 587–590).
- Booth, R. V., White, M. H., Wong, H.-S., & Krutsick, T. J. (1987). The effect of channel implants on MOS transistor characterization. *IEEE Transactions on Electron Devices*, 34(12), 2501–2509.
- Boucart, K., & Ionescu, A. M. (2008). A new definition of threshold voltage in tunnel FETs. *Solid-State Electronics*, 52(9), 1318–1323.
- Cree inc. c2m0280120d sic mosfet datasheet. <https://www.wolfspeed.com/media/downloads/171/C2M0280120D.pdf>. Accessed April 11, 2018.
- Cree inc. c3m0280090d sic mosfet datasheet. <https://www.wolfspeed.com/media/downloads/825/C3M0280090D.pdf>. Accessed April 11, 2018.
- DieterSchroder, K. (2006). *Semiconductor material and device characterization* (3rd ed.). Hoboken, New Jersey: Wiley.
- Dobrescu, L., Petrov, M., Dobrescu, D., & Ravariu, C. (2000). Threshold voltage extraction methods for MOS transistors. In *2000 International Semiconductor Conference. 23rd Edition. CAS 2000 Proceedings (Cat. No.00TH8486)* (Vol. 1, pp. 371–374).

- Garcia Sanchez, F. J., Ortiz-Conde, A., & Muci, J. (2006). Understanding threshold voltage in undoped-body MOSFETs: An appraisal of various criteria. *Microelectronics Reliability*, 46(5), 731–742.
- Glaser, J. S., Nasadoski, J. J., Losee, P. A., Kashyap, A. S., Matocha, K. S., Garrett, J. L., et al. (2011). Direct comparison of silicon and silicon carbide power transistors in high-frequency hard-switched applications. In *2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)* (pp. 1049–1056).
- Jouha, W., Oualkadi, A. E., Dherbécourt, P., Joubert, E., & Masmoudi, M. (2017). A new extraction method of SiC power MOSFET threshold voltage using a physical approach. In *2017 International Conference on Electrical and Information Technologies (ICEIT)* (pp. 1–6).
- Levenberg, K. (1944). A method for the solution of certain non-linear problems in least squares. *Quarterly of Applied Mathematics*, 2, 164–168.
- Marquardt, D. W. (1963). An algorithm for least-squares estimation of nonlinear parameters. *Journal of the Society for Industrial and Applied Mathematics*, 11(2), 431–441.
- McNutt, T. R., Hefner, A. R., Mantooth, H. A., Berning, D., & Ryu, S. H. (2007). Silicon carbide power MOSFET model and parameter extraction sequence. *IEEE Transactions on Power Electronics*, 22(2), 353–363.
- Ortiz-Conde, A., Garcia-Sanchez, F. J., Muci, J., Tern Barrios, A., Liou, J. J., & Ching-Sung, H. (2013). Revisiting MOSFET threshold voltage extraction methods. *Microelectronics Reliability*, 53(1), 90–104.
- Ortiz-Conde, A., Garcia Sanchez, F. J., Liou, J. J., Cerdeira, A., Estrada, M., & Yue, Y. (2002). A review of recent MOSFET threshold voltage extraction methods. *Microelectronics Reliability*, 42(4), 583–596.
- Ortiz-Conde, A., Rodriguez, J., Garcia Sanchez, F. J., & Liou, J. J. (1998). An improved definition for modeling the threshold voltage of MOSFETs. *Solid-State Electronics*, 42(9), 1743–1746.
- Raynaud, C., Tournier, D., Morel, H., & Planson, D. (2010). Comparison of high voltage and high temperature performances of wide bandgap semiconductors for vertical power devices. *Diamond and Related Materials*, 19(1), 1–6.
- Simonot, T., Rouger, N., Nguyen, X. H., Créquier, J. C., Bourennane, A., Sanchez, J. L., et al. (2010). Tension de seuil réduite pour composants de puissance à grille: Intérêts et conséquences. *Électronique de Puissance du Futur* (p. 4). Saint-Nazaire, France.
- Terada, K., Nishiyama, K., & Hatanaka, K.-I. (2001). Comparison of MOSFET-threshold-voltage extraction methods. *Solid-State Electronics*, 45(1), 35–40.
- Tsuno, M., Suga, M., Tanaka, M., Shibahara, K., Miura-Mattausch, M., & Hirose, M. (1998). *Reliable threshold voltage determination for sub-0.1 micron gate length MOSFETs* (pp. 111–116).
- Tsuno, M., Suga, M., Tanaka, M., Shibahara, K., Miura-Mattausch, M., & Hirose, M. (1999). Physically-based threshold voltage determination for MOSFET's of all gate lengths. *IEEE Transactions on Electron Devices*, 46(7), 1429–1434.
- Wong, H. S., White, M. H., Krutsick, T. J., & Booth, R. V. (1987). Modeling of transconductance degradation and extraction of threshold voltage in thin oxide MOSFET's. *Solid-State Electronics*, 30(9), 953–968.
- Zhao, T., Wang, J., Huang, A. Q., & Agarwal, A. (2007). Comparisons of SiC MOSFET and Si IGBT based motor drive systems. *2007 IEEE Industry Applications Annual Meeting*, 331–335.



W. Jouha Ph.D. student in thesis co-supervision between Abdelmalek Essaadi University, National school of applied sciences of Tangier, Morocco and University of Rouen, GPM Laboratory, Rouen, France. In 2014, he graduated as an engineer in electronics and automatic systems from National school of applied sciences of Tangier, Morocco. His thesis research concerns the study and modeling of power SiC MOSFETs degradations subjected to thermal and electrical constraints.

Ahmed El Oualkadi (M'02) received Ph.D. degree in electronics from the University of Poitiers, France, in 2004. From 2000 to 2003, he was a research assistant in the Laboratoire d'Automatique et d'Informatique Industrielle—Ecole Supérieure d'Ingénieurs de Poitiers, Electronics & Electrostatics Research Unit, University of Poitiers, France. In 2004, he was an assistant professor at University Institute of Technology, Angoulême, France. In 2005, he joined the Université Catholique de Louvain, Microelectronics Laboratory, Louvain-la-Neuve, Belgium, as a research fellow where he worked on the analog and mixed design of low power high temperature circuits and systems, in SOI technology, for wireless



communication. During this period, he has managed and participated in several European and regional projects in the areas of wireless communication and sensor networking. Currently, he is an associate professor in the Abdelmalek Essaadi University, National school of applied sciences of Tangier, Morocco. His main research interest is the analog IC, mixed-signal, RFIC and MMIC design for wireless communication and electronic circuit reliability.



Pascal Dherbécourt received a diploma degree and a Ph.D in physics of electronics of telecommunication in 2002. Between 1999 and 2008, he worked in the field of optical fibers telecommunications. In 2008, he joined the GPM Laboratory of University of Rouen and became co-founder and a member of Erdefi team (research team in reliability and failure analysis of electronic components). His main research interests are now reliability and failure analysis of high power microwave transistors for telecommunication and RADAR applications and switching power components. He is engaged in several national and international research projects. He participates in numerous

research projects in collaboration with major companies. He is the author and co-author of more than sixty articles in international journals and congresses. At University of Rouen, he found a bachelor program in electronics in 2005, he also develops training programs for aeronautics and space business.



Eric Joubert (born in 1965) received an MSc degree in electrical engineering from ESIGE-LEC Rouen, France in 1988 and the PhD degree in electrical engineering from University of Rouen, France, in 1993. He first worked at LCIA/INSA de Rouen from 1993 to 1998 in cartographic polarisation analysis for 3D metrology. He joined LEMI/University of Rouen in 1998 and began works on polarization effects in high speed optical fibers. He is now

working in GPM (Groupe Physique des Matériaux, UMR CNRS 6634) as associate professor. His major research interests also include polarization effects characterisation in optical system, optical metrology and micro-electronic behaviour characterisation by electroluminescence analysis.



Mohamed MASMOUDI received the Ph.D. degree in materials science from the University of Rouen, France, in 1997. He joined LEMI / University of Rouen in 1998 and began work on the electrical characterization of semiconductors. He is now working in GPM (Groupe Physique des Matériaux, UMR CNRS 6634). He has carried out research on transistors and his current major research interests include microelectronic reliability on power transistors like silicon-carbide metal-oxide-semiconductor field-effect transistors (MOSFET SiC).