Design of Asymmetrical Doherty GaN HEMT Power Amplifiers for 4G Applications

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Abstract. In this paper, a 2-stage Doherty power amplifier and a single class B at 3.800 GHz, based on a 10 W GaN-HEMT technology using the bandwidth up to 6 GHz have been designed. The Doherty structure employs a class B bias condition for the main and a class C configuration for the auxiliary devices in the Agilent's ADS design platform. An uneven Wilkinson power divider is applied to deliver more power to the auxiliary device in order to achieve proper load modulation. The RF performances of the Doherty amplifier have been compared with those of a class B amplifier alone. The simulation results exhibit that the Doherty architecture can be considered as an ideal candidate for maximizing average efficiency while simultaneously maintaining amplifier linearity.

Keywords: Doherty amplifier · Power amplifier · High efficiency

1 Introduction

Mobile telecommunication systems typically use complex modulation standards to send more information in a very dense constellation. It is common to have high data rate signals with large envelope fluctuation in the time domain resulting in high peak-to-average (PAR) ratio. In order to prevent in-band distortion and out-of-band emission as well as to satisfy the stringent linearity requirements imposed by the wireless communication standards, the Power Amplifier (PA) are usually operated at the back-off region leading to thermal problems, high energy consumption and/or shorter battery life. Therefore, the key issue in modern PA design is to develop techniques that are capable of improving the average efficiency and to reduce the power wastage. Several architectures have been proposed to enhance the average efficiency of the PA when excited with modulated signals [1]. Among them, the Doherty power amplifier using gallium–nitride (GaN) transistor, has been extensively investigated and widely deployed in modern digital transmitters [2].

The basic idea behind the Doherty amplifier is to employ an impedance inverting network to modulate the load presented to the carrier amplifier according to the current supplied by the Auxiliary device, leading to efficient operation [3].

The basic structure of the two stages DPA is depicted in Fig. 1. The modern DPAs are usually implemented by a proper combination of two active devices that operate as Carrier and Peaking power stages. It consists of a power splitter to properly divide the input signal to the device gates, and an output power combining network including an impedance inverter, to sum in phase the signals arising from the two active devices, and impedance transformer connected to the output load. Finally, a phase compensation network connected at the input of the peaking device compensates the phase variation introduced by the impedance inverter.
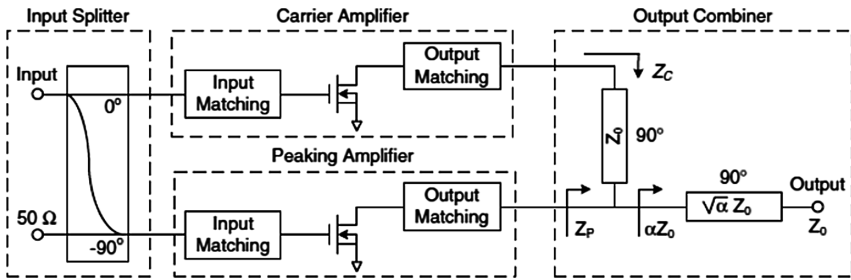

Fig. 1. Doherty power amplifier scheme [4]

Replacing the main and peaking transistors with two equivalent current sources in Fig. 2, the impedance seen by the Main amplifier can be changed by varying the current supplied of the peaking device, while the voltage swing across the Main has to be constant to maximize the efficiency. Therefore, it is necessary to impose an Impedance Inverting Network between the load and the main source. It is assumed that each current source is linearly proportional to the input voltage signal, in such a way, that the constant voltage value at the main terminals will be transformed into a constant current at the other terminals, without considering the value of the load [5].
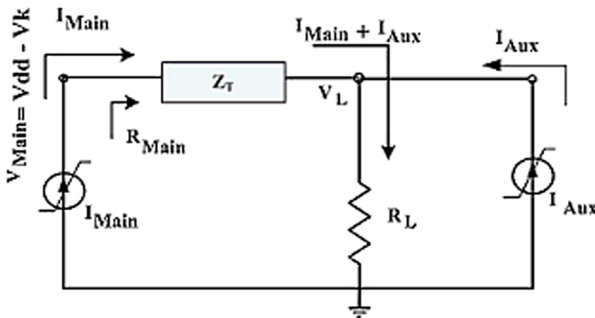

Fig. 2. Structure of equivalent circuit of Doherty amplifier

The organization of this paper is as follows: the working principle of the Doherty Power Amplifier is presented in Sect. 2; a single power amplifier and a Doherty power amplifier are designed in Sect. 3 by using the Cree's CGH40010 transistor in the 3.800 GHz band frequency available in the Agilent's ADS2016.01, whilst the DPA's input uneven power driving used to drive both the Main and the Auxiliary devices, and power combiner are discussed in this section. Then the DPA power gain behavior is discussed and compared with that of single PA according to simulation results; and finally in Sect. 4 the conclusion is given.

2 Doherty Amplifier Operation

The Doherty power amplifier has two distinct operating regions. The simplified output section of a DPA in the two operating regions is shown in Fig. 3. The first region known as the low power region, the power amplifier operates in the class of operation chosen for the main amplifier (in this work Class-B with short circuit harmonics). In this stage, there is not enough input power to turn on the auxiliary PA, which typically is biased in Class C condition. The requirement for this region is to maximize the efficiency by finding the optimum impedance whereby maximum voltage swing can be achieved at back-off [6]. In such a way, when the input power increases, the output power and efficiency increases at twice the normal growth rate.
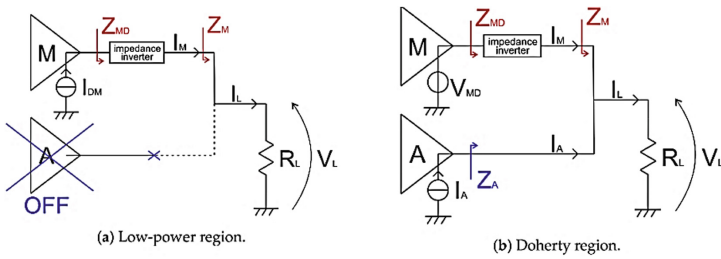

Fig. 3. Simplified equivalent output section of a Doherty Power Amplifier (DPA).

The second region is known as the Doherty power region, when the Main device drain voltage reaches its maximum swing at the desired back-off point, and cannot be increased any further; the Auxiliary amplifier is conducting current into the output load, as can be seen in Fig. 3. Since the Main PA preserves a constant output, voltage with increasing output current, the perceived impedance decreases towards the value of the characteristic impedance due to the quarter-wave impedance transformer [6]. The Main PA now acts as a controlled voltage source, operating at peak efficiency and delivers an increasing amount of power, while the Auxiliary device acts as a controlled current source where increasing the current and voltage swings, in proportion to the input voltage, leads to a reduction in the output impedance. At the end, for the peak envelope value, both devices achieve their saturation and observe an optimum resistance equal to the characteristic impedance of quarter-wave line.

Figure 4 shows the ideal behavior of the Main and Auxiliary PA efficiency. For the low power region, the efficiency of a Doherty amplifier is very similar to the efficiency of Class-B amplifier, however, it reaches the maximum value at the back-off point as a result of using twice the optimum load value. At the Doherty region, the efficiency of the Main device remains constant, due to the constant level of saturation, while the efficiency of the Auxiliary device starts to increase. The Doherty architecture is capable of providing the same maximum efficiency over the 6 dB power range.
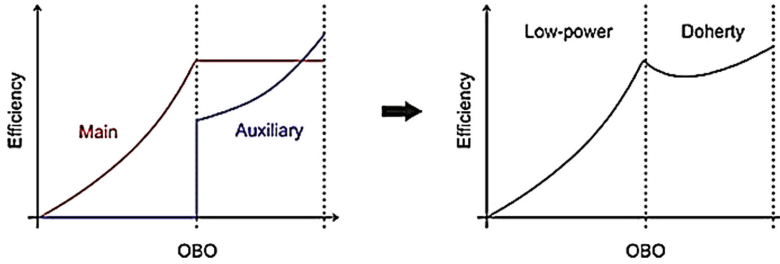

Fig. 4. Class-B/C Doherty power amplifier efficiency.

3   Design of Doherty Power Amplifier

In order to design a class B power amplifier as the Main device, the operating point of the transistor is located exactly at the boundary between the cutoff region and the active region (at –3.1 V) at the gate and 28 V at the drain, is set at the zero quiescent current so it conducts 50% of the RF and the drain current is a half-sinusoid. Figure 5(a) and (b) are the characteristics of the CGH40010F transistor, which show the variation of the drain current as a function of VDS and VGS respectively.
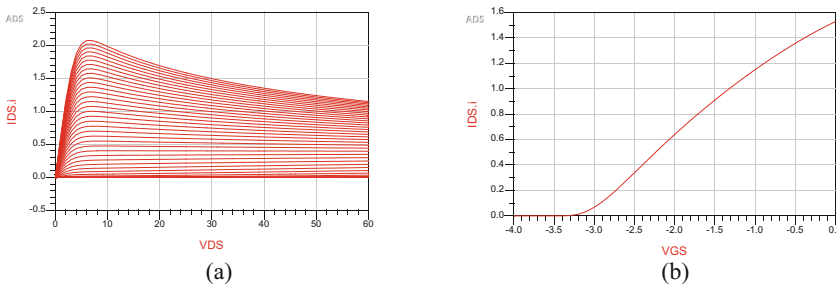

(a)   (b)

Fig. 5. (a) Plot of IDS vs VDS curvatures for different values of VGS and (b) Plot of IDS vs VGS for VDS = 28 V (The datasheet recommend 28 V at the drain.)

To find the optimal output impedances of the transistor operating in the linear region, the load pull simulation is performed using the non-linear model of the transistor. An optimum impedance for maximum efficiency at the low power region for the

main branch, and the optimum impedance for maximum power on the high power regime for both the main and peaking in the DPA must be selected. In order to determine the optimum load that device should see, the efficiency and output power in operating frequency are tracked through varying load impedances and proper impedances deliver maximum efficiency and maximum power should be selected.

In Fig. 6, the single load impedance in the center point of the PAE contours that gives the maximum efficiency of 68.27% - is selected for the output matching network. The output matching network imposes an optimum load for the fundamental frequency, and zero to second and third harmonics in class B (class B exploits the harmonics to increase efficiency). In order to minimize the signal reflection at the input of power amplifier, the input impedance of the PA should be matched with the characteristic impedance of the input source. The input matching circuits implements the conjugate matching between complex impedance of the power amplifier and the signal source impedance.
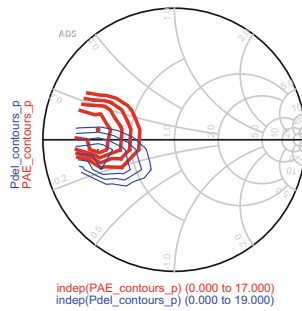

indep(PAE_contours_p) (0.000 to 17.000)
indep(Pdel_contours_p) (0.000 to 19.000)

Fig. 6. Load-Pull contours at 3.8 GHz (Blue - Power output; Red - PAE). (Color figure online)

As shown in Fig. 7, the output matching network of the DPA is composed by offset transmission lines with characteristic impedance of 50 Ω, connected after the matching circuits of the carrier and peaking amplifiers. The peaking transistor should be able to deliver sufficient output power to ensure proper load modulation for the main amplifier; therefore, an uneven power divider is designed and optimized in order to provide more power to the peaking amplifier than to the carrier PA from the source. The asymmetric powers are combined by the Doherty operation through a quarter-wave impedance converter. Consequently, a second quarter-wave transmission line should be added at the input of the Auxiliary PA to properly compensate the phase shifting introduced by the output λ/4 transformer.

3.1   Offset Line

The offset lines are very important components following the Main and Auxiliary amplifiers for proper load modulation. As shown in Fig. 8, in the low-power region, the load impedance seen by the Main amplifier become double and the output matching network of the main PA is designed to match the optimum impedance determined in
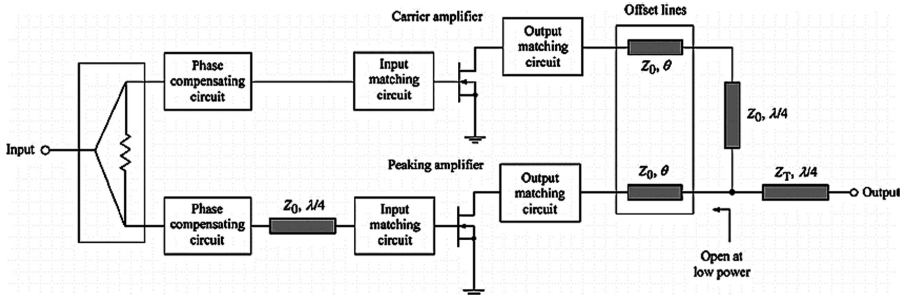
Fig. 7. Two-way Doherty amplifier block diagram

load pull for maximum efficiency and $2Z_{opt}$ to maximize the efficiency and gain; whilst at the output of the peaking amplifier, the offset line is adjusted to high impedance, as close as possible to an open circuit to prevent power leakage to the Main amplifier. The offset lines do not affect the overall matching condition and load modulation [7]. In the high power region, the main and peak currents sum in-phase and decreases. The load impedance of the carrier amplifier varies from $2Z_{opt}$ to Z_{opt}, and the peaking amplifier during the load modulation operation varies from infinite to Z_{opt}. The efficiency of the Doherty amplifier at the maximum input voltage is equal to the maximum efficiency of the amplifiers.
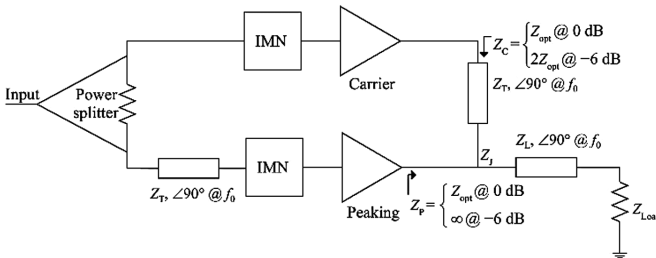

Fig. 8. Load-network schematic for each amplifier at the low and high power regions.

3.2   Power Splitter Design

In order to obtain high efficiency, an uneven Wilkinson power divider presented in Fig. 9 that is applied at the input circuit of the Doherty PA. In this work, the ratio between the input power of the carrier amplifier and peaking amplifier is 2:1. In fact, the peaking amplifier should be approximately double-sized of main amplifier to receive more power. As can be seen in Fig. 9, that unequal-split Wilkinson divider consist of four transmission lines with characteristic impedances of $Z0$, joined at their outputs with a resistor [8], which is located between the pads at the outputs.
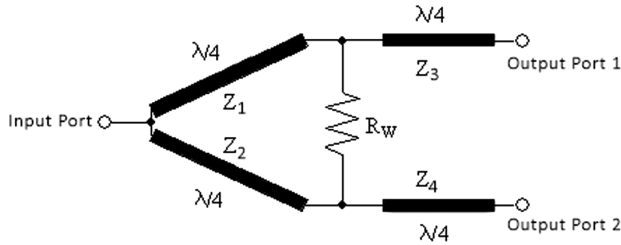
Fig. 9. Topology of unequal Wilkinson power splitter [9]

The asymmetrical input power splitting ensures a very good isolation between the main and peaking ports, and it also causes the saturation delay of the peaking amplifier to maintain high efficiency in the DPA over a wide dynamic range of the back-off power region. The amplifiers with uneven power drive show more efficient operation, with approximately 10–13% increase in ranges of drain efficiency and produce more power than even drive [10]. However, an uneven Doherty amplifier provides less linear gain in the low power region due to the smaller input power delivered to the main amplifier.

3.3 Output Combining Network Design

The Doherty output combining circuit consists of a quarter-wave transmission line with characteristic impedance of 50 Ω, which provides required phase delay and a quarter-wave transmission line of 35.35 Ω impedance that transforms the common load impedance to the final load impedance of 50 as shown in Fig. 10. In the low-power region, where the peak amplifier is turned off, the combining circuit acts as a 1:2 impedance transformer, providing the required load pulling for the main amplifier. In the case of the high power region, particularly at the maximum power point when the main and peak amplifiers deliver equal amounts of output power, the combining circuit functions as a 1:1 combiner.
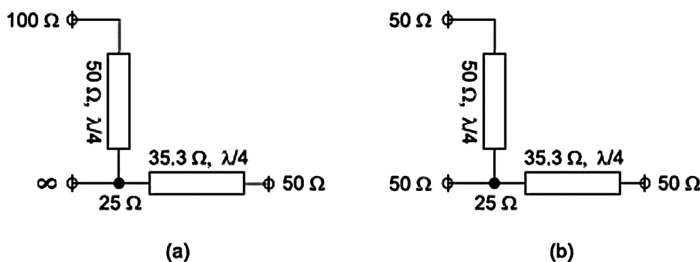

Fig. 10. Output combining network (a) in the low-power region and (b) at maximum power point where the output currents of the main and peaking amplifiers are combined [11].

3.4   Single Amplifier Design

The Class B power amplifier design contains bias networks, input-output AC matching networks, and the open stubs connected in parallel. The schematic simulation results in Fig. 11 indicate a small signal transducer gain to be flat at around 15 dB, and when the gain compression starts the gain decreases with increasing output power. The efficiency of the PA is an important measure of the battery life of the wireless transceivers. At 3.800 GHz the maximum drain efficiency of class B is 60.30% at input power of 35 dBm. This implies that the amplifier enters saturation after it reaches an output power of 40.58 dBm. The Power amplifier class B indicates a PAE of 54.71% at the output power of 40.12 dBm, and input power of 29 dBm.
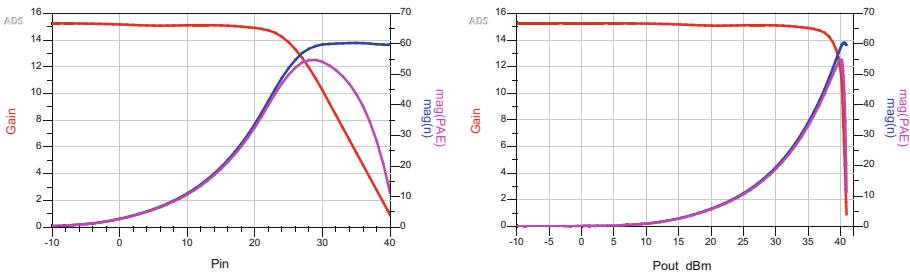

Fig. 11.   Simulation results of gain, PAE and efficiency.

3.5   Doherty Amplifier Design

In the proposed design, the single designed class B amplifier is used as the main amplifier. Hence, to complete the Doherty design, a class C amplifier is necessary as a peak amplifier with a supply voltage of 28 V. In order to maintain maximum power transfer, matching circuits are designed at the input and the output of the transistor realized by micro-strip transmission lines as well as bias networks. The used substrate within this work is Rogers4350B substrate with dielectric constant $\varepsilon r = 3.66$ and thickness h = 0.762 mm.

The results of power sweep for harmonic balance simulation is shown in Fig. 12. When the input signal is working at 3.800 GHz, it shows that due to the class C bias state of the peak transistor in the Doherty amplifier, the gain flatness of the Doherty amplifier is worse than the Single class B, which is flat at around 12 dB. On the contrary the power-added efficiency (PAE) of the Doherty amplifier at the output power of 35 dBm point is 52.2%, 10.2% higher than that of the single amplifier and the power-added efficiency of the Doherty amplifier at the maximum output power reaches 60.42%. It clearly indicates that the efficiency of the DPA is higher than that of the class B power amplifier. This is due to the Doherty principle and the electrical lengths of the delay and impedance inverter transmission line previously mentioned.

Figure 13 shows the appropriate impedance transformations on a Smith chart to determine the offset line length of each amplifier.
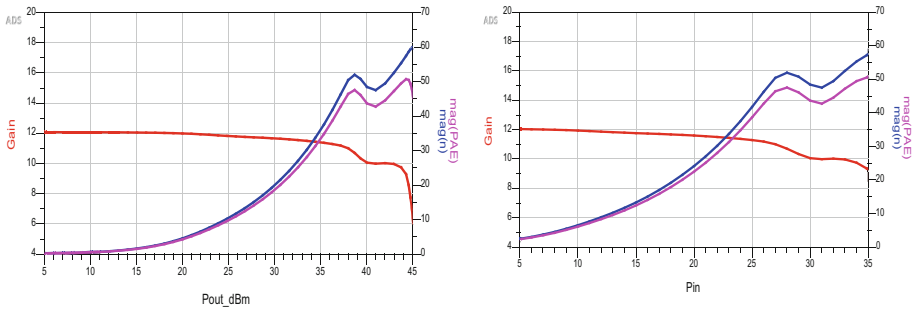
Fig. 12. Simulation results of Gain, PAE and efficiency.
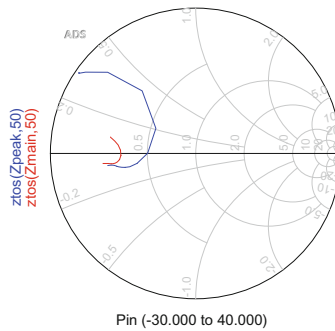

Fig. 13. Impedance transformations on the Smith chart. Red curve: the main amplifier, blue curve: peaking amplifier. (Color figure online)

Figure 14 shows the main and auxiliary device RF current and voltage amplitudes over the whole power range. It is clear that the peaking amplifier dose not consume any current at the low power region. Their voltage and current are close to 0 until 6 dBm.
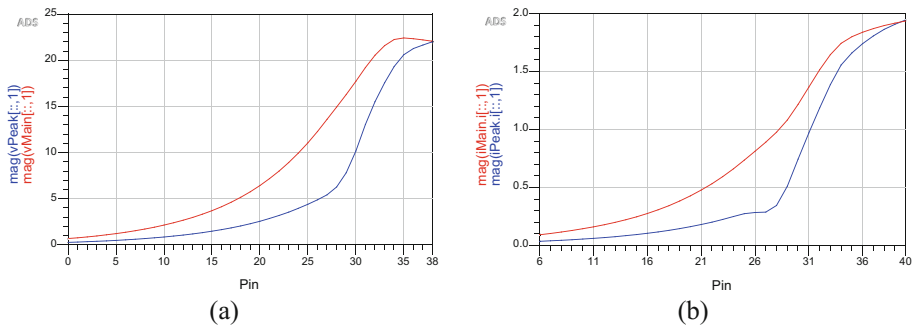

Fig. 14. (**a**) The output voltages of the carrier and the peaking amplifiers, (**b**) The output currents of the carrier and the peaking amplifiers.

For the upper 6 dB region, the peaking amplifier, and due to the Class-C bias, draws more input power, and also the current and voltage of the peaking amplifier increases very rapidly. At the maximum power point, the carrier and peaking amplifiers achieve the same amplitudes of current and voltage.

4   Conclusion

A class B power amplifier and a Doherty structure have been designed using a 10-W packaged GaN device (CGH40010) from Cree Inc. The single power amplifier class B is biased at threshold voltage. In order to drive the amplifier into the compression point, a 35 dBm of input power is required. At 3.800 GHz, the maximum drain efficiency of the PA is 60.30% at output power of 40.58 dBm. Also, the design procedure and final performance of a Doherty PA have been presented. The carrier amplifier and peaking amplifier were biased in Class-B and Class-C conditions, respectively, with a drain voltage of 28 V. In this design, the matching networks of the carrier and peaking amplifiers were designed to maximize the delivered power to the output. An offset line has been added at the output of the peaking amplifier in order to ensure the open circuit condition at the low power drive levels. This DPA attained an efficiency of 60.42% at 45.13 dBm output power. Thus, the DPA increases the power efficiency, especially at high power levels, in comparison with class B when they operate at their saturation level.

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