Chapter 7
Nature-inspired Single-electron Computers

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7.1 Introduction

A single-electron circuit is one that creates electronic functions by controlling movements of individual electrons [11]. The circuit uses tunneling junctions, each of which generally consists of two conducting materials facing each other very closely (statically, they are normal capacitors). Under a low-temperature environment, electron tunneling is governed by the physical phenomenon called the Coulomb blockade, where an electron does not tunnel through a junction if the tunneling increases the circuit's electrostatic energy (E_c). To comply with the Coulomb blockade, the capacitance of a tunneling junction must be sufficiently small; for example, if we use 1 pF of capacitance, E_c corresponds approximately to 1 mK in temperature (T). Generally, observing the Coulomb blockade in practical experimental environment (e.g., $T \sim 0.1$ K) is difficult because the blockade effect is disturbed by thermal fluctuations. Therefore, elemental devices of single-electron circuits, that is, tunneling junctions and capacitors, must be constructed in nanoscale (lower than a few tens of nanometers).

These intrinsic quantum behaviors may give us an insight in developing modern computing paradigms, including nature-inspired computing and quantum computing. However, if we employ conventional (deterministic) computing architectures, we need a fully worked-out plan for both computing and circuit architectures, for example, see [5, 10, 27, 29, 30]. Thermal noise tolerance is an important characteristic of single-electron computers, because the rate of random electron tunneling increases exponentially as the temperature increases. Several practical circuits have been developed by improving the process for fabricating ultra-low capacitance of tunneling junctions [29] and by using an error-compensation algorithm in the architecture [27].

On the other hand, one can easily observe robust, fault- and noise-tolerant systems in nature. For example, nature-inspired reaction-diffusion (RD) computers [3] can perform specific computing under natural environment without paying much

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attention to, for example, device-size variations, thermal fluctuations, etc., as compared to present nanoscale semiconductor artifacts for both analog and digital computing. How can we incorporate such robust properties into single-electron circuits? One possible way is to build an electrically equivalent circuit that implements convenient natural systems, for example, RD computers. Complementary metal-oxide-semiconductor (CMOS) and single-electron circuits for image restoration and computation of a Voronoi diagram (VD) have already been proposed in [20, 28]. The other way is to learn from central nervous systems where neurons are fluctuated by thermal noises, as well as single-electron circuits. Neurons would utilize thermal noise to detect weak neuronal signals buried under the noise. The reappearance of neuronal behaviors and matching properties between neurons are really poor compared with semiconductor neural devices; nevertheless, our brains work robustly.

Constructing an electrical analog of natural or biological systems would enable us to generate artificial dynamics on a LSI chip and to develop novel information processing systems. This chapter briefly introduces recent topics on the development of single-electron circuits that perform nonclassical computation inspired by chemical or biological systems. In Sect. 7.2, a novel single-electron device for the computation of a VD is introduced. A cellular-automaton model of VD formation [1, 2] is employed to construct the device that consists of three layers of a 2D array of single-electron oscillators. In Sect. 7.3, a single-electron neural circuit for a robust synchrony detection among burst spikes is presented. A simple single-electron circuit for a single-layer nanodot array is designed for implementing depressing synapses for efficient synchrony detection. The circuit can be used as a unit element for spiking neural networks and its applications. Although the synapse circuit consists of only three single-electron oscillators, they emulate fundamental properties of depressing synapses. This work has been extended to utilize stochastic resonance between single-electron neurons for possible robust computation on single-electron circuits (Sect. 7.4). In Sect. 7.5, a novel semiconductor device in which electronic-analogue dendritic trees grow on multilayer single-electron circuits is introduced as an extreme example of artificial life on single-electron circuits.

7.2 A Single-electron Reaction-diffusion Device for Computation of a Voronoi Diagram

Computation of VD is one of the typical problems in computer science, and VDs are used in graphics, statistics, geography, and economics [14, 18]. The key feature of VD construction is the partition of two- or three-dimensional space on a sphere of influences generated from a given set of objects, points, or arbitrary geometrical shapes. This section introduces a novel single-electron device for the computation of a VD. A cellular-automaton model of VD formation [1, 2] is used to construct the device that consists of three layers of a 2D array of single-electron oscillators.

The authors and several colleagues have proposed to use single-electron reaction–diffusion (SE-RD) devices for VD computation [20]. The original SE-RD

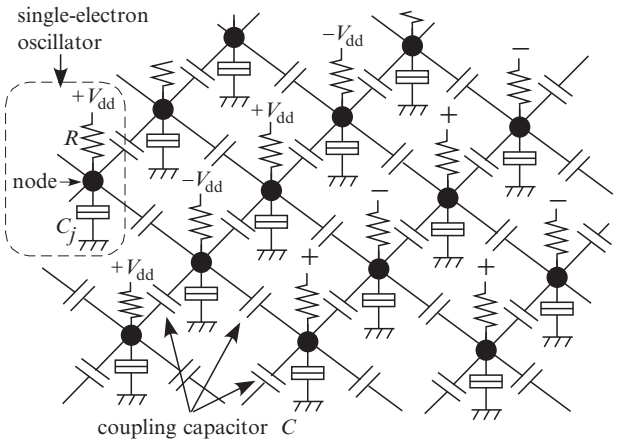

Fig. 7.1 Circuit configuration of single-electron reaction-diffusion device [23]

device consists of arrayed single-electron oscillators and can imitate the operation of chemical RD systems [23]. Figure 7.1 illustrates the original SE-RD device. The main component is a single-electron oscillator that consists of a tunneling junction C_j and a high resistance R connected in series at a node and biased by a positive voltage V_{dd} or a negative one $-V_{dd}$. It has voltage V_{node} of the node, and V_{node} shows the excitatory oscillation that is indispensable for imitating RD systems [23].

To compute a VD with RD systems, spatially localized waves that travel upon computing media at a constant speed are necessary [1, 2], that is, the wavefronts must be smooth and their speed must be constant. The original SE-RD device can generate nonlinear voltage waves. However, the device was not suitable for computing a VD because the wavefronts were not smooth, as shown in Fig. 7.2, and their spreading speeds were not constant. The stochastic tunneling of electrons at each oscillator is the reason why the waves cannot travel at a constant speed. To make the wavefronts smooth and the speed of the waves constant, new oscillators in which the tunneling probability is averaged are necessary. Therefore, the authors have developed new single-electron oscillators with multiple-tunneling junction (MTJ) as shown in Fig. 7.3. The MTJ oscillator consists of a MTJ C_m that has n tunneling junctions and a high resistance R connected in series at the node, and is biased by V_{dd}. It has voltage V_{node} that shows the excitatory oscillation like the original oscillator does. There are many tunneling junctions in the oscillator, and so the tunneling probability is averaged. Consequently, V_{node} changes smoothly as shown in Fig. 7.3b. The improved SE-RD device consists of these MTJ oscillators [20].

Adjacent oscillators have to be coupled with a capacitor for the voltage waves to travel on the MTJ device. Figure 7.4 shows simulation results of a one-dimensional chain of MTJ oscillators. In the figure, MTJ oscillators are denoted by A1, A2,..., with their nodes represented by closed circles that are connected to their adjacent oscillators through intermediary oscillators biased by a negative voltage $-V_{dd}$ (these are denoted by B1, B2, ..., with their nodes represented by open circles) and coupling

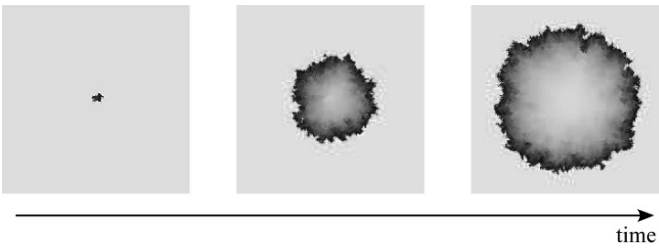

Fig. 7.2 Spatially localized voltage wave that is generated by the original SERD device (simulated). The device has 100×100 oscillators. Simulated with parameters: tunneling junction capacitance $C_j = 1$ aF, tunneling junction conductance = 1 μS, high resistance $R = 137.5$ MΩ, coupling capacitance $C = 1$ aF, bias voltage $V_{dd} = 16.5$ mV, and zero temperature [23]

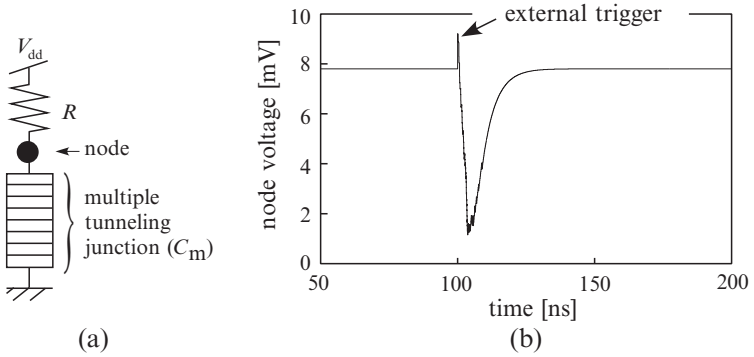

Fig. 7.3 Single-electron oscillator with multiple-tunneling junction. (**a**) Circuit configuration and (**b**) its operation (simulated). Simulated with parameters: tunneling junction capacitance $C_m = 10$ aF (500 aF/50 junctions), tunneling junction conductance = 5 μS, high resistance $R = 20$ GΩ, bias voltage $V_{dd} = 7.8$ mV, and zero temperature

capacitors C (Fig. 7.4a). When electron tunneling occurs in one oscillator in this structure, the node voltage of the oscillator decreases gently, and this induces electron tunneling in an adjacent intermediary oscillator. The induced tunneling changes the node voltage of the intermediary oscillator from low to high, and this further induces electron tunneling in an adjacent oscillator. Consequently, changes in node voltage that are caused by the electron tunneling are transmitted from one oscillator to another along the oscillator chain (Fig. 7.4b). Note that the voltage waves travel at almost constant speed because the tunneling probability is averaged over all oscillators.

A SE-RD device can be constructed by connecting MTJ oscillators into a network by means of intermediary oscillators and coupling capacitors, as shown in Fig. 7.5. Each oscillator is connected to its four adjacent oscillators by means of four intermediary oscillators and coupling capacitors. Nonlinear voltage waves travel on the device at a constant speed, as shown in Fig. 7.6. One can compute VDs by using

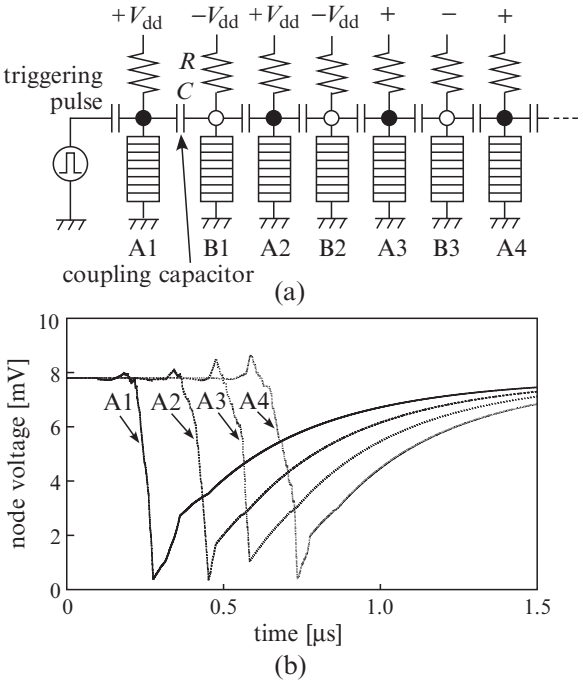

Fig. 7.4 One-dimensional chain of MTJ oscillators. (**a**) Circuit configuration and (**b**) its operation (simulated). Simulated with parameters: tunneling junction capacitance $C_m = 10\,aF$ (500 aF/50 junctions), tunneling junction conductance = 5 μS, high resistance $R = 20\,G\Omega$, coupling capacitance $C = 2.2\,aF$, bias voltage $V_{dd} = 7.8\,mV$, and zero temperature

the information on the collision points of the nonlinear waves. In [1, 2], a cell that connects eight adjacent cells changes its state according to the states of the adjacent cells. The cell state transition rule is

$$x^{t+1} = \begin{cases} \beta, & \text{if } x^t = \bullet \text{ and } 1 \le \sigma(x)^t \le 4, \\ \alpha, & \text{if } x^t = \beta \text{ and } 1 \le \sigma(x)^t \le 4, \\ x^t, & \text{otherwise,} \end{cases}$$

where x is the state of the middle cell, t is the time step, $\bullet$ is the resting cell, α is the colored precipitate, β is the reagent, and $\sigma(x)^t$ is the number of β cells in the eight adjacent cells. In this model, the collision points are memorized as the precipitate of reagents.

To apply this rule to single electron device, the authors used single-electron threshold detectors, specifically the single-electron boxes (SEB) for logic gate devices [19, 22]. The SEB consists of a single-electron trap (two identical tunneling junctions C_j connected in series, a capacitor C_L, and a bias voltage V_{dd}) as shown in Fig. 7.7a. This circuit has a hysteretic sawtooth function for V_{dd}, as shown in Fig. 7.7b. The authors made use of this characteristic for threshold operation.

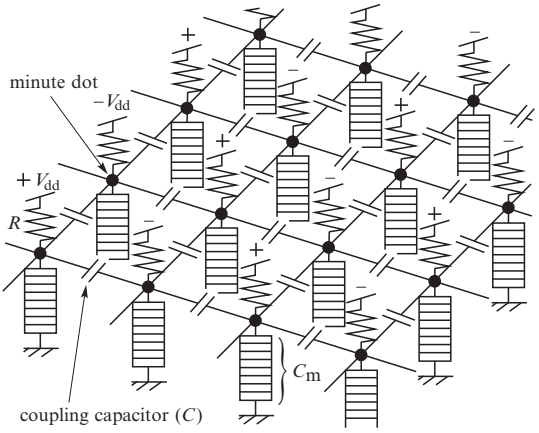

Fig. 7.5 Two-dimensional RD device consisting of network of MTJ single-electron oscillators. Each oscillator is connected with four neighboring oscillators by means of four intermediary oscillators and coupling capacitors

Fig. 7.6 Traveling nonlinear wave that is generated by the improved SE-RD device (simulated). 50×50 oscillators are placed in the device. This simulation used the same parameters as in Fig. 7.4b [20]

Let us consider the threshold operation for computing a VD based on the CA model, and assume the threshold value that is the number of β cells in the eight adjacent cells to be 4.5, that is, no electron tunneling occurs in the SEB when the node voltages of four or fewer adjacent oscillators are changed by electron tunneling in the oscillators. On the other hand, electron tunneling occurs in the SEB when the node voltages of five or more adjacent oscillators are changed. In addition, one can find the collision points by comparing the state of the center oscillator with the state of the SEB threshold detector. To compare the states, SEBs with the threshold set to 1.5 can be used, that is, no electron tunneling occurs in the SEB when electron tunneling occur in both the above SEB and the center oscillator.

Figure 7.8 shows a SE RD device with three layers for computing VDs. The top layer (Fig. 7.8a) is the MTJ device shown in Fig. 7.5. The middle layer (Fig. 7.8b) is the first logic layer of SEB threshold detectors. The SEB that is biased by the negative voltage $-V_{b1}$ (Fig. 7.8e) are directly placed under the oscillators biased by $+V_{dd}$ (oscillator 9 in Fig. 7.8) and connects to the eight adjacent oscillators of the top layer (oscillators 1–8 in Fig. 7.8d), that is, the SEB accepts eight signals from the

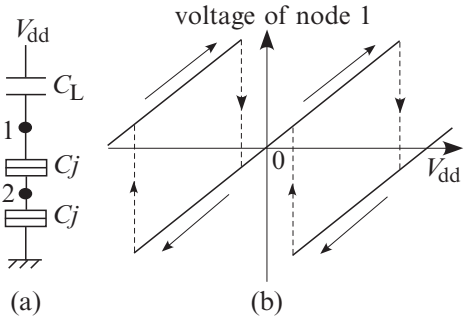

Fig. 7.7 Single-electron box. (**a**) Circuit configuration and (**b**) its operation [19, 22]

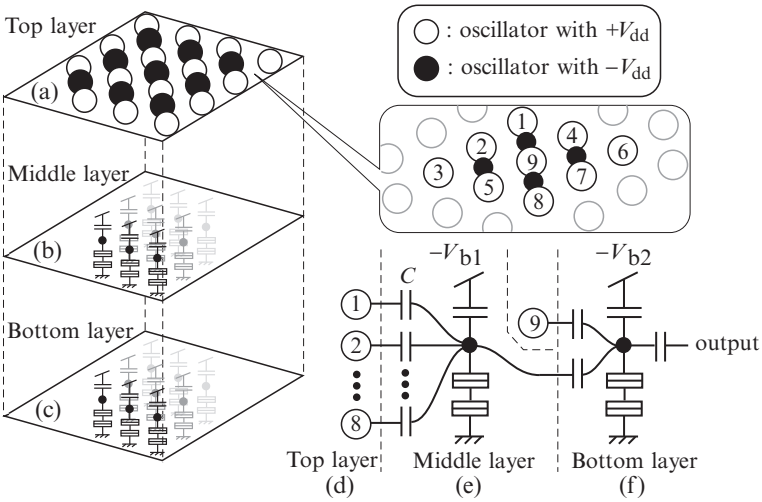

Fig. 7.8 SE RD device that has three layers for computing VDs. The top layer is the device shown in Fig. 7.5. The middle layer is the first logic layer with SEB threshold detectors. The bottom layer is the second logic layer and it produces the VD

eight oscillators as inputs. The bottom layer (Fig. 7.8c) is the second logic layer. The SEB that is biased by the negative voltage $-V_{b2}$ (Fig. 7.8f) connects to the oscillator 9 and the SEB in the second layer (Fig. 7.8e), that is, the second SEB accepts two signals from the oscillator 9 and the SEB in the second layer as inputs. The bottom layer produces the output, that is, its output is used to draw the VD.

Figures 7.9–7.11 show the simulated results. Figure 7.9 shows the density of node voltages on the top layer (bright and dark dots represent high and low voltages on the 2D device). Figures 7.10 and 7.11 show the voltages on the middle layer and on the bottom layer. In Fig. 7.10, "A" indicates the wavefront in the top layer, "B" indicates the wave-front in the middle layer, and "C" indicates collision points. In this simulation, three oscillators of the top layer were triggered as planar points for a VD. Nonlinear voltage waves traveled at a constant speed, and gave the data

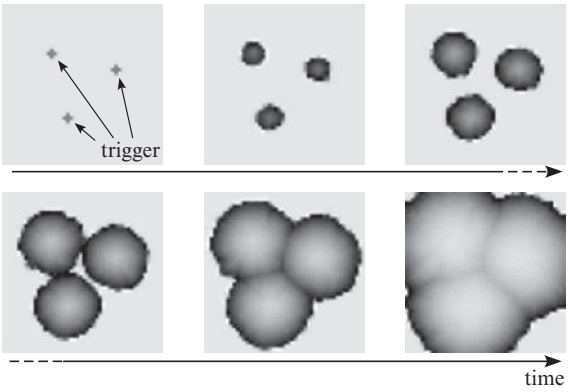

Fig. 7.9 Expanding circular pattern in the top layer of the device. Snapshots for six time steps. The simulation used the same parameters as in Fig. 7.4b for the simulation

to the middle and bottom layers. In the middle layer, the SEBs changed their node voltage when five or more oscillators of the upper eight oscillators changed their node voltage. Wavefronts in the top layer had four or fewer oscillators that changed their voltages. As a result, traveling nonlinear waves in this layer (B in Fig. 7.10) followed the waves in the top layer (A). When wave "A" collided with other waves in the top layer, the collision points had five or more oscillators that changed their voltages. Therefore, wave "B" in this layer overtook "A" and collided with other waves just like spanning a valley with a bridge (C). In the bottom layer, the SEBs changed their node voltages when both the voltage of the oscillators in the top layer and the SEBs in the middle layer are low. Namely, traveling waves that did not collide were memorized by the bottom layer as a high voltage. When the nonlinear waves of the top layer collided with each other, the voltages of the collision points in the top were low and the node voltages of the SEBs in the middle were high. As a result, the node voltages of the SEB in the bottom were kept low. Therefore, the bottom layer memorized the result of computing the VD (Fig. 7.12).

7.3 Neuronal Synchrony Detection on Single-electron Neural Networks

Synchrony detection between burst and nonburst spikes is known to be one functional example of depressing synapses. Kanazawa et al. demonstrated synchrony detection with CMOS depressing synapse circuits [12]. They found that the performance of a network with depressing synapses that discriminates between burst and random input spikes increases nonmonotonically as the static device mismatch is increased [4]. The authors have designed a single-electron depressing synapse and constructed the same network as in Kanazawa's study to develop

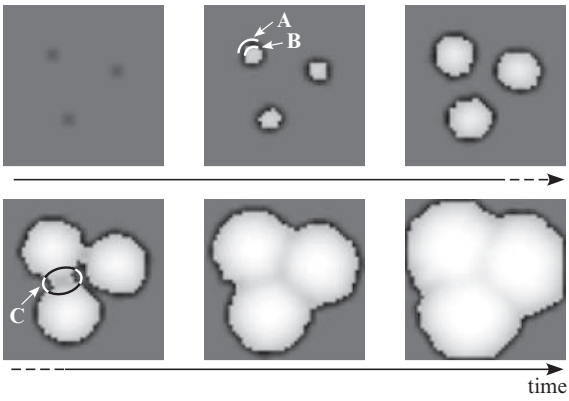

Fig. 7.10 Expanding circular pattern in the middle layer of the device. Snapshots for six time steps. Parameters: tunneling junction capacitance $C_j = 20\,\text{aF}$, tunneling junction conductance = $5\,\mu\text{S}$, bias capacitance $C_L = 10\,\text{aF}$, coupling capacitance $C = 2.2\,\text{aF}$, bias voltage $V_{b1} = 26.5\,\text{mV}$, and zero temperature

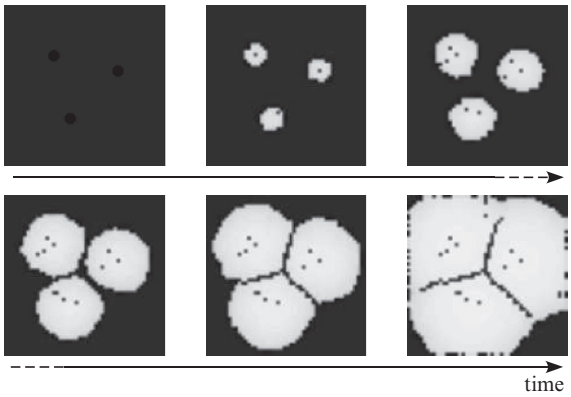

Fig. 7.11 Expanding circular pattern in the bottom layer of the device. Snapshots for six time steps. Traveling nonlinear waves in this layer construct a VD. Parameters are the same as in Fig. 7.10 without bias voltage $V_{b2} = 18.5\,\text{mV}$

noise-tolerant single-electron circuits. This section shows the temperature characteristics, and explores possible architecture that enables single electron circuits to operate over absolute zero temperature.

The authors and several colleagues have proposed neuromorphic single-electron circuits for fundamental neural components in modern spiking neural networks [24]. Our aim was to implement artificial neural networks on a single or multilayer nanodot array. A unit circuit consists of a pair of single-electron oscillators. Using these unit circuits with coupling capacitors, we design a single-electron neuron circuit that consists of excitable axons and dendrites, excitatory and inhibitory synapses, and a soma. The authors have demonstrated an application of the neuron circuit

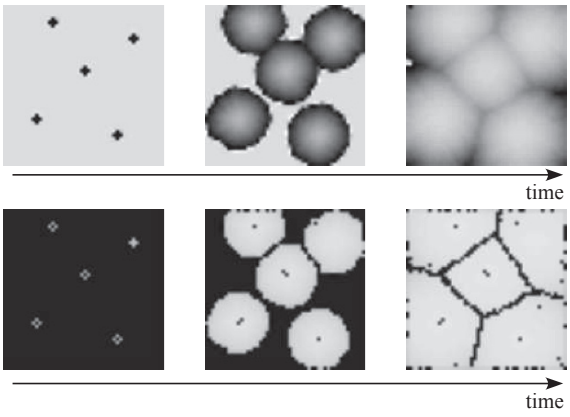

Fig. 7.12 Simulated results of VD computing with five planar points by using proposed device. Upper three snapshots show the voltage density of the top layer and the bottom three snapshots show the voltage density of the bottom layer

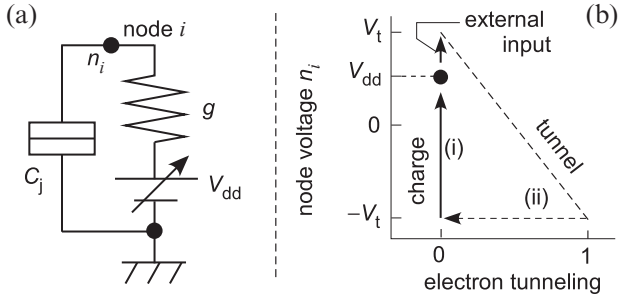

Fig. 7.13 Single-electron oscillator and phase diagram

in an inhibitory competitive neural network [24], where the neurons compete with each other in the temporal domain. However, we could observe expected neural competition at a very low temperature ($\leq$0.1 K). In this section, we explore a possible solution to improve the performance in another application, that is, neuronal synchrony detection, by using the proposed single-electron depressing synapse.

To design a depressing synapse circuit, we use a pair of single-electron oscillators that were proposed for a spiking neuron circuit [24] and an excitable media [23]. As shown in Fig. 7.13a, one oscillator consists of a tunneling junction (C_j), a conductive device (g), and a bias voltage source (V_{dd}). The oscillator has an island node n_i where excess electrons are stored. Figure 7.13b is a nominal phase diagram of this circuit for positive V_{dd}. The vertical and horizontal axes represent node voltage n_i and a tunneling phenomenon [= 1 (when an electron tunnels), 0 (else)] at C_j. Note that trajectories between the tunneling phenomenon (0 and 1) in the figure do

not have any quantitative physical meaning, but they have been used only to explain this circuit's operation. Let us assume that $V_{dd} < e/2C_j$ ($\equiv V_T$: tunneling threshold voltage of junction C_j). Because tunneling junction C_j is charged by V_{dd} [(i) in Fig. 7.13b], the circuit is stable when $n_i = V_{dd}$. Under this resting condition, if n_i is further increased by an external input and exceeds V_T, an electron tunnels from the ground to node i through junction C_j, which results in a sudden decrease in n_i from V_T to $-V_T$ [(ii) in Fig. 7.13b]. Then, V_{dd} starts charging C_j, and the circuit becomes stable again [(i) in Fig. 7.13b].

Note that there is a time lag from when the junction voltage exceeds V_T to when tunneling actually occurs. On can utilize this "monostable" (excitable) oscillatory property to produce the depressing characteristics of the synapses, that is, we regard an array of oscillators as a depressing synapse because input spike trains are depressed by each neuron operating in its refractory period. Therefore, we can use an array of single-electron oscillators to construct the single-electron depressing synapse (SEDS) shown in Fig. 7.14. It should be noted that the term of the refractory period increases as the values of g_{Na} and g_K increase [23].

A neuromorphic relationship exists between the proposed SEDS and electronic Hodgkin–Huxley (H-H) models: (1) a tunneling junction (C_j) corresponds to a membrane capacitance and voltage-controlled gates in the H-H models, (2) nonlinear chemical reactions between Na^+ and K^+ can be mediated by a coupling capacitance (C) because of the neuron's dielectric inside the soma.

Let us observe the depressing properties of a single SEDS through numerical simulations. Typical parameter values for the single-electron circuit [23], except for $g_{Na}(= g_K) = 5$, 2.5, and 1 μS were used. Figure 7.15 shows synaptic conductivities (approximately the number of post-synaptic spikes) for inter-spike intervals (ISIs) of input spike trains. As the ISI increases, the conductivity increases because each SEDS can easily be recovered from its depressed (refractory) period as the ISI increase. Because the depressed period increases as g_{Na} and g_K increase, the SEDS's conductivity for increasing ISIs decreases significantly.

Applications of SEDSs to synchrony detection has been demonstrated. We used a typical functional example of depressing synapses proposed by Senn [26]. He showed that an easy way to extract coherence information between cortical neurons is by projecting spike trains through depressing synapses onto a post-synaptic neuron [26]. We demonstrate it here by using single-electron synapse circuits.

Let us assume a simple circuit as shown in Fig. 7.16. The circuit is designed based on the construction of Senn's neural network. The bottom right part represents a post-synaptic neuron and the left part represents its dendrite with our synapse circuits. The post-synaptic neuron consists of a membrane capacitance (C_m) and a leak conductance (g_m). In this study, we omit a threshold (V_{th}) detector from the post-synaptic neuron circuit, that is, the post-synaptic neuron circuit never fires. The post-synaptic neuron accepts spike inputs from excitatory neurons through depressing synapses. If the post-synaptic neuron circuit has a firing function, it outputs a spike when its EPSP $< V_{th}$, and resets the EPSP after the firing. In this setup, the average values of the EPSP increase in proportion to the number of pre-synaptic active neurons. Therefore, it can detect the number of pre-synaptic active neurons

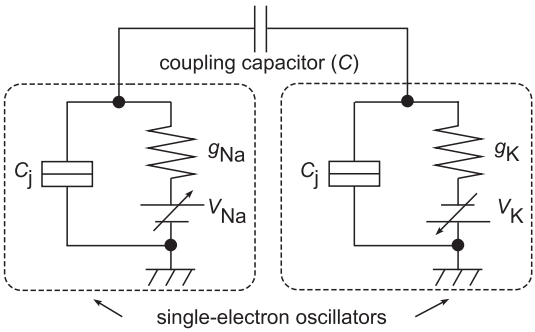

Fig. 7.14 Depressing synapse circuit with single-electron oscillator

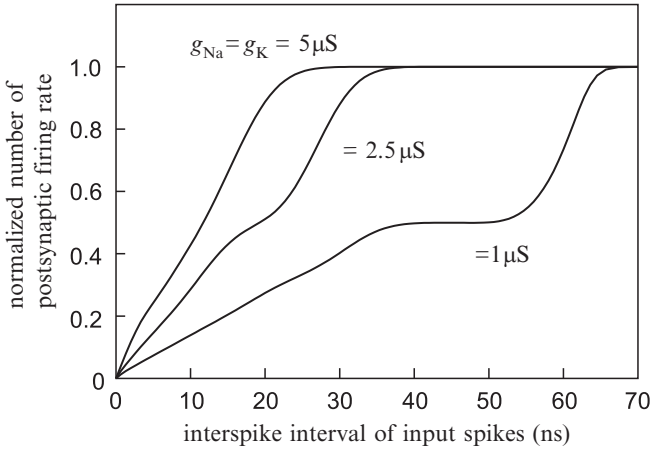

Fig. 7.15 Changes in postsynaptic firing rate of depressing synapse circuit against interspike interval of input spikes

by setting the appropriate threshold V_{th} corresponding to the number of active neurons. On the other hand, the EPSP also increases in proportion to the firing rate of spiking neurons. Therefore, the performance needed to discriminate the number of pre-synaptic active neurons largely deteriorates if the firing rate is not a constant value. During a burst input, the output current of the depressing synapse circuit that flows via a conductance (g') rapidly decreases for successive spikes due to the refractory properties of the single-electron oscillator. But during a nonbursting period, the oscillator has time to be in a resting period, and these results in a strong EPSP at the onset of the next burst. If we compare this dynamic response with that for a nondepressed synapse evoking the same EPSP on average, the depressed synapse will have a larger response at the burst onset and a smaller response toward the end of the burst.

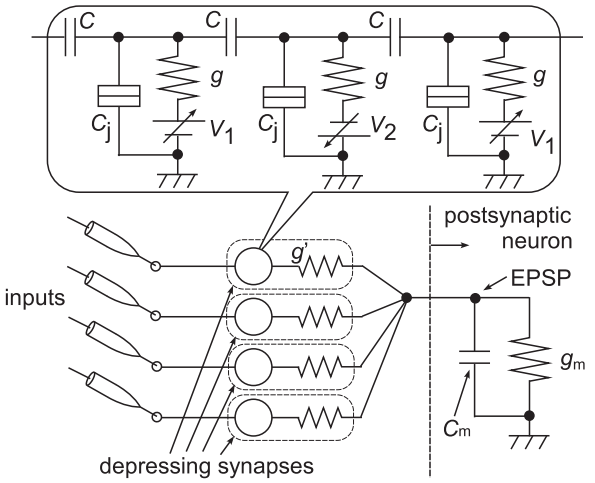

Fig. 7.16 Circuit configuration of depressing synapses with postsynaptic neuron circuit

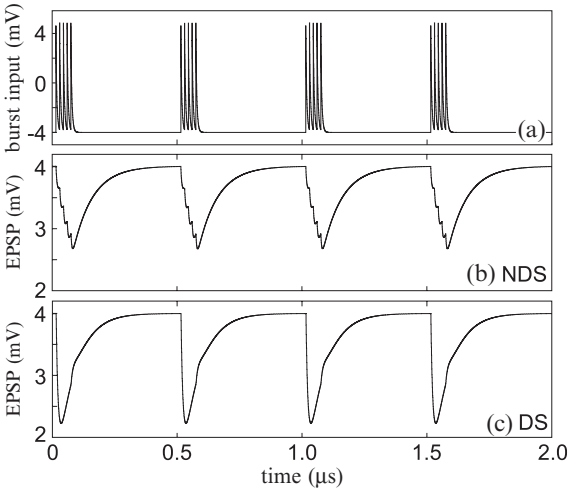

Fig. 7.17 Responses of EPSP for single burst input (**a**) via nondepressed (**b**) and depressed synapse circuit (**c**)

Figure 7.17 shows the response of the EPSP with bursting inputs for (a) a non-depressed synapse (b) and a depressed synapse circuit (c). The results ensure that the EPSP caused by the depressed synapse circuit has a larger response at the burst onset, as compared with a nondepressed synapse circuit.

Let us see that the depressing synapse circuit can detect the synchrony in the burst times. We used two bursting neurons as the input of the post-synaptic neuron that receives the burst inputs through depressed or nondepressed synapses.

Figures 7.18 and 7.19 show the results. When the input bursts were not synchronized (Fig. 7.6a, b), the peak EPSPs evoked by nondepressed [Fig. 7.18c] and depressed synapses (Fig. 7.18d) were both around 3 mV. But, when the input bursts were synchronized (Fig. 7.19a, b), the peak EPSPs evoked by depressed synapses (Fig. 7.19d) were significantly larger than the nondepressed synapses (Fig. 7.19c). Therefore, after defining an appropriate threshold V_{th} of the post-synaptic neuron, for example, $V_{\mathrm{th}} = 1.5\,\mathrm{mV}$ in the experiments, the post-synaptic neuron with the depressing synapse circuit can fire when the burst inputs are synchronized.

Figure 7.20a shows a simulated result of 100 neurons driven by random spike trains. According to Senn's report [26], there is experimental evidence to assume that before and during the tone, auditory cortical neurons fire in short bursts, with bursts of three to four spikes at 40–50 ms, repeated every 200–250 ms. During the tone, the burst onsets are assumed to be synchronized within the groups of 70 neurons that are randomly assembled anew for each burst. In our simulations, the overall firing rate of the population remains constant, apart from the short onset and offset of the tone when most cells burst together. This is because the bursting times of the groups alternate during the on-going tone (see Fig. 7.20b).

The neurons respond at the onset and offset by applying a tone stimulus (1.5–4.0 μs in Fig. 7.20). They correlate their bursts only between randomly assembled subgroups during the stimulus. Because the mean firing rate is on the background level during the tone (Fig. 7.20b), a post-synaptic neuron gathering the input spike trains through nondepressed synapses responds only at the stimulus onset and offset. With a depressing synapse, however, the post-synaptic neuron detects the correlated bursts, and then it fires as well (Fig. 7.20c), as shown in Senn's original work.

The difference in EPSP between burst and nonburst inputs represents the network's signal-to-noise (SN) ratio when the task is to discriminate burst spikes from nonburst ones. The results in Fig. 7.20c showed that it was around 1 mV. Note that the parameters of depressing synapse circuits were not optimized well. So what is the most important parameter to increase the difference? Apparently, it is the time constant of the depression because it determines the maximum EPSP, as shown in Fig. 7.19d. The constant is proportional to the junction capacitance and the channel conductance. The other important parameter is the ISI of the input bursting spikes. In the aforementioned simulations, the authors used typical bursting inputs that can easily be generated by external spike generators.

To consider the noise tolerance, we examine Monte-Carlo simulations for the network circuit with typical parameter sets. What we want here is to examine the quantitative difference between the original model [4] and the proposed single-electron circuit to optimize the performance. As described, the performance of the discrimination strongly depends on the SN ratio between the burst and the nonburst spike inputs. Increasing temperature results in an increase in the averaged EPSP. Our interest here is whether the SN ratio is constant or not for increasing the temperature. Of course, we need to recalculate an appropriate threshold for the discrimination. The following shows that the performance is definitely increased by increasing the temperature; however, all of the parameter sets are not optimized.

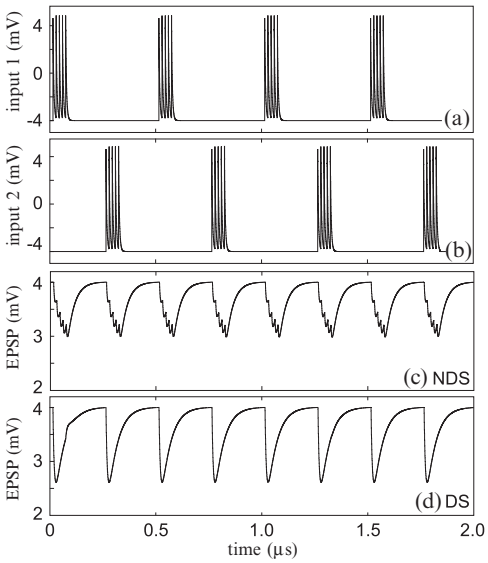

Fig. 7.18 Responses of EPSP for asynchronous burst input [(**a**) and (**b**)] via nondepressed (**c**) and depressed synapse circuit (**d**)

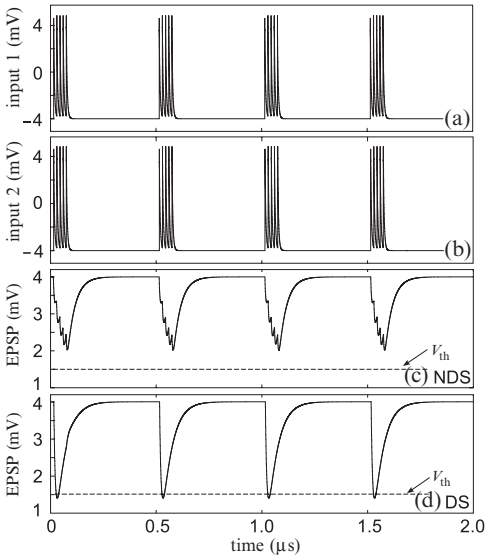

Fig. 7.19 Responses of EPSP for synchronous burst input [(**a**) and (**b**)] via nondepressed (**c**) and depressed synapse circuit (**d**)

To investigate the noise tolerance of Senn's network with our circuits, the 100-neuron network was simulated. To evaluate the noise tolerance, we calculate the difference between the averaged EPSP for the bursting and nonbursting periods and

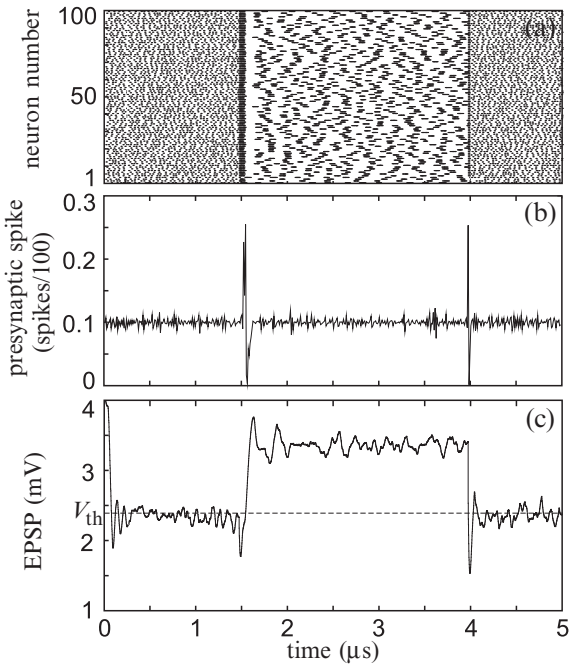

Fig. 7.20 Simulation results of 100-neuron network simulated by random spike trains through our depressing synapses

the threshold V_{th} that was defined as 2.4 mV in Fig. 7.20c as shown in Fig. 7.21. Ideally, the post-synaptic neuron must not fire during the nonbursting period but rather during the bursting period for the task of synchrony detection. The difference between the numbers thus represents the performance of this task. The difference between the averaged EPSP and V_{th} increased as the temperature increased during the nonbursting period. On the other hand, when $T > 0.5$ K, the difference started increasing. Namely, the performance of the synchrony detection did not change significantly due to an increase in T as long as $T < 0.5$ K. Remarkably, the difference (approximately performance of synchrony detection) changed nonmonotonically as T increased, as shown in Fig. 7.22.

The post-synaptic neuron circuit does not yet have any firing mechanism, because the circuit is a feed-forward neural network and because the important value for discriminating the burst spikes from the nonburst spikes is whether the EPSP is lower than the threshold or not. However, for the visualization alone, a significant difference is evident between the original model [4] and our circuit in Fig. 7.20c, where the EPSP is oppositely represented due to the lack of firing (discharging the membrane capacitance). The results shown in Fig. 7.22 indicated that the performance increased up to 0.5 K in the simulations when the temperature was increased. In our previous work [24], the maximum temperature for desired competitive operation was 0.1 K. Needless to say, the temperature is not enough to operate at room temperature. However, the phenomena where the performance increases monotonically

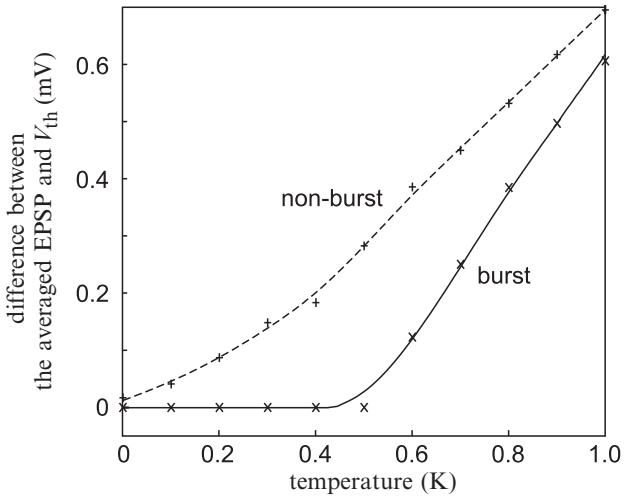

Fig. 7.21 Changes in the difference between the averaged EPSP and the threshold V_{th} during bursting and nonbursting period as a function of temperature

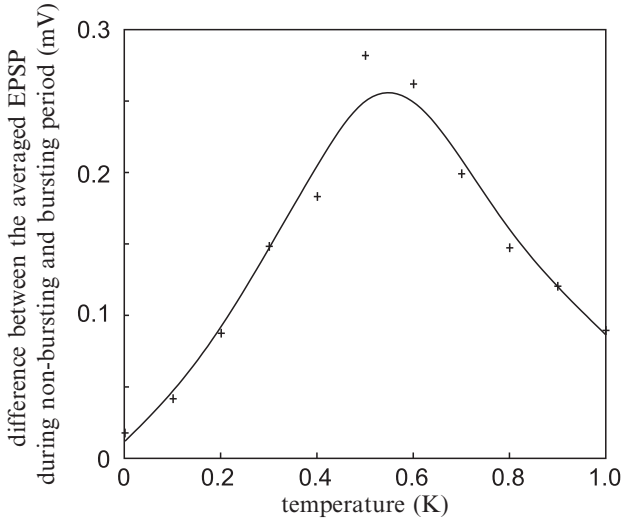

Fig. 7.22 Changes in the difference between the averaged EPSP during bursting and nonbursting period as a function of temperature

as the temperature increases have different physical meanings for conventional stochastic resonance. We are currently optimizing the device and environmental parameters to make the phenomena clear and to optimize these parameters.

7.4 Stochastic Resonance Among Single-Electron Neurons on Schottky Wrap-Gate Devices

Neuromorphic computing based on single-electron circuit technology has become widely noticed because of the recent claim about its massively increased computational efficiency and its increasing relevance between computer technology and nanotechnology. Its impact will be strongly felt when single-electron circuits based on a fault- and noise-tolerant neural structure are able to operate in a room-temperature environment. To fabricate such robust single-electron devices, the authors investigated stochastic resonance (cf. [8]) in an ensemble of single-electron boxes (SEB) [21]. We employed a single-electron transistor (SET) on a schottky wrap-gate (WPG) device [13], instead of a SEB, as a neuron, and examined statistical results of the network by numerical simulation.

The reason why we employ WPG-SETs instead of SEBs is that SETs have a switching characteristic as CMOS transistors do. A general SET consists of a capacitor (C) for an input terminal and two tunneling junctions (C_js) as shown in Fig. 7.23. A SET has three terminals, and one can connect controllable voltage sources to the terminals. Now let us connect terminals with bias V_d, input V_g, and ground, respectively, and control the switching characteristic by controlling the voltage sources. When the SET is in operation, an electron can tunnel through two C_js (between ground and a node, or between a node and V_d) in a low-temperature environment, because electron tunneling is governed by the physical phenomenon called the Coulomb blockade effect. In addition, one can easily observe the operations of practical SET devices. However, we must also be careful when we use single-electron circuits in a high-temperature environment. The reason is that the electrons randomly tunnel through C_js because the Coulomb blockade effect is disturbed by thermal fluctuations.

Let us consider SR among N SETs in a network, as shown in Fig. 7.23. When SETs are not connected with each other, electron tunneling in each SET's junction occurs independently. As in [8], we apply a common input to all the SETs and calculate the sum of outputs of the SETs. For simplicity, we apply a common input

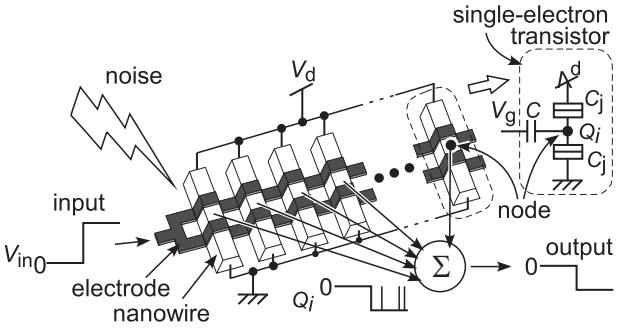

Fig. 7.23 Schematic image of SET array

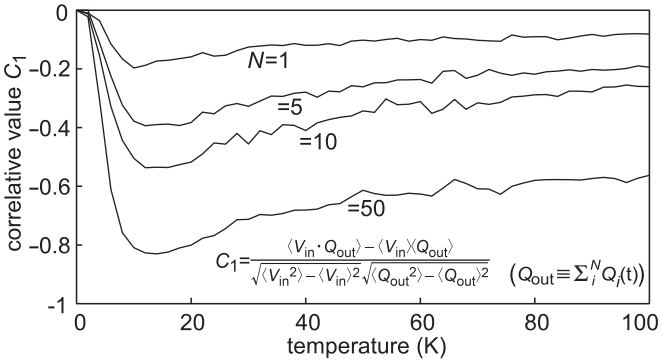

Fig. 7.24 Stochastic resonance in ensemble of single-electron transistors

voltage V_{in} to all the SETs as V_g, and do not consider practical circuits that calculate the sum of the changes in each node's electric charge Q_i. The ith SET's charge (Q_i) was increased with the input voltage, while the magnitude of the input was set to a very low value so that no electron would tunnel through C_js. Under this condition, increasing the magnitude of thermal noise (temperature) enables electrons to tunnel through each C_j.

Figure 7.24 shows simulation results of an ensemble of SETs for $N = 1$, 5, 10, and 50. The temperature was increased from 0 to 100 K and correlation values (C_1) between the input voltages and the summed output were calculated. The results showed characteristic signatures of SR-type behavior: a rapid rise to a peak, and then a decrease at high temperatures. One could observe that the magnitude of $|C_1|$ increased as N increased, as expected. The resonant temperatures were approximately 10 K for all the values of N. In addition, C_1 took a large value -0.6 at 100 K when $N = 50$, and increased as N increased. According to [8], the correlation value should become almost 1.0 when $N = 1{,}000$. The results indicate that when one employs such an SR network in single-electron circuits, it certainly acts as a transmission line that can cancel noises on the line, as well as, cancel the devices' intrinsic noises.

7.5 Single-electron Circuits Performing Dendritic Pattern Formation with Nature-inspired Cellular Automata

Ordered complex patterns can easily be observed everywhere in the natural world. Among these, bifurcated and branched patterns formed in open systems often serve as a basis for advanced functional structures. Indeed, these structures are essential for performing particular computational tasks in nature, for example, structures of a neuron's dendritic tree are responsible for various intelligent computing tasks. Recent advances in neuroscience have revealed that fundamental roles of these dendritic trees include not only the transmission of neuronal signals but also functional

computation utilizing multiple properties of membranes and spines (early works can be found in [6, 15]). To incorporate the functions performed by dendritic trees into neuromorphic hardware, the authors and several colleagues developed a single-electron circuit that self-organizes spatial dendritic patterns on a multilayer nanodot array. As the first step, let us see a cellular automaton (CA) model based on a behavioral model of bacteria colonies [17].

It is difficult to implement a huge amount of physical wiring, that is, axons and dendrites, on a 2D semiconductor chip because the wiring is fabricated by stacking several layers of only wiring. Again we here use single-electron circuits, which are believed to have potential for next-generation VLSIs, to increase the wiring density. We also actively incorporate quantum effects and sensitivity to thermal noise into the design of compact unit circuits for the proposed CA.

One of the features of neurons is the complexity of their forms, such as tree-like, branching dendritic form. The details of dendritic pattern formation in neural systems have been mainly studied from the viewpoint of molecular biology, rather than that of general physics. This kind of branching pattern is also observed in many other systems, including trees, crystal growth, protoplasmic streaming tubes of slime molds, bacterial colonies, etc. Because of generality of these kinds of patterns, several models have been proposed to describe complex branching patterns [7, 16, 32]. One of the best-known simple models is the diffusion limited aggregation (DLA) model [32]. Another well-known type of model is the RD model for the pattern formation of bacterial colonies, which exhibit more diverse patterns than the DLA model [16]. Two methods are used to describe RD systems; one is based on partial differential equations (PDE) [31] and the other on discretized CA [9]. Space, time, and state variables are generally discrete in the CA model, whereas they are continuous in the PDE representation of the RD system. Here we employ CA representation of RD dynamics based on bacterial colony pattern formation to represent dendritic patterns because of the variety of patterns available and its expansion for device applications.

The skeleton of the RD pattern formation model of a bacterial colony consists of movement/schism of bacteria, diffusion of nutrients, and consumption of nutrients by the bacteria. In the model, the dynamics are described as "reaction," the

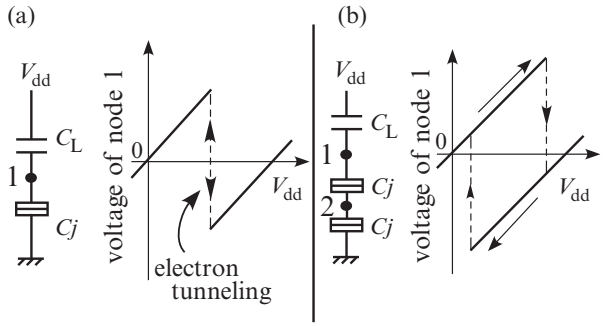

Fig. 7.25 Single-electron devices. (**a**) single-electron box, and (**b**) single-electron memory circuit

relationship of the bacteria and the nutrient, and "diffusion," which averages the bacteria or nutrient in the neighborhood. In CA models, the targeted space is divided into discrete areas of named cells. The time evolution of the state of each cell is decided by simple inner- and inter-cell rules, and a dynamic pattern or whole structure is generated from these local interaction rules. The algorithm of our CA model is as follows. Three variables are used to describe the state of the system in each cell; active bacteria (activator) a, inactive bacteria (inactivator, a trace of activator) w, and nutrient (substrate) f. The variables a and w take the digit value $\{0,1\}$, and f takes a digit or multivalue. When there are both a sufficient number of activators in the cell's neighborhood and sufficient substrate in the cell, the state of the activators becomes 1 $(a : 0 \rightarrow 1)$, and substrate f is depleted in the next step. After $(a \rightarrow 1)$, when the substrate in the cell itself is less than the threshold value as a result of depletion, the activator can no longer sustain an active state; the state of the activators becomes 0 $(a \rightarrow 0)$, and the state of the inactivator becomes 1 $(w \rightarrow 1)$. The substrate diffuses constantly with fluctuation. When there is insufficient substrate, the activators try to take up the limited substrate. As a result, the cluster of activators divides into several clusters, and a branching pattern appears as the cluster of cells, where inactivator $w = 1$.

To imitate the diffusion of the consumed substance with fluctuation in the model, we use an SE-RD device [23], SEBs, and SEM circuits [22] to implement the CA rules. A typical single-electron circuit consists of tunneling junctions, resistances, and capacitors. A tunneling junction that is similar to a capacitor is the main component of a single-electron circuit. In a junction, a quantum effect occurs. A point of difference between tunneling junctions and normal capacitors is that the two conductors of the junction face each other very closely. The junction has a threshold voltage value for the generation of a quantum effect that is electron tunneling. A single-electron passes through the junction when the junction potential is over the threshold voltage, and the potential of the junction changes suddenly. The tunneling event has a probability of occurring, given by

$$P(E) \sim \frac{1}{1 - \exp[-\Delta E/(k_{\mathrm{B}}T)]} \tag{7.1}$$

where P is the tunneling probability, E is the charging energy, k_{B} is the Boltzmann constant, and T is the temperature. The equation has a temperature factor. Therefore, the tunneling probability changes with the temperature. We would like to utilize this physical phenomenon to implement fluctuation in the diffusional operation of the CA model. The circuit configuration and example operations of an SE-RD device have already been shown in Figs. 7.1 and 7.2, respectively.

We use SEBs to change the input signals to binary signals. The left of Fig. 7.25a shows the circuit configuration of an SEB. It consists of a tunneling junction, bias capacitor, and bias voltage source. The right of Fig. 7.25a shows a sample operation. The SEB shows a positive voltage (logical 1) when no electron tunneling occurs, and a negative one (logical 0) when electron tunneling occurs. We also use SEMs as memory devices because they have a hysteretic function as a function of the input voltage. The left of Fig. 7.25b shows the circuit configuration of an SEM. It consists of two tunneling junctions, a bias capacitor, and a bias voltage source in series. The

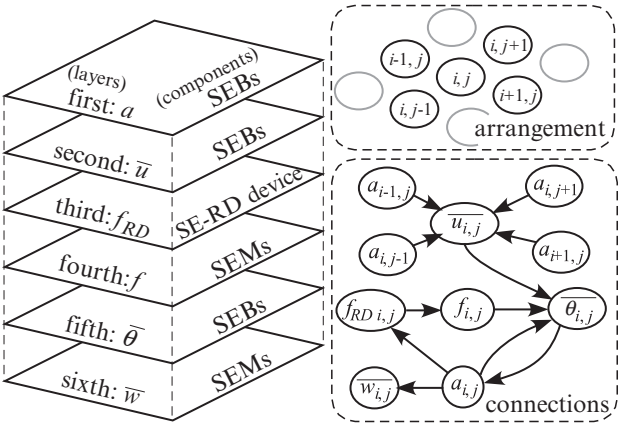

Fig. 7.26 Single-electron device for generation of dendritic patterns

right of Fig. 7.25b shows a sample operation [22]. The SEBs and SEMs play the role of active and inactive bacteria, respectively.

We design a new single-electron device based on the CA model, the SE-RD device, the SEBs, and the SEMs. The device consists of six layers (Fig. 7.26). We add two factors "$u_{i,j}$" and "$\theta_{i,j}$" to the device as supplementary functions. The first layer consists of arrayed SEBs that implements the "$a_{i,j}$" of the model. The second also consists of arrayed SEBs that implement the added factor "$u_{i,j}$." The third is the SE-RD device, and the fourth consists of arrayed SEMs. The third layer implements "$f_{i,j}$" in collaboration with the fourth layer. In this device, f takes a digit value. The fifth layer consists of arrayed SEBs that implement the added factor "$\theta_{i,j}$," and the sixth consists of arrayed SEMs that implement the "$w_{i,j}$" of the model. The unit circuits of each layer are assumed to be cells of the CA. The operations of each factor are represented by the following equations:

$$a_{i,j} = \begin{cases} 1 \text{ (if } \theta_{i,j} = 1), \\ 0 \text{ (otherwise)}, \end{cases} \tag{7.2}$$

$$u_{i,j} = \begin{cases} 1 \text{ (if } a_{i-1,j} + a_{i+1,j} + a_{i,j-1} + a_{i,j+1} = 1), \\ 0 \text{ (otherwise)}, \end{cases} \tag{7.3}$$

$$f_{\mathrm{RD}\ i,j} = \begin{cases} \mathrm{TN} \text{ (if } a_{i,j} = 1 \text{ or neighbor } f_{\mathrm{RD}} = \mathrm{TN}), \\ \mathrm{NT} \text{ (otherwise)}, \end{cases} \tag{7.4}$$

$$f_{i,j} = \begin{cases} 0 \text{ (if } f_{\mathrm{RD}\ i,j} = \mathrm{NT} \text{ or } f_{i,j} = 0), \\ 1 \text{ (otherwise)}, \end{cases} \tag{7.5}$$

$$\theta_{i,j} = \begin{cases} 1 \text{ (if } \overline{a_{i,j}} \cdot u_{i,j} \cdot f_{i,j} = 1), \\ 0 \text{ (otherwise)}, \end{cases} \tag{7.6}$$

$$w_{i,j} = \begin{cases} 1 \text{ (if } a_{i,j} + w_{i,j} = 1), \\ 0 \text{ (otherwise)}, \end{cases} \tag{7.7}$$

where "TN" and "NT" represent "tunneling" and "no tunneling," respectively.

In the simulation, the device had 200×200 elements in each layer. Figure 7.27 shows sample operations of the elements in each layer. In Fig. 7.27a, $a_{i,j}$ maintained a logical 0 state (negative voltage) until $\theta_{i,j}$ changed its 0 state to 1 (positive voltage). $u_{i,j}$ kept 0 state until neighbor a changed its 0 state to 1. $f_{i,j}$ ($f_{RD\ i,j}$) maintained 1 state until $a_{i,j}$ changed its 0 state to 1 or electron tunneling occurred in the neighboring f_{RD} and kept 0 state after it changed its state from 1 to 0. $w_{i,j}$ kept 1 state until $a_{i,j}$ changed its 0 state to 1 and kept 0 state after it changed its state from 1 to 0. Thus, the device implemented the CA model. However, operating errors sometimes occurred because of the tunneling probability in the device. Figure 7.27b shows sample operations. In the figure, p and q represent different points from i and j. Neighbors a, $u_{p,q}$, and $f_{p,q}$ operated well as did a, u, and f in Fig. 7.27a. $\theta_{p,q}$, however, showed a failed operation because of the tunneling probability. As a result, $a_{p,q}$ and $w_{p,q}$ could not change their state. This failed operation works as the diffusion of the consumed nutrient with fluctuation in the model. Figure 7.28 shows the results of a two-dimensional simulation. In the simulation, a spatio-temporal pattern was formed on the sixth (w) layer. The pattern grew from a planar point, but some parts of the growing points stopped because of both the correct and failed operations in each layer. As a result, a dendritic pattern appeared. This dendritic pattern will change with every simulation because of the tunneling probability.

7.6 Summary and Future Works

This chapter introduced four nature- or bio-inspired single-electron circuits for nonclassical computation, that is, computation of a Voronoi diagram (VD), burst or nonburst spike detection, weak signal transmission based on stochastic resonance (SR) under noisy environment, and dendritic pattern generation based on an artificial model of bacteria colonies.

First, a SE-RD devices for computing a VD was introduced. The novel SE-RD device consists of three layers. The top layer is an improved SE-RD device in which nonlinear voltage waves are generated and travel, and the middle and bottom layer are threshold detectors. The operations of the middle and bottom layer are based on the CA model [1, 2]. The bottom layer outputs the results of computing a VD by using data from the top and middle layers.

Second, a single-electron depressing synapse and its characteristics was introduced for considering possible applications on noise-tolerant synchrony detection. Previous works on CMOS VLSI showed that the network had great noise-tolerant ability for static noise embedded as device (threshold) mismatches of MOSFETs [4]. We expanded this notion to dynamic ones that are usually a common problem in the area of single-electron circuits. The results showed that the performance is greatly increased by increasing the temperature until $T \leq 0.5\,\mathrm{K}$ [25]. However, all the parameter sets are not optimized. The performance is apparently sensitive to the time constant of a single-electron oscillator and interspike intervals of input burst spikes. Our next goal is an appropriate theory for the emergence of the noise tolerance and

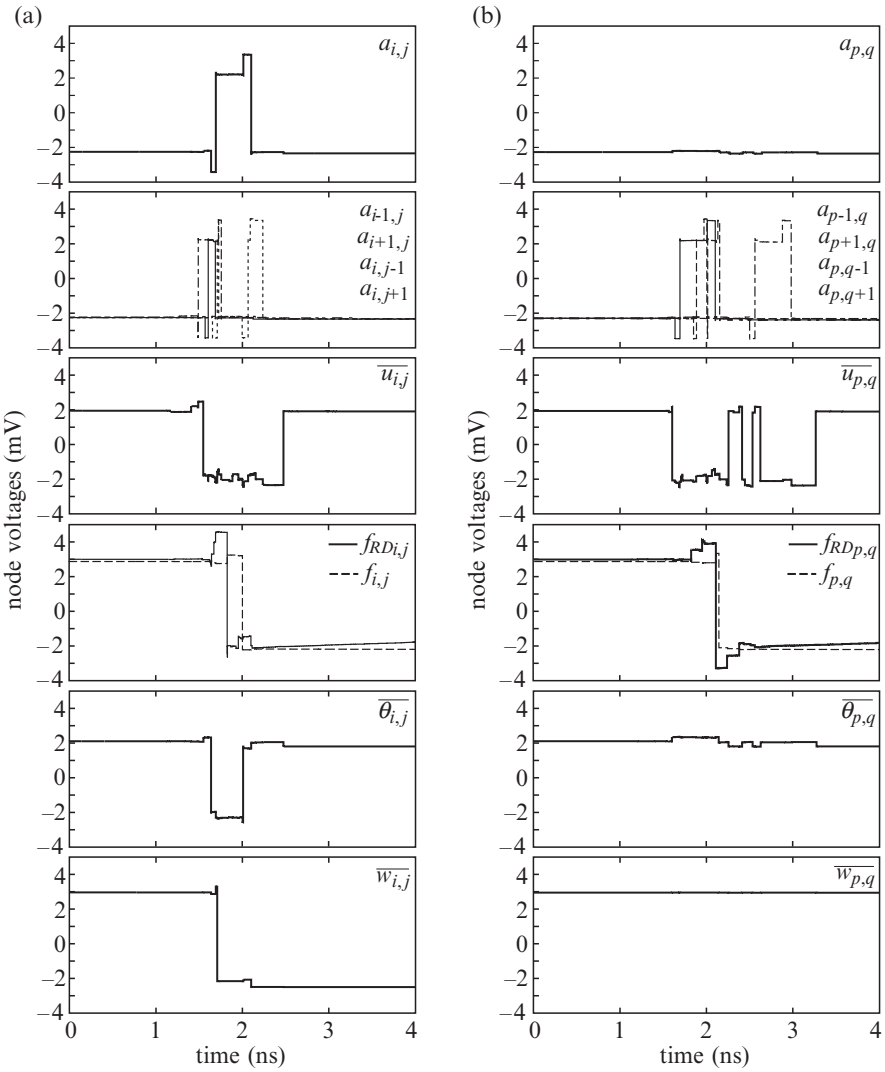

Fig. 7.27 Simulation results. (**a**) correct operations, (**b**) failed operations

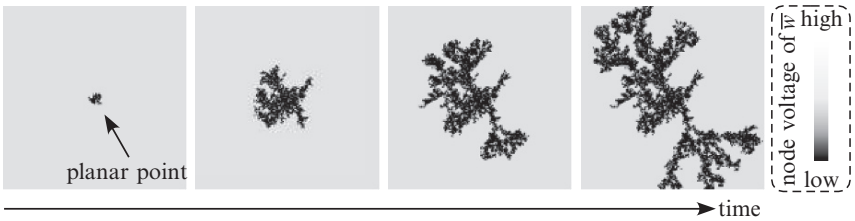

Fig. 7.28 Result of two-dimensional simulation of sixth layer

optimization of these parameters to explore the possible development of fault and noise-tolerant single electron computing devices.

Third, SR in an ensemble of single-electron neuromorphic devices was introduced. Recently, the authors and several colleagues have proposed a single-electron competitive neural network based on SR in an ensemble of single-electron boxes that can operate at room temperature [21]. Using realistic physical parameters, we confirmed the SR behavior of single-electron boxes. The resonant temperature was 20 K, independent of the number of boxes (N).

Finally, novel single-electron circuits for forming dendritic patterns were introduced. To construct the proposed device, we designed a six-layer single-electron circuit with nature-inspired cellular automata. The utilized cellular automaton had three factors. In the device, the top, second, and fifth layers consist of arrayed single-electron boxes, the fourth and sixth layers consist of arrayed single-electron memory circuits, and the third layer is an SE-RD device. Each layer described each factor of the CA rule with randomness. As a result, the device formed dendritic patterns in the sixth layer. These patterns will change with variations in the circuit parameters or temperature environment.

Recent progress in nanotechnology has certainly accelerated by advances in nanoscale processing, for example, elemental logic gates and memory cells for single-electron LSIs have been proposed in the literature, and significant reports of their fabrication have appeared. However, many problems concerning both static and dynamic "noises" still exist for practical use of single-electron circuits. Future works in this field is thus to find a clever way to cancel (or exploit if possible) the effects of thermal fluctuations in terms of circuit architecture, instead of improving nanoscale device fabrication technologies. Recently, neuromorphic computing based on single-electron circuits is gaining prominence because of its massively increased computational efficiency and the increasing relevance of computer technology and nanotechnology. The maximum impact of these technologies will be strongly felt when single-electron circuits based on fault- and noise-tolerant neural structures can operate at room temperature.

References

1. Adamatzky, A.: Reaction–diffusion algorithm for constructing discrete generalized voronoi diagram. Neural Networks World **6**, 635–643 (1994)
2. Adamatzky, A.: Voronoi-like partition of lattice in cellular automata. Math. Comput. Modelling 51–66 (1996)
3. Adamatzky, A., De-Lacy-Costello, B., Asai, T.: Reaction Diffusion Computers. Elsevier, Amsterdam (2005)
4. Asai, T., Kanazawa, Y., Hirose, T., Amemiya, Y.: A mos circuit for depressing synapse and its application to contrast-invariant pattern classification and synchrony detection. In: Proc. 2004 Int. Joint Conf. Neural Networksn, p. W107 (2004)
5. Benioff, P.: Quantum mechanical models of turing machines that dissipate no energy. Phys. Rev. Lett. **48**(23), 1581–1585 (1982)
6. Blackwell, K.T., Vogl, T.P., Alkon, D.L.: Pattern matching in a model of dendritic spines. Network Comput. Neural Syst. **9**(1), 107–121 (1998)

7. Carmeliet, P., Tessier-Lavigne, M.: Common mechanisms of nerve and blood vessel wiring. Nature **436**(7048), 193–200 (2005)
8. Collins, J.J., Chow, C.C., Imhoff, T.T.: Stochastic resonance without tuning. Nature **376**(6537), 236–238 (1995)
9. Gerhardt, M., Schuster, H., Tyson, J.J.: Cellular automaton model of excitable media II: Curvature, dispersion, rotating waves and meandering waves. Physica D **46**(3), 392–415 (1990)
10. Gershenfeld, N.A.: Bulk spin-resonance quantum computation. Science **275**(17), 350–356 (1997)
11. Gravert, H., Devoret, M.H.: Single Charge Tunneling – Coulomb Blockade Phenomena in Nanostructures. Plenum, New York (1992)
12. Kanazawa, Y., Asai, T., Ikebe, M., Amemiya, Y.: A novel cmos circuit for depressing synapse and its application to contrast-invariant pattern classification and synchrony detection. Int. J. Robotics Automation **19**(4), 206–212 (2004)
13. Kasai, S., Jinushi, K., Tomozawa, H., Hasegawa, H.: Fabrication and characterization of gaas single electron devices having single and multiple dots based on schottky in-plane-gate and wrap-gate control of two-dimensional electron gas. Jpn. J. Appl. Phys. **36**(3B), 1678–1685 (1997)
14. Klein, R.: Concrete and Abstract Voronoi Diagrams. Springer, Berlin (1990)
15. Mel, B.W.: Nmda-based pattern discrimination in a modeled cortical neuron. Neural Comput. **4**(4), 502–516 (1992)
16. Mimura, M., Sakaguchi, H., Matsushita, M.: Reaction–diffusion modelling of bacterial colony patterns. Physica A **282**(1–2), 283–303 (2000)
17. Motoike, I.N.: Simple modeling of branching pattern formation in a reaction diffusion system with cellular automaton. J. Phys. Soc. Jpn **76**(3), 034,002 (2007)
18. Okabe, A., Boots, B., Sugihara, K., Chiu, S.N.: Spatial Tesselations: Concepts and Applications of Voronoi diagrams. Wiley, Chichester (2000)
19. Oya, T., Asai, T., Amemiya, Y.: Single-electrron logic device with simple structure. Elec. Lett. **39**(13), 965–967 (2003)
20. Oya, T., Asai, T., Amemiya, Y.: A single-electron reaction-diffusion device for computation of a voronoi diagram. Int. J. Unconventional Comput. **3**(4), 271–284 (2007)
21. Oya, T., Asai, T., Amemiya, Y.: Stochastic resonance in an ensemble of single-electron neuromorphic devices and its application to competitive neural networks. Chaos, Solitons and Fractals **32**(2), 855–861 (2007)
22. Oya, T., Asai, T., Fukui, T., Amemiya, Y.: A majority-logic device using an irreversible single-electron box. IEEE Trans. Nanotech. **2**(1), 15–22 (2003)
23. Oya, T., Asai, T., Fukui, T., Amemiya, Y.: Reaction-diffusion systems consisting of single-electron circuits. Int. J. Unconventional Comput. **1**(2), 177–194 (2005)
24. Oya, T., Asai, T., Kagaya, R., Hirose, T., Amemiya, Y.: Neuromorphic single-electron circuit and its application to temporal-domain neural competition. In: 2004 Int. Symp. Nonlinear Theory and its Application, pp. 235–239 (2004)
25. Oya, T., Asai, T., Kagaya, R., Hirose, T., Amemiya, Y.: Neuronal synchrony detection on signle-electron neural network. Chaos, Solitons and Fractals **27**(4), 887–894 (2006)
26. Senn, W., Segev, I., Tsodyks, M.: Reading neuronal synchrony with depressing synapses. Neural Comput. **10**(4), 815–819 (1998)
27. Shor, P.W.: Scheme for reducing decoherence in quantum computer memory. Phys. Rev. A **52**(4), 2493–2496 (1995)
28. Suzuki, Y., Takayama, T., Motoike, I.N., Asai, T.: Striped and spotted pattern generation on reaction-diffusion cellular automata – Theory and lsi implementation. Int. J. Unconventional Comput. **3**(1), 1–13 (2007)
29. Takahashi, Y., Nagase, M., Namatsu, H., Kurihara, K., Iwadate, K., Nakajima, K., Horiguchi, S., Murase, K., Tabe, M.: Fabrication technique for si single-electron transistor operating at room-temperature. Elec. Lett. **31**(2), 136–137 (1995)
30. Tucker, J.R.: Complementary digital logic based on the coulomb blockade. J. Appl. Phys. **72**(9), 4399–4413 (1992)

31. Turing, A.M.: The chemical basis of morphogenesis. Phil. Trans. R. Soc. Lond. **237**(641), 37–72 (1952)
32. Witten, T.A., Sander, L.M.: Diffusion-limited aggregation, a kinetic critical phenomenon. Phys. Rev. Lett. **47**(19), 1400–1403 (1981)