Chapter 5
Emerging Oxide Resistance Change Memories

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The state of the art in resistance-based memory technology is presented. Recently memory technology has been focused on convergence towards ubiquitous memories which are non-volatile, have random access, and have fast programming times. This chapter is focused on electrically induced resistive change memories (including the resistive switching materials and mechanism) and other applications. Resistive random access memory (RRAM) has the simplest structure of new memory technologies, in fact the resistance change phenomenon can be observed in a metal–insulator–metal structure. Also, the switching speed has been reported to be about 10 ns and the resistance change effect scales down to cell sizes of 10×10 nm^2 [1, 2]. First, we review classification of resistance memory and materials: unipolar, bipolar, ionic, and electronic effect memory. The second section deals with structure of cell stack architecture, which is a very important merit of resistance memories in particular, RRAM cell scaling and RRAM integration. In the final section the superior intrinsic scaling characteristics of RRAM compared to charge-based devices, and multilevel cell (MLC) RRAM, are discussed. Finally, we conclude with some comments on the outlook, future works, and research necessary for realization of RRAM technology.

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5.1 Introduction

5.1.1 Overview of Oxide Resistance Change Memory

Oxide resistance change phenomenon was first discovered in the 1960s by Hickmott [3]. In the following three decades several other workers contributed towards what we today classify as RRAM [4–10]. In the early stages resistance change memories were distinguished by their current–voltage characteristics as either voltage controlled negative resistance (VCNR) or current-controlled negative resistance (CCNR) [11, 12]. Although the potential of resistance-based memories was apparent from an early stage, actual integration and fine-tuning of materials properties was a barrier difficult to overcome.

Renewed interest in RRAM occurred towards early 2000 when universal memories were becoming the goal of research. Several candidates which could potentially be as fast as dynamic RAM (DRAM), while being non-volatile began to emerge. Several of these candidates such as phase change RAM (PRAM), magnetic RAM (MRAM), and ferroelectric RAM (FRAM) have been mentioned in other chapters of this book and elsewhere [13–15]. Of these new memories, RRAM had several advantages such as simple composition and low temperature process, a simple metal–insulator–metal (MIM) structure, in addition to being completely complementary metal–oxide–semiconductor (CMOS) process compatible [10, 16, 17]. Table 5.1 is the ITRS Roadmap comparison of new memories comparing fundamental memory metrics: resistance-based memory has superior Retention and Speed, while lacking endurance, and having high programming current [15, 16, 18–28].

NAND Flash memory density has increased so quickly (64 Gb MLC in 2008, Samsung) that it was impractical for new memories to compete directly. More recently RRAM research has become focused on advantages such as low temperature processes, stackable cell structures, and multilevel characteristics. The simple cell structure of RRAM allows for more complicated device structures to be fabricated using minimal additional processing. Figure 5.1 compares several memory candidates with current mass production NAND Flash memory, FRAM, and MRAM. RRAM demonstrates fast programming speeds with high density which can be achieved by stacking and MLC.

In the earliest stages of RRAM research in 2000, a major limitation was that the exact mechanism behind the resistance change was not clear. Although the previous works since the 1970s had investigated the phenomena [3, 11, 29], no satisfactory consensus regarding the mechanism had been reached. A major reason for the confusion and complications behind the mechanisms had to do with the variety of materials each having its own explanation. Today we are beginning to see more direct evidence of the mechanisms behind switching and making progress into the fundamental physics behind RRAM [2, 30–33].

In order to give the reader an overview into the current state of RRAM research, this chapter will begin with a comparison and classification of RRAM materials and types. Next a discussion about the mechanism behind resistance change phenomenon

Table 5.1 Comparison of resistance-based memory devices under development

	Phase change memory	Nanomechanical memory	Filament formation/ rupture memory	Ionic memory	Electronic effects memory	Molecular memory
Storage mechanism	Reversibly changing amorphous and crystalline phases	Electrostatically controlled mechanical switch	Multiple mechanisms	Ion transport and redox reaction	Charge trapping Mott transition Schottky barrier effects	Multiple mechanisms
Cell elements	1T1R[a] or 1D1R[b]	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1 D1R	1T1R or 1D1R	1T1R or 1D1R
W/E time	50/120 ns [15]	3 ns [19]	5 ns/10 ns [21]	<50 ns [22]	100 ns [23]	0.2 s [26]
Feature size F (best projected)	65 nm (production)	5–10 nm	5–10 nm	5–10 nm	5–10 nm	5–10 nm
Cell area (best projected)	$4.8F^2$	$8/5F^2$	$8/5F^2$	$8/5F^2$	$8/5F^2$	$8/5F^2$
Retention time	>10 year	~days [20]	>1 year	>10 year	>1 year [24]	2 months [28]
Write cycles	1E8	>1E6 [20]	>1E6 [16]	>1E6 [22]	>1E3 [25]	>2E3 [27]

[a]1T1R:1transistor 1resistor
[b]1D1R:1diode 1resistor

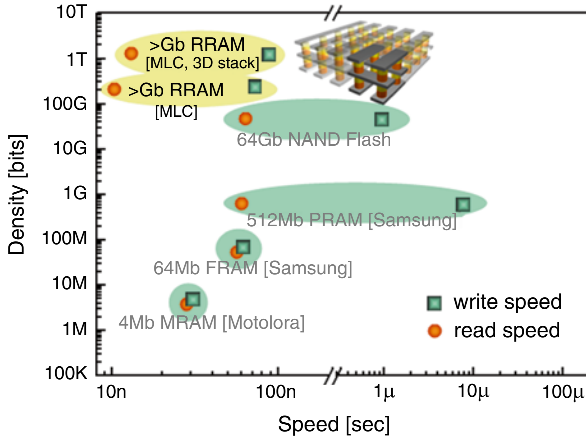


Fig. 5.1 Comparison of the cell operation speed versus memory density for NAND Flash, PRAM, FRAM, MRAM, and RRAM. Current RRAM materials show fast programming speeds on the order of 10 ns and have high density potential using MLC and 3D stack technology

will be presented. In the second section, we will discuss more current works regarding cell stacking architecture, and RRAM scaling. Finally we discuss the outlook for RRAM and offer our views into what further works are still required.

5.2 Resistance Change in Oxide-Based Materials

5.2.1 Resistance Switching Properties

Depending on the current–voltage characteristics we can divide resistance change phenomena into three broad categories: unipolar, bipolar (also called electronic effect), and threshold switching. Unipolar and bipolar switching types are nonvolatile in that even after removing the voltage the resistance values will remain at whichever state it is set to. In contrast threshold switching is volatile and requires a minimum voltage (V_{hold}) to maintain the low resistance state. Figure 5.2 shows a comparison of the current–voltage switching characteristics.

As seen in Fig. 5.2a unipolar switching is called such because the cell can be operated at either positive or negative bias exclusively. For example, the voltage (V_{set}) required to switch the cell to low resistance state (LRS) is positive just as the voltage (V_{reset}) required to return the cell to the high resistance state (HRS) is also positive. In addition the switching curve is completely symmetric in that any operation which can occur with positive bias can also occur at negative bias. Finally, the order of applied bias polarity does not matter: positive or negative bias can be used to set (HRS → LRS), and then a positive or negative bias can be used to reset (LRS → HRS).

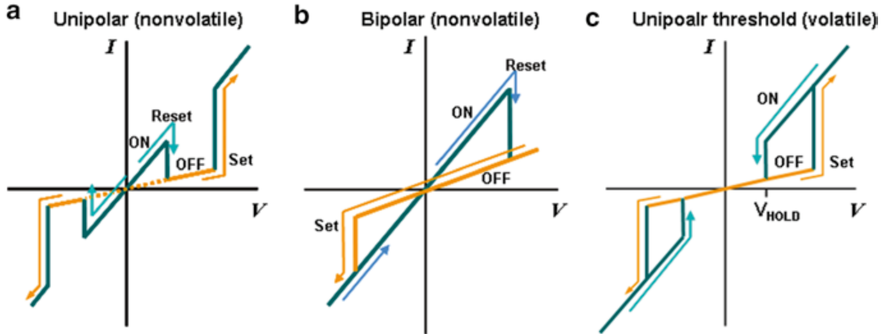


Fig. 5.2 (**a**) Typical unipolar memory switching. Switching curve is symmetric: set and reset operations are performed at the same polarity (**b**) Typical bipolar memory switching. Asymmetric switching: the set and reset operation takes place in one polarity: negative bias for set in this case (**c**) Threshold switching, hysteresis shows the value of the minimum voltage (V_{hold}) required to maintain the low resistance state

In contrast Fig. 5.2b shows the bipolar memory characteristic. In this example set occurs at negative bias while reset occurs at positive bias. In this case a voltage sweep (or pulse) of the same polarity as V_{set} will not reset the cell. Also even if the same type of electrode is used, for example Pt bottom and Pt top electrodes, set and reset operations can only be performed at their respective polarity. Finally Figure 5.2c shows threshold switching. Threshold switching occurs as unipolar and after reaching V_{set} the cell reaches the low resistance state. However upon lowering the voltage to below the minimum value of V_{hold}, the LRS is recovered.

The three of these types of switching can be used to describe the majority of oxide-based resistance change materials. It is interesting to note that different types of switching can occur even in the same material depending on factors such as: electroforming [11], doping concentration [34], stoichiometry [10], and physical parameters [16]. Although this broad range of properties might seem to decrease the value of oxide-based memories for memory applications, in fact the flexibility of switching properties allows for all-oxide-based devices and applications which have several advantages over devices which might require different materials for respective components such as memory cell and switch.

5.2.2 Oxide-Based Resistance Memory Classifications

5.2.2.1 Binary Oxides

Of oxide-based resistance change materials, the simplest class we can consider are the binary transition metal oxides (TMO). Examples of materials are: NiO [2], TiO_2 [35], ZnO [36], CuO [37], VO_2 [38], Ta_2O_5 [39], and HfO_2 [40]. The chemical composition

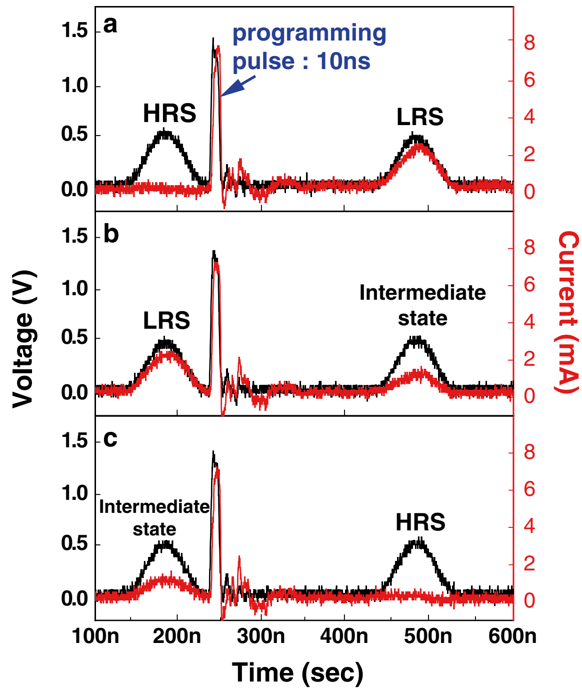


Fig. 5.3 Pulse experiments showing bistable resistance switching for 10 ns pulse width. (**a**) Switching from HRS to LRS, (**b**) switching from LRS to an intermediate state, and (**c**) switching from an intermediate state to HRS. Switching from HRS to LRS is induced by a single 1.5 V pulse with 10 ns duration while switching from LRS to HRS is caused by a series of two identical pulses with 10 ns separation time. Reprinted with permission from [1]. Copyright 2008, Wiley InterScience

is made of a transition metal and oxygen. The stoichiometry and doping concentration can easily be varied during fabrication and leads to the widest array of properties for any given material. For example, by varying oxygen partial pressure during NiO deposition, it has been reported that the resistivity can be varied [10]. Due to the simple composition almost any deposition method can be used to fabricate TMOs. Some methods which have been reported include: Sputter, atomic layer deposition (ALD) [41], metallorganic chemical vapor deposition (MOCVD) [42], anodization [3], sol-gel [43], and thermal oxidation [44]. TMO thin films are usually fabricated as polycrystalline thin films leading to isotropic and uniform properties over the film. Although the chemical composition is rather simple a variety of crystal structures occur for TMOs: rock-salt (NiO), rutile or anatase (TiO_2) [35], and even polycrystalline or amorphous structure (ZnO).

For resistance-change cells typically a metal–TMO–metal structure is used where the metals can be either the same or different. In the past, lateral structures have also been tested and shown to exhibit resistance switching. More recently lateral structures have been ignored in favor of vertical MIM structures which have more easily definable switching regions.

Figure 5.3 shows the impressive switching speeds in TMO based oxide memories. A Pt–NiO–Pt structure was fabricated and a pulse generator was used to test

the minimum switching speed [1]. The switching speed was shown to be possible for pulse durations of 10 ns. The programmed state was confirmed by a read pulse of 0.3 V before and after application of respective set/reset pulses.

All three types of switching discussed in Sect. 5.2.1 occur in TMOs. A complete discussion of the mechanism behind resistance switching is too broad a subject for this chapter; however a few well-known cases are presented. Perhaps the easiest mechanism to understand is the conductive filament mechanism being used to explain switching in films such as NiO [45]. During resistance switching when V_{set} is applied across top and bottom electrodes, a path which is highly conductive (but not necessarily metallic) is formed through the film. Then a subsequent V_{reset} causes the disruption of these filaments. The mechanism behind reset is believed to be related to Joule heating [2].

Figure 5.4 shows transmission electron microscopy (TEM) images filament paths formed through a NiO thin film. In NiO we were able to observe changes only near the grain boundaries in this case. However current paths might also be formed within the NiO bulk, but were unobservable. Figure 5.4a shows the high-resolution transmission electron microscopy (HR-TEM) image of the polycrystalline NiO layers that show the electrical switching behavior. A highly ordered, stoichiometric structure can be seen in the TEM image of the grain interior. The grain-boundary region in the boxed area of Fig. 5.4a was further studied by the inverse fast Fourier transform (IFFT) TEM method as shown in the left-hand side (Fig. 5.4b). The electron energy-loss spectroscopy (EELS) spectrum at the grain boundary exhibits only a sharp nickel L2,3 edge peak (854 eV) indicating that Ni becomes concentrated in this region after setting to low resistance state [46]. XPS data for two NiO samples deposited by reactive DC magnetron sputtering are compared in Fig. 5.4c. The most interesting feature in Fig. 5.4c is the coexistence of a metallic nickel peak, at 852.8 eV, and a NiO peak, at 854.3 eV, for NiO samples deposited at an O_2 partial pressure of 5 %, while the 30 % sample which does not show bistable resistance switching lacks these features. SIMS results in Fig. 5.4d show that the O atoms within the NiO layer diffuse out toward the platinum electrode after the electrical switching, indicating the nickel-rich condition in the NiO layer.

Metal–insulator–metal cells which follow the filament type unipolar mechanism are programmed as shown in Fig. 5.4e. In the pristine state the device begins in the high resistance state, and voltage sweep (or voltage pulse) of at least V_{set} is applied. In order to prevent electrical breakdown for electrical sweep measurements a current compliance value is used (10 mA in Fig. 5.4e). Subsequently, when the device is in the LRS, a second voltage sweep (or pulse) to V_{reset} will recover the device to the HRS. Reading of the states without affecting their values can be done at a voltage sufficiently smaller than V_{reset}. Also, in order to better understand the chaotic switching data distribution, Yoo et al. analyzed conducting filament paths of the oxide thin film by using statistical method [47].

Bipolar switching which occurs in TMO such as TiO_2 will be described more in detail in the next materials section as their behavior is similar to perovskites.

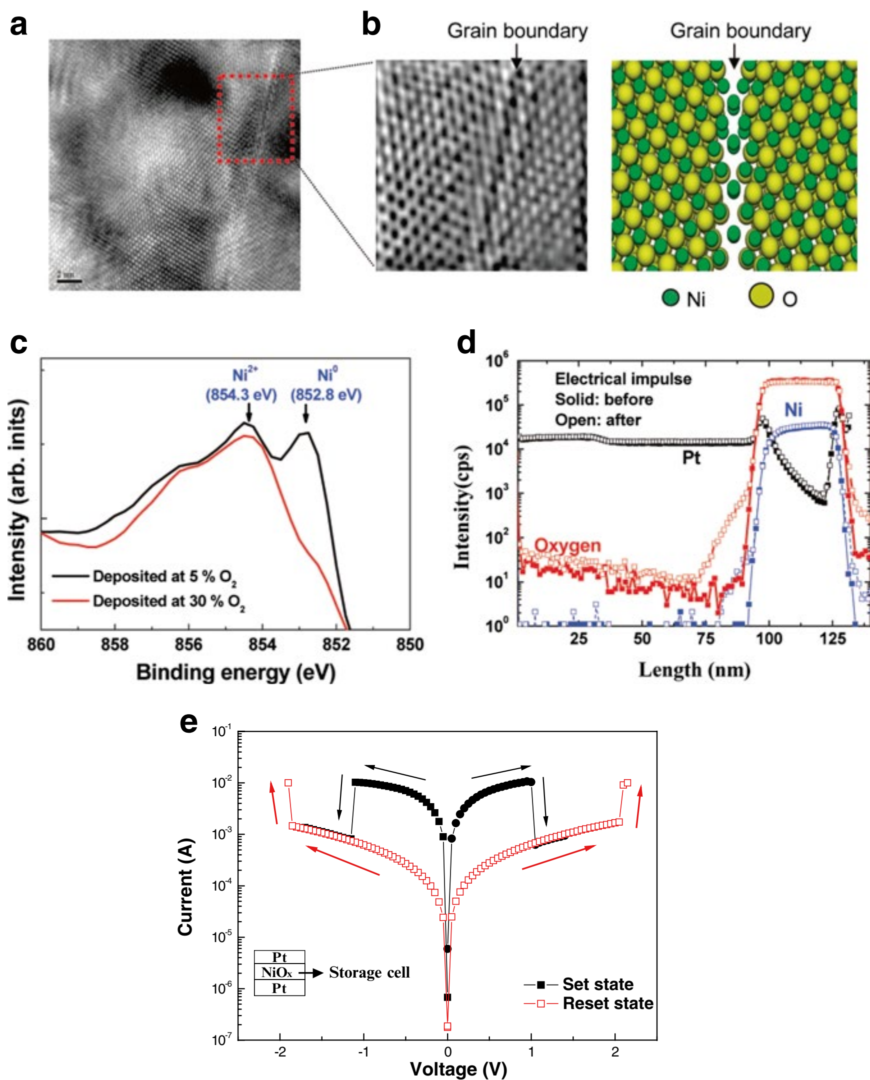


Fig. 5.4 (**a**) High-resolution transmission electron microscopy (HR-TEM) image of the NiO layer, which shows the electrical switching behavior; crystalline order can be seen in the bulk of grains, and scale bar represents 2 nm. (**b**) *Left panel* shows an inverse fast Fourier transform (IFFT) transmission electron microscopy (TEM) image of the boxed area in panel (**a**), showing the grain-boundary region; the right side is a schematic drawing of the grain boundary in NiO, showing the location of the cations (*small spheres*) and anions (*large spheres*). Nickel nanofilament precipitates are present at the grain boundary. (**c**) X-ray photoelectron spectroscopy (XPS) analysis of NiO samples; the NiO sample that was deposited at an oxygen partial pressure of 5 % shows the coexistence of Ni (852.8 keV) and NiO (854.3 keV) peaks. (**d**) Secondary-ion mass spectroscopy (SIMS) data (for the 5 % oxygen partial pressure sample) showing the movement of O and Ni across the electrodes before and after electrical impulses. (**e**) Typical unipolar switching in Pt/NiO/Pt. Switching curve is symmetric: set and reset operations are performed at the same polarity. Reprinted with permission from [2]. Copyright 2009, ACS

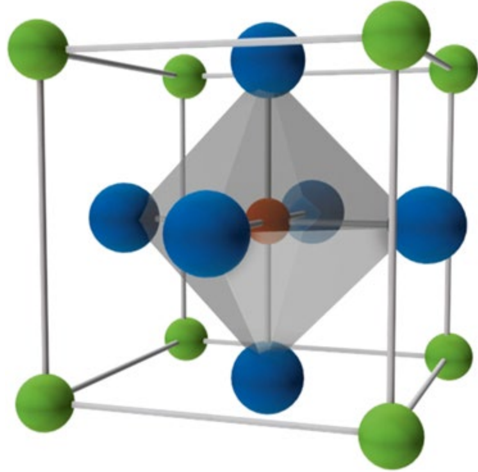


Fig. 5.5 Example of perovskite structure ($CaTiO_3$). Small atom at center is Ti^{4+}, Atoms at cube edges are Ca^{2+} and Atoms at face centers are O^{2-}

5.2.2.2 Perovskites

In the perovskite structure (ABO_3), atoms A sit at cube corner positions (0, 0, 0), B atoms sit at body center position (1/2, 1/2, 1/2), and oxygen atoms sit at face centered positions (1/2, 1/2, 0) as shown in Fig. 5.5.

An undersized B cation can be slightly offset from the center due to strong electric fields. The resulting electric dipole is responsible for the property of ferroelectricity in perovskites such as Barium Titanate. Perovskites such as $SrZrO_3$ [6], $Pr_{0.7}Ca_{0.3}MnO_3$ [7], LaCaMnO [48], $SrTiO_3$ [24] have demonstrated bistable resistance switching. Fabrication of perovskite oxides is more complex in comparison with transition metal oxides, and slight changes in the stoichiometry can lead to crystal distortions and unwanted effects [7]. The mechanism behind bipolar switching is attributed to three separate effects: Schottky barrier modulation by charge injection at the interface, reduction and modulation of oxygen ion at the interface, and charge trapping and detrapping at the vacancy sites. For most metal–oxide contacts there should be a formation of a metal–semiconductor Schottky barrier at the contact. Moreover bipolar resistance switching has never been reported for the case where both contacts to the oxide are purely ohmic [49]. At the metal–oxide interface trap states are formed as is usually the case [50]. When a bias is applied to the electrode, charge is injected by Schottky emission (electrode-limited), Pool–Frenkel emission (bulk limited), or Fowler–Nordheim tunneling at the high fields concentrated near the interface [51]. These injected charges can become trapped at defects such as vacancies, impurity, interstitials, or interfaces within the insulator. The trapped charges can effect the width and/or height of the electrostatic barrier at the metal–semiconductor junction modifying the resistance of the device [51]. For example in $Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO) and Nb doped $SrTiO_3$ (Nb:STO) samples, it was shown that the density of oxygen vacancies near the interface was important to bistable resistance switching. Sawa et al. described the mechanism behind the

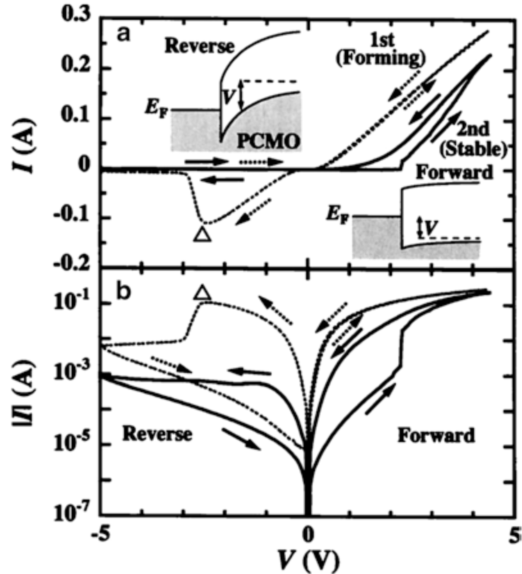


Fig. 5.6 *I–V* characteristics of a Ti/PCMO/SRO layered structure drawn in (**a**) linear and (**b**) semi-logarithmic current scales. Insets schematically show electronic band diagrams for a rectifying Ti/PCMO interface. Reprinted with permission from [49]. Copyright 2004, AIP

change in oxygen vacancies to be due to electrochemical migration of oxygen vacancies near the interface. While the complete role of oxygen vacancies in regard to bipolar switching is not fully understood, one explanation is that oxygen vacancies act as *n*-type donors in *n*-type oxides and acceptors in *p*-type oxides, the number of vacancies can effect the depletion layer width.

Figure 5.6 shows an example of bipolar resistance switching behavior in PCMO. Programming is done by voltage sweep to V_{set} in the direction of positive bias. Reset operation is performed with a voltage sweep to V_{reset} in the opposite direction (in Fig. 5.6). Read operation can be done with either positive or negative bias as long as the voltage is sufficiently lower than V_{reset} and V_{set}. The aforementioned charge injection and trapping mechanisms is modelled, showing how bistable resistance switching occurs.

In contrast to transition metal oxide materials, the electrodes on either side of perovskite based RRAM has been traditionally been different. Any type of electron conductor can be used in unipolar switching case of TMO, however modulation of a single barrier being easier than complexity involved with two barriers leads to different electrode selections. For example, Ohmic contact on one side, and Schottky contact on the other. Also the earliest reports for perovskite materials focused on high quality single crystal or epitaxial samples, leading to limitations during growth [6, 7]. We should note however currently bistable resistance switching has been shown for polycrystalline perovskite materials as well [52].

The Mott transition was reported for perovskite materials [53], the transition from weakly to strongly correlated electrons is used to explain the phenomenon in this case. The transitions are explained as occurring due to charge injection.

Ferroelectric polarization causes changes to the tunneling properties or the Schottky-type space-charge layer in adjacent semiconducting layers. The ferroelectric effect does not have any direct evidence to date and is mentioned here only for thoroughness.

5.2.2.3 Solid Electrolyte Based Materials

Another class of materials we will discuss are those based on solid electrolytes. Examples of materials of this class are primarily Ag and Cu-based in solid electrolyte systems [54, 55]. Oxides or Chalcogenides with a varying concentration of Ag or Cu are fabricated between one relatively inert electrode such as Pt or W and one electrochemically oxidizable electrode (Ag or Cu) which acts as a source and sink for mobile ions. Solid electrolyte based memories have also been called conductive bridging RAM (CBRAM), and programmable metallization cell (PMC) in the literature [55].

The current–voltage characteristics of ion based materials can be described as bipolar, that is set and reset operations occur at opposite polarities. However the mechanism behind resistance switching is different from previously mentioned bipolar memories. In this case the insulating matrix should exhibit ionic conductivity, applying a bias across the electrodes the conductive ions can migrate through the insulating matrix until a metallic filament path is formed through physical movement of ions. A schematic of the filament formation is shown in Fig. 5.7a. By applying a negative bias to the inert electrode, ions from the oxidizable electrode and within the electrolyte begin to form a filament path as they are reduced by electrons from the inert electrode. By applying high fields in the opposite direction the formed filament can be oxidized and broken again through ionic conduction.

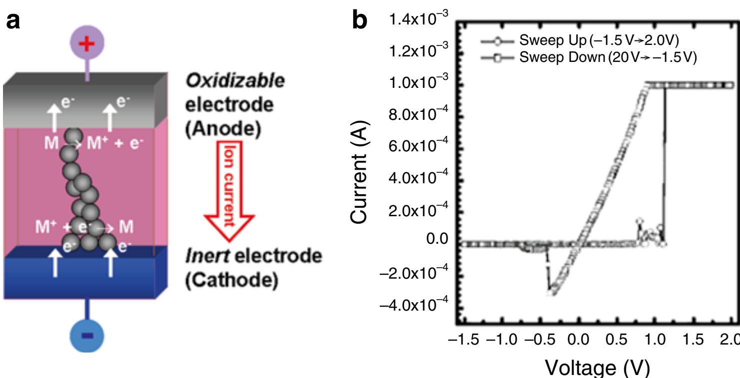
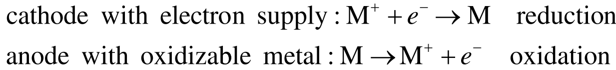


Fig. 5.7 (**a**) Schematic of formation of filament path in ion based memory cell. (**b**) A typical current–voltage plot for one cycle in a 0.5 μm diameter PMC device with a 200 nm thick silver-rich $Ge_{45}Te_{55}N$ (30 %) solid electrolyte using a 1 mA current limit. Reprinted with permission from [56]. Copyright 2006, The Electrochemical Society

The reactions taking place during oxidation and reduction are as follows:



$$\text{cathode with electron supply}: \mathrm{M}^{+} + e^{-} \rightarrow \mathrm{M} \quad \text{reduction}$$
$$\text{anode with oxidizable metal}: \mathrm{M} \rightarrow \mathrm{M}^{+} + e^{-} \quad \text{oxidation}$$

where M^+ is mobile ion, and e^- is electron.

In most cases an initial formation process is required before normal set/reset operations. The current and voltage levels during operation are typically much smaller (~10×–100×) than other resistance-based memories. Figure 5.7b demonstrates operation of ionic memory cell, the set voltage is ~1 V, the reset voltage is ~0.3 V, and the maximum current value is ~1 mA. The speed of the device is limited by ionic transport across the electrolyte layer, for very thin layers (<10 nm) the switching speed can be as low as a few tens of nanoseconds for Ag doped Ge–Se electrolytes system, which exhibit high ion mobility [55].

5.2.2.4 Summary

So far we have discussed just a few possible mechanisms and materials which show bistable resistance switching. Resistance switching seems almost universal across not only oxide materials but also polymers [57], molecules [26], and even carbon nanotubes [58]. The mechanism behind each is as varied as the type of materials. Unfortunately in most cases the switching mechanisms are still unclear although the switching phenomenon has been clearly observed. In spite of several models including band bending by charge trapping, conducting filament formation/rupture by Joule heating, and the change in the oxidation state of the cations, having been suggested clear experimental proof has been difficult to show.

Figure 5.8 shows the "family tree" for resistance-based memories including materials and shows where oxide-based memories mentioned fit into the bigger picture. Due to the scaling limit of conventional charge-based memory, non-charge-based memory such as resistance-based non-volatile memories have been proposed. However, the technology is not yet sufficient for application.

5.3 Oxide RRAM Based Materials and Applications

5.3.1 RRAM Scaling

The minimum cell size for resistance switching has not yet been shown, and theoretical modems have predicted that resistance switching should occur down to nearly the molecular size [2]. Figure 5.9 shows cell size vs the input switching power (left *y*-axis) LRS to HRS (calculated as $I_{\text{off}} \times V_{\text{off}}$) in the NiO sample. Corresponding switching time is shown in the same figure (right *y*-axis). Evidence shows that fewer and/or thinner filaments were formed at smaller cell sizes. The reduction in switching

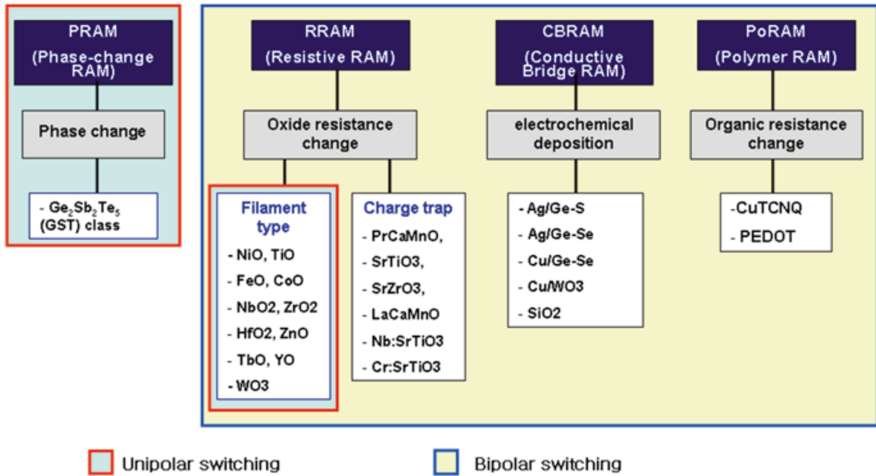


Fig. 5.8 Resistance change materials as switching mechanism

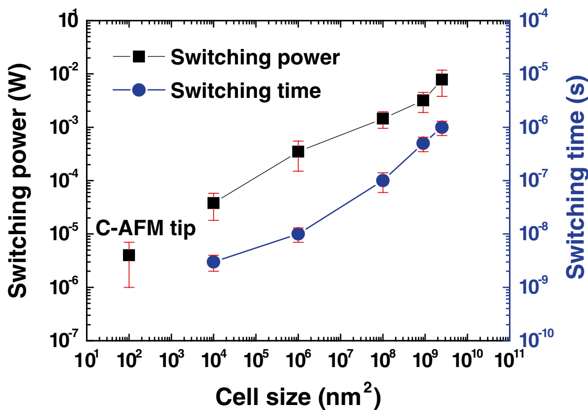


Fig. 5.9 Switching speed and input power by cell size. Cell size versus switching power and speed: power is calculated based on measurements from the LRS state to the HRS state by taking the product of maximum current and applied voltage. The error bar at the each node size is determined by the standard deviation of 5–10 successive measurements. The vertical error bars are experimental uncertainties that are due to the distribution of the switching operation. An additional data point for the current-sensing atomic force microscopy (CS-AFM) results is shown at 10×10 nm^2. Reprinted with permission from [2]. Copyright 2009, ACS

time is not accounted for by the decrease in the number of filaments alone; since they should rupture individually and switching time should be independent of cell size. It is reasonable that the resistivity of the filaments may be different in this case depending on cell size. Along with the fact that switching times begin to saturate as cell size decreases below 10×10 nm^2 we can explain this based on the thermal energies. The migration barrier of an oxygen atom has been calculated to have activation energies of 2–3 eV, depending on the charge states of the oxygen vacancy, for diffusion via vacancy mechanism.

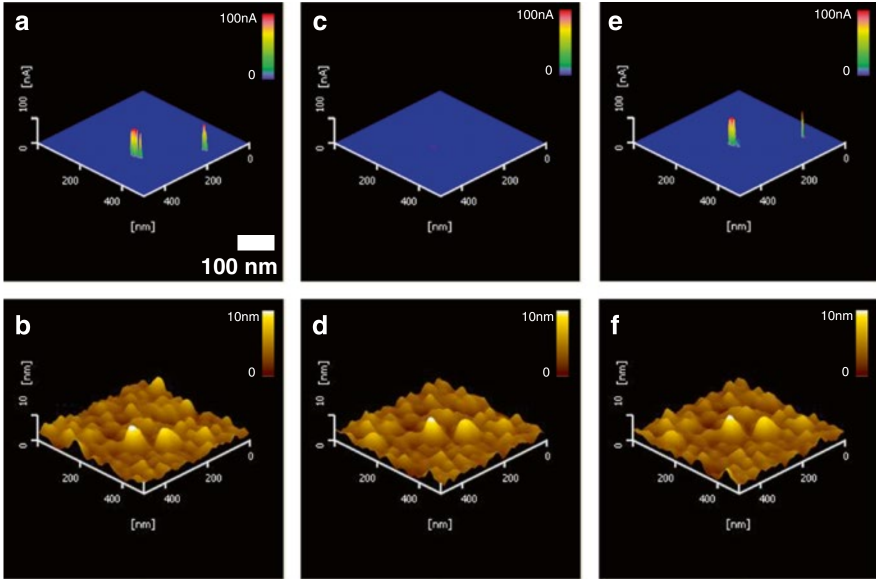


Fig. 5.10 Nanoscale switching current paths in NiO (**a**) Low resistance state (**c**) High resistance state (**e**) Low resistance state CS-AFM (*top*) and the corresponding topographical AFM images (*bottom*) of cell in the LRS and HRS states. (Control over the formation and destruction of nano-filament current paths is done by biasing the CS-AFM tip). R_{on} was switched by a CS-AFM scan with a 2.3 V bias [i.e., "SET" scan; (**a**) and (**b**)]; R_{off} was switched by a scan with a 1.5 V bias [i.e., "RESET" scan; (**c**) and (**d**)]; and Ron switched back again with 2.3 V (**e**, **f**). The local current images of both R_{on} and R_{off} were acquired with a bias of 0.05 V through the tip [59]. Reprinted with permission from [59]. Copyright 2007, Phys. Status Solidi (RRL)

Therefore during the time scale for device operations the thermal energy is critical for electromigration. Joule heating is thought to be the largest contributor to the thermal energy. Because the power scales with node area, the local temperatures are greater in smaller cell sizes and leads to the observed saturation in switching times.

Furthermore by using a conductive atomic force microscopy (AFM) tip, filamentary paths across NiO could be directly measured. Figure 5.10 shows the results of the experiment going from low resistance to high resistance then back to low resistance states [59]. The size of these paths was measured to be around 10 nm, however this is the same as the size of the AFM tip used in this cases, and even smaller filament paths should form. The conclusion so far has been that as far as scaling goes, bistable resistance switching should reach the limits of just a few unit cells.

5.3.2 Oxide-Based Switches for RRAM

Before going further into RRAM applications or structures, an important aspect of oxide-based RRAM are switch elements. Traditional DRAM uses a transistor to select the program cell and a capacitor to store the state (1T–1C). While continuing

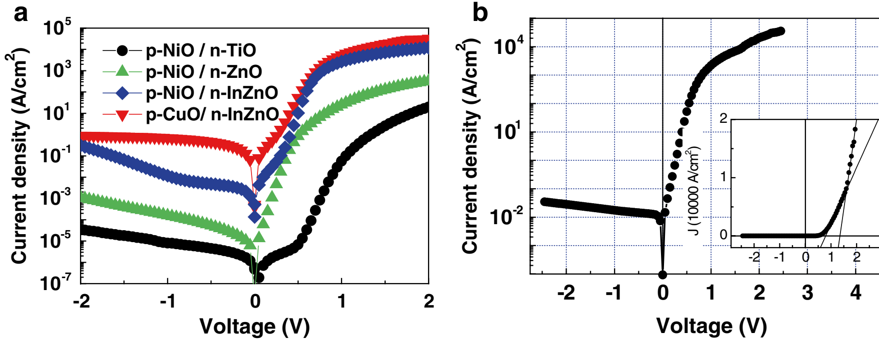


Fig. 5.11 (**a**) The difference in forward current density for some different oxide material combinations. (**b**) Current density versus applied voltage curve of Pt/CuO/IZO/Pt in semi-logarithmic scale. The *inset* is depicted in linear scale. *Lines* are guides to the eyes. Reprinted with permission from (**b**) [60], copyright 2008, Wiley InterScience

development towards oxide-based memories it becomes interesting to consider alternative to a traditional transistor-based switch element. In particular two switch elements which are composed to transitional metal oxides: The oxide *p–n* diode and threshold switch are discussed.

For use as a type of switch, oxide semiconductors can be made as both p- (NiO, CuO) and n-type (ZnO, TiO_2), and can further be combined into an oxide *p–n* heterojunction diode. In contrast to traditional Si diodes, oxide diodes can be fabricated as polycrystalline material with high current density. In addition typical processing temperatures are on the order of 500 °C compared to high temperature processes (~1,000 °C) required in Si. Currently an oxide diode combination which boasts both high rectifying ratio and current density is required. However initial feasibility studies of the diode and bistable resistance element (1Diode–1Resistor) have been reported [10]. For oxide-based diodes, it was experimentally shown that reducing the bandgap for both p- and n-type materials leads to increased forward current densities as shown in Fig. 5.11a. In case of *p*-CuO/*n*-IZO the current density under forward bias was about 3.5×10^4 A/cm^2 which is the highest reported record for oxide thin film diodes to the best of our knowledge. The rectifying characteristics of oxide *pn* diode are clearly shown in Fig. 5.11b.

A structure similar to this was connected in series with resistance switching element and shown to flow enough current to access the storage element (NiO) while the diode was under forward bias, and conversely deny access while under reverse bias [10]. Figure 5.12 shows the combined *I–V* characteristics and structure of the tested device.

As a second type of switch one possible form resistance switching can be exhibited in oxide materials is threshold switching characteristics. That is past a certain threshold voltage (V_{th}) the resistance value of the device decreases dramatically, and can be held in that state above a certain hold voltage. By combining a threshold element in series with a unipolar or bipolar switching element, a switch and storage unit can be used to address and store bits in an array. Threshold devices are easily

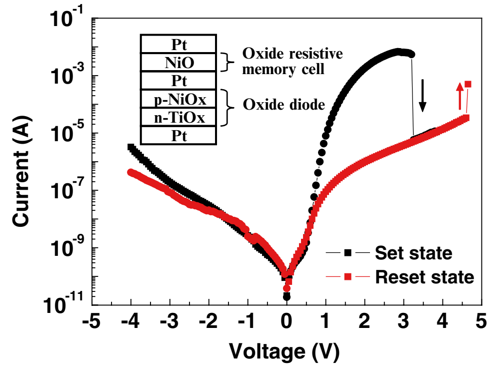


Fig. 5.12 *I–V* characteristics of a combined Pt/NiO/Pt/*p*-NiO_x/*n*-TiO_x/Pt structure, namely, 1Diode/1Resistor structure, a schematic diagram of which is shown in the inset. Reprinted with permission from [10] Copyright 2007, Wiley InterScience

fabricated using processes used for the storage element as well. For example, depositing NiO at high oxygen partial pressures leads to threshold switching behavior [8]. Other examples of threshold switching oxides are: VO_2 and chalcogenide-glass thin films [12]. Advantages that threshold devices have over transistors or diodes are much higher current densities, and being composed of a single layer rather than a *p–n* junction.

Experimental results showing the feasibility of a combined memory and threshold switching device are shown in Fig. 5.13 [61]. The memory switching element (NiO deposited at 5 % oxygen partial pressure) is tested first, and operation can be seen in Fig. 5.13a. Next the threshold switching element (VO_2 deposited at 20 % oxygen partial pressure) operation is shown in Fig. 5.13b. Finally the combined device operation is shown in Fig. 5.13c. Fig. 5.12 clearly indicates both the bistable switching characteristics of the NiO memory element and the threshold switching characteristics of the VO_2 switch element. Up to the threshold voltage the cell is inactive since the switch element is in the off state. Past the threshold voltage the cell is active since the switch element is in the on state and the stored information can be read by applying an appropriate reading voltage just above the threshold voltage. By applying a writing voltage comparable to V_{set} or V_{reset}, the cell can be accessed and programmed since both are higher than the threshold voltage. Additionally we can access a single cell exclusively by applying read or write voltage to that cell while applying a voltage less than the threshold voltage to all the other cells.

Both threshold switch and oxide diodes are advantageous for cross-point structures which can theoretically achieve the cell sizes of $4F^2$ (F: feature size used for patterning the cell). Additionally since the underlying film is not a major limitation and fabrication can be performed at low temperature stacking of several cross-point structures becomes possible. Figure 5.14a demonstrates a three-dimensional stacked structure using either threshold or oxide switch elements [61]. All fabrication steps can be performed using conventional semiconductor processing technologies available today and materials research such as increasing forward current density in oxide diode materials, and improving cell to cell V_{set} distribution in threshold switch and memory elements is the most important issue. The switch elements allow for

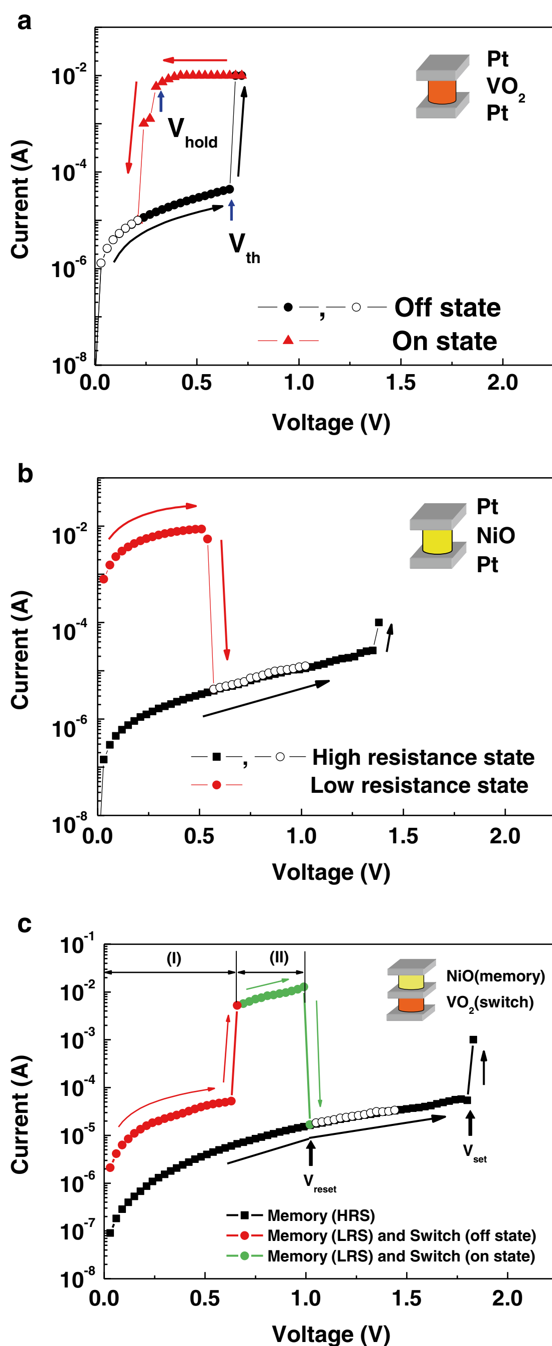


Fig. 5.13 (**a**) Threshold switching of a Pt/VO/Pt switch element and (**b**) Bistable resistance switching demonstrated for a Pt/NiO/Pt memory element where NiO film was deposited at 5 % oxygen partial pressure. (**c**) Programming characteristics of combined oxide switch and oxide memory elements. The figure clearly indicates both the bistable switching characteristics of the Pt/NiO/Pt memory element and the threshold switching characteristics of the Pt/VO_2/Pt switch element. In region (I), the cell is inactive since the switch element is in the off state. In region (II), the cell is activated since the switch element is in the on state and the stored information can be read by applying an appropriate reading voltage in that region. By applying a writing voltage comparable to V_{set} or V_{reset}, the cell can be accessed and programmed since both are higher than V_{th}. Therefore, we can access a single cell exclusively by applying read or write voltage to that cell while applying a voltage belonging to region (I) to all the other cells. Reprinted with permission from [61]. Copyright 2007, Wiley InterScience

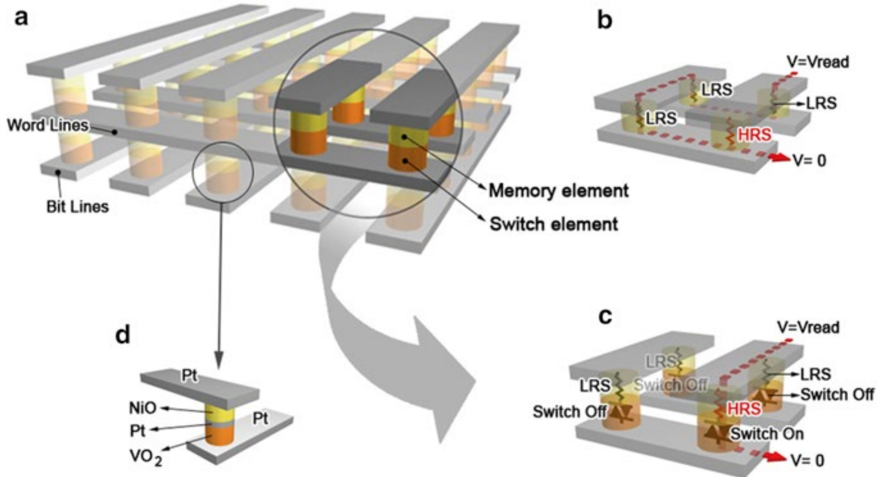


Fig. 5.14 (**a**) Generalized cross bar memory structure whose one bit cell of the array consists of a memory element and a switch element between conductive *lines on top* (word line) and *bottom* (bit line). (**b**) Reading interference in an array consisting of 2×2 cells without switch elements. (**c**) Rectified reading operation in an array consisting of 2×2 cells with switch elements. (**d**) Detailed structure of a single cell consisting of a Pt/NiO/Pt memory element and a Pt/VO_2/Pt switch element. Reprinted with permission from [61]. Copyright 2007, Wiley InterScience

random access to memory cells while preventing reading interference between neighboring cells. Figure 5.14b demonstrates a typical reading error which might occur without switching elements present due to current following path of least resistance. Finally by adding the switching element we can see how the reading errors can be corrected.

5.3.3 *RRAM State of the Art*

In order to reach extreme high density such as terabit era, not only will we need to scale down, but apply current flash technologies such as MLC and 3D cell stacking technologies. Figure 5.15 demonstrates the requirements for reaching these densities: current planar scaling works down to 20–30 nm and can achieve 100 Gb densities, having 3–4 bits per cell using MLC technology, and 4 to 5 stacked cell layers we can achieve approximately 1 Tb. However all these technologies must be incorporated into the final product, and the integration will not be trivial.

First considering the stacking requirement of 4–5 layers, one limitation which isn't immediately apparent is the area which peripheral circuits will consume on the chip. Figure 5.16a shows the stacking possible with Si based peripheral circuits. However by using an all-oxide based memory GaInZnO (GIZO) transistors can also be stacked three-dimensionally improving the use of expensive Si real estate. Figure 5.16b demonstrates how an idealized peripheral circuit structure can be stacked. In Fig. 5.16c a comparison is made between the required areas for both

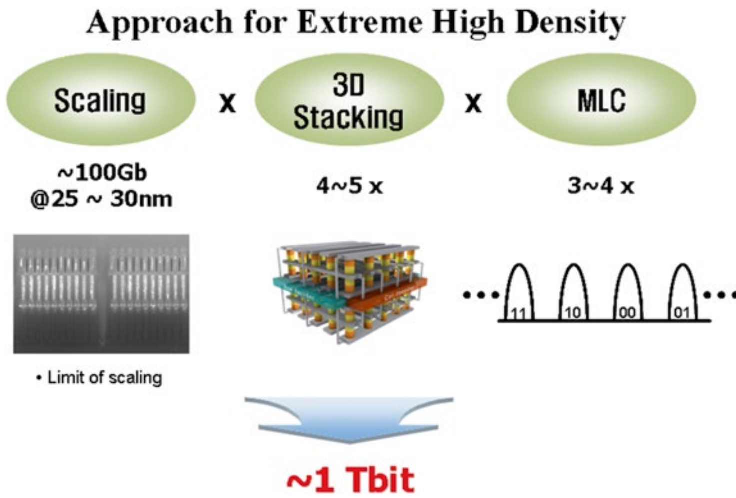


Fig. 5.15 Requirements of technologies required to reach extremely high density memories

types of structures, at ~4 stacks the area requirements for stacking begins to outweigh the benefits in a conventional Si peripheral circuit structure.

GIZO transistors in conjunction with RRAM cells have been tested and shown to be feasible, leading to even further advantages for all-oxide based memories. Figure 5.17a shows a schematic diagram of a combined GIZO select transistor with 1D–1R structure. The GIZO transistor is gated to 5 V and the saturation region during programming and full operation of the 1D–1R device can be seen in Fig. 5.17b. With the GIZO transistor gated at 1 V read operations is possible however, the current is insufficient to switch the state to of the 1D–1R device from low resistance to high resistance. Finally when the select transistor is not gated, there is only minimal leakage current.

Second, the scalability of 1D–1R devices should be investigated further. Below in Fig. 5.18 a 1D–1R device using selective epitaxial growth (SEG) of Si was used to test RRAM cell sizes of 50 nm over Si SEG diodes. As mentioned previously for 50 nm oxide diodes to become a reality research towards high forward current density materials is needed.

5.3.4 Summary

As described so far, several pieces required for extreme high density oxide-based resistance memories are already in place. Stacked one time programmable (OTP) memory is already being sold by Sandisk Corporation. Theoretically oxide-based memories can already be used to replace traditional Stacked OTP memories. Similarly the structure of stacked OTP memory can be easily fabricated using

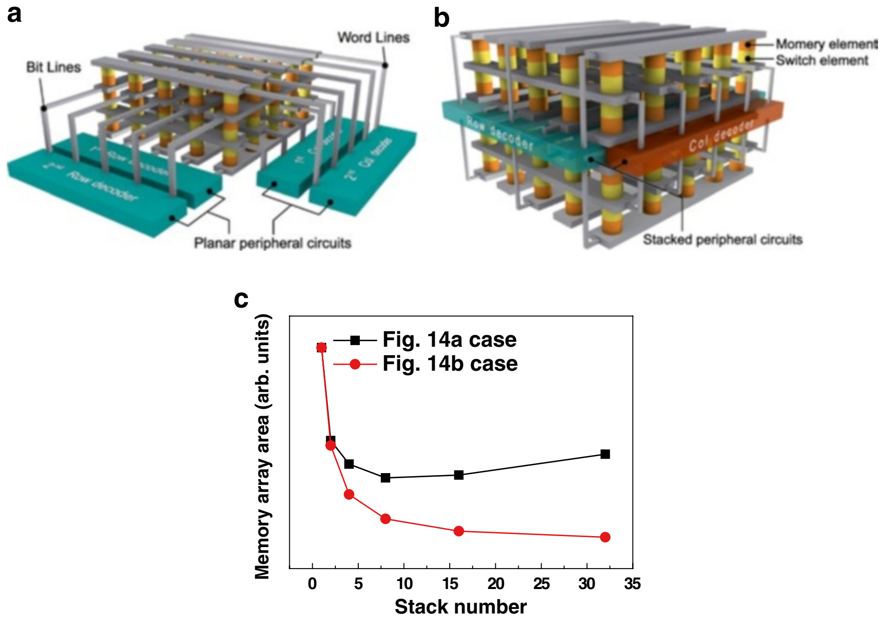


Fig. 5.16 (**a**) Diagram of currently proposed structure for stacked memories with peripheral circuit. (**b**) Conceptual diagram for ideal stacking structure utilizing stackable peripheral circuits. (**c**) Comparison of overall memory array area as a function of the number of stacks in planar structure and stacked structure. Planar structure shows diminishing returns and eventual increase at ~4 stacks. Reprinted with permission from [62]. Copyright 2009, Wiley InterScience

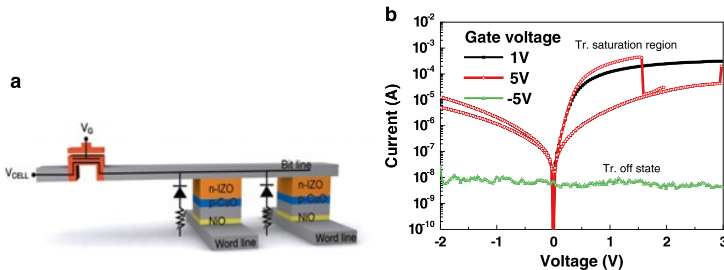


Fig. 5.17 (**a**) Schematic diagram of two 1D–1R cells connected to a GIZO select transistor. (**b**) Operation of a 1D–1R cell with a select transistor biased to off and on in both a saturation and in a linear regime. Reprinted with permission from [62]. Copyright 2009, Wiley InterScience

all-oxide materials as well. Figure 5.19 shows scanning electron microscope (SEM) cross section of stacked OTP memories, we should notice that there are no major limitations in the materials, or techniques, or processes discussed for oxide memory. Moreover low processing temperatures in oxide materials should allow for even more flexible device design.

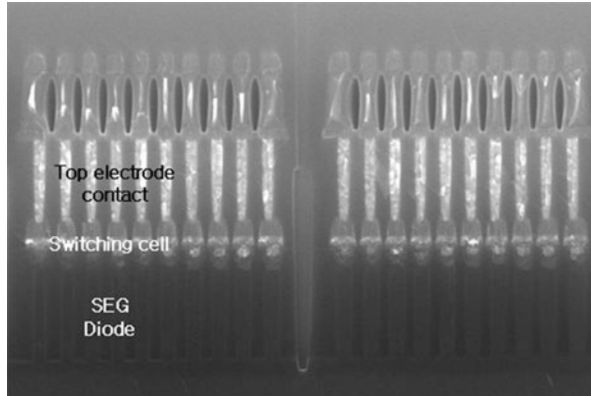


Fig. 5.18 Partial SEM image of the selective epitaxial growth (SEG) Si diode and resistance change memory array. 1D–1R array was fabricated using SEG diode for switch and NiO for storage

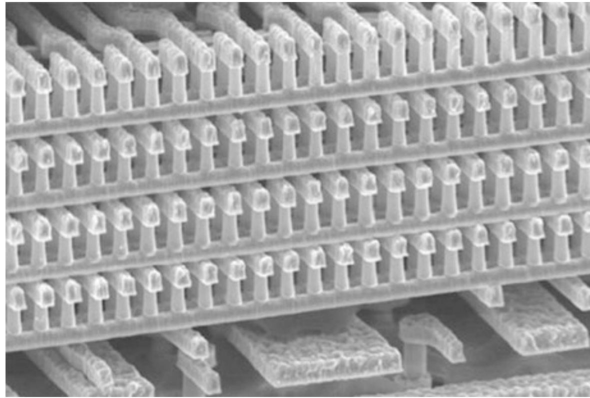


Fig. 5.19 Four layers of a cross-point diode memory array with tungsten bit and word lines in a 3D memory. Reprinted with permission from [63]. Copyright 2006, The Electrochemical Society

5.4 Outlook and Future of RRAM

The critical issues for the future development of RRAM devices are reliability, such as data retention and memory endurance (the number of erase and program cycles), and the characteristic variation from cell to cell and from chip to chip. In silicon most of these issues arise due to defects, impurities, or contamination. However in oxide-based devices variations in device characteristics seem almost intrinsic.

First by a more thorough study of behind the switching mechanisms an improvement in the reliability and predictability of oxide-based memories is required. Only then can we successfully design simulation and modeling tools and needed to design and test high density memory chips. Having been the subject of three decades of research still with no clear answer, this will obviously not be an easy task. On the bright side, experimental results have shown that oxide-based memories offer excellent scalability showing bistable resistance switching behavior down to just a few unit cells.

Second, a detailed look into the exact metal–insulator–metal structures and 1D–1R structure needs to be performed. Currently, most research is done with MIM cells combined in series with a switch element connected by a metal layer. However, during integration this structure (MIM-*p*type semiconductor -*n*type semiconductor–metal) is unwieldy. Initial steps towards improving the structure should be focused on eliminating the connecting metal layer. The final goal should be the discovery of a material which with a change in doping type, or stoichiometry can have the functions of both switch and storage elements.

Finally a method of controlling the electrical switching down to just a few atoms is needed. The author does not suggest to know the answer to how this can be possible, however by being able to control the exact type and degree of resistance switching previously unobtainable devices such as memristors become possible. By not being confined to be either "0" or "1," but being able to achieve a continuous number of resistance values more flexible device designs and circuit designs become possible.

5.4.1 Conclusion

This chapter has focused on introducing the past few years research being done in oxide-based resistance memories. Renewed interest over the past few years has led to several new results and ideas based on oxide materials. While previous results have given new hope for the future, realization of oxide-based resistance memories still requires much fundamental research. In particular the mechanisms behind switching need to be improved, and a unified model for threshold and bistable resistance switching is needed. Also a more quantitative description of the roles of defects and impurities is required. Both transition metal oxides and perovskites offer their own distinct advantages and it is not clear which material type or which switching type is superior at this time.

The different types of oxide materials, and switching phenomenon observed so far have allowed for interesting device applications, however materials research is the key issue for finally achieving mass producible memory. Terabit memory seems possible if certain key breakthroughs can be made: improvement of cell-to-cell programming variation, scaling issues down to 20 nm, oxide diode forward current density, and multilevel cell programming.

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