Chapter 1
Review of the Science and Technology for Low- and High-Density Nonvolatile Ferroelectric Memories

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1.1 Introduction

The new millennium has witnessed the coming to age of one of the major fields of research of the twentieth century, i.e., the field of ferroelectrics. Major advances occurred in the last two decades in research related to the science and technology of ferroelectric (high permittivity) and related metallic and metal-oxide thin films and their integration into layered heterostructures for application to the development of nonvolatile ferroelectric memories (FeRAMs). The high dielectric permittivities of perovskite-type materials can be advantageously used in dynamic random access memories (DRAM) [1], while the large values of switchable remanent polarization of ferroelectric materials are suitable for nonvolatile ferroelectric random access memories (FeRAM) [2–16]. The research performed during the last two decades focused on developing both the scientific and technological bases of ferroelectric films and layered heterostructures and their integration into ever evolving device architectures and the development of new device architectures for high-performance FeRAMs [1–10, 14–17].

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The research on materials and materials integration strategies triggered by the applications to FeRAMs demonstrated that the science of the complex oxide thin films relevant to FeRAMs is also important to a wide range of applications in discrete devices, utilizing the full range of the oxide film properties, including dielectric, ferroelectric, piezoelectric, electrostrictive, pyroelectric, optical, electro-optic, and magnetic properties, as well as electronic conduction, ionic conduction, and superconduction. Applications include multilayer capacitors for memories, piezoelectric film-based microelectromechanical systems (MEMS), boundary layer capacitors, varistors, gas sensors, radiation detectors, temperature sensors, transducers, switches, shutters, MHD electrodes, fuel cell electrolytes, concentration cell electrolytes, and electrolytes for high energy density batteries. These ceramics represent an important world market, which has been experiencing steady growth in recent years [18].

The major scientific and technological advances produced in the last 11 years in the materials science and devices related to the field of ferroelectric thin films have been possible because of substantial advances in the discovery of new ferroelectric materials and development and optimization of thin film deposition techniques, as well as the development of novel materials integration strategies and device concepts. As indicated above, ferroelectric thin films play a major role in a large variety of devices. However, nonvolatile ferroelectric random access memories (FeRAMs) represent the first ferroelectric thin film-based device introduced into a mass consumption market in the form of low density memory "smart cards" [19, 20]. Therefore, this chapter is dedicated to reviewing major advances made in science and technology related to FeRAMs.

Major advances were produced in thin film deposition techniques. Various physical vapor phase deposition techniques [plasma and ion beam sputter deposition (PSD and IBSD, respectively), pulsed laser ablation deposition (PLD), electron beam or oven-induced evaporation for molecular beam epitaxy (MBE), chemical solution methods (e.g., sol–gel processing and metalorganic decomposition-MOD), liquid source misted chemical deposition (LSMCD), and metalorganic chemical deposition vapor deposition (MOCVD)] have been optimized and extensively used in the past 11 years to investigate the synthesis of ferroelectric films and layered heterostructures [5–16]. However, MOCVD is the film synthesis technique most suitable for the fabrication of high-density FeRAMs, particularly for the new concepts currently being explored for high-density memories, which may require 3D capacitor structures with high aspect ratio, thus needing conformal growth of ferroelectric films with excellent composition and thickness uniformity. An alternative CVD technique that may be even better than MOCVD for coating high aspect ratio 3D nanoscale structures required for high-density FeRAMs is atomic layer deposition (ALD), which has been demonstrated to produce extremely conformal layers on nanoscale 3D structures. However, most work until now, using the ALD film deposition technique, focused on producing metallic and amorphous oxide layers [21]. Only recently, first attempts at producing perovskite oxide crystalline layers have been attempted [22], but much work is necessary to develop ALD as a reliable technique to synthesize crystalline oxide layers. A major issue in relation to film

synthesis by any of the methods described above is the difficulty in reliably producing device-quality films directly on large semiconductor substrates, in a way that is fully compatible with existing semiconductor process technology. Issues related to deposition techniques are reviewed in this chapter in view of work performed in several laboratories worldwide.

Film synthesis techniques discussed in this review include sputter deposition, laser ablation deposition, MOCVD, and the newest ALD techniques, since the first three represent the most utilized deposition methods in relation to the science and technology of ferroelectric thin films, and ALD represents the upcoming method for producing device-quality ferroelectric thin films. All the three techniques can produce films with device-quality characteristics. However, various requirements are necessary for the application of film synthesis methods to industrial processes. A manufacturing process for producing ferroelectric thin film-based devices should at least include the following characteristics (1) applicability of the processes to deposition of ferroelectric films and integration with metallic or conductive oxide electrode layers with different physical and chemical properties, (2) compatibility with integrated device processing, including production of as-deposited films with specific microstructures (perovskite, for example) on substrates at the lowest possible temperature, (3) production of device-compatible, highly oriented, or polycrystalline films and heterostructures with specific properties (e.g., fatigue free for a large number of polarization switching cycles, long polarization retention times, and no polarization imprint effects) over large area substrates ($\geq$200 mm in diameter), (4) ability to produce patterned structures, superlattices, and layered heterostructures, (5) reproducibility of the deposition process, and (6) low-cost deposition processes with capacity for high deposition rates.

A major focus of research related to the development of FeRAMs has been on the development of new materials in thin film form and materials integration strategies to produce capacitors with memory-compatible properties and their integration with semiconductor devices to fabricate FeRAMs. This work has been focused until recently on 0.18 μm feature size FeRAMs, which resulted in insertion into commercial "smart cards" and embedded memories with relatively low density. The next frontier is the development of materials, materials synthesis techniques, and materials integration and device fabrication strategies to produce the next generation of nanoscale high-density memories ($\geq$1 Gb). Therefore, research on this field is reviewed here as well.

A theoretical understanding of the behavior of ferroelectric thin films and device working principles has been critical to the advances achieved in the science and technology of FeRAMs, and therefore it is also briefly reviewed here.

Finally, major advances in memory concepts and implementation are critically reviewed and considered in view of future developments. Many University, National, Private, and Industrial Laboratories have made major contributions to the science and technology of ferroelectric thin films and devices. However, it is difficult to include in a limited space all the work performed by many groups around the world. Therefore, we apologize if some references have been overlooked.

1.2 Ferroelectric Thin Film Synthesis and Characterization

1.2.1 Magnetron Sputter Synthesis and Characterization of Ferroelectric Thin Films and Heterostructures

Several variations of the plasma sputter deposition technique have been developed and extensively used for the synthesis of electrode and ferroelectric layers both in the research laboratory environment and in industrial fabrication of FeRAMs. Basic phenomena occurring during the interaction of plasmas with the targets and substrates, during film synthesis, are important in that they determine to a large extent the composition, microstructure, and properties of the films.

Extensive work has been performed in recent years on plasma sputter deposition of ferroelectric thin films. Both single multicomponent oxide and multiple elemental metallic targets have been used to synthesize a wide range of ferroelectric materials in thin film form, including $BaTiO_3$ (BTO) [23], $Ba_xSr_{1-x}TiO_3$ (BST) [24, 25], $PbTiO_3$ (PT) [26], $Pb_{1-x}La_xTiO_3$ (PLT) [27], $PbZr_{1-x}Ti_xO_3$ (PZT) [28], and Pb_{1-x} La_x (Zr_y Ti_{1-y}) O_3 (PLZT) [29] and $SrBi_2Ta_2O_9$ (SBT) [30]. Early work demonstrated that highly *c*-axis-oriented PT thin films can be produced by r.f. magnetron sputtering only when using low deposition rates (<20 Å/min), gas pressure of about 7×10^{-3} Torr, and PbO-rich targets [27]. These results were explained on the basis that high gas pressures in the magnetron system increase the sputtering rate because of the production of a larger amount of ions in the plasma, while simultaneously decreasing the mean kinetic energy of the sputtered species arriving at the substrate, due to collisions with the plasma species. A reduced kinetic energy of the depositing species results in a lower mobility on the substrate surface at the deposition temperature. The combination of high sputtering rate (hence high deposition rate) and low mobility of the depositing species tend to inhibit the epitaxial growth of the film. This work [27] demonstrated the importance of controlling the deposition parameters to optimize film properties for particular device applications.

Magnetron sputtering has also been used to produce PZT films with controlled stoichiometry and properties, utilizing metallic elemental targets [28]. This work revealed that the growth of stoichiometric highly oriented films via elemental target magnetron sputter deposition is governed by three main processes: (a) formation of a reproducible oxide layer on the target surface, (b) the stability of oxide species formed during transport through the plasma towards the substrate, and (c) the nucleation and growth of the film on the substrate surface. Computer simulations of the transport of sputtered species in the plasma and experimental measurements of deposition rate vs. gas pressure and film composition vs. substrate–target distance indicated that complex plasma–surface interaction and material transport processes control film composition, microstructure, and resulting electrical properties [28].

Magnetron sputter deposition was also used to synthesize layered perovskite films. The material most extensively investigated has been SBT [3], since SBT-based capacitors, using Pt electrodes, exhibit practically no fatigue, long polarization retention, low leakage, and negligible imprint, all necessary properties that

enabled SBT-based capacitors to be the basis for current commercial FeRAM "smart cards" [29]. Research by various groups [7–16, 18, 19, 23–27] demonstrated that PZT films grown on Pt/Ti electrodes on Si was not an appropriate technology for producing reliable FeRAM capacitors. Studies of film growth processes via ion beam sputter deposition in conjunction with in situ time-of-flight ion scattering and direct recoil spectroscopy provided evidence for the explanation of why the Pt/Ti electrode heterostructure did not work properly and for the solution to the problem (see ion beam sputter deposition section). Briefly, work on plasma sputter synthesis of ferroelectric thin films demonstrated that geometry and deposition conditions played key roles on the synthesis of ferroelectric thin films, using this technique. The work on magnetron sputter deposition provides valuable data from the basic science point of view mainly, since MOCVD turned out to be the most appropriate technique for industrial manufacturing of FeRAMs.

1.2.2 Ion Beam Sputter Synthesis and Characterization of Ferroelectric Thin Films and Heterostructures

Ion beam sputter deposition (IBSD) was used mainly as a versatile film-synthesis method for investigating the synthesis of ferroelectric thin films and heterostructures to understand fundamental materials synthesis and integration processes to guide the work with the synthesis methods such as MOCVD that were used in industrial processes. Multiple ion beam multi-target [30] and single ion beam/multi-target (SIBMT) [31] sputter deposition techniques were developed and extensively used to study the synthesis of ferroelectric and metallic thin films and heterostructures. The SIBMT method was specifically used to produce heterostructure capacitors with metal, conductive oxide, and hybrid metal-oxide electrodes [32] in studies focused on understanding materials integration to control polarization fatigue, retention, and imprint. Although the IBSD technique has not been used as standard industrial fabrication method, it provided valuable information that contributed to the development of materials integration strategies for the fabrication of FeRAMs, particularly for PZT and SBT-based FeRAMs, as discussed below.

1.2.2.1 SIBMT-Based Studies to Understand Processing–Microstructure–Property Relationships of Ferroelectric PZT Thin Films and Heterostructures

The main focus on the studies discussed in this section was to understand the mechanism of polarization fatigue, imprint, and polarization retention loss in PZT-based capacitors with Pt electrodes as a function of polarization switching cycles. These problems were solved for PZT-based capacitors by replacing the Pt electrode layers with metal-oxide electrodes. In this sense, the first demonstration of an oxide electrode controlling fatigue in PZT-based capacitors was produced by Auciello et al.

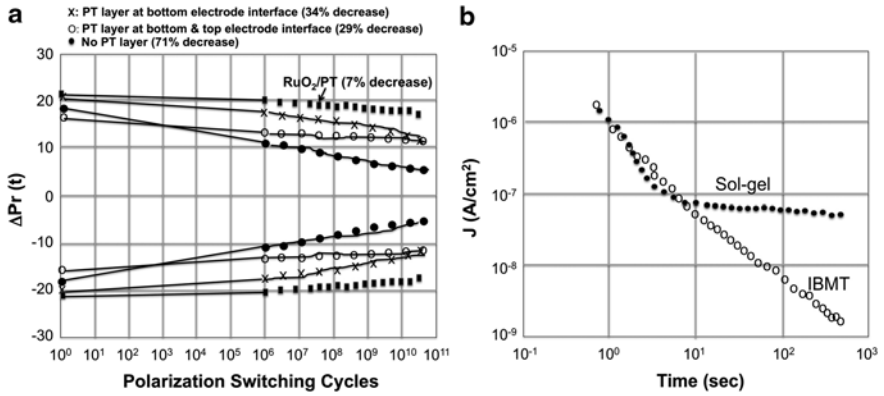

Fig. 1.1 **(a)** Change in remanent polarization vs. number of switching cycles (fatigue) of PZT-based capacitors with and without template $PbTiO_3$ (PT) layers at the bottom Pt electrode interface only [33] and of PZT capacitor with RuO_2/Pt electrodes on PT/PZT [34]. **(b)** Leakage current vs. time for leakage current of a RuO_2T/PZT/PT/RuO_2/MgO heterostructure capacitor produced with ion beam multi-target (IBMT) sputter deposition technique and a RuO_2/PZT/RuO_2/MgO capacitor produced with a sol–gel method [33]

using RuO_2 as the electrodes sandwiching a PZT ferroelectric layer [32]. The pioneering work on RuO_2 for PZT-based capacitors was subsequently confirmed by work performed by several groups using other electrically conductive oxide electrodes (e.g., RuO_2 [33], hybrid Pt/RuO_2 [34], $La_{0.5}Sr_{0.5}CoO_3$ (LSCO) [35], and hybrid Pt/LSCO [36]. More recently, IrO_x [37] and hybrid Ir/IrO_x [38] electrodes were developed to produce fatigue-free PZT capacitors, and these electrodes are being used in embedded FeRAMs, currently in commercial microcontroller systems [38]. The work performed by various groups also showed that electrode material and orientation and/or the PZT/electrode interface (including intermediate template layers) [33–36] were key to controlling of orientation of the ferroelectric layer and electrical properties of PZT-based heterostructure capacitors. Electrical characterization of PZT-based capacitors synthesized using a $PbTiO_3$ (PT) template layer at the bottom or top electrode/PZT interfaces revealed substantial differences in their fatigue behavior. Capacitors without the PT layer exhibited substantial fatigue (about 71 % reduction in remanent polarization), while those with one or two PT layers had substantially smaller fatigue (about 34 % and 29 % decrease, in remanent polarization, for one and two PT layers, respectively) (Fig. 1.1a) [33]. The incorporation of hybrid Pt/RuO_2 bottom electrode in the PZT capacitor, prior to producing the PT layer, resulted in highly oriented (001) PZT film and negligible fatigue ($\leq$7 % reduction in remanent polarization (Fig. 1.1a) [33, 34]). In addition, Al-Shareef/Auciello et al. demonstrated [34] that there was an optimum combination of individual layer thickness for RuO_2/Pt hybrid electrodes that yielded PZT capacitors with negligible fatigue (Fig. 1.1a) and low leakage (Fig. 1.1b). These results indicated that template layers such as PT contribute to eliminate the formation of undesirable second non-ferroelectric phases and/or charged defects (e.g., oxygen vacancies), which played a role in the fatigue process. The beneficial effects

of the PT layer(s) were enhanced by the hybrid metal-RuO_2 bottom electrode, although there was still a small decrease ($\leq$7 %) in remanent polarization after ~10^{10} switching cycles. These studies suggested that not only the electrode material but also the structure of the PZT/electrode interface played roles in the fatigue process in PZT-based capacitors. Another issue revealed by the SIBMT studies is that ion beam sputter deposition resulted in damage at the electrode/ferroelectric layers interface, due to scattered ions from the target impacting on the films [39]. This hypothesis was confirmed by the fact that pulsed laser ablation deposition and MOCVD synthesis of PZT/oxide capacitors showed practically no fatigue. In addition, measurements of DC leakage currents for PZT capacitors with various combinations of RuO_2, hybrid Pt/RuO_2, and co-deposited Pt/RuO_2 electrodes revealed that the bottom electrode layer plays a critical role in controlling leakage currents, through the control of the ferroelectric layer composition and microstructure, and control of oxygen vacancies at the electrode/PZT interface.

1.2.2.2 SIBMT-Based Studies to Understand Processing–Microstructure–Property Relationships of Ferroelectric SBT Thin Films and Heterostructures

The IBSD method was also used to investigate the synthesis of SBT films on various substrates, particularly in relation to understanding the initial stages of SBT growth by physical vapor deposition. For example, Im/Auciello et al. studied the initial growth of SBT films on various electrode structures such as Pt/Ti/SiO_2/Si, Pt/TiO_2/SiO_2/Si, Pt/Ta/SiO_2/Si, Ir/SiO_2/Si, and RuO_2/SiO_2/Si [40]. These experiments were carried out at 700 °C under P (O_2) = $5 \times 10-^4$Torr, since these are suitable parameters to synthesize SBT films via ion beam sputter deposition. These studies were performed using a unique time-of-flight mass spectroscopy of recoil ions (MSRI) technique developed by Krauss and Auciello [41] suitable for performing in situ characterization of film growth processes in high-pressure environments [41]. Briefly, the Ar^+ (~10 keV of energy) ion beam is directed a grazing incidence to the surface of the growing film, such that a single Ar^+ ion impacts on a single atom on the surface of the growing film (Fig. 1.2A), which is ejected and then injected into a differentially pumped column with a high-resolution time-of-flight mass spectrometer into the spectrometer detects the atoms ejected from the growing film surface producing spectra like those shown in Fig. 1.2B(a–c), where the peaks indicate the atoms that have been detected. The MSRI technique has atomic scale resolution, as indicated below in the description of the in situ*/real-time* analysis for SBT films grown on different substrates, via ion beam sputter deposition with an atomic oxygen beam directed at the surface, during film growth, to produce the SBT films. Details of the use of IBSD for growing films with in situ*/real-time MSRI* analysis can be seen in [41].

Figure 1.2B shows the following outstanding features: (a) when SBT is deposited on a Pt/TiO_2/SiO_2/Si heterostructure bottom electrode, where no Ti or Si segregation to the surface is observed [see absence of Ti or Si peaks in the spectrum of

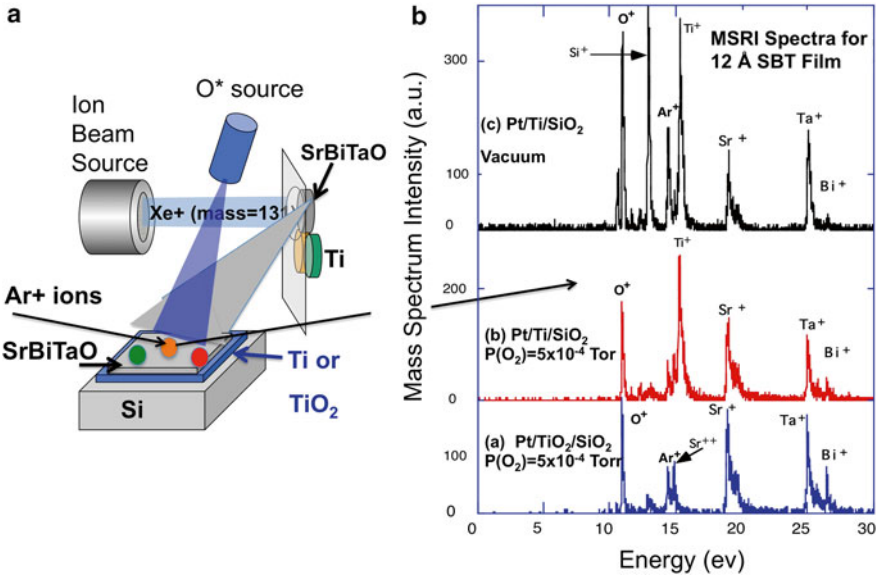

Fig. 1.2 (**A**) Schematic of the integrated ion beam sputter deposition (IBSD)/mass spectrometry of recoil ions (MSRI) used for in situ*/real-time* SBT film growth studies; (**B**) MSRI spectra, using a 10 keV Ar^+ primary ion beam probe, to characterize the initial stages of SBT film growth (at 12 Å of SBT film thickness) on $Pt/TiO_2/SiO_2/Si$, showing Bi incorporation (a), and on $Pt/Ti/SiO_2/Si$, showing no Bi incorporation, at 700 °C in oxygen [$P(O_2) = 5 \times 10^{-4}$ Torr]

Fig. 1.2B(a)], all three elements of Bi, Sr, and Ta are readily incorporated in the initial growth stages of a film deposited at 700 °C [Fig. 1.2B(a)]. On the other hand, when SBT is deposited on $Pt/Ti/SiO_2/Si$ at 700 °C, Bi is not efficiently incorporated into the SBT film while Sr and Ta are readily incorporated [Fig. 1.2B(b, c)]. A comparison of the relative intensity of the Bi peaks in all three cases reveals that the Bi concentration in the 12 Å SBT film grown on Pt/TiO_2 is more than twice the Bi concentration for SBT films grown on Pt/Ti with only Ti segregation to the surface to the Pt layer [Fig. 1.2(b)] and more than three times the Bi concentration on Pt/Ti with Ti and Si segregation [Fig.1.2(c)]. Since the peak heights of Sr and Ta are relatively similar in all three cases, it is concluded that the initial SBT films grown on Pt/Ti electrodes are Bi deficient compared to the films grown on Pt/TiO_2 electrodes. The inhibition of Bi incorporation on Pt surfaces with segregated Ti and Si species is due to the lower free energy of oxide formation for Ti and Si compared to Bi. That is, Ti and Si can thermodynamically reduce bismuth oxide to Bi at 700 °C in an oxygen environment when mixed on the surface. Because of the high vapor pressure of Bi at high temperatures, the reduced Bi readily evaporates from the surface. The in situ characterization of SBT film growth processes discussed above demonstrated that Pt/Ti is an unstable bottom electrode, while Pt/TiO_2 provides a stable electrode for vapor deposition of SBT films. These studies proved the value of understanding vapor-phase film growth processes to control film composition, microstructure, and properties for films used in the fabrication of commercial FeRAMs.

1.2.3 Pulsed Laser Ablation Synthesis and Characterization of Ferroelectric Films and Heterostructures

1.2.3.1 Processing–Microstructure–Property Relationships of PZT Films and Integration with Semiconductor Substrates

The pulsed laser ablation deposition (PLD) technique provided researchers with the capability to investigate the synthesis of multicomponent oxide thin films, including ferroelectric and associated conductive oxide layers, with controlled composition, microstructure, and properties in a rapid materials prototyping manner [17]. Studies of the PLD deposition process demonstrated that background gas pressure during deposition, substrate to target distance, laser energy and wavelength, and target-substrate relative geometric arrangement, among other parameters, had a significant effect on oxide film composition, microstructure, and properties. A systematic investigation of the ablation characteristics of PZT, LSCO, and other targets relevant to the synthesis of films for ferroelectric capacitors was performed by various groups to understand and control film deposition parameters that play fundamental roles in controlling the composition, microstructure, and properties of PZT-based capacitors for nonvolatile memories.

The power of the PLD method for the development of materials integration strategies was demonstrated by the growth of highly oriented PLZT films on SiO_2/Si substrates using a $Bi_4Ti_3O_{12}$ (BTO) template layer [36]. The presence of the thermal oxide on Si is important since it forms the basis for fabricating the pass-gate transistors in the Si-CMOS wafer. The BTO layer grew completely *c*-axis-oriented even on an amorphous layer such as SiO_2, although the film has very little crystallographic long-range correlation in the plane. Thus, the BTO layer provided a template with a perovskite structure to control the subsequent growth of the LSCO/PLZT/LSCO stack promoting the growth of the PLZT layer with [001] orientation, as illustrated by X-ray diffraction analysis [36]. The efficacy of the BTO template layer to control the orientation of the overlayer was further demonstrated by the fact that even metals, such as Pt (fcc; $a = 3.92$ Å), were grown on a BTO template with a preferred [001] orientation when deposited at the appropriate substrate temperature (400–500 °C).

PLZT-based capacitors used for the electrical tests discussed in this section were fabricated using blanket bottom electrodes and a combination of photolithographic lift-off in conjunction with either wet etching or dry ion beam milling to pattern the top electrodes to produce capacitors with 600 to 2 μm diameter (see schematic in Fig. 1.3a). Figure 1.3b shows polarization hysteresis loops for a LSCO/PZT/LSCO heterostructure grown on SiO_2/Si with the BTO template and a Pt layer underneath the LSCO, while Fig. 1.3c shows that the LSCO/PZT/LSCO/Pt capacitors exhibited fatigue-free (no reduction of polarization as a function of polarization switching cycles) polarization up to $\geq 10^{12}$ polarization switching cycles (value compatible with a commercial FeRAM). The PLZT-based capacitors with LSCO oxide electrodes, studied as described above, also exhibited negligible imprint, long polarization

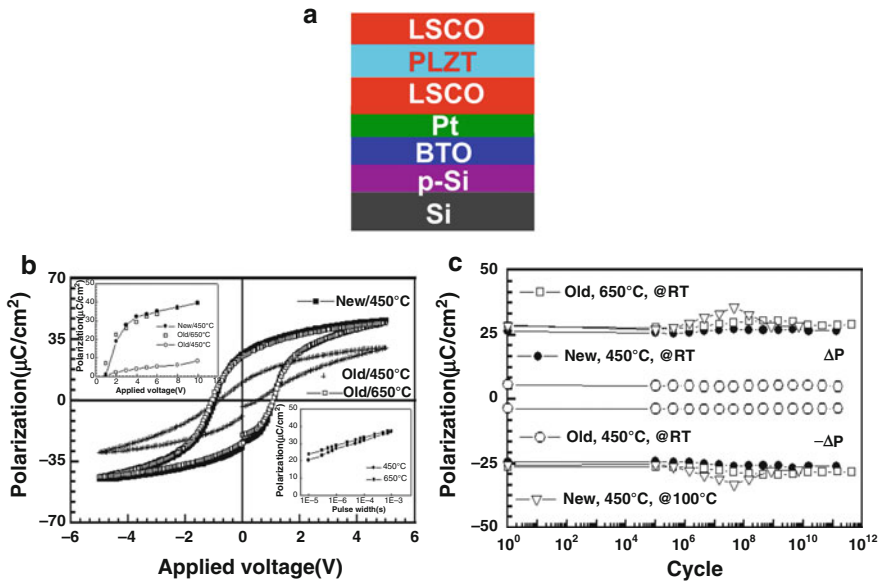

Fig. 1.3 (**a**) Schematic of a LSCO/PLZT/LSCO heterostructure capacitor grown on a p-Si substrate using a template $BTiO_3$ (BTO) layer to induce highly (001)-oriented PLZT ferroelectric film with high polarization; (**b**) pulsed hysteresis loops, and (**c**) polarization fatigue of the LSCO/PLZT/LSCO heterostructure capacitor grown on a SiO_2/Si substrate with a Pt/BTO heterostructure bottom electrode layer

retention, and low leakage, all parameters critical for the reliable performance of commercial FeRAMs.

More recently, the work on Ir [42] and Ir/IrO_x [37] electrodes and integration with PZT layers [38] provided the basis for the development and insertion in the market of low-density (≤4 Mb, 0.18 μm) node PZT-based embedded FeRAMs.

In summary, the synthesis of films for the fabrication of PZT-based capacitors using the PLD technique provided valuable information to advance other synthesis techniques, such as MOD and MOCVD, which are the film growth techniques used for an industrial process for the fabrication of PZT-based commercial FeRAMs.

1.2.3.2 Processing–Microstructure–Property Relationships of SBT Films and Integration with Semiconductor Substrates

Work on the synthesis and characterization of SBT thin films via a sol–gel process route demonstrated that the best ferroelectric properties were obtained for films that are nonstoichiometric (e.g., $Sr_{0.8}Bi_{2.2}Ta_2O_9$) [43]. Thus, studies by some groups focused on using pulsed laser deposition as a versatile rapid prototyping film growth

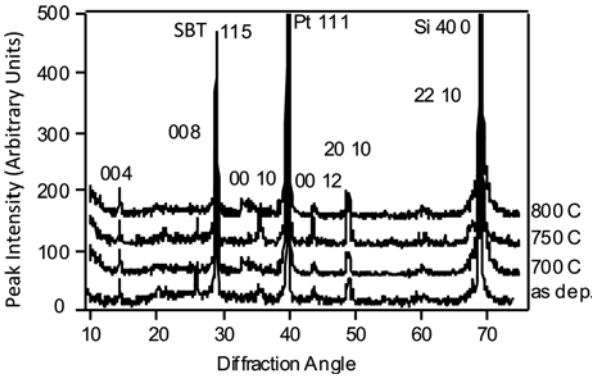

Fig. 1.4 XRD pattern for pulsed laser ablation deposition (PLD) as-deposited $SrBi_{2.1}Ta_2O_9$ and for the same films with subsequent annealing at temperatures in the range 700–800 °C

technique to understand both stoichiometry and process temperature effects on the synthesis of SBT films [44]. The work reported in [44] was focused on investigating the effect of Sr deficiency, where Sr atoms concentration was compensated by Bi atoms concentration. The ceramic targets used to grow the films were prepared according to this overall stoichiometry, with additional 5 % Bi excess to allow for Bi volatilization loss. Three different targets with controlled stoichiometry were used to grow SBT films, namely, $SrBi_{2.1}Ta_2O_9$, $Sr_{0.7}Bi_{2.3}Ta_2O_9$, and $Sr_{0.55}Bi_{2.4}Ta_2O_9$. SBT films were grown on $Pt/ZrO_2/SiO_2/Si$ substrates at 650 °C, via pulsed laser ablation deposition in 300 mTorr of oxygen. Films were annealed at 700 °C, 750 °C, and 800 °C for 1 h in oxygen at atmospheric pressure. Patterned Pt top electrodes were produced at 400 °C by ion beam sputter deposition and standard photolithography techniques followed by ion beam etching.

X-ray diffraction patterns (Fig. 1.4) for as-deposited and annealed $SrBi_{2.1}Ta_2O_9$ films revealed a broad peak between 32° and 38°, which was determined to be an artifact associated with the (200) double diffraction from the silicon substrate. These patterns reflected an increase in grain size or a decrease in inhomogeneous strain resulting from annealing, which is manifested as a narrowing of the (115) SBT peak.

SEM and EDS analysis of as-deposited SBT films with the composition range indicated above showed that as-deposited films have a fewer number of pinholes than those annealed at 800 °C. In addition, the density of pinholes decreased as the Sr/Bi ratio increased. That is, the highest concentration of pinholes was observed in the films produced by ablation of the $Sr_{0.55}Bi_{2.4}Ta_2O_9$ target. Films of this composition also contained many particles that appear to correlate with Bi-rich second phase. However, these particles were found to be bismuth deficient when compared to the film composition as measured by EDS. One possible explanation for this phenomenon is that a Bi-rich phase is formed during film deposition, but it decomposes

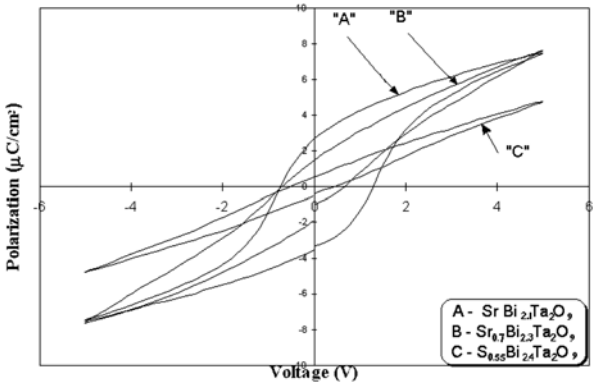

Fig. 1.5 Polarization hysteresis loops for PLD-SBT capacitors with different Sr/Bi ratio, for which the SBT films were annealed at 650 °C. All measurements were taken at 5 V on 40 × 40 μm² contacts

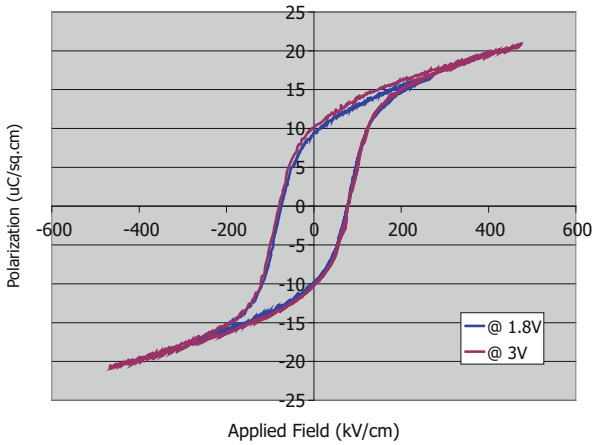

Fig. 1.6 Polarization hysteresis loops measured on a Pt/SBT/Pt capacitor with a 500 Å thick SBT layer. The remnant polarization is in the order of $2P_r \sim 20$ μC/cm²

during the post-growth annealing. Other films with compositions nominally closer to stoichiometry did not exhibit such particles even when post-annealed.

Measurement of polarization vs. electric field (Fig. 1.5) applied on a capacitor with the closest to stoichiometry SBT layer exhibited the highest remnant polarization and the best-shaped loop. However, the values of polarization observed for SBT-based capacitors produced by the PLD technique still are much lower that the highest values for SBT-based capacitors produced using MOD or MOCVD synthesis of SBT layers [45] (Compare Figs. 1.5 and 1.6).

1.2.4 Chemical Vapor Deposition and Characterization of Ferroelectric Thin Films

Of the variety of processing techniques for ferroelectric thin films, MOCVD provides the best film thickness and composition uniformity, high film densities, high deposition rates, and scalability to large wafer size for fabrication of FeRAMs. Moreover, the need for a high degree of film thickness conformality over the complex device topographies common in ULSI-scale circuits makes MOCVD the film synthesis method of choice for FeRAM fabrication. MOCVD is extensively utilized in many current commercial IC fabrication steps and manufacturers of MOCVD equipment, such as Aixtron (Germany), Applied Materials (USA), and ULVAC (Japan) supply commercial MOCVD systems for industrial production of ferroelectric thin films. Currently, a number of oxide ferroelectric thin film materials [17, 39–41, 43, 44] can now be routinely processed by MOCVD with quality similar to that of compound semiconductor films. In addition to ferroelectrics, a number of electrically conductive complex oxide thin films, critical for fabrication of PZT-based capacitors, have been successfully deposited by MOCVD (e.g., RuO_2) [46–48].

Work in the 1990s contributed to overcome processing challenges for MOCVD process of ferroelectric thin films [49, 50]. Efficient, reproducible MOCVD processes required development of precursors with sufficiently high vapor pressure to enable vapor-phase mixing of precursor components and transport of the reactants to the growing film. Adequate molecular stability of the precursor vapor was developed to prevent premature reaction or decomposition of the precursor during vapor-phase transport. These requirements spurred the development of new chemical approaches to precursor design [51, 52] and of alternative method of precursor vaporization and transport [53]. This section provides a brief overview of the synthesis of ferroelectric PZT and SBT thin films by thermal MOCVD.

1.2.4.1 Standard Precursor Delivery Techniques for MOCVD Synthesis of PZT Films

Many of the standard MOCVD systems design can be found in the appropriate literature [54, 55], so they will not be repeated here. Most systems include liquid source stainless-steel bubblers, equipped with temperature and pressure regulation, containing the organometallic precursors. The vapor-delivery-piping network is temperature regulated in order to prevent precursor vapor condensation that can lead to pipe clogging. Since the vapor pressure of most organometallic sources are nonlinear functions of both temperature and pressure, a stable precursor vapor pressure is maintained using constant source temperature and source pressure. In this case, the precursor mass transport is directly proportional to the flow rate of the inert carrier gas through the source bubbler. This type of system design is typical of an MOCVD apparatus using liquid sources. For low-vapor-pressure, solid source precursors, the traditional delivery technique of using direct sublimation of the solid

or evaporation of the melt into the carrier gas flowing through a bubbler can also be used [46–48]. For most deposition processes, the carrier gas is inert (e.g., He, N_2, Ar); however, active gases (e.g., NH_3) have occasionally been used to increase source vapor pressures [56]. For many of the organometallic precursors used in growth of electroceramic films, sufficient vapor pressures (≥0.05 Torr) are obtainable only at elevated temperatures (typically 50–250 °C) [57]. In order to prevent the condensation of precursors vapors in the delivery lines and clogging of the gas handling system, all portions of this network that transport chemical vapor must be heated to or above the evaporation temperature of the precursor. For some designs, parts of the deposition chamber will also require active heating to prevent condensation of precursors. In the case of PZT deposition using liquid sources, the source temperatures are moderate (~35–50 °C), well below the thermal decomposition temperature of these compounds (≥200 °C). Consequently, only moderate heating of the gas-handling system (~60 °C) is sufficient and a high degree of thermal uniformity is not critical.

For many material systems including electroceramic materials, thickness and compositional uniformity of the thin film improves during MOCVD when processing occurs at reduced deposition chamber pressure (i.e., ≤100 Torr). Low-pressure operation improves the flow pattern of gas through the deposition chamber by minimizing the role of heat and flow instabilities caused by temperature gradients. In addition, low-pressure operation suppresses gas-phase pre-reactions by increasing the linear velocity of the process gases through the deposition chamber, thereby reducing the residence time of the gas mixture in the chamber [58–60].

1.2.4.2 Alternative Precursor Delivery Techniques for MOCVD Synthesis of PZT Thin Films

Although many of the available precursors for electroceramic film growth have been successfully utilized to produce high quality ferroelectric films, significant deficiencies still exist with respect to the vapor pressure and vapor pressure stability of many of these compounds. This is especially true for the b-diketonate complexes of the alkaline earths (Ca, Sr, and Ba) [51, 52]. In order to obtain adequate mass transport using a conventional bubbler delivery line, the low vapor pressure of these compounds necessitates high source temperatures. At these elevated temperatures, these precursors are chemically unstable and they gradually decompose [51, 52]. Consequently, the vapor pressure of these compounds decreases as a function of time, detrimentally affecting film-growth reproducibility. In order to circumvent these problems, alternative methods of precursor delivery and vaporization have been developed.

A good alternative precursor delivery developed in recent years is known as liquid delivery or liquid source injection [61]. In this process, the low-vapor-pressure solid precursor is dissolved with an organic solvent to form a solution [61]. This delivery technique is compatible with both atmospheric- and low-pressure MOCVD

applications, and process tools of this type, incorporating up to four liquid source reservoirs, became commercially available [61, 62].

A second alternative delivery method, referred to as solid source delivery, takes advantage of the long-term instability of some of the b-diketonates at high source temperature. For short-term high-temperature exposure, the compounds have adequate chemical stability to exhibit reproducible vapor pressures characteristics. In this vaporization approach, only sufficient precursor material to sustain constant mass transport is exposed to the high thermal load required for vaporization [62]. A single solid-state precursor compound or a mixture of these compounds is fed into a high-temperature-gradient vaporization zone. Multicomponent precursor vapors are produced either by using multiple solid source delivery lines, each feeding a single precursor compound at a different metering rate, or by using a single solid source delivery line feeding a single powder containing the appropriate mixture of solid-state precursors required to produce the desired stoichiometric ratio [5]. This type of delivery line can be connected to any conventional MOCVD deposition chamber.

1.2.4.3 MOCVD Synthesis and Characterization of SBT Thin Films

As an example of the quality of ferroelectric films that can be produced by MOCVD, a discussion is presented here on efforts in the deposition of SBT thin films, considering that most mass consumption FeRAMs in "smart cards" and other RFID devices in the market today are based on SBT films.

The MOCVD deposition technique offers unique combination of composition controllability, high uniformity over large areas, high throughput, and a high degree of conformality over 3-D structures. Key elements in the successful MOCVD deposition of complex materials are the appropriate metal organic precursors and MOCVD tools. Requirement mandatory for the MOCVD growth chamber includes the capability of the reactor to precisely maintain stable process pressure, typically in the range of 0.1–10 Torr, as well as the demand for extremely uniform substrate temperature control during deposition. The precursor compounds are first vaporized and then transported to the substrate in the stream of an inert gas such as nitrogen or argon. Due to the narrow temperature window between condensation and decomposition for the precursor compounds, all boundary surfaces of the reactor and especially the showerhead must be precisely maintained at a certain temperature, typically in the range of 180–235 °C. The MOCVD deposition of SBT thin films can be carried out at temperatures as low as 350 °C using functionalized liquid alkoxide precursors such as strontium tantalum methoxy–ethoxy ethoxide and triphenyl bismuth (Kojundo chemical, Japan). Precursors are dissolved in organic solvents, toluene, and *n*-butyl acetate and dosed separately into the evaporator unit so that the film composition is precisely adjusted in order to obtain Sr deficient and Bi excess SBT films, which are known to exhibit the best electrical performance. The standard ferroelectric capacitor process flow consists of a low temperature deposition of

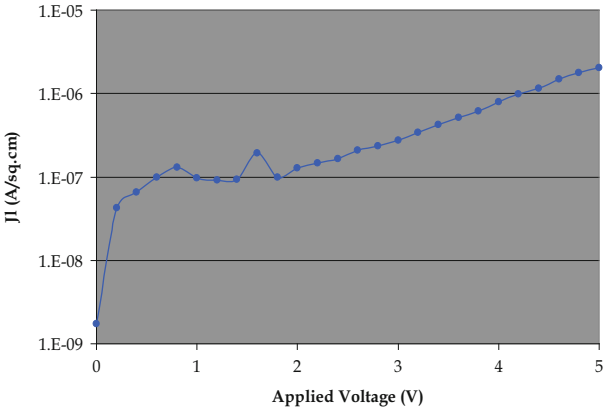

Fig. 1.7 Leakage current density of 0.1 μA/cm^2 at 1.8 V observed for a Pt/SBT/Pt capacitor with a 500 Å thick SBT layer and a remnant polarization of ~ 20 μC/cm^2 (shown in Fig. 1.6)

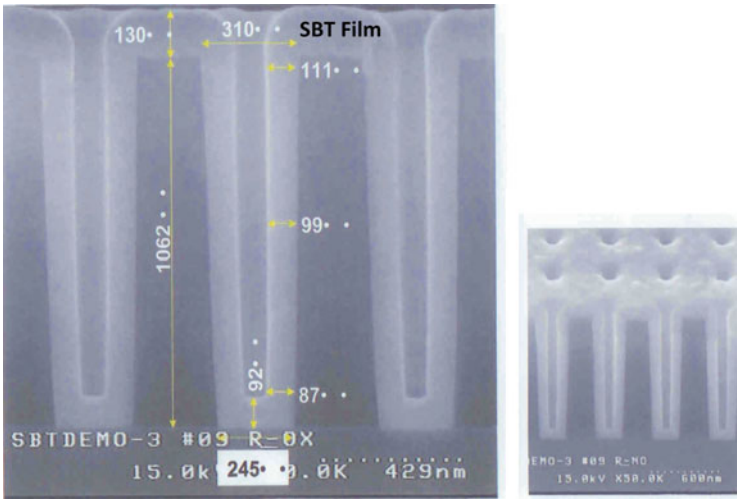

Fig. 1.8 Cross-section SEM picture of SBT film grown on high aspect ratio 3D structure for using MOCVD for future 3D nanoscale device fabrication

SBT, an electrode deposition and a subsequent recovery and crystallization annealing of the layers. Figure 1.6 illustrates the excellent ferroelectric properties of such processed films with the remnant polarization in the order of $2P_r \sim 20$ μC/cm^2 at 1.8 V (notice that 1.8 V and 3 V loops overlap) and low leakage current density of 0.1 μA/cm^2 at 1.8 V for 500 Å thin films (Fig. 1.7). Typical thickness variation on 200 mm diameter substrates is in the order of 0.5 % at 1σ.

Step coverage, another important intrinsic advantage of MOCVD deposition, is shown in Fig. 1.8, which is a cross-section SEM scan of a SBT film deposited on a 1 μm deep trench, revealing a step coverage of about 100 % for a 4:1 aspect ratio

trench. MOCVD is a mature and reliable deposition method with high degree of reproducibility mandatory for the manufacture of devices requiring a high-density memory, which goes beyond the limits of other mass production techniques, and that is why the technique is currently used for growing ferroelectric films in the manufacturing of ferroelectric memories.

1.3 Materials Integration Strategies for Low-Density FeRAMs

1.3.1 Critical PZT-Based FeRAM Materials Integration Issues

A critical issue for FeRAMs based on PZT ferroelectric films is that Pt electrodes induced polarization fatigue (loss of switchable polarization with repeated bipolar cycling) (see [16] that contains many articles addressing this important issue). Thus, in the case of the PZT-based FeRAMs it was imperative to use electrically conductive oxide electrodes, such as RuO_2 the first oxide electrode that demonstrated elimination of fatigue [19, 33, 34] and other oxide electrodes such as LSCO ([35], see Fig. 1.3). This dramatic effect of the contact electrode on the resistance to fatigue is illustrated in Fig. 1.3. This serious reliability problem in PZT ferroelectrics with Pt electrodes is the primary driver for the exploration of conducting oxide electrodes.

Epitaxial films can also be grown on Si substrates. However, the intrinsic differences in the chemistry of Si and the perovskite materials necessitate the use of buffer layers, a typical example being yttria-stabilized zirconia (YSZ). Furthermore, in order to induce heteroepitaxy in the ferroelectric capacitor, it is essential to use structural and chemical "templates" [35, 36]. For example, bismuth titanate (BTO), which is a layered perovskite (similar to YBCO), behaves as a template layer on top of (001)-oriented Si substrate.

These epitaxial heterostructures can then be used to optimize the structure of the PZT layer integrated on Si (the industrial substrate used for fabrication of FeRAMs), thus the ferroelectric properties.

1.3.2 Critical SBT-Based FeRAM Materials Integration Issues

A major advantage of the SBT film-based capacitors for FeRAMs is that Pt electrodes can be used without capacitors' fatigue, due to the fact that the bismuth oxide terminated layer for the SBT layered perovskite structure provide oxygen atoms at the SBT/Pt interface to control oxygen vacancies responsible for the polarization fatigue. In addition, because Pt has much lower resistivity (~12–15 μΩ cm) than oxide electrodes (≥80 μΩ cm) used for PZT-based capacitors, the RC time constant is much lower for SBT than for PZT-based FeRAMs, and that is why SBT-based

FeRAMs are currently used in the most commercialized FeRAMs in "smart cards" marketed by Panasonic, i.e., the SUICA (Super Urban Intelligent Card) smart card that lets people pay at vending machines, shops, public transportation, and much more in Japan.

1.4 FeRAM Fabrication Issues for Integration with the 0.35–45 nm CMOS Device Generations

In the first generation of FeRAMs, whether PZT or layered perovskite (such as SBT and SBTN)-based devices, the IC process geometry may involve thin film thickness of 60–150 nm. In the PZT devices, this meant that internal screening lengths (such as the surface extrinsic Debye length) would not interfere too severely with switching properties (L_d = 80–100 nm per surface). The introduction of impurity substitution to modify the PZT dielectric constant makes the materials more *n*-type and reduces the Debye length and the surface fields, resulting in increased endurance. Also, the use of semiconducting electrodes (such as IrO_x) moved the screening field maximum from the PZT surface onto the electrode making PZT apparently fatigue free. Such schemes are satisfactory to reduce fatigue, but optimization of the capacitor stack to reduce leakage and instability for high temperature storage is still ongoing in some PZT-oriented research programs.

Layered Perovskites such as SBT and SBTN have lower dielectric constants (better Debye lengths), and due to the layering Bi_2O_3 effect, local compensation on the surface and inter-grain decoration highly diminishes pinning fields and reduce fatigue. This local compensation lead to virtually fatigue-free behavior using standard Pt electrodes for capacitors with SBT layer thickness below 50 nm, resulting in the fabrication of FeRAM "smart cards" based on SBT capacitors. For commercialization of high-density FeRAMs, it is necessary to show that the ferroelectric film can scale below 100 nm in thickness as well as scaling down of electrode area into the nanoscale range.

A critical issue for the next generation of FeRAMs is that the process temperature of the ferroelectric thin films needs to be within the thermal budget allowed by the next generations of CMOS devices. This requirement is due to the fact that the ferroelectric capacitors for the FeRAM need to be integrated with CMOS transistors (Fig. 1.9a, b), which are the switch that applied voltage between the bottom and top electrodes to polarize the ferroelectric layer and imprint the unit of memory, while providing electrical isolation to inhibit cross-talking between memory cells. Figure 1.10a shows the allowable ferroelectric film processing temperature for the FeRAM-CMOS integration at the 0.18 μm node and Fig. 1.10b shows the schematic of the stacked cell for FeRAM-CMOS integration at the 45 nm node and the allowable processing temperature.

Another issue that needs to be addressed is the integration of robust hydrogen barriers to protect the ferroelectric capacitor-CMOS integrated FeRAM architecture

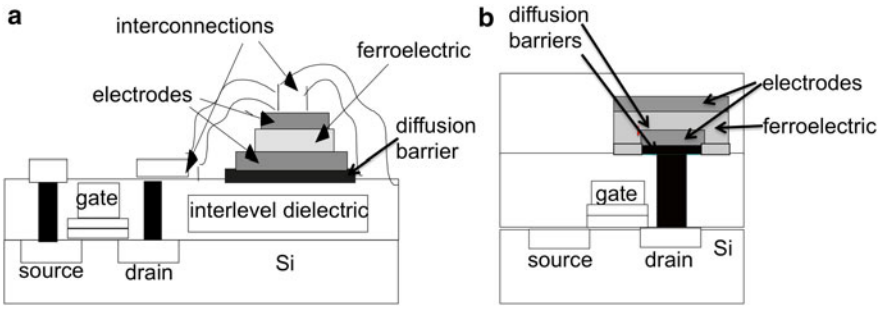

Fig. 1.9 (**a**) Schematic of low-density FeRAM structure with ferroelectric capacitor (micron size range) integrated with CMOS transistor for FeRAM cell with no cross-talking via electrical isolation provided by the CMOS transistor; (**b**) schematic of high-density FeRAM structure with ferroelectric capacitor (nanoscale size range) integrated with CMOS transistor for FeRAM cell with no cross-talking via electrical isolation provided by the CMOS transistor

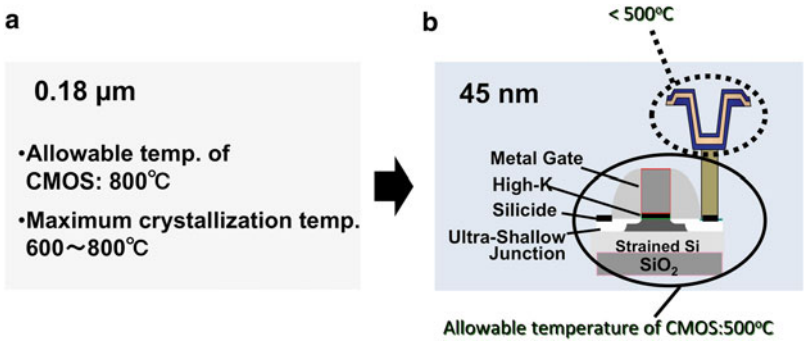

Fig. 1.10 (**a**) Allowable processing temperature of CMOS for FeRAM fabrication at the 0.18 μm node; (**b**) schematic of the stacked cell for FeRAM integrated with 48 nm node CMOS and allowable processing temperature

from interaction with hydrogen during the forming gas annealing process. Figure 1.11 shows a schematic of an integrated SBT ferroelectric capacitor-CMOS FeRAM architecture with the hydrogen barriers.

1.4.1 Stacked Cell Processing Issues

The issues for processing stacked cells in 0.35–0.13 μm and latter to 45 nm generations can be summarized as follows:

1. Use of chemical mechanical polishing (CMP) for planarization of the inter-level dielectric.
2. Use of a barrier metal to stop oxygen ions from diffusing and oxidizing the drain plug just below the ferro-capacitor bottom electrode. This creates a low dielectric

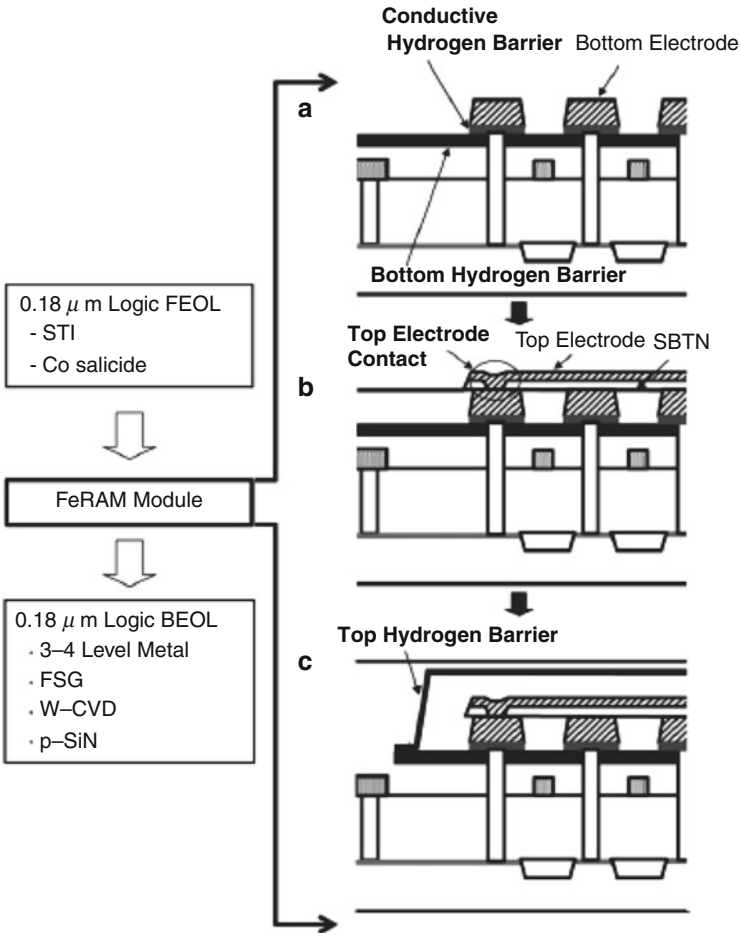

Fig. 1.11 Schematic of an integrated SBT ferroelectric capacitor-CMOS FeRAM architecture with the hydrogen barriers

constant parasitic capacitor, which can absorb most of the potential drop when voltage is applied to read or write into the ferro-capacitor.

3. Use of ferroelectric films of thickness ≤100 nm. Conformal deposition over bottom electrode is necessary.
4. Use of a ferro-capacitor capping layer to reduce H_2 degradation of the ferroelectric oxide stoichiometry (not to exceed 25 nm).
5. Use of Pt electrode to make an electrical connection with the Al interconnect buffer layer.
6. Use of low thermal budget annealing of the ferroelectric film. Temperature of 700 °C or less is preferred [RTO at 700 °C, and RTA (inert) at even low temperature]
7. Etching of the bottom electrode and the overall capacitor stack without sidewall degradation of the ferroelectric film.

The seven issues described above were properly addressed by the FeRAM community to optimize the processing to produce capacitor with the FeRAMs' compatible characteristics, i.e., (1) leakage below 1×10^{-8} A/cm^2, (2) fully saturated loops at 1.5 V away from the edge of the Q vs. V plot, (3) negligible fatigue up to $\geq 10^{12}$ polarization switching cycles (for thin films less than 100 nm and with fields as high as 250 kV/cm), (4) less than 4 % imprint at 85 °C after 10^9 unipolar disturbs (all measurements (store, stress, and probing at the opposite state) were performed at the elevated temperature), (5) $2P_r$ greater than 15 microcoulombs/cm^2 at the end of the encapsulation, (6) $\Delta(2P_r)$ during processing to be nearly zero. Deterioration of $2P_r$ shows intrinsic lack of stability of the capacitor material/electrodes, leading to imprint, fatigue, and leakage. Devices were designed wide margin sense amps to minimize these problems in low density FeRAMs, but the problem needs to be solved for advanced high-density memories where capacitors will have nanoscale dimensions. The thinner the film, the more prone to deterioration is the memory. This is particularly more stringent in 1T-1C FeRAM architectures.

Once optimized capacitor processes were achieved, device models and reliability models were used to track these parameters and provide memory designers with a design window. The models developed provided guidelines for design of memories with capacitors based on ferroelectric layers with ≤100 nm thicknesses. Layered perovskites, such as SBT, provided nano-compensation in the Bi_2O_3 layer, which counteracts oxygen vacancies in the bulk and inter-grain areas. Furthermore, Bi_2O_3 is active as a diffusion species around 650 °C, while in the case of PZT, PbO is already active around 300 °C. This is an important aspect of materials control in the ultra-thin regime needed for high-density FeRAMs. A low temperature (≤650 °C) process was developed to produce high-performance SBT films [63].

The use of stoichiometrically correct layered perovskites to obtain optimal ferroelectric capacitors with standard Pt electrodes simplifies materials control in any integration scheme. Unlike PZT, layered perovskites are not solid solution; therefore, they do not exhibit variations in ferroelectric properties within grain boundaries. The grains of layered perovskites are highly decorated with Bi_2O_3, making them nearly free of donor states (caused by traps in oxygen-deficient perovskites). In PZT, donor states are pinning sites that trap electrons creating Coulombic interactions that slowly freeze nearby domains. This process leads to fatigue and imprint, when using Pt electrodes; thus oxide electrodes were developed to eliminate fatigue by controlling oxygen vacancies at the Pt/PZT interface. In the case of fatigue, the domain is pinned. If fractional depinning occurs, charge compensation shifts the coercive field near the surface causing a temperature-dependent displacement of charge following the sense of a unipolar stressing field. Relaxation of this displaced charge occurs over a long period of time, giving the effect of imprint (in the memory array this causes checkerboard stuck bit failure or preferred state storage). This is accelerated in the dynamic imprint measurement technique. In this respect, the SBT film based capacitors are superior to PZT-based capacitors, even as demonstrated that Pt/SBT/Pt capacitors operate at temperatures up to 140 °C with negligible or no polarization fatigue (Fig. 1.12).

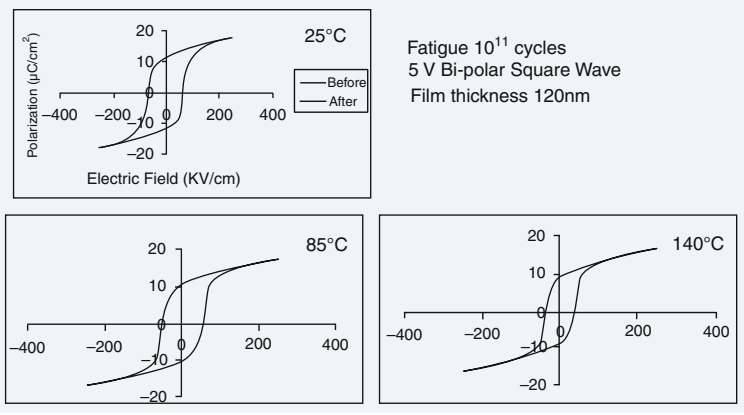

Fig. 1.12 Polarization hysteresis loops for three SBT capacitors tested for polarization fatigue at three different temperatures, showing the fatigue-free performance up to 140 °C operational temperature, a unique signature of SBT-based capacitors

1.4.2 Process Sequence Control

Once well-established thin film deposition processes were achieved, the integration issues were addressed. In the fabrication of FeRAMs, integration processes were developed to avoid or minimize degradation of the capacitor and minimize influence on CMOS device performance during the process sequence. The stack cell issues described above were the relevant areas of optimization. Device integrators worked with equipment vendors to establish modules in the CMOS process sequence that provided high degree of process integrity.

All SBT films used for capacitors discussed in this review were grown using a fourth generation cluster liquid source misted chemical deposition (LSMCD) tool built by Primaxx. Standard MOD solutions from Kojundo chemicals or Mitsubishi Materials were used for the Primaxx tool. Stoichiometric corrections for the low thermal budget were used for both SBT and SBTN. The figures shown here are only for SBT-based devices.

In relation to other processing issues discussed above for the stack cell in the 0.35 μm (and below) regime, it should be noted that item (1) is well standardized now. Item (2)-barrier metal typically involve alloys of TiN, IrO_x can also produce good results for the case of PZT-based capacitors. Item (5) is critical for extrinsic effects that may impact imprint and retention. Several theories of stress have been presented in the literature. Contact stress can be circumvented and has been done. The first order effect for a TiN/Al scheme is Ti oxidation and Ti diffusion through the Pt top electrode into the ferroelectric film. When this happens, shorting occurs. TiO_x poisoning of SBT can also occur when the Ti glue layer (in strapped cells—SiO_2/Ti/Pt bottom electrode stack) is greater in thickness than 10 % of the Pt electrode thickness. Both types of TiO_x penetration lead to shorts and poor retention.

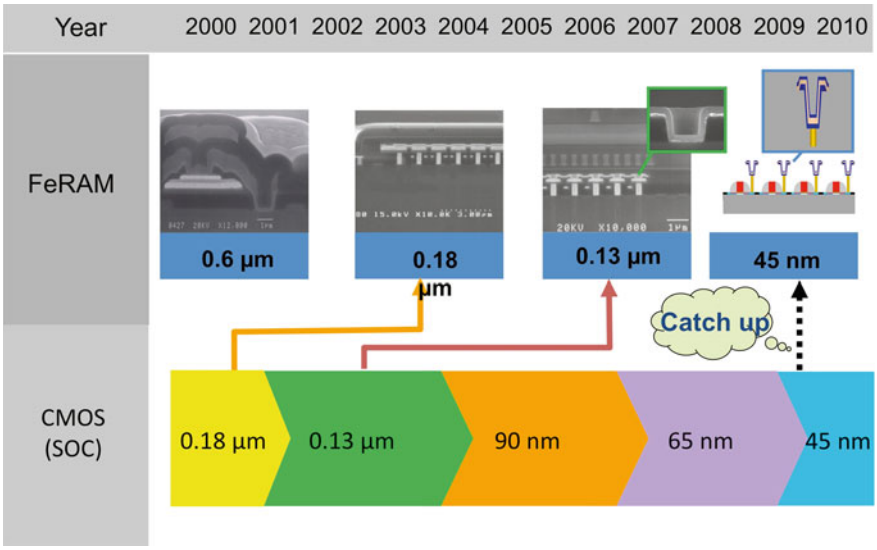

Fig. 1.13 Pathway for technology nodes for FeRAMs

However, this is completely under control in well-established process conditions, especially in ultra-thin regime.

Item (6) discussed above has been properly addressed for layered perovskites using processing temperatures as low as 650 °C. The data show that the ferroelectric properties of SBT capacitors involving 650 °C processing of the SBT layer are suitable for FeRAMs, and this is proven by the devices already introduced in the market, such as FeRAMs in "smart cards" like the Japanese SUICA card.

Further improvement of layered perovskite-based high-density 0.18–0.13-µm generation FeRAMs involves the use of MOCVD to synthesize the SBT layers. Aixtron has developed and commercializes an advanced liquid delivery system (LDS) for deposition of SBT films with FeRAM-compatible properties. Unlike conventional vaporizers, this proprietary LDS use the aerosol technique well matured in the LSMCD tool with high vapor pressure sources based on alkoxides. Aerosol misted CVD reduces carbon buildup and has lower vaporization temperatures due to large surface area to volume ratio of the aerosol vs. liquid drops used in conventional LDS. The main issue with MOCVD is cleanliness (no carbon residue), low-cost sources (alkoxides are preferred), and good 3D profiles. Because layered perovskites exhibit the best FeRAM-compatible properties when randomly oriented, they are better suited for 3D structures than PZT layers, which need *c*-axis orientation to exhibit the optimum polarization value and generally the best ferroelectric properties. The need to orient PZT layers in the lateral dimensions may further hamper the use of PZT in high-density FeRAMs that may require 3D nanostructures.

The technological pathway for FeRAMs from microscale low density memories to the nanoscale high-density memories is shown in Fig. 1.13. Materials integrations strategies will be critical to achieve the ultimate scaling to the lowest nanoscale dimensions needed for the highest density FeRAMs.

1.5 Critical Basic Physics Problems of FeRAMs: Current Understanding and Technological Implications

FeRAMs achieved a higher level of reliability once several issues such as surface polarization screening and contact interaction with defects were understood. Device physics played an important role in identifying these phenomena from a point of view of linking materials properties, proven history, and final electrical device characteristics. As already discussed above, the deposition techniques used to put the ferroelectric layer on the electrode significantly improved device performance and aided the understanding of stoichiometric variation of the oxide in the near electrode region.

In the thin film regime, the surface to bulk polarization ratio is significantly reduced as the overall thickness becomes comparable to the electrode screening length. As the polarization internal to the ferroelectric material reaches the near surface region, the outward field is cancelled by electrons supplied by electrodes. The gradient of the polarization is inversely proportional to the ferroelectric Debye length and consequently the dielectric constant. The PZT dielectric constant, being much larger than that of SBT, makes it more susceptible to restrictions in scaling as the surface space charge (polarization screening) is in the order of 50 nm vs. SBT's less than 10 nm. At the operating voltage, the space charge region can grow so large that the film can be completely depleted of free carriers needed to compensate domain distribution (polarization) in thermal equilibrium. Depleted devices still contain trapped electrons in oxygen vacancies that over time (and temperature) detrap causing a change in the polarization density and thus retention failure. As discussed in Sect. 1.2, in the case of PZT, a less conductive electrode like IrO_x afforded PZT to reduce high surface gradient of its polarization and thus reduce surface fields that are responsible for pinning domains. Ferroelectric domain pinning was observed in a transient current characteristic of PZT layers with Pt electrodes. Unsymmetrical pulses were observed with the lower current pulses showing higher negative current. This means that the integrated charge was pinned to a certain polarization level. In a hysteresis loop this appears as if the entire loop moves across the x-axis. The displaced loop results from the extra field needed to overcome the trapped charge density as described by

$$\Delta E_C = E_C(\mp)\frac{\Delta PA}{\epsilon_0 \epsilon_r}$$

where ΔE_C is a change in coercive field due to pinning, E_C is the coercive field, ΔP is the total polarization charge including non-switchable trapped charge, $\epsilon_0\epsilon_r$ is the ferroelectric dielectric constant at the coercive field, A is the area, and $(\mp)$ indicates that E_C can move on either polarity.

This effect is also known as imprint in the literature. It can be the first indication of an unstable device unsuitable for memory usage as the switching voltage cannot be assured in the memory design. This phenomenon can move the coercivity on

both sides of the *y*-axis as single polarity pulsing fix the trapped charge in one or the other near electrode region.

In the case of polarization retention, and especially retention after many cycles and over a wide range of temperatures, the usual Arrhenius curve is insufficient to describe the rate of decay of polarization. Two models, [A, B], incorporate similar physics and are described below.

Retention model:

Following Shimada's model, the decay of polarization over time is given by

$$P(t) = P_0 - m \log\left(\frac{t}{t_0}\right)$$

where $P(t)$ is the initial polarization, t_0 is the characteristic dwell time (pulse time), and m is the rate of polarization decay.

1.5.1 Microscale FeRAMs

Several critical basic physics problems related to degradation processes were addressed and solved to develop reliable commercial FeRAMs, now in the market. Several of the degradation phenomena are due to complex defect chemistry and microstructure in the perovskite ferroelectric layer and/or the ferroelectric/electrode interface. Phenomena, which were extensively studied and controlled, include all those discussed below:

(a) Polarization fatigue (decrease in switched charge with the number of polarization switching cycles) was determined to be due to pinning of domain walls and aided by electron injected through the electrode/ferroelectric interface into the ferroelectric layer and trapped in defects (most likely positively charged oxygen vacancies) [64]. Both oxygen vacancies in the bulk of the ferroelectric layer and at the electrode/ferroelectric interface appear to be contributors to fatigue.
(b) Imprint is the tendency of a ferroelectric layer to switch its polarization direction to a preferential state after being polarized in that state many times and then polarized in the opposite direction (this phenomenon is also attributed to the trapping of electrons at defects in the ferroelectric layer).
(c) Polarization retention relates to the capacity of a ferroelectric capacitor to maintain a certain level of polarization for long periods of time.
(d) Leakage current is the phenomenon whereby charges are lost from the capacitor; therefore, leakage should be minimized.

Materials integration strategies developed during the past several years resulted in the control of the capacitor degradation processes (fatigue, imprint, and leakage) described above. In the case of PZT film-based capacitors, the main strategy involved using conductive oxide electrodes or hybrid oxide-Pt electrodes [33, 34, 65], where the oxide electrode layer is in contact with the PZT film to control oxygen vacancies

and/or charge injection at the ferroelectric/electrode interface. In the case of the layered perovskite SBT, the degradation processes described above are controlled by the particular microstructure of the SBT material [66, 67], where the oxygen vacancies and/or charge injection at the ferroelectric layer/electrode (mainly Pt) interface appears to be controlled by an oxygen-rich/Bi layer. On the other hand, there is comparatively less understanding of the basic mechanism for polarization retention (or equivalently retention loss) in ferroelectric capacitors. Recent work involving nanoscale imaging of ferroelectric domains [68], using a piezoresponse atomic force microscopy technique, produced initial results which suggest that retention loss may be controlled by a random walk-type depolarization process. The exact physical basis for the retention loss is still undetermined. Work currently underway in several groups is necessary to unravel the details of the degradation mechanisms discussed above since they have important implications for ferroelectric memory technology.

1.5.2 Nanoscale FeRAMs

Nanoscale FeRAMs require very thin ferroelectric films (≤100 nm thick) and nanoscale capacitors (≤100 nm in diameter). The ferroelectric films with less than 100 nm thickness require synthesis with MOCVD and in the future ALD techniques capable of producing films with atomic scale interfaces with electrodes, which will be critical to achieve suitable polarization values for nanoscale FeRAMs. In this sense, Symetrix already demonstrated SBT films with thickness down to 50 nm, which exhibit good polarization vs. voltage curves.

1.6 Basic Unsolved Physics Problems Related to FeRAMs

1.6.1 Basic Science Issues

The field of integrated ferroelectrics continues to be driven by the potential applications of thin film ferroelectrics, such as in nonvolatile memories, DRAM storage capacitors, and infrared detectors. However, it is clear that for the long-term success of this field, the scientific underpinnings need to be well established. The science of ferroelectric materials by itself is probably quite well established. However, the transition from the microscale low density (low Mb range) to nanoscale high density (high MB range to Gb and Tb) requires to understand the synthesis of very thin films (≤50 nm), perhaps develop new ferroelectric materials with much higher polarization than present day materials, develop processes to fabricate 2D or 3D nanocapacitors (with dimensions ≤30 nm), and new nanoscale memory architectures, and understand phenomena in nanostructures. This work requires developing

new film synthesis techniques capable of producing ferroelectric films with extremely uniform composition and thickness on high aspect ratio nanostructures. For example, atomic layer deposition (ALD) may be the next method to supersede MOCVD to produce such films. Some key fundamental issues that require concerted and, in many cases, interdisciplinary effort for successful solution are discussed below.

1.6.1.1 What Are the Finite Size Effects in Ferroelectric Capacitor Properties? How Small Can a Ferroelectric Capacitor Be and Still Exhibit Ferroelectric Behavior?

NEC has reported switched polarization values for $0.7 \times 0.7 \times 0.2$ μm PZT capacitors. Mitsubishi and Symetrix have fabricated patterned 1.0 μm capacitor arrays [69]. Recently, polarization switching was measured in SBT capacitors fabricated with $0.1 \times 0.1 \times 0.05$ μm electrodes of Bi oxide. The actual ferroelectric capacitor dimensions for a 1 Gbit FeRAM must have submicron lateral area and probably contain a ferroelectric layer about 50 nm thick. The effects of constrained geometries on ferroelectric capacitors are still largely unknown. Using a combination of focused ion beam milling and electric force microscopy, Ganpule et al. have demonstrated that both PZT and SBT thin film capacitors can be scaled to at least 70 nm × 70 nm in lateral dimensions. Intensive studies are currently underway focused on investigating the physics and performance of nanoscale size devices leading to the direct exploration of fundamental size effects and possible phase transitions driven by size constraints [69]. Theoretical work [19] indicated that depolarization fields in a typical ferroelectric capacitor with semiconducting electrodes would destroy the polarization switching properties of ferroelectric layers thinner than 400 nm, while similar depolarizing fields would destroy the switching properties of ferroelectric layers only 4 nm thick when integrated with metallic electrode layers. Subsequent theories indicated that the minimum ferroelectric film thickness, which could sustain polarization switching, was about 2.5 nm [19]. However, recent experiments [24] demonstrated that polarization is achieved in $PbTiO_3$ (PTO) films of 3-unit cell layer thickness. These calculations were confirmed for PTO films in recent studies involving the use of the X-ray beam at the Advanced Photon Source (one of the two worldwide third generation X-ray synchrotron) at Argonne National Laboratory. These studies involved analyzing PTO film during and after growth using in situ X-ray scattering with atomic scale resolution [70]. The results showed that PTO films of 3-unit cells thick exhibit polarization, while films 2-unit cells thick do not exhibit polarization. Scaling of ferroelectric and dielectric properties with both thickness and lateral dimensions needs to be understood through a combination of experimental (fabrication, testing) and modeling studies. The use of sophisticated tools such as focused ion beam milling, templated growth, scanning force microscopy, and spectroscopy will be a strong focus of work in this area.

1.6.1.2 Stresses and the Role of Substrate-Film Interactions

The growth of ferroelectric thin films on substrates (which in most cases is Si) immediately places constraints, especially mechanically, which subsequently couples with the electrical and ferroelectric properties of the thin films. The magnitude of these coupling would likely depend on the coefficients in the Devonshire approximation of the free energy of the system. However, it is quite clear that the interplay between the mechanical properties of the substrate and the film can lead to suppressed polarization, dramatically decreased dielectric and piezoelectric coefficients, shifts in the phase transition temperatures, and possibly impact the polarization dynamics (switching and polarization relaxation). The interplay between substrate and film mechanical properties and its impact on electrical properties is an important area of R&D in microelectronics. A similar approach is undoubtedly required in the broad area of ferroelectric thin films, and a strong focus on this topic can be envisioned in the future, especially as devices make their way into the market and long-term reliability issues begin to dominate.

1.6.1.3 Polarization Dynamics

The role of stress impacts the polarization dynamics in thin films. The area of polarization dynamics itself is critical not only from the basic science but also from the device point of view. Indeed, it would be safe to assume that this is the most important of the fundamental topics that need a comprehensive and rigorous understanding, since this will ultimately impact the performance of ferroelectric devices. Polarization dynamics in ferroelectrics and dynamics encompasses a very broad bandwidth of timescales, from a few picoseconds for dipolar fluctuations in dielectrics such as BST to the 10-year retention time for ferroelectric memories that is impacted by the time-dependent changes in the remanent polarization. In between these two extremes, polarization switching occurs on timescales of a few nanoseconds while relaxation phenomena in relaxor ferroelectrics occur over timescales of a few seconds and longer. The interplay between thin film processing, microstructure, domain structure, and polarization dynamics is still poorly understood and will require measurements on carefully prepared and characterized test structures.

This can be illustrated through the case of retention loss in thin film ferroelectrics. Typically, the data on this topic present a log (time) dependence of the remanent polarization. However, in most cases, such a log (time) dependence is valid for a small time window. Furthermore, the log (time) function is mathematically unbounded at the extreme cases (i.e., at time = 0 and at time = infinity). Therefore, fundamental studies, including direct observations of the relaxation processes, correlation to macroscopic measurements on discrete capacitors and integrated memory cells, and the development of mathematical models to understand and predict the relaxation behavior, are required. The role of fluctuations (thermal, electrical, chemical, dipolar, etc.) and perturbations (structural, chemical electrical, etc.)

on the polarization dynamics should prove to be a fertile area of fundamental research in the future. It should be noted that there has been a considerable body of work on two other aspects of polarization dynamics in polar ferroelectrics, namely fatigue and imprint. Although these two problems were identified in the early years as "show-stoppers," it is safe to say that although there are technologically viable solutions to both these problems the fundamental understanding is far from complete.

Similarly, an important area of research for the future is the switching dynamics of nanoscale capacitors. In this case, not only is it important to understand the dynamics of the switching process beyond the Ishibashi–Avrami models, but equally important are approaches to measure the switching responses of sub-micron capacitors, especially in PZT and SBT thin films, both of which are known to switch over timescales shorter than 1 ns. Optical techniques (for example using femtosecond optical pulses to trigger and probe the switching process) will be required to obtain time-resolved information on switching.

The role of dipolar fluctuations in dielectrics such as BST and in most relaxors need to be investigated with high resolution (both spatial and temporal) probes. Novel probes such as NSOM and scanning microwave microscopy (SMWM) currently under development can potentially be useful in understanding the dipolar dynamics with high spatial resolution. A combination of microwave and optical measurements in conjunction with direct imaging of the structure (TEM, neutron diffraction, and synchrotron studies) should prove to be invaluable in providing unique insights into this complex problem.

1.6.1.4 Role of Defects

The impact of defects is one area that is possibly strongly overlooked. Although considerable amount of defect chemistry understanding is already in place for bulk ferroelectrics and dielectrics (e.g., PZT, BST) there is very little work on the characterization (by direct means) of defects in thin films. This is especially true of point defects such as oxygen vacancies and cationic defects, both of which are considered as critical in determining the properties of ferroelectrics and dielectrics. Direct determination with high spatial resolution and compositional precision of the defect chemistry in thin films still remains a paradigm. We believe that this complex problem will have to be addressed at some point in the evolution of integrated ferroelectric devices.

1.7 Future Directions

Current FeRAMs have nearly identical cell structures as the stacked cell DRAMs, which are aimed at greater than 4 Gb in density using high dielectric constant materials such as BST ($Ba_{1-x}Sr_xTiO_3$) and Ta_2O_5. This means that FeRAMs can now

enjoy all the process tools developed for DRAMs and go one step further in functionality by providing nonvolatility at low power. In the stacked cell configuration, a high-quality SBT thin film needs to be deposited with good step coverage, which can be obtained by MOCVD or LSMCD. Another interesting point is that SBT is a tantalate, which is compatible with silicon-based CMOSs, while strontium and bismuth have not proven to be deleterious to silicon.

Advanced MOSFETs for logic and other general uses are also adding Ta_2O_5 layers in the gate stack. This material change is required because the ever-thinning oxide demands of CMOSs, which recently has been found to be very difficult to be satisfied by simply reducing the SiO_2 thickness, due to the fundamental physical limit of SiO_2 as an insulator. The FLASH cell is being transformed by adding a ferroelectric switching gate in place of programming by tunneling. This evolution changes the scaling rules for FLASH radically and allows significant improvements such as writing speed, which could be equal to that of DRAMs.

As mentioned above, use of layered perovskites such as SBT with film thickness $\leq$100 nm yields FERAMs write voltage of about 1 V. As the polarization is screened near the surface, the dielectric constant of the film controls the screening length. In the case of SBT, the screening length is below 20 nm, which allows the use of thinner SBT film while retaining good electrical characteristics. Writing speeds $\leq$6 ns can be achieved at the capacitor level, even for capacitors with thick SBT films ($\geq$180 nm) and large areas. For these devices, the speed is limited by the CMOSs, not by the intrinsic characteristics of the SBT layer. FERAMs are the only fast write nonvolatile memories existing today. This characteristic and the nearly fatigue-free behavior with low power make FERAMs the mature evolution of CMOS in the nonvolatile memory area.

Currently, and in the foreseeable future, FERAMs have the potential of impacting three major markets in the \$150B dollar range. First, as stand-alone memories, FERAMs will be in direct competition with FLASH, EEPROMs, DRAMs, and SRAMs based on cost and density. However, in many cases, density and even cost may not be as important as high-speed write and nonvolatility. In the second market, FERAMs are already enjoying a great position in cost and functionality. This is the case of contactless smart cards and other RFID devices. In this case, the fast write speed and low power allows the use of smart cards or tags in a variety of applications such as ticketing, fare collections, and inventory control. Finally, where the logic unit is a microcontroller or DSP (digital signal processor), FeRAMs already has shown interesting "system-on-chip" capabilities without the added complications of power transistors such as in EEPROMs and FLASH. Also, smart cards with embedded microcontroller have demonstrated that NVFRAMs are poised to enter this market.

In summary, FeRAMs, circa 2000, have entered commercialization as stand-alone memories (in low and medium densities), contactless cards and tags, and in embedded microcontrollers. These are also among the fastest growing segments of the semiconductor industry. Adding to this the prospect of BST in DRAMs, ferroelectrics have entered the semiconductor device world in almost every market segment.

1.8 Conclusions

In conclusion, the science and technology of nonvolatile ferroelectric memories have experienced remarkable progress in the last 11 years, which resulted in the introduction into the market of the first products of mass consumption based on FeRAMs. The materials integration and fabrication strategies, in addition to device architectures, developed in this period are suitable for the fabrication of low-density FeRAMs, where the capacitors are located outside the CMOS transistor areas. However, the next generation of high-density FeRAMs requires nanoscale capacitors with 3D architectures. In addition, further work is necessary to clarify and or solve basic science issues related to ferroelectricity, particularly at the nanoscale. Given the remarkable progress in the science and technology of ferroelectric thin films during the last 10 years, it is expected that even more exciting times are ahead for the field of integrated ferroelectrics.

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