

Seungbum Hong · Orlando Auciello  
Dirk Wouters *Editors*

# Emerging Non-Volatile Memories

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# Preface

## Memory Technology Evolution and Need for New Memory Concepts

The extraordinary progress of silicon technology during the past 50+ years has also boosted silicon-based memories as SRAM, DRAM, and more recently Flash, to the current multi-gigabit densities available on a single chip at an ever decreasing cost per bit.

With the advent of multimedia applications, especially the demand for nonvolatile data storage has been growing strongly. Solid-state nonvolatile memories offer here a clear advantage both from the point of view of small form factor as of energy efficiency (low power), especially for mobile and portable systems. This trend, combined with the continuing scaling of Flash memories and associated lower bit cost, results in a continuous insertion of solid-state nonvolatile memory chips in what used to be hard disk-dominated markets.

However, there are a number of issues. First, the scaling pace is coming to a halt. This is most obvious for SRAM and DRAM memories, but also for Flash memories, and can be largely attributed to the fact that these memories are charge based. Therefore, there is a strong interest in the research for alternative memory concepts based on other mechanisms that would allow a further scaling. Second, there is a need for higher performance nonvolatile memories than those currently in the market. On the one hand, new applications of existing memory concepts, as for example Flash memory, used for solid-state disks, is hampered by its limited reliability and scalability to the ultimate nanoscale level. On the other hand, high performance nonvolatile memories could replace other volatile memories for specific application such as microcontrollers, which require embedded nonvolatile memories.

The information presented above explains why, during the past two decades, scientists and engineers started to investigate a number of alternative memory concepts. Interestingly, many of these concepts have a long history, and a number of them initially were conceived and investigated already time before the development of the Si-based memories. Recent material developments, particularly complex

oxides, in thin film form, are providing a new paradigm in materials for the next generation of nonvolatile memories with a great potential for replacing silicon-based memories. In fact, in this respect, ferroelectric random access nonvolatile memories (FeRAMS) have been introduced into the market about ten years ago, particularly in “smart cards,” which currently are reaching the one billion products mark from companies like Matsushita-Panasonic with the Suica card.

## **Outline of This Book**

The various chapters of this book are focused on discussing the science and technology of different main candidates for new emerging memory technologies, namely, ferroelectric memories (Chap. 1), magnetic memories (Chap. 2), multiferroic memories (combining both ferroelectric and magnetic properties) (Chap. 3), phase-change memories (Chap. 4), oxide resistance change memories (Chaps. 5 and 6), and finally probe memories (Chap. 7).

Research on these different material systems, however, also pointed out their potential not only for memories but also for making new devices that could be used for switching and logic applications. For example, Chap. 1 focuses on a discussion of multiferroic devices; Chap. 2 describes the science and technology not only for magnetic memories but also for spintronic-based devices and the possibility of hybrid “magnetic” electronics; and Chap. 6 discusses the oxide resistance change memory research, which resulted in the establishment of the memristor device and in more general reconfigurable electronic devices with useful properties for switching, memory, and logic.

The different memory technologies as discussed in this book are all in different stages of development. Some are already in the market, though in niche applications and larger technologies. Others are in advanced development in further scaled technologies. Still, others are in the exploration phase. The different chapters in this book aim to give insight into the principles, critical issues, and material-related properties of these different emerging concepts and may be a guideline to the reader interested to assess their potential for memory (or even beyond memory) application.

### ***Chapter 1: Ferroelectric Nonvolatile Memories (FeRAM)***

Thin-film ferroelectrics were widely investigated for ferroelectric nonvolatile memories (FeRAMs) in the early 1990s. While having excellent operational and reliability characterization, limitations in film deposition technology (precluding the possibility to go to 3D) at that time limited FeRAMs to smaller density memories. Hence Chap. 1 deals with progress in the synthesis and characterization of thin films and the materials integration strategies. Furthermore an overview of the current understanding of the critical basis physical problems is given.

## ***Chapter 2: Magnetic Nonvolatile Memories (MRAM)***

This chapter gives first an introduction into the spintronics phenomena of GMR, tunnel magnetoresistance, and spin-transfer. It then discusses the first-generation MRAM, based on field-induced magnetization, and then covers extensively the spin transfer torque (STT) MRAM including advanced concepts as perpendicular STT, multibit MRAM, and three-terminal MRAM devices. It then discusses beyond RAM applications and integrated CMOS/magnetic electronics, as well as design and modeling tools for general spintronics applications.

## ***Chapter 3: Multiferroic Memories***

This chapter starts with explaining the principle of magnetoelectricity in multiferroics and discussing single-phase multiferroic materials (e.g., BiFeO<sub>3</sub>), as well as horizontal multilayer and vertical nanostructures. It then deals with the design of multiferroic-based memories, the electric field control, and the concepts of multiferroic-based devices. Finally, challenges of multiferroic-based memories and devices are discussed.

## ***Chapter 4: Phase-Change Memories (PCRAM)***

Based on an analysis of the structure and bonding in the crystalline and amorphous phase, the material properties of phase-change materials (including their threshold switching) are discussed. The chapter goes then into the details of the phase transition including amorphization and glass physics and the process of crystallization and discusses atomistic and electrothermal modeling of the phase transition. Finally applications and outlook for optical and electronic storage are discussed.

## ***Chapter 5: Oxide Resistance Random Access Memories (OxRRAM)***

This chapter gives the basic properties and classification of memories based on resistive switching random access (RRAM). While focusing on OxRRAM based on binary oxide materials, also the solid electrolyte material systems are discussed. The 1D1R cell concept is presented including the selector switch, and possible dense cross-point arrays and 3D stacking are demonstrated. Finally the state of the art and further outlook are discussed.

### ***Chapter 6: Oxide-Based Memristive Nanodevices***

First, the switching mechanisms of memristive nanodevices based on oxide materials and how they can be used to build a whole family of new reconfigurable electronic devices with useful properties for switching, memory, and logic are explained. It then describes in more detail on the electroforming mechanism, which is the most crucial step in the operation of these devices. It is demonstrated how understanding of this mechanism enables device engineering, resulting in electroforming-free bilayer oxide devices.

### ***Chapter 7: Ferroelectric Probe Storage Devices***

Different from the new emerging memories described in the previous chapters, which consist of nonmoving solid-state memories that are fully controlled by electrical signals in the memory element array, in probe storage devices the memory elements array is purely passive and programmed/read through a (parallel array of) moveable probe(s). In that sense, their operation is more akin to that of a hard disk drive (HDD), although probe memories are typically based on different, nonmagnetic physical effects. In this chapter, the operation mechanism and the history of probe storage devices with special emphasis on ferroelectric materials are reviewed.

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**Part I**  
**Ferroic Memories**

# Chapter 1

## Review of the Science and Technology for Low- and High-Density Nonvolatile Ferroelectric Memories

Orlando Auciello, Carlos A. Paz de Araujo, and Jolanta Celinska

### 1.1 Introduction

The new millennium has witnessed the coming to age of one of the major fields of research of the twentieth century, i.e., the field of ferroelectrics. Major advances occurred in the last two decades in research related to the science and technology of ferroelectric (high permittivity) and related metallic and metal-oxide thin films and their integration into layered heterostructures for application to the development of nonvolatile ferroelectric memories (FeRAMs). The high dielectric permittivities of perovskite-type materials can be advantageously used in dynamic random access memories (DRAM) [1], while the large values of switchable remanent polarization of ferroelectric materials are suitable for nonvolatile ferroelectric random access memories (FeRAM) [2–16]. The research performed during the last two decades focused on developing both the scientific and technological bases of ferroelectric films and layered heterostructures and their integration into ever evolving device architectures and the development of new device architectures for high-performance FeRAMs [1–10, 14–17].

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The research on materials and materials integration strategies triggered by the applications to FeRAMs demonstrated that the science of the complex oxide thin films relevant to FeRAMs is also important to a wide range of applications in discrete devices, utilizing the full range of the oxide film properties, including dielectric, ferroelectric, piezoelectric, electrostrictive, pyroelectric, optical, electro-optic, and magnetic properties, as well as electronic conduction, ionic conduction, and superconduction. Applications include multilayer capacitors for memories, piezoelectric film-based microelectromechanical systems (MEMS), boundary layer capacitors, varistors, gas sensors, radiation detectors, temperature sensors, transducers, switches, shutters, MHD electrodes, fuel cell electrolytes, concentration cell electrolytes, and electrolytes for high energy density batteries. These ceramics represent an important world market, which has been experiencing steady growth in recent years [18].

The major scientific and technological advances produced in the last 11 years in the materials science and devices related to the field of ferroelectric thin films have been possible because of substantial advances in the discovery of new ferroelectric materials and development and optimization of thin film deposition techniques, as well as the development of novel materials integration strategies and device concepts. As indicated above, ferroelectric thin films play a major role in a large variety of devices. However, nonvolatile ferroelectric random access memories (FeRAMs) represent the first ferroelectric thin film-based device introduced into a mass consumption market in the form of low density memory “smart cards” [19, 20]. Therefore, this chapter is dedicated to reviewing major advances made in science and technology related to FeRAMs.

Major advances were produced in thin film deposition techniques. Various physical vapor phase deposition techniques [plasma and ion beam sputter deposition (PSD and IBSD, respectively), pulsed laser ablation deposition (PLD), electron beam or oven-induced evaporation for molecular beam epitaxy (MBE), chemical solution methods (e.g., sol-gel processing and metalorganic decomposition-MOD), liquid source misted chemical deposition (LSMCD), and metalorganic chemical deposition vapor deposition (MOCVD)] have been optimized and extensively used in the past 11 years to investigate the synthesis of ferroelectric films and layered heterostructures [5–16]. However, MOCVD is the film synthesis technique most suitable for the fabrication of high-density FeRAMs, particularly for the new concepts currently being explored for high-density memories, which may require 3D capacitor structures with high aspect ratio, thus needing conformal growth of ferroelectric films with excellent composition and thickness uniformity. An alternative CVD technique that may be even better than MOCVD for coating high aspect ratio 3D nanoscale structures required for high-density FeRAMs is atomic layer deposition (ALD), which has been demonstrated to produce extremely conformal layers on nanoscale 3D structures. However, most work until now, using the ALD film deposition technique, focused on producing metallic and amorphous oxide layers [21]. Only recently, first attempts at producing perovskite oxide crystalline layers have been attempted [22], but much work is necessary to develop ALD as a reliable technique to synthesize crystalline oxide layers. A major issue in relation to film

synthesis by any of the methods described above is the difficulty in reliably producing device-quality films directly on large semiconductor substrates, in a way that is fully compatible with existing semiconductor process technology. Issues related to deposition techniques are reviewed in this chapter in view of work performed in several laboratories worldwide.

Film synthesis techniques discussed in this review include sputter deposition, laser ablation deposition, MOCVD, and the newest ALD techniques, since the first three represent the most utilized deposition methods in relation to the science and technology of ferroelectric thin films, and ALD represents the upcoming method for producing device-quality ferroelectric thin films. All the three techniques can produce films with device-quality characteristics. However, various requirements are necessary for the application of film synthesis methods to industrial processes. A manufacturing process for producing ferroelectric thin film-based devices should at least include the following characteristics (1) applicability of the processes to deposition of ferroelectric films and integration with metallic or conductive oxide electrode layers with different physical and chemical properties, (2) compatibility with integrated device processing, including production of as-deposited films with specific microstructures (perovskite, for example) on substrates at the lowest possible temperature, (3) production of device-compatible, highly oriented, or polycrystalline films and heterostructures with specific properties (e.g., fatigue free for a large number of polarization switching cycles, long polarization retention times, and no polarization imprint effects) over large area substrates ( $\geq 200$  mm in diameter), (4) ability to produce patterned structures, superlattices, and layered heterostructures, (5) reproducibility of the deposition process, and (6) low-cost deposition processes with capacity for high deposition rates.

A major focus of research related to the development of FeRAMs has been on the development of new materials in thin film form and materials integration strategies to produce capacitors with memory-compatible properties and their integration with semiconductor devices to fabricate FeRAMs. This work has been focused until recently on  $0.18 \mu\text{m}$  feature size FeRAMs, which resulted in insertion into commercial “smart cards” and embedded memories with relatively low density. The next frontier is the development of materials, materials synthesis techniques, and materials integration and device fabrication strategies to produce the next generation of nanoscale high-density memories ( $\geq 1$  Gb). Therefore, research on this field is reviewed here as well.

A theoretical understanding of the behavior of ferroelectric thin films and device working principles has been critical to the advances achieved in the science and technology of FeRAMs, and therefore it is also briefly reviewed here.

Finally, major advances in memory concepts and implementation are critically reviewed and considered in view of future developments. Many University, National, Private, and Industrial Laboratories have made major contributions to the science and technology of ferroelectric thin films and devices. However, it is difficult to include in a limited space all the work performed by many groups around the world. Therefore, we apologize if some references have been overlooked.

## 1.2 Ferroelectric Thin Film Synthesis and Characterization

### 1.2.1 Magnetron Sputter Synthesis and Characterization of Ferroelectric Thin Films and Heterostructures

Several variations of the plasma sputter deposition technique have been developed and extensively used for the synthesis of electrode and ferroelectric layers both in the research laboratory environment and in industrial fabrication of FeRAMs. Basic phenomena occurring during the interaction of plasmas with the targets and substrates, during film synthesis, are important in that they determine to a large extent the composition, microstructure, and properties of the films.

Extensive work has been performed in recent years on plasma sputter deposition of ferroelectric thin films. Both single multicomponent oxide and multiple elemental metallic targets have been used to synthesize a wide range of ferroelectric materials in thin film form, including BaTiO<sub>3</sub> (BTO) [23], Ba<sub>x</sub>Sr<sub>1-x</sub>TiO<sub>3</sub> (BST) [24, 25], PbTiO<sub>3</sub> (PT) [26], Pb<sub>1-x</sub>La<sub>x</sub>TiO<sub>3</sub> (PLT) [27], PbZr<sub>1-x</sub>Ti<sub>x</sub>O<sub>3</sub> (PZT) [28], and Pb<sub>1-x</sub>La<sub>x</sub>(Zr<sub>y</sub>Ti<sub>1-y</sub>)O<sub>3</sub> (PLZT) [29] and SrBi<sub>2</sub>Ta<sub>2</sub>O<sub>9</sub> (SBT) [30]. Early work demonstrated that highly *c*-axis-oriented PT thin films can be produced by r.f. magnetron sputtering only when using low deposition rates (<20 Å/min), gas pressure of about  $7 \times 10^{-3}$  Torr, and PbO-rich targets [27]. These results were explained on the basis that high gas pressures in the magnetron system increase the sputtering rate because of the production of a larger amount of ions in the plasma, while simultaneously decreasing the mean kinetic energy of the sputtered species arriving at the substrate, due to collisions with the plasma species. A reduced kinetic energy of the depositing species results in a lower mobility on the substrate surface at the deposition temperature. The combination of high sputtering rate (hence high deposition rate) and low mobility of the depositing species tend to inhibit the epitaxial growth of the film. This work [27] demonstrated the importance of controlling the deposition parameters to optimize film properties for particular device applications.

Magnetron sputtering has also been used to produce PZT films with controlled stoichiometry and properties, utilizing metallic elemental targets [28]. This work revealed that the growth of stoichiometric highly oriented films via elemental target magnetron sputter deposition is governed by three main processes: (a) formation of a reproducible oxide layer on the target surface, (b) the stability of oxide species formed during transport through the plasma towards the substrate, and (c) the nucleation and growth of the film on the substrate surface. Computer simulations of the transport of sputtered species in the plasma and experimental measurements of deposition rate vs. gas pressure and film composition vs. substrate–target distance indicated that complex plasma–surface interaction and material transport processes control film composition, microstructure, and resulting electrical properties [28].

Magnetron sputter deposition was also used to synthesize layered perovskite films. The material most extensively investigated has been SBT [3], since SBT-based capacitors, using Pt electrodes, exhibit practically no fatigue, long polarization retention, low leakage, and negligible imprint, all necessary properties that

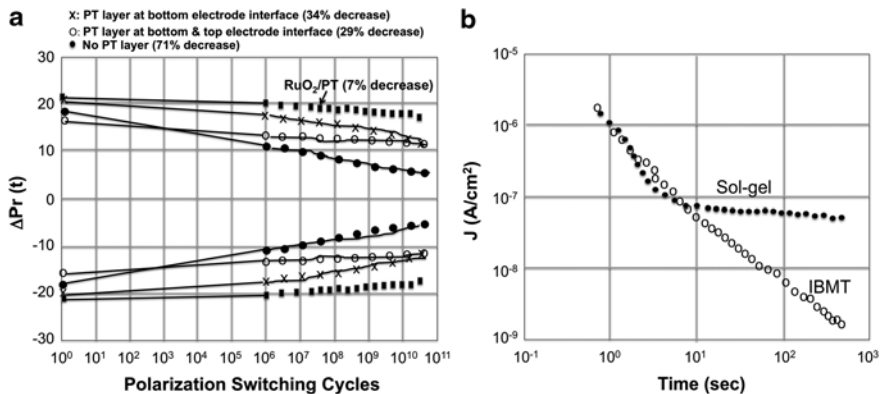
enabled SBT-based capacitors to be the basis for current commercial FeRAM “smart cards” [29]. Research by various groups [7–16, 18, 19, 23–27] demonstrated that PZT films grown on Pt/Ti electrodes on Si was not an appropriate technology for producing reliable FeRAM capacitors. Studies of film growth processes via ion beam sputter deposition in conjunction with in situ time-of-flight ion scattering and direct recoil spectroscopy provided evidence for the explanation of why the Pt/Ti electrode heterostructure did not work properly and for the solution to the problem (see ion beam sputter deposition section). Briefly, work on plasma sputter synthesis of ferroelectric thin films demonstrated that geometry and deposition conditions played key roles on the synthesis of ferroelectric thin films, using this technique. The work on magnetron sputter deposition provides valuable data from the basic science point of view mainly, since MOCVD turned out to be the most appropriate technique for industrial manufacturing of FeRAMs.

### ***1.2.2 Ion Beam Sputter Synthesis and Characterization of Ferroelectric Thin Films and Heterostructures***

Ion beam sputter deposition (IBSD) was used mainly as a versatile film-synthesis method for investigating the synthesis of ferroelectric thin films and heterostructures to understand fundamental materials synthesis and integration processes to guide the work with the synthesis methods such as MOCVD that were used in industrial processes. Multiple ion beam multi-target [30] and single ion beam/multi-target (SIBMT) [31] sputter deposition techniques were developed and extensively used to study the synthesis of ferroelectric and metallic thin films and heterostructures. The SIBMT method was specifically used to produce heterostructure capacitors with metal, conductive oxide, and hybrid metal-oxide electrodes [32] in studies focused on understanding materials integration to control polarization fatigue, retention, and imprint. Although the IBSD technique has not been used as standard industrial fabrication method, it provided valuable information that contributed to the development of materials integration strategies for the fabrication of FeRAMs, particularly for PZT and SBT-based FeRAMs, as discussed below.

#### **1.2.2.1 SIBMT-Based Studies to Understand Processing–Microstructure–Property Relationships of Ferroelectric PZT Thin Films and Heterostructures**

The main focus on the studies discussed in this section was to understand the mechanism of polarization fatigue, imprint, and polarization retention loss in PZT-based capacitors with Pt electrodes as a function of polarization switching cycles. These problems were solved for PZT-based capacitors by replacing the Pt electrode layers with metal-oxide electrodes. In this sense, the first demonstration of an oxide electrode controlling fatigue in PZT-based capacitors was produced by Auciello et al.



**Fig. 1.1** (a) Change in remanent polarization vs. number of switching cycles (fatigue) of PZT-based capacitors with and without template PbTiO<sub>3</sub> (PT) layers at the bottom Pt electrode interface only [33] and of PZT capacitor with RuO<sub>2</sub>/Pt electrodes on PT/PZT [34]. (b) Leakage current vs. time for leakage current of a RuO<sub>2</sub>/PZT/Pt/RuO<sub>2</sub>/MgO heterostructure capacitor produced with ion beam multi-target (IBMT) sputter deposition technique and a RuO<sub>2</sub>/PZT/RuO<sub>2</sub>/MgO capacitor produced with a sol-gel method [33]

using RuO<sub>2</sub> as the electrodes sandwiching a PZT ferroelectric layer [32]. The pioneering work on RuO<sub>2</sub> for PZT-based capacitors was subsequently confirmed by work performed by several groups using other electrically conductive oxide electrodes (e.g., RuO<sub>2</sub> [33], hybrid Pt/RuO<sub>2</sub> [34], La<sub>0.5</sub>Sr<sub>0.5</sub>CoO<sub>3</sub> (LSCO) [35], and hybrid Pt/LSCO [36]. More recently, IrO<sub>x</sub> [37] and hybrid Ir/IrO<sub>x</sub> [38] electrodes were developed to produce fatigue-free PZT capacitors, and these electrodes are being used in embedded FeRAMs, currently in commercial microcontroller systems [38]. The work performed by various groups also showed that electrode material and orientation and/or the PZT/electrode interface (including intermediate template layers) [33–36] were key to controlling of orientation of the ferroelectric layer and electrical properties of PZT-based heterostructure capacitors. Electrical characterization of PZT-based capacitors synthesized using a PbTiO<sub>3</sub> (PT) template layer at the bottom or top electrode/PZT interfaces revealed substantial differences in their fatigue behavior. Capacitors without the PT layer exhibited substantial fatigue (about 71 % reduction in remanent polarization), while those with one or two PT layers had substantially smaller fatigue (about 34 % and 29 % decrease, in remanent polarization, for one and two PT layers, respectively) (Fig. 1.1a) [33]. The incorporation of hybrid Pt/RuO<sub>2</sub> bottom electrode in the PZT capacitor, prior to producing the PT layer, resulted in highly oriented (001) PZT film and negligible fatigue ( $\leq 7$  % reduction in remanent polarization (Fig. 1.1a) [33, 34]). In addition, Al-Shareef/Auciello et al. demonstrated [34] that there was an optimum combination of individual layer thickness for RuO<sub>2</sub>/Pt hybrid electrodes that yielded PZT capacitors with negligible fatigue (Fig. 1.1a) and low leakage (Fig. 1.1b). These results indicated that template layers such as PT contribute to eliminate the formation of undesirable second non-ferroelectric phases and/or charged defects (e.g., oxygen vacancies), which played a role in the fatigue process. The beneficial effects

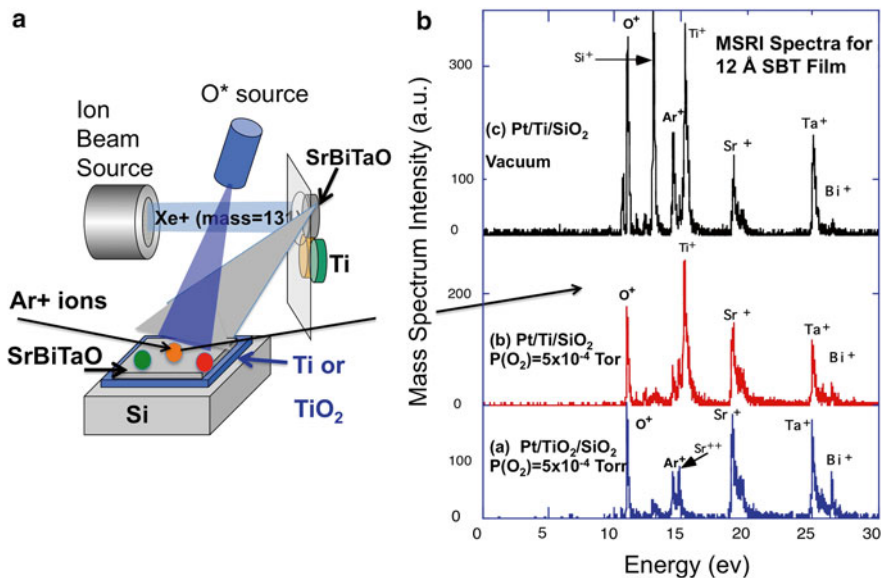


of the PT layer(s) were enhanced by the hybrid metal-RuO<sub>2</sub> bottom electrode, although there was still a small decrease ( $\leq 7\%$ ) in remanent polarization after  $\sim 10^{10}$  switching cycles. These studies suggested that not only the electrode material but also the structure of the PZT/electrode interface played roles in the fatigue process in PZT-based capacitors. Another issue revealed by the SIBMT studies is that ion beam sputter deposition resulted in damage at the electrode/ferroelectric layers interface, due to scattered ions from the target impacting on the films [39]. This hypothesis was confirmed by the fact that pulsed laser ablation deposition and MOCVD synthesis of PZT/oxide capacitors showed practically no fatigue. In addition, measurements of DC leakage currents for PZT capacitors with various combinations of RuO<sub>2</sub>, hybrid Pt/RuO<sub>2</sub>, and co-deposited Pt/RuO<sub>2</sub> electrodes revealed that the bottom electrode layer plays a critical role in controlling leakage currents, through the control of the ferroelectric layer composition and microstructure, and control of oxygen vacancies at the electrode/PZT interface.

#### 1.2.2.2 SIBMT-Based Studies to Understand Processing–Microstructure–Property Relationships of Ferroelectric SBT Thin Films and Heterostructures

The IBSD method was also used to investigate the synthesis of SBT films on various substrates, particularly in relation to understanding the initial stages of SBT growth by physical vapor deposition. For example, Im/Auciello et al. studied the initial growth of SBT films on various electrode structures such as Pt/Ti/SiO<sub>2</sub>/Si, Pt/TiO<sub>2</sub>/SiO<sub>2</sub>/Si, Pt/Ta/SiO<sub>2</sub>/Si, Ir/SiO<sub>2</sub>/Si, and RuO<sub>2</sub>/SiO<sub>2</sub>/Si [40]. These experiments were carried out at 700 °C under  $P(O_2) = 5 \times 10^{-4}$  Torr, since these are suitable parameters to synthesize SBT films via ion beam sputter deposition. These studies were performed using a unique time-of-flight mass spectroscopy of recoil ions (MSRI) technique developed by Krauss and Auciello [41] suitable for performing in situ characterization of film growth processes in high-pressure environments [41]. Briefly, the Ar<sup>+</sup> ( $\sim 10$  keV of energy) ion beam is directed a grazing incidence to the surface of the growing film, such that a single Ar<sup>+</sup> ion impacts on a single atom on the surface of the growing film (Fig. 1.2A), which is ejected and then injected into a differentially pumped column with a high-resolution time-of-flight mass spectrometer into the spectrometer detects the atoms ejected from the growing film surface producing spectra like those shown in Fig. 1.2B(a–c), where the peaks indicate the atoms that have been detected. The MSRI technique has atomic scale resolution, as indicated below in the description of the in situ/*real-time* analysis for SBT films grown on different substrates, via ion beam sputter deposition with an atomic oxygen beam directed at the surface, during film growth, to produce the SBT films. Details of the use of IBSD for growing films with in situ/*real-time* MSRI analysis can be seen in [41].

Figure 1.2B shows the following outstanding features: (a) when SBT is deposited on a Pt/TiO<sub>2</sub>/SiO<sub>2</sub>/Si heterostructure bottom electrode, where no Ti or Si segregation to the surface is observed [see absence of Ti or Si peaks in the spectrum of



**Fig. 1.2** (A) Schematic of the integrated ion beam sputter deposition (IBSD)/mass spectrometry of recoil ions (MSRI) used for in situ/real-time SBT film growth studies; (B) MSRI spectra, using a 10 keV Ar<sup>+</sup> primary ion beam probe, to characterize the initial stages of SBT film growth (at 12 Å of SBT film thickness) on Pt/TiO<sub>2</sub>/SiO<sub>2</sub>/Si, showing Bi incorporation (a), and on Pt/Ti/SiO<sub>2</sub>/Si, showing no Bi incorporation, at 700 °C in oxygen [P(O<sub>2</sub>) = 5 × 10<sup>-4</sup> Torr]

Fig. 1.2B(a)], all three elements of Bi, Sr, and Ta are readily incorporated in the initial growth stages of a film deposited at 700 °C [Fig. 1.2B(a)]. On the other hand, when SBT is deposited on Pt/Ti/SiO<sub>2</sub>/Si at 700 °C, Bi is not efficiently incorporated into the SBT film while Sr and Ta are readily incorporated [Fig. 1.2B(b, c)]. A comparison of the relative intensity of the Bi peaks in all three cases reveals that the Bi concentration in the 12 Å SBT film grown on Pt/TiO<sub>2</sub> is more than twice the Bi concentration for SBT films grown on Pt/Ti with only Ti segregation to the surface to the Pt layer [Fig. 1.2(b)] and more than three times the Bi concentration on Pt/Ti with Ti and Si segregation [Fig. 1.2(c)]. Since the peak heights of Sr and Ta are relatively similar in all three cases, it is concluded that the initial SBT films grown on Pt/Ti electrodes are Bi deficient compared to the films grown on Pt/TiO<sub>2</sub> electrodes. The inhibition of Bi incorporation on Pt surfaces with segregated Ti and Si species is due to the lower free energy of oxide formation for Ti and Si compared to Bi. That is, Ti and Si can thermodynamically reduce bismuth oxide to Bi at 700 °C in an oxygen environment when mixed on the surface. Because of the high vapor pressure of Bi at high temperatures, the reduced Bi readily evaporates from the surface. The in situ characterization of SBT film growth processes discussed above demonstrated that Pt/Ti is an unstable bottom electrode, while Pt/TiO<sub>2</sub> provides a stable electrode for vapor deposition of SBT films. These studies proved the value of understanding vapor-phase film growth processes to control film composition, microstructure, and properties for films used in the fabrication of commercial FeRAMs.

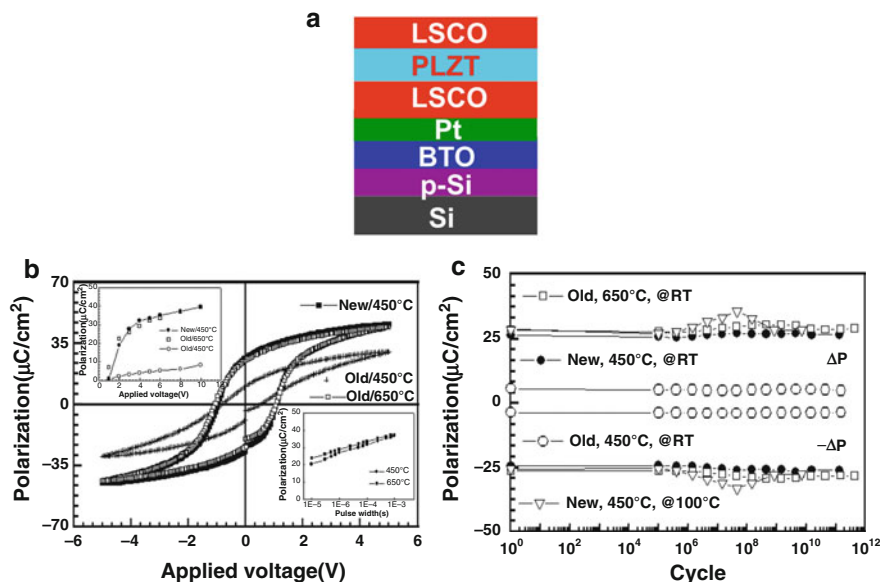
### 1.2.3 Pulsed Laser Ablation Synthesis and Characterization of Ferroelectric Films and Heterostructures

#### 1.2.3.1 Processing–Microstructure–Property Relationships of PZT Films and Integration with Semiconductor Substrates

The pulsed laser ablation deposition (PLD) technique provided researchers with the capability to investigate the synthesis of multicomponent oxide thin films, including ferroelectric and associated conductive oxide layers, with controlled composition, microstructure, and properties in a rapid materials prototyping manner [17]. Studies of the PLD deposition process demonstrated that background gas pressure during deposition, substrate to target distance, laser energy and wavelength, and target-substrate relative geometric arrangement, among other parameters, had a significant effect on oxide film composition, microstructure, and properties. A systematic investigation of the ablation characteristics of PZT, LSCO, and other targets relevant to the synthesis of films for ferroelectric capacitors was performed by various groups to understand and control film deposition parameters that play fundamental roles in controlling the composition, microstructure, and properties of PZT-based capacitors for nonvolatile memories.

The power of the PLD method for the development of materials integration strategies was demonstrated by the growth of highly oriented PLZT films on  $\text{SiO}_2/\text{Si}$  substrates using a  $\text{Bi}_4\text{Ti}_3\text{O}_{12}$  (BTO) template layer [36]. The presence of the thermal oxide on Si is important since it forms the basis for fabricating the pass-gate transistors in the Si-CMOS wafer. The BTO layer grew completely *c*-axis-oriented even on an amorphous layer such as  $\text{SiO}_2$ , although the film has very little crystallographic long-range correlation in the plane. Thus, the BTO layer provided a template with a perovskite structure to control the subsequent growth of the LSCO/PLZT/LSCO stack promoting the growth of the PLZT layer with [001] orientation, as illustrated by X-ray diffraction analysis [36]. The efficacy of the BTO template layer to control the orientation of the overlayer was further demonstrated by the fact that even metals, such as Pt (fcc;  $a = 3.92 \text{ \AA}$ ), were grown on a BTO template with a preferred [001] orientation when deposited at the appropriate substrate temperature (400–500 °C).

PLZT-based capacitors used for the electrical tests discussed in this section were fabricated using blanket bottom electrodes and a combination of photolithographic lift-off in conjunction with either wet etching or dry ion beam milling to pattern the top electrodes to produce capacitors with 600 to 2  $\mu\text{m}$  diameter (see schematic in Fig. 1.3a). Figure 1.3b shows polarization hysteresis loops for a LSCO/PZT/LSCO heterostructure grown on  $\text{SiO}_2/\text{Si}$  with the BTO template and a Pt layer underneath the LSCO, while Fig. 1.3c shows that the LSCO/PZT/LSCO/Pt capacitors exhibited fatigue-free (no reduction of polarization as a function of polarization switching cycles) polarization up to  $\geq 10^{12}$  polarization switching cycles (value compatible with a commercial FeRAM). The PLZT-based capacitors with LSCO oxide electrodes, studied as described above, also exhibited negligible imprint, long polarization



**Fig. 1.3** (a) Schematic of a LSCO/PLZT/LSCO heterostructure capacitor grown on a p-Si substrate using a template  $\text{BTiO}_3$  (BTO) layer to induce highly (001)-oriented PLZT ferroelectric film with high polarization; (b) pulsed hysteresis loops, and (c) polarization fatigue of the LSCO/PLZT/LSCO heterostructure capacitor grown on a  $\text{SiO}_2/\text{Si}$  substrate with a Pt/BTO heterostructure bottom electrode layer

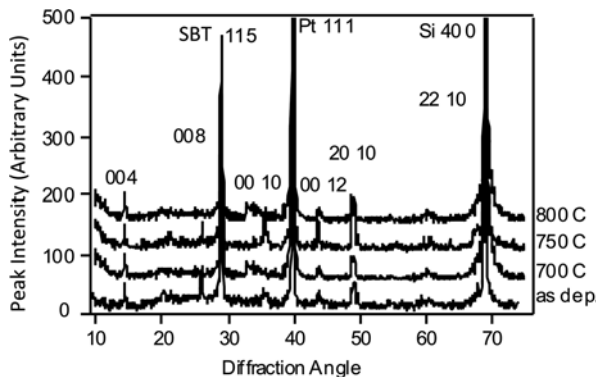
retention, and low leakage, all parameters critical for the reliable performance of commercial FeRAMs.

More recently, the work on Ir [42] and Ir/IrO<sub>x</sub> [37] electrodes and integration with PZT layers [38] provided the basis for the development and insertion in the market of low-density ( $\leq 4$  Mb,  $0.18 \mu\text{m}$ ) node PZT-based embedded FeRAMs.

In summary, the synthesis of films for the fabrication of PZT-based capacitors using the PLD technique provided valuable information to advance other synthesis techniques, such as MOD and MOCVD, which are the film growth techniques used for an industrial process for the fabrication of PZT-based commercial FeRAMs.

### 1.2.3.2 Processing–Microstructure–Property Relationships of SBT Films and Integration with Semiconductor Substrates

Work on the synthesis and characterization of SBT thin films via a sol–gel process route demonstrated that the best ferroelectric properties were obtained for films that are nonstoichiometric (e.g.,  $\text{Sr}_{0.8}\text{Bi}_{2.2}\text{Ta}_2\text{O}_9$ ) [43]. Thus, studies by some groups focused on using pulsed laser deposition as a versatile rapid prototyping film growth

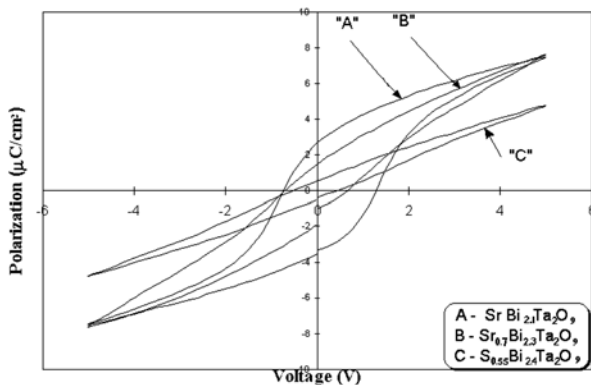


**Fig. 1.4** XRD pattern for pulsed laser ablation deposition (PLD) as-deposited SrBi<sub>2.1</sub>Ta<sub>2</sub>O<sub>9</sub>, and for the same films with subsequent annealing at temperatures in the range 700–800 °C

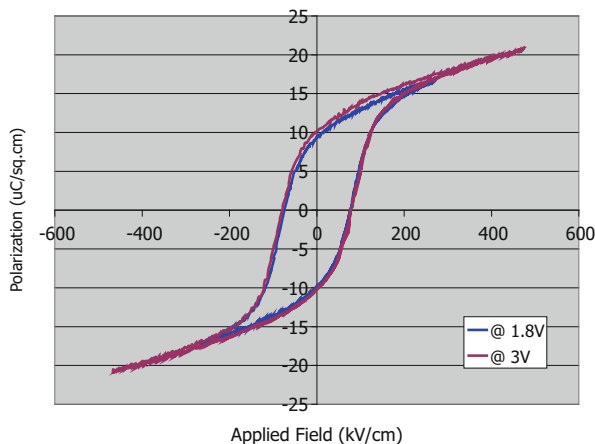
technique to understand both stoichiometry and process temperature effects on the synthesis of SBT films [44]. The work reported in [44] was focused on investigating the effect of Sr deficiency, where Sr atoms concentration was compensated by Bi atoms concentration. The ceramic targets used to grow the films were prepared according to this overall stoichiometry, with additional 5 % Bi excess to allow for Bi volatilization loss. Three different targets with controlled stoichiometry were used to grow SBT films, namely, SrBi<sub>2.1</sub>Ta<sub>2</sub>O<sub>9</sub>, Sr<sub>0.7</sub>Bi<sub>2.3</sub>Ta<sub>2</sub>O<sub>9</sub>, and Sr<sub>0.55</sub>Bi<sub>2.4</sub>Ta<sub>2</sub>O<sub>9</sub>. SBT films were grown on Pt/ZrO<sub>2</sub>/SiO<sub>2</sub>/Si substrates at 650 °C, via pulsed laser ablation deposition in 300 mTorr of oxygen. Films were annealed at 700 °C, 750 °C, and 800 °C for 1 h in oxygen at atmospheric pressure. Patterned Pt top electrodes were produced at 400 °C by ion beam sputter deposition and standard photolithography techniques followed by ion beam etching.

X-ray diffraction patterns (Fig. 1.4) for as-deposited and annealed SrBi<sub>2.1</sub>Ta<sub>2</sub>O<sub>9</sub> films revealed a broad peak between 32° and 38°, which was determined to be an artifact associated with the (200) double diffraction from the silicon substrate. These patterns reflected an increase in grain size or a decrease in inhomogeneous strain resulting from annealing, which is manifested as a narrowing of the (115) SBT peak.

SEM and EDS analysis of as-deposited SBT films with the composition range indicated above showed that as-deposited films have a fewer number of pinholes than those annealed at 800 °C. In addition, the density of pinholes decreased as the Sr/Bi ratio increased. That is, the highest concentration of pinholes was observed in the films produced by ablation of the Sr<sub>0.55</sub>Bi<sub>2.4</sub>Ta<sub>2</sub>O<sub>9</sub> target. Films of this composition also contained many particles that appear to correlate with Bi-rich second phase. However, these particles were found to be bismuth deficient when compared to the film composition as measured by EDS. One possible explanation for this phenomenon is that a Bi-rich phase is formed during film deposition, but it decomposes



**Fig. 1.5** Polarization hysteresis loops for PLD-SBT capacitors with different Sr/Bi ratio, for which the SBT films were annealed at 650 °C. All measurements were taken at 5 V on 40 × 40 μm<sup>2</sup> contacts



**Fig. 1.6** Polarization hysteresis loops measured on a Pt/SBT/Pt capacitor with a 500 Å thick SBT layer. The remnant polarization is in the order of  $2P_r \sim 20 \mu\text{C}/\text{cm}^2$

during the post-growth annealing. Other films with compositions nominally closer to stoichiometry did not exhibit such particles even when post-annealed.

Measurement of polarization vs. electric field (Fig. 1.5) applied on a capacitor with the closest to stoichiometry SBT layer exhibited the highest remnant polarization and the best-shaped loop. However, the values of polarization observed for SBT-based capacitors produced by the PLD technique still are much lower than the highest values for SBT-based capacitors produced using MOD or MOCVD synthesis of SBT layers [45] (Compare Figs. 1.5 and 1.6).

### ***1.2.4 Chemical Vapor Deposition and Characterization of Ferroelectric Thin Films***

Of the variety of processing techniques for ferroelectric thin films, MOCVD provides the best film thickness and composition uniformity, high film densities, high deposition rates, and scalability to large wafer size for fabrication of FeRAMs. Moreover, the need for a high degree of film thickness conformality over the complex device topographies common in ULSI-scale circuits makes MOCVD the film synthesis method of choice for FeRAM fabrication. MOCVD is extensively utilized in many current commercial IC fabrication steps and manufacturers of MOCVD equipment, such as Aixtron (Germany), Applied Materials (USA), and ULVAC (Japan) supply commercial MOCVD systems for industrial production of ferroelectric thin films. Currently, a number of oxide ferroelectric thin film materials [17, 39–41, 43, 44] can now be routinely processed by MOCVD with quality similar to that of compound semiconductor films. In addition to ferroelectrics, a number of electrically conductive complex oxide thin films, critical for fabrication of PZT-based capacitors, have been successfully deposited by MOCVD (e.g.,  $\text{RuO}_2$ ) [46–48].

Work in the 1990s contributed to overcome processing challenges for MOCVD process of ferroelectric thin films [49, 50]. Efficient, reproducible MOCVD processes required development of precursors with sufficiently high vapor pressure to enable vapor-phase mixing of precursor components and transport of the reactants to the growing film. Adequate molecular stability of the precursor vapor was developed to prevent premature reaction or decomposition of the precursor during vapor-phase transport. These requirements spurred the development of new chemical approaches to precursor design [51, 52] and of alternative method of precursor vaporization and transport [53]. This section provides a brief overview of the synthesis of ferroelectric PZT and SBT thin films by thermal MOCVD.

#### **1.2.4.1 Standard Precursor Delivery Techniques for MOCVD Synthesis of PZT Films**

Many of the standard MOCVD systems design can be found in the appropriate literature [54, 55], so they will not be repeated here. Most systems include liquid source stainless-steel bubblers, equipped with temperature and pressure regulation, containing the organometallic precursors. The vapor-delivery-piping network is temperature regulated in order to prevent precursor vapor condensation that can lead to pipe clogging. Since the vapor pressure of most organometallic sources are nonlinear functions of both temperature and pressure, a stable precursor vapor pressure is maintained using constant source temperature and source pressure. In this case, the precursor mass transport is directly proportional to the flow rate of the inert carrier gas through the source bubbler. This type of system design is typical of an MOCVD apparatus using liquid sources. For low-vapor-pressure, solid source precursors, the traditional delivery technique of using direct sublimation of the solid

or evaporation of the melt into the carrier gas flowing through a bubbler can also be used [46–48]. For most deposition processes, the carrier gas is inert (e.g., He, N<sub>2</sub>, Ar); however, active gases (e.g., NH<sub>3</sub>) have occasionally been used to increase source vapor pressures [56]. For many of the organometallic precursors used in growth of electroceramic films, sufficient vapor pressures ( $\geq 0.05$  Torr) are obtainable only at elevated temperatures (typically 50–250 °C) [57]. In order to prevent the condensation of precursors vapors in the delivery lines and clogging of the gas handling system, all portions of this network that transport chemical vapor must be heated to or above the evaporation temperature of the precursor. For some designs, parts of the deposition chamber will also require active heating to prevent condensation of precursors. In the case of PZT deposition using liquid sources, the source temperatures are moderate (~35–50 °C), well below the thermal decomposition temperature of these compounds ( $\geq 200$  °C). Consequently, only moderate heating of the gas-handling system (~60 °C) is sufficient and a high degree of thermal uniformity is not critical.

For many material systems including electroceramic materials, thickness and compositional uniformity of the thin film improves during MOCVD when processing occurs at reduced deposition chamber pressure (i.e.,  $\leq 100$  Torr). Low-pressure operation improves the flow pattern of gas through the deposition chamber by minimizing the role of heat and flow instabilities caused by temperature gradients. In addition, low-pressure operation suppresses gas-phase pre-reactions by increasing the linear velocity of the process gases through the deposition chamber, thereby reducing the residence time of the gas mixture in the chamber [58–60].

#### 1.2.4.2 Alternative Precursor Delivery Techniques for MOCVD Synthesis of PZT Thin Films

Although many of the available precursors for electroceramic film growth have been successfully utilized to produce high quality ferroelectric films, significant deficiencies still exist with respect to the vapor pressure and vapor pressure stability of many of these compounds. This is especially true for the b-diketonate complexes of the alkaline earths (Ca, Sr, and Ba) [51, 52]. In order to obtain adequate mass transport using a conventional bubbler delivery line, the low vapor pressure of these compounds necessitates high source temperatures. At these elevated temperatures, these precursors are chemically unstable and they gradually decompose [51, 52]. Consequently, the vapor pressure of these compounds decreases as a function of time, detrimentally affecting film-growth reproducibility. In order to circumvent these problems, alternative methods of precursor delivery and vaporization have been developed.

A good alternative precursor delivery developed in recent years is known as liquid delivery or liquid source injection [61]. In this process, the low-vapor-pressure solid precursor is dissolved with an organic solvent to form a solution [61]. This delivery technique is compatible with both atmospheric- and low-pressure MOCVD



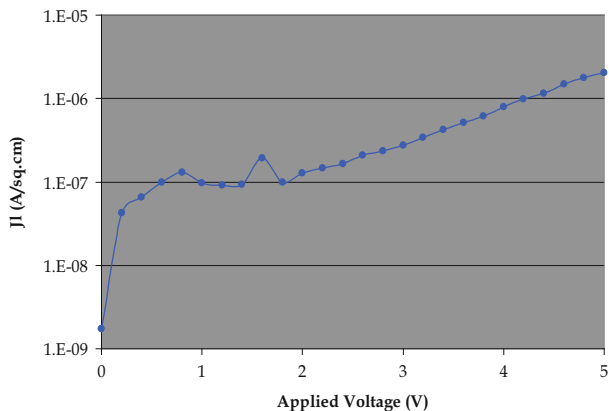
applications, and process tools of this type, incorporating up to four liquid source reservoirs, became commercially available [61, 62].

A second alternative delivery method, referred to as solid source delivery, takes advantage of the long-term instability of some of the  $\beta$ -diketonates at high source temperature. For short-term high-temperature exposure, the compounds have adequate chemical stability to exhibit reproducible vapor pressures characteristics. In this vaporization approach, only sufficient precursor material to sustain constant mass transport is exposed to the high thermal load required for vaporization [62]. A single solid-state precursor compound or a mixture of these compounds is fed into a high-temperature-gradient vaporization zone. Multicomponent precursor vapors are produced either by using multiple solid source delivery lines, each feeding a single precursor compound at a different metering rate, or by using a single solid source delivery line feeding a single powder containing the appropriate mixture of solid-state precursors required to produce the desired stoichiometric ratio [5]. This type of delivery line can be connected to any conventional MOCVD deposition chamber.

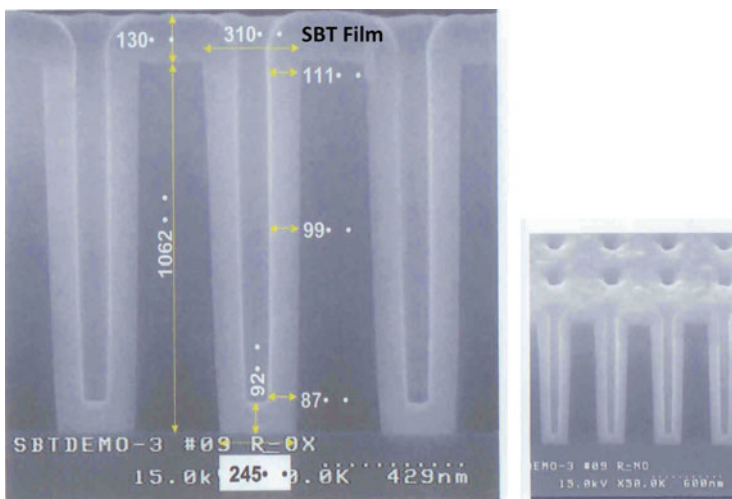
#### 1.2.4.3 MOCVD Synthesis and Characterization of SBT Thin Films

As an example of the quality of ferroelectric films that can be produced by MOCVD, a discussion is presented here on efforts in the deposition of SBT thin films, considering that most mass consumption FeRAMs in “smart cards” and other RFID devices in the market today are based on SBT films.

The MOCVD deposition technique offers unique combination of composition controllability, high uniformity over large areas, high throughput, and a high degree of conformality over 3-D structures. Key elements in the successful MOCVD deposition of complex materials are the appropriate metal organic precursors and MOCVD tools. Requirement mandatory for the MOCVD growth chamber includes the capability of the reactor to precisely maintain stable process pressure, typically in the range of 0.1–10 Torr, as well as the demand for extremely uniform substrate temperature control during deposition. The precursor compounds are first vaporized and then transported to the substrate in the stream of an inert gas such as nitrogen or argon. Due to the narrow temperature window between condensation and decomposition for the precursor compounds, all boundary surfaces of the reactor and especially the showerhead must be precisely maintained at a certain temperature, typically in the range of 180–235 °C. The MOCVD deposition of SBT thin films can be carried out at temperatures as low as 350 °C using functionalized liquid alkoxide precursors such as strontium tantalum methoxy–ethoxy ethoxide and triphenyl bismuth (Kojundo chemical, Japan). Precursors are dissolved in organic solvents, toluene, and *n*-butyl acetate and dosed separately into the evaporator unit so that the film composition is precisely adjusted in order to obtain Sr deficient and Bi excess SBT films, which are known to exhibit the best electrical performance. The standard ferroelectric capacitor process flow consists of a low temperature deposition of



**Fig. 1.7** Leakage current density of  $0.1 \mu\text{A}/\text{cm}^2$  at  $1.8 \text{ V}$  observed for a Pt/SBT/Pt capacitor with a  $500 \text{ \AA}$  thick SBT layer and a remnant polarization of  $\sim 20 \mu\text{C}/\text{cm}^2$  (shown in Fig. 1.6)



**Fig. 1.8** Cross-section SEM picture of SBT film grown on high aspect ratio 3D structure for using MOCVD for future 3D nanoscale device fabrication

SBT, an electrode deposition and a subsequent recovery and crystallization annealing of the layers. Figure 1.6 illustrates the excellent ferroelectric properties of such processed films with the remnant polarization in the order of  $2P_r \sim 20 \mu\text{C}/\text{cm}^2$  at  $1.8 \text{ V}$  (notice that  $1.8 \text{ V}$  and  $3 \text{ V}$  loops overlap) and low leakage current density of  $0.1 \mu\text{A}/\text{cm}^2$  at  $1.8 \text{ V}$  for  $500 \text{ \AA}$  thin films (Fig. 1.7). Typical thickness variation on  $200 \text{ mm}$  diameter substrates is in the order of  $0.5 \%$  at  $1\sigma$ .

Step coverage, another important intrinsic advantage of MOCVD deposition, is shown in Fig. 1.8, which is a cross-section SEM scan of a SBT film deposited on a  $1 \mu\text{m}$  deep trench, revealing a step coverage of about  $100 \%$  for a  $4:1$  aspect ratio

trench. MOCVD is a mature and reliable deposition method with high degree of reproducibility mandatory for the manufacture of devices requiring a high-density memory, which goes beyond the limits of other mass production techniques, and that is why the technique is currently used for growing ferroelectric films in the manufacturing of ferroelectric memories.

### 1.3 Materials Integration Strategies for Low-Density FeRAMs

#### 1.3.1 Critical PZT-Based FeRAM Materials Integration Issues

A critical issue for FeRAMs based on PZT ferroelectric films is that Pt electrodes induced polarization fatigue (loss of switchable polarization with repeated bipolar cycling) (see [16] that contains many articles addressing this important issue). Thus, in the case of the PZT-based FeRAMs it was imperative to use electrically conductive oxide electrodes, such as  $\text{RuO}_2$  the first oxide electrode that demonstrated elimination of fatigue [19, 33, 34] and other oxide electrodes such as LSCO ([35], see Fig. 1.3). This dramatic effect of the contact electrode on the resistance to fatigue is illustrated in Fig. 1.3. This serious reliability problem in PZT ferroelectrics with Pt electrodes is the primary driver for the exploration of conducting oxide electrodes.

Epitaxial films can also be grown on Si substrates. However, the intrinsic differences in the chemistry of Si and the perovskite materials necessitate the use of buffer layers, a typical example being yttria-stabilized zirconia (YSZ). Furthermore, in order to induce heteroepitaxy in the ferroelectric capacitor, it is essential to use structural and chemical “templates” [35, 36]. For example, bismuth titanate (BTO), which is a layered perovskite (similar to YBCO), behaves as a template layer on top of (001)-oriented Si substrate.

These epitaxial heterostructures can then be used to optimize the structure of the PZT layer integrated on Si (the industrial substrate used for fabrication of FeRAMs), thus the ferroelectric properties.

#### 1.3.2 Critical SBT-Based FeRAM Materials Integration Issues

A major advantage of the SBT film-based capacitors for FeRAMs is that Pt electrodes can be used without capacitors’ fatigue, due to the fact that the bismuth oxide terminated layer for the SBT layered perovskite structure provide oxygen atoms at the SBT/Pt interface to control oxygen vacancies responsible for the polarization fatigue. In addition, because Pt has much lower resistivity ( $\sim 12\text{--}15 \mu\Omega \text{ cm}$ ) than oxide electrodes ( $\geq 80 \mu\Omega \text{ cm}$ ) used for PZT-based capacitors, the RC time constant is much lower for SBT than for PZT-based FeRAMs, and that is why SBT-based

FeRAMs are currently used in the most commercialized FeRAMs in “smart cards” marketed by Panasonic, i.e., the SUICA (Super Urban Intelligent Card) smart card that lets people pay at vending machines, shops, public transportation, and much more in Japan.

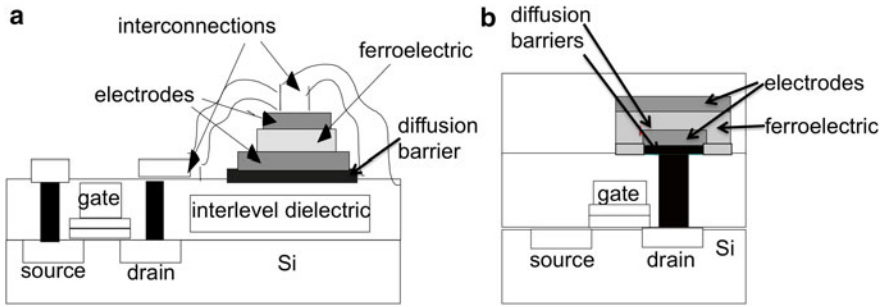
#### 1.4 FeRAM Fabrication Issues for Integration with the 0.35–45 nm CMOS Device Generations

In the first generation of FeRAMs, whether PZT or layered perovskite (such as SBT and SBTN)-based devices, the IC process geometry may involve thin film thickness of 60–150 nm. In the PZT devices, this meant that internal screening lengths (such as the surface extrinsic Debye length) would not interfere too severely with switching properties ( $L_d=80\text{--}100$  nm per surface). The introduction of impurity substitution to modify the PZT dielectric constant makes the materials more  $n$ -type and reduces the Debye length and the surface fields, resulting in increased endurance. Also, the use of semiconducting electrodes (such as  $\text{IrO}_x$ ) moved the screening field maximum from the PZT surface onto the electrode making PZT apparently fatigue free. Such schemes are satisfactory to reduce fatigue, but optimization of the capacitor stack to reduce leakage and instability for high temperature storage is still ongoing in some PZT-oriented research programs.

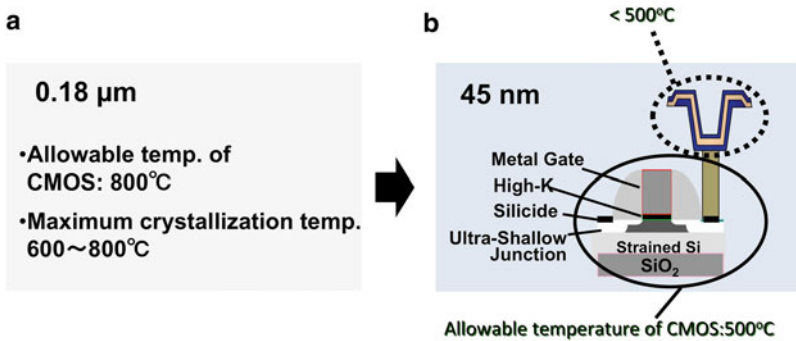
Layered Perovskites such as SBT and SBTN have lower dielectric constants (better Debye lengths), and due to the layering  $\text{Bi}_2\text{O}_3$  effect, local compensation on the surface and inter-grain decoration highly diminishes pinning fields and reduce fatigue. This local compensation lead to virtually fatigue-free behavior using standard Pt electrodes for capacitors with SBT layer thickness below 50 nm, resulting in the fabrication of FeRAM “smart cards” based on SBT capacitors. For commercialization of high-density FeRAMs, it is necessary to show that the ferroelectric film can scale below 100 nm in thickness as well as scaling down of electrode area into the nanoscale range.

A critical issue for the next generation of FeRAMs is that the process temperature of the ferroelectric thin films needs to be within the thermal budget allowed by the next generations of CMOS devices. This requirement is due to the fact that the ferroelectric capacitors for the FeRAM need to be integrated with CMOS transistors (Fig. 1.9a, b), which are the switch that applied voltage between the bottom and top electrodes to polarize the ferroelectric layer and imprint the unit of memory, while providing electrical isolation to inhibit cross-talking between memory cells. Figure 1.10a shows the allowable ferroelectric film processing temperature for the FeRAM-CMOS integration at the 0.18  $\mu\text{m}$  node and Fig. 1.10b shows the schematic of the stacked cell for FeRAM-CMOS integration at the 45 nm node and the allowable processing temperature.

Another issue that needs to be addressed is the integration of robust hydrogen barriers to protect the ferroelectric capacitor-CMOS integrated FeRAM architecture



**Fig. 1.9** (a) Schematic of low-density FeRAM structure with ferroelectric capacitor (micron size range) integrated with CMOS transistor for FeRAM cell with no cross-talking via electrical isolation provided by the CMOS transistor; (b) schematic of high-density FeRAM structure with ferroelectric capacitor (nanoscale size range) integrated with CMOS transistor for FeRAM cell with no cross-talking via electrical isolation provided by the CMOS transistor



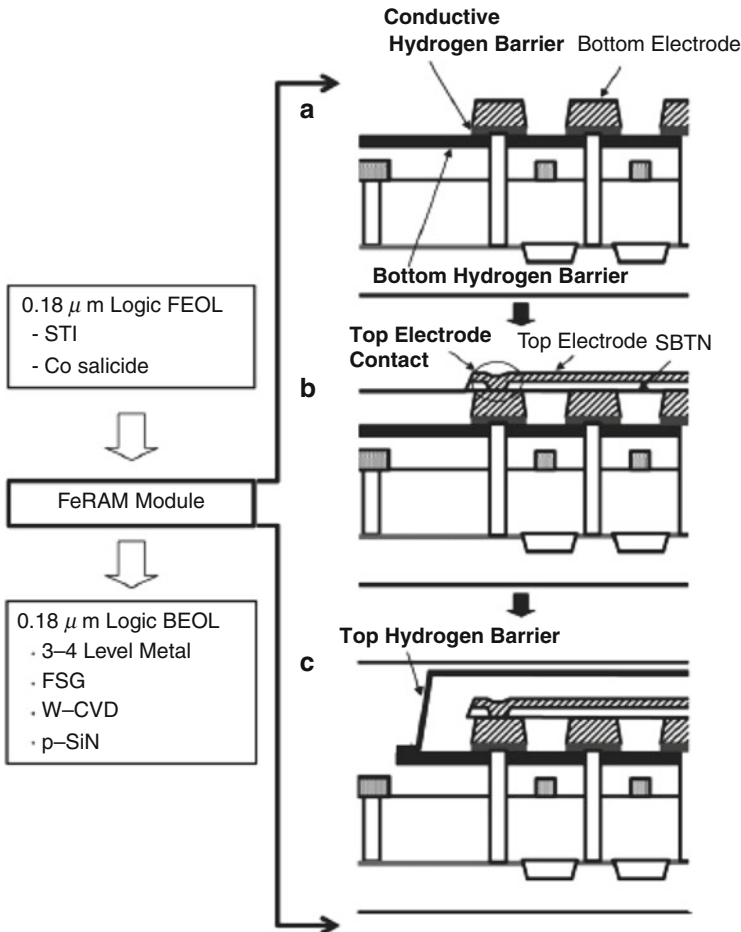
**Fig. 1.10** (a) Allowable processing temperature of CMOS for FeRAM fabrication at the 0.18 μm node; (b) schematic of the stacked cell for FeRAM integrated with 48 nm node CMOS and allowable processing temperature

from interaction with hydrogen during the forming gas annealing process. Figure 1.11 shows a schematic of an integrated SBT ferroelectric capacitor-CMOS FeRAM architecture with the hydrogen barriers.

### 1.4.1 Stacked Cell Processing Issues

The issues for processing stacked cells in 0.35–0.13 μm and latter to 45 nm generations can be summarized as follows:

1. Use of chemical mechanical polishing (CMP) for planarization of the inter-level dielectric.
2. Use of a barrier metal to stop oxygen ions from diffusing and oxidizing the drain plug just below the ferro-capacitor bottom electrode. This creates a low dielectric



**Fig. 1.11** Schematic of an integrated SBT ferroelectric capacitor-CMOS FeRAM architecture with the hydrogen barriers

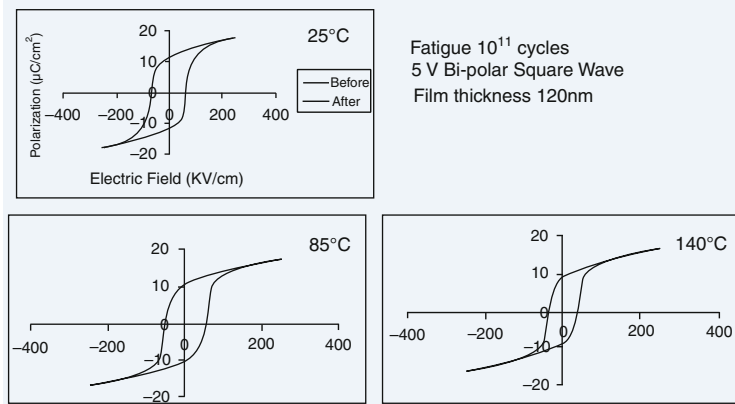
constant parasitic capacitor, which can absorb most of the potential drop when voltage is applied to read or write into the ferro-capacitor.

3. Use of ferroelectric films of thickness  $\leq 100$  nm. Conformal deposition over bottom electrode is necessary.
4. Use of a ferro-capacitor capping layer to reduce  $\text{H}_2$  degradation of the ferroelectric oxide stoichiometry (not to exceed 25 nm).
5. Use of Pt electrode to make an electrical connection with the Al interconnect buffer layer.
6. Use of low thermal budget annealing of the ferroelectric film. Temperature of  $700^\circ\text{C}$  or less is preferred [RTO at  $700^\circ\text{C}$ , and RTA (inert) at even low temperature]
7. Etching of the bottom electrode and the overall capacitor stack without sidewall degradation of the ferroelectric film.

The seven issues described above were properly addressed by the FeRAM community to optimize the processing to produce capacitor with the FeRAMs' compatible characteristics, i.e., (1) leakage below  $1 \times 10^{-8}$  A/cm<sup>2</sup>, (2) fully saturated loops at 1.5 V away from the edge of the Q vs. V plot, (3) negligible fatigue up to  $\geq 10^{12}$  polarization switching cycles (for thin films less than 100 nm and with fields as high as 250 kV/cm), (4) less than 4 % imprint at 85 °C after  $10^9$  unipolar disturbs (all measurements (store, stress, and probing at the opposite state) were performed at the elevated temperature), (5)  $2P_r$  greater than 15 microcoulombs/cm<sup>2</sup> at the end of the encapsulation, (6)  $\Delta(2P_r)$  during processing to be nearly zero. Deterioration of  $2P_r$  shows intrinsic lack of stability of the capacitor material/electrodes, leading to imprint, fatigue, and leakage. Devices were designed wide margin sense amps to minimize these problems in low density FeRAMs, but the problem needs to be solved for advanced high-density memories where capacitors will have nanoscale dimensions. The thinner the film, the more prone to deterioration is the memory. This is particularly more stringent in 1T-1C FeRAM architectures.

Once optimized capacitor processes were achieved, device models and reliability models were used to track these parameters and provide memory designers with a design window. The models developed provided guidelines for design of memories with capacitors based on ferroelectric layers with  $\leq 100$  nm thicknesses. Layered perovskites, such as SBT, provided nano-compensation in the Bi<sub>2</sub>O<sub>3</sub> layer, which counteracts oxygen vacancies in the bulk and inter-grain areas. Furthermore, Bi<sub>2</sub>O<sub>3</sub> is active as a diffusion species around 650 °C, while in the case of PZT, PbO is already active around 300 °C. This is an important aspect of materials control in the ultra-thin regime needed for high-density FeRAMs. A low temperature ( $\leq 650$  °C) process was developed to produce high-performance SBT films [63].

The use of stoichiometrically correct layered perovskites to obtain optimal ferroelectric capacitors with standard Pt electrodes simplifies materials control in any integration scheme. Unlike PZT, layered perovskites are not solid solution; therefore, they do not exhibit variations in ferroelectric properties within grain boundaries. The grains of layered perovskites are highly decorated with Bi<sub>2</sub>O<sub>3</sub>, making them nearly free of donor states (caused by traps in oxygen-deficient perovskites). In PZT, donor states are pinning sites that trap electrons creating Coulombic interactions that slowly freeze nearby domains. This process leads to fatigue and imprint, when using Pt electrodes; thus oxide electrodes were developed to eliminate fatigue by controlling oxygen vacancies at the Pt/PZT interface. In the case of fatigue, the domain is pinned. If fractional depinning occurs, charge compensation shifts the coercive field near the surface causing a temperature-dependent displacement of charge following the sense of a unipolar stressing field. Relaxation of this displaced charge occurs over a long period of time, giving the effect of imprint (in the memory array this causes checkerboard stuck bit failure or preferred state storage). This is accelerated in the dynamic imprint measurement technique. In this respect, the SBT film based capacitors are superior to PZT-based capacitors, even as demonstrated that Pt/SBT/Pt capacitors operate at temperatures up to 140 °C with negligible or no polarization fatigue (Fig. 1.12).



**Fig. 1.12** Polarization hysteresis loops for three SBT capacitors tested for polarization fatigue at three different temperatures, showing the fatigue-free performance up to 140 °C operational temperature, a unique signature of SBT-based capacitors

### 1.4.2 Process Sequence Control

Once well-established thin film deposition processes were achieved, the integration issues were addressed. In the fabrication of FeRAMs, integration processes were developed to avoid or minimize degradation of the capacitor and minimize influence on CMOS device performance during the process sequence. The stack cell issues described above were the relevant areas of optimization. Device integrators worked with equipment vendors to establish modules in the CMOS process sequence that provided high degree of process integrity.

All SBT films used for capacitors discussed in this review were grown using a fourth generation cluster liquid source misted chemical deposition (LSMCD) tool built by Primaxx. Standard MOD solutions from Kojundo chemicals or Mitsubishi Materials were used for the Primaxx tool. Stoichiometric corrections for the low thermal budget were used for both SBT and SBTN. The figures shown here are only for SBT-based devices.

In relation to other processing issues discussed above for the stack cell in the 0.35  $\mu\text{m}$  (and below) regime, it should be noted that item (1) is well standardized now. Item (2)-barrier metal typically involve alloys of TiN,  $\text{IrO}_x$  can also produce good results for the case of PZT-based capacitors. Item (5) is critical for extrinsic effects that may impact imprint and retention. Several theories of stress have been presented in the literature. Contact stress can be circumvented and has been done. The first order effect for a TiN/Al scheme is Ti oxidation and Ti diffusion through the Pt top electrode into the ferroelectric film. When this happens, shorting occurs.  $\text{TiO}_x$  poisoning of SBT can also occur when the Ti glue layer (in strapped cells— $\text{SiO}_2/\text{Ti}/\text{Pt}$  bottom electrode stack) is greater in thickness than 10 % of the Pt electrode thickness. Both types of  $\text{TiO}_x$  penetration lead to shorts and poor retention.



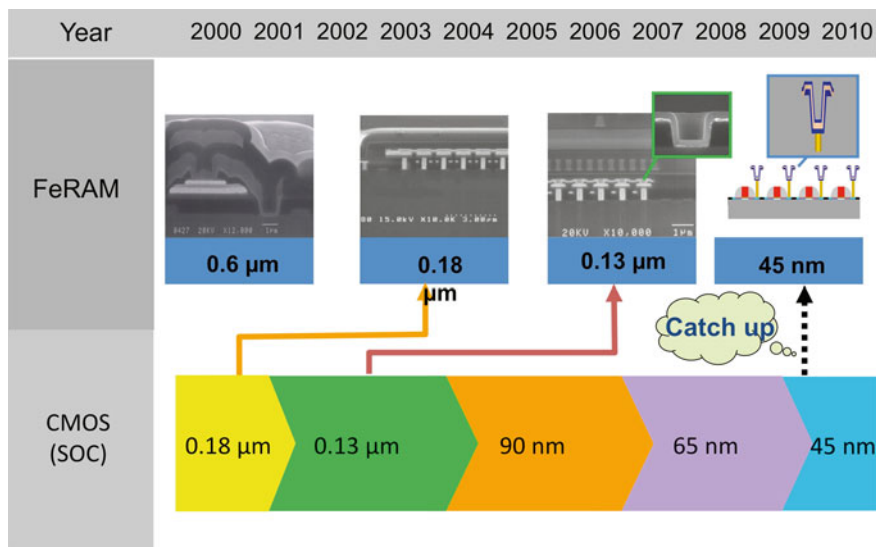


Fig. 1.13 Pathway for technology nodes for FeRAMs

However, this is completely under control in well-established process conditions, especially in ultra-thin regime.

Item (6) discussed above has been properly addressed for layered perovskites using processing temperatures as low as 650 °C. The data show that the ferroelectric properties of SBT capacitors involving 650 °C processing of the SBT layer are suitable for FeRAMs, and this is proven by the devices already introduced in the market, such as FeRAMs in “smart cards” like the Japanese SUICA card.

Further improvement of layered perovskite-based high-density 0.18–0.13-μm generation FeRAMs involves the use of MOCVD to synthesize the SBT layers. Aixtron has developed and commercializes an advanced liquid delivery system (LDS) for deposition of SBT films with FeRAM-compatible properties. Unlike conventional vaporizers, this proprietary LDS use the aerosol technique well matured in the LSMCD tool with high vapor pressure sources based on alkoxides. Aerosol misted CVD reduces carbon buildup and has lower vaporization temperatures due to large surface area to volume ratio of the aerosol vs. liquid drops used in conventional LDS. The main issue with MOCVD is cleanliness (no carbon residue), low-cost sources (alkoxides are preferred), and good 3D profiles. Because layered perovskites exhibit the best FeRAM-compatible properties when randomly oriented, they are better suited for 3D structures than PZT layers, which need *c*-axis orientation to exhibit the optimum polarization value and generally the best ferroelectric properties. The need to orient PZT layers in the lateral dimensions may further hamper the use of PZT in high-density FeRAMs that may require 3D nanostructures.

The technological pathway for FeRAMs from microscale low density memories to the nanoscale high-density memories is shown in Fig. 1.13. Materials integrations strategies will be critical to achieve the ultimate scaling to the lowest nanoscale dimensions needed for the highest density FeRAMs.

## 1.5 Critical Basic Physics Problems of FeRAMs: Current Understanding and Technological Implications

FeRAMs achieved a higher level of reliability once several issues such as surface polarization screening and contact interaction with defects were understood. Device physics played an important role in identifying these phenomena from a point of view of linking materials properties, proven history, and final electrical device characteristics. As already discussed above, the deposition techniques used to put the ferroelectric layer on the electrode significantly improved device performance and aided the understanding of stoichiometric variation of the oxide in the near electrode region.

In the thin film regime, the surface to bulk polarization ratio is significantly reduced as the overall thickness becomes comparable to the electrode screening length. As the polarization internal to the ferroelectric material reaches the near surface region, the outward field is cancelled by electrons supplied by electrodes. The gradient of the polarization is inversely proportional to the ferroelectric Debye length and consequently the dielectric constant. The PZT dielectric constant, being much larger than that of SBT, makes it more susceptible to restrictions in scaling as the surface space charge (polarization screening) is in the order of 50 nm vs. SBT's less than 10 nm. At the operating voltage, the space charge region can grow so large that the film can be completely depleted of free carriers needed to compensate domain distribution (polarization) in thermal equilibrium. Depleted devices still contain trapped electrons in oxygen vacancies that over time (and temperature) detrapp causing a change in the polarization density and thus retention failure. As discussed in Sect. 1.2, in the case of PZT, a less conductive electrode like  $\text{IrO}_x$  afforded PZT to reduce high surface gradient of its polarization and thus reduce surface fields that are responsible for pinning domains. Ferroelectric domain pinning was observed in a transient current characteristic of PZT layers with Pt electrodes. Unsymmetrical pulses were observed with the lower current pulses showing higher negative current. This means that the integrated charge was pinned to a certain polarization level. In a hysteresis loop this appears as if the entire loop moves across the  $x$ -axis. The displaced loop results from the extra field needed to overcome the trapped charge density as described by

$$\Delta E_C = E_C (\mp) \frac{\Delta P A}{\epsilon_0 \epsilon_r}$$

where  $\Delta E_C$  is a change in coercive field due to pinning,  $E_C$  is the coercive field,  $\Delta P$  is the total polarization charge including non-switchable trapped charge,  $\epsilon_0 \epsilon_r$  is the ferroelectric dielectric constant at the coercive field,  $A$  is the area, and  $(\mp)$  indicates that  $E_C$  can move on either polarity.

This effect is also known as imprint in the literature. It can be the first indication of an unstable device unsuitable for memory usage as the switching voltage cannot be assured in the memory design. This phenomenon can move the coercivity on

both sides of the y-axis as single polarity pulsing fix the trapped charge in one or the other near electrode region.

In the case of polarization retention, and especially retention after many cycles and over a wide range of temperatures, the usual Arrhenius curve is insufficient to describe the rate of decay of polarization. Two models, [A, B], incorporate similar physics and are described below.

Retention model:

Following Shimada's model, the decay of polarization over time is given by

$$P(t) = P_0 - m \log\left(\frac{t}{t_0}\right)$$

where  $P(t)$  is the initial polarization,  $t_0$  is the characteristic dwell time (pulse time), and  $m$  is the rate of polarization decay.

### 1.5.1 Microscale FeRAMs

Several critical basic physics problems related to degradation processes were addressed and solved to develop reliable commercial FeRAMs, now in the market. Several of the degradation phenomena are due to complex defect chemistry and microstructure in the perovskite ferroelectric layer and/or the ferroelectric/electrode interface. Phenomena, which were extensively studied and controlled, include all those discussed below:

- (a) Polarization fatigue (decrease in switched charge with the number of polarization switching cycles) was determined to be due to pinning of domain walls and aided by electron injected through the electrode/ferroelectric interface into the ferroelectric layer and trapped in defects (most likely positively charged oxygen vacancies) [64]. Both oxygen vacancies in the bulk of the ferroelectric layer and at the electrode/ferroelectric interface appear to be contributors to fatigue.
- (b) Imprint is the tendency of a ferroelectric layer to switch its polarization direction to a preferential state after being polarized in that state many times and then polarized in the opposite direction (this phenomenon is also attributed to the trapping of electrons at defects in the ferroelectric layer).
- (c) Polarization retention relates to the capacity of a ferroelectric capacitor to maintain a certain level of polarization for long periods of time.
- (d) Leakage current is the phenomenon whereby charges are lost from the capacitor; therefore, leakage should be minimized.

Materials integration strategies developed during the past several years resulted in the control of the capacitor degradation processes (fatigue, imprint, and leakage) described above. In the case of PZT film-based capacitors, the main strategy involved using conductive oxide electrodes or hybrid oxide-Pt electrodes [33, 34, 65], where the oxide electrode layer is in contact with the PZT film to control oxygen vacancies

and/or charge injection at the ferroelectric/electrode interface. In the case of the layered perovskite SBT, the degradation processes described above are controlled by the particular microstructure of the SBT material [66, 67], where the oxygen vacancies and/or charge injection at the ferroelectric layer/electrode (mainly Pt) interface appears to be controlled by an oxygen-rich/Bi layer. On the other hand, there is comparatively less understanding of the basic mechanism for polarization retention (or equivalently retention loss) in ferroelectric capacitors. Recent work involving nanoscale imaging of ferroelectric domains [68], using a piezoresponse atomic force microscopy technique, produced initial results which suggest that retention loss may be controlled by a random walk-type depolarization process. The exact physical basis for the retention loss is still undetermined. Work currently underway in several groups is necessary to unravel the details of the degradation mechanisms discussed above since they have important implications for ferroelectric memory technology.

### ***1.5.2 Nanoscale FeRAMs***

Nanoscale FeRAMs require very thin ferroelectric films ( $\leq 100$  nm thick) and nanoscale capacitors ( $\leq 100$  nm in diameter). The ferroelectric films with less than 100 nm thickness require synthesis with MOCVD and in the future ALD techniques capable of producing films with atomic scale interfaces with electrodes, which will be critical to achieve suitable polarization values for nanoscale FeRAMs. In this sense, Symetrix already demonstrated SBT films with thickness down to 50 nm, which exhibit good polarization vs. voltage curves.

## **1.6 Basic Unsolved Physics Problems Related to FeRAMs**

### ***1.6.1 Basic Science Issues***

The field of integrated ferroelectrics continues to be driven by the potential applications of thin film ferroelectrics, such as in nonvolatile memories, DRAM storage capacitors, and infrared detectors. However, it is clear that for the long-term success of this field, the scientific underpinnings need to be well established. The science of ferroelectric materials by itself is probably quite well established. However, the transition from the microscale low density (low Mb range) to nanoscale high density (high MB range to Gb and Tb) requires to understand the synthesis of very thin films ( $\leq 50$  nm), perhaps develop new ferroelectric materials with much higher polarization than present day materials, develop processes to fabricate 2D or 3D nanocapacitors (with dimensions  $\leq 30$  nm), and new nanoscale memory architectures, and understand phenomena in nanostructures. This work requires developing

new film synthesis techniques capable of producing ferroelectric films with extremely uniform composition and thickness on high aspect ratio nanostructures. For example, atomic layer deposition (ALD) may be the next method to supersede MOCVD to produce such films. Some key fundamental issues that require concerted and, in many cases, interdisciplinary effort for successful solution are discussed below.

#### **1.6.1.1 What Are the Finite Size Effects in Ferroelectric Capacitor Properties? How Small Can a Ferroelectric Capacitor Be and Still Exhibit Ferroelectric Behavior?**

NEC has reported switched polarization values for  $0.7 \times 0.7 \times 0.2 \mu\text{m}$  PZT capacitors. Mitsubishi and Symetrix have fabricated patterned  $1.0 \mu\text{m}$  capacitor arrays [69]. Recently, polarization switching was measured in SBT capacitors fabricated with  $0.1 \times 0.1 \times 0.05 \mu\text{m}$  electrodes of Bi oxide. The actual ferroelectric capacitor dimensions for a 1 Gbit FeRAM must have submicron lateral area and probably contain a ferroelectric layer about 50 nm thick. The effects of constrained geometries on ferroelectric capacitors are still largely unknown. Using a combination of focused ion beam milling and electric force microscopy, Ganpule et al. have demonstrated that both PZT and SBT thin film capacitors can be scaled to at least  $70 \text{ nm} \times 70 \text{ nm}$  in lateral dimensions. Intensive studies are currently underway focused on investigating the physics and performance of nanoscale size devices leading to the direct exploration of fundamental size effects and possible phase transitions driven by size constraints [69]. Theoretical work [19] indicated that depolarization fields in a typical ferroelectric capacitor with semiconducting electrodes would destroy the polarization switching properties of ferroelectric layers thinner than 400 nm, while similar depolarizing fields would destroy the switching properties of ferroelectric layers only 4 nm thick when integrated with metallic electrode layers. Subsequent theories indicated that the minimum ferroelectric film thickness, which could sustain polarization switching, was about 2.5 nm [19]. However, recent experiments [24] demonstrated that polarization is achieved in  $\text{PbTiO}_3$  (PTO) films of 3-unit cell layer thickness. These calculations were confirmed for PTO films in recent studies involving the use of the X-ray beam at the Advanced Photon Source (one of the two worldwide third generation X-ray synchrotron) at Argonne National Laboratory. These studies involved analyzing PTO film during and after growth using in situ X-ray scattering with atomic scale resolution [70]. The results showed that PTO films of 3-unit cells thick exhibit polarization, while films 2-unit cells thick do not exhibit polarization. Scaling of ferroelectric and dielectric properties with both thickness and lateral dimensions needs to be understood through a combination of experimental (fabrication, testing) and modeling studies. The use of sophisticated tools such as focused ion beam milling, templated growth, scanning force microscopy, and spectroscopy will be a strong focus of work in this area.

### 1.6.1.2 Stresses and the Role of Substrate-Film Interactions

The growth of ferroelectric thin films on substrates (which in most cases is Si) immediately places constraints, especially mechanically, which subsequently couples with the electrical and ferroelectric properties of the thin films. The magnitude of these coupling would likely depend on the coefficients in the Devonshire approximation of the free energy of the system. However, it is quite clear that the interplay between the mechanical properties of the substrate and the film can lead to suppressed polarization, dramatically decreased dielectric and piezoelectric coefficients, shifts in the phase transition temperatures, and possibly impact the polarization dynamics (switching and polarization relaxation). The interplay between substrate and film mechanical properties and its impact on electrical properties is an important area of R&D in microelectronics. A similar approach is undoubtedly required in the broad area of ferroelectric thin films, and a strong focus on this topic can be envisioned in the future, especially as devices make their way into the market and long-term reliability issues begin to dominate.

### 1.6.1.3 Polarization Dynamics

The role of stress impacts the polarization dynamics in thin films. The area of polarization dynamics itself is critical not only from the basic science but also from the device point of view. Indeed, it would be safe to assume that this is the most important of the fundamental topics that need a comprehensive and rigorous understanding, since this will ultimately impact the performance of ferroelectric devices. Polarization dynamics in ferroelectrics and dynamics encompasses a very broad bandwidth of timescales, from a few picoseconds for dipolar fluctuations in dielectrics such as BST to the 10-year retention time for ferroelectric memories that is impacted by the time-dependent changes in the remanent polarization. In between these two extremes, polarization switching occurs on timescales of a few nanoseconds while relaxation phenomena in relaxor ferroelectrics occur over timescales of a few seconds and longer. The interplay between thin film processing, microstructure, domain structure, and polarization dynamics is still poorly understood and will require measurements on carefully prepared and characterized test structures.

This can be illustrated through the case of retention loss in thin film ferroelectrics. Typically, the data on this topic present a log (time) dependence of the remanent polarization. However, in most cases, such a log (time) dependence is valid for a small time window. Furthermore, the log (time) function is mathematically unbounded at the extreme cases (i.e., at time=0 and at time=infinity). Therefore, fundamental studies, including direct observations of the relaxation processes, correlation to macroscopic measurements on discrete capacitors and integrated memory cells, and the development of mathematical models to understand and predict the relaxation behavior, are required. The role of fluctuations (thermal, electrical, chemical, dipolar, etc.) and perturbations (structural, chemical electrical, etc.)

on the polarization dynamics should prove to be a fertile area of fundamental research in the future. It should be noted that there has been a considerable body of work on two other aspects of polarization dynamics in polar ferroelectrics, namely fatigue and imprint. Although these two problems were identified in the early years as “show-stoppers,” it is safe to say that although there are technologically viable solutions to both these problems the fundamental understanding is far from complete.

Similarly, an important area of research for the future is the switching dynamics of nanoscale capacitors. In this case, not only is it important to understand the dynamics of the switching process beyond the Ishibashi–Avrami models, but equally important are approaches to measure the switching responses of sub-micron capacitors, especially in PZT and SBT thin films, both of which are known to switch over timescales shorter than 1 ns. Optical techniques (for example using femtosecond optical pulses to trigger and probe the switching process) will be required to obtain time-resolved information on switching.

The role of dipolar fluctuations in dielectrics such as BST and in most relaxors need to be investigated with high resolution (both spatial and temporal) probes. Novel probes such as NSOM and scanning microwave microscopy (SMWM) currently under development can potentially be useful in understanding the dipolar dynamics with high spatial resolution. A combination of microwave and optical measurements in conjunction with direct imaging of the structure (TEM, neutron diffraction, and synchrotron studies) should prove to be invaluable in providing unique insights into this complex problem.

#### 1.6.1.4 Role of Defects

The impact of defects is one area that is possibly strongly overlooked. Although considerable amount of defect chemistry understanding is already in place for bulk ferroelectrics and dielectrics (e.g., PZT, BST) there is very little work on the characterization (by direct means) of defects in thin films. This is especially true of point defects such as oxygen vacancies and cationic defects, both of which are considered as critical in determining the properties of ferroelectrics and dielectrics. Direct determination with high spatial resolution and compositional precision of the defect chemistry in thin films still remains a paradigm. We believe that this complex problem will have to be addressed at some point in the evolution of integrated ferroelectric devices.

### 1.7 Future Directions

Current FeRAMs have nearly identical cell structures as the stacked cell DRAMs, which are aimed at greater than 4 Gb in density using high dielectric constant materials such as BST ( $\text{Ba}_{1-x}\text{Sr}_x\text{TiO}_3$ ) and  $\text{Ta}_2\text{O}_5$ . This means that FeRAMs can now

enjoy all the process tools developed for DRAMs and go one step further in functionality by providing nonvolatility at low power. In the stacked cell configuration, a high-quality SBT thin film needs to be deposited with good step coverage, which can be obtained by MOCVD or LSMCD. Another interesting point is that SBT is a tantalate, which is compatible with silicon-based CMOSs, while strontium and bismuth have not proven to be deleterious to silicon.

Advanced MOSFETs for logic and other general uses are also adding Ta<sub>2</sub>O<sub>5</sub> layers in the gate stack. This material change is required because the ever-thinning oxide demands of CMOSs, which recently has been found to be very difficult to be satisfied by simply reducing the SiO<sub>2</sub> thickness, due to the fundamental physical limit of SiO<sub>2</sub> as an insulator. The FLASH cell is being transformed by adding a ferroelectric switching gate in place of programming by tunneling. This evolution changes the scaling rules for FLASH radically and allows significant improvements such as writing speed, which could be equal to that of DRAMs.

As mentioned above, use of layered perovskites such as SBT with film thickness  $\leq 100$  nm yields FERAMs write voltage of about 1 V. As the polarization is screened near the surface, the dielectric constant of the film controls the screening length. In the case of SBT, the screening length is below 20 nm, which allows the use of thinner SBT film while retaining good electrical characteristics. Writing speeds  $\leq 6$  ns can be achieved at the capacitor level, even for capacitors with thick SBT films ( $\geq 180$  nm) and large areas. For these devices, the speed is limited by the CMOSs, not by the intrinsic characteristics of the SBT layer. FERAMs are the only fast write nonvolatile memories existing today. This characteristic and the nearly fatigue-free behavior with low power make FERAMs the mature evolution of CMOS in the nonvolatile memory area.

Currently, and in the foreseeable future, FERAMs have the potential of impacting three major markets in the \$150B dollar range. First, as stand-alone memories, FERAMs will be in direct competition with FLASH, EEPROMs, DRAMs, and SRAMs based on cost and density. However, in many cases, density and even cost may not be as important as high-speed write and nonvolatility. In the second market, FERAMs are already enjoying a great position in cost and functionality. This is the case of contactless smart cards and other RFID devices. In this case, the fast write speed and low power allows the use of smart cards or tags in a variety of applications such as ticketing, fare collections, and inventory control. Finally, where the logic unit is a microcontroller or DSP (digital signal processor), FeRAMs already has shown interesting "system-on-chip" capabilities without the added complications of power transistors such as in EEPROMs and FLASH. Also, smart cards with embedded microcontroller have demonstrated that NVFRAMs are poised to enter this market.

In summary, FeRAMs, circa 2000, have entered commercialization as stand-alone memories (in low and medium densities), contactless cards and tags, and in embedded microcontrollers. These are also among the fastest growing segments of the semiconductor industry. Adding to this the prospect of BST in DRAMs, ferroelectrics have entered the semiconductor device world in almost every market segment.



## 1.8 Conclusions

In conclusion, the science and technology of nonvolatile ferroelectric memories have experienced remarkable progress in the last 11 years, which resulted in the introduction into the market of the first products of mass consumption based on FeRAMs. The materials integration and fabrication strategies, in addition to device architectures, developed in this period are suitable for the fabrication of low-density FeRAMs, where the capacitors are located outside the CMOS transistor areas. However, the next generation of high-density FeRAMs requires nanoscale capacitors with 3D architectures. In addition, further work is necessary to clarify and or solve basic science issues related to ferroelectricity, particularly at the nanoscale. Given the remarkable progress in the science and technology of ferroelectric thin films during the last 10 years, it is expected that even more exciting times are ahead for the field of integrated ferroelectrics.

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# Chapter 2

## Hybrid CMOS/Magnetic Memories (MRAMs) and Logic Circuits

B. Dieny, R. Sousa, G. Prenat, L. Prejbeanu, and O. Redon

### 2.1 Introduction to Spintronics Phenomena Used in MRAM

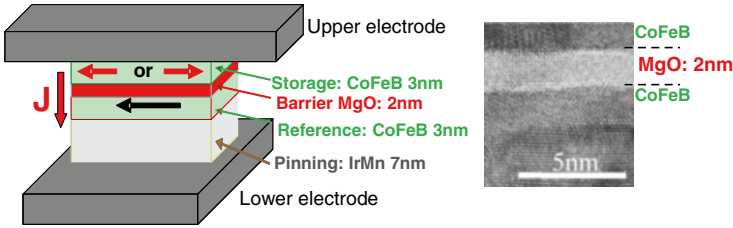
#### 2.1.1 GMR Discovery and Launching of Spin electronics

Spintronics (or spin electronics) is a continuously expanding area of research and development at the merge between magnetism and electronics. It aims at taking advantage of the quantum characteristic of the electrons, i.e., its spin, to create new functionalities and new devices. Spintronic devices comprise magnetic layers which serve as spin polarizers or analyzers separated by nonmagnetic layers through which the spin-polarized electrons are transmitted. It is considered that spintronics started in 1988 with the discovery of the giant magnetoresistance (GMR) effect, which corresponds to a large variation of the resistance of a magnetic multilayer under the application of a magnetic field [1]. Shortly later, spin valve structures were invented [2]. The latter exhibit GMR at low fields and thereby constitute very sensitive magnetic field sensors. In 1998, they were introduced as sensing elements in readback heads in computer disk drives. More than one billion of such read heads are produced each year. Besides the usual applications of hard disk drives in desktops,

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**Fig. 2.1** Schematic representation of a magnetic tunnel junction sandwiched between two electrodes and transmission electron cross-sectional micrograph showing an MgO barrier separating two CoFeB electrodes

laptops, or servers, the reduction in their form factor (one inch drive) has allowed to introduce magnetic disk drives in other consumer electronics products such as camcorders, or movie recorders.

### 2.1.2 Tunnel Magnetoresistance

In 1995, a second breakthrough was achieved with the discovery of room temperature tunnel magnetoresistance (TMR) in magnetic tunnel junctions (MTJs) [3, 4]. MTJs consist of a stack of two ferromagnetic layers separated by a thin insulating layer. The ferromagnetic layers are most commonly Co- or Fe-based alloys. This stack is sandwiched between a bottom and a top electrode (see Fig. 2.1). By applying a bias voltage between these electrodes, a current flows through the stack perpendicular to the interfaces. The electrons tunnel through the insulating barrier which is typically between 1 and 2 nm thick. The electrons emitted from one ferromagnetic layer are spin polarized in a direction parallel to the magnetization of this emitting layer. Their probability to go through the barrier depends on the magnetic state of the receiving ferromagnetic layer and in particular whether its magnetization is parallel or antiparallel to that of the emitting ferromagnetic layer. As a result, as in giant magnetoresistance, the resistance of the stack depends on the relative orientation of the magnetization in the two ferromagnetic layers adjacent to the tunnel barrier. This phenomenon is named “tunnel magnetoresistance (TMR)”.

In order to be able to change the relative orientation of the magnetization in the two ferromagnetic layers, the magnetization of one of these layers is generally pinned by exchange interaction with an adjacent antiferromagnetic layer (most commonly in IrMn or PtMn). The interfacial exchange coupling between a ferromagnetic layer and an antiferromagnetic layer is known as “exchange bias.” It results in a shift of the hysteresis loop of the coupled ferromagnetic layer around a finite magnetic field named the exchange bias field. This hysteresis loop shift can be viewed as a unidirectional anisotropy acting on the magnetization of the pinned ferromagnetic layer. It vanishes at a critical temperature called the blocking temperature which is typically of the order of 200 °C for IrMn and 300 °C for PtMn.

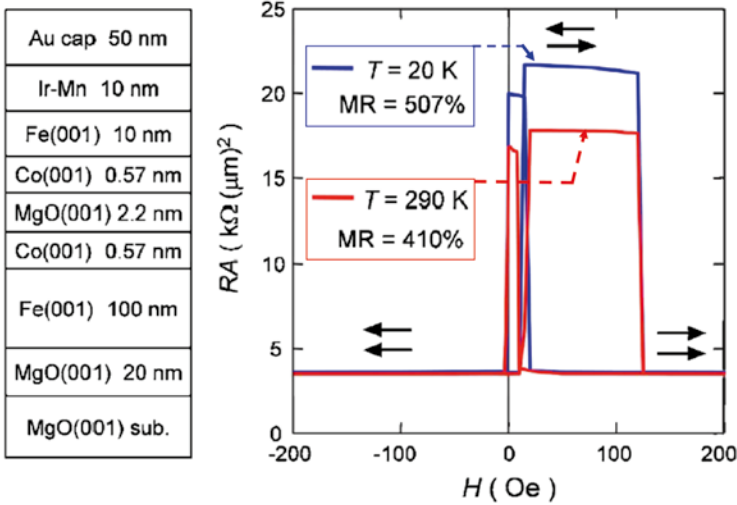


Fig. 2.2 Above 400 % tunnel magnetoresistance in MgO-based MTJ. From [7]

Physically, below the blocking temperature, the antiferromagnetic layer can be viewed as a block of ice trapping an arrow representing the magnetization of the adjacent ferromagnetic layer. When heated above its blocking temperature, the ice melts and the arrow can be switched. In MTJ, the ferromagnetic layer of pinned magnetization is often called the reference layer. In contrast, the magnetization of the other layer can be switched by application of an external magnetic field or by the action of the spin-polarized current flowing through the structure as explained further. The layer of switchable magnetization is called the sensing layer (in a sensor application) or the storage layer (in a memory application) (see Fig. 2.1).

TMR amplitudes between 20 and 50 % were first observed in alumina-based junctions [3, 4] but much larger amplitudes were later observed in crystalline MgO-based junctions [5, 6] exceeding 400 % [7, 8] and even 600 % at RT (see Fig. 2.2).

This huge increase in TMR amplitude between MgO- and Alumina-based MTJ is due to the crystalline nature of the MgO barriers. In MTJ comprising an amorphous barrier, the TMR only originates from the different densities of states at the Fermi level for spin  $\uparrow$  and  $\downarrow$  electrons along the interface between the tunnel barrier and the adjacent magnetic layer. In MTJ comprising a crystalline barrier, another phenomenon takes place: there is a filtering of the tunneling electrons according to the symmetry of their wave function. The electrons whose wave function has a symmetry compatible with that of the MgO crystallographic lattice can tunnel through the barrier much more easily than those with a different symmetry [9, 10]. It was shown that if the magnetic electrodes are Co-rich alloys of bcc structure, only or mainly spin  $\uparrow$  electrons have the adequate symmetry to propagate through the MgO barriers. As a result, a quasi-perfect spin filtering of the tunneling electrons takes place leading to an effective polarization of the tunneling electrons close to 100 % and therefore to very large TMR amplitude.

In MTJ, the resistance of the stack is largely dominated by the resistance of the tunnel barrier itself. The latter varies exponentially with its thickness. The appropriate quantity to characterize the resistance of the barrier is its Resistance  $\times$  Area product most often written as R.A product. R.A of MTJ can range from tenths of ohms.micron<sup>2</sup> ( $\Omega \mu\text{m}^2$ ) up to  $\text{M}\Omega \mu\text{m}^2$  or even more. By properly choosing the MTJ barrier thickness, it is then possible to adjust the resistance of MTJ pillars to the  $\text{k}\Omega$  range, which is the order of resistance of a passing CMOS field effect transistor (MOSFET). This is a considerable advantage of MTJ with respect to GMR metallic pillars. Indeed, in current-perpendicular-to-plane geometry, GMR metallic pillars have resistance in the range of  $10^{-2}$  to  $10^{-1} \Omega \mu\text{m}^2$  which is too low to be useable in combination with CMOS electronics. Furthermore, MTJ can be deposited on almost any substrate provided the starting roughness is low enough (typically rms below 4 Å). This means that MTJ can be deposited above CMOS integrated circuits and subsequently processed using a back-end magnetic process. Therefore MTJs provide a very nice route towards CMOS/magnetism integration. They allow the design and realization of spintronic devices in which CMOS components are vertically interconnected with MTJ through vias. This hybrid CMOS/MTJ technology can significantly help improving the performances of CMOS-only devices or realizing innovative functions. The introduction of magnetism in CMOS circuits allows bringing nonvolatility in CMOS circuits together with low power consumption, very large cyclability (i.e., ability to switch the magnetic state almost an unlimited number of times), and very fast switching speed (in the nanosecond range).

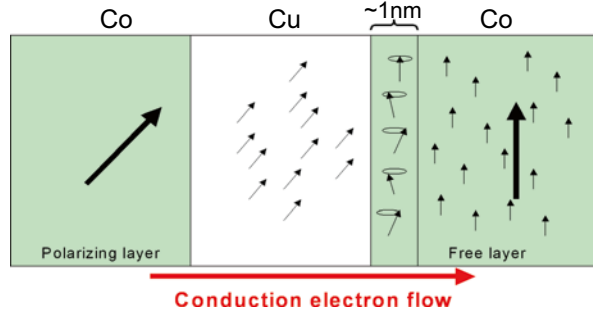
MTJs are now implemented in various applications in which their variable resistance is used to store an information (as for instance in nonvolatile magnetic memories, MRAMs), to process it (magnetic logic gates), or to define the function of CMOS logic circuits (reprogrammable logic).

### 2.1.3 Spin-Transfer Phenomenon

The magnetoresistance phenomena discussed in the previous sections (GMR or TMR) allow controlling an electron flow through a magnetic nanostructure by its magnetic state. The reciprocal phenomenon also exists. A spin-polarized current flowing through a magnetic nanostructure can influence its magnetic state. This is due to the exchange interaction between the spin of the incoming conduction electrons and the spin of the electrons responsible for the local magnetization. This phenomenon was first predicted by two theoreticians: Slonczewski and Berger in 1996 [11–14] and observed experimentally a few years later [15–17]. A simple picture of the phenomenon can be given in relation to Fig. 2.3.

Let us consider a sandwich structure comprising two ferromagnetic Co layers separated by a metallic nonmagnetic spacer as represented in Fig. 2.3. When a current flows from right to left, i.e., electrons flow from left to right, the conduction electrons become polarized when they traverse the left polarizing ferromagnetic layer because of spin-dependent scattering phenomena taking place in this layer.

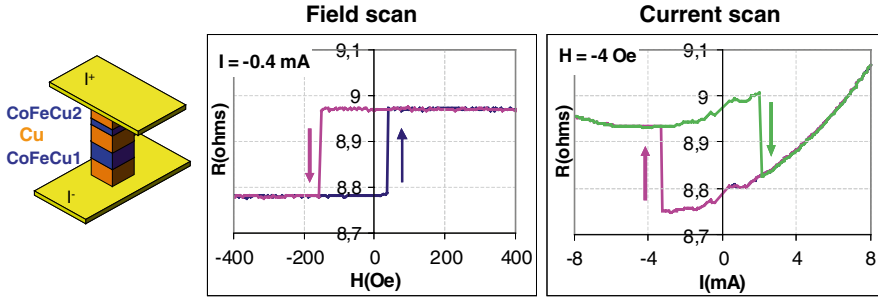
**Fig. 2.3** Schematic representation of the spin-transfer phenomenon



As a result, the current coming out of the left Co layer (polarizing layer) has a net spin polarization parallel to the magnetization of this left layer. The spin-polarized conduction electrons then drift through the Cu nonmagnetic metallic spacer and reach the interface of the right Co layer. The electrons are then partly reflected and partly transmitted at the Cu/Co interface. When penetrating in the free ferromagnetic layer, the spin of the transmitted electrons precess incoherently around the local exchange field which is along the magnetization of the right free layer. As a result, within a very short distance of the order of 1 nm, the direction of spin polarization of the incoming electrons is in average reoriented along the direction of the local magnetization. This spin polarization reorientation generates an incoming flow of angular momentum which is transmitted to the local magnetization and exerts a torque on it. This torque has been named spin-transfer torque. It contains two terms:  $I_{ST} = -\gamma a M \times (M \times M_P) - \gamma b (M \times M_P)$ .

The first term is usually called the spin-torque term or Slonczewski term [11, 12], the second one is called the effective field term. The magnitude of this second term is much smaller than the first one in metallic pillars (typically less than 10 %) [18]. However, in magnetic tunnel junctions, it can be of the order of 30–50 % of the spin-torque term. This difference originates from the fact that in MTJ, the electrons which can tunnel through the barrier are mainly those having a momentum close to the normal to the barrier. Indeed, for these electrons the effective thickness of the barrier is the smallest making the tunneling through the barrier easier than at oblique incidence. As a result of this momentum selection, the precessional motion of the spin of the tunneling electrons is more coherent when they enter the magnetic layer. This yields a larger amplitude of the effective field term. In metallic pillars, both terms are proportional to the current density and to the current polarization. In MTJ, the in-plane torque component has been found to vary essentially linearly with bias voltage but may also contain an additional quadratic component [19]. On the other hand, the perpendicular torque component exhibits a quadratic dependence on bias voltage with an additional linear variation in case of asymmetric tunnel junction, i.e., MTJ having two different magnetic electrodes [20]. Interestingly, the spin-torque term is nonconservative. It behaves like a damping or antidamping term depending on the current direction. Thus, the magnetization can pump energy from the spin current. This can generate very unusual dynamical effects:

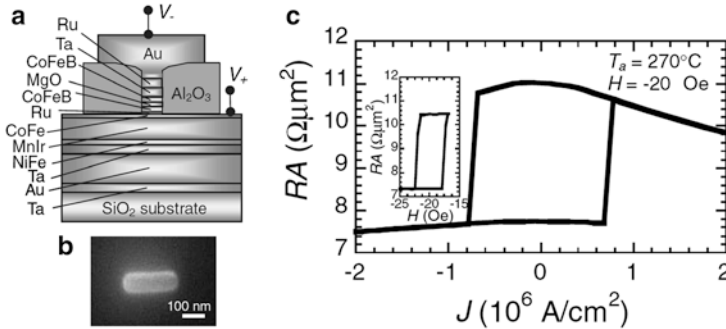




**Fig. 2.4** Illustration of spin-transfer magnetization switching. The composition of the sample was IrMn 7 nm/AP2 4.0 nm/Ru 0.8 nm/AP1 4.4 nm/Cu 2.6 nm/F 3.6 nm/Ta. From [17]. The *left picture* is a schematic representation of the multilayered stack patterned in the form of a “square” pillar of lateral size 130 nm. The *middle graph* is a plot of the usual CPP-GMR magnetoresistance response curve of the pillar when submitted to an in-plane field parallel to the direction of magnetization of the pinned layer. The *right graph* shows the magnetoresistance transfer curves as a function of the current flowing through the stack. The same transitions from parallel to antiparallel magnetic configurations are observed than in field scan but here due to spin transfer associated with the spin polarized current flowing through the stack

The spin-torque term can induce magnetization switching in a magnetic nanostructure traversed by a spin-polarized current. This was observed in sandwich nanopillars comprising a polarizing layer of fixed magnetization and another magnetic layer of switchable magnetization (often called “free layer”), these two layers being separated by a nonmagnetic spacer layer. This is illustrated as an example in Fig. 2.4 [17]. The left figure is a schematic representation of the stack comprising a CoFeCu(polarizing)/Cu(spacer)/CoFeCu(switchable) trilayer. The central figure illustrates magnetization switching when an external magnetic field is applied in the direction parallel to the magnetization of the pinned polarizing layer. The observed change of resistance is due to the current-perpendicular-to-plane GMR of the stack. The step of resistance takes place when the magnetization of the free layer switches. The low resistance state corresponds to parallel orientation of the magnetization in the pinned and free layers. The high resistance state is associated with antiparallel alignment. The most important part of this multilayer is the trilayer stack formed by the pinned reference layer named AP1 consisting of a CoFeCu alloy 4.4 nm thick, the free layer  $F$  of switchable magnetization also made of CoFeCu alloy 3.6 nm thick, and the nonmagnetic Cu spacer 2.6 nm thick. The pillars have a “square” section with a lateral size of 130 nm.

The right graph in Fig. 2.4 shows the resistance loop obtained when the current flowing through the structure is varied. The same transitions as in field scan between parallel and antiparallel magnetic configurations are observed. The magnetic switching of the free layer is not caused here by an external magnetic field but by the torque exerted on the free layer magnetization by the spin-polarized current coming or being reflected from the pinned layer. The switching takes place at current density of the order of  $j_c \sim 2.107$  A/cm<sup>2</sup>. The additional shifted parabolic



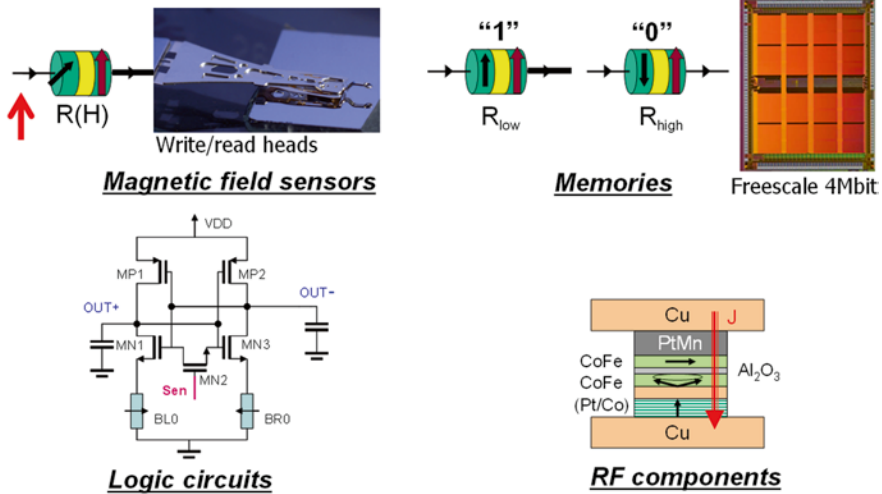
**Fig. 2.5** Example of current-induced switching in MTJ (from [21]). (a) Patterned pillar stack used for the experiment. The sample had been annealed at 270 °C to improve the crystallinity of the MgO barrier and adjacent CoFeB electrodes; (b) scanning electron microscopy image of the patterned MTJ before depositing the top electrode; (c) resistance  $\times$  area product versus current density flowing through the device showing the switching back and forth between antiparallel magnetic configuration (high-R state) and parallel magnetic configuration (low-R state). A weak magnetic field of  $-20$  Oe was applied during the experiment to compensate for the stray field from the reference layer acting on the storage layer. The *inset* shows for comparison the “usual hysteresis loop,” i.e., the same transition from high-R state to low-R state can be obtained at constant current by varying the magnetic field applied on the device

curvature seen on the right graph is due to a combination of Joule heating (quadratic contribution) and Peltier effect (linear effect) associated with the different nature of the bottom and top electrodes (NiFe bottom electrode versus Cu top electrode).

The spin-transfer-induced magnetization switching was first observed in metallic pillars but later on also in magnetic tunnel junctions [21–23] as illustrated in Fig. 2.5. Quite interestingly, the critical current densities required to switch the magnetization in magnetic tunnel junctions are much lower than in metallic pillars, typically by one order of magnitude (in the range of a few  $10^6$  A/cm<sup>2</sup> in MTJ versus a few  $10^7$  A/cm<sup>2</sup> in metallic pillars). This is explained both in terms of higher spin polarization of tunneling electrons in MTJ and angular selection of momentum for the tunneling electrons in MTJ.

The observation of current-induced switching of magnetization clearly illustrates that spin transfer provides a new way to manipulate the magnetization of magnetic nanostructures. So far, only external magnetic fields could be used to control the magnetic state of a magnetic nanostructure. Via spin transfer, spin-polarized currents can be used to produce the same effect. Since a current can be much more localized than a magnetic field, this approach offers outstanding advantages in terms of spatial control of switching as well as overall energy required for switching. Spin-transfer switching offers a very interesting write approach in MRAM as will be explained in a following section of this chapter.

Another quite interesting dynamic effect induced by spin torque under certain conditions is the generation of steady magnetic excitations. These excitations often



**Fig. 2.6** Illustration of the various classes of spintronic devices which can be conceived based on GMR, TMR, or spin transfer

take place when spin transfer and external applied magnetic field have opposite influence on the free layer magnetization, for instance one favoring parallel magnetic configuration whereas the other favoring antiparallel magnetic configuration. In this situation, the magnetization steadily pumps energy into the spin current to compensate the energy dissipation induced by the Gilbert damping. The frequency of these excitations is in the GHz range and varies with the current density flowing through the device. This very interesting phenomenon can be used in frequency tunable RF oscillators [24] but the discussion of this application is out of the scope of this chapter.

The various phenomena discussed above (GMR, TMR, spin transfer) have made possible the conception of several classes of spintronic devices. This is illustrated in Fig. 2.6. GMR and TMR have made possible the development of very sensitive magnetic field sensors which are being used as magnetoresistive read heads in hard disk drives. Magnetic tunnel junctions have become the basic elements of a new class of nonvolatile memories (MRAMs). In these memories spin transfer offers a very promising new write approach (see Sect. 2.2). MRAM chips already exist on the market (4 Mbit MRAM chips launched by Freescale in July 2006). Other classes of devices are still in research and development: logic circuits which combines MTJ together with CMOS components (see Sect. 2.3) and RF components taking advantage of the steady excitations induced by spin-transfer in combination with GMR or TMR to produce RF oscillatory voltage (not discussed here).

The following of this chapter is focussed on MRAM and logic applications using hybrid CMOS/MTJ technology.

## 2.2 Magnetic Random Access Memories

Several concepts of magnetic random access memories (MRAMs) have been proposed over the past 30 years based on different magnetic phenomena and materials. Among them, we may list the cross-tie RAM [25], then MRAM based on anisotropic magnetoresistance (AMR) materials followed by GMR MRAM [26]. The interest for MRAMs was renewed after the first successful attempts in fabricating spin-dependent magnetic tunnel junctions (MTJs) using amorphous  $\text{Al-O}_x$  barriers. Recent studies using crystalline MgO barriers have shown that it is possible to increase the available magnetoresistive signal up to 200 % resistance change at room temperature [5, 6], which is much larger than with the previously used spin-valve elements.

In the most basic implementation of MTJ-based MRAM, each memory cell consists of an MTJ connected in series with a selection transistor which can be viewed as a switch allowing the current to flow or not flow through the MTJ. The resistance of the memory bit is either low or high depending on the relative orientation of the magnetization of the free layer with respect to the fixed (pinned layer) layer (parallel or antiparallel magnetic configurations). These two configurations are used to binary store the information in MRAM.

In principle, MRAMs have the potential to combine nonvolatility, high speed, moderate power consumption, infinite endurance, and radiation hardness, all at low cost and easy to embed. However, MRAMs have not yet reached their expected performances. Large volume applications are still to be seen, with only field toggle switching-based 1–8 Mb standalone products currently available, at 180 nm technology node. The recent advent of spin-transfer torque (STT), however, has triggered a renewed interest in MRAM with the promises of much improved performances and greater scalability to very advanced technology node. As a consequence, MRAM is now viewed again as a credible replacement to existing technologies for applications where the combination of nonvolatility, speed, and endurance is required.

This chapter will present a review on the evolution of the writing and reading concepts in MRAMs, from fundamental research to the prototype chip demonstration. Challenges to overcome in order for MRAM to be a mainstream memory technology in future technology nodes will be further detailed. Potential applications of MRAM in embedded and standalone memory markets as well as for logic applications will be finally outlined.

### 2.2.1 *MRAM Based on Field-Induced Magnetization Switching*

Following the discovery of large TMR amplitudes at room temperature in  $\text{Al-O}_x$  based MTJs [3, 4], a regain of interest appeared for MRAM architectures. Since the late 1980s several magnetoresistive memories have been developed exploiting AMR

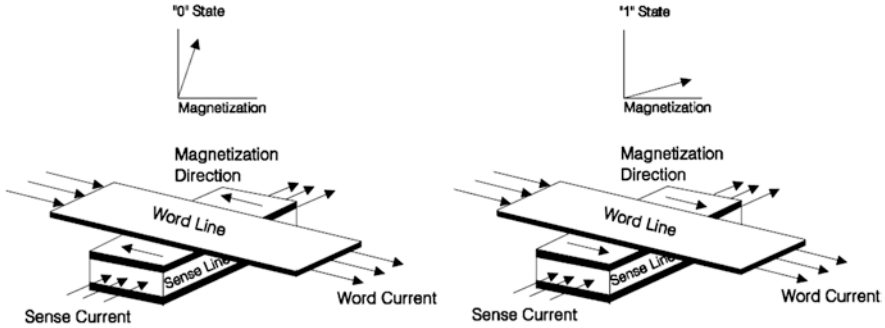
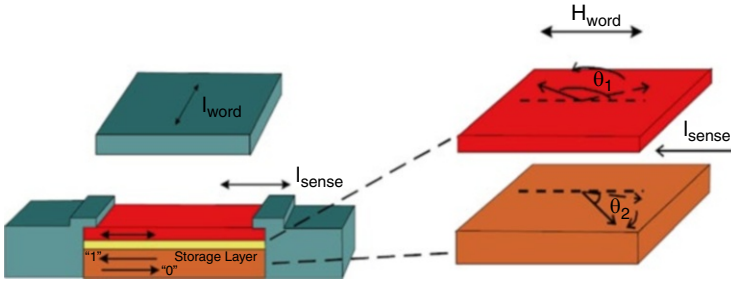


Fig. 2.7 Definition of the two digital states in an anisotropic MRAM structure (from [31])

or GMR effects [26, 27] but none of them have been competitive enough to overcome or even worry the mainstream CMOS memories. These first MRAM architectures had yet one advantage over their CMOS counterparts due to their radiation tolerance which makes them attractive for spatial and military applications [28]. Honeywell has been very active during this period to produce MRAM parts with capacity as large as 1 Mb and its product demonstrated its robustness when in 1986 NASA could retrieve data stored in the challenger magnetic memory after its dramatic explosion. However, these early magnetoresistive memories were suffering from important issues, mainly due to their low sheet resistances and low MR amplitudes.

The anisotropic MRAM developed in the early 1990s was using a simple cross-point architecture. They were based on the AMR phenomenon in magnetic transition metals (Ni, Fe, Co, and their alloys) which consists in a change of the electrical resistivity of these materials (by 2–4 %) as a function of the angle between the magnetization and the sense current. In most cases, the resistivity is largest when the current flows parallel to the magnetization and lowest when it flows perpendicular to it. The magnetic structure was using two equally thick FeCoNi layers separated by a thin Ta nonmagnetic layer. Each magnetic dot was patterned with an oblong shape and they were connected in series along their long direction [29, 30]. When a sense current was sent along these columns, the associated magnetic field could create a clockwise or anticlockwise alignment of the magnetization of the two magnetic layers along the short axis of the elements (see Fig. 2.7). Insulated word lines placed orthogonally create a magnetic field parallel to the long axis of said elements. By appropriate combination of sense and word current polarities during write operations “0” and “1” data could be encoded. The nondestructive read was ensured by a second combination of currents that allows exploiting the differential resistance due to the AMR effect. As the MR change in these elements was limited (1–2 %) and their individual resistance was small the read access time was about 250 ns in a 16 Kb MRAM chip [32] and the write currents were large (30 mA in the word line). Moreover scaling was an issue in this MRAM architecture as it impacted both the speed and the sensing margins.



**Fig. 2.8** Design and operation of a pseudo-spin-valve structure (from [31])

A second MRAM concept was introduced in the 1990s after the development of spin valves (SVs) [2], which is a nice exploitation at low fields of the GMR effect [1] discovered by Pr Fert and Grünberg. These SV systems consist in two magnetic layers separated by a nonmagnetic layer generally made of Cu. One of the magnetic layers has a fixed magnetization (if exchange biased with an antiferromagnetic materials) or requires a magnetic field of large amplitude to be switched, while the magnetization of the second can be rotated in a low/moderate magnetic field. Due to spin-dependent scattering, these systems exhibit a high resistance state (low resistance state) when the two magnetic layers are antiparallel (respectively, parallel). This simple embodiment is much more adapted for memory application than the previous concept and also benefits of a larger MR amplitude from 5 to 15 %. In a memory architecture the magnetic elements were patterned with elongated shapes of submicron dimensions to benefit from the demagnetization fields that define only two stable single domain magnetic states (along the long axis of the elements). The write operation required the application of two orthogonal fields: one generated along the hard axis (i.e., along the short axis) by the sense current flowing in the element that reduces the switching field and provides selectivity between the dots of the array and one applied along the easy axis to switch the magnetization of the soft magnetic layer. This second field was generated by the current flowing in an electrically isolated word line placed above and orthogonal to the long axis of the element (see Fig. 2.8).

This method using a superposition of two orthogonal magnetic fields is known as the Stoner–Wohlfarth switching. Two declinations of this concept were then proposed. The spin-valve MRAM stored the data in the soft layer while the hard layer was exchange biased with an antiferromagnetic material and thus theoretically never reoriented. The data were read out by performing a comparison between the voltage drop across the measured cell and the voltage drop of a reference cell [33]. This technique required the addition of an access transistor at each cell to steer the current path. The pseudo-spin valve MRAM used two magnetic layers with different coercive fields and the data were stored in the hard layer [34]. Upon reading, the soft magnetic layer was saturated with a defined sequence in the two possible orientations and the variation of the cell resistance was detected which gave access to the

data stored in the hard layer. This second technique being differential, no reference cell was required but the write currents were larger. Similarly to the anisotropic MRAM, the low sheet resistance was detrimental to get a high sensing margin for large arrays and the scalability was still poor.

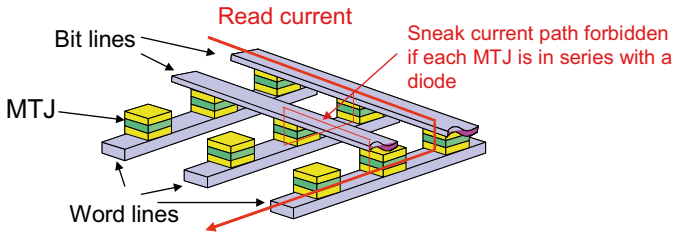
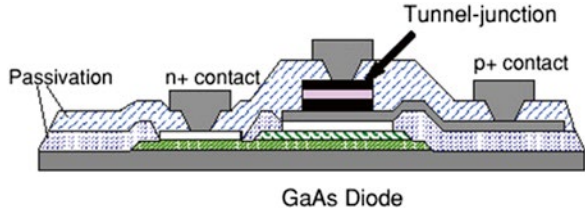
The advent of MTJs in 1995 opened new perspectives for MRAM products as the aforementioned limitations could be overcome. First, the MR amplitudes that were still modest in the first demonstrations [3, 4] rapidly increased over 50 % with the improvement of the magnetic electrodes, of the growth, oxidation and annealing conditions, and reached over 200 % in the early 2000s when the amorphous Al-O<sub>x</sub> barrier was replaced by the crystalline MgO barrier. Coherent tunnelling preventing mixing of the highly spin-polarized Bloch states could occur, leading to unprecedented MR amplitudes. In the most engineered systems TMR over 600 % could be achieved [8]. However, in practical systems with suitable magnetic properties, the TMR is generally about 200 %. Such high MR was an important breakthrough to make possible fast read operations even in large arrays. Second, the large impedance of the MTJ compared to the full metal AMR or spin-valve systems is more adapted with the CMOS circuitry. Even in a cell architecture comprising an MTJ associated with a FET selection transistor, high speed sensing can be possible. Last but not the least, the impedance of the MTJ can easily scale with the FET meaning that dense and large arrays can be designed. The only negative aspect of the MTJ is the TMR drop with increasing voltages which is quite detrimental from the read perspective.

With these improved features several memory architectures were feasible. The most compact was the cross-point architecture—as proposed in anisotropic MRAM—which was yet more adapted with the high impedance of the MTJ. In the paper by Wang [35] the architecture relies on high resistance MTJ to avoid sneak paths during write operation. For the read operation, all lines are carefully biased so that only one device is addressed. However, due to the large MTJ resistance and some unavoidable sneak current paths, the signal is weak and the read out is slow. The second architecture contains a selection device (a thin film diode) placed below each individual MTJ to more efficiently prevent sneak paths [36, 37] (see Fig. 2.9). During the read operation all the word lines that are connecting the cells below the diodes are biased with the same voltage as the top bit lines except for the addressed cell for which it is grounded. Thus, only one device is forward biased and the current that flows through it is detected (see Fig. 2.10). The main issue of such architecture is that it is very difficult to form compact diodes over the highly conducting word lines that can drive relatively high forward current to get a voltage drop across the diode substantially smaller than the voltage drop across the MTJ. The signal of the MTJ being diluted by the high resistance of the diode the sensing and the memory speed were affected and no attractive architecture could emerge.

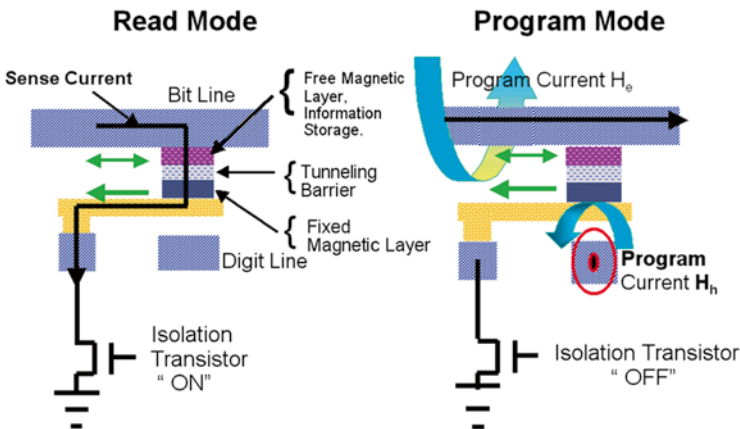
The last architecture involving a selection FET to prevent all sneak current paths has been the most successful to guarantee both high speed operations and correct sensing margin (Fig. 2.11). However, this latter architecture roughly doubles the cell area which impacted the memory compactness.



**Fig. 2.9** Cointegration of a tunnel junction and a planar thin film diode (from [36, 37])



**Fig. 2.10** Schematic of a memory array representing the current flow during read. Without diode, sneak current paths exist. If each MTJ is connected in series with a diode, sneak currents are dramatically reduced since the current can only flow vertically in one direction thanks to the diodes



**Fig. 2.11** Read and program modes in a SW-MRAM (from [38])

Motorola [38] and IBM [39] were the two main industrial players to rapidly recognize the potential of MTJ-based MRAM architectures. In the early 2000s, both were developing an MRAM architecture based on 1MTJ-1FET per cell and were exploiting the Stoner–Wohlfarth (SW) write scheme for the memory encoding.

The SW model gives the relationship between the strength of the field required to switch the magnetization and the direction of the applied field. Despite, this model is only valid for single domain configuration of the magnetic element and without temperature effects, it has been widely used to define the operation region



of the SW-MRAM. According to this model the angular dependence of the switching field  $H(\phi)$  is

$$H(\phi) = H(0) \left[ \cos^{2/3} \phi + \sin^{2/3} \phi \right]^{-3/2}$$

where  $H(0)$  is the field strength required when  $\phi=0$ . If the applied field is decomposed along the two  $x$ -component  $H_x$  and  $y$ -component  $H_y$  generated, respectively, by the digit and bit lines (see Figure) then the above equation can be rewritten in a form giving the condition of switching:

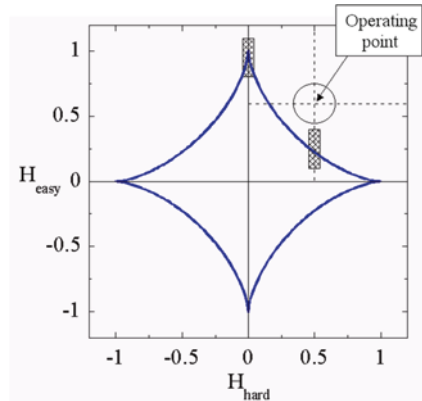
$$H_x^{2/3} + H_y^{2/3} \geq H(0)^{2/3}$$

This equation gives a starlike shape known as the switching astroid. For successful write operation any combination of  $H_x$  and  $H_y$  fields should fall outside the astroid as shown in Fig. 2.12. For minimum power consumption and optimum write margins, the combination should even fall in the area defined by the circle. Any appropriate combination of positive  $H_{\text{hard}}$  (corresponding to the bit line field) and positive  $H_{\text{easy}}$  (digit line field) will encode a digital “1” while a positive  $H_{\text{hard}}$  and a negative  $H_{\text{easy}}$  would encode a “0.”

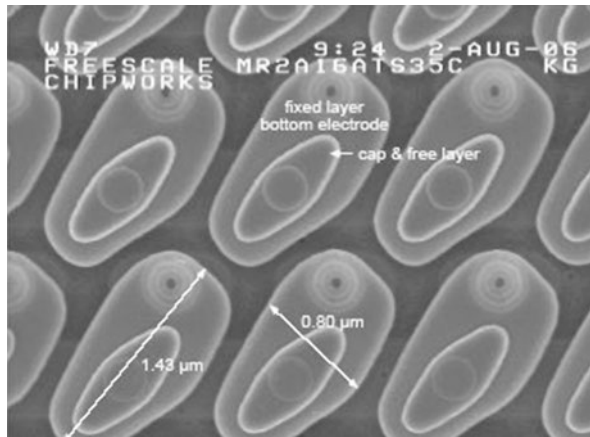
In the operating region, application of either  $H_x$  or  $H_y$  alone would not result in the data encoding. This is the basic principle of selection in the array where only the MTJ exposed to both  $H_x$  and  $H_y$  can be written.

This SW write scheme is efficient as long as all the bits constituting the array have identical or very similar magnetic properties. The distribution of the switching fields  $H(0)$  over the array should be as tight as possible to avoid write errors. The main parameters ruling the distribution widths are the uniformity of the chemical composition of the MTJ and the accuracy of the patterning process. Any defect or dispersion in the shape of the MTJ immediately results in a broadening of the switching field distribution. Similarly, the correct control of the shape upon scaling is very critical to tightly control the switching distribution. If the switching field of some bits gets too close to the astroid curve, its magnetic stability is reduced and it might be accidentally written due to thermal fluctuations even in the sole presence of the  $H_{\text{hard}}$  field. This problem known as the “half select instability” may also occur due to some irreproducibility in the switching process in the magnetic elements. Indeed, it has been observed that upon cycling, the switching field of a single element could vary over a relatively wide range depending on the magnetization reversal mechanism that occurred. These jumps between competing mechanisms are mainly due to the thermal fluctuations that cannot be neglected at room temperature. To prevent this detrimental effect of the thermal fluctuations, specific shapes were designed that proved to yield more repeatable switching process. This is the case of elongated hexagons as shown in Fig. 2.13 that were developed at Freescale. Element shapes with flat ends have more unpredictable switching mechanisms, as either C-state, S-states, or even vortex could develop due to large magnetic charges at their ends. Tapered ends are preferable to minimize magnetostatic fields although too sharp ends are difficult to technologically control.

**Fig. 2.12** Stoner–Wohlfarth astroid showing the optimum operating region for SW-MRAM (from [40])



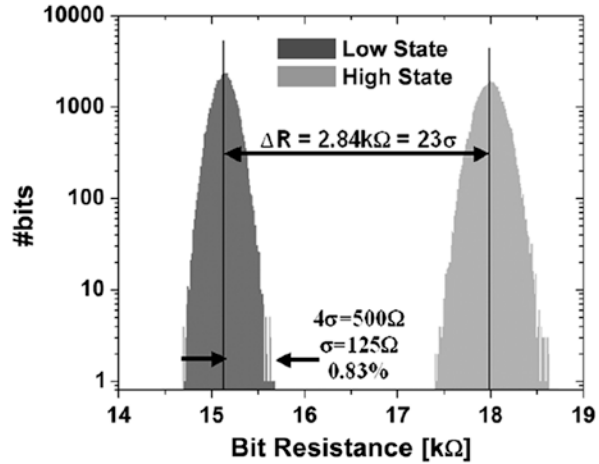
**Fig. 2.13** Shape of the MTJ elements in Freescale MRAM chip



Taking into account all these problems of switching field distributions and thermal fluctuations, the operating region of the SW-MRAM was quite reduced and often bits became inoperable. Industrials had thus to create redundancy bits to replace the defective ones. Due to the technological difficulties to produce a reliable product based on the SW write scheme, several industrials even stepped out of the MRAM arena, as Cypress or the IBM/Infineon alliance.

The read operation of this class of MRAM was greatly improved compared with all metal technologies (AMR or GMR based). However, large capacity chips required both large TMR and narrow distributions of the resistance in the two states (parallel and antiparallel configurations). In architectures using midpoint reference cells for the detection of the information stored in the magnetic bits a minimum of 12-sigma is required for multi-megabits arrays between the centers of the distribution of the resistance of high and low resistance states. In the 4 Mb demonstrator chip of Motorola published in 2005, thanks to an improved process control of the bit patterning, over 20-sigma separation was demonstrated giving ample read margin

**Fig. 2.14** Low and high resistance state distributions measured on a 4 Mbits MRAM chip of Motorola (from [41])

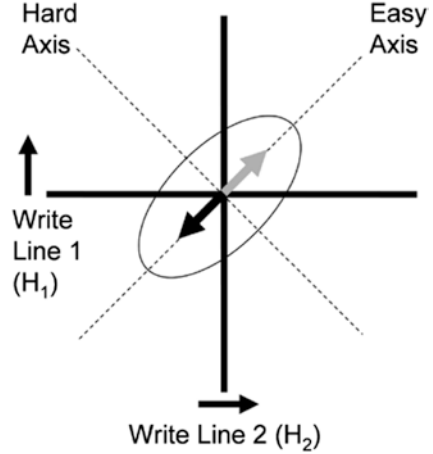


(see Fig. 2.14). The largest SW-MRAM chip that has been produced was the 16 Mb chip from the alliance IBM-Infineon [42], which is also the largest MRAM chip ever fabricated. It was built from a  $0.18 \mu\text{m}$  CMOS technology with three additional mask levels for the realization of the MRAM elements.

The cell size including the FET and the MTJ had a footprint of  $1.42 \mu\text{m}^2$  corresponding to  $44F^2$  which is almost tenfold larger than a NOR Flash cell. The write cycle time and the read access time were both of 30 ns but the average write and read currents were high with 80 mA and 25 mA, respectively [43]. One way to reduce the write currents in the bit and digit lines is the use of cladded Cu lines [44]. This technique, first proposed by Motorola, consists in embedding the Cu lines on three faces in magnetic materials with high permeability such as NiFe. It has the double advantage to guide the magnetic field on the region of interest and thus boost its magnitude roughly by a factor of 2 and to prevent stray magnetic field in the surrounding circuits. For similar switching conditions the required currents were thus divided by a factor 2.

In order to circumvent the intrinsic limitations of the SW-MRAM, L. Savtchenko from Motorola proposed in 2003 a new write technique that solved the issue of “half select instability” which is called the toggle switching [45]. This new switching approach is based on the unique property of synthetic antiferromagnetic layers which consist in a trilayer of two magnetic layers separated by a thin non magnetic layer of Ru. For proper choice of the Ru thickness (between 0.5 and 1 nm), the RKKY coupling between the two magnetic layers is antiparallel and its strength can be adjusted by finely tuning the Ru thickness. In zero magnetic field the tri-layer has a quasi-null remnant magnetization (when the two magnetic layers have identical thickness and chemical composition). This zero net moment as in an antiferromagnet has led to the name of “synthetic antiferromagnet” (SAF). In such system, there exists a critical field, called the spin-flop field ( $H_{sf}$ ), at which the two magnetizations that were antiparallel at low field suddenly rotate to be orthogonal to the applied

**Fig. 2.15** Schematic orientation of the bit with respect to the programming lines.  $H_2$  refers to the field generated by the bit line and  $H_1$  to the field generated by the digit line (from [41])

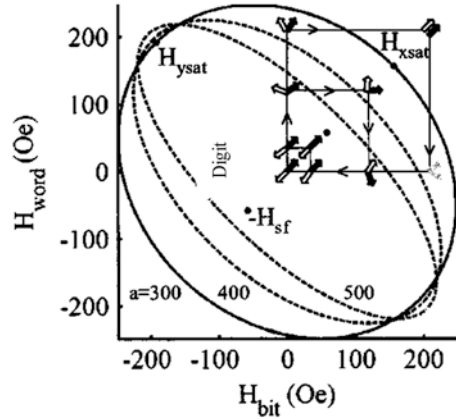


field while slightly scissoring in the direction of the field. For  $H > H_{sf}$ , the system presents a finite remnant magnetization that can be used to drive the system in the proper direction with a combination of fields applied along the hard and easy axes of the bit. To correctly exploit this phenomenon, the bit is patterned with an elongated shape and oriented at  $45^\circ$  with respect to the programming bit and digit lines [41] (Fig. 2.15).

With this tilted configuration, the activation energy of the system in the half selected configurations (i.e., when only  $H_1$  or  $H_2$  is applied) initially increases up to a field amplitude roughly equal to  $H_{sat}/2$  ( $H_{sat}$  being the field necessary to saturate the two magnetizations parallel to each other) then it decreases to reach zero about  $H_{sat}$  [46]. This is in dramatic contrast with the SW model where the activation energy is continuously reduced under half select configuration. This new approach thus confers a large stability to the encoded magnetic states.

The data encoding is depicted in the diagram of Fig. 2.16. For a correct toggle write, the sequence of  $H_{bit}$  and  $H_{digit}$  should swing around the  $H_{sf}$  field. If the field excursion does not turn around  $H_{sf}$  no switching occurs (see small square excursion at the centre). If the field excursion falls out of the saturation boundary then the bit would return in an undetermined configuration either “0” or “1” (large square path). In the intermediate case the system will first scissor in the direction of the sole digit field, then it will toggle towards the easy axis under the coincident digit and bit fields, toggle again in the direction of the sole bit field, and ends up in the opposite antiparallel state when all fields are suppressed. If the same sequence is applied again, the bit will be rewritten; it is thus important to know the initial configuration before write. When the shape of the bit is more elongated in the direction of the easy axis, the saturation boundary along x is reduced and the write margin is reduced (see dashed lines). When the field excursion is getting closer to  $H_{sf}$  the risk of soft errors is increased as the activation energy falls to zero along the easy axis when  $H = H_{sf}$ . To prevent such issue and get the largest operation region, it is preferable to have the intrinsic and shape anisotropies orthogonal to each other [47].

**Fig. 2.16** Critical switching curves for spin-flop switching in a toggle MRAM. The *solid line* corresponds to a circular dot and the *dashed line* to elongated shapes with  $AR=1.33$  and  $1.66$ . (from [46])



Toggle MRAMs have been extensively studied by Motorola, Freescale, and then Everspin (the spin-off of Freescale that industrialized the MRAM), and they are manufacturing a full family of MRAM products ranging from 256 Kb to 16 Mb for a large panel of applications. Toggle MRAM has taken market shares to the conventional Flash memory in the data storage industry where its speed and unlimited endurance were appreciated for data logging or file allocation tables. It is also advantageously replacing battery-backed SRAM in all systems where critical data should be rapidly stored upon power failure. Finally its historical advantage of radiation immunity makes it a natural choice for spatial and aeronautics applications (see [http://www.everspin.com/PDF/press/2009\\_sept\\_8\\_airbus.pdf](http://www.everspin.com/PDF/press/2009_sept_8_airbus.pdf)).

The commercialization by Freescale of a 4 Mbit MRAM is regarded as an outstanding achievement because it demonstrated that the integration of a front-end CMOS process together with a back-end magnetic process in a commercial product was possible. However, all MRAM technologies based on field-induced switching write schemes are poorly scalable. Indeed, all the concepts based on local magnetic fields and that required shape anisotropy to guarantee the stability of the stored data are inherently poorly scalable. The reason is the following: The energy barrier between the two states has to be kept above  $40 K_B T$  to guarantee 10 years data retention which implies either to maintain the magnetic volume or to increase the effective anisotropy. In both cases, the switching fields for SW write or the  $H_{sf}$  for toggle write drastically increases. The write power is thus continuously increasing which makes these concepts not viable at small technological nodes. The toggle MRAM is not predicted to operate for nodes smaller than 45 nm.

To circumvent this scalability issue of field-induced switching, several solutions have been proposed. They consist in different approaches for writing the information in the memory cell, i.e., switching the magnetization of the storage layer. These are thermally assisted write (TA-MRAM) and spin-transfer torque (STT-RAM) switching. Both TA-MRAM and STT-RAM represent real improvements compared with standard MRAM as explained in the following sections.

## 2.2.2 Thermally Assisted FIMS MRAM

### 2.2.2.1 General Principle of Thermally Assisted Approach

A thermally assisted switching (TAS) MRAM concept (TA-MRAM) was proposed to improve the thermal stability, write selectivity, and power consumption of MRAM cells [48–52]. A convenient approach to TA-MRAM is to heat directly with a current flow through the MRAM cell. This is the scheme developed by Spintec and Crocus Technology [48], in which a conventional MRAM junction is modified by replacing the simple ferromagnetic storage layer by an exchange-biased storage layer, i.e., a ferromagnetic storage layer exchange coupled to an antiferromagnetic layer. The write procedure requires heating above the storage layer blocking temperature and cooling down in the presence of a magnetic field. The reference and the storage layer must be exchange biased at different blocking temperatures. Typically PtMn with blocking temperatures of 350 °C is used in the reference layer and the storage layer antiferromagnet is chosen with a blocking temperature in the range of 180 °C to 250 °C, resulting in a large temperature difference in blocking temperatures for the reference and storage layers. The main advantages of this scheme is the use of a single field selection line, compared to other field write concepts, and realizing high thermal stability cell due to the exchange pinning. The temperature increase in the TA-MRAM cell is proportional to the dissipated power density  $P_d$ . This proportionality between the temperature increase and the power density can be observed directly from the linear decrease of the exchange-bias field both with the total heating power density and also with temperature. The total power density is essentially determined by the  $R \times A$  product (Resistance  $\times$  Area product) of the junction and the current density  $j$  as  $P_d = R \times A j^2$ . The maximum power density is limited by the junction breakdown voltage as  $j_{\max} = V_{bd} / R \times A$ .

A bit write sequence, illustrated in the bottom drawing in Fig. 2.17, starts from a given initial orientation of the magnetization of the exchange-biased storage layer, for instance, representing a low resistance state “0.” The corresponding storage layer loop is shifted around a negative field, as seen in Fig. 2.18 in the hysteresis cycle before the heating pulse is applied (curve labelled “before”). The reversal of the storage layer bias is achieved by heating the AF layer above its blocking temperature with a current pulse and applying simultaneously an external magnetic field  $H_{sw}$  larger than the coercive field of the storage layer. The field is applied in a direction that favors the antiparallel alignment of the storage and reference layers. The current pulse is terminated and the system is cooled in a magnetic field. This maintains the storage layer orientation and prevents freezing in a vortex-like configuration which may be induced by the circular symmetry of the Ampere field generated by the heating current. The result is a reversal of the pinning orientation of the storage layer and a bit state change to a high resistance “1.” As a result the storage layer loop is now shifted towards positive values as shown in Fig. 2.18 (curve labelled “after”).

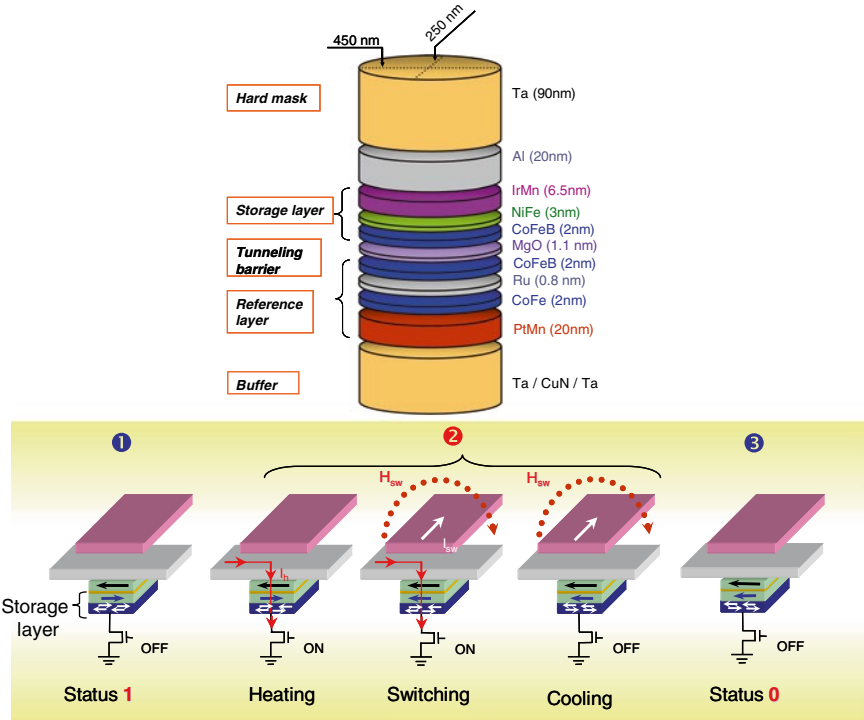


Fig. 2.17 *Top*: structure of a TA-MRAM cell. *Bottom*: writing steps of thermally assisted switching approach (as described in text)

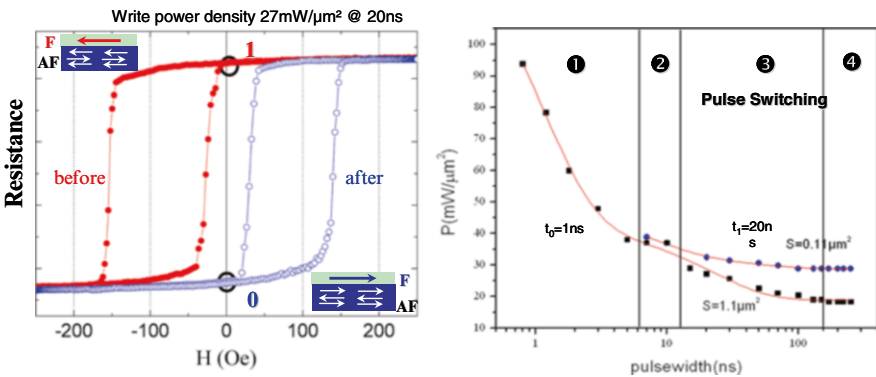


Fig. 2.18 *Left*: resistance hysteresis loops of the exchange-biased storage layer before and after writing showing the inversion of the hysteresis loop shift. Note that in both cases, only one remnant state is stable at zero field: either the low or high resistance state meaning that the memory is very stable against perturbing external field. *Right*: minimum heating power for writing as a function of heating pulse width

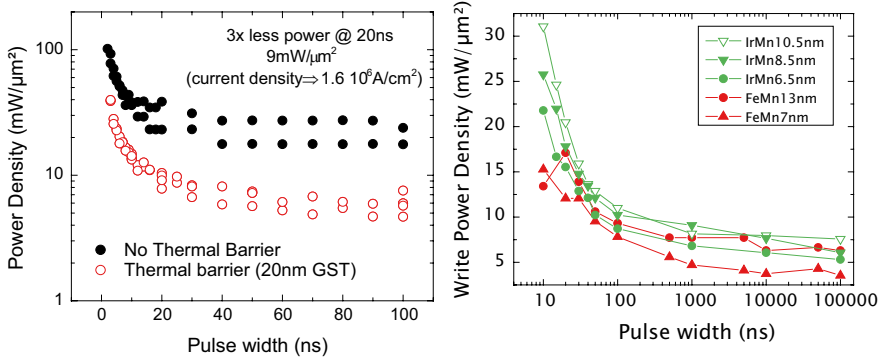
The first demonstrations of TA-MRAM were realized in micron-size junctions ( $2 \times 2 \mu\text{m}^2$ ) for DC currents [50] and current pulses down to 10 ns [51]. In DC current experiments, the storage layer loop could be shifted using a heating DC power density of  $3.2 \text{ mW}/\mu\text{m}^2$  applied in the presence of a 20 Oe field. The result is the reversal of the storage layer pinning direction. Subsequent dynamic writing demonstrations of TA-MRAM using current pulses less than 100 ns long were realized on sub-micron junctions patterned using e-beam lithography and ion beam etching, with typical stack structures of Ta 3/CuN 60/Ta 3/PtMn 20/CoFe 2/Ru 0.8/CoFeB 2/MgO 1.1+Ox/CoFeB 2/NiFe 3/IrMn 6.5 nm. For the particular demonstration illustrated in Fig. 2.18, the current pulses were 20 ns and the write power density was  $20\text{--}30 \text{ mW}/\mu\text{m}^2$ , which for the  $50 \Omega \mu\text{m}^2 R \times A$  product of these junctions results in a current density of  $2.3\text{E}6 \text{ A}/\text{cm}^2$ . This is about the same current density range as STT induced switching critical currents.

Measurements of the write power density as a function of pulse width from 300 ps to 300 ns show the existence of four different heating regimes in this time range: (1) a sharp increase of the power density for pulses shorter than 4 ns in region 1, (2) region 2 between 5 and 10 ns where the power density is almost constant, (3) a slow decrease of the power density in region 3 between 20 and 100 ns, (4) followed by an almost constant power density in region 4, for pulses larger than 150 ns. The physical origin of the different heating mechanisms could be identified using thermodynamic numerical simulations of the time-resolved heat equation. Generally, if at  $t=0$  a power density  $P_d$  is delivered to the tunnel junction, the temperature within the junction evolves according to the following equation:  $T = T_0 + \Delta T [1 - \exp(-t/\tau)]$ , where  $T_0$  is the initial temperature at  $t=0$ ,  $\Delta T$  is the temperature increase, and  $\tau$  is the characteristic heating time. Below 4 ns it is possible to write the cell at the cost of an increased power density. This is mostly an adiabatic heating regime where the heat remains confined to the junction region. The tunnel junction pillar reaches equilibrium in region 2, the bottom and top leads still remaining close to  $T_0$ . For longer heating pulses, in region 3, a gradual increase of the leads temperature takes place, as the power dissipated in the junction flows into the leads. Smaller junction sizes dissipate less power, resulting in less heating of the junction leads. Since the temperature increase of the leads adds to the temperature increase of the junction itself, larger junctions result in lower power densities because of the higher leads temperature increase. Finally in region 4 the junction pillar and also the leads both reach an equilibrium temperature.

### 2.2.2.2 Reducing the Heating Power Density

One way to increase the heating efficiency and reduce the power density is to insert low thermal conductivity materials at top and bottom of the magnetic tunnel junction stack, serving as thermal barriers between the junction and the electrical leads. This confines the heat to the junction volume, preventing lead heating and possible thermal cross talk. This has been used to reduce the write power density in TA-MRAM cells as shown in Fig. 2.19. The thermal barrier requires a thermal

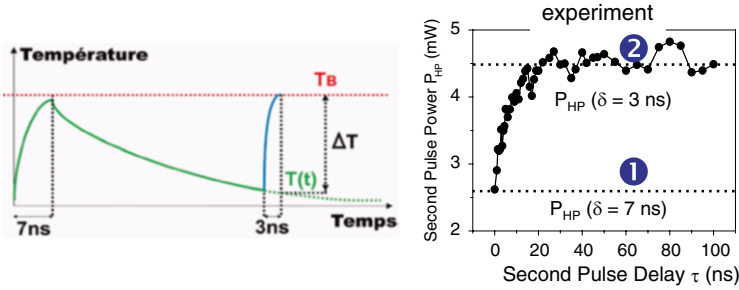




**Fig. 2.19** *Left*: comparison of heating power density for writing with and without in-stack thermal barriers. *Right*: comparison of heating power density for writing in MRAM cells comprising IrMn or FeMn exchange-biased storage layers

conductivity below 1.5 W/m/K, but at the same time the material needs to be electrically conducting. Such properties can be achieved for example with chalcogenide phase change materials in their crystalline phase [53]. This principle was applied to reduce the write power density by a factor of 3, when compared to cells without thermal barrier, as illustrated in Fig. 2.19. In this case a 20 nm layer of GeSbTe alloy was used to confine the heat, resulting in a write power density below 10 mW/μm² and a current density of 1.6E6 A/cm² for pulse widths of only 15–20 ns.

Another possibility to reduce the write power density is the use of AF materials with lower Néel temperature. As the write pulse width decreases from the quasi-static limit to below 10 ns, an increase in the required heating power density is observed. This increase is the consequence of the blocking temperature dependence on the measurement time. For longer times, the exchange loss is assisted by thermal relaxation, resulting in typical blocking temperatures that are much lower than the AF Néel temperature. As the pulse width is decreased, the blocking temperature increases and becomes closer and closer to the Néel temperature of the AF material. This is illustrated in Fig. 2.19 which compares the heating write power using IrMn with that for FeMn which has a much lower Néel temperature ( $T_{\text{Neel}} \sim 400$  °C for IrMn whereas  $T_{\text{Neel}} \sim 220$  °C for FeMn). In the region below 100 ns, a much lower heating power is required for the MRAM cell comprising FeMn than for its IrMn counterpart. In contrast, in the longer timescale, the heating write power densities are comparable for FeMn and IrMn. It is also evident that lower AF thickness results in lower write power density, i.e., blocking temperature, and this difference is maintained throughout the whole measurement range. The use of FeMn together with thermal barriers opens a way to reduce the write power density close to 5 mW/μm² and current densities in the 1E5 A/cm² range. This low write density can be combined with low switching fields, with values as low as 20 Oe having already been demonstrated. In conventional field write approaches such low switching fields



**Fig. 2.20** *Left*: principle of the two pulses experiment for determining the cooling rate of TA-MRAM cells. *Right*: write power required for writing with a second pulse of current (3 ns long) after application of a first heating pulse (7 ns long), the two pulses being separated by a varying delay. The experiment was carried out on a stack with thermal barrier. The derived characteristic cooling time is 14 ns

would result in unstable cells, but in the thermally assisted approach, an additional term is added to the energy barrier separating the two stable states. The energy barrier has an additional energy term corresponding to the exchange anisotropy energy which is temperature dependent as  $E_{\text{ex}}(T) = (J_{\text{ex}} / (M_s^2 t)) (1 - T/T_b)$ , where  $J_{\text{ex}}$  is the exchange constant,  $M_s$  the saturation magnetization of the pinned layer ferromagnet,  $t$  its thickness,  $T$  the temperature, and  $T_b$  the blocking temperature. When the system is in standby (i.e., not during a write event), this term provides additional thermal stability. Therefore it is possible to combine low writing fields once above the blocking temperature and good thermal stability of the cells.

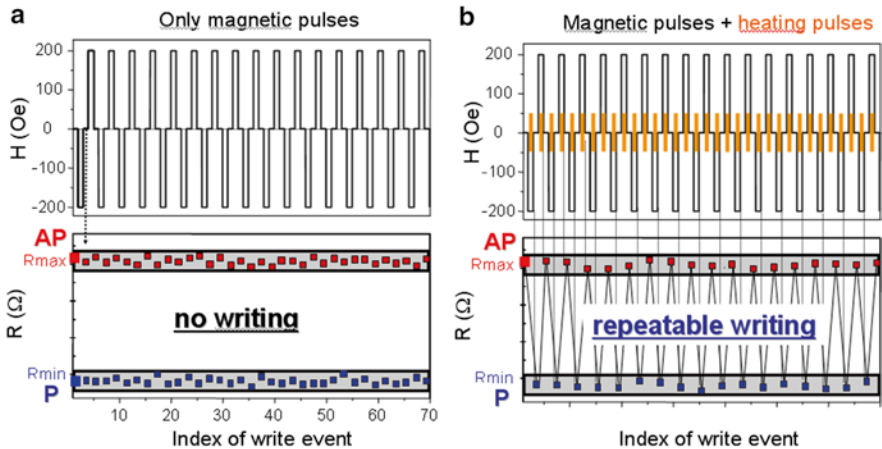
In conventional MRAM architecture the writing time required for the alignment of the storage layer along the applied field is about 3–7 ns [54, 55]. The TA-MRAM write cycle should match these values to be competitive compared to conventional magnetic field-induced switching MRAMs. The heating and cooling dynamics determine the total duration of the write cycle and speed at which cells can be rewritten. The heating dynamics can be investigated using the storage layer writing power density as a measure of the pillar temperature. The cooling time of pillar can be measured through a sequence of applied pulses [56]. A first pulse is applied to the junction resulting in a temperature increase. A second pulse is then applied at increasing delay after the initial pulse. The second pulse also results in a temperature increase that adds to the remaining temperature increase from the first pulse. If the time interval between the two pulses is long enough for the temperature to completely decay to the initial temperature value, the second pulse requires a write power density equal to that for a single isolated pulse. If this interval is shortened, a decrease in write power density is observed. The lowest power density is obtained when both pulses are consecutive. This process is illustrated in Fig. 2.20. From the write power density evolution, the characteristic cooling/heating time constant  $\tau$  of the cell can be determined. Typical values for this time constant are 4–6 ns in cells without thermal barriers and 14–16 ns in cells having a thermal barrier.

### 2.2.2.3 Write Selectivity and Protection Against Stray Fields

One unique feature of the TA-MRAM approach is that the layer stack used has already some protection against stray magnetic field erasure. This means that, due to the exchange biasing of the storage layer, the P and AP resistances remain unchanged, even if the MTJ is subject to magnetic field perturbations. This protection against magnetic erasure can be demonstrated by applying a magnetic perturbation field and then measuring the resistance state after the perturbation field is turned off. Without a heating pulse, both P and AP states are stable and insensitive to magnetic field perturbations. This offers a high protection against stray magnetic fields even in the absence of any magnetic shielding [57]. Selective writing of the memory cell can only be achieved by applying simultaneously a current pulse and a magnetic field. The memory cell then changes its resistance state each time between two well-defined resistance levels corresponding to the P and AP states as illustrated in Fig. 2.21.

### 2.2.2.4 TA-MRAM with Soft Reference Layer

In another embodiment, TA-MRAM can be implemented with still an exchange-biased storage layer but a soft reference layer. This means that instead of using an exchange-biased reference layer pinned by a high Néel temperature antiferromagnet (such as PtMn), the reference layer is made of a soft magnetic material. The writing process is the same as before. However, the reading is different. The reading is here a four-step process. The soft reference layer is first written in a predetermined



**Fig. 2.21** Illustration of the write selectivity in TA-MRAM resulting from the combination of heating pulse and application of a magnetic field. *Left*: application of pulses of magnetic field alone—no writing. *Right*: Combination of heating pulse and alternating pulses of magnetic field—repeatable writing of P and AP (0 and 1) magnetic states

direction by application of a first pulse of magnetic field (without heating pulse so as not to write the storage layer). Then the resistance of the MRAM cell is measured. Then the soft reference is written in the opposite direction and the new resistance is measured. If the second resistance value is higher than the first one, this implies that the first state was the parallel magnetic configuration so that the storage layer was pointing in the first predetermined direction. On the contrary, if the second resistance is lower than the first one, this means that the magnetization of the storage layer is pointing antiparallel to the first predetermined direction of application of the field.

The drawback of this embodiment is a slower reading process. The advantage however is that each cell is self-referenced so that the constraints on homogeneity of cell to cell resistance and magnetoresistance amplitude are much released.

Finally, it is interesting to note that in the field of magnetic recording technology (magnetic hard disk drive technology), there is also a very intense on-going R&D effort to develop heat-assisted magnetic recording. This is one of the routes investigated for maintaining the pace of increase of storage areal density in hard disk drives. In magnetic recording the application of the local write field is combined with a local heating produced by a near field plasmonic antenna. The physics in terms of thermal stability and write field amplitude is quite similar to that of TA-MRAM although the technologies involved are fairly different.

### ***2.2.3 First Generation of Spin-Transfer Torque MRAM***

The prediction of STT phenomena by Slonczewski [11, 12] and Berger [13, 14] in systems comprising two magnetic layers separated by a nonmagnetic layer has brought a renewed interest for MRAM applications. First, the possibility to write the storage layer using the sole current flowing through the MTJ is very attractive to reduce the write power consumption as high energy was required to produce the large magnetic field necessary to switch the bit both in SW and toggle write modes. Second, the STT write concept is intrinsically scalable as the switching current scales with the MTJ area; thus provided the MTJ can comply with the stability criteria at low dimensions, STT-RAM can be miniaturized down to very small technological nodes. Last, the suppression of the digit line allows designing much more compact cells with footprints competitive with other nonvolatile or volatile technologies.

The very first observation of STT switching in a spintronic system was performed by Myers et al. in a Co/Cu/Co trilayer where a local point contact was processed on the top magnetic electrode [58]. Despite clear evidence of Spin-transfer-induced switching was demonstrated in this report with both directions of the current, the required switching current density was very large over  $10^9$  A/cm<sup>2</sup>. As the magnetic layers had a much wider extension than the local point contact, the in-plane magnetic stiffness made the reversal of a local domain in the storage layer more difficult to achieve. A very high spin-polarized current density was thus necessary to switch locally the magnetization of the storage layer, and a bistable

configuration could be maintained at zero current only when the layer was thin enough. When the storage layer was too thick the written domain could not be maintained when the current was swept down due to the large intralayer coupling. More stable and reproducible results could be achieved when all the layers and the contact were patterned in a pillar-like shape [16]. Moreover, the switching current density was found to be at least one order of magnitude lower than in the point contact systems, simply because in this experiment, the spin-polarized current is incident on the storage layer and the current lines do not spread over the extended layers.

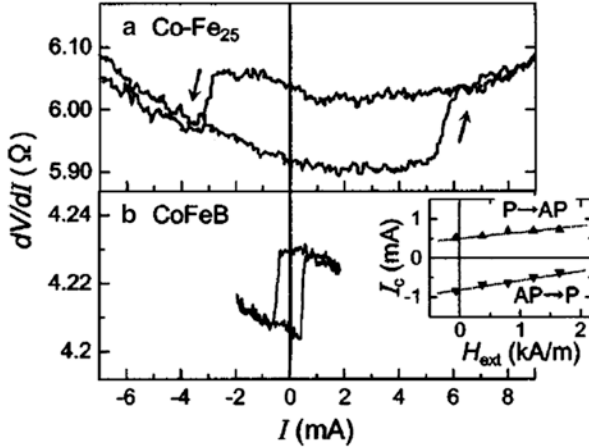
According to the STT theory [59], the critical current densities can be written in the form (CGS Units)

$$J_{cP \rightarrow AP}^+ = \frac{1}{\eta} \left( \frac{2e}{\hbar} \right) \alpha M_s t (H + H_k + 2\pi M_s)$$

$$J_{cAP \rightarrow P}^- = \frac{1}{\eta} \left( \frac{2e}{\hbar} \right) \alpha M_s t (H - H_k - 2\pi M_s)$$

$\eta$  is the spin polarization efficiency  $\eta = (p/2)/(1 + p^2 \cos \theta)$  in which  $p$  is the polarization of the magnetic electrodes and  $\theta$  the angle between the two magnetizations of the reference and storage layers.  $\alpha$  is the Gilbert damping constant,  $H_k$  is the effective anisotropy including both the intrinsic anisotropy and the shape anisotropy and  $2\pi M_s$  represents the out-of-plane demagnetization factor. The switching occurs when  $I_s > I_c^+$  for the transition from the parallel state (P) to the antiparallel state (AP) or when  $I_s < I_c^-$  to write from AP to P states. In most magnetic systems under study, the out-of-plane demagnetization term is always far above the effective anisotropy which means that the shape of the bit has very minor impact of the switching current ( $I_s$ ). This is in strong contrast with the field-induced magnetic switching (FIMS) approaches for which the shape had a strong influence on both the write current dispersion and intensity. From the above equations, one can readily observe that there are three main possibilities to reduce the critical current density (1) decrease the magnetization of the storage layer, (2) decrease the thickness of the storage layer, or (3) increase the polarization efficiency. Other more complex techniques have also been proposed recently and will be discussed in the following sections, in particular involving materials with out-of-plane magnetization.

One of the first attempts to reduce the critical current density for writing was proposed by Yagami et al. who proposed to replace the 2.5 nm CoFe<sub>25</sub> storage layer by a 2 nm thick CoFeB layer the  $M_s$  of which is only 40 % of the CoFe magnetization [60]. The study was performed on pseudo-spin valve structures of the form CoFe(10 nm)/Cu(6 nm)/storage. Using CoFeB storage layer,  $J_c$  was one order of magnitude lower than for CoFe one (see Fig. 2.22). However, decreasing the  $M_s$  of the layer also impacts the thermal stability of the layer for these in-plane magnetized materials. Indeed, the thermal stability is ruled by the  $KV/k_B T$  ratio where  $K$  is the effective anisotropy of the layer dominated here by the in-plane shape anisotropy. When CoFe was replaced by CoFeB the coercivity of the layer (which can be assimilated to the anisotropy in single domain bits) dropped from 400G to 170G leading to a  $KV/k_B T \sim 28$  which is insufficient to guarantee 10 years data retention.

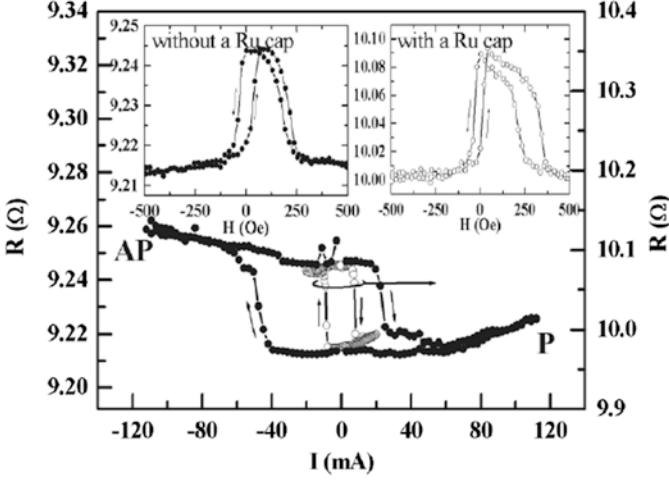


**Fig. 2.22** Change in differential resistance ( $dV/dI$ ) for DC injected currents for two storage layer compositions. The *inset* in (b) corresponds to the variation of the  $I_c$  with an applied external field (from [60])

This decrease of the effective anisotropy can be compensated simply by changing the aspect ratio of the bit. Thus elongating the bit from an aspect ratio (AR) of 1.5 to 2.6 is sufficient to recover a  $KV/k_B T \sim 70$ . As discussed previously the change of shape has a very minor effect on  $J_c$ . For MRAM application, the use of low  $M_s$  materials is a good strategy, especially as the thermal stability can be recovered by adjusting the shape of the element with minor penalty on  $J_c$ .

Another interesting attempt to reduce  $J_c$  is the use of a synthetic antiferromagnetic (SAF) storage layer. In such system the effective  $M_{st}$  can be strongly reduced while the magnetic volume is kept large ensuring a good thermal stability [61, 62]. Using a SAF storage layer is much more efficient than simply reducing the layer thickness which would inevitably led to a poor  $KV/k_B T$  ratio. A further advantage of using a SAF storage layer is the more homogeneous internal field within the magnetic layers due to flux closure between the two antiparallel layers constituting the SAF. This improved homogeneity of the internal field yields a more reproducible STT switching and correlatively narrower distributions in write current. This approach can be combined with the use of low  $M_s$  materials.

The last approach consisted in trying to improve the spin polarization efficiency in spin-valve structure by inserting a material with large spin scattering effect on top of the storage layer in order to improve the spin polarization inside the region of interest due to a modification of the spin accumulation landscape. This effect has been observed in an exchange-biased spin-valve structure by the group of Jiang et al. [63]. Comparing two structures of the form  $\text{Cu}(20 \text{ nm})/\text{IrMn}(10 \text{ nm})/\text{CoFe}(5 \text{ nm})/\text{Cu}(6 \text{ nm})/\text{CoFe}(2.5 \text{ nm})/\text{Ru}(d)/\text{Cu}(5 \text{ nm})/\text{Ta}(2 \text{ nm})$  with  $d=0$  or  $0.45 \text{ nm}$ , they observed one order of magnitude difference in  $J_c$  from  $2.10^8 \text{ A/cm}^2$  to  $2.10^7 \text{ A/cm}^2$  thanks to the addition of the Ru capping layer above the storage layer (see Fig. 2.23). Similar behavior can be observed with FeMn material which is also a strong spin scattering layer [64].



**Fig. 2.23**  $R(I)$  curves for two Spin-valve structures comprising a thin Ru cap layer (white symbols) or not (black symbols). Insets are the  $R(H)$  loops of the same structures (from [63])

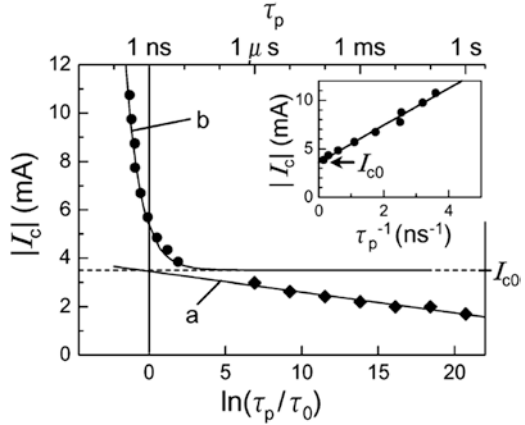
Another interesting feature of the STT switching is that it is also a thermally activated process similarly to the SW or toggle switching but with qualitatively different behavior. The first observation of this thermal activation was given by Myers et al. [65], when they observed in their Co/Cu/Co structures that  $J_c$  was increasing when temperature was decreased or when the current sweeping rate was increased. Actually depending on the current pulse duration ( $\tau_p$ ), two distinct regimes could be observed. For  $\tau_p$  shorter than few ns, the system is in a quasi-adiabatic regime meaning that the STT is not assisted upon writing by thermal fluctuations to overcome the energy barrier separating the two magnetic states. The energy to provide is thus constant which means that  $J_c$  is inversely proportional to  $\tau_p$ . In this first regime the critical current density is expressed as [66]

$$J_c = J_{c0} \left( 1 + \frac{\tau_{\text{relax}}}{\tau_p} \ln \left( \frac{\pi/2}{\theta_0} \right) \right)$$

where  $J_{c0}$  is the critical current density at 0 K,  $\tau_{\text{relax}}$  is the relaxation time of the magnetization ( $\sim 0.5$  ns), and  $\theta_0$  is the initial small angle of the magnetization due to temperature-induced magnetization fluctuations  $\theta_0 \sim \sqrt{k_B T / KV}$ . The asymptotic limit of  $J_c$  in this first regime is  $J_{c0}$  when  $\tau_p \gg \tau_0$ , i.e., in quasi-static measurements. When  $\tau_p$  is larger than  $\tau_0$  then the switching is dominated by the thermal effect and the critical current density is expressed as

$$J_c = J_{c0} \left( 1 - \left( \frac{k_B T}{KV} \right) \ln \left( \frac{\tau_p}{\tau_0} \right) \right)$$

**Fig. 2.24** Critical current for switching from AP  $\rightarrow$  P states as a function of current pulse duration  $\tau_p$  (from [67]). The region labelled a corresponds to the thermally activated regime while the region labelled b is the quasi-adiabatic regime

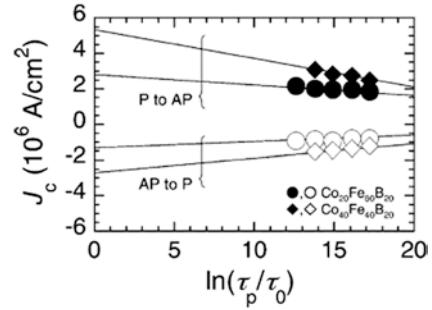


When  $\tau_p = \tau_0$  then  $J_c = J_{c0}$ , this is where the two regimes overlap as shown in Fig. 2.24. In order to compare the performance of different structures, the authors often refer to the  $J_{c0}$  value that is a good metrics. From the above equation, one can see that in the thermally activated regime—which is the regime of use in most MRAM applications— $J_c$  is inversely proportional to the thermal stability criteria which means that it is impossible to optimize both the thermal stability and  $J_c$ .

Following all these attempts to reduce the critical current densities, researchers have tried to transfer the STT write mechanism from pure metallic systems that were incompatible with MRAM applications to MTJ systems. The main issue was to adapt the MTJ resistance area (RA) product to withstand the high current density required to switch the magnetization of the storage layer without breaking the fragile oxide barrier. For  $J_c \sim 10^7$  A/cm<sup>2</sup>, the RA value should be as low as few  $\Omega \mu\text{m}^2$  to keep the voltage drop across the junction below 0.3 V. Fuchs et al. were the first to demonstrate STT switching in Al-O<sub>x</sub>-based MTJ having an RA between 1 and 4  $\Omega \mu\text{m}^2$  and a modest TMR of  $\sim 10\%$ . The storage layer consisted of a 2 nm thick low  $M_s$  CoFeB materials in order to minimize  $J_c$ . The switching occurred similarly to the metallic systems and they observed that the  $J_c$  per unit of layer thickness was about  $\frac{1}{2}$  to  $\frac{1}{3}$  of the value reported for spin-valve structures [68]. This difference was attributed to the higher spin-transfer efficiency in MTJ compared to spin valves. This explanation was confirmed later in another set of experiments comparing the performances of STT between MTJ made either from Al-O<sub>x</sub> or MgO barriers. Huai et al. could demonstrate that  $J_{c0}$  was varying inversely with  $(\text{TMR})^{1/2}$  and thus that large TMR systems had larger spin-transfer efficiency  $\eta$  [69]. In this study the MTJs were composed of a synthetic reference layer and simple storage layers made of 2.5 nm of CoFeB. The MgO-based MTJs exhibit a TMR of 150% with an RA of 50  $\Omega \mu\text{m}^2$  whereas the Al-O<sub>x</sub>-based MTJs had 25% TMR with an RA of 15  $\Omega \mu\text{m}^2$ . The  $J_{c0}$  was found drastically different with 2–3 MA/cm<sup>2</sup> for MgO barriers and 5–12 MA/cm<sup>2</sup> for Al-O<sub>x</sub> barriers reflecting the primary importance of  $\eta$  for the STT performance.



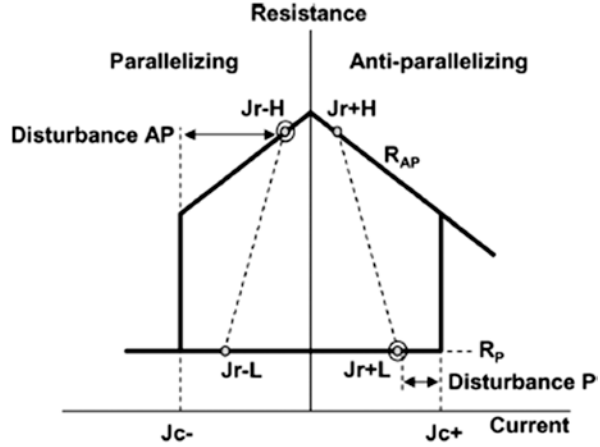
**Fig. 2.25**  $J_c$  as a function of  $\ln(\tau_p/\tau_0)$  for MTJ with SAF storage of two different compositions (from [71])



Finally, MgO-based MTJs incorporating a synthetic ferrimagnetic layers have been developed and evaluated for STT-RAM application [70]. The storage layers were composed of a trilayer  $\text{CoFeB}(t_1=2 \text{ nm})/\text{Ru}(x)/\text{CoFeB}(t_2=2 \text{ nm})$  where  $x$  was varied from 0.6 nm to 3 nm to probe the different RKKY interactions, i.e., ferromagnetic or antiferromagnetic couplings. From the experiments, it appears that the SAF storage layer with strong RKKY coupling gives the lowest  $J_{c0} \sim 5 \cdot 10^6 \text{ A/cm}^2$  while SyF with ferromagnetic coupling has higher  $J_{c0} \sim 1.1 \cdot 10^7 \text{ A/cm}^2$ . Combining very low  $M_s$  materials and SAF storage layer has led to remarkably low  $J_{c0}$  of 2 MA/cm<sup>2</sup> (see Fig. 2.25) compatible with MRAM implementation with acceptable RA level to guarantee large TMR [71].

STT-RAM developments have progressed a lot during these last years. As explained previously, STT-RAMs have some interesting features with respect to SW-MRAM or Toggle-MRAM, especially in terms of write power consumption and scalability. With  $J_c \sim 2 \text{ MA/cm}^2$  the switching current can be as low as 200  $\mu\text{A/bit}$  for a 100 nm diameter bit while the RA of the MTJ can be  $\sim 50 \Omega \mu\text{m}^2$  for a write voltage of  $\sim 1 \text{ V}$  which is safe in terms of MTJ reliability for short write current pulses (a few ns). The STT-RAM concept suffers however from two main difficulties (1) writing the bit requires the use of bipolar write current through the junction and (2) a read current can create a disturbance of the written state. The first point is solved by using a specific design based on switchable current source and sink at each cell, to allow propagating downward and upward currents in the bit [72]. In order to explain the strategy to minimize the read disturbance, one has to remember that each direction of the current favors a single state. For example, positive  $J_c$ , where current flows upward so the electrons flow from the storage layer to the reference layer favors an antiparallel alignment of the magnetizations. When the bit lies in the AP state and a positive read current ( $J_r$ ) is applied there is no possible disturbance as the read current stabilizes the AP state. If the bit lies in the P state, a positive  $J_r$  could conversely create a disturbance as shown in Fig. 2.26 [72]. The disturbance margin is determined by the difference of the read current ( $J_r$ ) and the critical current ( $J_c$ ). For a defined read voltage, the read current is much larger in the P state than in the AP state due to the difference of resistance between these two states. As a quite large read voltage is required to achieve high speed operation, the disturbance margin for positive read current can be small and there is a risk of soft errors. On the contrary if one uses a negative read current which stabilize the P state, the disturbance margin is much larger. Indeed, in this case, the margin is given by

**Fig. 2.26** Explanation of the read disturbance effect in STT-RAM chip (from [72])



the distance between  $J_r$  and  $J_c$ , corresponding to the critical current for the transition from AP to P state. As the resistance in the AP state is large,  $J_r$  is small compared to  $J_c$  even for a large read voltage. This margin is even larger if the TMR is increased as the read current in AP state will be even smaller.

Hitachi has produced a 2 Mb demonstrator chip with a 0.2  $\mu\text{m}$  CMOS technology and MgO-based MTJ bits. In this chip they could demonstrate proper switching with 100 ns write time and 200  $\mu\text{A}$  write current. The read access was  $\sim 40$  ns and the read voltage was optimized as described previously to avoid any disturbance. This chip has been submitted to  $10^9$  cycles without degradation of the two states resistance. More recent studies have shown that write voltage in STT-MRAM chips can be maintained below 0.5V for pulse width of the order of 10ns. This write voltage is sufficiently low compared to the breakdown voltage for this pulse width ( $\sim 1.5\text{V}$ ) to insure a cyclability of  $10^{16}$  (10 to power 16) cycles.

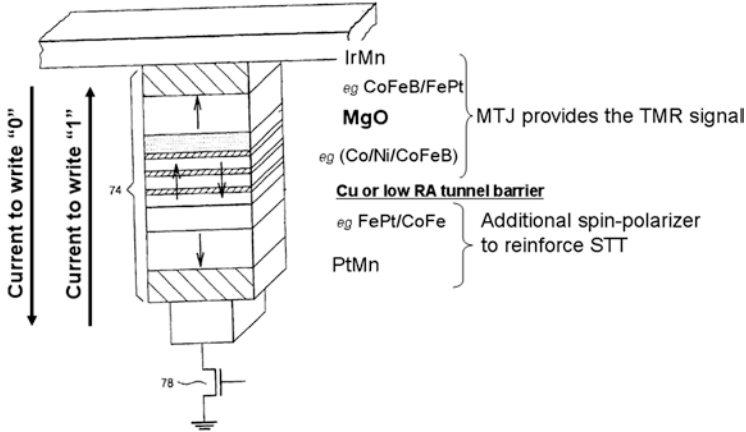
## 2.2.4 Advanced MRAM Concepts

### 2.2.4.1 Perpendicular STT MRAM

Devices that show a magnetic anisotropy normal to the film surface hold great promise towards faster and smaller magnetic bits in data-storage applications. They have many advantages compared to in-plane magnetized MTJs:

The switching current density is expected to be significantly reduced because the two terms present in the expression of the critical current density partially balance each other. In this configuration, the critical current density can be written

$$j_{\text{WRout-of-plane}} = \left( \frac{2e}{\hbar} \right) \frac{\alpha t_{\text{F}}}{P} (2K_{\text{eff}})$$



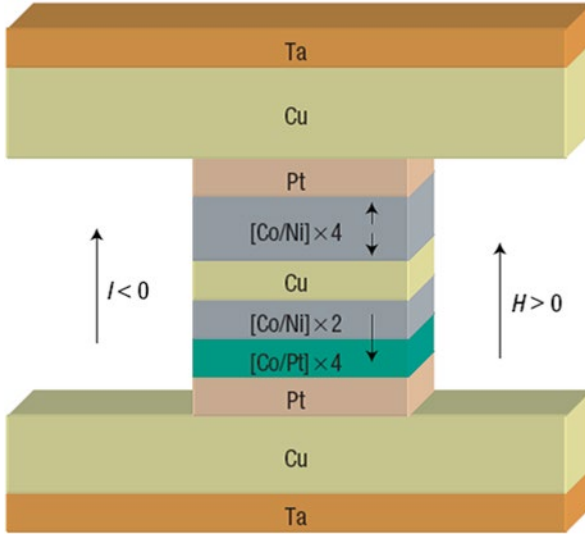
**Fig. 2.27** Improved STT-MRAM cell offering better thermal stability and reduced write current [48]

where  $K_{\text{eff}}$  represents the effective perpendicular anisotropy which takes into account the perpendicular anisotropy of bulk or interfacial origins minus the out-of-plane demagnetizing energy of the layer.

The thermal energy barrier is provided by this large effective perpendicular anisotropy instead of the in-plane shape anisotropy. For comparison, in MRAM systems based on field-induced magnetic switching, high coercive fields and large anisotropy were problematic. However, in STT-MRAM these same properties become an advantage, since they enable the thermal stability of magnetic elements beyond the 45 nm technology node. As a consequence, elongated cell shapes are no longer needed and perpendicular MTJs can use circular cells. This facilitates manufacturability at smaller technology nodes and leads to smaller switching current for a given critical current density (for a given minimum feature size, the circular area is smaller compared to elongated shape area).

Finally, dipolar field interaction between neighboring cells can also be reduced in high-bit density layout.

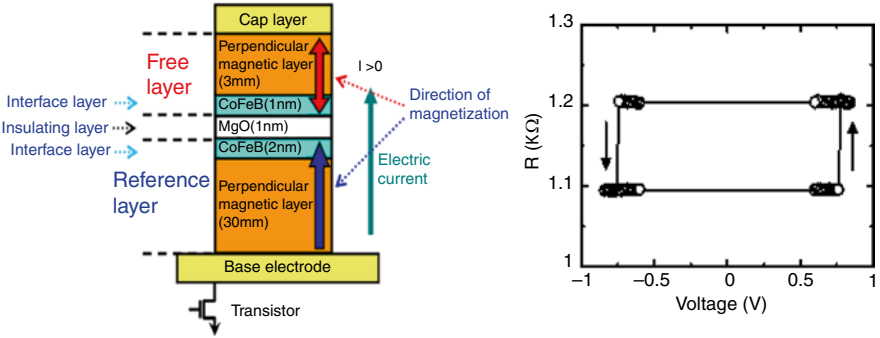
A detailed theoretical analysis of STT switching in MTJ with perpendicular anisotropy for 28 nm technology node has been presented at IEDM 2007 [73]. In order to further push the superparamagnetic limit, Spintec already proposed almost 10 years ago [48] to use MTJ stacks having perpendicular-to-plane magnetization and to increase the spin-torque efficiency by integrating in the stack two pinned layers on both side of the storage layer (see Fig. 2.27). These two pinned layers have opposite magnetization so that for both polarity of the current, there are additional contributions of the direct spin-polarized current originating from one of these layers and of the reflected spin-polarized current originating from the other. In addition, the two spacer layers separating the storage layer from the two pinned layers must have different resistance (RA product) to avoid compensation of their magnetoresistive effects. Therefore one can be a tunnel barrier whereas the other should be a metallic spacer or a tunnel barrier of lower RA than the first one.



**Fig. 2.28** Schematic representation of patterned Co/Ni samples. The reference layer is a composite  $[\text{Co/Pt}] \times 4 / [\text{Co/Ni}] \times 2$  multilayer and the free layer is a  $[\text{Co/Ni}] \times 4$  multilayer. The magnetization direction of the reference layer, positive field direction, and the direction of electron flow for negative current are shown (from reference [74])

The first experimental demonstrations of perpendicular STT switching have been realized in metallic spin-valve systems with out-of-plane anisotropy [74]. The authors used a  $(\text{Co/Pt})/(\text{Co/Ni})$  multilayer for the reference magnetization and either  $(\text{Co/Ni})$  or  $(\text{Co/Pt})$  as the free layer (see Fig. 2.28). The best results in terms of switching current density and GMR amplitude were observed for Co/Ni multilayers, which have higher giant magnetoresistance values and spin-torque efficiencies than Co/Pt multilayers. Pt is indeed known to have large spin-orbit interactions which induce spin-memory loss resulting in poorer performances. Critical currents for reversal of the magnetization of  $3\text{--}8 \times 10^7 \text{ A/cm}^2$  were obtained. They are comparable to many in-plane magnetized devices, which typically have lower coercive fields. These values however were larger than expected likely due to enhanced Gilbert damping values ( $\alpha$  in the preceding formula) in these perpendicularly magnetized systems as compared to their in-plane counterparts.

Presently there is a wide gap between in-plane and perpendicular anisotropy magnetic tunnel junctions as the STT understanding in MgO-based in-plane MTJs is more advanced as compared to perpendicular MTJs. However, the current interest for perpendicular MTJs and their implementation in MRAM are quite important and the field progresses quite fast. In state-of-the-art in-plane MgO tunnel junctions, TMR of 600 % was reported using CoFeB electrodes and annealing temperatures up to  $400 \text{ }^\circ\text{C}$  [8]. These large TMR signals occur because the spin-polarized electrons are filtered by the crystalline MgO barrier, according to their band symmetry. This additional filtering occurs when both electrodes on either side of the MgO present a



**Fig. 2.29** Cell structure of TbCoFe/CoFeB-based perpendicular MTJs (*left*) resistance versus voltage pulses for the perpendicular MTJ structure schematically shown at *left* (*right*). From [82]

body-centered-cubic (bcc) structure with the same crystalline orientation as the MgO one. The initially amorphous CoFeB adopts this structure upon annealing at temperatures above 300 °C, with a crystal nucleation starting from the MgO interface. Exactly this point is the challenge in the integration of perpendicular anisotropy materials with MgO barriers. Generally perpendicular anisotropy materials have a face-centered-cubic (fcc) structure, resulting in a greatly reduced TMR for MgO barriers.

Although the first realizations of perpendicular tunnel junctions used alumina barriers [75, 76], work has now focussed on crystalline MgO barriers. The most successful approach in perpendicular systems published up to now [77] has been using ordered FePt alloys as bottom and top electrodes, with a TMR ratio of 100 %. Systems based on rare earth alloys (TbCoFe, GdCoFe) are also promising, with TMR ratio of 64 % [78] and 78 % [79]. The major drawback of such structures is their poor thermal stability. Multilayered (Co/Pt)- or (Co/Pd)-based structures are more thermally stable, but show somewhat lower performances (10–30 % TMR in mixed (Pd/Co)/MgO/(Co/Pt) structures [80], 10 % at Spintec for Pt/Co/MgO/Co/Pt structures). The most promising results recently presented [81] concern structures based on “mixed” electrodes, one consisting on ordered L10-FePt, and the other one on multilayered (Co/Pt), and using thin CoFeB layers in contact with the MgO barrier.

Toshiba has been first to present STT switching in MTJs with perpendicular anisotropy having a typical stack composed of TbCoFe/CoFeB/MgO/CoFeB/TbCoFe (as shown in Fig. 2.29) and patterned in a circular shape [82]. Electrical measurements have shown a low 15 % TMR while the critical currents extracted from switching curves at current pulse width ranged from 30 to 100 ns were in the range of  $5 \times 10^6$  A/cm<sup>2</sup>. Coercive fields 1.2 kOe give a large thermal stability  $\Delta = 107$ , large compared to less than  $40 k_B T$  of in-plane anisotropy cells at similar critical current densities.

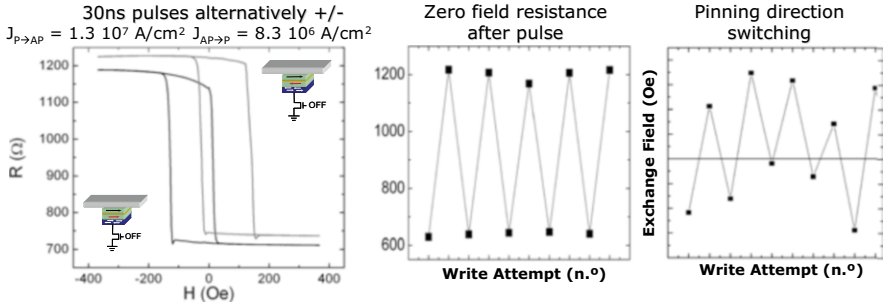
Lower critical currents of  $2.7 \times 10^6$  A/cm<sup>2</sup> and higher TMR of 60 % have also been demonstrated in MgO-based perpendicular MTJs consisting of CoFeB wedge/[Pd/Co]<sub>x2</sub>/Pd free layer and a FePt/CoFeB reference layer. This study revealed also that the damping parameter increases as the free CoFeB thickness is decreased. This means that better performance in terms of ratio of the switching current density to the thermal stability factor is obtained for thicker CoFeB layers.

More recently [83], critical switching current density as low as  $5 \times 10^5$  A/cm<sup>2</sup> has been reported in TbCoFe/CoFeB/MgO/CoFeB/L10-FePd structures. These results show that critical current densities close to or even smaller than  $1 \times 10^6$  A/cm<sup>2</sup> can be achieved in such perpendicular junctions. However, the most promising approach seems to rely on the use of the perpendicular anisotropy which exists at the interface between magnetic transition metal and oxide [122, 123]. Crossover for in-plane to perpendicular anisotropy in Pt/CoFe/AlO<sub>x</sub> as a function of the Al degree of oxidation: a very accurate control of the oxidation of tunnel barrier.

### 2.2.4.2 Thermally Assisted STT-MRAM

As previously explained, there are several advantages in using a thermally assisted MRAM concept, the main one being the decoupling of the thermal stability and the power consumption, since the bit can have simultaneously a low write field at the write temperature and be stable in the operating temperature range. The issue with the field-driven writing of TA-MRAM cells is that the magnetic field needs to be generated by a current line. TA-MRAM requires a single magnetic field and lower field values compared to the toggle MRAM approach, thus lowering the total power consumption. However, the write field does not scale with cell size and can be at best kept constant, unlike STT-RAM where the write current scales with cell size. Also, the heating current is not the bottleneck, since the use of thermal barriers has already demonstrated a heating current density in the  $1\text{--}2\text{E}6$  A/cm<sup>2</sup> range, similar to the lowest values of spin-transfer torque MRAM cells (STT-RAM). It is possible to still use the thermally assisted concept but to combine it with an alternative method to switch the storage layer once the cell is brought above the blocking temperature. This can be achieved by exploiting the STT effect to switch an exchange-biased storage layer [48]. In this case it is possible to combine the added stability obtained from the exchange biasing to retain the information with the reduction of the current through cell size scaling, since the cell switching occurs at a constant current density, typically in the  $1\text{E}6$  A/cm<sup>2</sup> range. The first demonstration of this concept was realized in 2009 [84]. The magnetic stack was Ta 3/CuN 30/Ta 5/PtMn 20/CoFe 2/Ru 0.74/CoFeB 2/MgO 1.1 natural oxidation/CoFeB 2/NiFe 3/IrMn 6.5/Ta 5 (thicknesses in nm) patterned to 140 nm diameter circular cells. The storage layer is pinned by IrMn and the hysteresis cycles show a pinning field of  $\sim 50$  Oe, as shown in Fig. 2.30.

The resistance state was switched between the low resistance and high resistance states by applying current pulses of alternating polarity across the junction. Each



**Fig. 2.30** *Left*: magnetoresistance loops showing the reversal of the exchange pinning direction after applying 30 ns pulses. The *inset* represents the exchange bias field after pulses of alternating current direction (*top*). *Center*: resistance at zero field after each pulse. The writing is reproducible in both directions with stable values for parallel and antiparallel resistances. *Right*: Exchange bias field after alternating write events

pulse first creates a temperature increase above the antiferromagnet blocking temperature. With the ferromagnetic layer no longer pinned, the spin-polarized current simultaneously exerts a torque on the ferromagnetic storage layer reversing its magnetization direction depending on the current direction. Once the voltage is turned off, the junction cools down and the antiferromagnet freezes the new ferromagnet direction. Figure 2.30 shows this writing process with 30 ns pulses applied in a sequence of positive and negative polarity resulting in a zero field resistance that is alternating between the low and high resistance states. Additionally, there is also a change in the storage layer pinning direction as can be seen from the alternating positive and negative exchange bias field values. The critical current density required for switching the exchange pinned layer was 8 and 13E6 A/cm<sup>2</sup>, respectively, for the antiparallel to parallel and the parallel to antiparallel transitions. Similar structures without exchange biasing resulted in critical current densities of 8 and 13E6 A/cm<sup>2</sup>, virtually identical to thermally assisted cells, meaning that the heating is not the limiting factor and that the exchange pinning does not increase the critical current density. The thermal stability barrier can be estimated by fitting the switching probability by the theoretical Néel–Brown relaxation expression for the STT switching [66] resulting in  $KV/k_B T = 80$ . This shows how the thermally assisted approach can benefit the STT-RAM concept. Many times the write current density is reduced by lowering the total magnetic moment of the storage layer, which inevitably leads to a lower thermal stability barrier  $\Delta E$ . Long-term data retention requires  $\Delta E > 40\text{--}60 k_B T$ , therefore low write current cannot be achieved by reducing the storage layer magnetization. The reduction of the storage layer magnetization can then only be compensated by a higher effective anisotropy using elongated shapes for in-plane magnetized materials, thus increasing  $\Delta E$  at the cost of the cell size and integration density. Therefore as long as the power density required to heat the storage layer can be achieved with a current density that is below the critical current density of STT, the thermally assisted STT concept represents an improvement over conventional STT concepts.

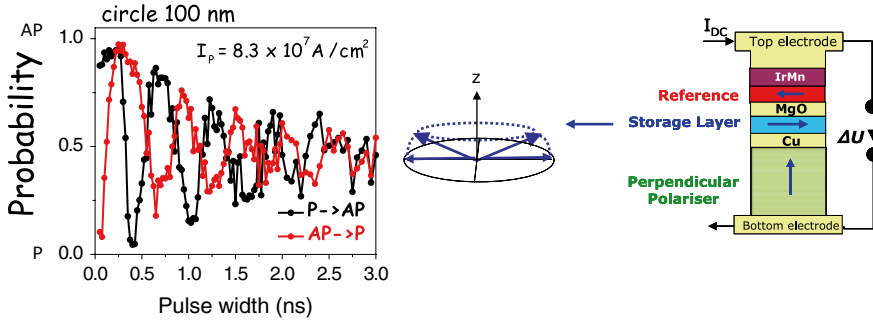
### 2.2.4.3 STT-MRAM with Perpendicular Polarizer

Until now the possibilities to reduce the power to write one cell have all concentrated on reducing the write threshold of critical current density or power density in thermally assisted concepts. This reduction actually reduces the current value that the selection transistor has to sink/drive, and therefore smaller transistor sizes can be achieved. Another possibility to reduce the total energy used to write one bit is to reduce the time that current/power needs to be applied to switch the magnetic configuration of the storage element. If the power/current density remains constant, reducing the pulse time from 20 ns to 0.2 ns reduces the total energy by a factor of 100. To achieve sub-ns switching times, it is possible to take advantage of the precessional motion of the magnetization around the effective field direction before it aligns itself with this direction. The precession frequency can be calculated from Kittel's formula  $(2\pi f/\gamma)^2 = 4\pi M_s \times H_{\text{eff}}$ , where  $f$  is the frequency,  $\gamma$  the gyromagnetic ratio,  $M_s$  the saturation magnetization, and  $H_{\text{eff}}$  the effective field. Typically  $f$  is in the GHz frequency range for common ferromagnetic materials.

The precessional switching approach had already been explored in magnetic field-driven switching concepts [85, 86]. In this case a magnetic field pulse was applied in the hard axis direction. The magnetization starts precessing around the hard axis direction and, by doing so, acquires an out-of-plane component. Even at small angles, this out-of-plane magnetization generates a large demagnetizing field in the out-of-plane direction, becoming the new dominant field direction. The magnetization then precesses around this out-of-plane field direction. At each half precession period the magnetization rotates by  $180^\circ$  and therefore changes from the initial magnetization direction to the opposite direction, all this at GHz frequencies. By properly timing the field pulse duration to stop at a half precession, it is possible to achieve sub-ns switching of the magnetization. In the magnetic field-driven precessional switching this half precession corresponded to 140 ps [85, 86]. Field precessional switching was not pursued in actual MRAM demonstrations, because the currents required to generate the hard axis field are large and cannot be scaled down by cell size reduction. Another problem is to randomly write a single cell in a matrix, since all cells along the current line would be switched. Adding an additional field created by a second field line could perhaps be used to achieve the write selection, but the whole write process would quickly become unmanageable in large arrays and with limited scaling perspectives.

Recently a more promising way to achieve precessional switching in the GHz range with real scaling possibilities was proposed [87, 88] based on spin-transfer oscillators. These spin oscillators use a perpendicular spin polarizer to induce the precession of an in-plane ferromagnetic layer, without external applied field [89]. In this case the precession frequency can be controlled by the current density flowing through the device. The demonstration of precessional switching was realized in full metallic current-perpendicular-to-plane GMR systems [88]. The structure in this case corresponded to a bottom perpendicular spin polarizer based on a Co/





**Fig. 2.31** Illustration of the concept of spin-transfer precessional switching. The stack (*right*) includes a perpendicular spin polarizer, the precessing storage layer, and the reference layer. This latter layer is aimed to convert the storage layer direction change into a resistance change. The *graph* shows how the probability of magnetic switching of the storage layer oscillates between parallel and antiparallel alignment as a function of current pulse duration with a frequency of GHz for a current density of  $8E6 \text{ A/cm}^2$

Pt multilayer separated from a NiFe 3/Co 0.5 nm storage layer by a Cu spacer. The reference layer was Co 3 nm pinned by an IrMn layer. The storage layer magnetization precesses around the normal to the layers for current densities higher than

$$j_c = \left( \frac{2e}{\hbar} \right) \frac{M_s t H_k}{g} \cdot 2$$

density up to a maximum equal to  $2\gamma M_s$ . Figure 2.31 illustrates this concept of the spin-transfer precessional switching.

The storage layer changes its magnetic orientation from the initial direction to the opposite  $180^\circ$  direction within 250 ps and back to the initial direction after 500 ps. The switching probability of the initial precession is 100 %, while for subsequent precessions there is a gradual lack of precession coherence, which is not detrimental to the application, since only the initial half precession is actually required to realize the switching. The precession can be induced by a current density of  $\sim 8E7 \text{ A/cm}^2$  and it is actually independent of the current direction. This is shown by the two different traces, one starting at the parallel configuration, while the other starting in the antiparallel configuration. This is important, since the transistor to be connected to these cells can be optimized for one current polarity. This means that higher currents per transistor lateral size can be achieved, ultimately allowing for smaller cells. The same switching process can be used with magnetic tunnel junction cells. Assuming that the same current density is required to achieve precessional switching in a magnetic tunnel junction having  $5 \Omega \mu\text{m}^2$  and  $0.01 \mu\text{m}^2$  area, this would yield a total energy to write a bit cell of 8 pJ. This concept of spin-transfer precessional switching can also be very interesting for nonvolatile logic applications for which speed is very important (see Sect. 2.3).

#### 2.2.4.4 Multibit MRAM Concepts

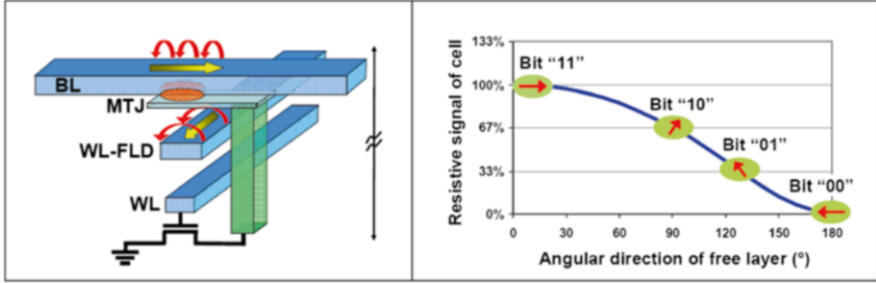
In order to be competitive with other types of memory devices, the memory density of MRAM chips must be increased. The common method to increase the memory density is by shrinking the cell size. A different approach is to create a multibit memory cell having more than 2 resistive states per given cell.

Various approaches have been proposed in the literature in order to obtain a multibit memory cell:

*By using a pair of memory cells at each intersection between word and bit lines [90]:* For achieving a multibit memory cell per intersection between the word and bit lines, the authors designed a pair of memory cells, used for a 2 bit per intersection architecture. The demonstration of the functioning of this type of architecture has been realized using finite element micromagnetic simulations. The proposed design allows the realization of a 2 bit or 4 bit memory per intersection, which can be used directly to reduce the number of word and bit lines on the memory chip.

*By using various shapes of the memory cell both for the conventional FIMS [91, 92] and toggle architectures [93].* Ju and Allegranza [93] proposed a multibit MRAM cell with toggle switching where the multibit stack consists again of multiple conventional toggle MRAM connected in series. All the cells in the proposed concept are identical except that their cell geometry, anisotropy, and pinned directions are presenting different orientations. The selectivity at write is ensured by using three phases of word and bit line current. This allows generating a contiguous magnetic field. Two-, four-, and six-bit toggle cell configurations are found to be feasible.

*By using a rotating field in a classical thermally assisted cell (TA-MRAM) with an exchange-biased storage layer [48].* In the TA-MRAM approach, the use of a circular shape eliminates the shape anisotropy term [94]. Furthermore, at the write temperature, the exchange anisotropy energy caused by the pinning of the storage layer by the antiferromagnetic layer is cancelled so that the barrier height for magnetization switching is reduced to the magnetocrystalline anisotropy energy. It should be stressed that the simple use of a circular geometry without using the approach of thermally assisted writing would not guarantee the required functionality because it would then be impossible to ensure a low power consumption together with thermal and temporal stability of the written bit. To achieve a multilevel capability, an additional word line (WL) can generate an in-plane vector field, as laid out in Fig. 2.32 [95]. This method allows the FL to be set into four different directions, thereby writing 2 bits into 4 different resistance levels as shown in Fig. 2.32. Using the crossed bit and word lines for field generation, a cell layout for the 2-bit cell ( $10F^2$  per 2 bits) shows a 70 % increase in bit density at 65 nm node, compared with two conventional cells. The data on multilevel switching clearly demonstrate the writing of four equidistant levels and their subsequent readout on MTJs smaller than 100 nm. By using an MgO-based stack with an MR of  $\sim 120$  % at an RA of about  $20 \Omega \mu\text{m}^2$ , the authors achieved a sufficiently large read window for four different states.



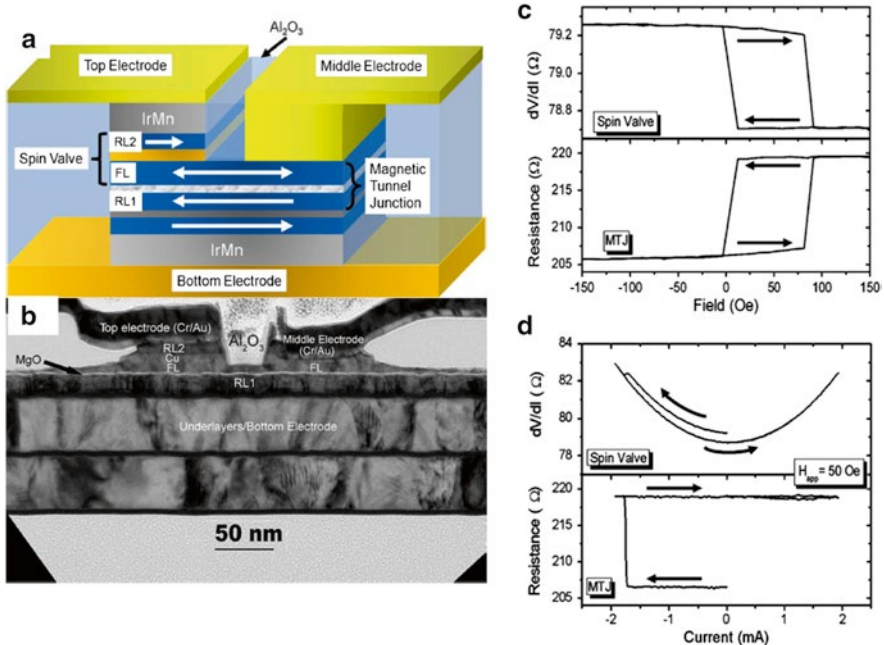
**Fig. 2.32** *Left:* schematic diagram of multilevel MRAM using an additional field generating word line (WL-FLD) under MTJ for 2 bits per cell operation. *Right:* angular dependence of the MR signal on the FL orientation. A 2-bit memory cell is defined by four different resistance states (MR levels). The multilevel information is stored in the angular orientation of the FL, which will be set by crossed WL and BL fields. The exchange bias is used to freeze in the angular information. The writing direction of intermediate states is set to equally space the levels

By using a double tunnel barrier in TA-MRAM [96] or in STT-MRAM [97] with critical currents different for each tunnel barrier. Redon [96] proposed a new multibit concept based on thermally assisted MRAM. The concept is based on the magnetostatic interaction between two adjacent storage layers separated by an antiferromagnetic exchange biasing layer combined with the use of a double tunnel barrier structure. The magnetostatic coupling between the two storage layers sets an antiparallel alignment of their two magnetizations when the temperature of the system exceeds the blocking temperature of the antiferromagnetic layer (see the working principle in the TA-MRAM paragraph, Sect. 2.2.2). The use of the magnetostatic coupling between ferromagnetic storage layers allows suppressing the second field line (see previous paragraph) which simplifies the architecture of the memory cell.

Multibit MRAMs may enable significant increase in memory density with modest increase in processing cost.

### 2.2.4.5 3-Terminals STT MRAM Concepts

One of the remaining hard points in the development of STT-MRAM is the long-term reliability of the tunnel barrier. Indeed, at each write event, the tunnel barrier is submitted to a pulse of voltage of the order of 0.7 V to 1 V. Since the barrier is typically 1 nm thick, this represents an electrical field across the oxide barrier of the order of  $10^9$  V/m which is approaching the values for which electrical breakdown of the barrier may occur. In order to circumvent this issue, several groups including Cornell, NEC, and Hitachi [98] have proposed concepts of three-terminal STT-MRAM cells in which the write current does not flow across the tunnel barrier thereby limiting the electrical stress during write.



**Fig. 2.33** Example of 3-terminal MRAM cell proposed by Hitachi [98]. (a): Schematic representation of the MRAM cell. (b): Cross-sectional transmission electron microscopy view of the device. (c): Simultaneous measurements of the spin-valve differential resistance response versus field (measured between the top and middle electrodes) and of the tunnel junction response (measured between the top and bottom electrodes). (d) Simultaneous measurements of the spin-valve differential resistance response versus current flowing from top and middle electrodes (measured between the top and middle electrodes) and magnetoresistance of the tunnel junction response (measured between the top and bottom electrodes)

One of the proposed concepts is illustrated in Fig. 2.33: Each MRAM cell consists of a magnetic tunnel junction having three electrical connections. One of the connections (named bottom electrode in Fig. 2.33) is as usual at the bottom of the cell and most often connects the bottom part of the MTJ (i.e., the underlayer of the antiferromagnetic pinning layer) to a selection transistor. In addition, two other contacts are connecting the top part of the MTJ, i.e., its storage layer. One of the contacts is made of a Cu spacer plus another pinned ferromagnetic layer. This contact together with the free layer of the MTJ constitutes a so-called spin-valve stack which exhibits GMR properties. This stack is connected to the so-called top electrode (see Fig. 2.33 left). The second top contact to the middle electrode is made of a simple nonmagnetic metal such as Cu and Al. Writing an information in the memory means, as for conventional MRAM cell, orientating the magnetization of the free parallel or antiparallel to that of the reference layer of the MTJ. This is achieved by sending a pulse of current between the top electrode and the middle electrode. This current flows through the top contact, then in the plane of the free

layer, then in the middle contact to the middle electrode. By traversing the pinned layer of top contact, the conduction electrons become spin polarized. They then exert a STT on the left extremity of the free layer which nucleates a reversed domain underneath the contact. At this point, the free layer is divided into two magnetic domains, one nucleated underneath the top contact and one in the original magnetization direction. These two domains are separated by a domain wall. Still due to spin-transfer effect, the current flowing in the free layer exerts a pressure on this domain wall which then propagates across the entire free layer leading to a complete switching of its magnetization. The magnetization can then be switched back by using a write current of opposite polarity. By this mechanism, the free layer magnetization can be switched without current flowing through the barrier.

The readout is performed as usual by sending a current from the top contact to the bottom contact and thereby measuring the resistance of the tunnel junction. This approach therefore allows for an ST writing scheme without tunnel barrier wear-out issues while retaining the benefits for readout of the large TMR signals from MTJs [98]. The drawback is of course the increased cell size due to the requirement of making two isolated contacts on top of each memory cell.

### ***2.2.5 Perspectives on MRAM***

The R&D on MTJ-based MRAM started in 1996 right after the discovery of TMR effect in MTJ at room temperature [3, 4]. Ten years later, a first MRAM product was shipped by Freescale. Since then, two major breakthroughs further boosted the development in the field and opened new perspectives to increase MRAM performances: one has been the discovery of giant TMR in crystalline MgO-based MTJ [5, 6] and the prediction and observation of spin-transfer magnetization switching [11–14, 16, 58]. With the development of perpendicular MTJ and of thermally assisted write schemes, it is more and more clear that high density STT-MRAMs will reach market soon. The field has progressed very fast between 2008 and 2010 and all major IC companies are intensifying their R&D on MRAM. There are still issues related to the magnetic back-end technology, especially the etching of these complicated MTJ stacks which is rather difficult. The reliability of the tunnel barriers still needs to be improved to reach the expected  $10^{16}$  cycles, but any new technology takes time to get stabilized. The outstanding work performed at Freescale and Everspin with the commercialization of their 4 Mbit then 16 Mbit MRAM chips has already shown that the integration of CMOS technology with back-end magnetic technology is possible, at least with field-induced writing. For STT writing, there are more constraints since three voltage distributions must be well separated across the MRAM chip: the distribution of breakdown voltages, the distribution of write voltages, and the distribution of read voltages. This is why further stacks optimizations and process developments are still required but the perspectives in terms of reachable density are much better with STT write scheme.

Compared to other technology of nonvolatile memories, MRAMs offer a set of unique qualities. Compared to FLASH, they have much higher cyclability. A value of  $10^{16}$  cycles is already achieved in the products from Everspin (MRAM written by field). For STT writing,  $10^{13}$  cycles has already been demonstrated and steady improvements are observed. This cyclability is also much better than in ferroelectric (FeRAM), phase change (PCRAM), or resistive oxide (RRAM) memories. In terms of speed, MRAM can be quite fast. Everspin MRAMs have a cycle time of about 35 ns. However, we have seen in Sect. 2.4.3 that, thanks to precessional STT switching, an MTJ can be written with current pulse as short as 100 ps [88]. This means that the speed limitation is not going to originate from the magnetic element itself but from the surrounding electronics. MRAM may not be as fast as the fastest SRAM but may reach speed comparable to the middle range SRAM and clearly faster than DRAM.

In terms of footprint, STT-MRAMs are quite compact. An MRAM cell consisting of a simple MTJ interconnected with a CMOS transistor has a footprint of about  $8F^2$ . This is larger than for NAND FLASH but comparable to DRAM and much smaller than SRAM.

In addition, MRAMs are immune to ionizing radiations which makes them also quite interesting for spatial applications.

Thanks to this unique set of characteristics, MRAMs should have a bright future in the memory arena especially as embedded memories. Furthermore, their speed, cyclability, and possibility to be grown above CMOS circuits make them also very attractive for innovative architectures in which logic and memory are much more intermixed than in conventional architectures. This is the topic of the next section.

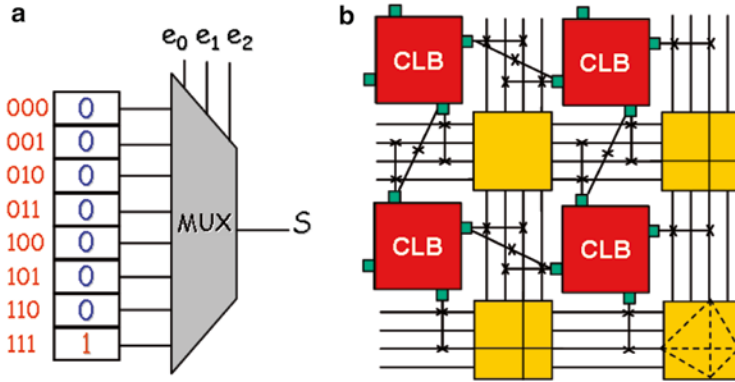
## 2.3 Beyond MRAM, CMOS/Magnetic Integrated Electronics

### 2.3.1 *From CMOS Electronics to Integrated CMOS/Magnetic Electronics*

#### 2.3.1.1 Power Consumption in CMOS Circuits

In the early 1960s, the first integrated circuits appeared, allowing integrating complex functions on the same die. Since then, the complexity and performances of circuits steadily increased following the well-known Moore's law. The latter predicted that the density and speed of integrated circuits would double every 18 months.

Several families of logic circuits exist nowadays. The ASICs (application specific integrated circuits) are designed and optimized to perform a given function (for example, a processor). Reprogrammable circuits are characterized by the fact that their functionality can be changed while keeping the same hardware. Due to their low cost, they are traditionally used for low-volume production or prototyping. But nowadays, new applications are emerging, such as the possibility to perform



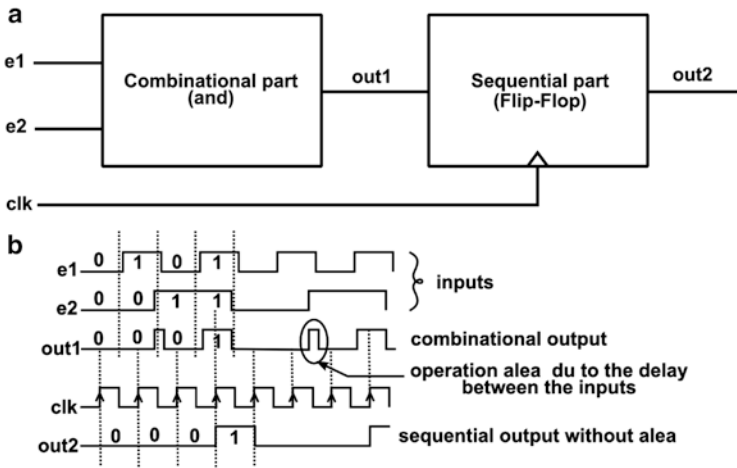
**Fig. 2.34** An elementary LUT (a) performing a “AND” logic function and a full FPGA composed of interconnected LUTs (b)

dynamically reconfigurable computing, i.e., to change the functionality of the circuit during operation to optimize the performance. The most popular reprogrammable circuits today are the FPGAs (field programmable gate arrays [99]) based on a matrix of programmable elementary functions, routed by a programmable system of interconnections (Fig. 2.34). An elementary logic function is called a LUT for look-up table (Fig. 2.34a). It consists of a configuration memory and a multiplexer. The values of the inputs “ $e_1$ ,” “ $e_2$ ,” and “ $e_3$ ” define the address of a memory cell, the value of which is routed to the output. In the example presented here, we see that only the combinations of inputs “ $e_1$ ”= ‘1,’ “ $e_2$ ”= ‘1,’ and “ $e_3$ ”= ‘1’ yields ‘1’ as output. The programmed function is therefore a 3-inputs “AND” logic gate. An  $n$ -input LUT requires a  $2^n$ -bit configuration memory and can perform any of the  $2^{2n}$

possible  $n$ -input functions. A LUT is integrated in an elementary CLB (configurable logic bloc). These CLBs are interconnected by means of interconnection blocks which are also programmable (Fig. 2.34b). The functionality of the circuit is thus stored in a configuration memory. FPGAs are generally based on SRAM or Flash memories. SRAM-based FPGAs are easy to reconfigure in terms of speed and power consumption. They can be used to perform dynamically reconfigurable computing. However, the configuration memory being volatile, an additional nonvolatile memory is required to permanently store information. Flash-based FPGAs are intrinsically nonvolatile, but they are slow and power consuming when writing. This does not allow dynamic reconfiguration. An MRAM-based FPGA can mix the advantages of these two kinds of FPGAs yielding a high-speed, low-power, and nonvolatile FPGA [100].

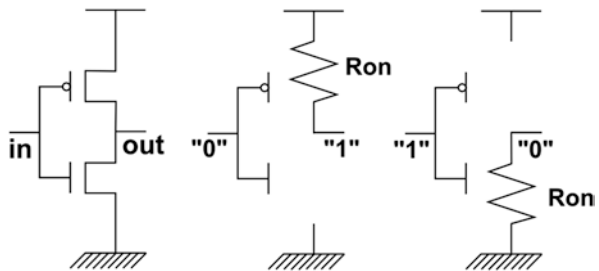
Logic circuits are typically based on a combinational part and a sequential part. The outputs of the combinational part change as a function of the inputs. Due to the different delays in the different paths of the circuits, errors may occur when the inputs do not change at the same time. To avoid these problems, a sequential part is used to synchronize the circuit at a clock rate (Fig. 2.35). The sequential part is





**Fig. 2.35** A logic circuit composed of a combinational and a sequential part (a) and the resulting timing diagram for a simple “AND” logic function (b)

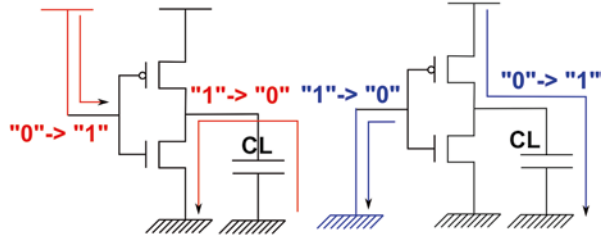
**Fig. 2.36** Principle of operation of a CMOS inverter



typically composed of Flip-Flops, memory elements which validate an input to the output on a clock edge. Figure 2.35a shows an example of a 2-input “AND” function. The output of this gate is connected to a Flip-Flop. Figure 2.35b shows the timing diagram: due to the delay between the inputs “ $e_1$ ” and “ $e_2$ ,” soft errors (area) may appear in “ $out_1$ .” The “ $clk$ ” signal is used to validate the output once all the inputs are stabilized, so that the signal “ $out_2$ ” does not suffer from this problem. We understand here that the maximum frequency of operation of the circuit (clock frequency) is determined by the delays in the circuit. Besides the distributed memory elements constituted by the Flip-Flops (containing the active data of the circuit), a memory is required to store the results of the calculations and the instructions of the codes. In the case of processors, two main architectures exist: the von Newman architecture, where the same memory contains the data and the instructions and the Harvard architecture in which the data and instructions memories are separated. In any case, logic and memory remain separate parts of the circuit.



**Fig. 2.37** Dynamic power consumption in a CMOS inverter



Nowadays, the design of digital circuits is based on CMOS (complementary metal oxide semiconductor) technology: each circuit consists of a stage of NMOS transistors and a stage of PMOS transistors, the two stages never being “on” at the same time. Figure 2.36 shows an example of a simple CMOS inverter. An inverter is used to perform the most simple logic operation, i.e., changing a logic ‘1’ into ‘0’ and vice versa. When the input signal is ‘0’ (low voltage level), the NMOS transistor is “off,” while the PMOS transistor is “on” with a parasitic  $R_{on}$  resistance. Since no current flows through the inverter, the output voltage is equal to the power supply voltage which codes a logic ‘1.’ Following the same principle, a logic ‘1’ at the input yields a ‘0’ at the output. This complementary design technique is widely used because it has theoretically no static power consumption and a very good stability. However, CMOS technology reaches physical limits and the Moore law begins to get out of breath: the increase of density and clock speed results in heating issues and huge power consumption.

Power consumption in CMOS circuits has several origins and can be separated in dynamic and standby power consumptions. The dynamic power consumption is the power required to perform the logic operations of the circuit. It results from the current required to charge and discharge the parasitic capacitances of the circuit (Fig. 2.37) and of the short circuit current: when the state of a logic circuit changes from a logic state to another, it goes through an intermediate state where the two stages of transistors are driving current together. This results in a peak of current flowing from the power supply  $V_{dd}$  to the ground  $G_{nd}$  through the inverter. Figure 2.38a shows the simulated result of the transient regime for a simple inverter: From top to the bottom, the figure shows the input of the inverter, its output, and the current flowing through it. Figure 2.38b shows a zoom on the switching event where we can clearly see the pulse of short circuit current. The dynamic power consumption is given by  $P_{dyn} = (C_L V_{swing} V_{dd} + V_{dd} I_{short-circuit}) f_{clk} \alpha$ .  $C_L$  is the full load capacitance of the gate (comprising the load capacitance of the gate itself and the input load capacitance of the next stage),  $V_{dd}$  is the supply voltage,  $V_{swing}$  is the output signal swing range (which is equal to  $V_{dd}$  in classical CMOS design techniques), and  $I_{short-circuit}$  is the current flowing through the gate during switching events. The first part of the expression represents the power required to charge  $C_L$  during a switching event and the second one represents the power lost by short circuit effect. The average power consumption is obtained by multiplying the result by the clock frequency  $f_{clk}$  and an activity factor  $\alpha$ .

The standby power consumption exists as soon as the circuit is powered, even when it is not performing any operation. It essentially results from the leakage

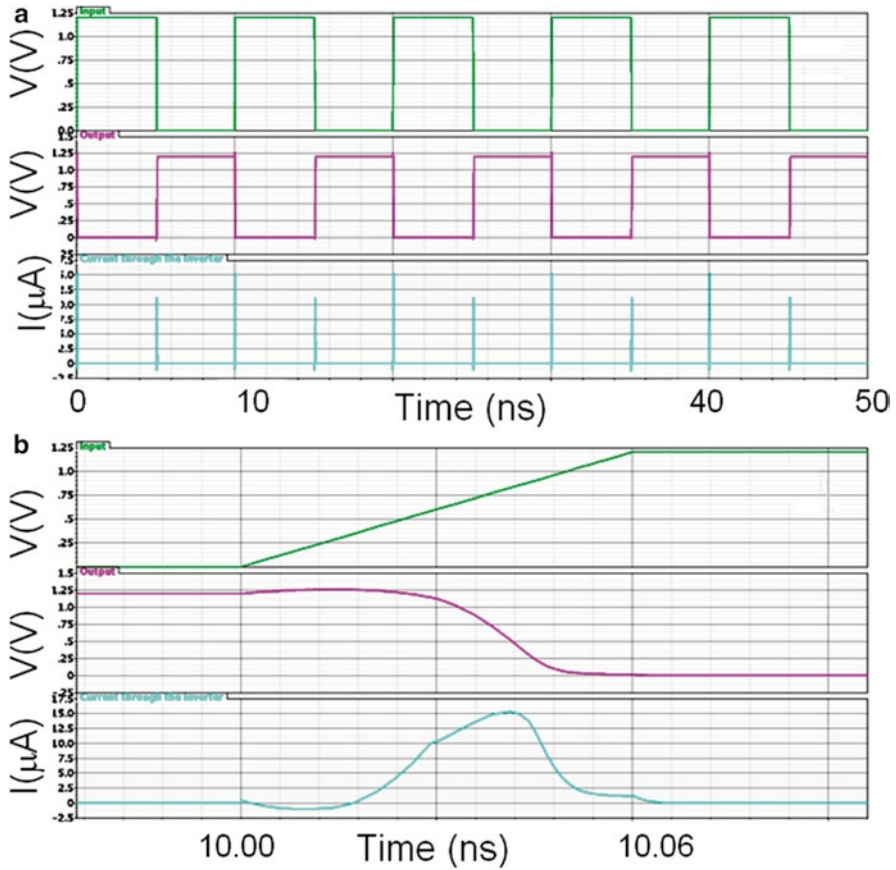


Fig. 2.38 Short circuit current during a switching event in a CMOS inverter. Transient simulation of the inverter (a) and zoom on a switching event (b)

currents of transistors [101]. The main contributions to the leakage are the gate tunnelling current, the subthreshold current, and the inverse diode current (Fig. 2.39). The expression of the static power consumption is given by  $P_{stat} = V_{dd}I_{leak}$ , where  $V_{dd}$  is the power supply and  $I_{leak}$  is the sum of all the leakage currents.

Nowadays, in advanced CMOS technologies, due to the increasing operation frequency of circuits and to the length, capacity, and resistivity of interconnects, the dynamic currents in the circuit tend to increase. However, due to the decreasing dimension of devices, the leakage currents increase much faster. As a result in advanced technologies, the standby power consumption exceeds the dynamic power consumption. Figure 2.40 shows the static and dynamic power consumptions per inch square versus technology nodes.

Several solutions are considered to reduce power consumption of CMOS circuits.

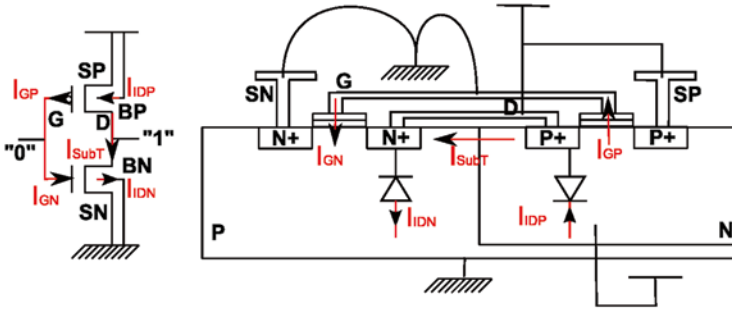
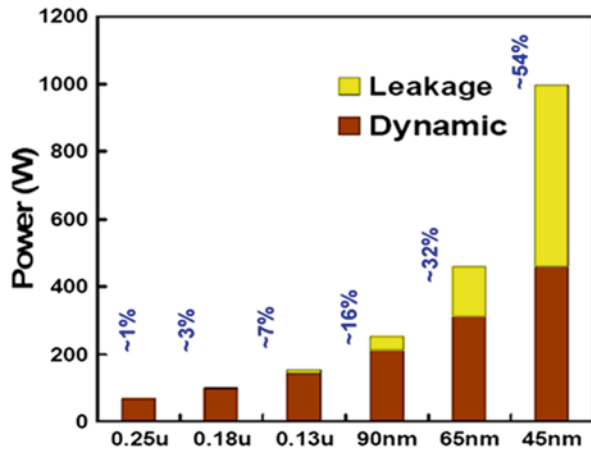


Fig. 2.39 Leakage in a CMOS inverter

Fig. 2.40 Evolution of power consumption for CMOS circuits versus technological node



### 2.3.1.2 Reduction of the Dynamic Power Consumption

The first idea to reduce the dynamic power consumption is to reduce the supply voltage: since  $V_{swing} = V_{dd}$  in classical CMOS design techniques, this results in a quadratic reduction of the power consumption. Moreover, it also reduces exponentially the subthreshold leakage. However, reducing the supply voltage reduces the range of operation and the stability of the data and globally degrades performance. Since the dynamic power consumption is directly proportional to the clock frequency, it is also possible to reduce the clock frequency for the parts of the circuit which do not require high speed operation. New design techniques can also be used to reduce the dynamic power consumption.

- The MOS current mode logic (MCML [102]) allows reducing the signals voltage swing. This allows considerably reducing the dynamic power consumption and improving the speed. However, this technique suffers from intrinsic static power consumption.
- The dynamic logic families consist in a “precharge” phase, during which the output nodes are precharged to the supply voltage and an “evaluate” phase during

which the outputs are calculated according to the values of the inputs and made available. In these circuits, the PMOS network is not necessary. A few PMOS transistors are only used to precharge the circuit. The main advantage of this approach is the reduction of the parasitic capacitance due to the suppression of the PMOS transistors. This allows increasing the density, improving the speed, and reducing the dynamic power consumption. The main drawback of this approach is that logic functions are intrinsically sequential and therefore hard to cascade.

- The respective advantages and drawbacks of these design techniques make them more or less efficient in terms of performances and power consumption according to the application. It is also possible to use different design techniques in a chip or to combine the various approaches: for example, a design technique called dynamic current mode logic (DyCML [103]) was proposed, which combines the advantages of MCML and dynamic logic.

### 2.3.1.3 Reduction of Standby Power Consumption

Clock gating techniques consist in isolating the unused parts of the circuit from the clock to avoid standby activity. This is performed at the system level. But even when no switching event occurs, leakage currents are flowing through the devices, resulting in static power consumption.

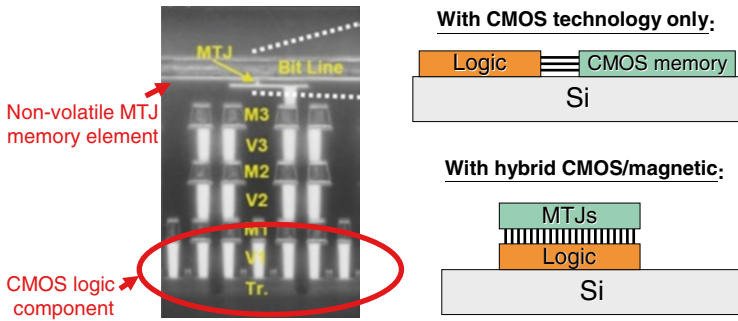
- To increase the performance of MOS circuits, the current generated by the transistor must be increased. This can be performed by increasing the MOS capacitance value (the “on” current of transistors is proportional to this capacitance). This is the reason why the oxide thickness is reduced at each technological node. But the reduction of the gate oxide thickness exponentially increases the probability of tunnelling through the gate and correlatively the gate leakage current. The solution to solve this problem is to use materials with higher dielectric constant called high-K materials [104].
- The other main contribution to leakage in MOS transistor is the subthreshold current which flows between the drain and the source even when the gate voltage is below the threshold voltage ( $V_t$ ). The solution to decrease the subthreshold current is to increase the threshold voltage, but this results in performance degradation, since the “on” current generated by the transistor is reduced when the threshold voltage is increased. Several techniques allow finding a trade-off between performance and consumption. A first technique, called MTCMOS for multiple threshold CMOS [105], consists in using transistors with different  $V_t$  in the same circuit. Recent technologies integrate several types of transistors with high or low  $V_t$ , for this purpose. This technique is used in particular for power rail gating which consists in switching off the power supply of unused blocks of the circuit to avoid leakage currents. This is performed by means of isolation transistors. Since these transistors also suffer from leakage and do not require a high operation speed, they are designed with a high  $V_t$ .
- It is possible for the designer to change by design the  $V_t$  value. This can be achieved by changing the polarization of the source of the transistor for example

by stacking transistors [106]. Note that in CMOS logic gates, transistors in series are already stacked. This can be exploited in design of these gates to reduce power consumption. Another approach is to change the polarization of the bulk of the transistors [107]. Classically, this is only possible for P-type transistors since the bulk of N-type transistors are connected to the same substrate. However, in modern technologies, it is possible to have separate N-well for NMOS (this is often referred to as triple-well CMOS process). This approach allowing  $V_t$  to be changed in a range of values is called VTCMOS (for variable threshold CMOS). However, whatever the value of the  $V_t$ , there is always remaining leakage.

In the techniques consisting in switching off the power supply of unused blocks, it is necessary to keep the power supply on specific memory elements to preserve data or to save data in a dedicated nonvolatile memory. A solution to avoid this problem is to directly use nonvolatile memories as working memories, so that the power supply can be switched-off at any time without losing information. Currently, the most widely used nonvolatile memory is the Flash memory. However, its large power consumption at writing and its poor cyclability strongly limit the frequency at which data can be stored. Other nonvolatile technologies are currently under investigation such as PCRAM (phase change RAM), FeRAM (ferroelectric RAM), RRAM (resistive oxide RAM) and MRAM. An example of logic circuit proposed by Rohm Company, made nonvolatile by replacing the internal registers by FeRAM registers, showed a very significant reduction of power consumption [108]. Comparable results can be expected using MRAM technology, by making the internal registers or Flip-Flops non-volatile [109, 110]. However, the advantages of MRAM technology in terms of low-power consumption, speed, cyclability, hardness to radiations, and their ability to be manufactured above the CMOS elements allow not only to make the memory parts of the circuit nonvolatile, but also to introduce memorization capabilities in the logic part of the circuit itself. This concept is often referred to as “logic-in-memory” [111]. In this framework, it is possible to develop “Janus” components, presenting two faces (as the mythological divinity), i.e., a logic function in CMOS technology right on the Si substrate and a memory capability built above the logic function in back-end magnetic technology, the two functions being interconnected by vertical vias (see Fig. 2.41 left). In addition to reduce the standby power consumption, this concept allows multiplying and shortening interconnections between logic and memory, reducing footprint, improving speed, and reducing dynamic power consumption (Fig. 2.41).

### 2.3.2 *Examples of CMOS/Magnetic Integrated Devices*

To illustrate the possibilities brought by the magnetic back-end technology for “logic-in-memory” concepts, here are presented two circuits designed and fabricated by Tohoku University in collaboration with Hitachi. The first one is a magnetic nonvolatile full adder [112]. A full adder performs a 1-bit binary addition (Fig. 2.42). The inputs (“A” and “B”) are the bits to be added and a carry possibly

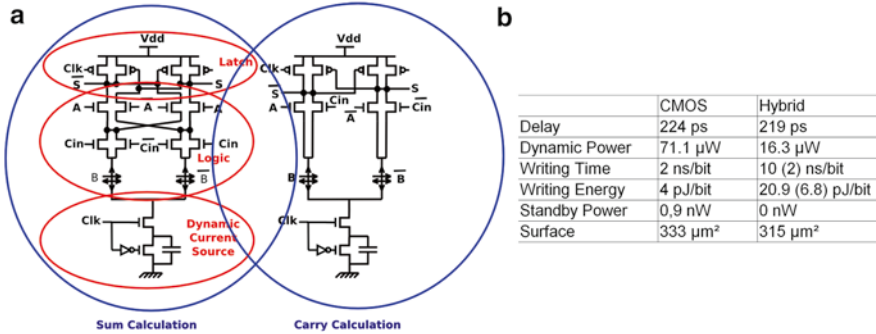


**Fig. 2.41** *Left:* principle of Janus (logic–memory) components. *Right:* logic-in-memory (multiplying and shortening the interconnections between logic and memory parts of a circuit)

A	B	C <sub>in</sub>	out	C <sub>out</sub>
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

**Fig. 2.42** Truth table of a full adder

coming from a previous operation (“ $C_{in}$ ”). The result is the sum (“out”) and the carry of the addition (“ $C_{out}$ ”).  $n$  elementary full adders can be cascaded to make a  $n$ -bit binary adder. In the circuit proposed by Tohoku University, one of the inputs (“ $B$ ”) is coded in the magnetic state of a differential pair of MTJ. The second input “ $A$ ” and the carry “ $C_{in}$ ” are connected to differential pairs of MOS transistors. The design is based on the dynamic current mode logic (DyCML): the circuit (Fig. 2.43a) comprises a latch to amplify the difference of current between the two paths of the circuit and to convert it into an output voltage. According to the “ $A$ ” and “ $C_{in}$ ” values, the connection of the differential pair of MTJ to the amplifier is modified so that the output value depends on the “ $A$ ,” “ $B$ ,” and “ $C_{in}$ ” values, the input “ $B$ ” being nonvolatile. The classical current mode logic (CML) design technique is particularly adapted to read resistances, but suffers from static power consumption due to the static current required to measure resistance. To solve this problem, in the DyCML technique, the outputs are precharged to the power supply level  $V_{dd}$  and a virtual ground (dynamic current source) is used so that there is never a direct path between the ground and the power supply. A prototype was fabricated in a CMOS 180nm technology, giving promising results (Fig. 2.43b). Since the input “ $B$ ” is made nonvolatile, the standby power required to preserve its value is virtually reduced to zero. The use of a current mode logic approach allows reducing the output signal swing and thus the dynamic power consumption and improving the speed of the circuit. The use of a dynamic design technique allows reducing the number of



**Fig. 2.43** Full adder proposed by Tohoku University in collaboration with Hitachi (a) and comparison between its performance and those of a classical CMOS full adder. (from [112])

transistors and correlatively the size of the circuit and lowering the dynamic power consumption.

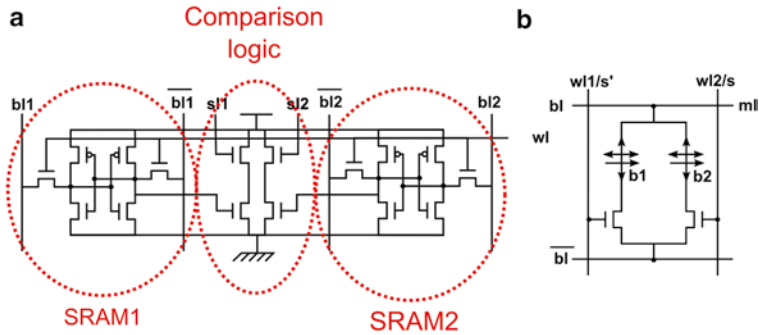
This circuit is a simple example which illustrates the potential advantages offered by using MTJs to add nonvolatile memory functionality to logic circuits and how design techniques can be adapted to lead to innovative hybrid CMOS/magnetic architectures.

Another example proposed by Tohoku University and Hitachi is a magnetic ternary content addressable memory (MTCAM [113]). A content addressable memory is addressed by content instead of address: while a classical memory returns (or write) the word corresponding to a given address, a CAM returns the address(es) containing a given word. CAMs are used in particular in network routers, fully parallel CMOS imagers, or processors caches. Ternary CAMs allow a mask operation, i.e., the ability to localize the addresses of words ignoring some bits. For example, a search operation on the word ‘011x’ can return the address(es) containing the words ‘0111’ and ‘0110.’ The main limitation of this type of memory is the cell area. Indeed, a classical CAM cell consists of two SRAM cells acting as memory elements and a logic part to compare the content of the two cells (Fig. 2.44a). In the TCAM proposed by Tohoku University, the storage elements are replaced by simple MTJs and the comparison is performed in current mode, resulting in a much smaller cell area. Again, the incorporation of MTJs together with MOS transistors allows mixing the memory and logic capabilities into the same circuit. Another MTCAM scheme was proposed by SPINTEC [114], in which a thermally assisted switching magnetic tunnel junction is used to perform the memorization and the comparison within a single device.

### 2.3.3 Modelling Tools for the Design of Hybrid CMOS/MTJ Circuits

Designing hybrid architectures embedding CMOS and magnetic devices requires integrating the magnetic devices in standard design suites of microelectronics.





**Fig. 2.44** Comparison between a standard 16 transistors CAM cell (a) and the MTCAM cell proposed by Tohoku University (b)

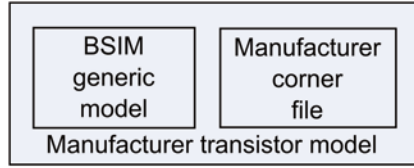
A design suite is a set of tools allowing to conceive microelectronic circuits, to simulate their electrical properties, draw their layout, and check them before manufacturing. The first tool of a design suite is an electrical simulator which allows simulating the electrical behavior of a circuit made of interconnected devices. The first electrical simulator was developed by Berkeley University in the 1970s and is called SPICE [115] (for simulation program with integrated circuit emphasis). Today, all the standard simulators of the industry are based on SPICE principle: SPECTRE for Cadence design suite, Eldo for Mentor Graphics, and HSPICE for Synopsys. The operation of the electrical simulator, which solves the Kirchhoff laws in voltage and currents, requires a netlist describing how the different devices are interconnected in the circuit and a specific formalism for the models describing the behavior of each device. This behavior is actually described by its Jacobian matrix, i.e., the generalized current/voltage characteristic. A device with  $n$  nodes is described by a  $n \times n$  matrix  $J$  where  $J_{ij}$  is the derivative of the current entering by the node  $i$  as a function of the voltage at the node  $j$ . Such Jacobian matrix has the following form:

$$J = \begin{pmatrix} J_{11} & J_{12} & \dots & \dots \\ J_{21} & \dots & \dots & \dots \\ \dots & \dots & \dots & \dots \\ \dots & \dots & \dots & J_{nn} \end{pmatrix}, J_{i,j} = \left( \frac{\partial I_i}{\partial V_j} \right)_{(I,V)}$$

The first electrical equivalent model of the transistor was also developed by Berkeley and is called BSIM for Berkeley short-channel IGFET model. Any device has to be described by an equivalent electrical circuit where all the physical quantities are represented by currents or voltages. The BSIM model of the transistor is a generic model describing the physical behavior of the device. The parameters corresponding to the devices of one given technology are provided by the manufacturer in the form of a “corner file” (Fig. 2.45).

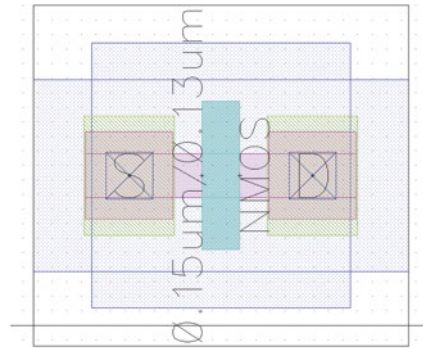
Once the correct behavior of the circuit is checked by simulation, the physical design of the circuit can begin: it consists in physically drawing the layout of the





**Fig. 2.45** Generic model of a device (here, for instance, of a transistor) associated with a corner file from a given manufacturer thus providing the device expected properties for this manufacturer technology

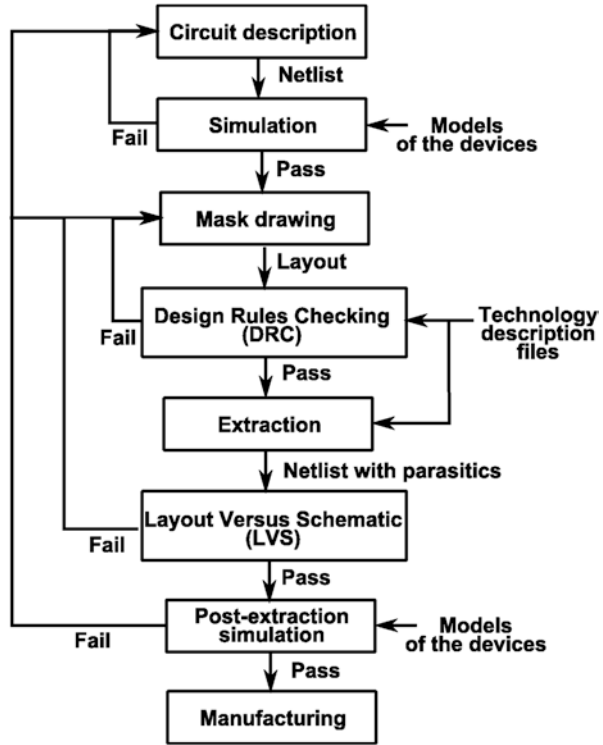
**Fig. 2.46** Example of pCell describing an NMOS transistor of the CMOS 0.13 mm technology from STMicroelectronics



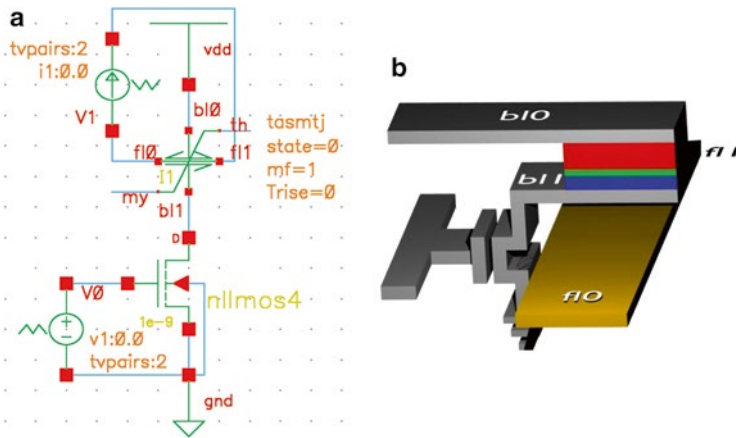
masks required to fabricate the successive layers of the circuit. A layout is then constituted of geometrical shapes representing the devices and interconnections of the different layers. To ease the layout drawing process, pCells (parameterized cell) can be provided by the manufacturer. A pCell is a layout of a particular device that can be included in the layout of the circuit (Fig. 2.46).

The dimension of the device, for example the size of a transistor, can be directly chosen by the designer and the shape of the pCell is automatically adapted to respect the design rules. Once the layout is drawn, several verification tools are used to check it. The DRC (design rules checking) tool is used to check if the layout respects the design rules of the technology (minimum size of the transistors gate, minimum space between interconnections, etc.). Then an extraction step is used to identify the devices and their interconnections from the layout. This step results in a netlist of the layout view of the circuit. This netlist contains the devices themselves, but since the topology of the circuit is now known, parasitic capacitances and resistances can also be extracted. The netlist obtained from the layout can then be compared to the netlist of the schematic view used for the simulation to check if the fabricated circuit will really correspond to the simulated circuit (LVS, layout versus schematic). Using the extracted netlist, it is also possible to perform a post-extraction simulation which takes into account the parasitic loads. After all these verifications, the layout can be converted into a standard format (GDSII) and send to the manufacturer for fabrication. Figure 2.47 summarizes the design flow of an integrated circuit, at transistor level (full custom design).

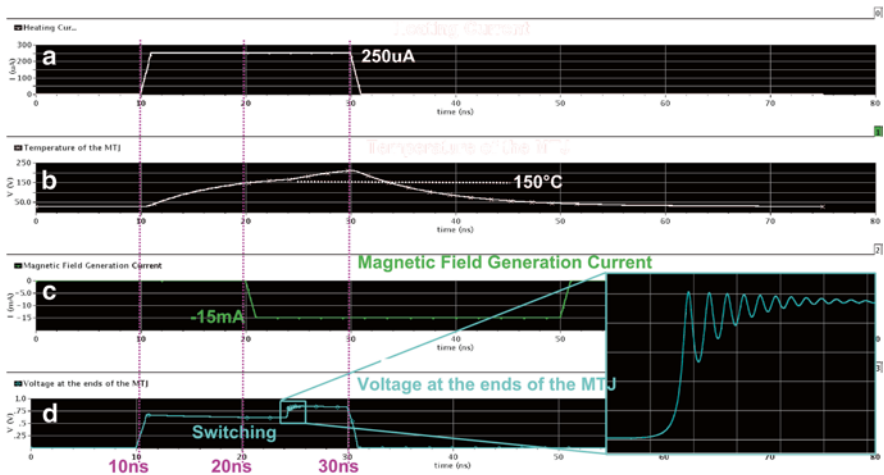
**Fig. 2.47** Design flow in microelectronics for “full custom” design



All steps of the design flow and the corresponding tools require information about the technology: parameters of the devices models are provided in corner files, design rules and extraction parameters are provided in technology files. All this information is part of a “design kit,” which is provided by the manufacturer and is compatible with a given design suite. It is necessary to provide a magnetic design kit to be able to design hybrid circuits containing magnetic devices using a standard design suite. Work along this line has been carried out by several groups. Several SPICE-like models of the MTJ were presented in literature [109, 110, 116, 117]. The model developed at SPINTEC [118–120], valid for all the MTJ writing schemes (FIMS, TAS, STT), is written in C language, compiled for SPECTRE simulator of Cadence. It takes into account the static and dynamic behaviors of the magnetization under external applied field or STT, the dependence of the resistance upon the magnetic state, the dynamic evolution of the temperature, and the dependence of the magnetic and transport parameters versus temperature. The compiled model is generic and contains the equations governing the physical behavior of the MTJ. The parameters corresponding to a given technology are provided via a corner file. Figure 2.48a shows a schematic window in Cadence design suite, which represents a very simple MRAM memory cell composed of an MTJ connected in series with a selection transistor. Figure 2.48b explains the labelling of the nodes: b10 and b11



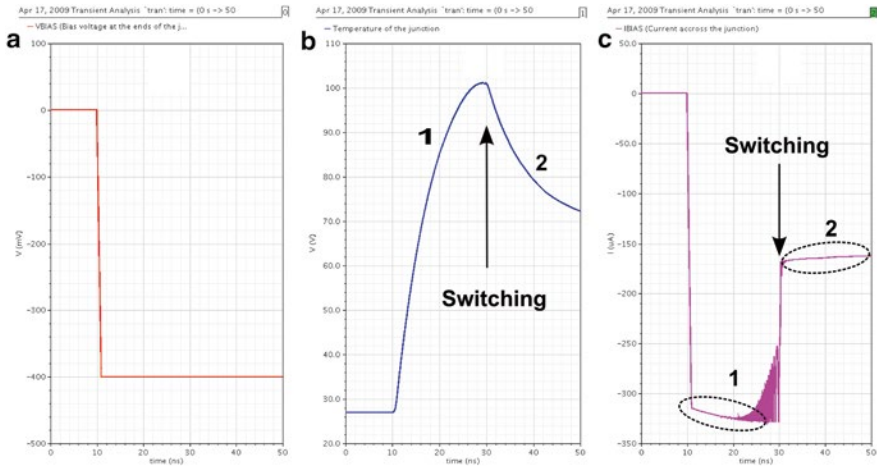
**Fig. 2.48** (a) Schematics under Cadence of a simple MRAM memory cell composed of an MTJ realized in back-end magnetic process above a selection transistor. (b): Explanation of the nodes labelling



**Fig. 2.49** Simulation results for a TAS memory cell. Heating current (a), resulting increase of temperature (b), current used to generate the writing magnetic field (c), and resulting voltage across the MTJ (d)

represent the top and bottom ends of the MTJ (bl1 is connected to the selection transistor). fl0 and fl1 are the ends of a current line possibly required for magnetic field generation.

Figure 2.49 shows simulation results for a thermally assisted switching (TAS) writing scheme. Figure 2.49a, b, respectively, shows the heating current through the junction and the resulting increase of temperature of the junction. Figure 2.49c, d, respectively, represents the current through the current line to generate the writing

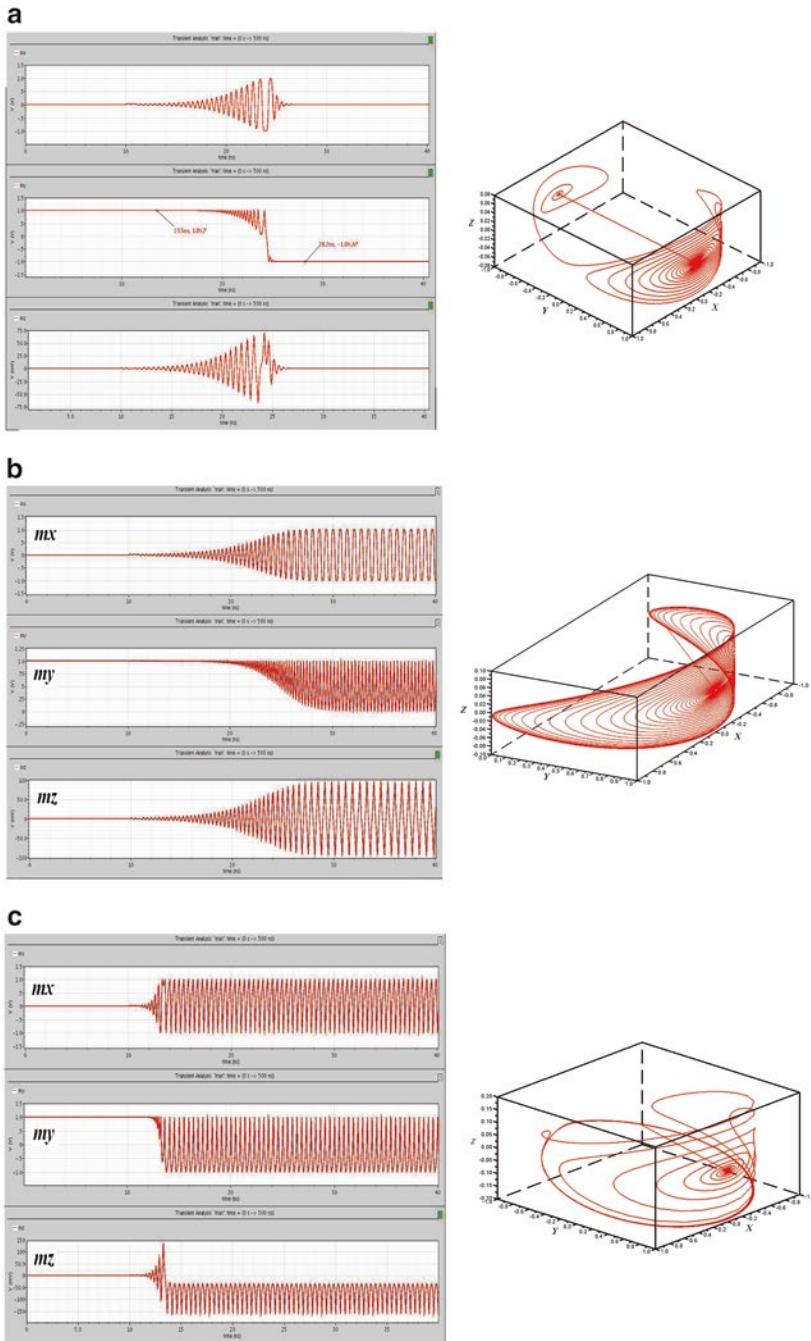


**Fig. 2.50** Simulation results for an STT memory cell. Voltage across the MTJ (a), dynamic evolution of the temperature (b), and current through the MTJ (c)

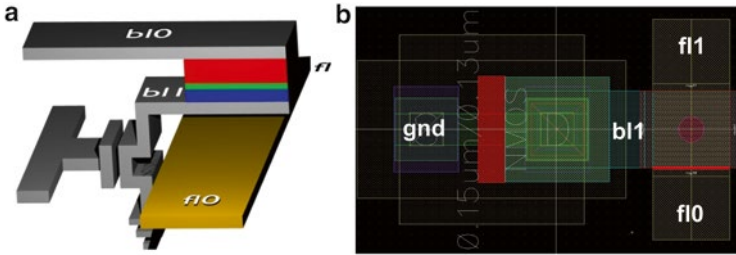
magnetic field and the voltage across the junction. For a heating current large enough to reach the blocking temperature of the storage layer, the voltage exhibits a step like behavior when a magnetic field is applied: this is due to the magnetization switching and the resulting change of resistance. Oscillations can be seen around the magnetization switching due to the peculiar magnetization dynamics during switching which is taken into account in the model. We can also notice that even before and after switching, the voltage is not constant. This is due to the variation of the conductance associated with the temperature variation of the junction. Finally, at magnetic switching, the temperature dynamics changes because the resistance changes and correlatively the power dissipated in the MTJ by Joule heating.

Figure 2.50 shows an example of simulation results for STT switching: Fig. 2.50a represents the voltage applied to the junction to generate the spin-polarized current. Figure 2.50b, c, respectively, shows the increase of temperature and the current through the junction. Again, we see the transient behavior of the switching for an STT writing scheme. Furthermore in MTJ, it is possible, by properly combining the influence of the STT generated by the spin-polarized current flowing through the MTJ with that of an external magnetic field, to generate steady precessions of the magnetization of the MTJ soft layer. This is very interesting for designing frequency tunable RF oscillators. According to the respective value of the current and the field, we can obtain switching (Fig. 2.51a), in-plane precessions (Fig. 2.51b), or out-of-plane precessions (Fig. 2.51c). Results obtained using the present model were compared to previously published theoretical macrospin calculations and are in very good agreement.\*\*\*

CMOS technology files have been adapted by the CMP (Centre-Multi-Project) [121] to integrate the magnetic back-end technology of Crocus-Technology and of LETI. This modification was made for Austria Micro-Systems 350n and



**Fig. 2.51** Precessional modes of the magnetization for an MTJ submitted to the combined influence of the spin-transfer torque generated by the spin-polarized current flowing through the MTJ and an external magnetic field. Depending on the values of current and field, various regimes can be observed: switching of the magnetization (a), in-plane precessions (b), and out-of-plane precessions (c)



**Fig. 2.52** Schematics describing the memory cell (a) and corresponding layout with the pCell of the MTJ and the pCell of the transistor (b)

STMicroelectronics 130nm CMOS technologies. A pCell of the MTJ has also been provided (Fig. 2.52). This environment can be integrated in the Cadence design suite to integrate MTJs exactly as standard electronic devices.

### 2.3.4 Perspectives

Hybrid CMOS/magnetic circuits look very promising for circumventing the limits of conventional CMOS electronics. At the moment, the magnetic back-end process is not as mature as the CMOS one. Important process variations are still observed in the fabrication of magnetic devices. Furthermore, a few questions remain open about the physics of spin-transfer torque. This still limits the accuracy of the models and the reliability of the design, forcing to take large design margins and thereby limiting the possibilities of optimization in terms of performances. However, steady technological progresses are achieved in this hybrid CMOS/MTJ integration thanks to all the ongoing R&D effort on MRAM. Since the technology is very similar for MRAM and hybrid CMOS/MTJ nonvolatile logic, these progresses will directly benefit this field. When this hybrid technology is stabilized, characterization results with good statistics will become available to improve the accuracy of the models and to standardize the design and fabrication tools. Nevertheless, several circuits have already been fabricated yielding very encouraging results. Moreover, the writing schemes based on the STT or thermal assistance are very scalable, since the switching of the magnetic state is driven by current density. The advantages of mixing MTJs with CMOS devices should become more and more obvious with advanced technologies. Of course, this new technology can be used together with other design techniques to improve circuits' performances, especially in terms of power consumption. Further research is required to investigate how these different techniques can be combined. In particular, we have seen that some of these techniques are efficient at the full system level. It is then necessary to evaluate the opportunities provided by this technology for complete systems and in comparison or combination with existing techniques and for advanced technologies.

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# Chapter 3

## Emerging Multiferroic Memories

Lane W. Martin, Ying-Hao Chu, and R. Ramesh

### 3.1 Introduction

Thus far in this book, we have focused on ferroelectric and magnetic spin torque transfer memories. In this chapter, we describe the recent discoveries in the emerging field of multiferroic-based memories. In the last decade, considerable attention has been focused on the search for and characterization of new multiferroic materials as scientists and researchers have been driven by the promise of exotic materials functionality (especially electric field control of ferromagnetism). In this chapter we develop a holistic picture of multiferroic materials, including details on the nature

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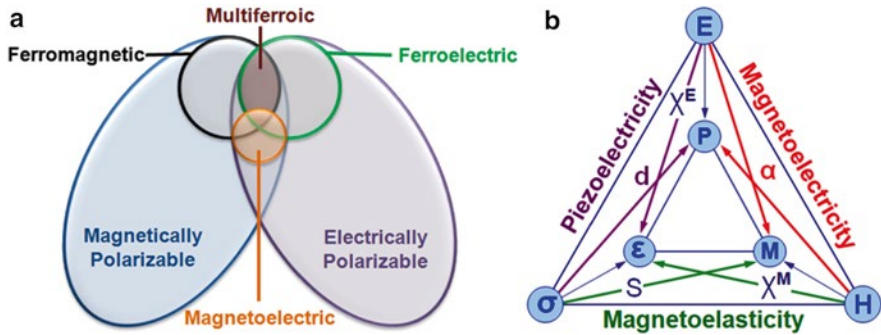
of order parameters and coupling in these materials, the scarcity of such materials, routes to create and control the properties in these materials, and prospects for these materials in next generation devices—with special attention given to memory applications.

Complex oxides represent a vast class of materials encompassing a wide range of crystal structures and functionalities. Amongst these interesting properties, the study of magnetic, ferroelectric, and, more recently, multiferroic properties has driven considerable research. Specifically, in the last few years there has been a flurry of research focused on multiferroic and magnetoelectric materials [1–3]. From the investigation of bulk single crystals to novel characterization techniques that probe order parameters, coupling, spin dynamics, and more this is truly a diverse field, rich with experimental and theoretical complexity. By definition, a single-phase multiferroic [4] is a material that simultaneously possesses two or more of the so-called ferroic order parameters—ferroelectricity, ferromagnetism, and ferroelasticity. Magnetoelectric coupling typically refers to the linear magnetoelectric effect or the induction of magnetization by an electric field or polarization by a magnetic field [5]. The promise of coupling between magnetic and electronic order parameters and the potential to manipulate one through the other has captured the imagination of researchers worldwide. The ultimate goal for device functionality would be a single-phase multiferroic with strong coupling between ferroelectric and ferromagnetic order parameters making for simple control over the magnetic nature of the material with an applied electric field at room temperature.

Driven by advances in the synthesis of both bulk and thin-film versions of these materials (see, for example, [6, 7], respectively), there has been a renewed interest in these materials for a number of applications. As part of this chapter we will discuss a number of different classes of multiferroic materials, coupling between order parameters in these materials, a number of model multiferroic thin film systems that are candidate materials for memory applications, as well as the state-of-the-art work on multiferroics based devices, before finally developing a picture of the advances, both in terms of basic materials and device architectures, needed to see multiferroic-based memories significantly impact the technology landscape.

## 3.2 Multiferroic Materials

Multiferroism describes materials in which two or all three of the properties ferroelectricity (spontaneous polarization that is both stable and can be switched by application of an electric field), ferromagnetism (spontaneous magnetization that is stable and can be switched by application of a magnetic field), and ferroelasticity (spontaneous deformation that is stable and can be switched by application of an electric field) occur in the same phase. The overlap required of ferroic materials to be classified as *multiferroic* is shown schematically in Fig. 3.1a. Only a small subgroup of all magnetically and electrically polarizable materials are either ferromagnetic or ferroelectric and fewer still simultaneously exhibit both order parameters.



**Fig. 3.1** (a) Relationship between multiferroic and magnetoelectric materials. Illustrates the requirements to achieve both in a material (adapted from [7]). (b) Schematic illustrating different types of coupling present in materials. Much attention has been given to materials where electric and magnetic order is coupled. These materials are known as magnetoelectric materials (adapted from [8])

In these select materials, however, there is the possibility that electric fields cannot only reorient the polarization but also control magnetization; similarly, a magnetic field can change electric polarization. This functionality offers an extra degree of freedom and we refer to such materials as *magnetoelectrics* (Fig. 3.1b). Magnetoelectricity is an independent phenomenon that can arise in any material with both magnetic and electronic polarizability, regardless of whether it is multiferroic or not. By the original definition a magnetoelectric multiferroic must be simultaneously both ferromagnetic and ferroelectric [4], but it should be noted that the current trend is to extend the definition of multiferroics to include materials possessing two or more of any of the ferroic or corresponding antiferroic properties such as antiferroelectricity (possessing ordered dipole moments that are aligned antiparallel and therefore cancel each other completely across the sample) and antiferromagnetism (possessing ordered magnetic moments that are aligned antiparallel and therefore cancel each other completely across the sample). More recently it has also been extended to include the so-called ferrotoroidic order (a spontaneous order parameter that is taken to be the curl of a magnetization or polarization) [8]. This said, it should be abundantly obvious why there has been considerable renewed interest in these materials over the last decade. The prospects for these materials in applications are wide ranging and have driven a spectrum of both fundamental and applied studies. Multiferroics have been proposed for use in applications ranging from next generation logic and memory to sensing to tunable RF and much more. Although we will only explicitly explore the implications for memory applications, it is important to recognize the versatile possibilities for these materials.

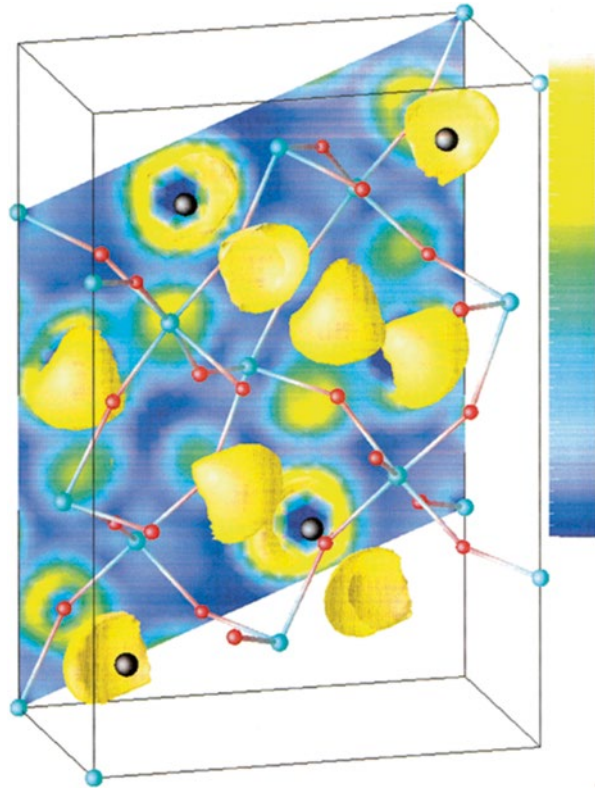
With this as a background, the single largest limiting factor that has kept multiferroics from making substantial in-roads into current technology is the scarcity of multiferroics. This scarcity has been recently reviewed by Khomskii [9]. Taking as an example the perovskite ( $ABO_3$ ) compounds, one can obtain a detailed list of

magnetic perovskites in the tables compiled by Goodenough and Longo [10] and further investigation will reveal similar tables of ferroelectric perovskites compiled by Mitsui et al. [11]. What becomes apparent after investigating these tables is that there is essentially no overlap between these lists—magnetism and ferroelectricity in materials are seemingly incompatible. Key insights into this scarcity of multiferroic phases can be understood by investigating a number of factors including symmetry, electronic properties, and chemistry [12, 13]. To begin, it should be noted that there are only 13 point groups that can give rise to multiferroic behavior. Strong magnetism in itinerant ferromagnets requires the presence of conduction electrons in partially filled inner shells (*d*- or *f*-shells); even in double exchange ferromagnets such as the manganites, magnetism is mediated by incompletely filled *3d* shells. The situation in ferroelectrics, however, is somewhat more complicated as many different mechanisms for ferroelectric ordering and a number of different types of ferroelectrics exist. Generally it is observed, however, that ferroelectrics (which are by definition insulators) typically possess (for instance, in transition metal oxides) cations that have a formal  $d^0$  electronic state. This  $d^0$  state is thought to be required to drive the formation of strong covalency with the surrounding oxygen, thereby, shifting the transition metal ion from the center of the unit cell and inducing a spontaneous polarization (this is the so-called second-order Jahn–Teller effect) [14]. The second-order Jahn–Teller effect describes the structural changes resulting from a non-degenerate ground-state interacting with a low-lying excited state and it occurs when the energy gap between the highest occupied (HOMO) and lowest unoccupied (LUMO) molecular orbital is small and there is a symmetry allowed distortion permitting the mixing of the HOMO and LUMO states. Mathematically, the second-order Jahn–Teller effect can be understood through the use of second-order perturbation group theory, but this is beyond the scope of this chapter [15]. Thus, in the end, it becomes clear that there exists a seeming contradiction between the conventional mechanism of off-centering in a ferroelectric and the formation of magnetic order which helps explain the scarcity of ferromagnetic–ferroelectric multiferroics. The focus of many researchers, therefore, has been on designing and indentifying new mechanisms that lead to magnetoelectric coupling and multiferroic behavior. In the following section we will investigate a number of these pathways.

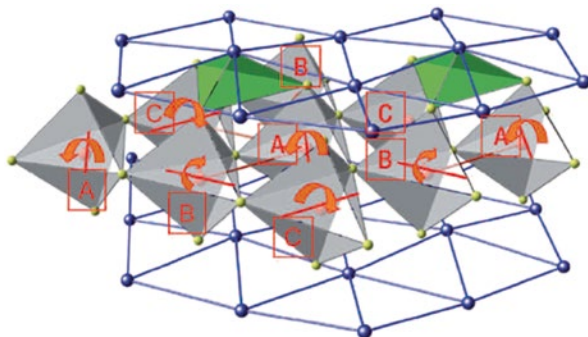
An investigation of these various pathways to multiferroism is aided by separation of all multiferroic materials into one of two types [16]. Type I multiferroics are materials in which ferroelectricity and magnetism have different sources and appear largely independent of one another. One can create a Type I multiferroic, for instance, by engineering the functionality on a site-by-site basis in model systems such as the perovskites ( $ABO_3$ ) where one can make use of the stereochemical activity of an *A*-site cation with a lone pair (i.e.,  $6s$  electrons in Bi or Pb) to induce a structural distortion and ferroelectricity while inducing magnetism with the *B*-site cation. This is the case in the multiferroics  $\text{BiFeO}_3$  [17],  $\text{BiMnO}_3$  [18, 19], and  $\text{PbVO}_3$  [20–23]. From the microscopic view, it can be understood that the orientation of the lone-pairs in the materials can give rise to local dipoles that can order thereby creating a



**Fig. 3.2** Electron localization function representation of the isosurface of the valence electrons in  $\text{BiMnO}_3$  projected within a unit cell. Dark colors correspond to a lack of electron localization and light to complete localization (adapted from [24])



net polarization as has been demonstrated with *ab initio* models (Fig. 3.2) [24]. Much like the polarization observed in the classic ferroelectrics (i.e.,  $\text{BaTiO}_3$ ), materials such as  $\text{BiFeO}_3$  and  $\text{BiMnO}_3$  are referred to as *proper* ferroelectrics. In a proper ferroelectric structural instability towards a polar state, associated with the electronic pairing, is the main driving force for the transition. If, on the other hand, polarization is only a part of a more complex lattice distortion or if it appears as an accidental by-product of some other ordering, the ferroelectricity is called *improper* [25]. One pathway by which one can obtain an improper ferroelectric, Type I multiferroic is through geometrically driven effects where long-range dipole–dipole interactions and anion rotations drive the system towards a stable ferroelectric state. This is thought to drive multiferroism in materials such as the hexagonal manganites (i.e.,  $\text{YMnO}_3$ ) (Fig. 3.3) [26, 27]. Again, in these materials ferroelectricity is achieved despite violating the requirement of having a  $d^0$  electron configuration on the *B*-site cation. Despite this fact, the resulting ferroelectric transition temperatures for these hexagonal manganites are typically quite high ( $\sim 900$ – $1,000$  K)—suggesting a robustness to the order parameter. Recent results also suggest that the off-center shift of the  $\text{Mn}^{3+}$  ions (which, it should be noted, are not Jahn–Teller ions) from the center

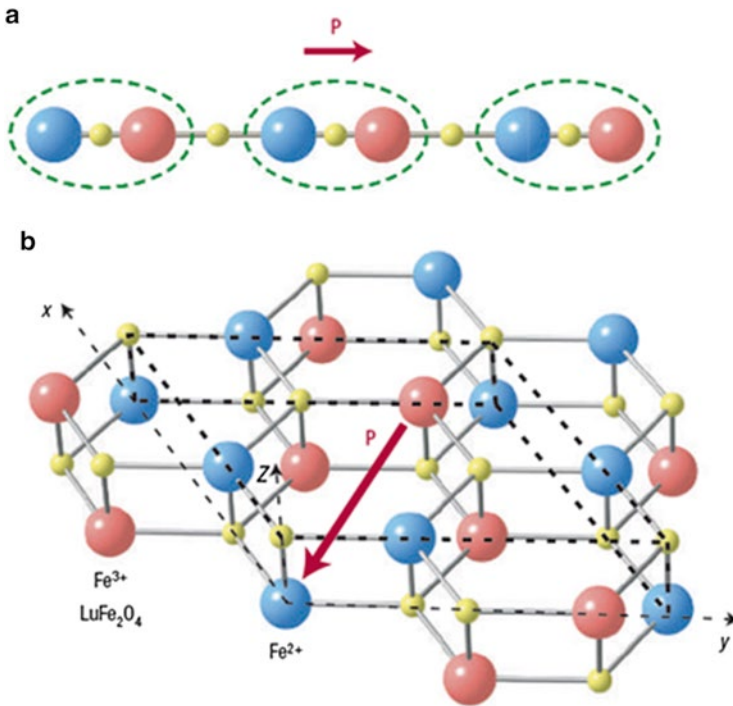


**Fig. 3.3** Schematic illustration of the cooperative rotation of bipyramids in  $\text{YMnO}_3$  that give rise to ferroelectric polarization. The resulting rotations are shown with the *arrows* (adapted from [26])

of the  $\text{O}_5$  trigonal bipyramid are quite small and are, in turn, not the major mechanism for ferroelectric order in the system. Instead it is thought that the main dipole moments are formed (for instance, in  $\text{YMnO}_3$ ) by the Y–O pairs—thus suggesting that the mechanism of ferroelectricity in these materials is distinctly different from that observed in classic ferroelectric materials such as  $\text{BaTiO}_3$  [27].

Still another pathway by which one can achieve improper ferroelectricity in a Type I multiferroic is via charge ordering where non-centrosymmetric charge ordering arrangements result in ferroelectricity in magnetic materials as is found, for instance, in  $\text{LuFe}_2\text{O}_4$  [28]. It has long been known that in many narrow band metals with strong electronic correlations, charge carriers become localized at low temperatures and form periodic superstructures. The most famous example is magnetite ( $\text{Fe}_3\text{O}_4$ ), which undergoes a metal–insulator transition at  $\sim 125$  K (the Verwey transition) with a rather complex pattern of ordered charges of iron ions [29, 30]. This charge ordering (which occurs in a non-symmetric manner) induces an electric polarization. More recently it has been suggested that the coexistence of bond-centered and site-centered charge ordering in  $\text{Pr}_{1-x}\text{Ca}_x\text{MnO}_3$  leads to a non-centrosymmetric charge distribution and a net electric polarization (Fig. 3.4a) [31]. In the case of  $\text{LuFe}_2\text{O}_4$ , the charge ordering results in a bilayer structure and appears to induce electric polarization. The average valence of Fe ions in  $\text{LuFe}_2\text{O}_4$  is  $2.5+$ , and in each layer these ions form a triangular lattice. Below  $\sim 350$  K, it is thought that alternating layers with  $\text{Fe}^{2+}:\text{Fe}^{3+}$  ratios of 2:1 and 1:2 are produced, which result in a net polarization (Fig. 3.4b) [28].

So far we have investigated Type I multiferroics, where magnetism and ferroelectricity result from two unrelated mechanisms. In these systems because the ordering results from very different mechanisms, one would not, a priori, expect there to be strong magnetoelectric coupling in these materials. On the other hand, Type II multiferroics are materials in which magnetism causes ferroelectricity—implying a strong coupling between the two order parameters. The prototypical examples of this sort of behavior are  $\text{TbMnO}_3$  [32] and  $\text{TbMn}_2\text{O}_5$  [33] where ferroelectricity



**Fig. 3.4** (a) Illustration describing how ferroelectric order can be achieved in charge-ordered systems. The *spheres* correspond to cations with more/less charge and ferroelectricity is induced by the presence of simultaneous site-centered and bond-centered charge ordering. Dimers are marked by the *dashed lines*. (b) Charge ordering in LuFe<sub>2</sub>O<sub>4</sub> with a triangular lattice of Fe-ions in each layer—charge transfer from the top to bottom layer gives rise to a net electric polarization (adapted from [2])

is induced by the formation of a symmetry-lowering magnetic ground state that lacks inversion symmetry. For instance, in TbMnO<sub>3</sub>, the onset of ferroelectricity is directly correlated with the onset of spiral magnetic order at ~28 K [34]. The intimate connection between magnetic and ferroelectric order results in extraordinary coupling—including the ability to change the direction of electric polarization with an applied magnetic field in TbMnO<sub>3</sub> [32] and switching from positive to negative polarization in TbMn<sub>2</sub>O<sub>5</sub> with a magnetic field [33]. The true nature of the mechanism for ferroelectric ordering in these materials is still under debate. Current theories have noted that for most of these materials the ferroelectric state is observed only when there is a spiral or helicoidal magnetic structure. The idea is that via some mechanism, for instance the Dzyaloshinskii–Moriya antisymmetric exchange interaction [35, 36] which is a relativistic correction to the usual superexchange with strength proportional to the spin–orbit coupling constant, the magnetic spiral can exert an influence on the charge and lattice subsystems, thereby creating ferroelectric order. Similar effects have also been observed in Ni<sub>3</sub>V<sub>2</sub>O<sub>8</sub> [37].

### 3.3 Principles of Magnetoelectricity in Multiferroics

From an applications standpoint, the real interest in multiferroic materials lies in the possibility of strong magnetoelectric coupling and the possibility to create new functionalities in materials. The magnetoelectric effect was proposed as early as 1894 by Curie [38], but experimental confirmation of the effect remained elusive until work on  $\text{Cr}_2\text{O}_3$  in the 1960s [39–42]. As early as the 1970s a wide range of devices, including devices for the modulation of amplitudes, polarizations, and phases of optical waves, magnetoelectric data storage and switching, optical diodes, spin-wave generation, amplification, and frequency conversion had been proposed that would take advantage of magnetoelectric materials [43]. The magnetoelectric effect in its most general definition delineates the coupling between electric and magnetic fields in matter. Magnetoelectric coupling may exist regardless of the nature of the magnetic and electrical order parameters and can arise from direct coupling between two order parameters or indirectly via the lattice or strain. A better understanding of magnetoelectric coupling arises from expansion of the free energy of a material, i.e.

$$F(\vec{E}, \vec{H}) = F_0 - P_i^S E_i - M_i^S H_i - \frac{1}{2} \epsilon_0 \epsilon_{ij} E_i E_j - \frac{1}{2} \mu_0 \mu_{ij} H_i H_j - \frac{1}{2} \beta_{ijk} E_i H_j H_k - \frac{1}{2} \gamma_{ijk} H_i E_j E_k - \dots \quad (3.1)$$

with  $\vec{E}$  and  $\vec{H}$  as the electric field and magnetic field, respectively. Differentiation leads to the constitutive order parameters polarization

$$P_i(\vec{E}, \vec{H}) = -\frac{\partial F}{\partial E_i} = P_i^S + \epsilon_0 \epsilon_{ij} E_j + \alpha_{ij} H_j + \frac{1}{2} \beta_{ijk} H_j H_k + \gamma_{ijk} H_i E_j + \dots \quad (3.2)$$

and magnetization

$$M_i(\vec{E}, \vec{H}) = -\frac{\partial F}{\partial H_i} = M_i^S + \mu_0 \mu_{ij} H_j + \alpha_{ij} E_i + \beta_{ijk} E_i H_j + \frac{1}{2} \gamma_{ijk} E_j E_k + \dots \quad (3.3)$$

where  $\epsilon$  and  $\mu$  are the electric and magnetic susceptibilities, respectively, and  $\alpha$  represents the induction of polarization by a magnetic field or magnetization by electric field and is designated the linear magnetoelectric effect. It should be noted that higher order magnetoelectric effects like  $\beta$  and  $\gamma$  are possible, however, they are often much smaller in magnitude than the lowest order terms. Furthermore, it can be shown that the magnetoelectric response is limited by the relation  $\alpha_{ij}^2 < \epsilon_{ii} \mu_{jj}$  or more rigorously  $\alpha_{ij}^2 < \chi_{ii}^e \chi_{jj}^m$  where  $\chi^e$  and  $\chi^m$  are the electric and magnetic susceptibilities. This means that the magnetoelectric effect can only be large in ferroelectric and/or ferromagnetic materials. To date the largest magnetoelectric responses have

been identified in composite materials where the magnetoelectric effect is the product property of a magnetostrictive and a piezoelectric material and in multiferroic materials [5].

Symmetry also has a key role to play in magnetoelectricity. In fact, Curie's early work had already pointed to the fact that symmetry was a key issue in the search for magnetoelectric materials, but it was not until much later that researchers realized magnetoelectric responses could only occur in time-asymmetric materials [44]. Detailed symmetry analyses [45–47] have produced lists of magnetoelectric point groups and tensor elements. By definition the magnetoelectric effect involves both magnetic and electric fields, thereby ruling out materials with either time reversal or inversion symmetry. In the end there are only 58 magnetic point groups that allow the magnetoelectric effect. These symmetry concerns have led to a strict set of criteria that must be met for a material to exhibit magnetoelectric behavior.

### 3.4 Multiferroic Materials for Memory Applications

Multiferroics have a storied history dating back to the 1950s. At that time, Soviet scientists attempted to replace partially diamagnetic ions with paramagnetic ones on the *B*-site of oxyoctahedral perovskites [48, 49] making the phases  $\text{Pb}(\text{Fe}_{1/2}\text{Nb}_{1/2})\text{O}_3$  and  $\text{Pb}(\text{Fe}_{1/2}\text{Ta}_{1/2})\text{O}_3$  which were found to be both ferroelectric and antiferromagnetic. This sparked the birth of the field of multiferroics. Following this initial period of interest throughout the 1960s and 1970s, these materials were relegated to the realms of physics novelty as the complex nature of these materials made it quite difficult to produce high quality materials that possessed the desired combination of properties. The so-called renaissance of magnetoelectric multiferroics [50] came in the early 2000s as combined advances in the production of high-quality thin films and bulk single crystals were augmented by significant advances in materials characterization (especially scanning probe, optical, neutron, and synchrotron-based techniques) made it, for the first time, possible to synthesize high-quality samples and characterize multiple order parameters in these materials.

Today there are roughly four major classes of multiferroic materials (1) materials with the perovskite structure, (2) materials with hexagonal structure, (3) boracites, and (4)  $\text{BaMF}_4$  compounds. Briefly we will investigate each of these classes of multiferroics before proceeding to focus on one major example. Let us begin at the end of the list by investigating multiferroics with  $\text{BaMF}_4$  ( $M = \text{Mg, Mn, Fe, Co, Ni, and Zn}$ ) structure. These materials have been studied since the late 1960s and are typically defined by their orthorhombic structure and  $2mm$  point group symmetry [51, 52]. Often their extrapolated Curie temperatures are very high (in excess of the melting point) and at low temperatures ( $<100$  K) the ferroelastic, ferroelectric structure exhibits antiferromagnetic or weakly ferromagnetic order [53]. Moving on to some of the other common multiferroic structures, the boracites, with general chemical formula  $M_3\text{B}_7\text{O}_{13}\text{X}$  ( $M = \text{Cr, Mn, Fe, Co, Cu, Ni}$ ;  $\text{X} = \text{Cl, Br}$ ), are typically ferroelastic ferroelectric, antiferromagnets (and occasionally weakly ferromagnetic).

In some cases the ferroelectric Curie temperature can exceed room temperature, but (again) the magnetic ordering temperatures are generally less than 100 K [53]. The materials undergo a classic transition from a high-temperature cubic phase ( $-43m$  symmetry) [54] at high temperatures to an orthorhombic structure ( $mm2$  symmetry). Note that some phases also possess subsequent phase transitions to  $m$  and  $3m$  symmetry at lower temperatures [55, 56]. The third common class of multiferroic materials are those possessing hexagonal structure and general chemical formula  $ABO_3$  or  $A_2B'B''O_6$ . Of these materials, the best known and studied are the hexagonal ferroelectric, antiferromagnetic manganites ( $RMnO_3$ ,  $R = \text{Sc, Y, In, Ho, Er, Tm, Yb, Lu}$ ) which were first discovered in the late 1950s [57, 58]. These materials are defined by  $6mm$  symmetry and up to four long-range ordered subsystems, including the ferroelectric lattice with Curie temperatures typically between 570 and 990 K [53, 58], the antiferromagnetic  $Mn^{3+}$  lattice with Néel temperatures typically between 70 and 130 K [59], and two rare-earth sublattices with magnetic order temperatures below  $\sim 5$  K [60]. This brings us to the oldest and best known class of multiferroic materials that are based on the perovskite structure with general chemical formula  $ABO_3$ ,  $A_2B'B''O_6$ , or a large variety of doped or chemically substituted phases. Generally multiferroic perovskites do not possess ideal cubic symmetry ( $m3m$ ), but have some slight deformation (i.e., a rhombohedral distortion as is the case in  $\text{BiFeO}_3$  which has  $3m$  symmetry). There are a large number of multiferroic perovskites (for a nice listing see [53]), but by far the most widely studied material has been  $\text{BiFeO}_3$ . Bismuth ferrite or  $\text{BiFeO}_3$  is a ferroelastic ferroelectric, antiferromagnet with high ordering temperatures and can be chemically alloyed to tune the properties. Because of the versatility of this material, the high ordering temperatures, and the robust order parameters, it has attracted unprecedented attention since the first half of the 2000s.

The re-emergence of interest in multiferroics has been driven, in part, by the development of thin film growth techniques that allow for the production of non-equilibrium phases of materials and strain engineering of existing materials [61]. Thin films offer a pathway to the discovery and stabilization of a number of new multiferroics in conjunction with the availability of high-quality materials that can be produced in larger lateral sizes than single crystal samples. Much of the recent success in strain engineering of multiferroics has arisen from the development of new oxide substrate materials. Techniques and materials developed during the intense study of high-temperature superconductors in the 1980s and 1990s have led to a wide variety of oxide substrates. Many of the current technologically relevant multiferroics materials possess perovskite or perovskite-derived structures and thus chemically and structurally compatible perovskite substrates are needed [62]. These substrates include  $\text{YAlO}_3$ ,  $\text{LaSrAlO}_4$ ,  $\text{LaAlO}_3$ ,  $\text{LaSrGaO}_4$ ,  $\text{NdGaO}_3$ ,  $(\text{LaAlO}_3)_{0.29}(\text{Sr}_{0.5}\text{Al}_{0.5}\text{TaO}_3)_{0.71}$  (LSAT),  $\text{LaGaO}_3$ ,  $\text{SrTiO}_3$ ,  $\text{DyScO}_3$ ,  $\text{GdScO}_3$ ,  $\text{SmScO}_3$ ,  $\text{KTaO}_3$ , and  $\text{NdScO}_3$  that give quality starting materials with lattice parameters from as low as  $\sim 3.70$  Å to  $\sim 4.0$  Å. Using such substrates, multiferroic thin films and nanostructures have been produced using a wide variety of growth techniques including sputtering, spin coating, pulsed laser deposition, sol-gel processes, metal-organic chemical vapor deposition, molecular beam epitaxy, and more.

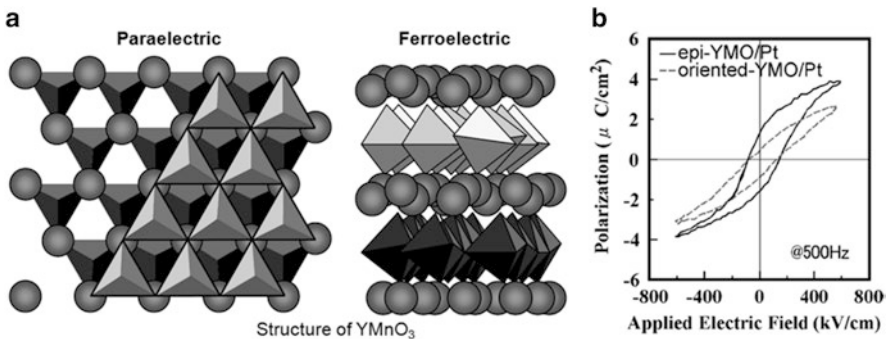


Despite the fact that there are a number of algorithms with which one can create multiferroism in materials, to date only a limited number of single-phase multiferroics produced as thin films include the hexagonal manganites and Bi- and Pb-based perovskites. In this section we will investigate these single-phase thin film multiferroics in more detail.

### 3.4.1 Manganite Thin Films

The rare-earth manganites ( $RE\text{MnO}_3$ ) are an intriguing materials system and depending on the size of the  $RE$  ion the structure takes on an equilibrium orthorhombic ( $RE=\text{La-Dy}$ ) or hexagonal ( $RE=\text{Ho-Lu}$ , as well as  $\text{Y}$ ) structure [63]. All of the hexagonal rare-earth manganites are known to show multiferroic behavior with relatively high ferroelectric ordering temperatures (typically in excess of 590 K) and relatively low magnetic ordering temperatures (typically between 70 and 120 K) [64]. In these hexagonal phases, the ferroelectric ordering is related to the tilting of the rigid  $\text{MnO}_5$  trigonal bipyramid [27]. On the other hand, only the orthorhombic phases with  $RE=\text{Dy, Tb, and Gd}$  are multiferroic in nature and have very low ( $\sim 20\text{--}30$  K) ferroelectric ordering temperatures [32, 65]. In these materials the ferroelectricity arises from magnetic ordering induced lattice modulations.

One of the earliest thin-film multiferroic manganites to be produced was the hexagonal manganite  $\text{YMnO}_3$  (Fig. 3.5a) [67]. Work on  $\text{YMnO}_3$  in the 1960s suggested that it was both a ferroelectric [63] and an A-type antiferromagnet [59]; however, it was not until sometime later that the true nature of ferroelectricity in this material was understood to arise from long-range dipole-dipole interactions and oxygen rotations working together to drive the system towards a stable ferroelectric state [27]. The first films [67] were grown via radio-frequency magnetron sputtering and obtained epitaxial (0001) films on  $\text{MgO}$  (111) and  $\text{ZnO}$  (0001)/sapphire (0001)



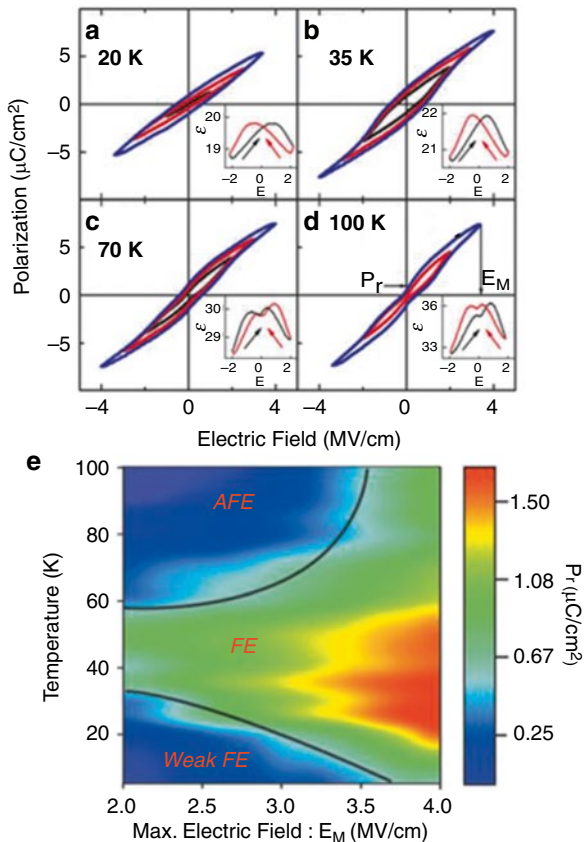
**Fig. 3.5**  $\text{YMnO}_3$ . (a) The crystal structure of  $\text{YMnO}_3$  in the paraelectric and ferroelectric phases. The trigonal bipyramids depict  $\text{MnO}_5$  polyhedra and the spheres represent Y ions. (Adapted from [27]) (b)  $P$ - $E$  hysteresis of the epitaxial-YMO/Pt and the oriented-YMO/Pt. (Adapted from [66])

and polycrystalline films on Pt (111)/MgO (111). It was soon shown that using the epitaxial strain intrinsic to such thin films, one could drive the hexagonal phase of  $\text{YMnO}_3$  to a metastable, non-ferroelectric orthorhombic perovskite phase by growth on the appropriate oxide substrates including  $\text{SrTiO}_3$  (001) and  $\text{NdGaO}_3$  (101) [68]. This work was of great interest because it was the first evidence for a competition between hexagonal and orthorhombic  $\text{YMnO}_3$  phases and how epitaxial thin film strain could be used to influence the structure of this material. This is a perfect example of the power of epitaxial thin film growth and how it can give researchers access to high pressure and temperature phases that are not easily accessible by traditional bulk synthesis techniques. Since this time  $\text{YMnO}_3$  has been grown on a number of other substrates including Si (001) [67, 69],  $\text{Pt/TiO}_2/\text{SiO}_2/\text{Si}$  (001) [70], Y-stabilized  $\text{ZrO}_2$  (111) [71], and GaN/sapphire (0001) [72, 73] and with a wide range of deposition techniques including sputtering [69, 72], spin coating [70], sol-gel processes [74], pulsed laser deposition [75, 76], metal-organic chemical vapor deposition [77], and molecular beam epitaxy [72].

Although thin films of  $\text{YMnO}_3$  typically exhibit a reduction in the ferroelectric polarization as compared to bulk single crystals [67], high quality epitaxial films of  $\text{YMnO}_3$  have also been shown to possess better ferroelectric properties than oriented-polycrystalline films (Fig. 3.5b) [66]. Polarization–electric field ( $P$ – $E$ ) hysteresis loops for  $\text{YMnO}_3$  films have revealed that the saturation polarization in  $\text{YMnO}_3$  is rather small (just a few  $\mu\text{C}/\text{cm}^2$ ) and that films can have a retention time of  $10^4$  s at  $\pm 15$  V applied voltages. Such results have led some to suggest that  $\text{YMnO}_3$  films could be a suitable material for ferroelectric gate field-effect transistors [66], but the high growth temperatures (800 °C [66, 78]–850 °C [79]) make it impractical for integration into current applications. Work has also shown that doping the  $A$ -site with more than 5 %-Bi can decrease the deposition temperatures to under 700 °C without detrimentally affecting the electric properties of the material [79]. Like many other manganites, however,  $A$ -site doping can also have strong effects on the properties of  $\text{YMnO}_3$  [80].  $A$ -site doping with Zr has been shown to decrease leakage currents, while doping with Li and Mg has been found to lead to increases in leakage currents, and finally Li-doping can also drive the antiferromagnetic  $\text{YMnO}_3$  to become a weak ferromagnet [78]. The weak ferromagnetic moment is thought to have arisen from a small canting of the Mn spins. The hope that by controlling the carrier concentration researchers could make the normally antiferromagnetic  $\text{YMnO}_3$  a robust ferromagnet has not been realized. Additionally, doping on the  $B$ -site has been shown to enhance the magnetoelectric coupling in the form of changes in the magnetocapacitance by two orders of magnitude [81].

Over the last few years thin films of a wide range of hexagonal- $\text{REMnO}_3$  materials have been grown. This includes studies of films with  $RE = \text{Nd, Ho, Tm, Lu}$  [82],  $\text{Yb}$  [83], and more recently  $\text{Tb}$  [84],  $\text{Dy, Gd, and Sm}$  [85]. Despite all of this focus, researchers have yet to find a  $\text{REMnO}_3$  compound that exhibits both room temperature ferroelectricity and magnetism, but hexagonal manganites remain a diverse system with intriguing scientific implications for multiferroic materials. An increasing amount of work has been reported on thin films of  $\text{TbMnO}_3$ , including the first report of in early 2005 [86]. Soon after, Lee et al. [84] showed that a hexagonal thin





**Fig. 3.6**  $\text{TbMnO}_3$ . Ferroelectric properties of hexagonal  $\text{TbMnO}_3$  as a function of the electric field at selected temperatures. Polarization versus electric field hysteresis loops measured at 2 kHz at (a) 20 K, (b) 35 K, (c) 70 K, and (d) 100 K. Insets show the hysteresis loops of the dielectric constant versus the electric field at 100 kHz. (e) A phase diagram showing the ferroelectric and antiferroelectric regions as a function of temperature and electric field. The maximum remnant polarization value is also plotted. (Adapted from [84])

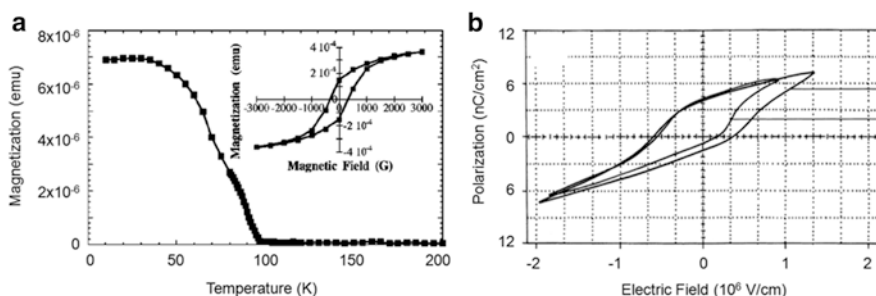
film form of  $\text{TbMnO}_3$  can be stabilized that shows 20 times larger remnant polarization and an increase in the ferroelectric ordering temperature to near 60 K (Fig. 3.6). More recently, studies have also demonstrated the ability to create ferromagnetic interactions (below an ordering temperature of  $\sim 40$  K) in partially strained  $\text{TbMnO}_3$  films on  $\text{SrTiO}_3$  substrates [87, 88] and possible connection between the domain structure of these films and the enhanced magnetization [89]. What has become apparent is that these hexagonal/orthorhombic manganites serve as a model system in the study of the power of thin film epitaxy to engineer new phases and properties—and the role of epitaxial strain in stabilizing the hexagonal- $\text{REMnO}_3$  phases is paramount in creating high quality samples of these materials for further study. Additionally, more recently the  $\text{REMn}_2\text{O}_5$  ( $\text{RE}=\text{rare earth, Y, and Bi}$ ) family of

materials has been studied extensively and has been shown to possess intriguing fundamental physics including coinciding transition temperatures for magnetism and ferroelectricity as well as strong coupling between these order parameters [33]. Prior to 2010, most studies focused on these materials were centered on bulk or single crystal samples and only recently have thin films for these materials been created [90].

### 3.4.2 *BiMnO<sub>3</sub> Thin Films*

Conventional growth of bulk samples of the ferromagnetic, ferroelectric [18]  $\text{BiMnO}_3$  required high temperatures and pressures [91] because the phase is not normally stable at atmospheric pressure. Such phases lend themselves well to thin film growth where epitaxial strain stabilization of metastable phases can be achieved. The first growth of  $\text{BiMnO}_3$  thin films was on  $\text{SrTiO}_3$  (001) single crystal substrates using pulsed laser deposition [92] and was quickly confirmed in other studies [93]. Films of  $\text{BiMnO}_3$  have been found to be ferroelectric below  $\sim 450$  K and undergo an unusual orbital ordering leading to ferromagnetism at  $\sim 105$  K (Fig. 3.7a) [19].

Temperature-dependent magnetic measurements have also shown that the ferromagnetic transition temperature varies depending on the substrate and can be as low as 50 K on  $\text{LaAlO}_3$  [94]. This depression in Curie temperature has been attributed to concepts as varied as stoichiometry issues, strain, and size effects. The ferromagnetic nature of  $\text{BiMnO}_3$  has led some to study it as a potential barrier layer in magnetically and electrically controlled tunnel junctions [95] and eventually led to the production of a four-state memory concept based on La-doped  $\text{BiMnO}_3$  multiferroics [96]. Gajek et al. reported La-doped  $\text{BiMnO}_3$  films that retained their multiferroic character down to thicknesses less than 2 nm and proved that multiferroic materials could be used to create new memories by demonstrating the possibility of spin-dependent tunneling using multiferroic barrier layers in magnetic tunnel junctions.

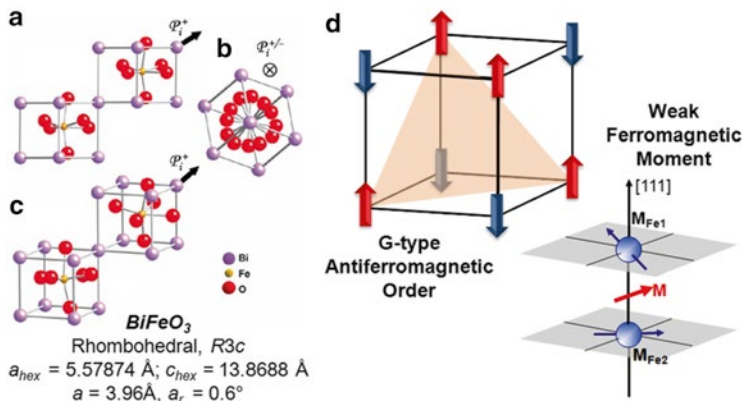


**Fig. 3.7**  $\text{BiMnO}_3$ . (a) Magnetization curve of a  $\text{BiMnO}_3$  film cooled under no applied magnetic field. The *inset* shows the ferromagnetic hysteresis loop at 5 K. (Adapted from [92]) (b)  $P$ - $E$  hysteresis loop of a thin film of  $\text{BiMnO}_3$  on Si (100) above and below the ferromagnetic  $T_C$ . (Adapted from [18])

More recently, significantly La-doped BiMnO<sub>3</sub> films have been shown to exhibit a 70-fold increase in the magnetodielectric effect compared to pure BiMnO<sub>3</sub> [97]. Unfortunately, it coincides with a decrease in the ferroelectric Curie temperature to ~150 K and is observed only at applied magnetic fields of 9T. Additionally, optical second-harmonic measurements with applied electric fields [93], as well as Kelvin force microscopy techniques [94], have been used to confirm the presence of ferroelectric polarization in BiMnO<sub>3</sub> films. High levels of leakage, however, have limited direct  $P$ - $E$  hysteresis loop measurements (Fig. 3.7b) on thin film samples and recently the reanalysis of diffraction data [98] and first-principles calculations [99] have called into question the ferroelectricity in BiMnO<sub>3</sub>. Some calculations have predicted a small polar canting of an otherwise antiferroelectric structure (weak ferroelectricity) that could be used to explain the experimental findings [100]. Regardless, recent studies of dielectric properties of BiMnO<sub>3</sub> thin films done using impedance spectroscopy between 55 and 155 K reveal that there is a large peak in the dielectric permittivity in thin films at the paramagnetic–ferromagnetic transition that could point to indirect coupling effects via the lattice in this material [101].

### 3.4.3 BiFeO<sub>3</sub> Thin Films

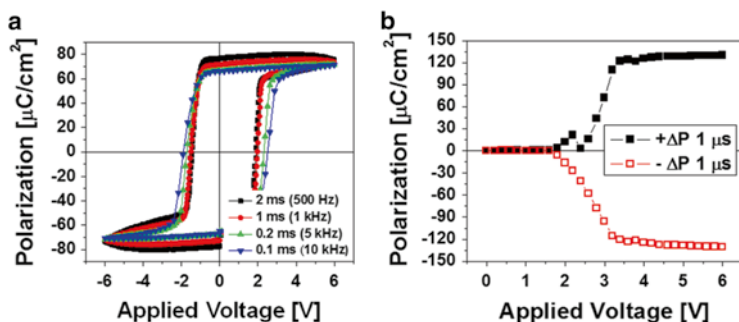
No other single-phase multiferroic has experienced the same level of attention as BiFeO<sub>3</sub> in the last 7 years and because of this we will discuss the evolution of this material in more length. The perovskite BiFeO<sub>3</sub> was first produced in the late 1950s [102] and many of the early studies were focused on the same concepts important today—the potential for magnetoelectric coupling [103]. Throughout the 1960s and 1970s much controversy surrounded the true physical and structural properties of BiFeO<sub>3</sub>, but as early as the 1960s BiFeO<sub>3</sub> was suspected to be an antiferromagnetic, ferroelectric multiferroic [104, 105]. The true ferroelectric nature of BiFeO<sub>3</sub>, however, remained somewhat in question until ferroelectric measurements made at 77 K in 1970 [105] revealed a spontaneous polarization of ~6.1  $\mu\text{C}/\text{cm}^2$  along the 111-direction which were found to be consistent with the rhombohedral polar space group  $R3c$  determined from single crystal X-ray diffraction [106] and neutron diffraction studies [107]. These findings were at last confirmed by detailed structural characterization of ferroelectric/ferroelastic monodomain single crystal samples of BiFeO<sub>3</sub> in the late 1980s [103]. Chemical etching experiments on ferroelastic single domains later proved without a doubt that the BiFeO<sub>3</sub> was indeed polar, putting to rest the hypothesis that BiFeO<sub>3</sub> might be antiferroelectric, and proved that the ferroelectric/ferroelastic phase was stable from 4 K to ~1,103 K [108]. The structure of BiFeO<sub>3</sub> can be characterized by two distorted perovskite blocks connected along their body diagonal or the pseudocubic  $\langle 111 \rangle$ , to build a rhombohedral unit cell (Fig. 3.8a). In this structure the two oxygen octahedra of the cells connected along the  $\langle 111 \rangle$  are rotated clockwise and counterclockwise around the  $\langle 111 \rangle$  by  $\pm 13.8(3)^\circ$  and the Fe-ion is shifted by 0.135 Å along the same axis away from the oxygen octahedron center position. The ferroelectric state is realized by a large displacement of the Bi-ions relative to the FeO<sub>6</sub> octahedra (Fig. 3.8a–c) [103, 111].



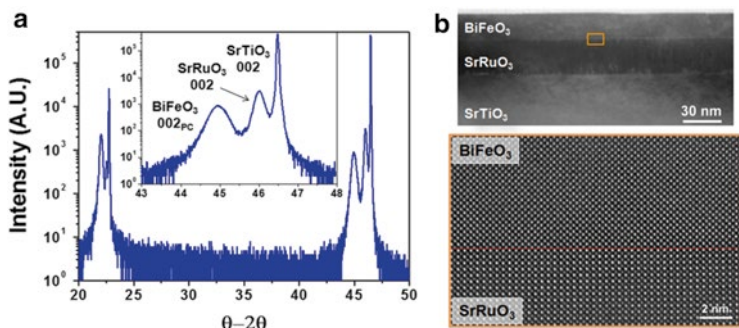
**Fig. 3.8** BiFeO<sub>3</sub>. (a) Structure of BiFeO<sub>3</sub> shown looking (a) down the pseudocubic-[109], (b) down the pseudocubic-[110] polarization direction, and (c) a general three-dimensional view of the structure. (d) The magnetic structure of BiFeO<sub>3</sub> is shown including G-type antiferromagnetic ordering and the formation of the weak ferromagnetic moment. (Adapted from [7])

During the 1980s, the magnetic nature of BiFeO<sub>3</sub> was studied in detail. Early studies indicated that BiFeO<sub>3</sub> was a G-type antiferromagnet (G-type antiferromagnetic order is shown schematically in Fig. 3.8d) with a Néel temperature of  $\sim 673 \text{ K}$  [112] and possessed a cycloidal spin structure with a period of  $\sim 620 \text{ \AA}$  [113]. This spin structure was found to be incommensurate with the structural lattice and was superimposed on the antiferromagnetic order. It was also noted that if the moments were oriented perpendicular to the  $\langle 111 \rangle$ -polarization direction the symmetry also permits a small canting of the moments in the structure resulting in a weak ferromagnetic moment of the Dzyaloshinskii–Moriya type (Fig. 3.8d) [35, 36].

In 2003 a paper focusing on the growth and properties of thin films of BiFeO<sub>3</sub> spawned a hailstorm of research into thin films of BiFeO<sub>3</sub> that continues to the present day. The paper reported enhancements of polarization and related properties in heteroepitaxially constrained thin films of BiFeO<sub>3</sub> [17]. Structural analysis of the films suggested differences between films (with a monoclinic structure) and bulk single crystals (with a rhombohedral structure) as well as enhancement of the polarization up to  $\sim 90 \mu\text{C}/\text{cm}^2$  at room temperature and enhanced thickness-dependent magnetism compared to bulk samples. In reality, the high values of polarization observed actually represented the intrinsic polarization of BiFeO<sub>3</sub>. Limitations in the quality of bulk crystals had kept researchers from observing such high polarization values until much later in bulk samples [109]. More importantly this report indicated a magnetoelectric coupling coefficient as high as  $3 \text{ V}/\text{cm Oe}$  at zero applied field [17]. A series of detailed first-principles calculations utilizing the local spin-density approximation (LSDA) and LSDA+U methods helped shed light on the findings in this paper. Calculations of the spontaneous polarization in BiFeO<sub>3</sub> suggested a value between  $90$  and  $100 \mu\text{C}/\text{cm}^2$  (consistent with those measured in 2003) [110] which have since been confirmed by many other experimental reports (an example is shown in Fig. 3.9) [114].



**Fig. 3.9** (a) Ferroelectric polarization—electric field hysteresis loop of epitaxial  $\text{BiFeO}_3$  thin film measured at various frequencies and (b) PUND measurement for varying voltages at 1  $\mu\text{s}$  voltage pulses. (Adapted from [114])



**Fig. 3.10** (a) X-ray diffraction results from a fully epitaxial, single-phase  $\text{BiFeO}_3/\text{SrRuO}_3/\text{SrTiO}_3$  (001) heterostructure. (b) Low- and high-resolution transmission electron microscopy images of this same heterostructure (adapted from [7])

Today, much progress has been made in understanding the structure, properties, and growth of thin films of  $\text{BiFeO}_3$ . High quality epitaxial  $\text{BiFeO}_3$  films have been grown via molecular beam epitaxy [115, 116], pulsed laser deposition [17, 117], radio-frequency (RF) sputtering [118, 119], metal-organic chemical vapor deposition (MOCVD) [120, 121], and chemical solution deposition (CSD) [122] on a wide range of substrates including traditional oxide substrates as well as Si [117, 123] and GaN [124]. This work has shown that high quality films, like those shown in Fig. 3.10 can be produced. Typical XRD  $\theta-2\theta$  measurements (Fig. 3.10a) show the ability of researchers to produce high quality, fully epitaxial, single-phase films of  $\text{BiFeO}_3$  (data here is for a  $\text{BiFeO}_3/\text{SrRuO}_3/\text{SrTiO}_3$  (001) heterostructure). Detailed XRD analysis has shown that films possess a monoclinic distortion of the bulk rhombohedral structure over a wide range of thicknesses, but the true structure of very thin films (<15 nm) remains unclear [125]. The quality of such heterostructures as produced by pulsed laser deposition can be probed further by transmission electron microscopy (TEM) (Fig. 3.10b). TEM imaging reveals films that are uniform

over large areas and with the use of high-resolution TEM we can examine the atomically abrupt, smooth, and coherent interface between  $\text{BiFeO}_3$  and a commonly used bottom electrode material  $\text{SrRuO}_3$ .

### 3.4.3.1 Controlling Domain Structures in $\text{BiFeO}_3$

Today, aided by such thin film synthesis techniques, significant advances have been made in controlling domain structures in thin films of  $\text{BiFeO}_3$ . This work, in turn, has enabled significant progress in the understanding of this complex multiferroic material. In addition to being of great interest for photonic devices, nanolithography, and more, fine control of the domain structures and the ability to create extremely high quality thin films of these materials make it possible to probe a number of important questions related to this material. To begin this discussion, it is essential that we first understand what kinds of domain patterns can be obtained in rhombohedral ferroelectrics. Several theoretical studies have been published that provide equilibrium domain patterns of rhombohedral ferroelectrics such as  $\text{BiFeO}_3$ . On the  $(001)_c$  perovskite surface, there are eight possible ferroelectric polarization directions corresponding to four structural variants of the rhombohedral ferroelectric. Early work published by Streiffer et al. [126] found that domain patterns can develop with either  $\{100\}_c$  or  $\{101\}_c$  boundaries for  $(001)_c$  oriented rhombohedral films. In both cases, the individual domains in the patterns are energetically degenerate and thus equal width stripe patterns are theoretically predicted. Zhang et al. [127] have gone on to use phase field simulations to understand how strain state can affect the polarization variants and to predict the domain structures in epitaxial  $\text{BiFeO}_3$  thin films with different orientations. In these models, long-range elastic and electrostatic interactions were taken into account as were the effects of various types of substrate constraints on the domain patterns. These findings suggest that the domain structure of  $\text{BiFeO}_3$  thin films can be controlled by selecting proper film orientations and strain constraints. Moreover, these phenomenological analyses reveal that both the depolarization energy and the elastic energy play a key role in determining the equilibrium domain structures. For instance, in the case of an asymmetrical electrostatic boundary condition (i.e., the presence of a bottom electrode) the dominant domain scaling mechanism changes from electrostatic-driven to elastic-driven. Therefore, the domain size scaling law in epitaxial  $\text{BiFeO}_3$  films is predicted to show a different behavior from the conventional elastic domains: the 101-type or the so-called  $71^\circ$  domains are expected to be much wider than the 100-type or the so-called  $109^\circ$  domains despite the fact that these  $\{100\}$  boundaries possess a larger domain wall energy.

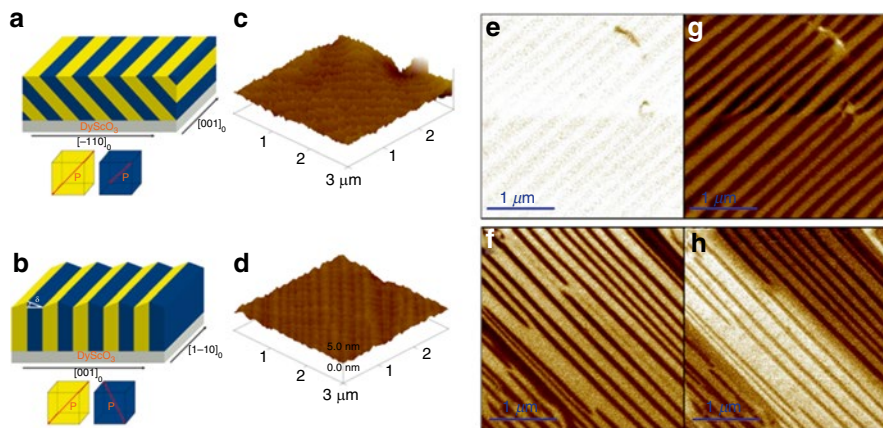
Experimental demonstration of similar ideas has progressed in recent years. In 2006, Chu et al. [128] demonstrated an approach to create one-dimensional nanoscale arrays of domain walls in epitaxial  $\text{BiFeO}_3$  films. Focusing on  $\text{BiFeO}_3/\text{SrRuO}_3/\text{DyScO}_3$  (110) heterostructures, the authors took advantage of the close lattice matching between  $\text{BiFeO}_3$ ,  $\text{SrRuO}_3$ , and  $\text{DyScO}_3$  (110) and the anisotropic in-plane lattice parameters of  $\text{DyScO}_3$  ( $a_1=3.951 \text{ \AA}$  and  $a_2=3.946 \text{ \AA}$ ) to pin the



structure of the  $\text{SrRuO}_3$  layer and, in turn, the ferroelectric domain structure of  $\text{BiFeO}_3$ . This anisotropic in-plane strain condition leads to the exclusion of two of the possible structural variants. Phase field modeling of the ferroelectric domain structure in such heterostructures predicted stripe-like ferroelectric domain structures which were confirmed in the final  $\text{BiFeO}_3$  films. The growth mechanism of the underlying SRO layer was found to be important in determining the final ferroelectric domain structure of the  $\text{BiFeO}_3$  films. SRO layers grown via step-bunching and step-flow growth mechanisms resulted in ferroelectric domain structures with 4-polarization variants and 2-polarization variants, respectively. These films have been shown to exhibit excellent ferroelectric properties with room temperature  $2P_r = 120\text{--}130 \mu\text{C}/\text{cm}^2$  and strong intrinsic ferroelectric properties [114].

In 2007, Chu et al. [129] further demonstrated the ability to create different domain structures in epitaxial  $\text{BiFeO}_3$  films on (001), (110), and (111)  $\text{SrTiO}_3$  substrates that were consistent with phase field models. Such a result made a connection between the theoretical predictions and experiments and offered one pathway for researchers to simplify the complex domain structure of the  $\text{BiFeO}_3$  films. What was discovered was that one must induce a break in the symmetry of the various ferroelectric variants. One avenue to accomplish this is through the use of vicinal  $\text{SrTiO}_3$  substrates. Beginning with a (001) oriented substrate, one can progressively tilt the crystal along different directions to end up with different orientations. For instance, by tilting  $45^\circ$  along the 010-direction one can obtain a (110) oriented substrate, while tilting by another  $45^\circ$  along the 110-direction gives rise to a (111) oriented substrate. Through the use of carefully controlled, vicinally cut (001)  $\text{SrTiO}_3$  substrates researchers were able to demonstrate fine control of the ferroelectric domain structure in  $\text{BiFeO}_3$ . This includes evolving the domain structure from possessing 4-variants, 2-variants, and 1-variant. Added control comes from the use of asymmetric boundary conditions including the use of  $\text{SrRuO}_3$  bottom electrodes that drives the out-of-plane component of polarization to be preferentially downward pointing. Other reports have also demonstrated similar findings in films grown on highly miscut  $\text{SrTiO}_3$  (001) substrates [119]. These films represent an important step forward in that they provide a set of model thin films that can be used to further explore the magnetoelectric properties of this system as well as its interactions with other layers. Additionally, multiferroic materials with electrically controllable periodic domain structures such as these could be of great interest for applications in photonic devices.

Finally, in 2009, Chu et al. [130], through the careful control of electrostatic boundary conditions, such as the thickness of the underlying  $\text{SrRuO}_3$  bottom electrode, were able to demonstrate the creation of ordered arrays of the prototypical domain structures as predicted by Streiffer et al. nearly 10 years earlier [126] (Fig. 3.11a, b). Figure 3.11a represents a series of  $71^\circ$  domain walls located on 101-type planes and Fig. 3.11b represents a series of  $109^\circ$  domain walls located on 100-type planes. When the bottom electrode layer is thick (typically  $>10$  nm and thus a good metal) the presence of an asymmetric boundary condition results in the formation of a film that is fully out-of-plane polarized downward towards the  $\text{SrRuO}_3$  layer and elastic energy is the dominant energy in the system. On the other



**Fig. 3.11** Ordered arrays of ferroelectric domains and domain walls. (a) and (b) Schematics of equilibrium structure of an ordered array of 71° and 109° domain walls, respectively. (c) and (d) Surface topography as measured by AFM of 71° and 109° domain walls samples, respectively. Out-of-plane (e) and (f) as well as in-plane (g) and (h) PFM images for samples possessing ordered arrays of 71° and 109° domain walls. (Adapted from [130])

hand, when the  $\text{SrRuO}_3$  layer is very thin, electrostatic energy becomes the dominant energy and drives the film to have domains alternatively pointing up and down. The surface morphology of the resulting films with 71° (Fig. 3.11c) and 109° (Fig. 3.11d) is consistent with the theoretically predicted structure. The corresponding out-of-plane (Fig. 3.11e, f) and in-plane (Fig. 3.11g, h) PFM images confirm the presence of the periodic, equilibrium domain structures. Similarly, studies focused on  $\text{BiFeO}_3$  films grown on the new substrate  $\text{TbScO}_3$  (which has  $<-0.3\%$  lattice mismatch with  $\text{BiFeO}_3$ ) resulted in  $\text{BiFeO}_3$  films possessing ordered arrays of (010) domain walls [131].

In addition to epitaxial growth control of ferroelectric domain structures, recent advances in scanning probe-based manipulation of ferroelectric domain structures have opened up the next level of control. Zavaliche et al. [111] have developed a standard procedure to use PFM to characterize and understand the domain structure of such ferroelectric materials. These studies have identified locally three possible polarization switching mechanisms namely 71°, 109°, and 180° rotations of the polarization direction. 180° polarization reversals appear to be the most favorable switching mechanism in epitaxial films under an applied bias along [001]. A combination of phase field modeling and scanning force microscopy of carefully controlled, epitaxial [109]  $\text{BiFeO}_3$  films with a simplified domain structure revealed that the polarization state can be switched by all three primary switching events by selecting the direction and magnitude of the applied voltage [132]. Moreover, the instability of certain ferroelastic switching processes and domains can be dramatically altered through a judicious selection of neighboring domain walls. The symmetry breaking of the rotationally invariant tip field by tip motion enables deter-



ministic control of non-180° switching in rhombohedral ferroelectrics. The authors also demonstrated the controlled creation of a ferrotoroidal order parameter. The ability to control local elastic, magnetic and toroidal order parameters with an electric field will make it possible to probe local strain and magnetic ordering, and engineer various magnetoelectric, domain-wall-based and strain-coupled devices.

For eventual device applications, the use of a coplanar epitaxial electrode geometry has been proposed to aid in controlling multiferroic switching in BiFeO<sub>3</sub> [133]. PFM has been used to detect and manipulate the striped ferroelectric domain structure of a BiFeO<sub>3</sub> thin film grown on DyScO<sub>3</sub> (110) substrates. Time-resolved imaging revealed ferroelastic switching of domains in a needle-like region that grew from one electrode toward the other. Purely ferroelectric switching was suppressed by the geometry of the electrodes. Such results demonstrate the capability to control the ferroelectric order parameter and domain structures in device architectures.

### 3.4.3.2 Evolution of Magnetism and Domain Wall Functionality in BiFeO<sub>3</sub>

The ability to control domain structures has also been demonstrated to have serious implications for the evolution of magnetism in thin films (i.e., variations from the bulk picture and the mechanism of enhanced magnetism in thin films) and has suggested the strong role of domain walls in determining macroscopic properties. In this section we investigate the evolution of magnetic properties in BiFeO<sub>3</sub>.

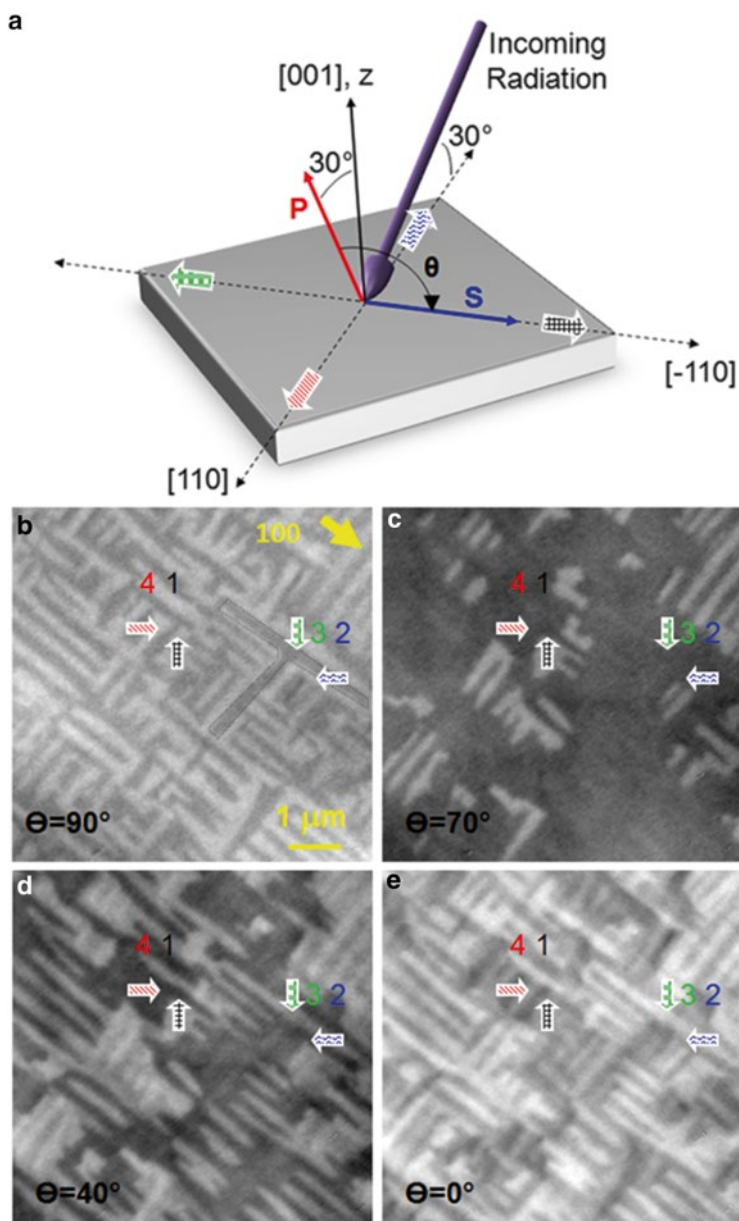
Early theoretical treatments attempted to understand the nature of magnetism and coupling between order parameters in BiFeO<sub>3</sub>. Such calculations confirmed the possibility of weak ferromagnetism arising from a canting of the antiferromagnetic moments in BiFeO<sub>3</sub>. The canting angle was calculated to be ~1° and would result in a small, but measurable, magnetization of ~8 emu/cm<sup>3</sup> or ~0.05 μ<sub>B</sub> per unit cell [134]. It was also found that the magnetization should be confined to an energetically degenerate easy {111} perpendicular to the polarization direction in BiFeO<sub>3</sub>. These same calculations further discussed the connection of the weak ferromagnetism and the structure (and therefore ferroelectric nature) of BiFeO<sub>3</sub>. This allowed the authors to extract three conditions necessary to achieve electric-field-induced magnetization reversal (1) the rotational and polar distortions must be coupled; (2) the degeneracy between different configurations of polarization and magnetization alignment must be broken; (3) there must be only one easy magnetization axis in the (111) which could be easily achieved by straining the material [134].

This work coincided with considerable experimental work reporting on the nature of magnetism in thin film BiFeO<sub>3</sub>. This subject, although contentious for some time, appears to be nearly fully understood. The original work of Wang et al. presented an anomalously large value of magnetic moment (of the order of 70 emu/cm<sup>3</sup>) [17], which is significantly higher than the expected canted moment of ~8 emu/cm<sup>3</sup>. There have been several studies aimed at clarifying the origins of this anomalous magnetism. Eerenstein et al. [135] proposed that the excess magnetism was associated with magnetic second phases (such as γ-Fe<sub>2</sub>O<sub>3</sub>); this was supported by

the studies of Béa et al. [136] who showed that  $\text{BiFeO}_3$  films, when grown under reducing conditions (for example, under oxygen pressures lower than  $1 \times 10^{-3}$  Torr) showed enhanced magnetism as a consequence of the formation of magnetic second phases. It is, however, important to note that low oxygen pressure during growth is not the cause for the enhanced moment in the 2003 report by Wang et al. where films were grown in oxygen pressures between 100 and 200 mTorr and cooled in 760 Torr rendering formation of such secondary magnetic phases thermodynamically unlikely and there was no evidence (despite extensive study of samples with X-ray diffraction and transmission electron microscopy techniques) for such second phases. Furthermore, subsequent X-ray magnetic circular dichroism studies supported the assertion that this magnetism is *not* from a magnetic  $\gamma\text{-Fe}_2\text{O}_3$  impurity phase [137]. To date, additional mixed reports—including reports of enhanced magnetism in nanoparticles of  $\text{BiFeO}_3$  [138] as well as the observation of samples exhibiting no such enhancement—have been presented.

What has emerged, however, is that the synthesis process can have considerable effect on the overall magnetic properties of this complex material—especially in the study of epitaxially strained thin films. For instance, Ederer and Spaldin found that only one easy magnetization axis in the energetically degenerate 111-plane of  $\text{BiFeO}_3$  might be selected when one was to strain the material appropriately [134]. Until recently this scientifically and technologically important question of how magnetic order in multiferroics such as  $\text{BiFeO}_3$  develops with strain and size effects had remained unanswered. In early 2010, using angle and temperature-dependent dichroic measurements and photoemission spectromicroscopy (Fig. 3.12), Holcomb et al. [139] discovered that the antiferromagnetic order in  $\text{BiFeO}_3$  did indeed evolve and change systematically as a function of thickness and strain. Lattice mismatch induced strain was found to break the easy-plane magnetic symmetry of the bulk and leads to an easy axis of magnetization that can be controlled via the sign of the strain—110-type for tensile strain and 112-type for compressive strain. This understanding of the evolution of magnetic structure and the ability to manipulate the magnetism in this model multiferroic has significant implications for eventual utilization of such magnetoelectric materials in applications.

Also during the last few years, a number of exciting findings have come to light that are poised to definitively answer the questions surrounding the wide array of magnetic properties observed in  $\text{BiFeO}_3$  thin films. There is now a growing consensus that epitaxial films (with a thickness less than  $\sim 100$  nm) are highly strained and thus the crystal structure is more akin to a monoclinic phase rather than the bulk rhombohedral structure. Furthermore, a systematic dependence of the ferroelectric domain structure in films as a function of the growth rate has been observed [140]. Films grown very slowly (for example by MBE, laser-MBE, or off-axis sputtering) exhibit a classical stripe-like domain structure that is similar to ferroelastic domains in tetragonal  $\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$  films. Due to symmetry considerations, two sets of such twins are observed. These twins are made up of  $71^\circ$  ferroelastic walls, that form on the  $\{101\}$ -type planes (which is a symmetry plane). In contrast, if the films are grown rapidly (as was done in the original work of Wang et al. [17]) the domain structure is dramatically different. It now resembles a mosaic-like ensemble that

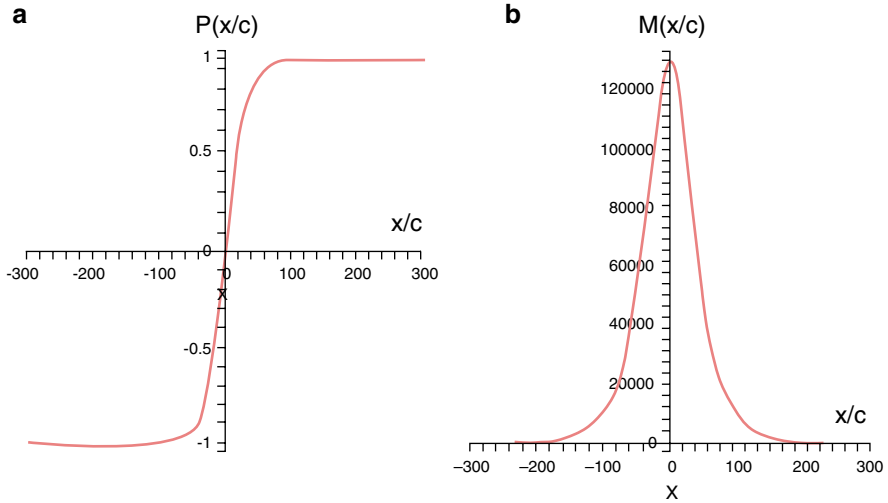


**Fig. 3.12** (a) Schematic illustrating the experimental geometries used to probe the angle dependent linear dichroism in BiFeO<sub>3</sub>. Photoemission electron microscopy images of BiFeO<sub>3</sub> at several angles of the electric vector of incident linear polarization  $\alpha$ . The outlined arrows show the in-plane projection of the four ferroelectric directions. Images of domain structures taken at (b)  $\theta = 90^\circ$ , (c)  $\theta = 70^\circ$ , (d)  $\theta = 40^\circ$ , and (e)  $\theta = 0^\circ$  (adapted from [139])

consists of a dense distribution of  $71^\circ$ ,  $109^\circ$ , and  $180^\circ$  domain walls. It should be noted that  $109^\circ$  domain walls form on  $\{001\}$ -type planes (which is not a symmetry plane for this structure). Preliminary measurements reveal a systematic difference in magnetic moment between samples possessing different types and distributions of domain walls. The work of Martin et al. [140] suggests that such domain walls could play a key role in the many observations of enhanced magnetic moment in  $\text{BiFeO}_3$  thin films.

This suggestion builds off of the work of Přívratká and Janovec [141, 142], where detailed symmetry analyses were used to conclude that magnetoelectric coupling could lead to the appearance of a net magnetization in the middle of antiferromagnetic domain walls. Specifically, they showed that this effect is allowed for materials with the  $R3c$  space group (i.e., that observed for  $\text{BiFeO}_3$ ). Although such analysis raises the possibility of such an effect, the group-symmetry arguments do not allow for any quantitative estimate of that moment. The idea that novel properties could occur at domain walls in materials presented by Přívratká and Janovec is part of a larger field of study of the morphology and properties of domains and their walls that has taken place over the last 50 years with increasing recent attention given to the study novel functionality at domain walls [143–145]. For instance, recent work has demonstrated that spin rotations across ferromagnetic domain walls in insulating ferromagnets can induce a local polarization in the walls of otherwise non-polar materials [2, 145], preferential doping along domain walls has been reported to induce 2D superconductivity in  $\text{WO}_{3-x}$  [146] and enhanced resistivity in phosphates [147], while in paraelectric (non-polar)  $\text{SrTiO}_3$  the ferroelastic domain walls appear to be ferroelectrically polarized [148]. Taking this idea one step further, Daraktchiev et al. [149, 150] have proposed a thermodynamic (Landau-type) model with the aim of quantitatively estimating whether the walls of  $\text{BiFeO}_3$  can be magnetic and, if so, to what extent they might contribute to the observed enhancement of magnetization in ultrathin films. One can develop a simple thermodynamic potential incorporating two order parameters expanded up to  $P^6$  and  $M^6$  terms (the transitions in  $\text{BiFeO}_3$  are found experimentally to be first order, and the low-symmetry  $(\pm P_0, 0)$  phase is described here) with biquadratic coupling between the two order parameters (biquadratic coupling is always allowed by symmetry, and therefore always present in any system with two order parameters). Because biquadratic free energy terms such as  $P^2M^2$  are scalars in any symmetry group, this potential can be written thusly:

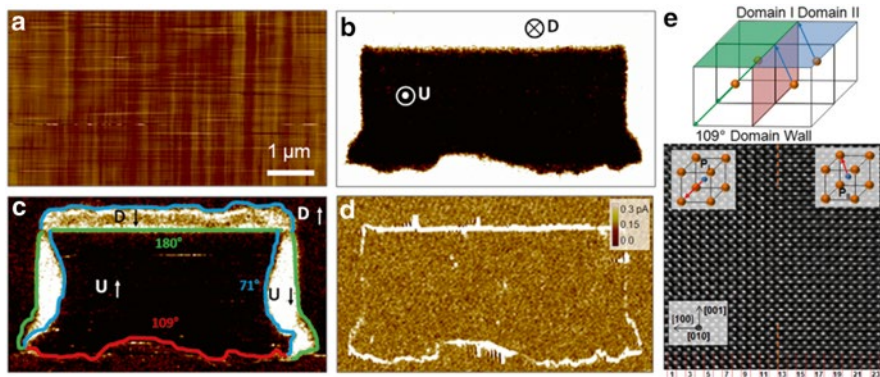
$$\begin{aligned}
 G_{\text{MP}} &= G_0 + \frac{\kappa}{2}(\nabla P)^2 + \frac{\lambda}{2}(\nabla M)^2 + L_{\text{MP}}(P, M) \\
 &= G_0 + \frac{\kappa}{2}(\nabla P)^2 + \frac{\lambda}{2}(\nabla M)^2 + \frac{\alpha}{2}P^2 + \frac{\beta}{4}P^4 + \frac{\eta}{6}P^6 \\
 &\quad + \frac{a}{2}M^2 + \frac{b}{4}M^4 + \frac{n}{6}M^6 + \frac{\gamma}{2}P^2M^2
 \end{aligned} \tag{3.4}$$



**Fig. 3.13** Shape of (a) ferroelectric polarization and (b) magnetism across a domain wall in BiFeO<sub>3</sub> (adapted from [149, 150])

When one goes from  $+P$  to  $-P$ , it is energetically more favorable for the domain wall energy trajectory not to go through the center of the landscape ( $P=0, M=0$ ), but to take a diversion through the saddle points at  $M_0 \neq 0$ , thus giving rise to a finite magnetization (Fig. 3.13). The absolute values of the magnetic moment at the domain wall will depend on the values of the Landau coefficients as well as the boundary conditions imposed on the system, namely whether the material is magnetically ordered or not. Analysis of the phase space of this thermodynamic potential shows that it is possible for net magnetization to appear in the middle of ferroelectric walls even when the domains themselves are not ferromagnetic (Fig. 3.13b). The authors of this model note, however, that it is presently only a *toy model* which does not take into account the exact symmetry of BiFeO<sub>3</sub>, so it cannot yet quantitatively estimate how much domain walls can contribute to the magnetization. The exact theory of magnetoelectric coupling at the domain walls of BiFeO<sub>3</sub> also remains to be formulated.

Recently, a holistic picture of the connection between processing, structure, and properties has brought to light the role of magnetism at ferroelectric domain walls in determining the magnetic properties in BiFeO<sub>3</sub> thin films. By controlling domain structures through epitaxial growth constraints and probing these domain walls with a range of techniques (including detailed magnetotransport studies) He et al. [151] have demonstrated that the formation of certain types of ferroelectric domain walls (i.e., 109° walls) can lead to enhanced magnetic moments in BiFeO<sub>3</sub>. Building off of the work of Martin et al. [140], the authors of this study were able to demonstrate that samples possessing 109° domain walls show significant magnetoresistance (up



**Fig. 3.14** Conduction at domain walls in  $\text{BiFeO}_3$ . (a) Topographic image of the surface of a model  $\text{BiFeO}_3/\text{SrRuO}_3/\text{SrTiO}_3$  (110) sample. Corresponding (b) out-of-plane and (c) in-plane piezoresponse force microscopy image of an electrically poled region of this film. (d) Conducting-atomic force microscopy image reveals that  $109^\circ$  and  $180^\circ$  domain walls are conducting. (e) Schematic illustration of a  $109^\circ$  domain wall and a corresponding high-resolution transmission electron microscopy image of a  $109^\circ$  domain wall (adapted from [152])

to 60 %). In summary, it appears certain domain walls can give rise to enhanced magnetic behavior in  $\text{BiFeO}_3$  thin films.

It is also important to note that Seidel et al. [152], motivated by the desire to understand similar magnetic properties at domain walls in  $\text{BiFeO}_3$ , undertook a detailed scanning probe-based study of these materials and discovered a new and previously unanticipated finding: the observation of room temperature electronic conductivity at certain ferroelectric domain walls. The origin of the observed conductivity was explored using high-resolution transmission electron microscopy and first-principles density functional computations. The results showed that domain walls in a multiferroic ferroelectric such as  $\text{BiFeO}_3$  can exhibit unusual electronic transport behavior on a local scale that is quite different from that in the bulk of the material. Using a model (110)-oriented  $\text{BiFeO}_3/\text{SrRuO}_3/\text{SrTiO}_3$  heterostructure with a smooth surface (Fig. 3.14a), the researchers were able to switch the  $\text{BiFeO}_3$  material in such a way that enabled them to create all the different types of domain walls possible in  $\text{BiFeO}_3$  (i.e.,  $71^\circ$ ,  $109^\circ$ , and  $180^\circ$  domain walls) in a local region (Fig. 3.14b, c). Conducting-atomic force microscopy (c-AFM) measurements (Fig. 3.14d) revealed conduction at  $109^\circ$  and  $180^\circ$  domain walls. Detailed high-resolution transmission electron microscopy studies (Fig. 3.14e) revealed this conductivity was, in part, structurally induced and can be activated and controlled on the scale of the domain wall width—about 2 nm in  $\text{BiFeO}_3$ . From the combined study of conductivity measurements, electron microscopy analysis, and density functional theory calculations, two possible mechanisms for the observed conductivity at the domain walls have been suggested: (1) an increased carrier density as a consequence of the formation of an electrostatic potential step at the wall; and/or (2)

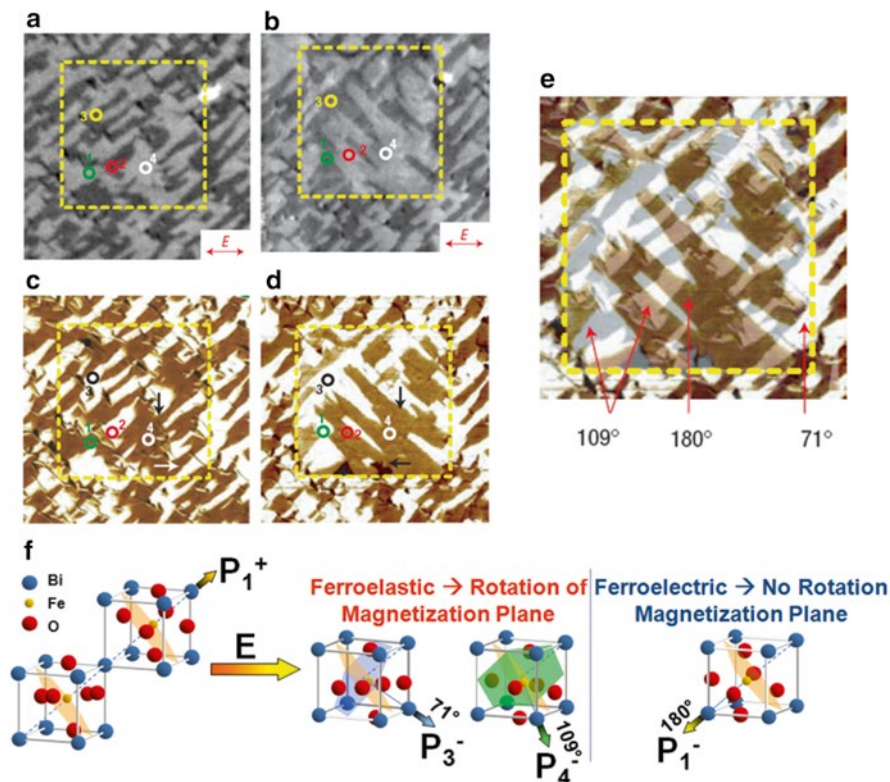
a decrease in the band gap within the wall and corresponding reduction in band offset with the *c*-AFM tip. It was noted that both possibilities are the result of structural changes at the wall and both may, in principle, be acting simultaneously, since they are not mutually exclusive.

It is important to step back and recognize the importance of these discoveries and the implications for this work on memory applications. For some time now, domain walls in ferromagnets have been explored for logic and storage applications (see, for example, [153]). Since 2000 there has been increasing effort to probe domain walls in materials for functional devices—including the pioneering work of Allwood et al. [154] who identified possible circuit manifestations for AND and NOR gates using magnetic domain walls. More recently, domain walls in other systems—especially ferroelectric and multiferroic systems—have joined the fray. The observation of conducting domain walls provides an exciting opportunity to create yet another pathway by which it might be possible to store information. This would be particularly facilitated if the conduction at the walls were to be made significantly larger. Research in this direction, however, is still in its infancy, but this topic appears to be an attractive topic for future research. An insulator–metal transition would be a highly desirable pathway to accomplish such large changes in conduction, that are controllable with electric fields. Finally, E. Salje recently summarized the status and promise of twin boundaries in ferroelectrics, as well as curved interfaces between crystalline and amorphous materials, for future device applications [155]. In the end, interface engineering has experienced a great increase in attention of the last decade and the development of new phenomena at interfaces is poised to enable new devices and applications in the future.

### 3.4.3.3 Magnetoelectric Coupling in BiFeO<sub>3</sub>

Although many researchers anticipated strong magnetoelectric coupling in BiFeO<sub>3</sub>, until the first evidence for this coupling in 2003 there was no definitive proof. Two years after this first evidence, a detailed report was published in which researchers observed the first visual evidence for electrical control of antiferromagnetic domain structures in a single-phase multiferroic at room temperature. By combining X-ray photoemission electron microscopy (PEEM) imaging of antiferromagnetic domains (Fig. 3.15a, b) and piezoresponse force microscopy (PFM) imaging of ferroelectric domains (Fig. 3.15c, d) the researchers were able to observe direct changes in the nature of the antiferromagnetic domain structure in BiFeO<sub>3</sub> with application of an applied electric field (Fig. 3.15e) [156]. This research showed that the ferroelastic switching events (i.e., 71° and 109°) resulted in a corresponding rotation of the magnetization plane in BiFeO<sub>3</sub> (Fig. 3.15f) and has paved the way for further study of this material in attempts to gain room temperature control of ferromagnetism (to be discussed in detail later). This work has since been confirmed by neutron diffraction experiments in single crystal BiFeO<sub>3</sub> as well [157, 158].





**Fig. 3.15** Determination of strong magnetoelastic coupling in BiFeO<sub>3</sub>. Photoemission electron microscopy (PEEM) images before (a) and after (b) electric field poling. The arrows show the X-ray polarization direction during the measurements. In-plane piezoresponse force microscopy images before (c) and after (d) electric field poling. The arrows show the direction of the in-plane component of ferroelectric polarization. Regions 1 and 2 (marked with green and red circles, respectively) correspond to 109° ferroelectric switching, whereas 3 (black and yellow circles) and 4 (white circles) correspond to 71° and 180° switching, respectively. In regions 1 and 2 the PEEM contrast reverses after electrical poling. (e) A superposition of in-plane PFM scans shown in (c) and (d) used to identify the different switching mechanisms that appear with different colors and are labeled in the figure (adapted from [156]). (f) Schematic illustration of coupling between ferroelectricity and antiferromagnetism in BiFeO<sub>3</sub>. Upon electrically switching BiFeO<sub>3</sub> by the appropriate ferroelastic switching events (i.e., 71° and 109° changes in polarization) a corresponding change in the nature of antiferromagnetism is observed

#### 3.4.3.4 Routes to Enhance Properties in BiFeO<sub>3</sub>

One considerable challenge to the full acceptance of BiFeO<sub>3</sub> into modern technology has been the traditionally leaky nature of this material. Unlike more traditional ferroelectric materials—which are robust electronic insulators—multiferroic materials such as BiFeO<sub>3</sub> are asked to perform multiple tasks (i.e., magnetism and ferroelectricity) and thus the electronic structure is highly susceptible to defects which



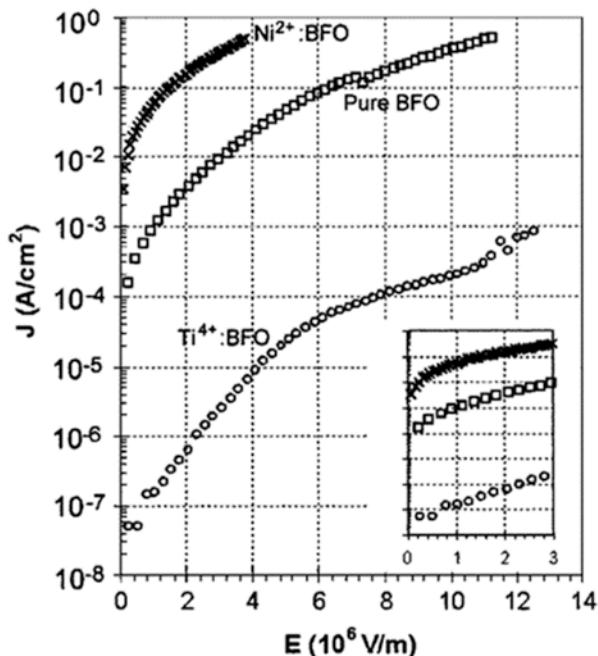
can reduce the resistance of the material. In turn, researchers have attempted to take head-on the common challenges that have traditionally limited the widespread usage of such materials in devices—high leakage currents, small remnant polarizations, high coercive fields, ferroelectric reliability, and inhomogeneous magnetic spin structures [159]. The most common practice in this spirit is to study doped or alloyed (here used interchangeably)  $\text{BiFeO}_3$  thin films (both *A*-site and *B*-site doping) in an attempt to improve these various areas of concern. In this section we will describe the work done to date on chemical routes to control properties in  $\text{BiFeO}_3$ .

Following the rejuvenation of interest in  $\text{BiFeO}_3$  in the early 2000s, a number of studies came forth aimed at understanding how to enhance properties in this exciting material. One of the earliest studies looked at alloying the *B*-site of  $\text{BiFeO}_3$  with the transition metal ions  $\text{Ti}^{4+}$  and  $\text{Ni}^{2+}$  which are similar in size to the  $\text{Fe}^{3+}$  ion [160]. The idea was that the addition of 4+ ions into the  $\text{BiFeO}_3$  would require charge compensation which would be achieved either by filling of oxygen vacancies, decreasing the valence of the Fe-ions, or creation of cation vacancies. On the other hand, addition of 2+ ions would likely create anion vacancies or change the Fe-ion valence. In the end the hope was that  $\text{Ti}^{4+}$  alloying would help to eliminate oxygen vacancies and  $\text{Ni}^{2+}$  alloying would introduce more oxygen vacancies. This study, in turn, showed that alloying with  $\text{Ti}^{4+}$  led to an increase in film resistivity by over three orders of magnitude while doping with  $\text{Ni}^{2+}$  resulted in a decrease in resistivity by over two orders of magnitude (Fig. 3.16). Additionally, the study suggested that the current–voltage behavior was affected by the alloying and that increased densities of oxygen vacancies lead to higher levels of free carriers and higher conductivity. Over the next few years numerous other reports of the effect of alloying on the properties of  $\text{BiFeO}_3$  were published. Other studies also focused on *B*-site alloying, including alloying with Nd which helped to enhance piezoelectricity in the films and improve electric properties [161, 162], doping with Cr which was shown to greatly reduce leakage currents in  $\text{BiFeO}_3$  films [163], and others.

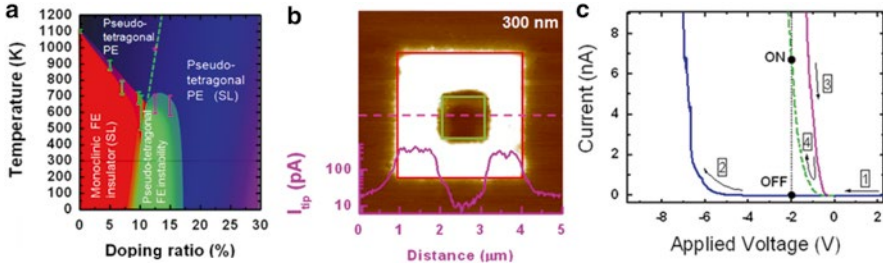
Although there are a number of studies on *B*-site alloyed  $\text{BiFeO}_3$ , greater attention has been given to *A*-site alloyed phases. The most widely studied dopants are materials from the Lanthanide series—especially La, Dy, Gd, etc. As early as 1991 work on these materials was undertaken [164], but again it was not until after 2003 that the number of studies on these alloyed systems really took off. Early studies probe the effect of La-alloying on the magnetic structure of  $\text{BiFeO}_3$  and showed that the spin-modulated structure disappeared in single crystals with only 20 % addition of La [165]. Soon after studies on La-alloyed thin films showed that the structure of the films was greatly affected and that the ferroelectric fatigue life was seemingly enhanced [159, 166]. Later studies showed that careful control of La-doping could be used to control domain structures, switching, and produce robust ferroelectric properties in films on Si substrates [167]. Other studies have also investigated Ba- [168], Sr-, Ca-, and Pb-doping [169], and many others. It should be noted that there are numerous studies of *A*-site alloying, too many to be covered thoroughly here.

Another exciting discovery occurred when researcher doped rare-earth elements into  $\text{BiFeO}_3$ . Upon doping  $\text{BiFeO}_3$  with Sm (at ~14 % Sm), a lead-free morphotropic phase boundary was discovered [170]. The researchers found a rhombohedral

**Fig. 3.16** Leakage current density as a function of applied electric field for pure and doped  $\text{BiFeO}_3$  thin films.  $\text{Ti}$ -doped  $\text{BiFeO}_3$  is shown to have significantly reduced leakage currents. *Inset* shows a zoom in of the low voltage region of the data (adapted from [160])



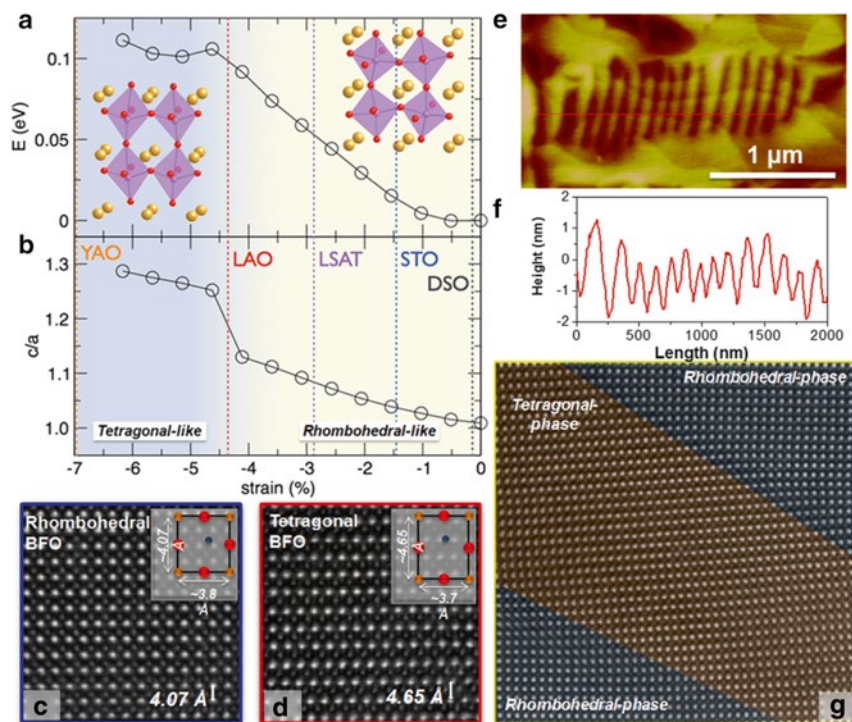
to pseudo-orthorhombic structural transition (and an associated ferroelectric to anti-ferroelectric transition) that produced an out-of-plane piezoelectric coefficient comparable to  $\text{PbZr}_x\text{Ti}_{1-x}\text{O}_3$  materials near the chemically derived morphotropic phase boundary in that material. Further investigations of this morphotropic phase boundary have investigated the effects of  $\text{Sm}$  doping and have shown that the  $\text{Sm}^{3+}$  first creates antiparallel cation displacements in local pockets and, with additional  $\text{Sm}$ , a series of phase transitions and superstructural phases are formed [171, 172]. This work has recently culminated in the observation of a universal behavior in such rare-earth substituted versions of  $\text{BiFeO}_3$  [173]. By combining careful experimental and first-principles approaches to the study of complex phase development in this system, researchers have discovered that the structural transition between a rhombohedral ferroelectric phase and an orthorhombic phase with a double-polarization hysteresis loop and significantly enhanced electromechanical response is found to occur independent of the rare-earth dopant species as long as the average ionic radius of the A-site cation is controlled. Despite the somewhat complicated phase space related to such doped versions of  $\text{BiFeO}_3$ , researchers have been able to identify and manipulate dopants to greatly enhance the properties of this material. The work in alloyed  $\text{BiFeO}_3$  materials was undertaken with the expectation that this would present an exciting pathway to unprecedented control and properties in this material. The findings, although useful and insight full, had failed to produce a ground breaking discovery until very recently. In 2009, Yang et al. [174], building off of the prior observation of the development of interesting materials phenomena such as high- $T_C$  superconductivity in the cuprates and colossal magnetoresistance in the manganites



**Fig. 3.17** (a) Pseudo-phase diagram of the evolution of structures and properties in Ca-doped  $\text{BiFeO}_3$ . (b) Conducting-atomic force microscopy image of an electrically poled and re-poled area of a doped  $\text{BiFeO}_3$  film. The as-grown state (*outside the outer box*) is insulating in nature, the electrically poled area (*inside the outer box and outside the inner box*) has become conducting, and the area that has been electrically poled twice (*inside inner box*) is insulating again. (c) Illustration of the process to create a multi-state memory from such physical properties (adapted from [174])

arise out of a doping-driven competition between energetically similar ground states, investigated doped multiferroics as a new example of this generic concept of phase competition. The results were the observation of an electronic conductor–insulator transition by control of band-filling in Ca-doped  $\text{BiFeO}_3$ . Application of electric field enables us to control and manipulate this electronic transition to the extent that a  $p$ – $n$  junction can be created, erased, and inverted in this material. A ‘dome-like’ feature in the doping dependence of the ferroelectric transition is observed around a Ca concentration of 1/8, where a new pseudo-tetragonal phase appears and the electric modulation of conduction is optimized (Fig. 3.17a). c-AFM images (Fig. 3.17b) reveal that upon application of an electric field the material becomes conducting and that subsequent application of electric fields can reversibly turn the effect on and off. It has been proposed that this observation could open the door to merging magnetoelectrics and magnetoelectronics at room temperature by combining electronic conduction with electric and magnetic degrees of freedom already present in the multiferroic  $\text{BiFeO}_3$ . Figure 3.17c shows the quasi-non-volatile and reversible modulation of electric conduction accompanied by the modulation of the ferroelectric state. The mechanism of this modulation in Ca-doped  $\text{BiFeO}_3$  is based on electronic conduction as a consequence of the naturally produced oxygen vacancies that act as donor impurities to compensate Ca acceptors and maintain a highly stable  $\text{Fe}^{3+}$  valence state.

As we have noted, epitaxy presents a powerful pathway to control the phase stability and electronic properties in thin-film systems [175]. The  $\text{BiFeO}_3$  system presents a fascinatingly complex strain-driven structural evolution. Although the structure of  $\text{BiFeO}_3$  had been studied for many years [103, 107, 176], in 2005 the structural stability of the parent phase had come into question [177, 178]. This was followed, in turn, by a number of thin-film studies reporting that a tetragonally distorted phase (derived from a structure with  $P4mm$  symmetry,  $a \sim 3.665 \text{ \AA}$ , and  $c \sim 4.655 \text{ \AA}$ ) with a large spontaneous polarization may be possible [177, 179, 180]. In 2009, the so-called mixed-phase thin films possessing tetragonal- and



**Fig. 3.18** Strain-induced phase complexity in BiFeO<sub>3</sub>. First-principle calculations provide information on the strain evolution of (a) the overall energy of the system and (b) the  $c/a$  lattice parameter ratio. High-resolution transmission electron microscopy (HRTEM) reveals the presence of two phase (c) a monoclinic version of the bulk rhombohedral phase and a (d) high-distorted monoclinic version of a tetragonal structure. These complex phase boundaries manifest themselves on the surface of the sample as imaged via (e) atomic force microscopy and these features correspond to dramatic surface height changes as shown from (f) the line trace. (g) HRTEM imaging of boundaries shows a smooth transition between phases. (Adapted from [181])

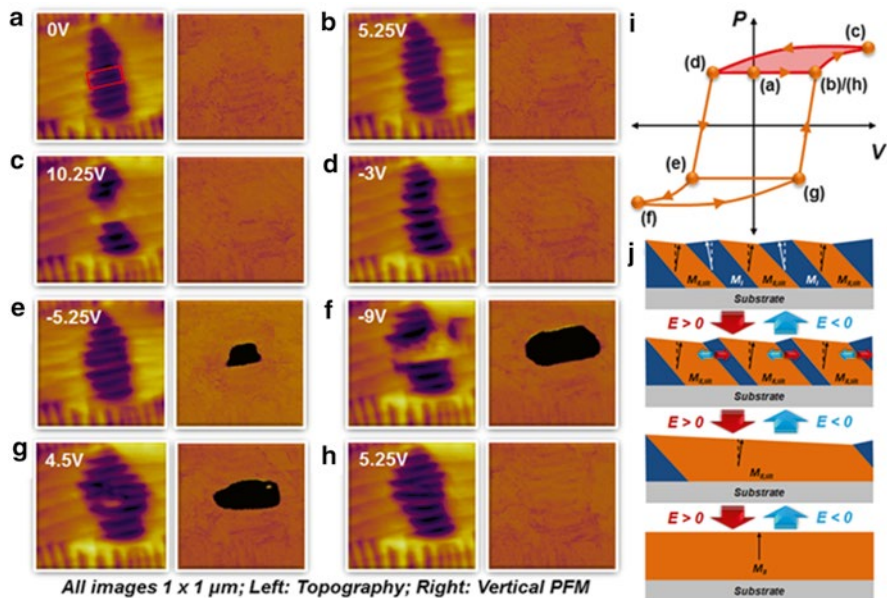
rhombohedral-like phases in complex stripe-like structures (and large electromechanical responses) [181] dramatically changed the study of structures in BiFeO<sub>3</sub>. It was found that the rhombohedral bulk crystal structure of the parent phase can be progressively distorted into a variety of unit cell structures through epitaxial strain. Ab initio calculations of the role of epitaxial strain clearly demonstrate how it can be used to drive a strain-induced structural change in BiFeO<sub>3</sub> (Fig. 3.18a, b). These calculations suggest that at a certain value of epitaxial strain, in the absence of misfit accommodation through dislocation formation, the structure of BiFeO<sub>3</sub> morphs from the distorted rhombohedral parent phase to a tetragonal-like (actually monoclinic) structure that is characterized by a large  $c/a$  ratio of  $\sim 1.26$ . Direct atomic resolution images of the two phases (Fig. 3.18c, d) clearly show the difference in the crystal structures.

Much recent attention has been given to what happens when films are grown at intermediate strain levels (e.g.,  $\sim 4.5\%$  compressive strain, corresponding to growth on  $\text{LaAlO}_3$  substrates). It has been observed that the result is a nanoscale mixed-phase structure (Fig. 3.18e, f). Figure 3.18g is an atomic resolution TEM image of the interface between these two phases and reveals one of the most provocative aspects of these structures. Although there is a large “formal” lattice mismatch between the two phases, the interface appears to be coherent, i.e., it shows no indication for the formation of interphase dislocations. Indeed, this mismatch appears to be accommodated by the gradual deformation of the structure between different phases.

Considerable detail has emerged concerning the symmetry of these phases including the fact that the so-called tetragonal-like phase is actually monoclinically distorted (possessing *Cc*, *Cm*, *Pm*, or *Pc* symmetry) [182–185]. Other techniques such as second harmonic generation have been used to probe these different structures as well [186]. Recent reports [187] have also investigated the driving force for the formation of these so-called mixed-phase structures and have revealed a complex temperature- and thickness-dependent evolution of phases in the  $\text{BiFeO}_3/\text{LaAlO}_3$  system. A thickness-dependent transformation from the monoclinically distorted tetragonal-like phase to a complex mixed-phase structure likely occurs as the consequence of a strain-induced spinodal instability. Additionally, a breakdown of this strain-stabilized metastable mixed-phase structure to non-epitaxial microcrystals of the parent rhombohedral structure of  $\text{BiFeO}_3$  is observed to occur at a critical thickness of  $\sim 300$  nm. Other reports have demonstrated routes to stabilize these structures [188]. At the same time, electric field-dependent studies to these mixed-phase structures have also revealed the capacity for large electromechanical responses (as large as  $4\text{--}5\%$ ). In situ TEM studies coupled with nanoscale electrical and mechanical probing suggest that these large strains result from the motion of boundaries between different phases [189]. Despite this work, a thorough understanding of the complex structure of these phase boundaries in  $\text{BiFeO}_3$  remained incomplete until 2011.

A perspective by Scott [190] discussed the symmetry and thermodynamics of the phase transition between these two phases as well as a number of other model isosymmetric phase transitions in other crystal systems. Soon after, a very detailed thermodynamic and elastic domain theory analysis of the mixed-phase structure was completed by Ouyang et al [191]. In that treatment, a balance of interdomain elastic, electrostatic, and interface energies was analyzed and compared to provide an anticipated low-energy structural configuration. Subsequent studies by Damodaran et al. [192] helped uniquely identify and examine the numerous phases present at these phase boundaries and resulted in the discovery of an intermediate monoclinic phase in addition to the previously observed rhombohedral- and tetragonal-like phases. Further analysis determined that the so-called mixed-phase regions of these films were not mixtures of the parent rhombohedral- and tetragonal-like phases, but were mixtures of highly distorted monoclinic phases with no evidence for the presence of the rhombohedral-like parent phase. This work helped confirm the mechanism for the enhanced electromechanical response and provide a





**Fig. 3.19** AFM image (*left*) and vertical PFM image (*right*) of 100 nm BiFeO<sub>3</sub>/La<sub>0.5</sub>Sr<sub>0.5</sub>CoO<sub>3</sub>/LaAlO<sub>3</sub> (001) in the (a) as-grown state and after being poled in the box at (b) 5.25 V, (c) 10.25 V, (d) -3 V, (e) -5.25 V, (f) -9 V, (g) 4.5 V, and (h) 5.25 V. (All images are 1 × 1 μm). (i) A schematic hysteresis loop with letters corresponding to the images in (a–h) shows the multiple pathways to enhanced electromechanical response. (j) Illustration of the proposed mechanism for the large electromechanical response without the need for ferroelectric switching. (Adapted from [192])

model for how these phases interact at the nanoscale to produce large surface strains (Fig. 3.19). By undertaken local electric field switching studies and navigating the hysteretic nature of electric field response in this material, a number of important features were revealed: (1) the large surface strains (4–5 %) occur any time the material transforms from a mixed-phase structure to the highly distorted monoclinic phase, (2) transformations between these two states are reversible, and (3) there are numerous pathways to achieve large electromechanical responses in these materials—including ones that do not need ferroelectric switching. The key appears to be the ability to transform between the different phases through a diffusion-less phase transition (akin to a martensitic phase). Similar discussions of the nature of the electric field driven phase transformation have also been reported [193]. This report additionally included single-point spectroscopic studies that suggest that the tetragonal-like to rhombohedral-like transition is activated at a lower voltage compared to a ferroelectric switching of the tetragonal-like phase and the formation of complex rosette domain structures that have implications for future devices.

A number of additional studies on these strain-induced phases have been reported in recent months. This includes considerable discussion on magnetic and magneto-electric properties of these materials. Researchers have investigated the emergence of

an enhanced spontaneous magnetization in the so-called mixed-phase structures [194]. Using X-ray magnetic circular dichroism-based photoemission electron microscopy coupled with macroscopic magnetic measurements, the researchers found that the spontaneous magnetization of the new intermediate monoclinic phase is significantly enhanced above the expected moment of the parent phase as a consequence of a piezomagnetic coupling to the adjacent tetragonal-like phase. Soon after this report, researchers suggested that the magnetic Néel temperature of the strained  $\text{BiFeO}_3$  is suppressed to around room temperature and that the ferroelectric state undergoes a first-order transition to another ferroelectric state simultaneously with the magnetic transition [195]. This has strong implications for room temperature magnetoelectric applications. This observation builds off of a detailed neutron scattering study of a nearly phase-pure film of the highly distorted tetragonal-like phase which confirms antiferromagnetism with largely G-type character and a  $T_N=324$  K, a minority magnetic phase with C-type character, and suggests that the coexistence of the two magnetic phases and the difference in ordering temperatures from the bulk phase can be explained through simple Fe–O–Fe bond distance considerations [196]. At the same time, other reports suggest the possibility of a reversible temperature-induced phase transition at about 373 K in the highly distorted tetragonal-like phase as studied by temperature-dependent Raman measurements [197]. Similar results have been reported from temperature-dependent X-ray diffraction studies that reveal a structural phase transition at  $\sim 373$  K between two monoclinic structures [198]. Finally there are reports of a concomitant structural and ferroelectric transformation around 360 K based on temperature-dependent Raman studies. This work suggests that the low-energy phonon modes related to the  $\text{FeO}_6$  octahedron tilting show anomalous behavior upon cooling through this temperature—including an increase of intensity by one order of magnitude and the appearance of a dozen new modes [199]. Truly this is an exciting and fast-moving field of study today. Such electric field and temperature-induced changes of the phase admixture is also reminiscent of the CMR manganites or the relaxor ferroelectrics and is accompanied by large electromechanical strains, but there appears to be much more to these mixed-phase structures. Such structural softness in regular magnetoelectric multiferroics—i.e., tuning the materials to make their structure strongly reactive to applied fields—makes it possible to obtain very large magnetoelectric effects [200].

All of these observations of exotic phenomena have implications for memories and future devices. For instance, the recent observation of large piezoelectric responses in mixed-phase, strained  $\text{BiFeO}_3$  thin films could provide a possible pathway to enable probe based data storage elements [201]. Such materials require considerable development before they can be utilized in devices and a number of key questions must be answered in this regard. Among the most important for this application is what is the smallest length scale of coexistence of these two phases? This question is motivated by the desire to create the mixed phases responsible for the large electromechanical effects on the same length scales as relaxor ferroelectrics (i.e., just a few nm). Likewise, the possibility of converting an insulating, ferroelectric state in doped  $\text{BiFeO}_3$  (such as in the example shown above of Ca-doped  $\text{BiFeO}_3$ ) into a relatively conducting state could be used for information storage

purposes. However, the exact physical mechanisms behind such changes in conductivity are still unclear. An ideal scenario would be one in which the insulating, ferroelectric state is converted into a conducting state via a true phase transition that is triggered by an electric field. Such a sophisticated mechanism is still not available.

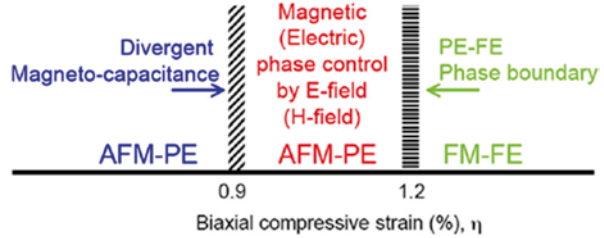
### 3.4.4 Other Single-Phase Multiferroics

Finally, we note that a number of other candidate multiferroic materials with lone-pair active *A*-sites and magnetic transition metal *B*-sites have been produced in the last few years. As early as 2002, Hill et al. [202] had predicted BiCrO<sub>3</sub> to be antiferromagnetic and antiferroelectric, but not until 2006 were thin films of this material produced. Thin films of BiCrO<sub>3</sub> were grown on LaAlO<sub>3</sub> (001), SrTiO<sub>3</sub> (001), and NdGaO<sub>3</sub> (110) substrates and were shown to be antiferromagnetic, displaying weak ferromagnetism, with an ordering temperature of ~120–140 K. Early reports suggested that these films showed piezoelectric response and a tunable dielectric constant at room temperature [203] while others suggested that the films were antiferroelectric as predicted in theory [204]. Other phases of interest include BiCoO<sub>3</sub>. Bulk work on BiCoO<sub>3</sub> [205] and theoretical predictions of giant electronic polarization of more than 150 μC/cm<sup>2</sup> [206] have driven researchers to attempt creating this phase as a thin film as well. To date only solid solutions of BiFeO<sub>3</sub>–BiCoO<sub>3</sub> have been grown via MOCVD [207]. Another phase similar to BiCoO<sub>3</sub> that has been produced as a thin film is PbVO<sub>3</sub> [22], PbVO<sub>3</sub> films were grown on LaAlO<sub>3</sub>, SrTiO<sub>3</sub>, (La<sub>0.18</sub>Sr<sub>0.82</sub>)(Al<sub>0.59</sub>Ta<sub>0.41</sub>)O<sub>3</sub>, NdGaO<sub>3</sub>, and LaAlO<sub>3</sub>/Si substrates and were found to be a highly tetragonal perovskite phase with a *c/a* lattice parameter ratio of 1.32. Further analysis of this material using second harmonic generation and X-ray dichroism measurements revealed that PbVO<sub>3</sub> is both a polar, piezoelectric and likely an antiferromagnet below ~130 K [23]. There has also been attention given to double-perovskite structures such as Bi<sub>2</sub>NiMnO<sub>6</sub> which have been shown to be both ferromagnetic (*T*<sub>C</sub>~100 K) and ferroelectric with spontaneous polarization of ~5 μC/cm<sup>2</sup> [208].

It is also important to note the power of first-principles investigations and the strong predictive power of modern computational approaches and the role they have played in the discovery and study of multiferroics (for complete review of first-principles approaches to multiferroics see [209–211]). For instance, in 2006 Fennie and Rabe predicted a design strategy by which one could induce multiferroicity in materials such as EuTiO<sub>3</sub> (Fig. 3.20) [212]. By applying tensile strain to the material, normally a paraelectric antiferromagnet, it was suggested that a ferromagnetic and ferroelectric phase could be produced. Recent results suggest that indeed this should be possible. Soon after similar predictions suggested multiferroic behavior might be possible in phases such as FeTiO<sub>3</sub> [213]. This prediction has also been confirmed experimentally [214]. At high pressures (or strains) FeTiO<sub>3</sub> takes on a LiNbO<sub>3</sub>-like structure, a combination of piezoresponse force microscopy, optical second harmonic generation, and magnetometry has since revealed that this phase is



**Fig. 3.20** Schematic phase diagram describing the strain-driven changes in  $\text{EuTiO}_3$ —candidate material for strain-driven multiferroism (adapted from [212])



both ferroelectric and displays a weak ferromagnetic response. More recently, new calculations have suggested the material  $\text{SrMnO}_3$  could also exhibit strain-driven multiferroicity [215]. Although these are but a few of the many examples of the close interaction between computation and experimental work, they are illustrative of the power of modern approaches to modeling and predicting materials properties. It is clear that such approaches will continue to play an essential role in the future development of this field.

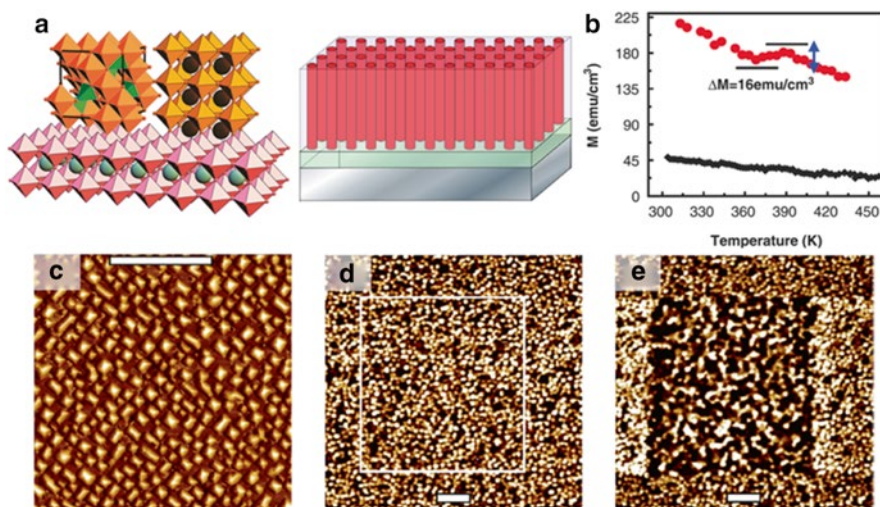
### 3.4.5 Horizontal Multilayer Structures

Beyond single-phase multiferroics, great strides have been made in the area of composite magnetoelectric systems. These systems operate by coupling the magnetic and electric properties between two materials, generally a ferroelectric material and a ferrimagnetic material, via strain. An applied electric field creates a piezoelectric strain in the ferroelectric, which produces a corresponding strain in the ferrimagnetic material and a subsequent piezomagnetic change in magnetization or the magnetic anisotropy. Work started in the field several decades ago using bulk composites, although experimental magnetoelectric voltage coefficients were far below those calculated theoretically [216]. In the 1990s theoretical calculations showed possible strong magnetoelectric coupling in a multilayer (2-2) configuration; an ideal structure to be examined by the burgeoning field of complex oxide thin-film growth [217]. In this spirit, researchers experimentally tested a number of materials in a laminate thick-film geometry, including ferroelectrics such as  $\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$  [218–223],  $\text{Pb}(\text{Mg}_{0.33}\text{Nb}_{0.67})\text{O}_3$ - $\text{PbTiO}_3$  (PMN-PT) [224], and ferromagnets such as  $\text{TbDyFe}_2$  (Terfenol-D) [218],  $\text{NiFe}_2\text{O}_4$  [219, 221],  $\text{CoFe}_2\text{O}_4$  [223],  $\text{Ni}_{0.8}\text{Zn}_{0.2}\text{Fe}_2\text{O}_4$  [220],  $\text{La}_{0.7}\text{Sr}_{0.3}\text{MnO}_3$  [222],  $\text{La}_{0.7}\text{Ca}_{0.3}\text{MnO}_3$  [222], and others. These experiments showed great promise and magnetoelectric voltage coefficients up to  $\Delta E/\Delta H = 4,680$  mV/cm Oe have been observed. Work also continued investigating thin-film heterostructures by combining such ferroelectrics as  $\text{Ba}_{0.6}\text{Sr}_{0.4}\text{TiO}_3$ ,  $\text{BaTiO}_3$  [225], and PMN-PT [226] with ferromagnets such as  $\text{Pr}_{0.85}\text{Ca}_{0.15}\text{MnO}_3$  [225] and  $\text{Tb-Fe/Fe-Co}$  multilayers [226]; however, these attempts were unable to produce magnetoelectric voltage coefficients above a few tens of mV/cm Oe. Current theories suggest that the in-plane magnetoelectric interface is limiting the magnitude of this coefficient due to the clamping effect of the substrate on the ferroelectric phase [227]. Since the

amount of strain that can be imparted by the ferroelectric phase is limited via this in-plane interfacial geometry, the magnetoelectric voltage coefficient can be reduced by up to a factor of five. A set of excellent reviews of this film can be found in [228–231].

### 3.4.6 Vertical Nanostructures

A seminal paper by Zheng et al. [232] showed that magnetoelectric materials could also be fabricated in a nanostructured columnar fashion (Fig. 3.21a). By selecting materials that spontaneously separate due to immiscibility, such as spinel and perovskite phases [216], one can create nanostructured phases made of pillars of one material embedded in a matrix of another. In this initial paper, researchers reported structures consisting of  $\text{CoFe}_2\text{O}_4$  pillars embedded in a  $\text{BaTiO}_3$  matrix. The large difference in lattice parameter between these phases leads to the formation of pillars with dimensions on the order of tens of nanometers, which ensures a high interface-to-volume ratio, an important parameter when attempting to couple the two materials via strain. Such structures were shown to exhibit strong magnetoelectric coupling (Fig. 3.21b) via changes in magnetization occurring at the



**Fig. 3.21** Multiferroic Nanostructures. (a) Schematic illustrations of vertical nanostructure of spinel pillars embedded in a perovskite matrix grown on a perovskite substrate. (b) Magnetization versus temperature curve measured at 100 Oe showing a distinct drop in magnetization at the ferroelectric Curie temperature—proof of strong magnetoelectric coupling. (c) Surface topography of a  $\text{CoFe}_2\text{O}_4/\text{BiFeO}_3$  nanostructure as imaged by atomic force microscopy. Magnetic force microscopy scans taken in the same area before (d) and after electrical poling at  $-16 \text{ V}$  (e) (Scale bars are  $1 \mu\text{m}$ ). (Adapted from [232, 233])

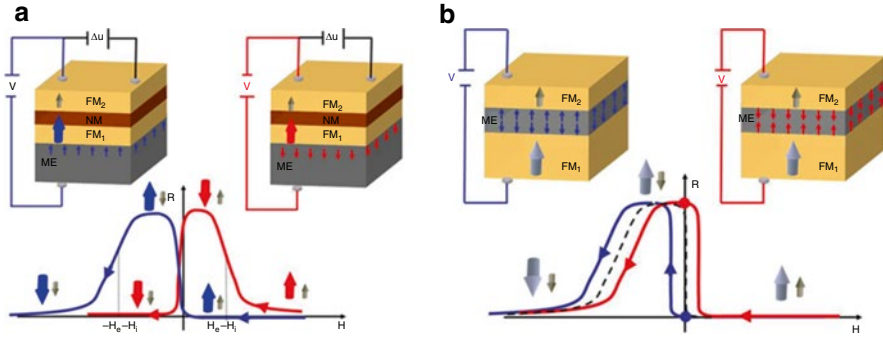
ferroelectric Curie temperature of the matrix material. These nanostructures, in which the interface is perpendicular to the substrate, remove the effect of substrate clamping and allow for better strain-induced coupling between the two phases. An explosion of research into alternate material systems followed as the design algorithm proved to be widely applicable to many perovskite-spinel systems. Nanostructured composites with combinations of a number of perovskite ( $\text{BaTiO}_3$  [234],  $\text{PbTiO}_3$  [235],  $\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$  [236, 237], and  $\text{BiFeO}_3$  [238, 239]) and spinel ( $\text{CoFe}_2\text{O}_4$  [236, 237],  $\text{NiFe}_2\text{O}_4$  [235, 238], and  $\gamma\text{-Fe}_2\text{O}_3$  [239]) or corundum ( $\alpha\text{-Fe}_2\text{O}_3$  [239]) structures have been investigated. The magnetic properties of such systems are generally well-behaved, but the ferroelectric properties are highly dependent on the synthesis technique. When satisfactory ferroelectric properties can be produced, more substantial magnetoelectric voltage coefficients are generally achieved. Pulsed laser deposition has proven to be a successful growth technique for achieving satisfactory properties in these nanostructured films [234, 240, 241].

Zavaliche et al. [242] showed  $\Delta E/\Delta H = 100$  V/cm Oe at room temperature in a system comprised of  $\text{CoFe}_2\text{O}_4$  pillars embedded in a  $\text{BiFeO}_3$  matrix. These films were analyzed with scanning probe techniques that utilized both magnetized and conducting tips. Typical surface morphology for such samples is shown in Fig. 3.21c. Magnetic measurements show the preference of such structures to maintain magnetization along the length of the nanopillars. Magnetic force microscopy scans both before (Fig. 3.21d) and after electric field poling (Fig. 3.21e) show a significant number of  $\text{CoFe}_2\text{O}_4$  pillars switch their magnetic state from a downward direction to an upward direction upon application of an electric field [233]. This work further showed that the magnetization-switching event was non-deterministic and could be improved by applying a small magnetic field (700 Oe) to the sample. This field is essential to break time reversal symmetry and overcome the degeneracy between the up and down magnetization states. Nonetheless, these structures have been shown to be very versatile and offer an excellent opportunity for electrically controlled magnetic storage.

We also note that other interesting nanoscale composite geometries have been investigated. Using anodized aluminum oxide templates, Liu et al. [243] successfully synthesized nanowires of  $\text{NiFe}_2\text{O}_4$  surrounded by a shell of PZT. However, successful magnetoelectric coupling has been not yet shown in such a system. Overall, it has been shown that nanostructured composite multiferroics have shown significantly enhanced magnetoelectric properties over traditional multilayer heterostructures and are excellent candidates for a wide range of devices that would take advantage of the strong magnetoelectric coupling that can be achieved in these structures.

### 3.5 Design of Multiferroic-Based Memories

One of the major questions in the study of multiferroics today is how and when will multiferroics make their way into a room temperature device and what will these devices look like? Device manifestation of multiferroics and magnetoelectrics can be broadly classified into a number of areas, including (1) information storage elements



**Fig. 3.22** Multiferoic-based Magnetoelectronics. **(a)** Schematic of the magnetoresistance curve of a GMR device involving a magnetoelectric, multiferroic film as a pinning layer. Half-hysteresis curves are shown, after saturation at positive field values. The change of polarity of the magneto-electric, multiferroic layer upon application of an electric field changes the direction of the net magnetization of the pinning field. The pinned layer (FM1) switches first at large positive field, or second at large negative field. The low field magnetic configuration is therefore either antiparallel or parallel, controlled by the magnetoelectric, multiferroic. **(b)** Schematic of the magnetoresistance curve of a TMR device involving a magnetoelectric, multiferroic film as a tunnel barrier. Half-hysteresis curves are shown, after saturation at positive field values. The arrows denote the magnetization directions, with the bottom layer FM1 being harder (or pinned) than the top one FM2. The *dashed curve* is the expected TMR behavior. The change of voltage polarity changes the direction of the net magnetization of the magnetoelectric, multiferroic layer, adding an exchange bias magnetic field to the resistance curve. The *two curves* indicate shifting of half-hysteresis curves towards positive or negative fields, depending on the polarity of the applied voltage. At zero magnetic field, the change of voltage polarity changes the resistance value of the device (*dashed*). (Adapted from [244])

(i.e., memories), (2) information processing elements (i.e., logic elements), (3) sensors, (4) high-frequency RF elements, and more. In this chapter, we will focus predominantly on memories, but will touch on others as needed.

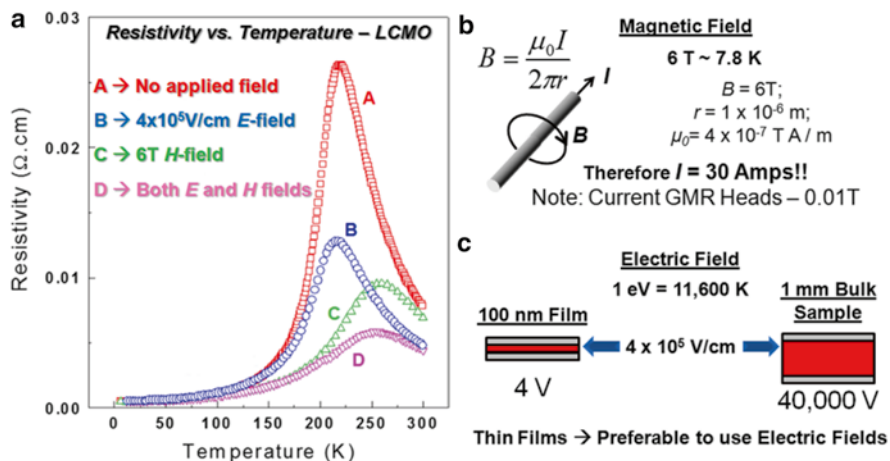
The focus of this book is on emerging non-volatile memories. Multiferroics and magnetolectrics are but in the infancy of their investigation and thus there are limited reports of full-scale devices based on these materials. However, as early as 2005, a number of what were referred to as *magnetolectronics* based on magneto-electric materials were proposed [244]. The idea was a simple one, to use the net magnetic moment created by an electric field in a magnetolectric thin film to change the magnetization of a neighboring ferromagnetic layer through exchange coupling. The authors went on to propose a number of electrically tunable giant magnetoresistance (GMR) spin valves (Fig. 3.22a) and tunnel magnetoresistance (TMR) (Fig. 3.22b) elements that could be made possible if such structures could be achieved. One additional field that could be greatly affected by this research is the burgeoning field of spintronics. Spin-based electronics, or spintronics, have already found successful application in magnetic read-heads and sensors that take advantage of GMR and TMR effects. The future of spintronics is partially focused on evolving beyond passive magnetolectronic components, like those used today, to devices which combine memory and logic functions in one [245]. There has been

growing interest in studying a direct method for magnetization reversal involving spin-transfer from a spin-polarized current injected into the device. This effect has been theoretically predicted by Slonczewski [246, 247] and Berger [248], and has been experimentally confirmed by several groups [249–252]. And it is at this point that the first major stumbling block is met.

From these initial experiments and theoretical treatments, it was found that significant current densities (larger than  $10^7$  A/cm<sup>2</sup>) were required for switching the orientation of even a magnetic nanowire [250]. One option is to further scale down materials so that spin-transfer becomes a more attractive alternative to stray magnetic field techniques. In the end, integration of such effects into actual devices has been limited because there are a number of technical difficulties involved in reliably making such small structures, applying such large currents—while avoiding heating of the samples, and based on the fact that the intrinsic sample resistance (on the order of a few ohms) further limits the practical use for GMR devices. Similar issues are found in TMR devices, which are hindered by the fact that a large current density must pass through a very thin insulator and the few reports on TMR systems to date have been inconclusive [253, 254].

At the heart of what Binek and Doudin [244] were asking in 2005 was whether we should attempt to use currents or some alternative method (i.e., electric field) to create actual devices with new functionalities. Materials discoveries aside, a critical materials physics question emerges from this question that lies at the heart of the last 20 years of research on correlated oxides as well. This has to do with the role of energy scales (as well as time and length scales) of relevance to the ultimate implementation of these materials into actual devices. Let us explore this issue in a bit more detail using the data presented in Fig. 3.23 for the colossal magnetoresistant (CMR) manganites (data shown here is for  $\text{La}_{0.7}\text{Ca}_{0.3}\text{MnO}_3$  (LCMO)) as a frame of reference. Over the past 20 years, there has been extensive research conducted on these materials. By far the most interesting aspect of these very intriguing materials is the large (colossal) change in resistance that occurs with the application of a magnetic field of several Tesla ( $6T$  in the present example) (shown in the green data in Fig. 3.23a). It has also been demonstrated that a commensurate “colossal electroresistance” can be obtained with electric fields of the order of a few hundred kV (shown in blue in Fig. 3.23a) [255]. Let us now compare these two energy scales and ask the question: how do these two types of fields compare from the perspective of external power requirements?

We can understand this through a simple thought experiment. If one needed to generate the necessary magnetic field of  $6T$  at a distance of  $1\ \mu\text{m}$  from a metal wire (Fig. 3.23b), a current of  $\sim 30$  A would be required! We note that a  $6T$  magnetic field translates to a temperature scale in the material of  $\sim 8$  K [256], which is significantly smaller than the critical temperatures (for example, the magnetic transition temperature or the peak in the resistivity). Regardless, this current is prohibitive both from the point of view of the integrity of the metal wire that would carry the current as well as the power requirements—especially as device sizes are decreased. Let us now examine an alternative pathway to achieve the same effect through the use of an electric field (Fig. 3.23c). If one desires to create the appropriate electric field needed to observe colossal electroresistance in a  $100\ \text{nm}$  thick film, a potential of



**Fig. 3.23** Motivation for electric field control of properties. (a) Resistivity versus temperature for  $\text{La}_{0.7}\text{Ca}_{0.3}\text{MnO}_3$  thin films with no applied field (red), applied electric field (blue), applied magnetic field (green), and both applied electric and magnetic fields (pink). Energy scales in materials dictate the eventual incorporation of such materials into device structures. (b) The production of the large magnetic fields ( $\sim 6\text{T}$ ) required for colossal magnetoresistance in CMR materials requires large currents ( $\sim 30 \text{ A}$ ) while (c) production of the appropriate electric fields to produce colossal electroresistance ( $\sim 4 \text{ V}$  for a 100 nm thick thin film) are much more reasonable and possible in standard semiconductor electronics circuitry. (Adapted from [255])

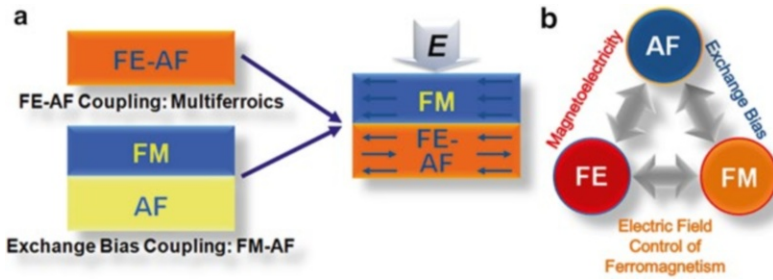
only 4 V is required. This is easily generated by standard semiconductor electronics circuitry. However, if the thickness of the material is, say 1 mm, then a potential of 40,000 V is required to generate the same field.

These two scenarios present a number of important considerations. First, if the energy scales for manipulation of these materials (be they CMR or multiferroics) do not become significantly smaller, then the use of magnetic fields to probe and manipulate them becomes technologically prohibitive. Indeed, this can be identified as the most important reason why CMR based systems have not become commercially viable. Second, if these energy scales are indeed maintained, it is clear that using thin film heterostructures and manipulating them with electric fields is a more attractive way to proceed in terms of technological manifestations of these phenomena. These ideas form the technological foundation for the next section of our treatment.

### 3.5.1 Electric Field Control of Ferromagnetism

The overall motivating question for this section is a simple one: can we deterministically control ferromagnetism at room temperature with an electric field? One possible solution to this question is to utilize heterostructures of existing multiferroic materials, such as  $\text{BiFeO}_3$ , to create new pathways to functionalities not

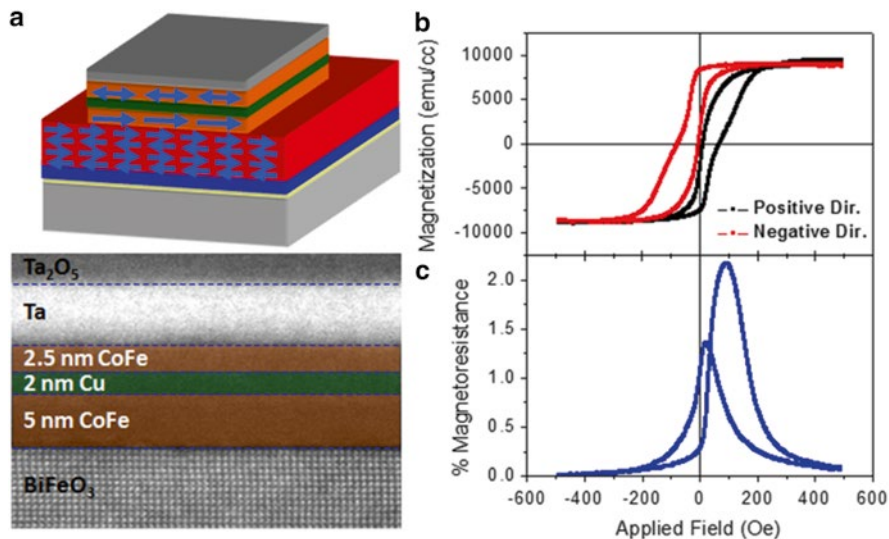




**Fig. 3.24** Schematics illustrating the design algorithm for gaining electrical control of ferromagnetism. (a) By combining multiferroics together with traditional ferromagnets, we can create heterostructures that might have new functionalities. (b) These structures rely on two types of coupling—magnetoelectric and exchange bias—to gain electrical control of ferromagnetism. (Adapted from [7])

presented in nature. Such a concept is illustrated in Fig. 3.24. The idea is to take advantage of two different types of coupling in materials—*intrinsic* magnetolectric coupling like that in multiferroic materials such as  $\text{BiFeO}_3$  which will allow for electrical control of antiferromagnetism and the *extrinsic* exchange coupling between ferromagnetic and antiferromagnetic materials—to create new functionalities in materials (Fig. 3.24a). By utilizing these different types of coupling we can then effectively couple ferroelectric and ferromagnetic order at room temperature and create an alternative pathway to electrical control of ferromagnetism (Fig. 3.24b). But what exactly are the opportunities for using multiferroics to gain electrical control over interactions like exchange bias anisotropy? Until recently the materials and the understanding of the appropriate materials did not exist to make this a plausible undertaking. Let us investigate, in detail, the work done in this field of study.

In the time since the proposal of these magnetoelectronics, studies have been done on a number of multiferroic materials. Among the earliest work was a study of heterostructures of the soft ferromagnet permalloy on  $\text{YMnO}_3$  [257]. This report found that, indeed, the multiferroic layer could be used as an antiferromagnetic pinning layer that gives rise to exchange bias and enhanced coercivity, but suggested that  $\text{YMnO}_3$  would likely be an inappropriate choice for continued study as these values varied greatly with crystal orientation and rendered actual device generation unlikely. Soon after this initial result, Marti et al. [258] reported the observation of exchange bias in all-oxide heterostructure of the ferromagnet SRO and the antiferromagnetic, multiferroic  $\text{YMnO}_3$ . In both of these studies, the exchange bias existed only at very low temperatures due to the low magnetic ordering temperature of the  $\text{YMnO}_3$ . Around the same time, the first studies using  $\text{BiFeO}_3$  as the multiferroic, antiferromagnetic layer were appearing with hopes that these intriguing properties could be extended to high temperatures. As part of this J. Dho et al. [259] showed the existence of exchange bias in spin-valve structures based on permalloy and  $\text{BiFeO}_3$  at room temperature and Béa et al. [260] extended this idea to demonstrate how  $\text{BiFeO}_3$  films could be used in first generation spintronics devices. This work

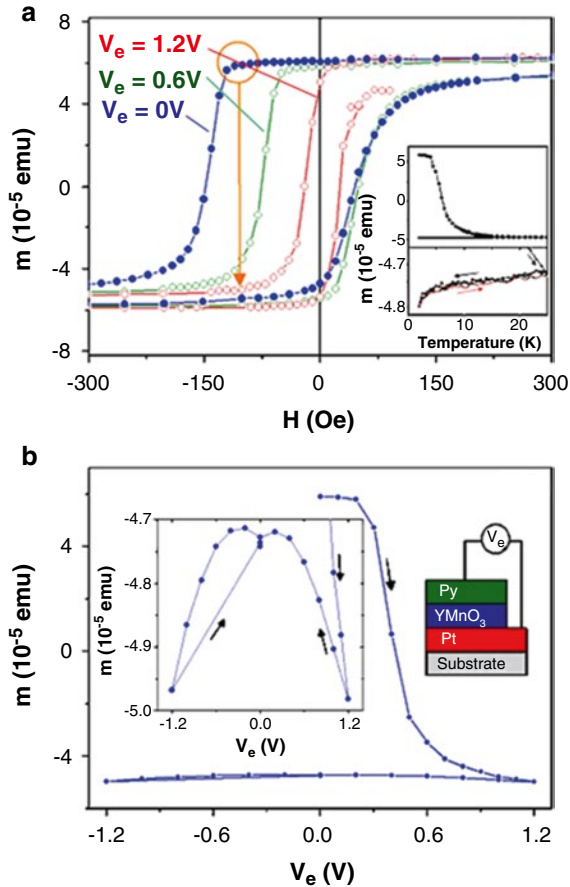


**Fig. 3.25** Spin valve structures based on  $\text{Co}_{0.9}\text{Fe}_{0.1}/\text{Cu}/\text{Co}_{0.9}\text{Fe}_{0.1}/\text{BiFeO}_3$  heterostructures. (a) Schematic illustration and scanning transmission electron microscopy image of the actual device. (b) Magnetic hysteresis loops of spin valve structures. (c) Current-in-plane magnetoresistance measurements. (Adapted from [261])

included the use of ultrathin  $\text{BiFeO}_3$  tunnel barriers in magnetic tunnel junctions with LSMO and Co electrodes where positive TMR up to  $\sim 30\%$  was observed at 3 K and also demonstrated that room temperature exchange bias could be generated using  $\text{CoFeB}/\text{BiFeO}_3$  heterostructures. Finally, Martin et al. [261] reported the growth and characterization of exchange bias and spin-valve heterostructures based on  $\text{Co}_{0.9}\text{Fe}_{0.1}/\text{BiFeO}_3$  heterostructures on Si substrates. In this work large negative exchange bias values (typically 150–200 Oe in magnitude) were observed along with the absence of a training effect—or a systematic decrease in the magnitude of the exchange bias with repeated magnetic cycling (confirming the results of Bea et al. [260])—even with over 14,000 magnetic cycles. This work also demonstrated room temperature magnetoresistance of  $\sim 2.25\%$  for spin-valve structures of 2.5 nm  $\text{Co}_{0.9}\text{Fe}_{0.1}/2$  nm Cu/5 nm  $\text{Co}_{0.9}\text{Fe}_{0.1}/100$  nm  $\text{BiFeO}_3$  (Fig. 3.25). What these initial studies established was that exchange bias with antiferromagnetic multiferroics was possible in a static manner, but these studies had not yet demonstrated dynamic control of exchange coupling in these systems.

A first attempt at this concept was done by Borisov et al. [262] who reported that they could affect changes on the exchange bias field in  $\text{Cr}_2\text{O}_3(111)/(\text{Co}/\text{Pt})_3$  heterostructures by using the magnetoelectric nature of the substrate ( $\text{Cr}_2\text{O}_3$ ) and a series of different cooling treatments with applied electric and magnetic fields. A unique aspect of this work was the ability to change the sign of the exchange bias with different field cooling treatments. Dynamic switching of the exchange bias field with an applied electric field, however, remained elusive until a report by Laukhin et al.



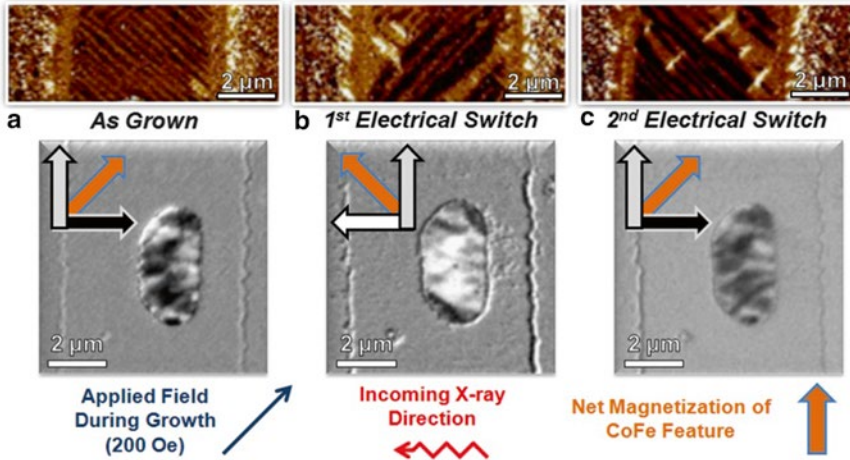


**Fig. 3.26** Low temperature electric field control of ferromagnetism. (a) Magnetization loops for permalloy/YMnO<sub>3</sub>/Pt, measured at 2 K, after cooling the sample from 300 K in a 3 kOe field, under various biasing-voltage ( $V_e$ ) values. The circle and arrow illustrate schematically the expected change of magnetization when biasing the sample by an electric field. The *inset* shows the temperature dependence of the magnetization at  $H = 100$  Oe and  $V_e = 0$  when heating the sample from 2 K to 25 K (*top panel*) and subsequent cooling-heating-cooling cycles between 25 K and 2 K (*bottom panel*). (b) Dependence of the magnetization on  $V_e$  measured at 2 K in  $H = 100$  Oe field after cooling the sample from 300 K in 3 kOe field. The *inset* shows (*left*) a zoom of the  $-1.2$  to  $1.2$  V portions of the bias excursion and (*right*) a sketch of the sample structure and electric biasing. (Adapted from [263])

[263] focusing on YMnO<sub>3</sub> at 2 K. Utilizing heterostructures of permalloy and (0001) YMnO<sub>3</sub> films, the authors demonstrated that after cooling samples from 300 to 2 K in an applied field of 3 kOe and at various applied electric field biases, significant changes in the magnitude of magnetization were observed (Fig. 3.26a). Subsequent cycling of the voltage at low temperatures resulted in reversal of the magnetization direction in the heterostructure (Fig. 3.26b).

In the last few years, significant advances in the understanding of the interactions present in such heterostructures have been presented. Initial reports noted an inverse relationship between domain size in BiFeO<sub>3</sub> film and the exchange bias measured in CoFeB/BiFeO<sub>3</sub> heterostructures [264]. This initial report offered little detail on how the domain structures were controlled and the nature of the domain walls present in the films. A study that soon followed found a correlation not only to the density of domain walls but also to the density of certain types of domain walls [140]. What was observed was the presence of two distinctly different types of magnetic properties for Co<sub>0.9</sub>Fe<sub>0.1</sub>/BiFeO<sub>3</sub> heterostructures. Through careful control of the growth process—specifically controlling the growth rate of the BiFeO<sub>3</sub> films—the authors were able to create two starkly different types of domain structures: so-called stripe- and mosaic-like domain structures. These different structures were found to possess vastly different fractions of the different domain walls that can exist in BiFeO<sub>3</sub>. It was observed that not only was there an inverse relationship between domain size and the magnitude of the exchange bias measured, but that it was directly related to the density and total length of 109° domain walls present in the sample. In addition to identifying the importance of 109° domain walls in creating exchange bias (and in turn suggesting the relationship with enhanced magnetism in BiFeO<sub>3</sub> thin films), this report outlined the idea that two distinctly different types of exchange interactions are occurring in these exchange bias heterostructures. The first interaction was called an *exchange bias* interaction and takes place between pinned, uncompensated spin occurring at 109° domain walls in BiFeO<sub>3</sub> and spins in the Co<sub>0.9</sub>Fe<sub>0.1</sub> layer. This interaction results in a shift of the magnetic hysteresis loop for the ferromagnetic layer. The second interaction has been called an *exchange enhancement* interaction and it arises from an interaction of the spins in the ferromagnet and the fully compensated (001) surface of the G-type antiferromagnetic surface of BiFeO<sub>3</sub>. This interaction results in an enhancement of the coercive field of the ferromagnetic layer.

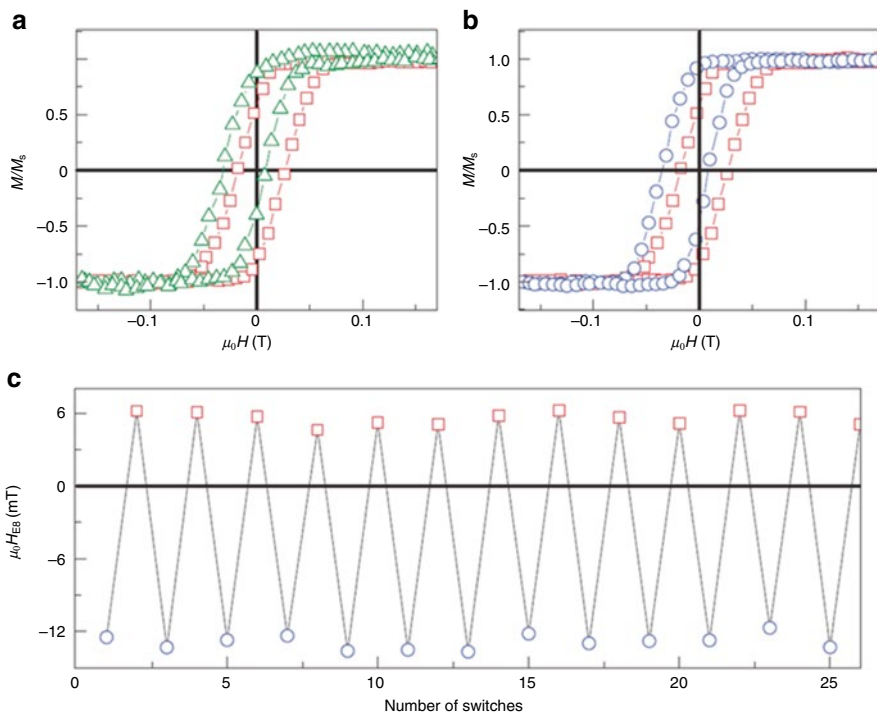
Utilizing these findings, researchers have moved to create the first room temperature devices designed to enable control of ferromagnetism with an electric field. Initial results point to the ability to utilize the above *exchange enhancement* interaction to deterministically change the direction of ferromagnetic domains by 90° upon application of an applied electric field (Fig. 3.27) [265]. By creating very high quality Co<sub>0.9</sub>Fe<sub>0.1</sub>/BiFeO<sub>3</sub>/SrRuO<sub>3</sub>/SrTiO<sub>3</sub> (001) heterostructures, the authors were able to demonstrate the first example of a room temperature device structure that utilizes a multiferroic material to access new functionalities in materials. This work also outlined the complexity of such an undertaking. It has become apparent that in order to achieve significant advances with such systems one will need to understand and be able to control (at least at some level) the coupling between the two (in this case dissimilar) materials. This requires that one will have a perfunctory understanding of the various energies-scales at play (including shape anisotropy effects, how processing effects the interfacial coupling strength, magnetostriction effects, and more). This initial work also demonstrated the importance of length scales in this work as the observed ferromagnetic domain structures were typically much more



**Fig. 3.27** Electric field control of ferromagnetic domain structures at room temperature. In-plane piezoresponse force microscopy images of ferroelectric domain structure (*top*) and corresponding photoemission electron microscopy image of ferromagnetic domain structure (*bottom*) of  $\text{Co}_{0.9}\text{Fe}_{0.1}$  features on  $\text{BiFeO}_3$  as a function of applied electric field in the (a) as-grown state, (b) after application of an electric field, and (c) following application of the opposite electric field. This represents the first demonstration of reversible electric field control of ferromagnetic domain structures at room temperature. (Adapted from [265])

complex than the underlying ferroelectric domain structures suggesting that diminished feature sizes could give rise to single magnetic domain configurations and therefore a more robust and simple device. In this spirit, current work is focused on making the coupling in such heterostructures more robust in hopes of extending this coupling to high temperatures and producing more deterministic control of electric field switching.

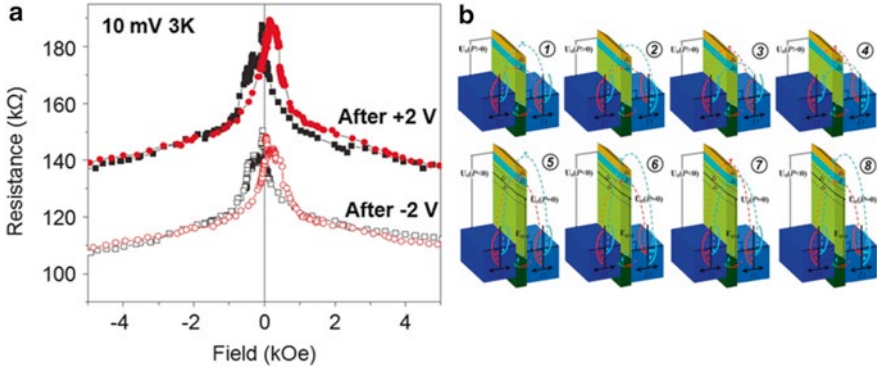
More recently, He et al. [266] have reported the exciting possibility of obtaining deterministic,  $180^\circ$  switching control of ferromagnetic structures using one of the oldest known multiferroics— $\text{Cr}_2\text{O}_3$ . The elegance of this finding lies in the discovery of new phenomena on the (0001) surface of  $\text{Cr}_2\text{O}_3$ . Specifically, through the use of a combination of magnetometry, spin-polarized photoemission spectroscopy, symmetry arguments, and first-principles calculations researchers have demonstrated that there is an electrically switchable magnetization at this surface in  $\text{Cr}_2\text{O}_3$ . By coupling the  $\text{Cr}_2\text{O}_3$  to an out-of-plane magnetized ferromagnetic Pd/Co multilayer, they have demonstrated isothermal switching of exchange bias between positive and negative values (Fig. 3.28). By applying combination electric- and magnetic-fields the researchers were able to demonstrate the ability to change the direction of exchange bias without changing the direction of the applied magnetic field. This represents a strong step forward in the understanding of multiferroic materials and further proof of the power of these materials for next generation applications.



**Fig. 3.28** (a) Exchange-biased hysteresis loops of  $\text{Cr}_2\text{O}_3$  (0001)/Pd 0.5 nm/(Co 0.6 nm, Pd 1.0 nm)<sub>3</sub> at  $T=303$  K after initial magnetoelectric annealing in  $E=0.1$  kV/mm and  $\mu_0 H=77.8$  mT. Hysteresis loops are measured by polar Kerr magnetometry in  $E=0$ , respectively. The *squares* show the virgin curve with a positive exchange-bias field of  $\mu_0 H_{EB}=+6$  mT. Isothermal-field exposure in  $E=-2.6$  kV/mm and  $\mu_0 H=+154$  mT gives rise to a loop with a negative exchange-bias field of  $\mu_0 H_{EB}=-13$  mT (*triangles*). (b) The *squares* show the same virgin reference loop. The *circles* show the hysteresis loop after isothermal-field exposure in  $E=+2.6$  kV/mm and of  $\mu_0 H=-154$  mT, giving rise to the same negative exchange bias of  $\mu_0 H_{EB}=-13$  mT. (c)  $\mu_0 H_{EB}$  versus number of repeated isothermal switching through exposure to  $E=+2.6$  kV/mm (*circles*) and  $E=2.0$  kV/mm (*squares*) at constant  $\mu_0 H=-154$  mT, respectively (adapted from [266])

### 3.5.2 Multiferroic-Based Devices

In 2007, Scott offered a brief, but elegant summary of where multiferroic-based devices, especially memory applications, might make an impact [267]. It is important to note that although ferroelectric random access memories (FeRAMs) have achieved fast access speeds (5 ns) and high densities (64 Mb) in a number of different materials, they remain limited by the need for a destructive read and reset operation. By comparison, magnetic random access memories (MRAMs) have been lagging far behind, although Freescale Corporation reported commercial production in 2006 of a smaller MRAM for testing. The appeal of multiferroics is that they offer the possibility of combining the best qualities of FeRAMs and MRAMs: fast



**Fig. 3.29** Multiferroic-based devices. (a) Tunnel magnetoresistance curves at 4 K at  $V_{dc} = 10$  mV in an  $\text{La}_{2/3}\text{Sr}_{1/3}\text{MnO}_3/\text{La}_{0.1}\text{Bi}_{0.9}\text{MnO}_3$  (2 nm)/Au junction, after applying a voltage of +2 V (filled symbols) and -2 V (open symbols). The combination of the electroresistance effect and the tunnel magnetoresistance produces a four-resistance-state system. (Adapted from [96]) (b) The sketch of the potential profiles for each of the eight configurations of a multiferroic-based tunnel junction. Here, the arrows denote majority- and minority-spin carriers,  $D$  displays the electronic density of states. (Adapted from [270])

low-power electrical write operation, and non-destructive magnetic read operation. At the 256 Mbit level, such memory devices [268] would be a “disruptive technology” and could eliminate competition such as EEPROMs (electrically erasable programmable read-only memories) for applications including megapixel photomemories for digital cameras or audio memories in devices such as mp3 players.

With this in mind, over the last few years, a number of new devices based on multiferroic materials and heterostructures have been demonstrated and proposed. In early 2007, Ju et al. [269] presented a theoretical investigation of an electrically controllable spin filter based on a multiferroic tunnel junction that could be switched between multiple resistance states. Soon after this, Gajek et al. [96] demonstrated the production of four logic states based on ultrathin multiferroic films used as barriers in spin-filter-type tunnel junctions. The junctions were made of  $\text{La}_{0.1}\text{Bi}_{0.9}\text{MnO}_3$  which was proven to be both ferroelectric and magnetic down to film thickness of only 2 nm and the devices exploited the magnetic and ferroelectric degrees of freedom of that layer. The ferromagnetism permitted read operations reminiscent of MRAM and the electrical switching evoked FeRAM write operations without the need for destructive ferroelectric readout. The results (Fig. 3.29a) suggest that it is possible to encode quaternary information by both ferromagnetic and ferroelectric order parameters, and to read it non-destructively by a resistance measurement. This work represented the starting point for future studies on the interplay between ferroelectricity and spin-dependent tunneling using multiferroic barrier layers and, in a wider perspective, suggested a new pathway toward novel reconfigurable logic spintronic architectures.

Yang et al. [270] proposed that eight different logic states could be achieved by combining spin-filter effects and the screening of polarization charges between two

electrodes through a multiferroic tunnel barrier (Fig. 3.29b). In this work, the conductance ratio was found to be dependent on the magnitude of the ferroelectric polarization, exchange splitting, barrier width, and bias voltage. In 2009, Jia and Berakdar [271] proposed a modified spin-field-effect transistor fabricated in a two-dimensional electron gas (2DEG) formed at the surface of multiferroic oxides with a transverse helical magnetic order. The local magnetic moments in the oxide are said to induce a resonant momentum-dependent effective spin-orbit interaction acting on the 2DEG and thus the carrier spin precession is dependent on the magnetic spin helicity that can be electrically controlled in the multiferroic. Such a device could, in turn, be used as a nanometer-scale, decoherence-suppressed spin field-effect transistor and as a nanometer flash-memory device.

As a final note, there are other possible applications for multiferroics and magnetoelectrics that might make impact in the coming year. The first is in sensors. By far, the quickest implementation of multiferroics and magnetoelectrics, especially bi-layered systems (consisting of a piezoelectric/magnetostrictive composite) is in magnetic field sensing elements. The work of Srinivasan, Viehland, and co-workers [228, 231] has already shown proof of this concept. These structures sense changes in magnetic field as a voltage signal through the mechanical coupling between the piezoelectric and magnetostrictive layer. The key advantage of this approach is its inherent simplicity, i.e., it does not require sophisticated processing, small dimensions, or expensive peripheral circuitry. Furthermore, there is a current trend to utilize antiferromagnetic resonance in ultrahigh frequency signal processing—opening up a new door for multiferroics to make in-roads into devices. This is an area that has not been well explored to date, but the idea is to take advantage of the possibility of controlling antiferromagnetic resonance with electric fields, thereby utilizing pre-existing multiferroic materials. Previous work (as is illustrated in Fig. 3.15) clearly demonstrated that the antiferromagnetic order of multiferroics such as  $\text{BiFeO}_3$  can be manipulated through electric field control of ferroelectricity [156, 158]. The question of interest today is to what frequency can this coupling be pushed? It is well known that as a consequence of the large magnetic anisotropy fields, resonance in antiferromagnets occurs at a frequency much higher than in conventional ferromagnets [272, 273]. In the case of the related orthoferrites (the parent compound to  $\text{BiFeO}_3$ ) antiferromagnetic resonances occur in the few hundred GHz range, thus opening up the frequency range from  $\sim 100$  GHz to 1 THz for future applications in signal processing.

### 3.6 Challenges for Multiferroic-Based Memories and Devices

The memory market is a highly competitive, as illustrated by the DRAM and Flash product evolution over the past decade or so. Thus, by far the biggest challenge facing new materials systems, such as multiferroic and magnetoelectric systems, is the ability to make a memory product that is competitive with the existing volatile and nonvolatile memories. Within the nonvolatile memory market-space, two fundamental attributes control the market penetration by any given technology. The first is

the density, often quantified in Flash. For SRAM and DRAM products the figure of merit is “ $F^2$ ” where “ $F$ ” is the minimum feature dimension. In CMOS based memories such as the ones described above,  $F$  generally relates to the characteristic CMOS generation, controlled by the gate metal lateral dimensions. Clearly, the smallest dimension could be simply  $F^2$ , i.e., the metal gate sets the storage cell dimension as well. This has not been achieved in *any* memory architecture. As a comparison, state-of-the-art Flash works at  $8F^2$ , while SRAMS work at  $40F^2$ . State-of-the-art FeRAM designs project a  $16\text{--}20F^2$  cell size, still significantly larger than Flash, while MRAMS are even larger (due to the need for an additional transistor). Multiferroics, can in principle, compete in this space if the multiple functionality (i.e., both the charge and the spin degrees of freedom) is capitalized. Challenges are present at the processing level as well. These challenges are also common to FeRAMs, namely the integration of complex oxides onto a Si-CMOS platform. Very little work has been done to explore the integration of multiferroics on such a platform. Likewise, the effect of polycrystallinity in multiferroic materials on the ultimate properties and performance needs to be explored in greater detail. Additionally, the reliability and robustness of switching processes and logic states have to be carefully studied as well. Finally, on a fundamental level, the limits of coupling behavior need to be fully explored.

### 3.7 Conclusions: Looking to the Future

We are poised at a very interesting juncture in the evolution of these novel materials. It has been over a decade since the reincarnation of multiferroics and magnetoelectrics. In this time, much progress has been made in synthesis, characterization, and theoretical treatments of such materials. It is, however, clear that the next few years are particularly critical in terms of the evolution of these materials into real applications. Thus, the concerted and collaborative effort of materials scientists, physicists, and device engineers is essential. Particularly, the critical role of device physicists in designing new possible pathways to use the multiferroic behavior is obvious. It may only be through the development of revolutionary new capabilities that the significant energy barrier to system development will be overcome. The onus is on the researchers of today to provide the impetus for this significant investment of time and money.

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**Part II**  
**Resistance and Phase Change Memories**

# Chapter 4

## Phase-Change Materials for Data Storage Applications

Dominic Lencer, Martin Salinga, and Matthias Wuttig

### 4.1 The Basic Principle of Phase-Change Based Data Storage

A particular promising approach for data storage devices is based on the fast reversible switching of so-called *phase-change materials* between an amorphous and a crystalline state. Both phases are characterized by very different material properties, thus providing the contrast required to distinguish between logical states. Phase-change recording was initiated in the 1960s by S. Ovshinsky [1] and is the state-of-the-art technique for rewritable optical storage. It is also among the most promising candidates to succeed Flash memory as Phase-Change Random Access memory (PCRAM) [2–4].

The principle of operation of phase-change based devices is illustrated in Fig. 4.1. A phase-change material is switched between the crystalline and amorphous state by providing a precisely controlled amount of heat. Currently, either laser pulses or electrical pulses are employed as heat sources. Starting from a crystalline bit, the temperature needs to be elevated above the liquidus temperature  $T_1$  using a short, high intensity (high current) pulse. Since only a spatially confined region is heated up, a huge temperature gradient between the molten bit and the surrounding material is obtained, leading to high cooling rates of about  $10^{10}$  K/s once the external stimulus is turned off. If the melt cools fast enough, crystallization is bypassed and a melt-quenched amorphous bit is formed once the temperature falls below a critical temperature, the glass transition temperature  $T_g$ . In this temperature regime, the

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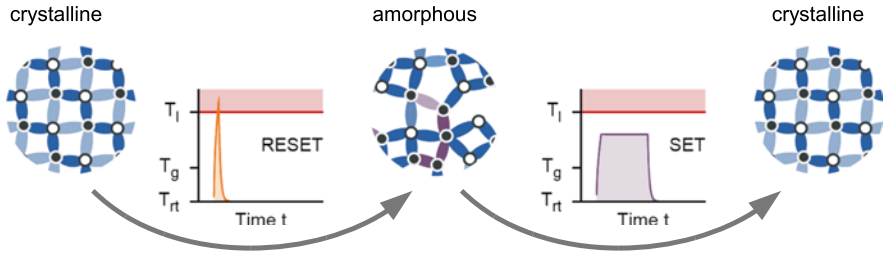
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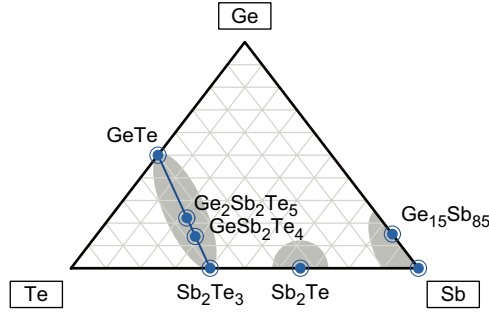
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**Fig. 4.1** The operation principle of phase-change devices is based on the reversible switching between the crystalline and amorphous state. Amorphization (also called *RESET*-operation) of a bit proceeds via melt-quenching, employing short current or laser pulses as heat sources. Here, a huge temperature difference between the confined melt and the surrounding material leads to extremely high cooling rates. Thus, the disorder of the liquid is frozen in. Crystallization (*SET*-operation) requires annealing of an amorphous bit at a temperature below the melting temperature for the atoms to adopt the energetically favorable crystalline order. From [5]

atomic mobility is so small that crystallization, though energetically favorable, is kinetically hindered. To switch from the amorphous back to the crystalline state, the temperature of the bit needs to be elevated for a sufficiently long period of time to a temperature where the atomic mobilities are high enough for crystallization to occur. Hence, the sample has to be heated significantly above the glass transition temperature. To read out whether a bit is amorphous or crystalline, low intensity (low current) pulses are employed to distinguish between low and high reflectivity (conductivity). Noteworthy are the timescales of phase-change recording; crystallization is typically the slowest process involved. Nevertheless, under optimal conditions it may proceed in a matter of nanoseconds. At ambient conditions, however, crystallization of an amorphous bit must not take place within many years to ensure data retention. This means that the crystallization rate of phase-change materials must increase by up to twenty orders of magnitude while the temperature is elevated by only a few hundred Kelvin. Besides the phase transition kinetics, optical and/or electrical contrast is of utmost importance for phase-change materials. In order to distinguish between the phases, their material properties, namely resistivity and conductivity, must differ significantly. In addition, specific applications call for further requirements, such as a small density change upon crystallization.

A number of materials have empirically been confirmed to meet the requirements named above. Most of the material families already identified can be found in the ternary Ge:Sb:Te-phase diagram shown in Fig. 4.2. On the pseudo-binary line connecting GeTe and  $\text{Sb}_2\text{Te}_3$ , the most prominent materials such as  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  are located [6, 7]. Besides  $\text{Sb}_2\text{Te}_3$ , also  $\text{Sb}_2\text{Te}$  offers suitable properties when combined with fractions of silver and indium, for instance, yielding the widely employed AgInSbTe (abbrev. AIST) [8]. Finally, another material family that has attracted considerable interest in the last years is found here, namely modifications of antimony such as  $\text{Ge}_{15}\text{Sb}_{85}$  [9, 10]. It stands out since it does not contain a chalcogen



**Fig. 4.2** Most phase-change materials are found within the ternary Ge:Sb:Te-phase diagram. In particular, the pseudo-binary line between GeTe and Sb<sub>2</sub>Te<sub>3</sub> stands out as it hosts the most prominent phase-change materials composed as (GeTe)<sub>m</sub>(Sb<sub>2</sub>Te<sub>3</sub>)<sub>n</sub>, with  $m$  and  $n$  being integer numbers. From [5]

component, despite the fact that this was commonly assumed to be a requirement. It can be understood as “doped” antimony.<sup>1</sup>

For the development of phase-change materials, it is necessary to understand the phases involved in phase-change recording, that is liquid, amorphous, and crystalline phase. This is a challenging task since none of the employed phases represents equilibrium-conditions, either inherently (amorphous phase) or due to the fast switching. Thus, since the phases are not unique (i.e., depending on the preparation conditions), their characterization is hampered. Furthermore, also the transition between the phases needs to be investigated and modeled. It is the aim of this chapter to briefly review the current state of research on selected aspects of phase-change materials. Therefore, one switching cycle, that is from crystalline over the liquid to the amorphous state, and back again to the crystalline state, is discussed.

## 4.2 The Crystalline Phase

The crystalline structures of phase-change materials, such as the well-studied and widely employed Ge:Sb:Te-materials (e.g., Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub>), typically exhibit a number of generic features. Along the lines of Da Silva et al. [11, and the references therein], the two limiting cases of the pseudobinary line, GeTe and Sb<sub>2</sub>Te<sub>3</sub>, are well suited to discuss these. GeTe exhibits a structure that closely resembles the rocksalt-structure, with Ge occupying the cation, and Te the anion sublattice. Yet, at temperatures below approximately 700 K, there is a displacement of the atomic positions along the [1 1 1]-direction. This leads to a splitting of the bonds from six equal to three strengthened, short and three weakened, long ones. These Peierls-like distortions

<sup>1</sup>Doping in the field of phase-change materials refers to much larger concentrations (typically on the order of some percent) than in usual semiconductors.



lead to an opening of the gap, and reduce the energy of the occupied states. The unit cell exhibits a slight rhombohedral distortion as a consequence of the atomic displacement [see 12, and references therein]. Also the structure of  $\text{Sb}_2\text{Te}_3$  can be understood in terms of a distorted rocksalt-like atomic arrangement. Again, there is an atomic alternation, and antimony has only tellurium neighbors in an octahedral environment. Yet, the sequence of alternating layers (“Te–Sb–Te–Sb–Te”) is terminated by adjacent Te-planes due to the tellurium-excess. The distance between these Te-planes is large compared to the Sb–Te-distances, and the bonding between them is explained in terms of the Van der Waals-interaction.

The Ge:Sb:Te-compounds inherit the structure ingredients mentioned before. In the metastable crystalline phase formed by fast annealing, they exhibit a rocksalt-like structure, with tellurium occupying the anion sublattice. The cation sublattice is initially randomly occupied by germanium, antimony and intrinsic vacancies. Thus, there is atomic alternation and a principal octahedral coordination. Via density functional theory calculations, energetically optimal sublattice occupations, towards which the systems tend by annealing, have been determined [11, 13, 14]. Yet, the theoretically most favorable structure is likely not obtained in experiments given the mismatch between optical properties calculated for those structures and measured ones [15]. Just like, GeTe, the atomic positions exhibit (Peierls-like) distortions from the high-symmetry-positions. The magnitude of the atomic displacements has been determined to amount to about 0.2 Å per atom by a variety of experimental [16, 17] and theoretical investigations [18–21]. For compositions close to GeTe, also a rhombohedral distortion of the unit cell is observed [22]. The aforementioned occurrence of intrinsic vacancies in the Ge:Sb:Te-systems, a rather unusual structural feature, has attracted considerable interest [23]. It has been argued to arise to balance the number of p-electrons per lattice site,  $N_p^\square$ . The respective count given  $n_i$  atoms per formula unit reads

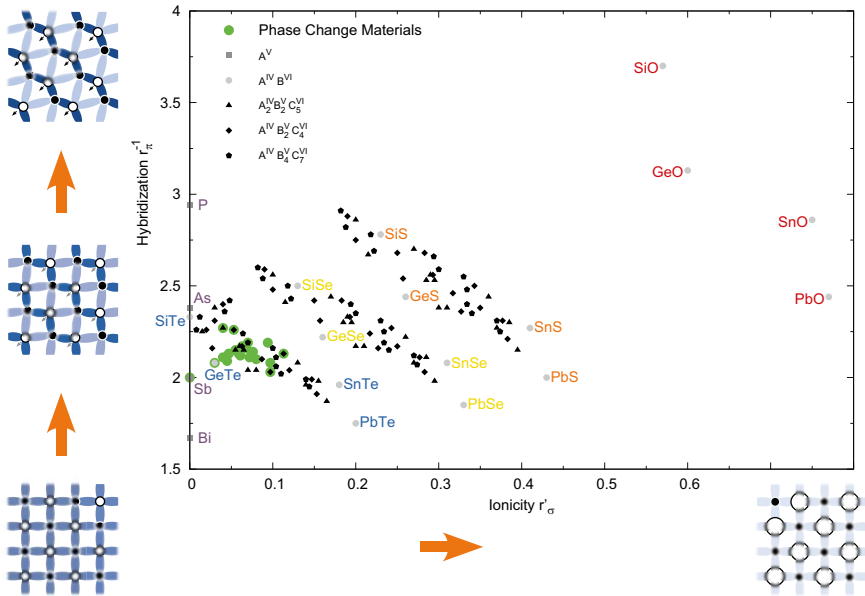
$$N_p^\square = \frac{2n_{\text{Ge}} + 3n_{\text{Sb}} + 4n_{\text{Te}}}{n_{\text{Ge}} + n_{\text{Sb}} + n_{\text{Te}} + n_{\text{V}}}. \quad (4.1)$$

Those compositions along the GeTe– $\text{Sb}_2\text{Te}_3$  pseudobinary line that form stable phases correspond to a number of three with  $n_{\text{V}} = n_{\text{Te}} - (n_{\text{Ge}} + n_{\text{Sb}})$  (i.e., by balancing the mismatch between the number of anions and cations by intrinsic vacancies).

The atomic arrangement and the resulting electronic structure of phase-change materials in the crystalline phase have been identified as key to understanding the contrast between the phases. Investigations of the dielectric function at and below the band gap have shown that phase-change materials exhibit a significant increase of the low-energy limit of the real part of the dielectric function (i.e.,  $\epsilon_\infty$ ) in the crystalline phase that is absent in both the amorphous phase and other semiconductors [24]. This electronic polarizability enhancement stems from a peculiar type of covalent bonding called *resonant bonding*; in a situation where more bonds are formed than can be saturated with the present number of valence electrons—the ratio being about two for phase-change materials—the groundstate wavefunction can be viewed as a superposition of energetically equivalent *contributing states* in

which only saturated bond are allowed. The energy of the system is reduced as compared to the energy of the contributing states by the resonance energy. Depending on the amplitude of the resonance energy, the electronic structure is very sensitive to external perturbations. This leads to the fingerprint effects of resonant bonding, large optical dielectric constants  $\epsilon_\infty$ , and Born effective charges  $Z^*$  [25]. The resonance is counteracted by the static, Peierls-like atomic distortions that lead to a smaller number of more saturated covalent bonds. Nevertheless, for small distortions resonance effects are weakened but prevail; density functional perturbation theory calculations on GeTe prove, that, while the Peierls-like distortion and the subsequent cell distortion significantly reduce the values of Born effective charge and optical dielectric tensor, they nevertheless remain anomalously large [12].

In order to assist this design rule, it is desirable to have a simple recipe for suitable materials. Based on the work by Littlewood [26], a two-dimensional map has been proposed [12], see Fig. 4.3. It is spanned by two coordinates,  $r'_\sigma$  and  $r_\pi^{-1}$ , that provide measures of the ionicity of the bonding and the tendency towards hybridization, respectively. The former quantity is derived from the size mismatch of the constituting atoms, the latter from the energetic splitting of s- and p-levels; the



**Fig. 4.3** Empiric map for materials with about three p-electrons per atomic site and even numbers of anions and cations. The axes that span the map are the tendency towards hybridization,  $r_\pi^{-1}$ , and the ionicity,  $r'_\sigma$ , both defined in the text. The coordinates of a large number of materials have been calculated (see the supplement to [12] for an index of materials). Phase-change materials are located within a small region of the map that is prone to the occurrence of resonant bonding. The graphs on the outside illustrate the weakening of resonance effects as one leaves this region due to the formation of less, more saturated covalent bonds via distortions or due to charge localization at the ions due to increasing ionicity. From [12]

larger the split, the less likely is hybridization, which is required for atomic distortions. A pronounced ionicity is unfavorable for phase-change materials since it weakens the covalent (resonant) bonds. A significant probability of hybridization/atomic distortions, on the other hand, also counteracts the resonance-character of the bonds. Thereby, phase-change materials should be located in a region of the map where both quantities are small to ensure the required contrast. Indeed, empirically identified phase-change materials shown as green dots in Fig. 4.3 span only a small region in the lower left corner.

The electrical properties of crystalline phase-change materials are dominated by the tendency towards forming large quantities of defects. As has been shown for GeTe [27], this shifts the Fermi-energy into the valence band, giving rise to p-type conductivity. Hence, the conductivity in the crystalline phase typically is metal-like, and orders of magnitudes larger than in the amorphous phase [28, 29]. Recently, it has been shown that disorder, likely due to the sublattice occupation, has a pronounced impact on the electronic mobility. In result, a metal-insulator-transition is observed for multi-component materials such as GeSb<sub>2</sub>Te<sub>4</sub> upon annealing, by which ordering of the sublattice is thermally triggered [30].

### 4.3 From the Crystalline to the Amorphous Phase

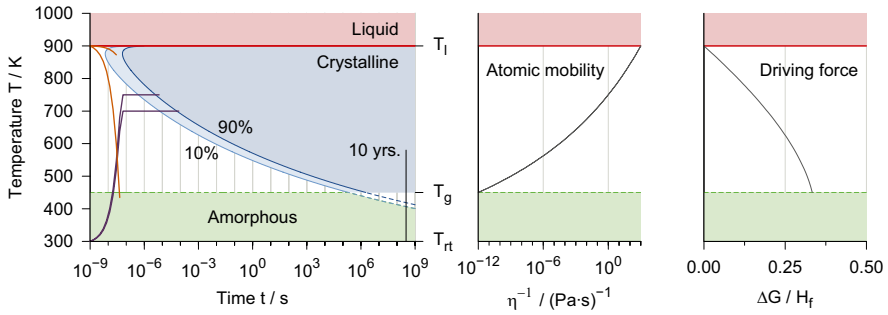
After a basic introduction into the phase-change cycle has been given already in the beginning of this chapter, a more detailed view shall be presented here. Therefore, Fig. 4.4 shows the phase transitions in terms of a time–temperature-transformation diagram. As this figure describes, the principle of phase-change materials relies on a peculiar interplay of the temperature-dependent atomic mobility  $D$ , that is inversely related to the macroscopic viscosity  $\eta$  via the Stokes–Einstein relation,

$$D(T) \propto T / \eta(T) \quad (4.2)$$

and Gibbs free energy  $G$ . The difference in  $G$  between the phases is the driving force for phase transitions; in equilibrium, the phase that minimizes  $G$  is adopted, but on small timescales, the finite atomic mobility kinetically hinders the establishment of equilibrium conditions. This enables the preparation of glassy bits by “freezing” a configuration of the undercooled liquid.

#### 4.3.1 Glass Formation

As a melt is quenched, it becomes increasingly rigid. Once a critical temperature, the glass transition temperature  $T_g$ , is passed and given that crystallization has been avoided, the atomic mobility becomes too small for structural rearrangements as required to reach equilibrium. Small atomic mobilities at ambient temperatures are



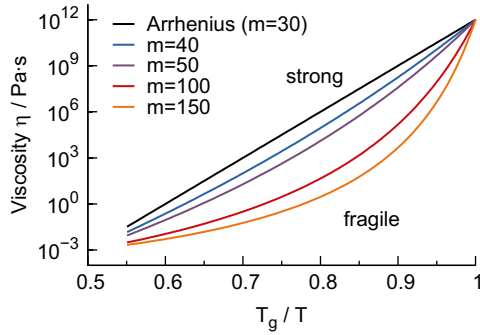
**Fig. 4.4** The graph on the *left* schematically shows the transformation of a fixed volume of a phase-change material depending on the time spent at a certain temperature. The crystallization of 10 and 90 %, respectively, of the material is indicated by *grey lines/areas*. As one cools the melt below the liquidus temperature  $T_l$  (typically around 900 K), the atomic mobility, shown in the *middle*, is very large. However, since the driving force for crystallization, that is the difference in Gibbs free energy between (undercooled) liquid and crystal, visualized on the right in units of the heat of fusion  $H_f$ , is small, crystallization does not take place immediately. It may thus be bypassed, if the melt is quenched sufficiently fast. This is visualized by two constant rate-quenching processes starting at  $T_l$ , the slower of which leads to partial crystallization. Typically, quenching rates of  $10^{10}$  K/s are required. At low temperatures, the driving force becomes larger, but the vanishing atomic mobility kinetically hinders crystallization. Eventually, as the glass transition temperature  $T_g$  (typically ranging around half  $T_l$ ) is passed, an amorphous bit is formed. While ideally it is long-time stable against crystallization at ambient conditions, it crystallizes in fractions of seconds if the temperature is elevated and kept for a sufficiently long time. Two annealing processes starting at room temperature  $T_n$  are indicated. Obviously, crystallization time and temperature are mutually dependent. From [5]

a key requirement for the stability of an amorphous bit. The mobilities, on the contrary, must not be small at elevated temperatures to enable fast crystallization. The glass transition temperature is commonly defined as the temperature, at which the viscosity equals  $1 \cdot 10^{12}$  Pa·s. The resulting glass is out of thermal equilibrium. Thus, a glass is always subject to “aging” effects, evidencing the relaxation towards equilibrium conditions.

To assess the ease of glass formation, it is instructive to note that the shape of the area in Fig. 4.4 that refers to crystallization is strongly affected by the temperature-dependence of the viscosity. Whether a glass may be formed at small cooling rates (*easy glass former*) or whether this may only be facilitated via rapid quenching (*marginal or bad glass former*) as in the case of phase-change materials, can thus be linked to the viscosity. The temperature-dependence of  $\eta$  varies among materials as is shown in Fig. 4.5. If it is Arrhenius-like, a liquid is called *strong*. However, many materials exhibit a behavior empirically described by the Tamann–Vogel–Fulcher ansatz

$$\eta(T) = \eta_0 \cdot \exp(A / (T - T_0)) \tag{4.3}$$

with  $\eta_0$ ,  $A$  and  $T_0$  being constants. Such liquids are referred to as *fragile*. As a measure of the deviation from Arrhenius-behavior, the fragility  $m$  is introduced as a steepness-index at  $T_g$  via



**Fig. 4.5** The viscosity of a liquid typically depends exponentially on temperature. If the dependence is Arrhenius-like, it is called a strong liquid. If the dependence at  $T_g$  is steeper, the liquid is referred to as fragile. The deviation from Arrhenius-behavior is indicated by the steepness at  $T_g$ , the fragility  $m$ . From [5]

$$m = \frac{\partial(\log_{10} \eta)}{\partial(T_g / T)} \Big|_{T = T_g}. \quad (4.4)$$

A detailed review of these aspects has been given by Angell et al. [31]. For phase-change applications, a rather fragile liquid appears favorable since the crystallization speed would increase with temperature (above  $T_g$ ) more rapidly.

Glass transition temperatures can experimentally be assessed via differential scanning calorimetry since the transition from the glass to an undercooled liquid appears as an endothermic step. Such measurements have shown that for phase-change materials,  $T_g$  adopts values of about 450 K, ranging around half the liquidus temperatures [32]. Empirically, this ratio between  $T_g$  and  $T_l$  characterizes phase-change materials as marginal glass formers [see 33, and the references therein].

### 4.3.2 Glass Rigidity and Bond Constraint Theory

In order to design a phase-change material, it is desirable to have a theory that connects stoichiometry with structure, but also with glass forming ability. Thus, the concept of *bond constraint theory* will be briefly explained. This theory is an approach to characterize the rigidity of an amorphous covalent network, based on the (mean) atomic coordination. In order to fix an object at a given place, three constraints are required. If more are present, the loss of one does not generally lead to the release of this fixation. Less constraints, on the other hand, leave open degrees of freedom, giving room to limited movement (i.e., so-called floppy modes). It is hence reasonable to classify covalent networks such as glasses according to the number of constraints per atom,  $n_c$ . An *ideal* glass has a value of three, whereas *floppy* glasses have less and *stressed rigid* glasses more constraints per atom.

Moreover, bond constraint theory also provides a link between  $n_c$  and the experimentally accessible coordination number,  $r$ . Given that in a covalent network the number of bond-stretching constraints equals half the number of bonds and the respective number of bond-bending constraints sums up to  $2r - 3$ , then the total relationship as proposed by Phillips [34] reads

$$n_c(r) = \frac{5}{2}r - 3 \Leftrightarrow r = \frac{2}{5}(n_c + 3). \quad (4.5)$$

This implies that in an ideal glass,  $n_c=3$ , the average coordination should take the value 2.4. Vice versa, since the average coordination is often characteristic for an atomic species, changing the stoichiometry of a glass allows to modify  $r$  and thereby to affect the rigidity of the glass. In this context, it is worth noting the so-called  $8 - N$ -rule; with  $N$  being the number of valence electrons of an atom, this rule states that generally, the coordination in a covalent environment is equal to  $8 - N$ . For instance, germanium with its two s- and two p-valence electrons is expected to be fourfold coordinated, while antimony would accordingly adopt a threefold and tellurium a twofold coordination. The  $8 - N$ -rule successfully explains and predicts the atomic coordination for a wide range of materials composed of elements from the groups V, VI, and VII [35]. But as one goes down in the fourth column of the periodic table, the limits of the  $8 - N$ -rule become obvious; elemental lead is not tetrahedrally, but octahedrally coordinated, owing to the fact that due to relativistic effects hybridization becomes unfavorable [26].

It has been found that in many cases it is not a single point but rather an extended region, the so-called intermediate phase, which separates floppy and stressed rigid glasses. Thus, instead of one there are two rigidity transitions upon variation of  $r$  as evidenced by experiments for chalcogenide glasses, with the intermediate phase marking a range of *isostatic* rigidity [36]. Interestingly, a link between rigidity of the glass and the temperature-dependence of the viscosity of the liquid has been discussed. In [37], it has been claimed that both floppy and stressed rigid glasses exhibit fragile liquids, whereas intermediate glasses should exhibit strong liquids.

Easy glass formation is expected only for ideal/intermediate glasses [37]. This is unfavorable for fast crystallizing phase-change materials as argued before. Indeed, typical phase-change materials yield, according to the  $8 - N$ -rule, numbers of  $r$  between 2.6 and 3.2, locating them in the region of stressed rigid glasses. The coordination numbers derived from structural investigations (see Sect. 4.4.1) tend to be higher as will be shown below, so phase-change materials are seemingly even more stressed rigid than expected by the  $8 - N$ -rule. Recently, extensive work on the rigidity and application of bond constraint theory in the ternary Ge:Sb:Te phase diagram has been presented by Micoulaut et al. [38]. Employing density functional theory calculations, these authors were able to prove that phase-change materials indeed fall into the stressed rigid regime.

Due to the importance of  $T_g$  for data retention, a large body of work on phase-change materials is concerned with means of material modifications to increase the value of  $T_g$ . In general, a host phase-change material such as  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  or antimony

is chosen for its optical and electrical properties in the amorphous and crystalline phase. Then, the impact of the addition of other elements is investigated. In the framework of bond constraint theory, the observed increase of  $T_g$  via the addition of so-called network forming elements, for instance from group IV, to a host phase-change material can be understood by the resulting increase of the average coordination number  $r$ . One important aspect not included in bond constraint theory, though, is the fact that not only the number of bonds but also the bond energies need to be taken into consideration. Thus, the dependence of  $T_g$  on  $r$  via stoichiometry variation may deviate from a monotonous increase. An improved model was proposed by Lankhorst [39] (see also [40]) that empirically relates  $T_g$  to the enthalpy of atomization of an amorphous network. The latter is calculated from the bond enthalpies of all bonds present in the system. It has been successfully applied to resolve the impact of Al- and Cu-doping on the glass transition temperature in Ge:Sb and Sb:Te as has been confirmed by experiment [41]. A complimentary study on Al-doping of Ge:Te was conducted by Katsuyama and Matsumara [42]. The Lankhorst-model comes at the expense of simplicity as for the bond energies the atoms participating in each bond need to be explicitly known. Hence, structural information on phase-change materials in the amorphous phase is required.

## 4.4 The Amorphous Phase

The amorphous phase of typical phase-change materials is studied intensively regarding two aspects; the structure is investigated in order to link it to the properties of the glass as well as the fast kinetics. Its electrical conductivity, on the other hand, is of crucial importance for upcoming electrical memories. Both fields shall be addressed in this section.

### 4.4.1 Atomic Structure

Since amorphization via melt-quenching relies on a rapid decrease of atomic mobilities, it can be expected that the glass inherits structural features of the liquid. Consequently, the investigation of the structure of both the liquid and the amorphous phase is of interest. The aim of these studies is twofold; on the one hand, similarities and differences with respect to the crystalline phase are investigated. This way, the contrast between the phases could possibly be linked to the difference in bonding. Moreover, it is often argued that fast kinetics would imply that the structural rearrangements upon crystallization are necessarily small. On the other hand, the identification of coordination numbers and bond types enables the application of concepts introduced in the last section, such as bond constraint theory, beyond approximations (e.g., without relying on the  $8 - N$ -rule).

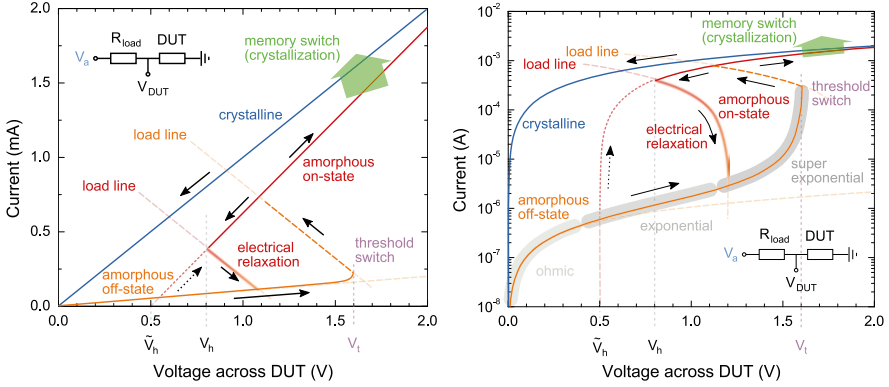
As of today, there are numerous experimental and theoretical studies available in the literature. Regarding the liquid phase, Steimer et al. [43] performed neutron diffraction experiments on a wide range of materials, and found that phase-change materials exhibited octahedral coordination. Further confirmation of the prevalence of this structural motif is given by theoretical studies [44]. Moreover, an alternation between atomic species (e.g., ABAB) is observed [20]. Thus, the structure of the melt is apparently similar to that of the crystalline state. The identification of octahedral or tetrahedral bonding geometries is a recurring motif in the literature. The reason why the occurrence of octahedral geometries is of interest is the fact that it is rather unexpected according to the  $8 - N$ -rule. For germanium,  $sp_3$ -hybridization may be regarded as the energetically most favorable electronic structure to achieve a fourfold coordination as adopted in elemental germanium. The presence of non-tetrahedrally coordinated germanium in phase-change materials thus is remarkable and clearly caused by its bonding environment.

The vitrified, amorphous phase is easier to investigate as the temperature does not need to be elevated. Yet, the published studies, that treat GeTe and  $Ge_2Sb_2Te_5$  in particular, come to significantly different conclusions. The problem, to what extent the experimental results depend on the sample preparation and thermal history, remains unclear as of this writing. In many studies, the use of as-deposited amorphous samples is necessary to yield the required, large amount of amorphous material. Yet, the kinetics of as-deposited amorphous and melt-quenched amorphous phase differ significantly, which must have its origin in structural differences [45].

Initially, EXAFS- and XANES-data (extended x-ray absorption fine structure and x-ray absorption near-edge spectroscopy, respectively) were interpreted in terms of the so-called umbrella flip-model, where germanium switches from tetrahedral to octahedral positions upon crystallization. Apart from this, chemical ordering and octahedral bonding of the remaining species was concluded [16, 46]. Many successive studies interpreted the phase transition along the lines of this model, see, for instance, [47–50]. Subsequent experimental studies, in particular those by Jovari et al. [51, 52], rejected such simple structural models, yet confirmed the presence of tetrahedral coordination of germanium. Kohara et al. [53], on the contrary, found a correlation between tetrahedral coordination and the occurrence of homopolar bonds; due to chemical ordering in  $Ge_2Sb_2Te_5$  and thereby the absence of homopolar (or Ge–Sb) bonds, octahedral coordination was obtained for germanium.

The obvious differences between structure models derived from experiments alone have motivated various large-scale molecular-dynamics simulations. Materials investigated span the pseudobinary line  $(GeTe)_m(Sb_2Te_3)_n$  from GeTe [54, 55] over  $Ge_8Sb_2Te_{11}$  [56] and  $Ge_2Sb_2Te_5$  [20, 21, 54, 57–60] to  $Sb_2Te_3$  [61]. In these simulations, the link between tetrahedral germanium and the occurrence of bonds other than Ge–Te is confirmed. The concentration of tetrahedral germanium is about one third, leaving octahedrally coordinated germanium atoms as the majority species. Moreover, cavities as precursors of the intrinsic vacancies found in the metastable crystalline phase have been identified. It is observed that coordination numbers—despite the ambiguity in defining them—tend to be slightly larger than those derived





**Fig. 4.6** The current–voltage characteristics of phase-change materials (device under test, DUT), shown schematically in both linear (*left*) and logarithmic scaling (*right*), exhibit an interesting effect called threshold switching. For small electric fields the curves of the low resistive, crystalline and the high resistive, amorphous phase differ significantly. However, the situation changes if a critical voltage (corresponding to a field strength of some ten  $V/\mu\text{m}$ ) is exceeded. The amorphous phase suddenly becomes much more conductive, switching to the so-called *ON-state* as opposed to the *OFF-state*. This effect, called threshold switching, enables sufficient joule heating for crystallization (memory switching) at moderate voltages. Further aspects of threshold switching marked in the graphs are discussed in the text. From [65]

from the 8 –  $N$ -rule. Hence, phase-change materials are seemingly even more stressed rigid than expected from the 8 –  $N$ -rule.

#### 4.4.2 Electrical Properties

The electrical conductivity of amorphous phase-change materials exhibits a pronounced dependence on the strength of the applied electric field as shown in Fig. 4.6. Two states can be discerned, the amorphous *OFF-* and *ON-*states. Until a critical field is reached, the threshold field  $E_t$  (or threshold voltage  $V_t$ ), the system remains in the *OFF-state*. Here, the conductivity remains small and exhibits a thermally activated transport behavior,

$$\sigma(T) = \sigma_0 \exp\left(-\frac{E}{kT}\right) \quad (4.6)$$

with an activation energy of approximately half the measured optical gap,  $E_{\text{A cond.}} \approx 1/2 E_{\text{G opt}}$ . When the field exceeds the threshold value, the conductivity increases significantly (*ON-state*). Threshold fields are typically about some ten  $V/\mu\text{m}$  ([62] and the references therein [63, 64]). From a technical point of view, this behavior is very desirable since crystallization of an amorphous bit is facilitated via Joule-heating. Without the *threshold switching*, large voltages would need

to be applied in order to drive a sufficiently large current for heating and thus crystallization to occur. Threshold switching is to be distinguished from *memory switching* that refers to crystallization, whereas threshold switching is a fully reversible phenomenon specific to the amorphous phase.

The discovery of threshold switching for data storage devices dates back to the pioneering work by Ovshinsky [1], and many models have been proposed to account for it ever since. Most authors suppose that threshold switching is an electronic (rather than a thermal or structural) effect. Emin [66] concludes that at elevated fields, the density of small polarons becomes larger. Thus, due to their proximity, lattice deformation becomes unfeasible once the threshold field is reached. Therefore, carriers may not localize anymore and the material becomes highly conductive. In the picture of Ielmini and Zhang [67], Ielmini [68] (and the references therein), that is Poole–Frenkel conduction, the electric field increases the probability of a carrier that occupies one trap to get to another one nearby. At low fields, this requires extended states. At the threshold field, also direct tunneling becomes possible, leading to the conductivity increase. Another model presumes that threshold switching stems from a field- and carrier density-dependent generation mechanism, thus providing a positive feedback once a critical field is attained. At low fields, however, recombination counterbalances the generation [62, 69, 70]. There are various possible microscopic models that could account for this phenomenological effect such as impact ionization [71]. An alternative to the electronic models of threshold switching is provided by field-induced nucleation [72]. It is argued that at the threshold field, a crystalline filament forms in the amorphous volume, connecting the electrodes. The origin of this effect is ascribed to a field-dependence of the free energy of the system. For further details, the interested reader is referred to [4, 65].

An issue important for so-called *multi-level storage* is the drift of the amorphous resistivity with time. Multi-level storage aims at increasing the storage density by differentiating more than two logical states per cell. This is done by varying the volume of the amorphized part of the cell. However, one finds that the resistivity of a (partially) amorphous cell steadily increases with time. Multi-level storage is only feasible, if this drift is confined to a small resistivity interval associated with one logical state. The increase obeys a power law dependence on time. As the process is temperature-activated, it can be accelerated by raising the temperature. Since progressing crystallization is expected to lead to a drop in resistivity as the crystalline phase is more conductive, drift cannot be explained by the formation of crystalline nuclei. Moreover, since also threshold voltages tend to drift in the same fashion, a common origin of both effects is anticipated. There are multiple candidates to explain the resistance drift effect. Yet, this topic is still up to debate. Most authors consider a general time and temperature-dependence of the parameters entering Eq. (4.6), in particular of the activation energy [73].

On the one hand, a change in the size of the gap due to stress relief has been discussed. In this universal model, hydrostatic pressure is exerted on the amorphous volume after quenching due to the significant density increase as seen by X-ray reflectometry measurements [74]. The stress causes the gap and thus the activation energy to decrease. The recovery of the gap then leads to the observed drift [75, 76].

On the other hand, models involving a change in the occurrence of particular electronic states have been proposed. More specifically, the presence of valence alternation pairs (VAPs) and an increase in their number, resulting in an increasing resistivity, have been suggested [75, 77]. This, however, is to be contrasted with studies that question the presence of VAPs in phase-change materials [21, 78]. Another model (see [79] and references therein) also aims at localized states at the gap edges, which might arise as tails; charge transport via hopping involving these states is hampered, if the respective density of states decreases. If the states vanish due to structural relaxation, a decrease in the hopping-conductivity results in a resistance drift. In addition, the position of the Fermi-level may be expected to move towards the middle of the gap, if it had previously been pulled towards one edge by these states.

## 4.5 Crystallization of an Amorphous Bit

After the discussion of the properties of both the crystalline and the amorphous phase, as well as the process of amorphization in the preceding sections, only the process of crystallization remains to return to the initial point of the phase-change cycle. Commonly, this phase transition is modeled along the lines of the classical theory of crystallization.

### 4.5.1 Classical Theory of Crystallization

Within this theoretical framework, two mechanisms of crystallization are discernible, nucleation and growth. Nucleation is the process of forming a crystalline nucleus within an amorphous matrix. Growth refers to the progression of the phase front separating amorphous and crystalline regions. The driving force for crystallization is the free energy gain. Since an energy barrier separates amorphous and crystalline structures, sufficient thermal energy has to be provided to enable the system to overcome it. Nucleation is typically modeled in a continuum-approximation, neglecting the discrete atomic structure. Then, the formation of a crystalline nucleus involves the formation of a continuous interface. The difference in free energy  $\Delta G(r)$  for a spherical crystalline cluster of radius  $r$  within a liquid (undercooled melt) is

$$\begin{aligned}\Delta G(r) &= V(r) \cdot \Delta G_v + A(r) \cdot \sigma \\ &= \frac{4}{3} \pi r^3 \cdot \Delta G_v + 4 \pi r^2 \cdot \sigma ,\end{aligned}\tag{4.7}$$

with  $V$  and  $A$  being volume, and surface of the nucleus,  $\Delta G_v$  the difference in  $G$  between the two phases per unit volume, and  $\sigma$  the interfacial energy per unit surface area. At the critical radius,

$$r_c = \frac{2\sigma}{|\Delta G_v|} \quad (4.8)$$

$\Delta G(r)$  exhibits a maximum. So only nuclei of a sufficient initial size larger than  $r_c$  gain energy by growth. Below this critical size, their dissolution is energetically preferred as it removes the interface. According to Becker and Döring, a steady-state distribution of subcritical clusters is formed after an incubation time  $\tau$ . Recently, Lee et al. [80] proposed fluctuation transmission electron microscopy to experimentally study the evolution of such subcritical nuclei in thin films upon laser irradiation. From the steady-state distribution, a steady-state nucleation rate  $I_{ss}$  given by

$$I_{ss} \propto \eta(T)^{-1} \exp\left(-\frac{\Delta G(r_c)}{k_B T}\right) = \eta(T)^{-1} \exp\left(-\frac{16\pi}{3k_B T} \frac{\sigma^3}{(\Delta G_v)^2} \cdot f(\theta)\right) \quad (4.9)$$

is derived. For the moment, we shall neglect the factor  $f(\theta)$ , thus setting it to unity. Once postcritical crystalline nuclei have been formed, their speed of growth for sizes  $r \gg r_c$  is derived in the framework of classical crystallization theory as

$$u(T) = \frac{\partial r}{\partial t} \propto \frac{T}{\eta(T)} \left[ 1 - \exp\left(-\frac{\Delta G(T)}{k_B T}\right) \right]. \quad (4.10)$$

The temperatures at which nucleation and growth exhibit their respective peak values are not the same. Furthermore, process might be more dominant than the other. Hence, nucleation-dominated and growth-dominated crystallization have been observed in the rather large volumes encountered in optical recording, leading to a sub-classification of phase-change materials. In the case of nucleation-dominated crystallization, the time it takes to crystallize an amorphous bit does not depend on its volume to a first approximation. Growth-dominated materials, on the contrary, do exhibit a volume dependence; the smaller the volume, the quicker it is completely crystallized [81]. In general, the sub-classification becomes less helpful for small volumes, where geometry and interfaces play a more important role, increasing the contribution of crystal growth to the transformation. By amorphization of a bit, usually a crystalline rim is created. Hence, the process of growth is typically decisive in electronic phase-change memories, also because no incubation time as for nucleation is involved.

So far, we have only considered homogeneous phases. However, the activation energies can be affected by introducing heterogeneities. This is incorporated into the framework of crystallization theory by the factor  $f(\theta)$ , with  $\theta$  being the wetting angle. Impurities and interfaces can catalyze nucleation, but also, they can hinder growth. If heterogeneous sites play a dominant role, crystallization shifts from being triggered in the whole volume of the material to the vicinity of these heterogeneous sites. Interfaces are almost inevitable in phase-change recording. In nano-scaled electrical devices, their presence near the active material cannot be avoided.

In fact, the choice of the dielectric capping material in optical discs [82, 83] or electrode material in electrical memory cells [84] has been shown to significantly influence the crystallization behavior; below a thickness of about 5 nm, crystallization temperatures are even dominated by the choice of the interface material.

The actual configuration of the amorphous phase itself has a pronounced impact on the crystallization properties. Particular structural features of an as-deposited amorphous phase, that are not present in a melt-quenched amorphous phase, might vanish for good after the first crystallization, and thus be irrelevant for applications that involve countless numbers of cycles. Various authors have noted that the first crystallization of an as-deposited amorphous phase may be different from recrystallization of a melt-quenched phase [85–88].

As mentioned already in Sect. 4.3.2, tuning the crystallization kinetics by “doping” (stoichiometry variation) is routinely investigated in the field of phase-change materials. The interested reader is referred to the article of Zhou [89]. Notably, two scenarios can be discerned; a nucleation-dominated material may crystallize faster if doped with a certain element. However, the same dopant may impede growth in a growth-dominated material.

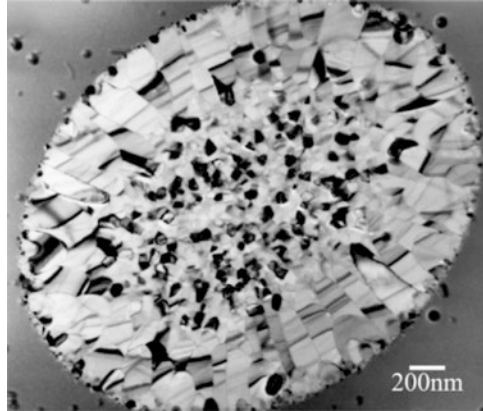
One can distinguish between three temperature regimes relevant for research on the crystallization kinetics. The first regime is located at around the glass transition temperature. In this temperature interval, crystallization ought to proceed very slowly. Experimentally, this enables the direct observation of nucleation and growth. This has been demonstrated using high-resolution transmission electron microscopy [90, 91] and atomic force microscopy [92]. From such measurements, data retention at a given temperature can be assessed. A second temperature regime of interest is situated at around the liquidus temperature. The small driving force for crystallization enables to study the undercooling of droplets employing differential thermal analysis, and thereby the determination of the interfacial energy  $\sigma$  [93]. The experimentally most challenging yet technologically relevant temperature regime is located in the temperature regime where crystallization proceeds the fastest. Here, materials are tested under operation conditions, either embedded in production-type samples or using specialized equipment to spatially and or temporally resolve the phase transition. In particular, the minimum crystallization time is assessed this way.

Information on the physical processes that lead to crystallization can also be reconstructed from the morphology of a crystallized bit [85, 94, 95]. In particular transmission electron microscopy as presented by Friedrich et al. [96]—shown in Fig. 4.7—yields detailed insight into the distribution and shape of crystallites, from which the distribution of nuclei and their growth may be inferred.

### 4.5.2 Atomistic Modeling of Crystallization

So far, we have employed the continuum approximation, neglecting the discrete atomic structure. The energy barrier separating the phases has not been linked to the composition or the microscopic structure. Thus, it is desirable to improve the

**Fig. 4.7** Transmission electron micrograph of a laser-crystallized spot in an as-deposited amorphous  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ -film. From [96]



understanding of the crystallization kinetics by developing and testing atomistic models of the phase transition.

A remarkable, now however somewhat obsolete model for Ge:Sb:Te-systems was given by Kolobov et al. [16], the so-called umbrella-flip model. It stated that the main structural rearrangement taking place upon crystallization is a flip of germanium from tetrahedral to octahedral sites. Since this model not only gave an intuitive explanation of why the phase transition proceeds so fast, yet involved a change in bonding significant enough to account for the contrast observed, it attracted much attention. The extensive theoretical simulations and experimental studies in recent years that have been addressed before, however, show that while tetrahedrally coordinated germanium-atoms are indeed present in the amorphous phase, they represent only a minority, making up only roughly one third of all germanium atoms. Also, they typically involve homopolar Ge–Ge or Ge–Sb bonds (“wrong bonds”) rather than only Ge–Te bonds as stated by the umbrella-flip model.

Though a simple local structural scheme like the umbrella-flip model is appealing, it is unlikely that such a model realistically or universally accounts for the phase transition in phase-change materials. Therefore, research has shifted to molecular dynamics simulations of the amorphous phase of particular materials as discussed before, and even the simulation of complete phase-change cycles [58].

## 4.6 Applications Employing Phase-Change Materials

The aim of the last part of the present chapter is to give an overview over the various applications that employ phase-change materials, and an outlook on their future development.

### 4.6.1 *Optical Storage*

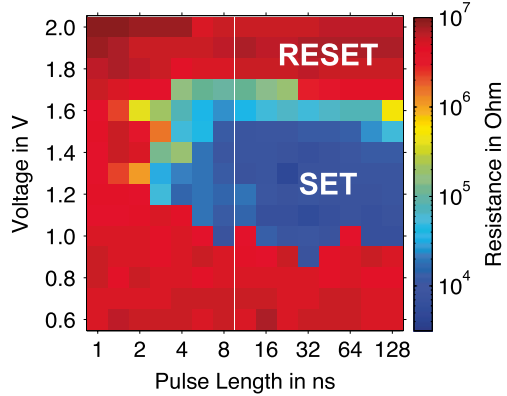
Presently, optical data storage devices represent the most common application of phase-change based recording. With the introduction of blue laser light and a further increase of the numerical aperture, the race for higher resolution and hence the development of this field may at first seem to have come to an end. Room for increasing storage capacity would be left only by increasing the number of data layers per disk. At present, a 100 GB disk employing three data layers marks the upper limit for such data storage devices, paving the way to the fourth generation of commercial optical phase-change based media [97]. However, another way of increasing capacity has been found in the course of phase-change research, that is near-field recording. The so-called Super-RENS effect (super-resolution near-field structure) refers to the observation that structures smaller than the diffraction limit can be fabricated by combining phase-change films with an additional thin layer in close proximity [98]. In an elegant realization, the part of the optical system that needs to be located very close to the phase-change film to enable near-field recording is incorporated into the disk structure itself. The extra layer typically functions as a dynamic aperture, which should at the same time be small and highly transmissive (aperture-type Super-RENS). Materials successfully employed for these mask layers typically comprise materials related to phase-change materials such as antimony [98, 99],  $\text{Sb}_2\text{Te}_3$  [100] and  $\text{PbTe}$  [101] or even phase-change materials themselves [102]. The effect of super-resolution may be achieved by various types of interaction between matter and light. No consensus on the exact origin of the Super-RENS-effect using the aforementioned materials has been reached yet [102–108].

### 4.6.2 *Electronic Storage*

When phase-change materials were introduced in 1968 by Ovshinsky [1], electronic memories were among their first suggested applications. Nevertheless, only now that the discovery of fast-switching phase-change materials meets the ability to create nano-scaled structures, it is possible to create competitive, non-volatile phase-change based electronic memories: *phase-change random access memory*, usually abbreviated *PRAM* or *PCRAM*. As can be seen from the PTE-diagram shown in Fig. 4.8, operation can be facilitated on the timescale of few nanoseconds which is orders of magnitude faster than Flash. PCRAM makes extensive use of the threshold switching effect presented in Sect. 4.4.2. In order to supply sufficient Joule heating power  $P_J = U \cdot I = U^2 / R(U)$  to quickly raise the temperature to levels high enough for crystallization to take place on a small timescale (cf. Fig. 4.6), very high voltages would be required, if threshold switching would not occur. Thus, it allows to avoid voltage upconversion.

Various designs of PCRAM cells have been proposed. A line-cell is simply a lateral line of a phase-change material that connects two electrodes. This concept

**Fig. 4.8** Characterization of the re-crystallization of a PCRAM-device employing GeTe as the active material using an electric tester. The different grey scales show the resistance change upon the application of electrical pulses of given length and voltage. Crystallization can be triggered by applying pulses as short as only about 5 ns. Modified from [81]



appears advantageous due to the ease of fabrication and low power consumption of these cells [63]. More common is a vertical stack of layers, where a small volume of phase-change is located on top of a highly resistive heater element. Here, a portion of the phase-change volume that is close to the heater, that typically features a reduced diameter to increase the current density, is switched between the phases. Recently, an improved version of a PCRAM-cell has been realized that comfortably integrates the cell selector into the cell design [109]. By the use of an Ovonic threshold-switch (OTS) rather than a bipolar junction transistor, for instance, a selector with no more than the same spatial footprint as the memory cell itself (i.e.,  $4F^2$ ,  $F$  being the feature size) is possible. The OTS is just a thin layer of a material that exhibits threshold-switching. If the voltage drop over the OTS (due to the voltage applied between word- and bit-line) exceeds the threshold field, the memory cell that is in series with the OTS is selected. The simple design may also allow the stacking of layers of PCRAM-cells, increasing the storage density by making use of the third dimension.

Among the criteria for a memory technique to be promising, scalability is a key requirement. Lack of scalability is one of the reasons why alternatives to Flash memory are actively pursued. Two factors may be discerned when scalability is addressed. On the one hand, the phase-change material must retain its properties despite reduction of its volume. On the other hand, the space taken up by dielectrics and the electronics necessary to address and control the memory cell must be taken into account as well. Nano-scaling is particularly advantageous to phase-change memory, since both energy consumption and crystallization time decrease upon volume reduction. The latter stems from the fact that for small memory cells, crystallization dominantly takes place via growth. The impact of nano-scaling on the material and device characteristics has recently been summarized in a detailed report by Raoux et al. [3]. Other aspects that can be subsumed under scalability are the aforementioned prospect of stackability as well as multi-level storage via control of the amorphized volume fraction.

So far, the advantages of PCRAM over competing memory technologies have been given in terms of its non-volatility, speed, and attainable storage density.



Another aspect, however, is cyclability (i.e., the number of possible write-cycles). The two main wear processes identified so far are electromigration and void formation. It is found that for cells based on Ge:Sb:Te-materials, the spatial distribution of the elements changes upon set and reset operations. In particular, antimony accumulates at the cathode, pushing germanium aside. Thus, the composition in the active volume and thereby the cell properties change. Operation at reversed polarity, though, can “repair” such a cell [110]. The density change upon crystallization and atomic mobility may also hamper the electrical contact via void formation [111]. In addition, degradation of the electrodes (e.g., diffusion into the phase-change material) and phase segregation in the case of non-stoichiometric materials may also be regarded as limiting factors. Nevertheless, though the exact number of possible cycles depends on a variety of factors, it is generally expected to exceed the corresponding value of Flash by some orders of magnitude.

Beyond optical and electrical data storage, various further uses have been developed. To mention one notable idea, the fact that the resistivity of a phase-change cell depends on its history (i.e., more than just two logical states can be represented by one cell, multi-level storage) has led to the proposal of using such devices to emulate the behavior of synapses, paving the way for cognitive information processing [112]. In that sense, phase-change based data storage does not only hold the potential to serve as a fast and reliable, universal non-volatile memory. Moreover, this technology could also revolutionize the way we process data.

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# Chapter 5

## Emerging Oxide Resistance Change Memories

Myoung-Jae Lee

The state of the art in resistance-based memory technology is presented. Recently memory technology has been focused on convergence towards ubiquitous memories which are non-volatile, have random access, and have fast programming times. This chapter is focused on electrically induced resistive change memories (including the resistive switching materials and mechanism) and other applications. Resistive random access memory (RRAM) has the simplest structure of new memory technologies, in fact the resistance change phenomenon can be observed in a metal–insulator–metal structure. Also, the switching speed has been reported to be about 10 ns and the resistance change effect scales down to cell sizes of  $10 \times 10 \text{ nm}^2$  [1, 2]. First, we review classification of resistance memory and materials: unipolar, bipolar, ionic, and electronic effect memory. The second section deals with structure of cell stack architecture, which is a very important merit of resistance memories in particular, RRAM cell scaling and RRAM integration. In the final section the superior intrinsic scaling characteristics of RRAM compared to charge-based devices, and multilevel cell (MLC) RRAM, are discussed. Finally, we conclude with some comments on the outlook, future works, and research necessary for realization of RRAM technology.

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## 5.1 Introduction

### 5.1.1 Overview of Oxide Resistance Change Memory

Oxide resistance change phenomenon was first discovered in the 1960s by Hickmott [3]. In the following three decades several other workers contributed towards what we today classify as RRAM [4–10]. In the early stages resistance change memories were distinguished by their current–voltage characteristics as either voltage controlled negative resistance (VCNR) or current-controlled negative resistance (CCNR) [11, 12]. Although the potential of resistance-based memories was apparent from an early stage, actual integration and fine-tuning of materials properties was a barrier difficult to overcome.

Renewed interest in RRAM occurred towards early 2000 when universal memories were becoming the goal of research. Several candidates which could potentially be as fast as dynamic RAM (DRAM), while being non-volatile began to emerge. Several of these candidates such as phase change RAM (PRAM), magnetic RAM (MRAM), and ferroelectric RAM (FRAM) have been mentioned in other chapters of this book and elsewhere [13–15]. Of these new memories, RRAM had several advantages such as simple composition and low temperature process, a simple metal–insulator–metal (MIM) structure, in addition to being completely complementary metal–oxide–semiconductor (CMOS) process compatible [10, 16, 17]. Table 5.1 is the ITRS Roadmap comparison of new memories comparing fundamental memory metrics: resistance-based memory has superior Retention and Speed, while lacking endurance, and having high programming current [15, 16, 18–28].

NAND Flash memory density has increased so quickly (64 Gb MLC in 2008, Samsung) that it was impractical for new memories to compete directly. More recently RRAM research has become focused on advantages such as low temperature processes, stackable cell structures, and multilevel characteristics. The simple cell structure of RRAM allows for more complicated device structures to be fabricated using minimal additional processing. Figure 5.1 compares several memory candidates with current mass production NAND Flash memory, FRAM, and MRAM. RRAM demonstrates fast programming speeds with high density which can be achieved by stacking and MLC.

In the earliest stages of RRAM research in 2000, a major limitation was that the exact mechanism behind the resistance change was not clear. Although the previous works since the 1970s had investigated the phenomena [3, 11, 29], no satisfactory consensus regarding the mechanism had been reached. A major reason for the confusion and complications behind the mechanisms had to do with the variety of materials each having its own explanation. Today we are beginning to see more direct evidence of the mechanisms behind switching and making progress into the fundamental physics behind RRAM [2, 30–33].

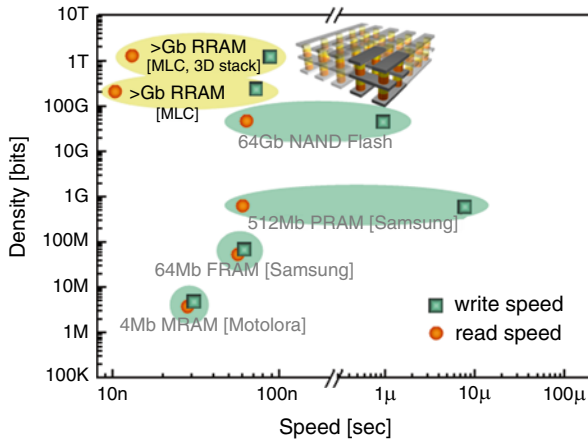
In order to give the reader an overview into the current state of RRAM research, this chapter will begin with a comparison and classification of RRAM materials and types. Next a discussion about the mechanism behind resistance change phenomenon



**Table 5.1** Comparison of resistance-based memory devices under development

	Phase change memory	Nanomechanical memory	Filament formation/rupture memory	Ionic memory	Electronic effects memory	Molecular memory
Storage mechanism	Reversibly changing amorphous and crystalline phases	Electrostatically controlled mechanical switch	Multiple mechanisms	Ion transport and redox reaction	Charge trapping Mott transition Schottky barrier effects	Multiple mechanisms
Cell elements	1T1R <sup>a</sup> or 1D1R <sup>b</sup>	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R
W/E time	50/120 ns [15]	3 ns [19]	5 ns/10 ns [21]	<50 ns [22]	100 ns [23]	0.2 s [26]
Feature size F (best projected)	65 nm (production)	5–10 nm	5–10 nm	5–10 nm	5–10 nm	5–10 nm
Cell area (best projected)	4.8F <sup>2</sup>	8/5F <sup>2</sup>	8/5F <sup>2</sup>	8/5F <sup>2</sup>	8/5F <sup>2</sup>	8/5F <sup>2</sup>
Retention time	>10 year	~days [20]	>1 year	>10 year	>1 year [24]	2 months [28]
Write cycles	1E8	>1E6 [20]	>1E6 [16]	>1E6 [22]	>1E3 [25]	>2E3 [27]

<sup>a</sup>1T1R: 1T1R resistor<sup>b</sup>1D1R: 1D1R resistor



**Fig. 5.1** Comparison of the cell operation speed versus memory density for NAND Flash, PRAM, FRAM, MRAM, and RRAM. Current RRAM materials show fast programming speeds on the order of 10 ns and have high density potential using MLC and 3D stack technology

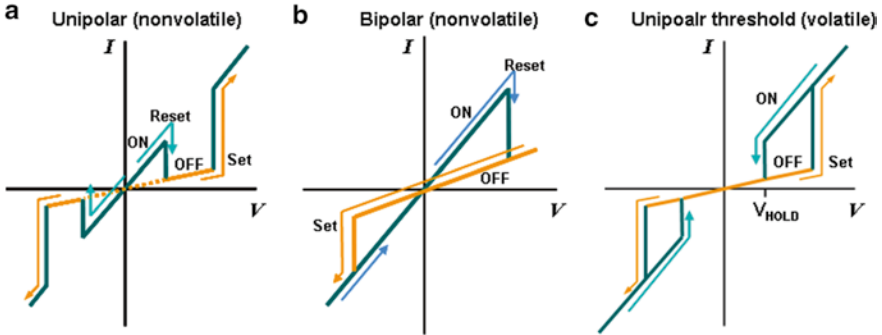
will be presented. In the second section, we will discuss more current works regarding cell stacking architecture, and RRAM scaling. Finally we discuss the outlook for RRAM and offer our views into what further works are still required.

## 5.2 Resistance Change in Oxide-Based Materials

### 5.2.1 Resistance Switching Properties

Depending on the current–voltage characteristics we can divide resistance change phenomena into three broad categories: unipolar, bipolar (also called electronic effect), and threshold switching. Unipolar and bipolar switching types are non-volatile in that even after removing the voltage the resistance values will remain at whichever state it is set to. In contrast threshold switching is volatile and requires a minimum voltage ( $V_{\text{hold}}$ ) to maintain the low resistance state. Figure 5.2 shows a comparison of the current–voltage switching characteristics.

As seen in Fig. 5.2a unipolar switching is called such because the cell can be operated at either positive or negative bias exclusively. For example, the voltage ( $V_{\text{set}}$ ) required to switch the cell to low resistance state (LRS) is positive just as the voltage ( $V_{\text{reset}}$ ) required to return the cell to the high resistance state (HRS) is also positive. In addition the switching curve is completely symmetric in that any operation which can occur with positive bias can also occur at negative bias. Finally, the order of applied bias polarity does not matter: positive or negative bias can be used to set (HRS  $\rightarrow$  LRS), and then a positive or negative bias can be used to reset (LRS  $\rightarrow$  HRS).



**Fig. 5.2** (a) Typical unipolar memory switching. Switching curve is symmetric: set and reset operations are performed at the same polarity (b) Typical bipolar memory switching. Asymmetric switching: the set and reset operation takes place in one polarity: negative bias for set in this case (c) Threshold switching, hysteresis shows the value of the minimum voltage ( $V_{\text{hold}}$ ) required to maintain the low resistance state

In contrast Fig. 5.2b shows the bipolar memory characteristic. In this example set occurs at negative bias while reset occurs at positive bias. In this case a voltage sweep (or pulse) of the same polarity as  $V_{\text{set}}$  will not reset the cell. Also even if the same type of electrode is used, for example Pt bottom and Pt top electrodes, set and reset operations can only be performed at their respective polarity. Finally Figure 5.2c shows threshold switching. Threshold switching occurs as unipolar and after reaching  $V_{\text{set}}$  the cell reaches the low resistance state. However upon lowering the voltage to below the minimum value of  $V_{\text{hold}}$ , the LRS is recovered.

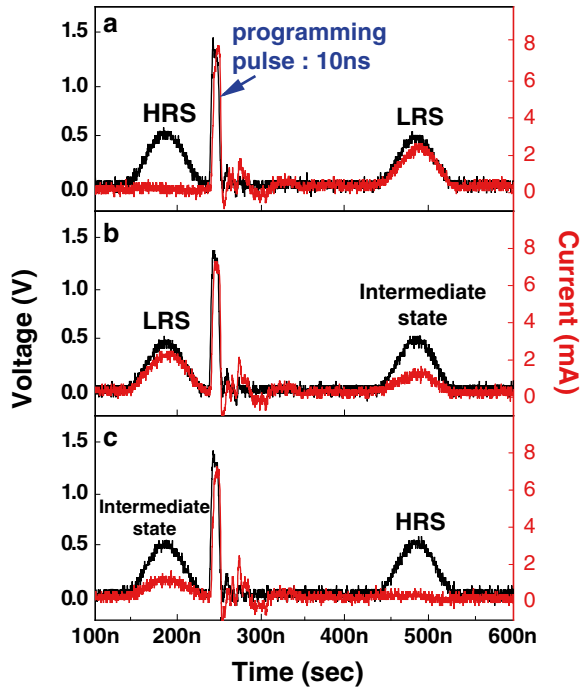
The three of these types of switching can be used to describe the majority of oxide-based resistance change materials. It is interesting to note that different types of switching can occur even in the same material depending on factors such as: electroforming [11], doping concentration [34], stoichiometry [10], and physical parameters [16]. Although this broad range of properties might seem to decrease the value of oxide-based memories for memory applications, in fact the flexibility of switching properties allows for all-oxide-based devices and applications which have several advantages over devices which might require different materials for respective components such as memory cell and switch.

## 5.2.2 Oxide-Based Resistance Memory Classifications

### 5.2.2.1 Binary Oxides

Of oxide-based resistance change materials, the simplest class we can consider are the binary transition metal oxides (TMO). Examples of materials are: NiO [2], TiO<sub>2</sub> [35], ZnO [36], CuO [37], VO<sub>2</sub> [38], Ta<sub>2</sub>O<sub>5</sub> [39], and HfO<sub>2</sub> [40]. The chemical composition

**Fig. 5.3** Pulse experiments showing bistable resistance switching for 10 ns pulse width. (a) Switching from HRS to LRS, (b) switching from LRS to an intermediate state, and (c) switching from an intermediate state to HRS. Switching from HRS to LRS is induced by a single 1.5 V pulse with 10 ns duration while switching from LRS to HRS is caused by a series of two identical pulses with 10 ns separation time. Reprinted with permission from [1]. Copyright 2008, Wiley InterScience



is made of a transition metal and oxygen. The stoichiometry and doping concentration can easily be varied during fabrication and leads to the widest array of properties for any given material. For example, by varying oxygen partial pressure during NiO deposition, it has been reported that the resistivity can be varied [10]. Due to the simple composition almost any deposition method can be used to fabricate TMOs. Some methods which have been reported include: Sputter, atomic layer deposition (ALD) [41], metallorganic chemical vapor deposition (MOCVD) [42], anodization [3], sol-gel [43], and thermal oxidation [44]. TMO thin films are usually fabricated as polycrystalline thin films leading to isotropic and uniform properties over the film. Although the chemical composition is rather simple a variety of crystal structures occur for TMOs: rock-salt (NiO), rutile or anatase ( $\text{TiO}_2$ ) [35], and even polycrystalline or amorphous structure (ZnO).

For resistance-change cells typically a metal–TMO–metal structure is used where the metals can be either the same or different. In the past, lateral structures have also been tested and shown to exhibit resistance switching. More recently lateral structures have been ignored in favor of vertical MIM structures which have more easily definable switching regions.

Figure 5.3 shows the impressive switching speeds in TMO based oxide memories. A Pt–NiO–Pt structure was fabricated and a pulse generator was used to test

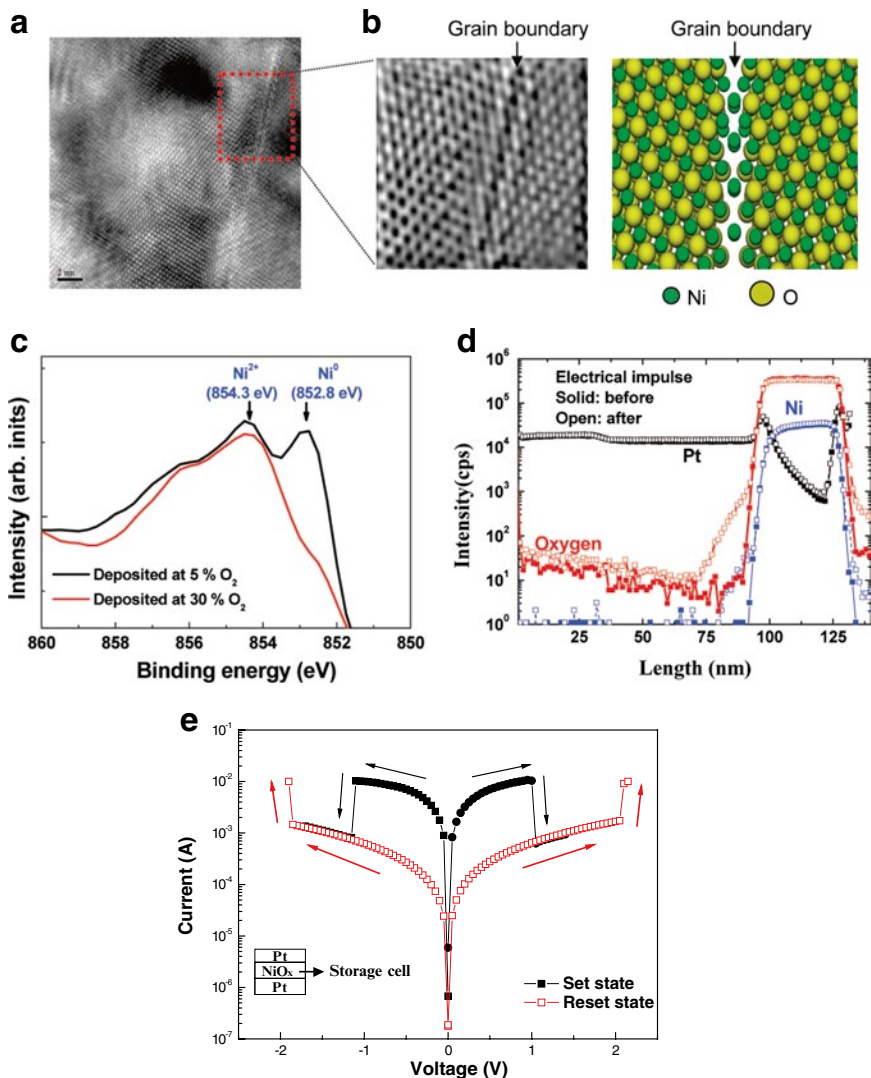
the minimum switching speed [1]. The switching speed was shown to be possible for pulse durations of 10 ns. The programmed state was confirmed by a read pulse of 0.3 V before and after application of respective set/reset pulses.

All three types of switching discussed in Sect. 5.2.1 occur in TMOs. A complete discussion of the mechanism behind resistance switching is too broad a subject for this chapter; however a few well-known cases are presented. Perhaps the easiest mechanism to understand is the conductive filament mechanism being used to explain switching in films such as NiO [45]. During resistance switching when  $V_{\text{set}}$  is applied across top and bottom electrodes, a path which is highly conductive (but not necessarily metallic) is formed through the film. Then a subsequent  $V_{\text{reset}}$  causes the disruption of these filaments. The mechanism behind reset is believed to be related to Joule heating [2].

Figure 5.4 shows transmission electron microscopy (TEM) images filament paths formed through a NiO thin film. In NiO we were able to observe changes only near the grain boundaries in this case. However current paths might also be formed within the NiO bulk, but were unobservable. Figure 5.4a shows the high-resolution transmission electron microscopy (HR-TEM) image of the polycrystalline NiO layers that show the electrical switching behavior. A highly ordered, stoichiometric structure can be seen in the TEM image of the grain interior. The grain-boundary region in the boxed area of Fig. 5.4a was further studied by the inverse fast Fourier transform (IFFT) TEM method as shown in the left-hand side (Fig. 5.4b). The electron energy-loss spectroscopy (EELS) spectrum at the grain boundary exhibits only a sharp nickel L<sub>2,3</sub> edge peak (854 eV) indicating that Ni becomes concentrated in this region after setting to low resistance state [46]. XPS data for two NiO samples deposited by reactive DC magnetron sputtering are compared in Fig. 5.4c. The most interesting feature in Fig. 5.4c is the coexistence of a metallic nickel peak, at 852.8 eV, and a NiO peak, at 854.3 eV, for NiO samples deposited at an O<sub>2</sub> partial pressure of 5 %, while the 30 % sample which does not show bistable resistance switching lacks these features. SIMS results in Fig. 5.4d show that the O atoms within the NiO layer diffuse out toward the platinum electrode after the electrical switching, indicating the nickel-rich condition in the NiO layer.

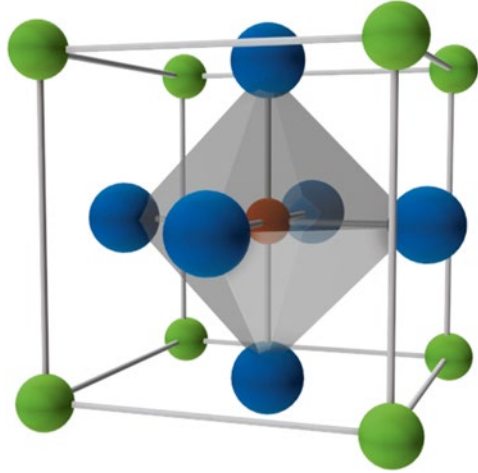
Metal–insulator–metal cells which follow the filament type unipolar mechanism are programmed as shown in Fig. 5.4e. In the pristine state the device begins in the high resistance state, and voltage sweep (or voltage pulse) of at least  $V_{\text{set}}$  is applied. In order to prevent electrical breakdown for electrical sweep measurements a current compliance value is used (10 mA in Fig. 5.4e). Subsequently, when the device is in the LRS, a second voltage sweep (or pulse) to  $V_{\text{reset}}$  will recover the device to the HRS. Reading of the states without affecting their values can be done at a voltage sufficiently smaller than  $V_{\text{reset}}$ . Also, in order to better understand the chaotic switching data distribution, Yoo et al. analyzed conducting filament paths of the oxide thin film by using statistical method [47].

Bipolar switching which occurs in TMO such as TiO<sub>2</sub> will be described more in detail in the next materials section as their behavior is similar to perovskites.



**Fig. 5.4** (a) High-resolution transmission electron microscopy (HR-TEM) image of the NiO layer, which shows the electrical switching behavior; crystalline order can be seen in the bulk of grains, and scale bar represents 2 nm. (b) *Left panel* shows an inverse fast Fourier transform (IFFT) transmission electron microscopy (TEM) image of the boxed area in panel (a), showing the grain-boundary region; the right side is a schematic drawing of the grain boundary in NiO, showing the location of the cations (*small spheres*) and anions (*large spheres*). Nickel nanofilament precipitates are present at the grain boundary. (c) X-ray photoelectron spectroscopy (XPS) analysis of NiO samples; the NiO sample that was deposited at an oxygen partial pressure of 5 % shows the coexistence of Ni (852.8 keV) and NiO (854.3 keV) peaks. (d) Secondary-ion mass spectroscopy (SIMS) data (for the 5 % oxygen partial pressure sample) showing the movement of O and Ni across the electrodes before and after electrical impulses. (e) Typical unipolar switching in Pt/NiO/Pt. Switching curve is symmetric: set and reset operations are performed at the same polarity. Reprinted with permission from [2]. Copyright 2009, ACS

**Fig. 5.5** Example of perovskite structure ( $\text{CaTiO}_3$ ). Small atom at center is  $\text{Ti}^{4+}$ , Atoms at cube edges are  $\text{Ca}^{2+}$  and Atoms at face centers are  $\text{O}^{2-}$

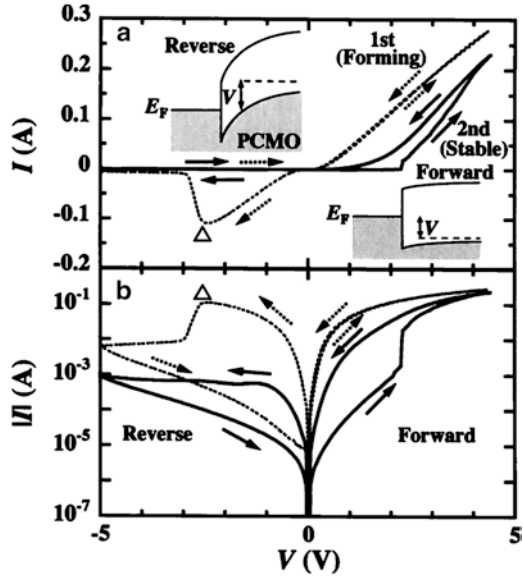


### 5.2.2.2 Perovskites

In the perovskite structure ( $\text{ABO}_3$ ), atoms A sit at cube corner positions  $(0, 0, 0)$ , B atoms sit at body center position  $(1/2, 1/2, 1/2)$ , and oxygen atoms sit at face centered positions  $(1/2, 1/2, 0)$  as shown in Fig. 5.5.

An undersized B cation can be slightly offset from the center due to strong electric fields. The resulting electric dipole is responsible for the property of ferroelectricity in perovskites such as Barium Titanate. Perovskites such as  $\text{SrZrO}_3$  [6],  $\text{Pr}_{0.7}\text{Ca}_{0.3}\text{MnO}_3$  [7],  $\text{LaCaMnO}$  [48],  $\text{SrTiO}_3$  [24] have demonstrated bistable resistance switching. Fabrication of perovskite oxides is more complex in comparison with transition metal oxides, and slight changes in the stoichiometry can lead to crystal distortions and unwanted effects [7]. The mechanism behind bipolar switching is attributed to three separate effects: Schottky barrier modulation by charge injection at the interface, reduction and modulation of oxygen ion at the interface, and charge trapping and detrapping at the vacancy sites. For most metal–oxide contacts there should be a formation of a metal–semiconductor Schottky barrier at the contact. Moreover bipolar resistance switching has never been reported for the case where both contacts to the oxide are purely ohmic [49]. At the metal–oxide interface trap states are formed as is usually the case [50]. When a bias is applied to the electrode, charge is injected by Schottky emission (electrode-limited), Pool–Frenkel emission (bulk limited), or Fowler–Nordheim tunneling at the high fields concentrated near the interface [51]. These injected charges can become trapped at defects such as vacancies, impurity, interstitials, or interfaces within the insulator. The trapped charges can effect the width and/or height of the electrostatic barrier at the metal–semiconductor junction modifying the resistance of the device [51]. For example in  $\text{Pr}_{0.7}\text{Ca}_{0.3}\text{MnO}_3$  (PCMO) and Nb doped  $\text{SrTiO}_3$  (Nb:STO) samples, it was shown that the density of oxygen vacancies near the interface was important to bistable resistance switching. Sawa et al. described the mechanism behind the

**Fig. 5.6**  $I$ - $V$  characteristics of a Ti/PCMO/SRO layered structure drawn in (a) linear and (b) semi-logarithmic current scales. Insets schematically show electronic band diagrams for a rectifying Ti/PCMO interface. Reprinted with permission from [49]. Copyright 2004, AIP



change in oxygen vacancies to be due to electrochemical migration of oxygen vacancies near the interface. While the complete role of oxygen vacancies in regard to bipolar switching is not fully understood, one explanation is that oxygen vacancies act as  $n$ -type donors in  $n$ -type oxides and acceptors in  $p$ -type oxides, the number of vacancies can effect the depletion layer width.

Figure 5.6 shows an example of bipolar resistance switching behavior in PCMO. Programming is done by voltage sweep to  $V_{\text{set}}$  in the direction of positive bias. Reset operation is performed with a voltage sweep to  $V_{\text{reset}}$  in the opposite direction (in Fig. 5.6). Read operation can be done with either positive or negative bias as long as the voltage is sufficiently lower than  $V_{\text{reset}}$  and  $V_{\text{set}}$ . The aforementioned charge injection and trapping mechanisms is modelled, showing how bistable resistance switching occurs.

In contrast to transition metal oxide materials, the electrodes on either side of perovskite based RRAM has been traditionally been different. Any type of electron conductor can be used in unipolar switching case of TMO, however modulation of a single barrier being easier than complexity involved with two barriers leads to different electrode selections. For example, Ohmic contact on one side, and Schottky contact on the other. Also the earliest reports for perovskite materials focused on high quality single crystal or epitaxial samples, leading to limitations during growth [6, 7]. We should note however currently bistable resistance switching has been shown for polycrystalline perovskite materials as well [52].

The Mott transition was reported for perovskite materials [53], the transition from weakly to strongly correlated electrons is used to explain the phenomenon in this case. The transitions are explained as occurring due to charge injection.

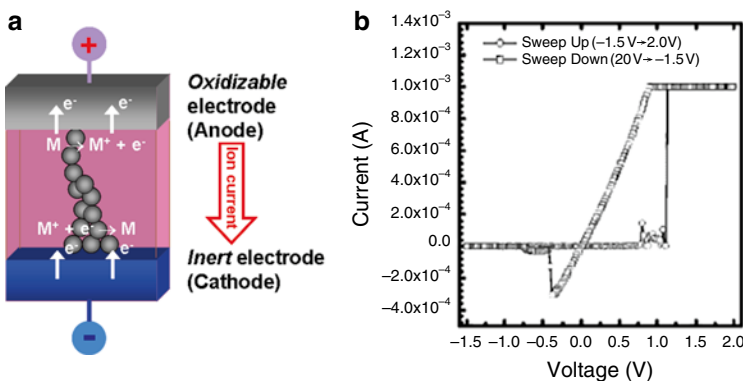


Ferroelectric polarization causes changes to the tunneling properties or the Schottky-type space-charge layer in adjacent semiconducting layers. The ferroelectric effect does not have any direct evidence to date and is mentioned here only for thoroughness.

### 5.2.2.3 Solid Electrolyte Based Materials

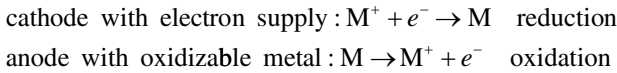
Another class of materials we will discuss are those based on solid electrolytes. Examples of materials of this class are primarily Ag and Cu-based in solid electrolyte systems [54, 55]. Oxides or Chalcogenides with a varying concentration of Ag or Cu are fabricated between one relatively inert electrode such as Pt or W and one electrochemically oxidizable electrode (Ag or Cu) which acts as a source and sink for mobile ions. Solid electrolyte based memories have also been called conductive bridging RAM (CBRAM), and programmable metallization cell (PMC) in the literature [55].

The current–voltage characteristics of ion based materials can be described as bipolar, that is set and reset operations occur at opposite polarities. However the mechanism behind resistance switching is different from previously mentioned bipolar memories. In this case the insulating matrix should exhibit ionic conductivity, applying a bias across the electrodes the conductive ions can migrate through the insulating matrix until a metallic filament path is formed through physical movement of ions. A schematic of the filament formation is shown in Fig. 5.7a. By applying a negative bias to the inert electrode, ions from the oxidizable electrode and within the electrolyte begin to form a filament path as they are reduced by electrons from the inert electrode. By applying high fields in the opposite direction the formed filament can be oxidized and broken again through ionic conduction.



**Fig. 5.7** (a) Schematic of formation of filament path in ion based memory cell. (b) A typical current–voltage plot for one cycle in a 0.5  $\mu\text{m}$  diameter PMC device with a 200 nm thick silver-rich  $\text{Ge}_{45}\text{Te}_{55}\text{N}$  (30 %) solid electrolyte using a 1 mA current limit. Reprinted with permission from [56]. Copyright 2006, The Electrochemical Society

The reactions taking place during oxidation and reduction are as follows:



where  $M^+$  is mobile ion, and  $e^-$  is electron.

In most cases an initial formation process is required before normal set/reset operations. The current and voltage levels during operation are typically much smaller ( $\sim 10\times$ – $100\times$ ) than other resistance-based memories. Figure 5.7b demonstrates operation of ionic memory cell, the set voltage is  $\sim 1$  V, the reset voltage is  $\sim 0.3$  V, and the maximum current value is  $\sim 1$  mA. The speed of the device is limited by ionic transport across the electrolyte layer, for very thin layers ( $< 10$  nm) the switching speed can be as low as a few tens of nanoseconds for Ag doped Ge–Se electrolytes system, which exhibit high ion mobility [55].

#### 5.2.2.4 Summary

So far we have discussed just a few possible mechanisms and materials which show bistable resistance switching. Resistance switching seems almost universal across not only oxide materials but also polymers [57], molecules [26], and even carbon nanotubes [58]. The mechanism behind each is as varied as the type of materials. Unfortunately in most cases the switching mechanisms are still unclear although the switching phenomenon has been clearly observed. In spite of several models including band bending by charge trapping, conducting filament formation/rupture by Joule heating, and the change in the oxidation state of the cations, having been suggested clear experimental proof has been difficult to show.

Figure 5.8 shows the “family tree” for resistance-based memories including materials and shows where oxide-based memories mentioned fit into the bigger picture. Due to the scaling limit of conventional charge-based memory, non-charge-based memory such as resistance-based non-volatile memories have been proposed. However, the technology is not yet sufficient for application.

### 5.3 Oxide RRAM Based Materials and Applications

#### 5.3.1 RRAM Scaling

The minimum cell size for resistance switching has not yet been shown, and theoretical models have predicted that resistance switching should occur down to nearly the molecular size [2]. Figure 5.9 shows cell size vs the input switching power (left y-axis) LRS to HRS (calculated as  $I_{\text{off}} \times V_{\text{off}}$ ) in the NiO sample. Corresponding switching time is shown in the same figure (right y-axis). Evidence shows that fewer and/or thinner filaments were formed at smaller cell sizes. The reduction in switching

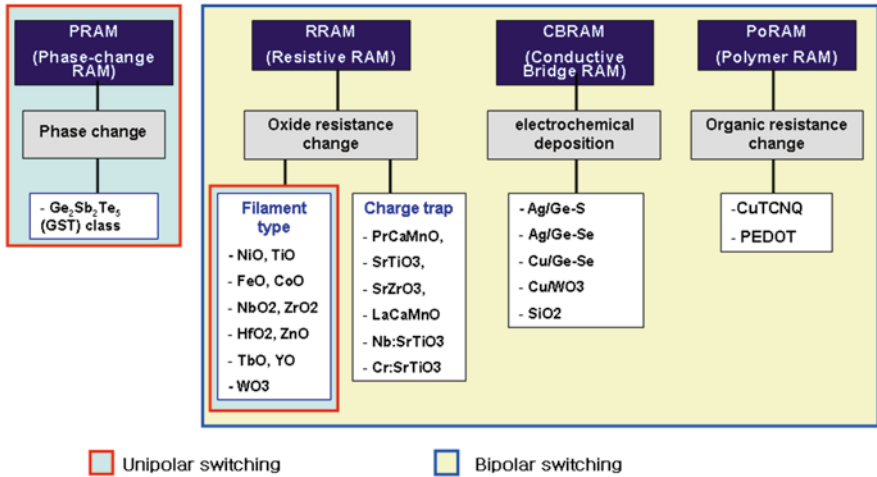


Fig. 5.8 Resistance change materials as switching mechanism

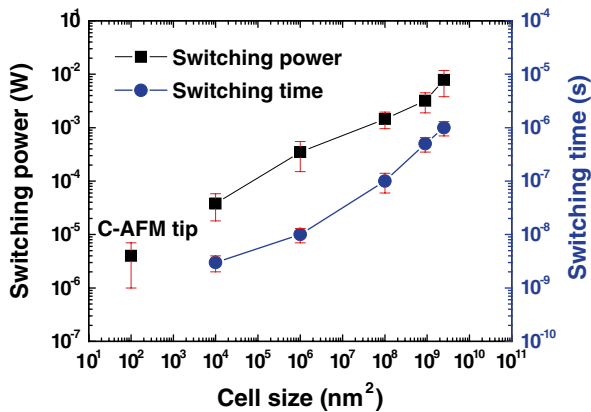
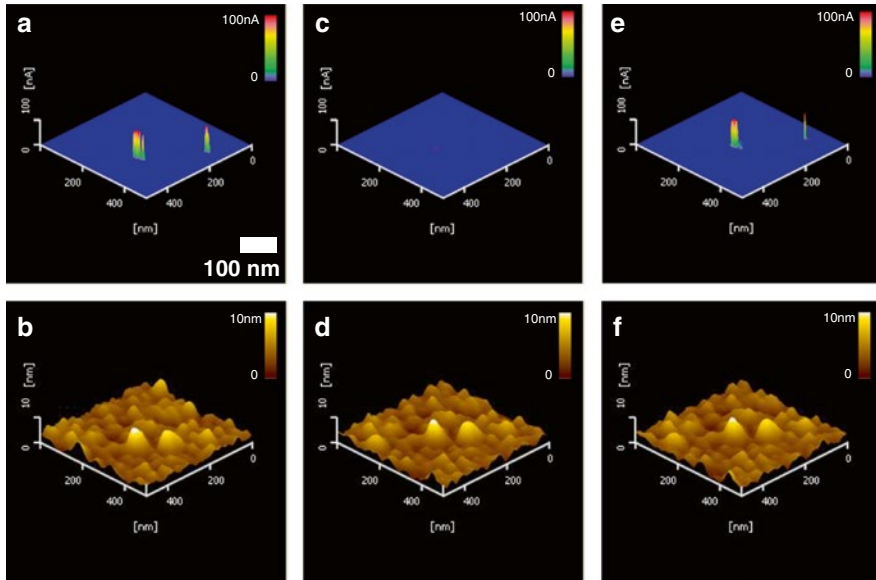


Fig. 5.9 Switching speed and input power by cell size. Cell size versus switching power and speed: power is calculated based on measurements from the LRS state to the HRS state by taking the product of maximum current and applied voltage. The error bar at each node size is determined by the standard deviation of 5–10 successive measurements. The vertical error bars are experimental uncertainties that are due to the distribution of the switching operation. An additional data point for the current-sensing atomic force microscopy (CS-AFM) results is shown at  $10 \times 10 \text{ nm}^2$ . Reprinted with permission from [2]. Copyright 2009, ACS

time is not accounted for by the decrease in the number of filaments alone; since they should rupture individually and switching time should be independent of cell size. It is reasonable that the resistivity of the filaments may be different in this case depending on cell size. Along with the fact that switching times begin to saturate as cell size decreases below  $10 \times 10 \text{ nm}^2$  we can explain this based on the thermal energies. The migration barrier of an oxygen atom has been calculated to have activation energies of 2–3 eV, depending on the charge states of the oxygen vacancy, for diffusion via vacancy mechanism.



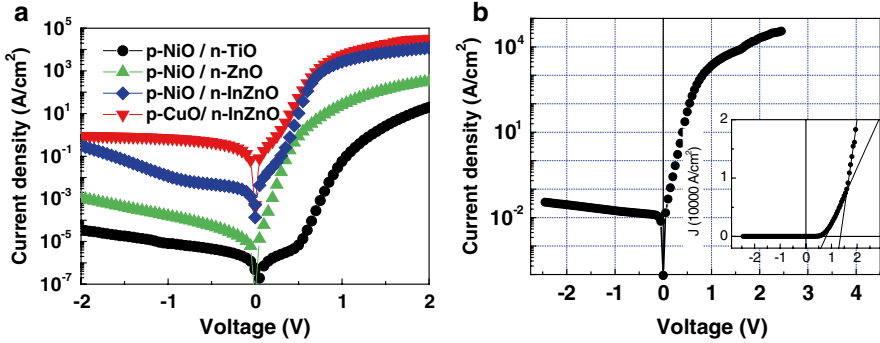
**Fig. 5.10** Nanoscale switching current paths in NiO (a) Low resistance state (c) High resistance state (e) Low resistance state CS-AFM (*top*) and the corresponding topographical AFM images (*bottom*) of cell in the LRS and HRS states. (Control over the formation and destruction of nanofilament current paths is done by biasing the CS-AFM tip).  $R_{on}$  was switched by a CS-AFM scan with a 2.3 V bias [i.e., “SET” scan; (a) and (b)];  $R_{off}$  was switched by a scan with a 1.5 V bias [i.e., “RESET” scan; (c) and (d)]; and  $R_{on}$  switched back again with 2.3 V (e, f). The local current images of both  $R_{on}$  and  $R_{off}$  were acquired with a bias of 0.05 V through the tip [59]. Reprinted with permission from [59]. Copyright 2007, Phys. Status Solidi (RRL)

Therefore during the time scale for device operations the thermal energy is critical for electromigration. Joule heating is thought to be the largest contributor to the thermal energy. Because the power scales with node area, the local temperatures are greater in smaller cell sizes and leads to the observed saturation in switching times.

Furthermore by using a conductive atomic force microscopy (AFM) tip, filamentary paths across NiO could be directly measured. Figure 5.10 shows the results of the experiment going from low resistance to high resistance then back to low resistance states [59]. The size of these paths was measured to be around 10 nm, however this is the same as the size of the AFM tip used in this cases, and even smaller filament paths should form. The conclusion so far has been that as far as scaling goes, bistable resistance switching should reach the limits of just a few unit cells.

### 5.3.2 Oxide-Based Switches for RRAM

Before going further into RRAM applications or structures, an important aspect of oxide-based RRAM are switch elements. Traditional DRAM uses a transistor to select the program cell and a capacitor to store the state (1T–1C). While continuing



**Fig. 5.11** (a) The difference in forward current density for some different oxide material combinations. (b) Current density versus applied voltage curve of Pt/CuO/IZO/Pt in semi-logarithmic scale. The *inset* is depicted in linear scale. *Lines* are guides to the eyes. Reprinted with permission from (b) [60], copyright 2008, Wiley InterScience

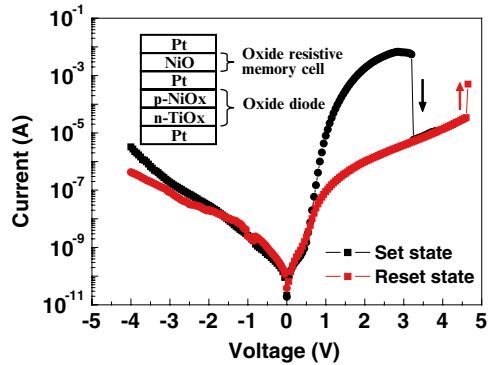
development towards oxide-based memories it becomes interesting to consider alternative to a traditional transistor-based switch element. In particular two switch elements which are composed to transitional metal oxides: The oxide  $p$ - $n$  diode and threshold switch are discussed.

For use as a type of switch, oxide semiconductors can be made as both  $p$ - (NiO, CuO) and  $n$ -type (ZnO, TiO<sub>2</sub>), and can further be combined into an oxide  $p$ - $n$  heterojunction diode. In contrast to traditional Si diodes, oxide diodes can be fabricated as polycrystalline material with high current density. In addition typical processing temperatures are on the order of 500 °C compared to high temperature processes (~1,000 °C) required in Si. Currently an oxide diode combination which boasts both high rectifying ratio and current density is required. However initial feasibility studies of the diode and bistable resistance element (1Diode–1Resistor) have been reported [10]. For oxide-based diodes, it was experimentally shown that reducing the bandgap for both  $p$ - and  $n$ -type materials leads to increased forward current densities as shown in Fig. 5.11a. In case of  $p$ -CuO/ $n$ -IZO the current density under forward bias was about  $3.5 \times 10^4$  A/cm<sup>2</sup> which is the highest reported record for oxide thin film diodes to the best of our knowledge. The rectifying characteristics of oxide  $pn$  diode are clearly shown in Fig. 5.11b.

A structure similar to this was connected in series with resistance switching element and shown to flow enough current to access the storage element (NiO) while the diode was under forward bias, and conversely deny access while under reverse bias [10]. Figure 5.12 shows the combined  $I$ - $V$  characteristics and structure of the tested device.

As a second type of switch one possible form resistance switching can be exhibited in oxide materials is threshold switching characteristics. That is past a certain threshold voltage ( $V_{th}$ ) the resistance value of the device decreases dramatically, and can be held in that state above a certain hold voltage. By combining a threshold element in series with a unipolar or bipolar switching element, a switch and storage unit can be used to address and store bits in an array. Threshold devices are easily

**Fig. 5.12**  $I$ - $V$  characteristics of a combined Pt/NiO/Pt/ $p$ -NiO $_x$ / $n$ -TiO $_x$ /Pt structure, namely, 1Diode/1Resistor structure, a schematic diagram of which is shown in the inset. Reprinted with permission from [10] Copyright 2007, Wiley InterScience

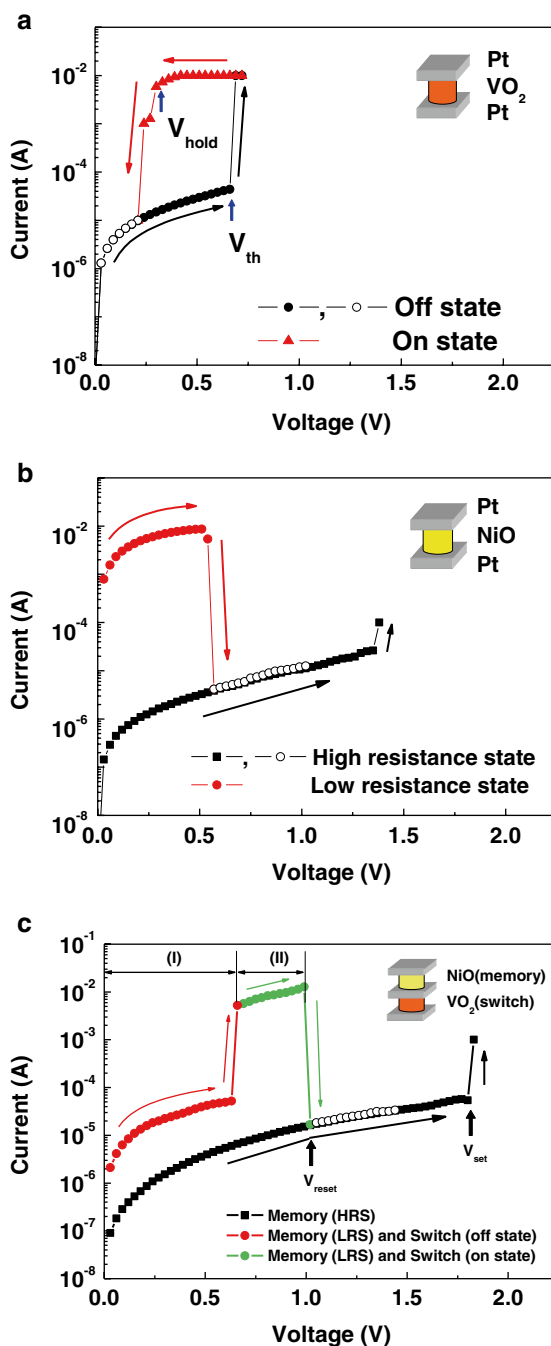


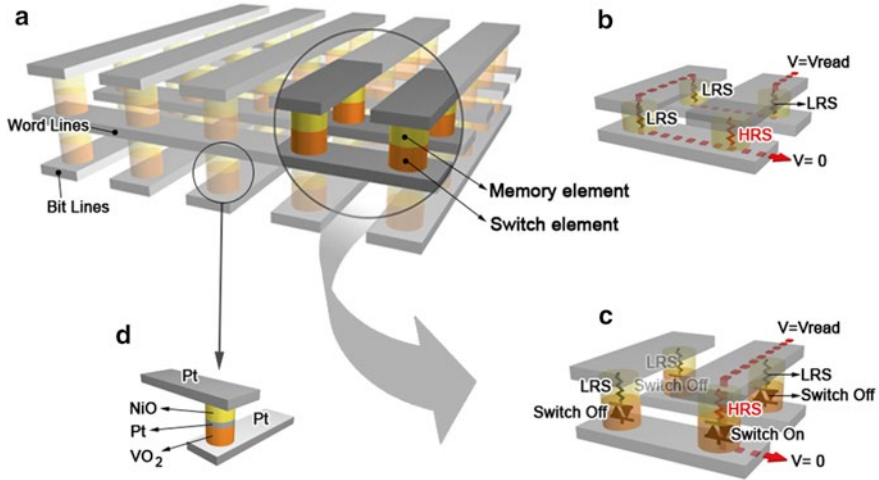
fabricated using processes used for the storage element as well. For example, depositing NiO at high oxygen partial pressures leads to threshold switching behavior [8]. Other examples of threshold switching oxides are: VO<sub>2</sub> and chalcogenide-glass thin films [12]. Advantages that threshold devices have over transistors or diodes are much higher current densities, and being composed of a single layer rather than a  $p$ - $n$  junction.

Experimental results showing the feasibility of a combined memory and threshold switching device are shown in Fig. 5.13 [61]. The memory switching element (NiO deposited at 5 % oxygen partial pressure) is tested first, and operation can be seen in Fig. 5.13a. Next the threshold switching element (VO<sub>2</sub> deposited at 20 % oxygen partial pressure) operation is shown in Fig. 5.13b. Finally the combined device operation is shown in Fig. 5.13c. Fig. 5.12 clearly indicates both the bistable switching characteristics of the NiO memory element and the threshold switching characteristics of the VO<sub>2</sub> switch element. Up to the threshold voltage the cell is inactive since the switch element is in the off state. Past the threshold voltage the cell is active since the switch element is in the on state and the stored information can be read by applying an appropriate reading voltage just above the threshold voltage. By applying a writing voltage comparable to  $V_{\text{set}}$  or  $V_{\text{reset}}$ , the cell can be accessed and programmed since both are higher than the threshold voltage. Additionally we can access a single cell exclusively by applying read or write voltage to that cell while applying a voltage less than the threshold voltage to all the other cells.

Both threshold switch and oxide diodes are advantageous for cross-point structures which can theoretically achieve the cell sizes of  $4F^2$  ( $F$ : feature size used for patterning the cell). Additionally since the underlying film is not a major limitation and fabrication can be performed at low temperature stacking of several cross-point structures becomes possible. Figure 5.14a demonstrates a three-dimensional stacked structure using either threshold or oxide switch elements [61]. All fabrication steps can be performed using conventional semiconductor processing technologies available today and materials research such as increasing forward current density in oxide diode materials, and improving cell to cell  $V_{\text{set}}$  distribution in threshold switch and memory elements is the most important issue. The switch elements allow for

**Fig. 5.13** (a) Threshold switching of a Pt/VO/Pt switch element and (b) Bistable resistance switching demonstrated for a Pt/NiO/Pt memory element where NiO film was deposited at 5 % oxygen partial pressure. (c) Programming characteristics of combined oxide switch and oxide memory elements. The figure clearly indicates both the bistable switching characteristics of the Pt/NiO/Pt memory element and the threshold switching characteristics of the Pt/VO<sub>2</sub>/Pt switch element. In region (I), the cell is inactive since the switch element is in the off state. In region (II), the cell is activated since the switch element is in the on state and the stored information can be read by applying an appropriate reading voltage in that region. By applying a writing voltage comparable to  $V_{set}$  or  $V_{reset}$ , the cell can be accessed and programmed since both are higher than  $V_{th}$ . Therefore, we can access a single cell exclusively by applying read or write voltage to that cell while applying a voltage belonging to region (I) to all the other cells. Reprinted with permission from [61]. Copyright 2007, Wiley InterScience





**Fig. 5.14** (a) Generalized cross bar memory structure whose one bit cell of the array consists of a memory element and a switch element between conductive lines on top (word line) and bottom (bit line). (b) Reading interference in an array consisting of  $2 \times 2$  cells without switch elements. (c) Rectified reading operation in an array consisting of  $2 \times 2$  cells with switch elements. (d) Detailed structure of a single cell consisting of a Pt/NiO/Pt memory element and a Pt/VO<sub>2</sub>/Pt switch element. Reprinted with permission from [61]. Copyright 2007, Wiley InterScience

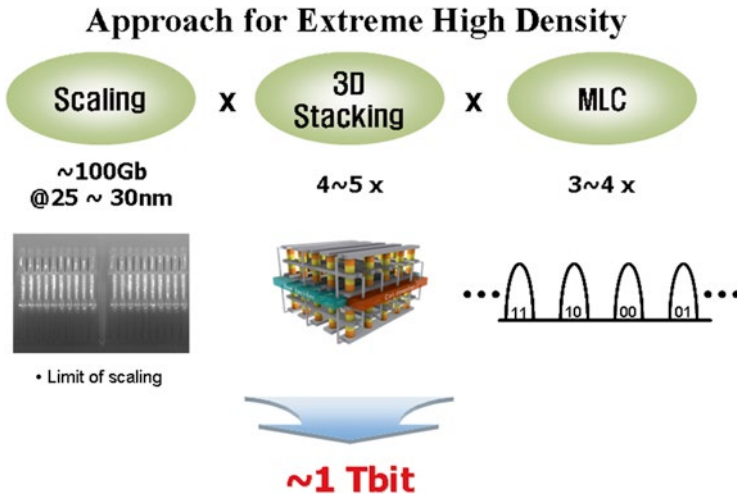
random access to memory cells while preventing reading interference between neighboring cells. Figure 5.14b demonstrates a typical reading error which might occur without switching elements present due to current following path of least resistance. Finally by adding the switching element we can see how the reading errors can be corrected.

### 5.3.3 RRAM State of the Art

In order to reach extreme high density such as terabit era, not only will we need to scale down, but apply current flash technologies such as MLC and 3D cell stacking technologies. Figure 5.15 demonstrates the requirements for reaching these densities: current planar scaling works down to 20–30 nm and can achieve 100 Gb densities, having 3–4 bits per cell using MLC technology, and 4 to 5 stacked cell layers we can achieve approximately 1 Tb. However all these technologies must be incorporated into the final product, and the integration will not be trivial.

First considering the stacking requirement of 4–5 layers, one limitation which isn't immediately apparent is the area which peripheral circuits will consume on the chip. Figure 5.16a shows the stacking possible with Si based peripheral circuits. However by using an all-oxide based memory GaInZnO (GIZO) transistors can also be stacked three-dimensionally improving the use of expensive Si real estate. Figure 5.16b demonstrates how an idealized peripheral circuit structure can be stacked. In Fig. 5.16c a comparison is made between the required areas for both





**Fig. 5.15** Requirements of technologies required to reach extremely high density memories

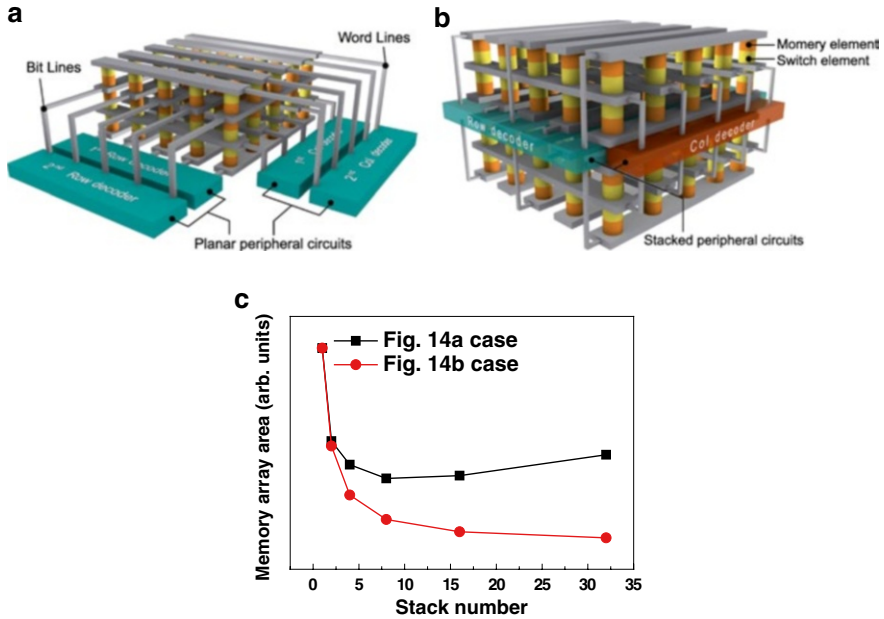
types of structures, at ~4 stacks the area requirements for stacking begins to outweigh the benefits in a conventional Si peripheral circuit structure.

GIZO transistors in conjunction with RRAM cells have been tested and shown to be feasible, leading to even further advantages for all-oxide based memories. Figure 5.17a shows a schematic diagram of a combined GIZO select transistor with 1D–1R structure. The GIZO transistor is gated to 5 V and the saturation region during programming and full operation of the 1D–1R device can be seen in Fig. 5.17b. With the GIZO transistor gated at 1 V read operations is possible however, the current is insufficient to switch the state to of the 1D–1R device from low resistance to high resistance. Finally when the select transistor is not gated, there is only minimal leakage current.

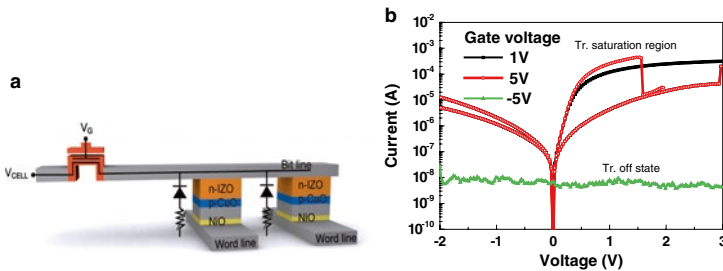
Second, the scalability of 1D–1R devices should be investigated further. Below in Fig. 5.18 a 1D–1R device using selective epitaxial growth (SEG) of Si was used to test RRAM cell sizes of 50 nm over Si SEG diodes. As mentioned previously for 50 nm oxide diodes to become a reality research towards high forward current density materials is needed.

### 5.3.4 Summary

As described so far, several pieces required for extreme high density oxide-based resistance memories are already in place. Stacked one time programmable (OTP) memory is already being sold by Sandisk Corporation. Theoretically oxide-based memories can already be used to replace traditional Stacked OTP memories. Similarly the structure of stacked OTP memory can be easily fabricated using



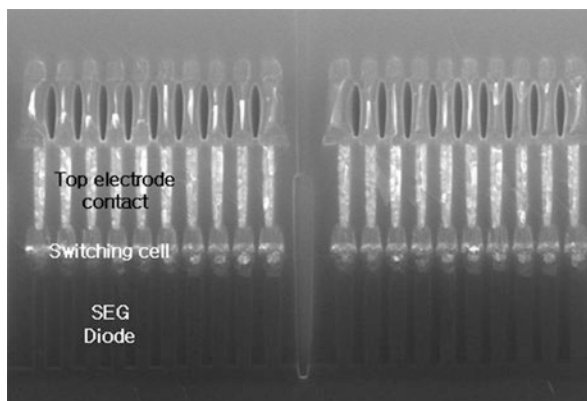
**Fig. 5.16** (a) Diagram of currently proposed structure for stacked memories with peripheral circuit. (b) Conceptual diagram for ideal stacking structure utilizing stackable peripheral circuits. (c) Comparison of overall memory array area as a function of the number of stacks in planar structure and stacked structure. Planar structure shows diminishing returns and eventual increase at ~4 stacks. Reprinted with permission from [62]. Copyright 2009, Wiley InterScience



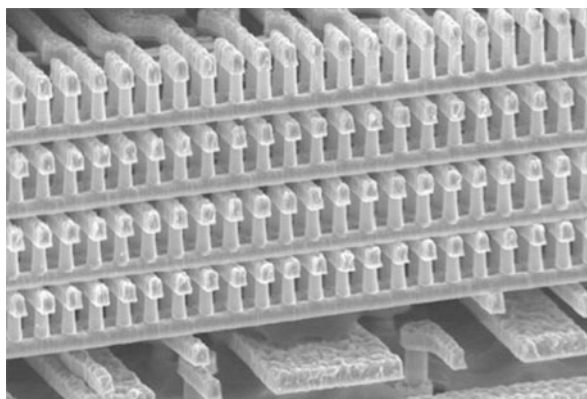
**Fig. 5.17** (a) Schematic diagram of two 1D-1R cells connected to a GIZO select transistor. (b) Operation of a 1D-1R cell with a select transistor biased to off and on in both a saturation and in a linear regime. Reprinted with permission from [62]. Copyright 2009, Wiley InterScience

all-oxide materials as well. Figure 5.19 shows scanning electron microscope (SEM) cross section of stacked OTP memories, we should notice that there are no major limitations in the materials, or techniques, or processes discussed for oxide memory. Moreover low processing temperatures in oxide materials should allow for even more flexible device design.

**Fig. 5.18** Partial SEM image of the selective epitaxial growth (SEG) Si diode and resistance change memory array. 1D–1R array was fabricated using SEG diode for switch and NiO for storage



**Fig. 5.19** Four layers of a cross-point diode memory array with tungsten bit and word lines in a 3D memory. Reprinted with permission from [63]. Copyright 2006, The Electrochemical Society



## 5.4 Outlook and Future of RRAM

The critical issues for the future development of RRAM devices are reliability, such as data retention and memory endurance (the number of erase and program cycles), and the characteristic variation from cell to cell and from chip to chip. In silicon most of these issues arise due to defects, impurities, or contamination. However in oxide-based devices variations in device characteristics seem almost intrinsic.

First by a more thorough study of behind the switching mechanisms an improvement in the reliability and predictability of oxide-based memories is required. Only then can we successfully design simulation and modeling tools and needed to design and test high density memory chips. Having been the subject of three decades of research still with no clear answer, this will obviously not be an easy task. On the bright side, experimental results have shown that oxide-based memories offer excellent scalability showing bistable resistance switching behavior down to just a few unit cells.

Second, a detailed look into the exact metal–insulator–metal structures and 1D–1R structure needs to be performed. Currently, most research is done with MIM cells combined in series with a switch element connected by a metal layer. However, during integration this structure (MIM-*p*-type semiconductor -*n*-type semiconductor–metal) is unwieldy. Initial steps towards improving the structure should be focused on eliminating the connecting metal layer. The final goal should be the discovery of a material which with a change in doping type, or stoichiometry can have the functions of both switch and storage elements.

Finally a method of controlling the electrical switching down to just a few atoms is needed. The author does not suggest to know the answer to how this can be possible, however by being able to control the exact type and degree of resistance switching previously unobtainable devices such as memristors become possible. By not being confined to be either “0” or “1,” but being able to achieve a continuous number of resistance values more flexible device designs and circuit designs become possible.

### 5.4.1 Conclusion

This chapter has focused on introducing the past few years research being done in oxide-based resistance memories. Renewed interest over the past few years has led to several new results and ideas based on oxide materials. While previous results have given new hope for the future, realization of oxide-based resistance memories still requires much fundamental research. In particular the mechanisms behind switching need to be improved, and a unified model for threshold and bistable resistance switching is needed. Also a more quantitative description of the roles of defects and impurities is required. Both transition metal oxides and perovskites offer their own distinct advantages and it is not clear which material type or which switching type is superior at this time.

The different types of oxide materials, and switching phenomenon observed so far have allowed for interesting device applications, however materials research is the key issue for finally achieving mass producible memory. Terabit memory seems possible if certain key breakthroughs can be made: improvement of cell-to-cell programming variation, scaling issues down to 20 nm, oxide diode forward current density, and multilevel cell programming.

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# Chapter 6

## Oxide Based Memristive Nanodevices

J. Joshua Yang and Gilberto Medeiros-Ribeiro

Transition metal oxide thin films play an indispensable role in nanoelectronic and nanoionic devices [1–3] proposed for the next generation non-volatile memory [4–14], neuromorphic computing [15], stateful logic [16] and hybrid CMOS–Memristor circuits [17]. The promise of metal oxide thin films comes from their wide range of electrical properties, ranging from insulating, semiconducting, metallic to even superconducting behavior [3] with exquisite dependence on the doping level. A trace level of compositional change in oxides induces a large amount of defects, which serve as native dopants in the oxide films and dramatically change their conductance [18]. Microscopically in a thin film device, the slight compositional change is in the embodiment of ionic motion, which gives rise to memristive switching under an electric field [19–21].

In this chapter, we will first discuss the memristive switching mechanism and a family of nanodevices based on this mechanism, and then describe the electroforming mechanism and finally how to engineer the device properties during fabrication.

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## 6.1 Section 1: Switching mechanism

### 6.1.1 Introduction

Existing materials and technologies in the semiconductor industry are approaching their physical limits, and technology breakthroughs in materials and device concepts are required as device sizes continuously decrease [22]. Developing nanoscale memory-bit cells [4, 23] for non-volatile random access memory (NVRAM) is one key technological requirement to extend the functional equivalent of Moore's law [24] for Boolean computing. Ultra-high density analog resistive memory cells (RRAM) may also enable a new era of non-Boolean neuromorphic computing [25, 26]. Metal oxides have attracted significant attention as the insulating layer in metal-insulator-metal crosspoint cells for RRAMs and NVRAMs [27] because of their wide range of electrical properties—most are wide bandgap semiconductors susceptible to doping by a variety of defects and impurities. Many are intrinsically “self-doped” by native interstitial or vacancy point defects. Consequently, engineering metal oxide based resistive switches is still in its infancy. The mechanisms for switching, for example, have created an intense debate in the literature. Different models have been suggested, including alteration of the bulk insulator resistivity by defects or trapped carriers [28–36], modification of the metal-insulator interface resistivity by defects or trapped carriers [37–43] or the formation of localized metal-atom chains that bridge the electrode materials under an electric field [44, 45]. Indeed, several different mechanisms may co-exist, and different mechanisms could be dominant in different materials systems. This uncertainty is exacerbated by the great difficulty in characterizing the physical changes responsible for the electrical switching, since the active regions of the devices are extremely small and buried under a metal contact. Therefore, even though nanoscale metal/oxide/metal switches have the potential to transform the market for non-volatile memory as well as provide disruptive synapse-like devices for neuromorphic computing, research progress has been hindered for years in part by the difficulty in developing a unifying formalism containing coupled electronic and ionic phenomena that dominate such nanoscale oxide devices. An analytic theory of “memristor” (short for memory-resistor) behavior was first predicted from fundamental symmetry arguments in 1971 [20] but has only recently been shown to naturally explain such coupled electron-ion dynamics, yet in a semi-quantitative fashion [19].

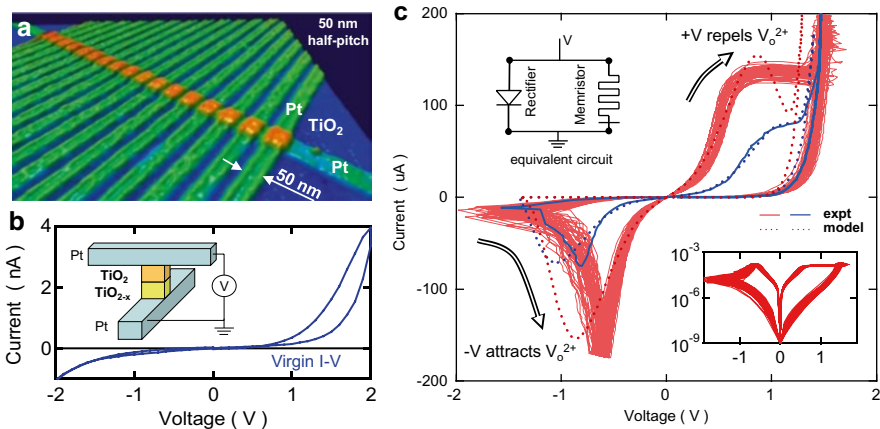
Here we provide experimental evidence to support this general model of memristive electrical switching in these systems. Micro- and nano-scale titanium dioxide ( $\text{TiO}_2$ ) junction devices have been built with Pt electrodes that exhibit fast bipolar non-volatile switching. We will demonstrate that switching involves changes to the electronic barrier at the Pt/ $\text{TiO}_2$  interface due to the drift of positively charged oxygen vacancies under an applied electric field. Vacancy drift towards the interface creates conducting channels that shunt, or “short-circuit,” the electronic barrier to switch ON. Vacancy drift away from the interface annihilates such channels, recovering the electronic barrier to switch OFF. Using this model we have built  $\text{TiO}_2$  crosspoints with engineered oxygen vacancy profiles that predictively control the switching polarity and conductance. We manipulate and ultimately engineer the



device structure to reveal that the mechanism for  $\text{TiO}_2$  switching is the shunting and recovery of the metal/oxide interfacial electronic barrier caused by the localized drift of oxygen vacancies.

### 6.1.2 Experiment

The Pt and Ti metal layers were deposited by electron-beam evaporation at room temperature. The Ti dioxide films were fabricated by either sputter-deposition or atomic layer deposition (ALD) methods. The  $\text{TiO}_2$  layer used for the junctions shown in Fig. 6.1 was 50 nm thick and was deposited by sputtering from a  $\text{TiO}_2$  target with 3 mTorr Ar and 250 °C substrate temperature. The  $\text{TiO}_2$  (15 nm)/ $\text{TiO}_{2-x}$  (15 nm) bi-layer films used for the junctions shown in Fig. 6.4 were synthesized by ALD at 200 °C with an additional in-situ annealing in an  $\text{N}_2$  environment at 300 °C. The annealing process was carried out following the first 15 nm deposition to create

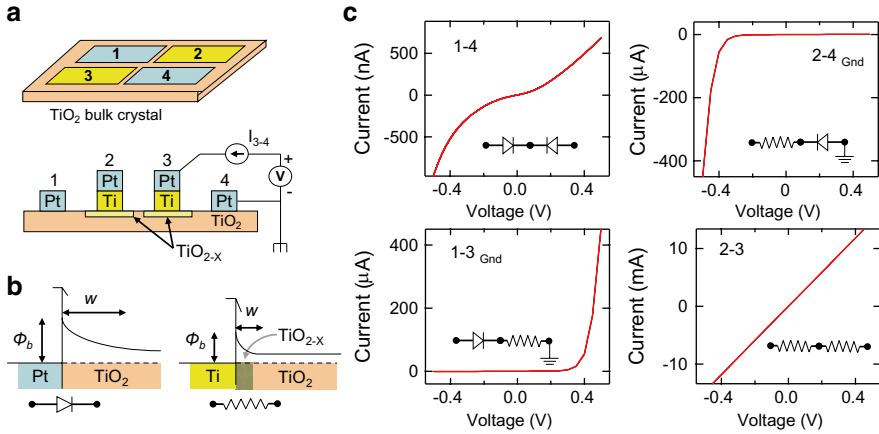


**Fig. 6.1** Bipolar reversible and non-volatile switching of nanoscale  $\text{TiO}_{2-x}$  devices. **(a)** An AFM image of  $1 \times 17$  nano-crosspoint devices with 50 nm half-pitch. Pt nanowires fabricated by nano-imprint lithography sandwich a 50 nm thick  $\text{TiO}_2$  insulating thin film. **(b)** The initial  $I$ - $V$  curve of the device in its virgin (pre-switching) state exhibits a rectifying characteristic. (*inset*) The 50 nm  $\text{TiO}_2$  actually has two constituent layers; a  $\text{TiO}_2$  layer rests on top of a  $\text{TiO}_{2-x}$  layer (see text). All electrical voltages were applied with the lower nanowire electrode grounded. **(c)** Experimental (*solid*) and modeled (*dotted*) switching  $I$ - $V$  curves are 50 experimental switching loops traversed as figure-of-eights that show a high degree of repeatability. The *solid* curve with a lower current level is an experimental switch loop that demonstrates the multiple resistive states of the device. The  $I$ - $V$  trace of the device in the ON state exhibits a symmetric “sinh-like” curve while the OFF state shows an asymmetric rectifying curve similar to the virgin state. (*inset*) The log scale switching  $I$ - $V$  curves show a  $\sim 10^3$  ON/OFF conductance ratio. An equivalent circuit model (*inset*) consists of a rectifier in parallel with a memristor. The memristor symbol is modified here with a bar to indicate its polarity: a positive bias applied to the end of the memristor with the bar switches it ON, i.e. with this bias polarity the resistance of the memristor decreases. This memristor+rectifier circuit model, implemented as (Eq. 6.1), yields the *dotted lines* (Macmillan Publishers Limited)

oxygen vacancies in the lower half of the  $\text{TiO}_2$  film, or was carried out following the full 30 nm deposition to create oxygen vacancies in the upper half of the  $\text{TiO}_2$  film. Titanium (IV) isopropoxide precursor was used with water as the oxidizing agent for the ALD  $\text{TiO}_2$  films. A variety of physical characterizations have been carried out on the Ti dioxide single crystal and thin films, including infra-red spectroscopy, Raman spectroscopy, X-ray diffraction, Rutherford backscattering spectroscopy, depth profiled X-ray photoelectron spectroscopy, ultra-violet visible absorption spectroscopy, and electrical Hall Effect measurements [46]. The Ti (1.5 nm adhesion layer)+Pt (8 nm) electrode used for the 50 nm $\times$ 50 nm nano-junctions shown in Fig. 6.1 was patterned by ultraviolet-nanoimprint lithography. The Ti (5 nm adhesion layer)+Pt (15 nm) electrode used for the micro-junctions (5  $\mu\text{m}\times$ 50  $\mu\text{m}$ ) shown in Fig. 6.4 was fabricated using a metal shadow mask. The single crystal  $\text{TiO}_2$  rutile was a commercial single crystal purchased from MTI Corporation. A single irreversible forming step was necessary for the as-prepared (virgin) devices before they exhibited repeatable switching cycles; for the nanodevices this forming occurred at approximately +8 V and 10  $\mu\text{A}$ . A HP 4156 semiconductor parameter analyzer was used for the electrical characterization with a four-probe DC measurement method. The bottom electrodes of the junctions were grounded during all the electrical measurements.

### 6.1.3 Switching Behavior

A promising switching behavior we observed in both micron- and nano-scale crosspoint devices is the bipolar, reversible, and non-volatile switching of Pt/ $\text{TiO}_2$ /Pt structures with ON/OFF conductance ratios of  $\sim 10^3$ . Figure 6.1a presents an AFM image of crosspoint nanodevices with a 50 nm thick  $\text{TiO}_2$  insulator sandwiched between 50 nm wide top and bottom Pt nanowire electrodes fabricated by nanoimprint lithography [47, 48]. For electrical testing, we apply a bias voltage to the top electrode with the bottom electrode grounded. The initial current–voltage ( $I$ – $V$ ) curve of the device in its virgin (pre-switching) state exhibits a rectifying characteristic (Fig. 6.1b). After a single irreversible forming step, multiple switching  $I$ – $V$  curves in Fig. 6.1c demonstrate a high degree of repeatability, while utilizing different current compliance reveals multiple resistive states of the device. The device was switched ON only by a negative bias and OFF only by the opposite (positive) bias (this is the definition of a bipolar switch). This switching polarity was defined by the device fabrication procedure and was independent of the voltage bias polarity of the forming step, which induces a profound and essentially permanent change to the oxide film via electro-reduction [49], which will be discussed in detail in Sect. 6.3. The  $I$ – $V$  trace (Fig. 6.1c) of the device in the ON state was an exponential function in both quadrants, well fit by the form  $I \sim \beta \sinh(\alpha V)$ , which is often characteristic of electron tunneling, thermionic emission over a barrier, or a combination of both. In the OFF state the  $I$ – $V$  curve was rectifying, similar to the virgin state. These  $I$ – $V$  curves contain valuable information to decipher the nature of the ON and OFF states. For instance, the rectification suggests that the OFF state may be limited by Schottky-like transport at one of the metal–oxide interfaces. However,



**Fig. 6.2** Junctions on single crystal  $\text{TiO}_2$  show the role of the interface in determining the electrical behavior. **(a)** A schematic of the electrodes and the single crystal. Four adjacent pads were deposited as pairs of Pt and Ti/Pt contacts. **(b)** Energy diagram shows the low  $V_O$  concentration under the Pt pads maintains the Schottky-like barrier (denoted as a rectifier) between Pt and  $\text{TiO}_2$  to produce rectifying junctions, whereas the high  $V_O$  concentration at the interface under the Ti/Pt pads collapses the Schottky-like barrier and produces ohmic contacts (denoted as a resistor). **(c)** The four-probe  $I$ - $V$  curves between the combinations of the four pads in **(a)**. The insets to these  $I$ - $V$  diagrams are the corresponding equivalent circuit diagrams consisting of two electronic elements (rectifier or resistor) in series (Macmillan Publishers Limited)

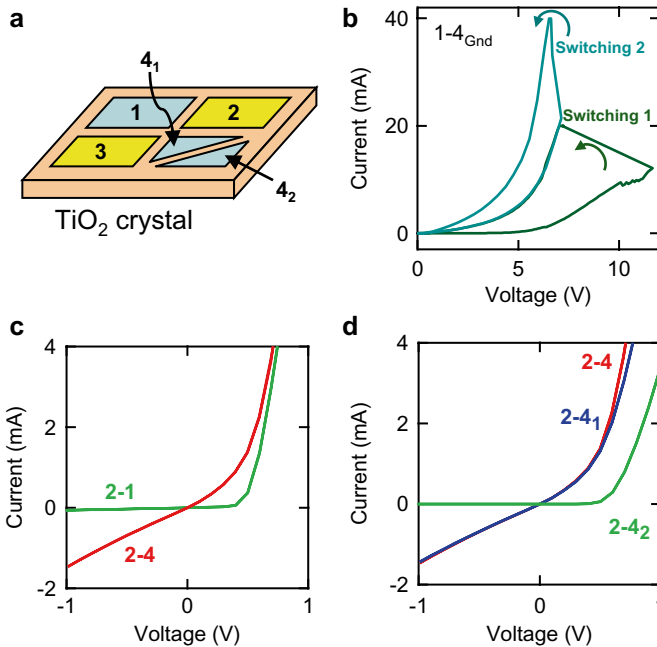
for the thin film device structure of Fig. 6.1, the top and bottom interfaces of the device cannot be isolated for electrical characterization before or after a switching event, and thus it is not possible to identify the separate role of each interface. Therefore, a new experimental design that enables the junction interfaces to be studied separately is needed to obtain better insight into the switching.

Single crystalline  $\text{TiO}_2$  was used to elucidate how the metal/oxide interfaces control the device resistance. As shown in Fig. 6.2a, a single crystal of rutile  $\text{TiO}_2$  (bandgap  $E_g \sim 3.0$  eV) was first annealed in a 95 %  $\text{N}_2$  and 5 %  $\text{H}_2$  gas mixture at 550 °C for 2 h to create an oxygen-deficient layer near the surface. Oxygen vacancies ( $V_O$ ) in  $\text{TiO}_2$  are known to act as n-type dopants [18], transforming the insulating oxide into an electrically conductive doped semiconductor. Metal–semiconductor contacts are typically ohmic in the case of very heavy doping, and rectifying (Schottky-like) in the case of low doping [50]. We deposited two pairs of  $(100 \mu\text{m})^2$  Pt and Ti electrode contact pads onto the single crystal, as shown schematically in Fig. 6.2a: pads #1 and #4 were Pt films (80 nm thick) while pads #2 and #3 were Ti films (5 nm) with Pt (80 nm) to cap them. The 5 nm Ti layer was used as a chemically reactive contact to further reduce the  $\text{TiO}_2$  and create a locally high concentration of oxygen vacancies close to the metal–semiconductor interface. The four-probe electrical measurement between these two Ti pads showed a  $\sim 40$  Ohm resistance and a linear  $I$ - $V$  (labeled 2–3) in Fig. 6.2c, demonstrating that both interfaces were ohmic and the bulk resistance of the annealed single crystal was low. In contrast, the electrical resistance between the two chemically unreactive Pt contact pads #1 and #4 was four orders of magnitude higher with a symmetric nonlinear  $I$ - $V$  characteristic

(Fig. 6.2c). The  $I$ - $V$  between unmatched contacts #1 (Pt) and #3 (Ti) with pad #3 grounded exhibited a rectifying characteristic similar to that observed for the nanoscale thin film device of Fig. 6.1. Since the interface under pad #3 was known to be ohmic, and the rutile bulk resistivity was low, we directly infer that the electronic transport was controlled by a Schottky-like barrier under pad #1, *i.e.* between the pure Pt contact and the n-type (reduced) rutile. The opposite polarity rectifying  $I$ - $V$  curve measured between pads #2 (Ti) and #4 (Pt) with pad #4 grounded revealed a similar Schottky-like contact under pad #4. These measurements were confirmed by measuring all Pt-Ti two-terminal permutations. As the energy diagram in Fig. 6.2b illustrates schematically, the high  $V_O$  concentration under the Ti electrodes (and the lower Ti workfunction) serve to collapse the Schottky-like barrier and produce ohmic contacts, whereas the low  $V_O$  concentration under the Pt pads maintains the Schottky-like barrier between Pt and Ti dioxide to produce rectifying junctions. When the rutile single crystal was annealed further at higher temperature and longer time (e.g. 900 °C, 5 h) to increase the near surface  $V_O$  concentration, even the pure Pt contacts became ohmic. Comparing these data to the rectifying  $I$ - $V$  curves of the thin film nanodevice in Fig. 6.1, we conclude that the top interface of the thin film device is non-ohmic (conceivably Schottky-like) and the bottom interface is ohmic for both the virgin state and the OFF switch state.

To explore the ON switch state, an increasing positive voltage bias was applied on Pt pad #1 with Pt pad #4 grounded, until the device switched to a more conductive state as shown by the “Switching 1” curve in Fig. 6.3b. This switching was non-volatile; a subsequent voltage sweep (Switching 2 curve) retraced the first high conductivity curve until the device switched to an even more conductive state. In order to determine whether the switching took place under the positively biased contact #1 or the (effectively) negatively biased contact #4, an  $I$ - $V$  curve for each was measured separately using the ohmic Ti contact #2. The  $I$ - $V$  curve measured between contacts #1 and #2 maintained the rectifying characteristic with very little change. However, as shown in Fig. 6.3c, the rectifying behavior of electrode #4 was dramatically reduced. Thus, only the Schottky-like barrier at the negatively biased interface was affected by the switching event. This can be explained by the fact that oxygen vacancies in  $\text{TiO}_2$  are known to be positively charged and mobile [51]; the negatively biased electrode attracts  $V_{Os}$  from the rutile crystal to the interface, causing a partial collapse of the Schottky-like barrier.

The question that remains is whether the change at the interface under contact #4 is uniform or localized, since Szot et al. [4] have observed the formation of localized regions of high conductance under a contact to a switched metal oxide. To investigate this issue, pad #4 was cut into two halves, denoted as #4<sub>1</sub> and #4<sub>2</sub> in Fig. 6.3a. The  $I$ - $V$  curves between ohmic Ti pad #2 and these two Pt half-pads are presented in Fig. 6.3d to compare them with the  $I$ - $V$  between pad #2 and the uncut pad #4. This shows that the interface change was localized under Pad #4<sub>1</sub>, because the  $I$ - $V$  curve for pads #2 and #4<sub>2</sub> was still a nearly ideal rectifier. The localized nature of the switching demonstrates that one or more conductance channels penetrated the Schottky-like barrier under pad #4<sub>1</sub>.



**Fig. 6.3** Switching is local and occurs at the Pt/TiO<sub>2</sub> interface. (a) A schematic of the junctions with the single crystal TiO<sub>2</sub>. Pads 1 and 4 are Pt; pads 2 and 3 are Ti. After the initial measurements in (b), pad 4 was cut in half. (b)  $I$ - $V$  curves of two switching cycles between pad 1 and 4 with pad 4 grounded. (c) The  $I$ - $V$  curves between pad 2 (grounded) and pad 1 and pad 4 after “Switching 2,” showing the change during switching is only under effectively negatively charged Pad 4. (d) Pad 4 was cut into two halves, 4<sub>1</sub> and 4<sub>2</sub> after Switching 2. The  $I$ - $V$  curves between Pad 2 (grounded) and 4<sub>1</sub> (4<sub>2</sub>) demonstrate that the interface change under Pad 4 is localized to the 4<sub>1</sub> part (Macmillan Publishers Limited)

### 6.1.4 Switching Mechanism

Based on the experimental results from the thin film and single crystal devices, we propose a general model to explain the switching behavior of the nanodevice in Fig. 6.1. The rectifying  $I$ - $V$  curve of the device in its virgin state (Fig. 6.1b) indicates that there are more  $V_{OS}$  at the bottom interface and the non-ohmic contact at the top interface dominates the electrical transport in the device. A negative voltage applied to the top electrode attracts positively charged  $V_{OS}$  in the oxide towards that electrode. The  $V_{O}$  dopants drift in the electric field through the most favorable diffusion paths, such as grain boundaries, to form channels with a high electrical conductivity. Once one or more conductance channels penetrate the electronic barrier, the device is switched ON, producing a symmetric exponential  $I$ - $V$  that is the result of tunneling through a thin residual barrier. In order to switch the device OFF, a voltage with the reverse polarity is applied. A positive bias on the top electrode repels the  $V_{OS}$  in the conducting channel away from the top interface and the original

electronic barrier is recovered. The switching OFF is thus not the result of the rupture of a conducting channel by Joule heating (even though the process may be heat assisted), as proposed for models of uni-polar switching [14], because it is bias polarity dependent. It is crucial to note that the ON and OFF switching events occur at one interface only: the rectifying non-ohmic (top) interface, as opposed to the ohmic-like (bottom) interface. The applied voltage bias may also alter the concentration of  $V_O$  at the bottom interface but this variation is not significant enough to change the ohmic contact property of that interface because (1) that interface has a very large concentration of vacancies, and (2) the electric field there is smaller due to the high conductivity. The non-ohmic interface has a very small concentration of vacancies, and is thus sensitive to change and concentrates most of the electric field due to its low conductivity. The two interface junctions are in series, and in such deliberately asymmetric devices the total resistance is always controlled by the more resistive non-ohmic interface. The devices were also found to switch ON and OFF at lower voltages (e.g., 0.1 V lower) than that shown in Fig. 6.1c, but with much longer time constants (hours), which is consistent with a slower nonlinear vacancy drift velocity under lower electric field.

This model can be represented by the equivalent circuit for the device shown as an inset in Fig. 6.1c, i.e. a rectifier in parallel with a memristor [19, 20]. This switching model is fundamentally different from either the filamentary conduction model, which neglects the important role of the interface, or the modified Schottky barrier model, which assumes a uniform interfacial change. Instead, this model is inspired by the parallel conduction model [52, 53], which posits that a macroscopic Schottky barrier is essentially a collection of a very large number of nanoscale diodes in parallel, with the net current–voltage characteristic of the junction determined mainly by the diode with the lowest Schottky barrier height as long as it has a large enough cross-section that it is not “pinched off” by the potential of the surrounding material [54]. As native n-type dopants, a cluster of  $V_O$ s can significantly lower the local potential within the  $TiO_2$ , or even change the titania stoichiometry. Under a negative bias, the  $V_O$ s drift towards the electronic barrier and form a conductive channel that shunts the rectifier. Coupled transport of charged dopants and electrons under a voltage bias that produces a switching effect has recently been shown to be the basis for long-predicted memristor behavior. Using basic symmetry arguments, Leon Chua proposed in 1971 [20] that a fourth fundamental passive circuit element must exist to complement the resistor, capacitor, and inductor. Resistors-with-memory, or “memristors” as he called them, operate as dynamical resistors that change their state according to the time integral of applied current or voltage. For our devices, an equation that describes the current–voltage switching characteristic of the memristor + rectifier equivalent circuit shown in Fig. 6.1c is

$$I = w^n \beta \sinh(\alpha V) + \chi (\exp(\gamma V) - 1) \quad (6.1)$$

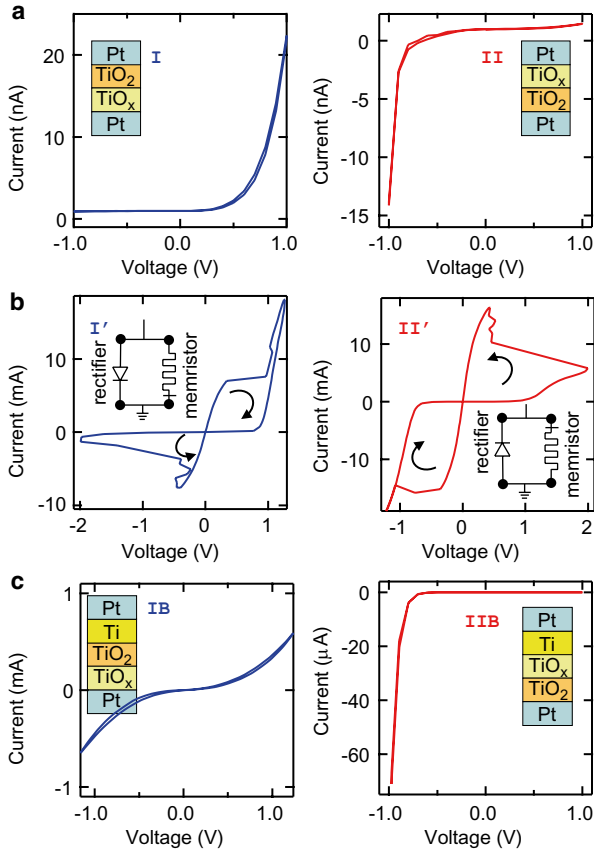
which was chosen more for its simplicity and ability to reproduce the  $I$ – $V$  behavior than as a detailed physics model. A more sophisticated model describing the

dynamical behavior of memristors can be in [55]. In the first term, which represents a flux-controlled memristor,  $\beta \sinh(\alpha V)$  is the approximation we use for the ON state of the memristor, which is essentially electron tunneling through a thin residual barrier,  $\alpha$  and  $\beta$  are fitting constants that are used to characterize the ON state, and  $w$  is the *state variable* of the memristor. In this case  $w$  is proportional to the time integral of the voltage applied to the device (or, equivalently the magnetic flux from Faraday's Law of induction, although no extrinsic magnetic fields are involved here), and is normalized to have values between 0 (OFF) and 1 (ON). If  $n=1$ , then the drift velocity of the  $V_{OS}$  is directly proportional to the applied electric field. The second term in Eq. 6.1 represents the  $I$ - $V$  approximation for the rectifier, and  $\chi$  and  $\gamma$  are the fitting constants used to characterize the net electronic barrier when the memristor is switched OFF. The exponent  $n$  of the state variable is used as a free parameter in the model that we adjust to modify the switching between the ON and OFF states of the device to be consistent with the experimental observations. We find that the best agreement between our model and the measured switching characteristics (see Fig. 6.1c) occurs for  $n$  in the range from 14 to 22, which we interpret as evidence for a highly nonlinear dependence of the effective vacancy drift velocity on the voltage applied to the device.

According to our model, the rectification and switching polarities are both determined by the initial distribution of  $V_{OS}$  in the oxide layer. We tested this prediction by fabricating thin film samples with engineered oxygen vacancy distributions. The oxide layers of these samples were actually bi-layers of  $TiO_2$  and  $TiO_{2-x}$  (containing a high concentration of  $V_{OS}$ ) formed by intentionally creating one layer of oxide with a deficit of oxygen. As shown in Fig. 6.4a, by reversing the fabrication sequence of the  $TiO_2$  and  $TiO_{2-x}$  layers for samples I and II, we inverted *both* the rectification polarity of the virgin state  $I$ - $V$  curves *and* simultaneously the polarity of the ON-OFF switching (Fig. 6.4b). Both results confirm the above switching model. In a second convincing test, an additional 5 nm Ti layer was interposed at the top interface of both samples to create yet more  $V_{OS}$  at this interface only. In Fig. 6.4c, we see that the virgin  $I$ - $V$  characteristics have been modified in opposite ways. As expected, sample IB became symmetric and very conductive—the current-limiting non-ohmic contact was reduced by the extra Ti. In contrast, sample IIB became even more rectifying; here, the extra Ti created a better ohmic contact but did not affect the non-ohmic contact.

These experimental results establish that electrical conduction in metal/oxide/metal thin film devices is controlled by a spatially heterogeneous metal/oxide electronic barrier. Memristive electrical switching proceeds via drift of positively charged oxygen vacancies acting as native dopants to form (turn ON) or disperse (turn OFF) locally conductive channels through the electronic barrier. The location, concentration, and distribution of oxygen vacancies in the as-fabricated  $TiO_2$  film control the conductance, rectification, and switching polarity of the device.

Based on the above understanding of switching mechanism, a family of nanodevices can be realized with a simple metal/oxide/metal structure, which will be addressed in Sect. 6.2.



**Fig. 6.4** Thin-film  $\text{TiO}_{2-x}$  devices with controlled oxygen vacancy profiles verify the switching mechanism. (a) Sample I and II with reversed layer sequences of 15 nm  $\text{TiO}_{2-x}$  and 15 nm  $\text{TiO}_{2-x}$  (more  $V_{\text{OS}}$ ) layers show opposite polarities of  $I-V$  curves in their virgin states. (b) The switching polarities of these two samples are also opposite. (c) Introducing more  $V_{\text{OS}}$  by adding a 5 nm Ti layer to the top interfaces of these two samples changes the  $I-V$  curves in totally different ways, confirming the dominant role of the non-ohmic interfaces in the thin-film devices (Macmillan Publishers Limited)

## 6.2 Section 2: A Device Family

### 6.2.1 Concept of the Device Family

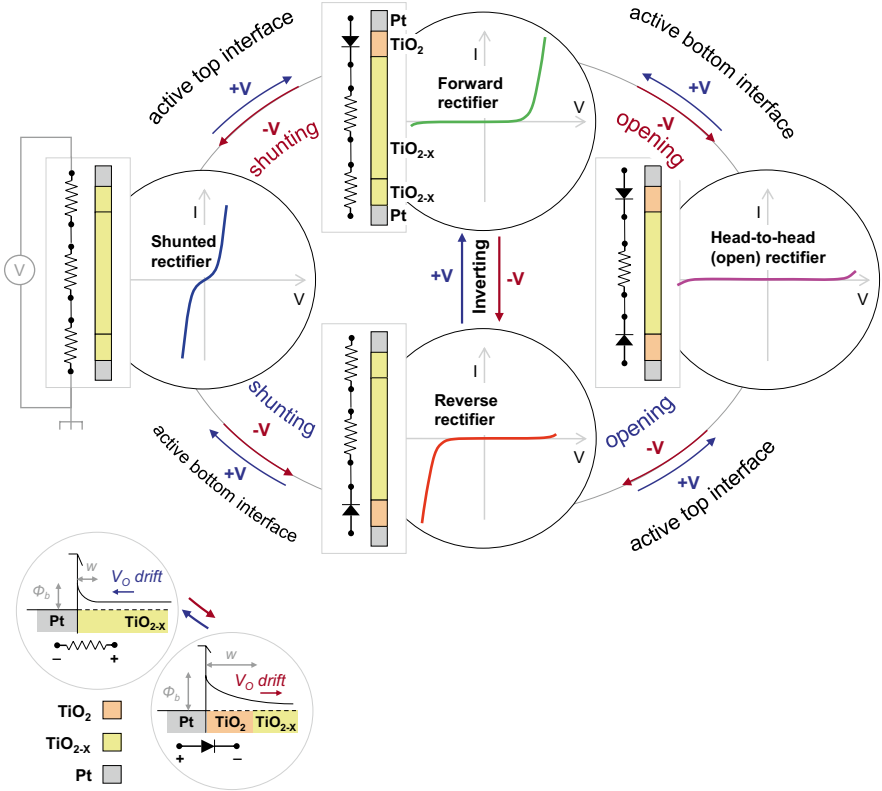
Moore's law will come to an end in a decade or so and the emphasis in electronics design will have to shift to devices that are not just increasingly infinitesimal but increasingly capable. In this section we demonstrate the concept and realization of a class of such nanodevices with extremely simple structures, reconfigurable two-terminal electronic circuit elements that behave as networks of memristive switches



[19–21] and rectifiers in parallel and series combinations, based on the physical properties of a metal/oxide/metal system. The two metal/semiconductor contacts can be either rectifying or conductive, depending on the concentration of dopants at the respective interface [46], which provides four different current–voltage characteristics. By forcing charged dopants into or out of the interface region with an applied electric field pulse, devices can be switched from one type of stable operation to another in five different ways. A family of devices built to express these properties displays a rich set of behaviors that provide new opportunities for nanoelectronics [56]. Intentionally combining memristive switching and nonlinear Schottky-like rectification, which can be embodied at metal–semiconductor interfaces, enables one to build a family of reconfigurable electronic devices with interesting and useful properties for switching, memory, and logic. In fact, the entire family of compound circuit elements can be constructed from a relatively simple metal/oxide/metal framework that yields different two-terminal devices depending on the initial distribution of oxygen vacancies. These unique devices will enhance the toolkit of circuit designers and may allow new nanoelectronic architectures in a variety of applications including memory [57, 58], logic [59, 60], synaptic computing [61, 62], and other circuits [62, 63] in a very small footprint, typically  $4 F^2$ , with  $F$  as the critical dimension of the latest technology node.

More specifically, each device has two metal/oxide interfaces that influence the electronic transport perpendicular to the tri-layer, depending on whether oxygen vacancies drift to either interface or not. In Fig. 6.5, we classify four different quasi-static electrical characteristics or end-states of the devices, i.e. *forward rectifier*, *reverse rectifier*, *shunted rectifier* (characterized by a lower resistance, symmetric  $I$ – $V$  plot) and *head-to-head rectifiers* (a high resistance or effectively open state). Which quasi-static state dominates is determined not only by the distribution of  $V_{OS}$  in the thin film of  $TiO_2$  between the two Pt electrodes but also by the choice of the circuit ground. These states will be stable as long as the voltage biases applied to the devices are small enough or fast enough that the distribution of the  $V_{OS}$  is not perturbed.

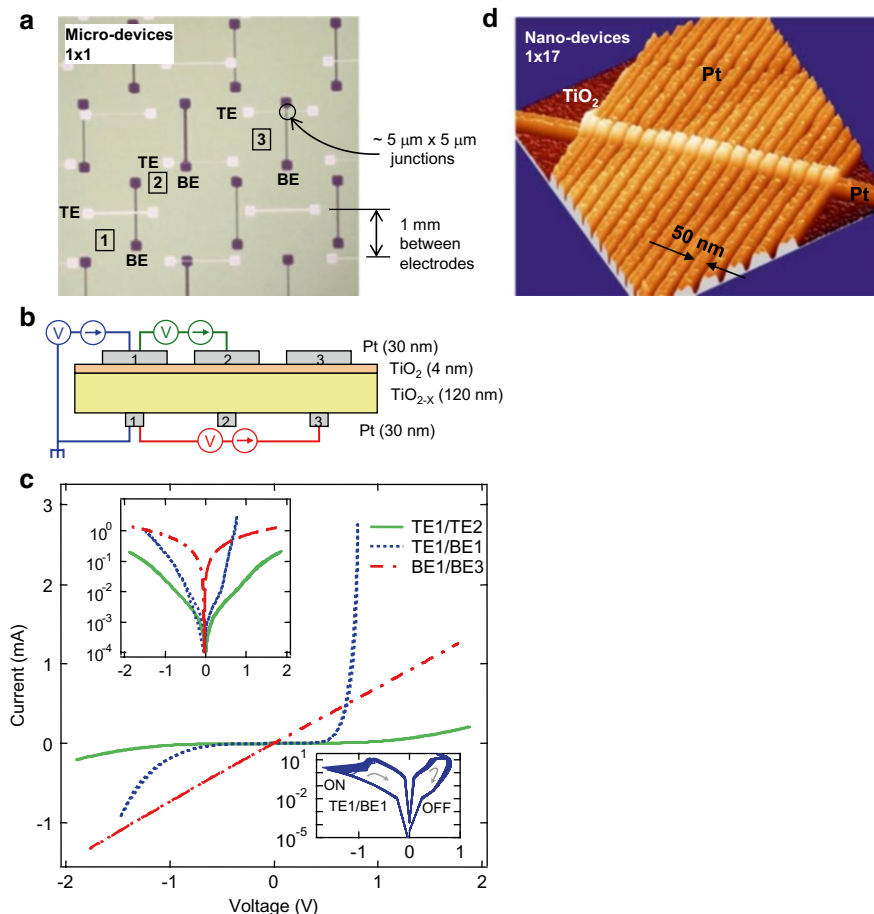
The reconfiguration of the semiconductor doping profiles due to the drift of  $V_{OS}$  under the electric field can in principle lead to six different electrical switching transitions between pairs of the four device states classified above, as illustrated in Fig. 6.5. (1) *Shunting* is exemplified by the switching between the forward rectifier and the shunted rectifier. The bottom interface of the junction is heavily doped and remains ohmic (or at least highly conductive) with negligible changes during the switching. The transition is initiated when a sufficiently large negative bias applied on the top electrode attracts positively charged  $V_{OS}$  to the top interface, switching the device from a forward rectifier to a shunted rectifier. An opposite bias repels the  $V_{OS}$  to switch the device back to the forward rectifier. Of course, the transitions between a reverse and a shunted rectifier can also be called shunting, as labeled in Fig. 6.5. (2) *Opening* is switching between a forward or reverse rectifier and a head-to-head rectifier. In the reverse rectifier case, the bottom interface remains unchanged and only the top interface is actively switched. Conversely, the forward rectifier case has an active bottom interface. In both cases, the unchanged interface (with very few



**Fig. 6.5** A family of device states exists when two dynamic metal (Pt)/semiconductor (TiOx) junctions are operated in series. Schematic drawings of the four current-transport end-states and the modes of switching between them: the  $I$ - $V$  characteristics and the corresponding oxygen vacancy ( $V_o$ ) profiles in the oxide layers are shown for the quasi-static states, with orange indicating lower  $V_o$  concentrations (semi-insulating  $TiO_2$ ). A high concentration of vacancies at the metal–semiconductor interface produces an essentially ohmic contact, whereas a low concentration yields a Schottky-like rectifier or blocking contact (*lower left*). Positively charged  $V_o$ s drift towards or away from an interface depending on the as-fabricated  $V_o$  distribution and the applied voltage polarity, resulting in switching between different states (Copyright Wiley Verlag GmbH & KGaA. Reproduced with permission)

$V_o$  dopants) remains rectifying during switching. (3) *Inverting* is different; it involves simultaneous and opposite changes at both electrodes, resulting in switching between a reverse rectifier and a forward rectifier. The last switching type, between the shunted rectifier and the head-to-head rectifier, has not been observed to date in a real device. The reason for this is clear, since it would require the  $V_o$ s drift in opposite directions simultaneously away from the two interfaces.

The two interfaces of the device are the keys to both the transport and switching. We first performed experiments (Fig. 6.6) to demonstrate the role of  $V_o$ s in modulating the properties of the interfaces. Figure 6.6a presents an optical micro-



**Fig. 6.6** Nonlinear electronic transport is controlled by the oxygen vacancy ( $V_o$ ) doped metal/oxide interfaces. **(a)** Optical microscope image of a micro-device sample. The dumbbell-shaped bottom electrodes (BE—vertical) and top electrodes (TE—horizontal) are separated by the blanket Ti oxide layer. **(b)** Schematic drawing. The oxide is a 4 nm  $\text{TiO}_2$ /120 nm  $\text{TiO}_{2-x}$  sputter-deposited bi-layer. Current–voltage  $I$ – $V$  measurements were made between pairs of the electrodes. **(c)** Linear and semi-log  $I$ – $V$  plots. *Dashed line*: ohmic conduction between two bottom Pt/ $\text{TiO}_{2-x}$  electrodes. *Solid line*: highly resistive and symmetric conduction between two top Pt/ $\text{TiO}_{2-x}$  electrodes. *Dotted line*: forward rectification from a top Pt/ $\text{TiO}_2$  electrode to the bottom Pt/ $\text{TiO}_{2-x}$  electrode. The *lower right inset* shows reversible switching operation with a zero bias resistance ratio of  $\sim 1000$  for a device defined by the electrodes TE1 and BE1. **(d)** AFM images of  $1 \times 17$  crosspoint nanodevices as used for the shunting and inverting transition measurements. The top and bottom electrodes for all devices are Pt and the insulating layer is a blanket film of  $\text{TiO}_2$  with an engineered distribution of oxygen vacancies (Copyright Wiley-VCH Verlag GmbH & Co. KGaA. Reproduced with permission)

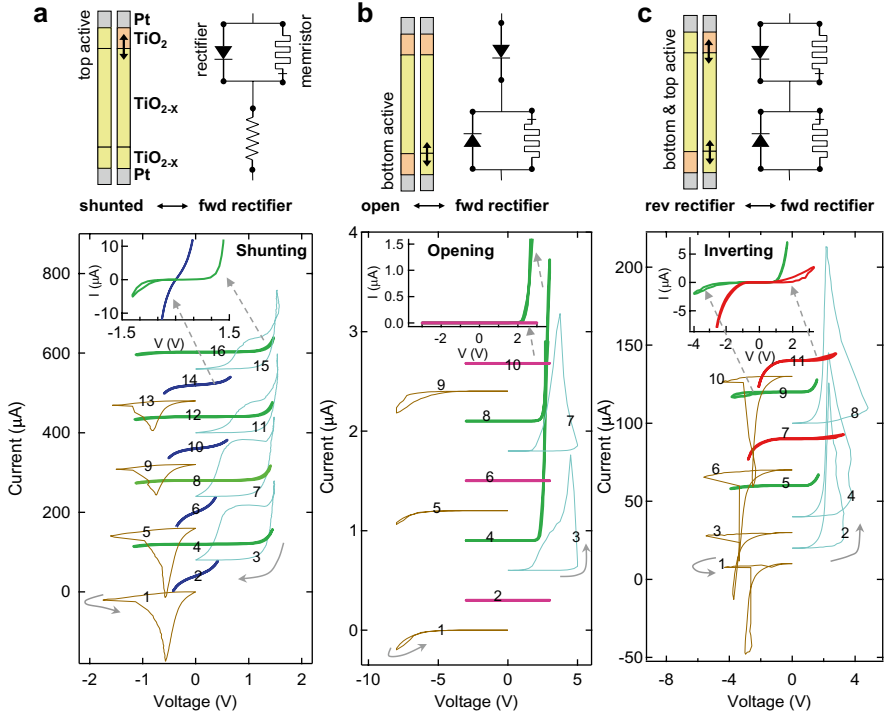
scope image of several devices that consist of Pt top electrodes (TEs) and bottom electrodes (BEs) separated vertically by a blanket titanium oxide layer. The titanium oxide layer is actually a bi-layer consisting of a very thin (4 nm) nearly stoichiometric  $\text{TiO}_2$  layer and a thicker (120 nm)  $\text{TiO}_{2-x}$  layer with a high concentration of  $V_{\text{Os}}$  (Fig. 6.6b). The  $\text{TiO}_{2-x}$  layer is an n-type semiconductor with a carrier concentration of  $\sim 10^{19} \text{ cm}^{-3}$  as determined from Hall measurements. Any pair of electrodes in Fig. 6.6a forms a two-terminal device as schematically shown in Fig. 6.6b, from which an  $I$ - $V$  curve can be obtained (Fig. 6.6c). The  $I$ - $V$  curve between two bottom electrodes (e.g., BE1 and BE3) is linear, revealing ohmic contacts at both the Pt/ $\text{TiO}_{2-x}$  interfaces. In contrast, the  $I$ - $V$  curve between two top electrodes (e.g., TE1 and TE2) is symmetric and nonlinear, revealing blocking contacts at both Pt/ $\text{TiO}_2$  interfaces. The much lower current between the top electrodes compared to the bottom electrodes shows that the blocking interfaces dominate the electrical transport. A rectifying  $I$ - $V$  is obtained between electrodes TE1 and BE1, consistent with the fact that the corresponding device has one blocking (Pt/ $\text{TiO}_2$ ) interface and one ohmic (Pt/ $\text{TiO}_{2-x}$ ) interface. Reversible switching  $I$ - $V$  loops between TE1 and BE1 similar to those previously reported are shown as the lower inset to Fig. 6.6c.

Crosspoint devices have been built to demonstrate the device concepts shown in Fig. 6.5. Figure 6.6d presents an atomic force microscope (AFM) image of a  $1 \times 17$  set of nanodevices ( $50 \text{ nm} \times 50 \text{ nm}$ ) as used for the shunting and inverting transition measurements. An ultra-high density two-dimensional array of such configurable memristive nanodevices suitable for memory or logic applications has also been built.

## 6.2.2 Realization of the Device Family

The as-fabricated state of a junction, i.e. the initial  $V_{\text{O}}$  profile, in large degree determines the switching character of the device. The initial  $V_{\text{O}}$  profile can be controlled by engineering the structure and/or the fabrication conditions of the device. In the following, we demonstrate three types of switching in real devices.

Figure 6.7a presents the experimental data for a *shunting* transition. The bottom electrode is grounded and the voltage is applied to the top electrode for all electrical measurements in this study. The device was fabricated to have a very asymmetric distribution of  $V_{\text{Os}}$ , with the top interface having a much smaller concentration than the bottom interface which thus remains ohmic during switching. The active region is the top interface, governing the electronic transport of the junction and the switching. A positive bias on the top electrode repels the positively charged  $V_{\text{Os}}$  from the top interface and switches the device from a conducting to a rectifying state. A negative bias on the top electrode attracts the  $V_{\text{Os}}$  to the top interface and shunts the rectifier at the top interface, switching the device to a symmetric higher conductance



**Fig. 6.7** Experimental current–voltage data for shunting (a), Opening (b), and Inverting (c), transitions, the end-states after switching the devices, and their corresponding equivalent circuits. For each transition type, the  $I$ – $V$  curves are numbered in the sequence in which they were collected. These  $I$ – $V$  curves are shown with a certain current offset for clarity.  $I$ – $V$  loops on the left and right sides represent negative and positive transition voltage sweeps (on TE), respectively. After each transition sweep (negative or positive), an interrogation  $I$ – $V$  was collected to determine the device state after switching. The upper-left insets display the two end-states corresponding to each transition type, (a), Shunting transition data from a  $50\text{ nm} \times 50\text{ nm}$  nanodevice. The device is switched to a forward rectifier with a positive bias. The device is switched to a symmetric low resistance state with a negative bias. Depending on the magnitude of the bias, the device can be switched continuously between the end-states, with higher resistances shown by the smaller loops for the last two shunting-transition sweeps. The equivalent network for this device consists of a rectifier in parallel with a memristor. (b) Opening transition data from a  $5\text{ }\mu\text{m} \times 5\text{ }\mu\text{m}$  device, to yield a current high enough for low noise measurements. The device is switched to the head-to-head or open state with a negative bias. The device is switched to the forward rectifier in series with a shunting-transition device. (c) Inverting transition data from a  $50\text{ nm} \times 50\text{ nm}$  device. The rectifying direction of the test  $I$ – $V$  curve is inverted after each transition induced by a positive or negative bias. The equivalent circuit consists of two head-to-head shunting-transition devices in series (Copyright Wiley-VCH Verlag GmbH & Co. KGaA. Reproduced with permission)

state. Depending on the length and magnitude of the bias, the device can be configured continuously between the two end-states. This is exemplified in Fig. 6.7a, where the final two symmetric  $I$ – $V$  states have a higher resistance than the first two. We have previously shown that a simple equivalent network (Fig. 6.7a) with a

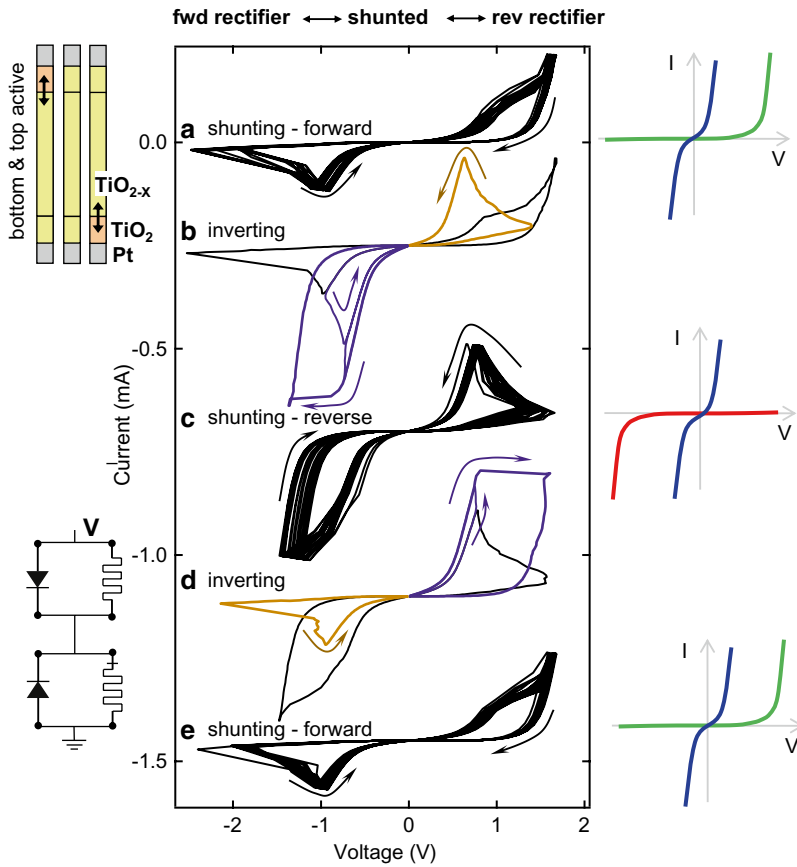
memristor in parallel with a rectifier describes the switching and end-state  $I$ - $V$  behavior of such a device reasonably well.

The electrical data for the *opening* transition is shown in Fig. 6.7b. The two interfaces of this device are also engineered to be asymmetric. The more resistive top interface remains rectifying during the transition and the active region is the bottom interface. A negative voltage sweep to  $-8$  V pulls positive  $V_{OS}$  away from the bottom interface and leaves the device in a very high resistance head-to-head or open state, as revealed by the quasi-static  $I$ - $V$  curves. The positive bias transition sweep to  $+5$  V then switches the bottom interface to an ohmic state, and the electrical transport of the device is again limited by the rectifying top interface. Expanded-scale  $I$ - $V$  curves for both head-to-head and forward rectifier states are shown as an inset to Fig. 6.7b. The equivalent circuit for this device adds an anti-parallel rectifier in series with the shunting transition device of Fig. 6.7a. An opening-transition device is ideal as a bit cell in a crossbar memory, since it effectively eliminates the problem of cross talk or current sneak-paths in this highly interconnected architecture [64]. In addition, the operating power for this type of device is extremely low. We anticipate good scalability of this structure, with switching and reading at the nA current level for nanoscale devices based on the  $\mu$ A currents used to switch the micro-scale device in Fig. 6.7b (used for this demonstration to prove low noise operation).

Figure 6.7c presents the electrical data for the *inverting* transition. This device was carefully fabricated with an almost symmetric  $V_O$  concentration profile. With a positive voltage sweep on the top electrode,  $V_{OS}$  are repelled from the top interface and simultaneously attracted to the bottom interface, resulting in a higher concentration of  $V_{OS}$  at the bottom and a forward rectifier state. A negative transition sweep reverses the  $V_O$  profile in the oxide layer and switches the device to the reverse-rectifier state. The equivalent network (inset in Fig. 6.7c) for an inverting-transition device is just two head-to-head shunting-transition devices in series.

In addition to the above transitions between pairs of the four end-states, transitions involving three end-states are also possible and lead to interesting triply configurable devices that may find unique applications in some new electronic circuits, e.g. synaptic computing. Figure 6.8 exemplifies such a device that has the same equivalent network as that of the *inverting*-transition device, except in this case there are two types of transitions: shunting to switch the device reversibly from either a forward or reverse rectifier to the shunted state, and inverting to switch the device from the forward to the reverse rectifier state and back.

In this section, we have introduced a family of reconfigurable nanodevices based on the interaction between the memristive switching and rectification properties at the two interfaces of metal/oxide/metal crosspoint devices. Four different  $I$ - $V$  end-states are possible depending on the transport properties at the two interfaces of a crosspoint, and it is possible at present to build three types of devices that exhibit transitions between pairs of these states by controlling the initial distribution of  $V_{OS}$  in the oxide layer. An interesting triply configurable device has also been demonstrated.



**Fig. 6.8** Triply configurable device involving three end-states (forward, shunted, and reverse rectifier) instead of just two end-states. The junction area is  $50 \text{ nm} \times 50 \text{ nm}$ . The transition sweeps are lettered in sequence: (a) 20 shunting transition cycles from the forward rectifier state; (b) application of larger negative transition sweeps cause the device to invert from the forward to a reverse rectifier states; (c) 20 shunting transition cycles from the reverse rectifier state; (d) application of larger positive transition sweeps cause the device to invert from the reverse to the forward rectifier state; and (e) 20 more shunting transition cycles from the forward rectifier state. The resistance ratio for either rectifier state to the shunted state at  $+0.5 \text{ V}$  is about 1000 (Copyright Wiley-VCH Verlag GmbH & Co. KGaA. Reproduced with permission)

These devices may find promising applications for their ability to be field configured into a particular state (forward or reverse rectifier, conductor or open) or for their actual switching properties as the transition between states under an applied voltage bias. However, before these devices can be used in a circuit in a reliable and predictable fashion, there are some issues that need to be addressed first, including electroforming and device engineering as shown in the following sections.

## 6.3 Section 3: Electroforming Mechanism

### 6.3.1 Introduction

Memristive switching mechanism and a family of nanodevices have been introduced in the previous section. In fact, resistive switching in metal oxides has seen more than four decades of scientific research [4, 28, 32, 35, 38, 39, 65–70], motivated in large part by that prospect of a fast and high density NVRAM technology [27, 28, 71–76]. The continuous resistance change exhibited by oxide switches also appears to meet analog switch requirements for neuromorphic computing [15, 25, 26]. Despite this promise, answers to some key questions have remained elusive for the devices due to the lack of solid experimental evidence and the metal oxide technology has not yet matured.

The least understood and most problematic step in the operation of these metal oxide switches is typically the “electroforming” process, a one-time application of high voltage or current that produces a significant and irreversible change of electronic conductivity [77–80]. Subsequent to this change the devices operate as tunable resistance switches, but with a wide variance of properties dependent on the details of the electroforming. This variance is an Achilles’ heel limiting the adoption of metal oxide switches in computing circuits. In this section, we explain the electroforming mechanism for a bipolar metal/oxide/metal switch by identifying the active species responsible for the irreversible change, the behavior under bipolar forming voltages, and the relation to subsequent electrical switching. Based on these insights, we postulate and then demonstrate a method to eliminate the electroforming process altogether. This understanding yields new control and repeatability to promise improved engineering of the switches for future nanoscale integrated circuits.

### 6.3.2 Experiment

In the following study, all the metal layers, including Pt and Ti, were deposited via e-beam evaporation at 300 K. The TiO<sub>2</sub> layers were deposited by sputtering from a polycrystalline rutile TiO<sub>2</sub> target with the Ar pressure of ~1.5 mTorr and the substrate temperature of 250–300 °C. The Ti (1.5 nm adhesion layer)+Pt (8 nm) electrode used for the 50 nm×50 nm nano-junctions was patterned by ultraviolet-nanoimprint lithography. The Ti (5 nm adhesion layer)+Pt (15 nm for BE and 30 nm for TE) electrodes used for the micro-junctions (5 μm×5 μm) were fabricated using a metal shadow mask. The highly reduced TiO<sub>2-x</sub> layer was deposited by reactive-sputtering from a Ti target with Ar and O<sub>2</sub> gas mixture. A HP 4156 semiconductor parameter analyzer was used for the electrical characterization with the four-probe DC measurement method. All voltages were applied to the top electrode (TE); the bottom electrodes (BE) of the junctions were electrically grounded during all measurements. All electrical measurements were done in air at 300 K.



### 6.3.3 Gas Bubble Formation

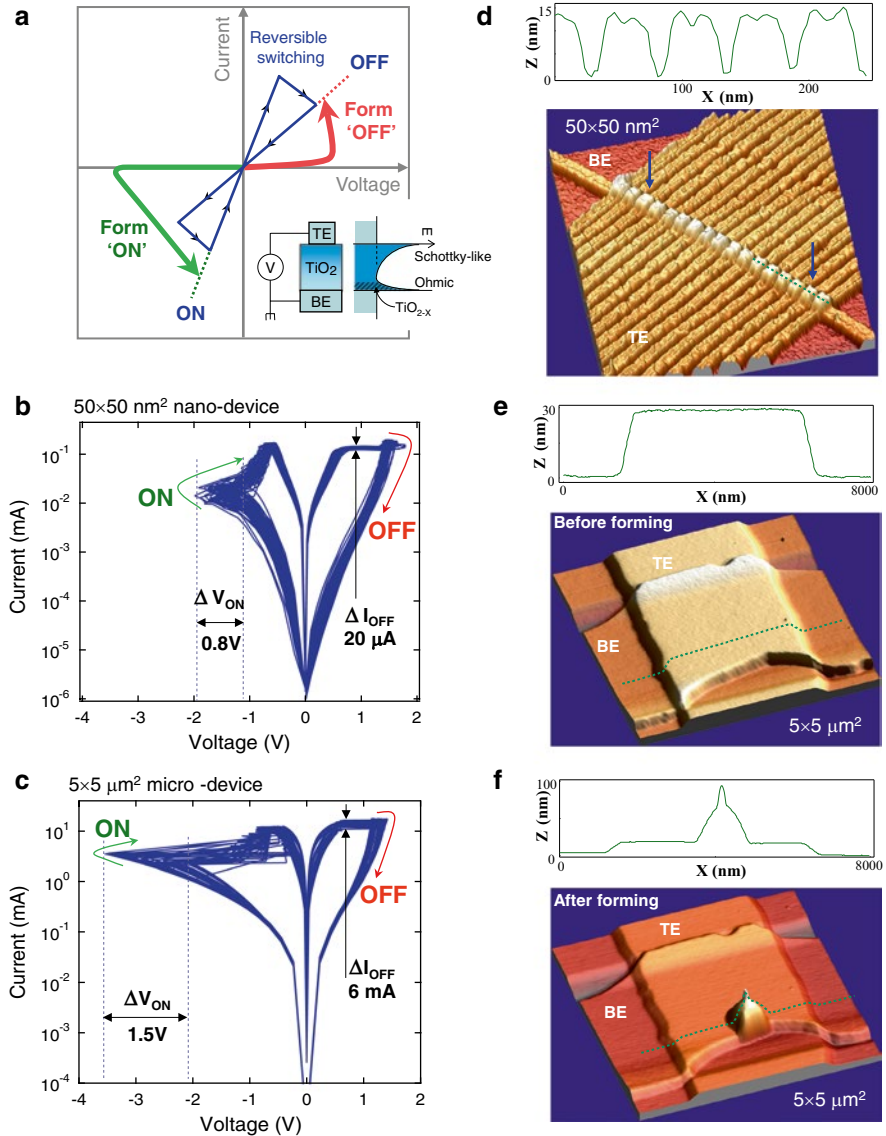
The idealized electrical behavior of a memristive oxide switch is shown in Fig. 6.9a. Repeatable ON/OFF switching follows a “bowtie” or “figure-8” shaped current-voltage  $I$ - $V$  curve. This repeatable switching is only arrived at, however, after a one-time electroforming step of high positive voltage or high negative voltage changes the device from a virgin near-insulating state into an ON/OFF switching state. As shown, opposite polarities of forming voltage and current typically produce opposite initial states of the switch. In this example, a positive voltage on the top electrode (TE) forms the device into the OFF state. A negative voltage forms the device into the ON state (the bottom electrode (BE) is grounded for all electrical measurements in this report). After electroforming, both nanoscale and micron scale devices show repeatable non-volatile bipolar switching (Fig. 6.9b, c). These devices are switched ON by a negative voltage and switched OFF by a positive voltage on the top electrodes. Polarity of switching is usually controlled by the asymmetry of the interfaces as fabricated; for all reported devices the top interface is Schottky-like and the bottom interface is Ohmic-like (Fig. 6.9a, inset).

Figure 6.9d presents atomic force microscopy (AFM) images for nanodevices with a 50 nm thick  $\text{TiO}_2$  insulator sandwiched between 50 nm wide Pt nanowire electrodes, as fabricated by nanoimprint lithography (NIL) [47, 48]. The  $\text{TiO}_2$  is a sputter-deposited amorphous or nanocrystalline thin film. Among these  $1 \times 17$  nano-junctions, the 2nd and the 15th junctions (indicated by arrows) have been electrically formed and switched, including more than 50 cycles for the 2nd junction. An AFM cross-section profile is also shown. For the nano-junctions, no topographic difference can be detected between the formed devices and the virgin devices.

In striking contrast, clear physical deformation appeared for the micro-devices after electroforming. Figure 6.9e, f shows AFM images of a micro-device before and after a one-time negative voltage electrical forming process. A large dome-like physical deformation has appeared along the edge of the bottom electrode (Fig. 6.9f). Dimensions of the dome in cross-section show a diameter of about  $1 \mu\text{m}$  and a height of about 50 nm. An eruption-like feature is visible on the top of the dome. This device consisted of  $5 \mu\text{m}$  wide, 15 nm thick top, and 30 nm thick bottom Pt electrodes separated by a 50 nm thick blanket  $\text{TiO}_2$  layer.

Physical deformations have been reported to accompany electroforming in metal/oxide/metal structures since the 1960s, however the causes are still controversial and have been attributed to a number of mechanisms including electrode melting, solid electrolysis, and others [81–87]. Electro-reduction has been shown in bulk oxide materials under electric bias [49, 88]. The physical deformation behavior in our devices shows a strong dependence on bias polarity and junction size. We test these dependences to establish oxygen ion and oxygen vacancy creation via electro-reduction of the  $\text{TiO}_2$  as the core mechanism behind the physical deformation and electrical conductivity changes during electroforming.

In our Pt/ $\text{TiO}_2$ /Pt crosspoint junctions, the middle  $\text{TiO}_2$  film is always a blanket layer across the wafer and the junction is defined by the overlapping area of the top



**Fig. 6.9** Electrical switching and forming for nano- and micro-devices. Voltages are applied to the top electrode (TE); the bottom electrode (BE) is grounded for all measurements in this report. (a) Schematic of the forming step and subsequent bipolar reversible switching. The device can be irreversibly formed either by a positive bias to the "OFF" state or by a negative bias to the "ON" state. (inset) Polarity of switching is usually controlled by the asymmetry of the interfaces as fabricated; the top interface is Schottky-like and the bottom interface is Ohmic-like. (b, c) 50 cycles of the bipolar switching for a  $50 \times 50 \text{ nm}^2$  nanodevice and a  $5 \times 5 \mu\text{m}^2$  macro-device. Both devices are switched ON by a negative bias and OFF by a positive bias on the top electrodes. The variances of ON switching voltage ( $V_{\text{ON}}$ ) and OFF switching current ( $I_{\text{OFF}}$ ) are larger for the micro-device.

and bottom electrodes. We postulate the physical deformation occurs when negatively charged oxygen ions drift to the positively biased electrode (anode) and are discharged there to form  $O_2$  gas, which accumulates to a certain pressure and then erupts from the mechanically weakest part of the thin films.

Why is there no physical deformation observed in the nanodevices? The nanodevices are 100 times smaller in linear dimension and  $10^4$  times smaller in volume than the micro-devices (the  $TiO_2$  film thickness is the same). Assuming that the oxide film is reduced to a certain degree when the device is electroformed, we see that the amount of material decomposition, gas produced, and pressure accumulated before deformation in a nanoscale device may be  $\sim 10^4$  times smaller than for a micro-scale device. Amplifying this difference, diffusion of gas to escape at the electrode edges should also be  $(100)^2 \approx 10^4$  times faster. Although a qualitatively similar switching behavior has been observed for both micro- and nano-junctions, the reproducibility of each switching loop in the nanodevice is better than in the micro-device; voltage and current variances are lower (Fig. 6.9b, c). We attribute this improved performance to less physical disruption during the electroforming process.

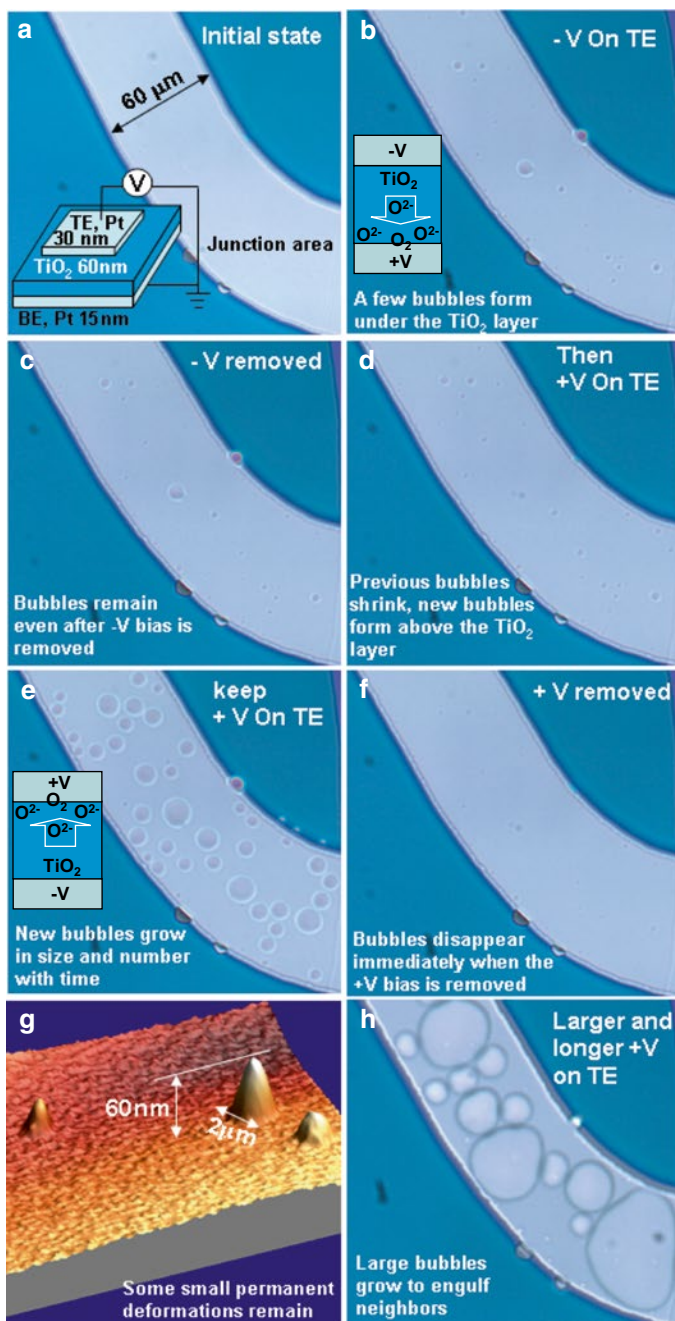
In order to more clearly observe the gas bubble behavior, an even larger  $60 \mu m$  device was tested (Fig. 6.10). In such a large device, more gas is likely produced and it is more difficult ( $\sim 100$  times slower again compared to the  $5 \mu m$  devices) for the gas to diffuse to the edge of the electrodes. The schematic inset to Fig. 6.10a shows the device configuration. Both the Pt bottom electrode and the  $TiO_2$  layer are blanket films and the Pt top electrode defines the junction area. In Fig. 6.10b,  $-4 V$  applied to the top electrode (TE) induced a few bubbles, readily visible in the optical microscope images. The bubbles remain after removing the bias, as shown in Fig. 6.10c. An opposite bias of  $+4 V$  leads to the shrinking of the previous bubbles, and the simultaneous formation of small new bubbles (Fig. 6.10d). The new bubbles grow in number and size in Fig. 6.10e when the positive voltage is maintained. After the removal of the  $+4 V$ , the bubbles shrink and disappear completely within seconds (Fig. 6.10f). Close inspection by AFM reveals remnant eruption-like features on the surface of the top electrode (Fig. 6.10g). A larger or longer applied voltage causes growth and agglomeration of bubbles, resulting in fewer, larger bubbles (Fig. 6.10h).

In the case of a negative voltage on the top electrode, oxygen gas would form under the  $TiO_2$  layer and be contained by the  $60 \text{ nm } TiO_2$  and  $30 \text{ nm Pt}$  top electrode

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←

**Fig. 6.9** (continued) The ON/OFF conductance ratios are  $\sim 10^3$  for both devices; the current level of the nanodevice is  $\sim 100\times$  smaller, the area of the nanodevice is  $\sim 10^4$  smaller. (d) AFM image of  $1 \times 17$  nano-junctions. The cross-section profile shows  $50 \text{ nm}$  half-pitch and  $13 \text{ nm}$  height nanowires. The 2nd and 15th junctions (indicated by *arrows*) were electrically formed “ON,” and do not show any detectable deformation. (e) AFM image of a  $5 \times 5 \mu m^2$  junction before electrical forming. The cross-section profile shows about  $5 \mu m$  width and  $30 \text{ nm}$  height of the top electrode (TE). (f) AFM image of the same micron junction after a negative bias forming process. Remarkably, a  $1 \mu m \times 50 \text{ nm}$  bubble has formed along the edge of the bottom electrode (BE). A distinct pointed tip suggests gas eruption (IOP Publishing Ltd)



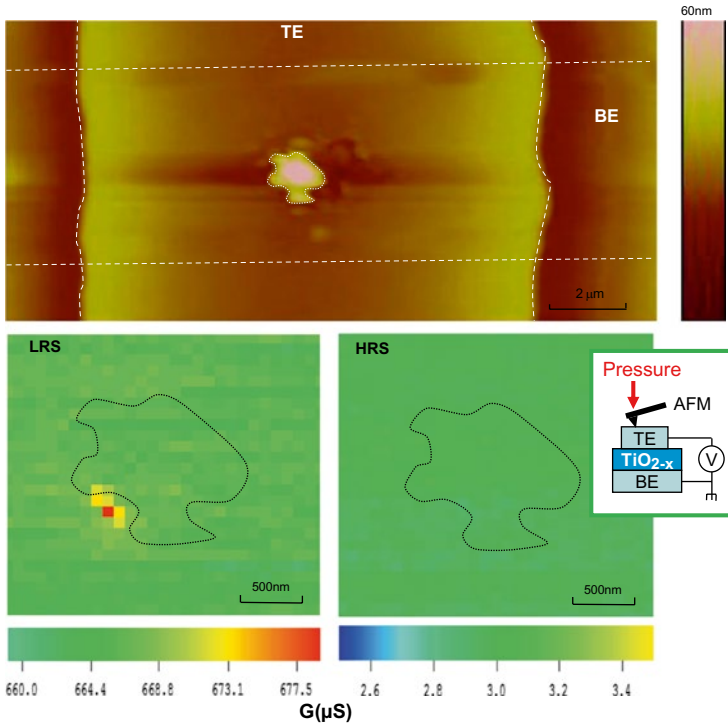
**Fig. 6.10** Device image and schematic (a), Gas bubble behavior under (b, c) negative bias, then under (d, e, f, g, h) positive bias. (g) Atomic features remaining after the bias voltage were removed. Videos of bubble evolution are available in the Supplemental information (IOP Publishing Ltd)

layers, illustrated schematically in Fig. 6.10b. Conversely, with a positive voltage on the top electrode, gas would form above the  $\text{TiO}_2$  and be contained only by the Pt electrode (schematic in Fig. 6.10e). We postulate that a higher gas pressure is needed to form a bubble under the  $\text{TiO}_2$  (Fig. 6.10b), which leads to fewer and smaller gas bubbles compared to bubbling above the  $\text{TiO}_2$  (Fig. 6.10e). These bubbles usually do not disappear until a positive voltage is applied (Fig. 6.10d), when the gas may be reincorporated into the film via electrochemical reaction. The gas formed above the  $\text{TiO}_2$  film readily escapes at the top electrode edge or through small eruption features on the top electrode surface (Fig. 6.10g), so that these gas bubbles remain only a few seconds after removing the positive voltage. This scenario is further supported by delamination experiments in which  $-V$  electroforming usually creates a round hole through the  $\text{TiO}_2$  layer while  $+V$  forming essentially leaves the  $\text{TiO}_2$  layer intact but just causes some deformation in the top Pt layer [89], as it will be discussed in more detail below.

A clear spatial correlation between the oxygen bubbles and the electrical switching is demonstrated via the Local Pressure-modulated Conductance Microscopy (LPCM) technique [90], as shown in Fig. 6.11. An AFM image shows a bubble formed in the center of the junction area after a negative voltage electroforming process. The creation of oxygen gas is accompanied by the concomitant creation of oxygen vacancies ( $V_O$ ) in the  $\text{TiO}_2$ , or more precisely the  $\text{TiO}_{2-x}$ . Such vacancies are known to dope the semiconducting  $\text{TiO}_2$  to high conductivities [18]. With the LPCM technique, a small  $\sim 50$  mV bias is applied between the top and bottom electrodes and the current flowing is monitored while scanning an AFM tip in contact mode over the top electrode. The AFM is not electrically connected—it simply serves to apply local pressure. Previous experiments [91, 92] have established that local strain induced by the AFM tip reduces the gap between the electrode and the tip of a conducting channel inside the oxide film, typically causing a slightly higher current to flow through the junction. When such a spatially localized current increase occurs during scanning, the position of the AFM tip reveals the location of the conducting channel(s). One such channel is found immediately adjacent to the bubble area in the low resistance state. This conduction channel vanishes when the device is switched back to the high resistance state.

### 6.3.4 *Electroforming Mechanism*

From the observations of Figs. 6.9, 6.10, and 6.11, we conclude that the electroformation in the metal/oxide/metal devices is an electro-reduction process that creates localized, high conductance channels of an oxygen-vacancy-rich phase through the oxide film. Oxygen gas forms at the anode, where oxygen ions are attracted and discharged. However, the oxygen ions and vacancies are likely created wherever in the junction there is a high electric field and resistance. The switching junctions studied are typically quite asymmetric, consisting of a more conductive Ohmic-like interface (the bottom interface for our devices) and a more resistive Schottky-like

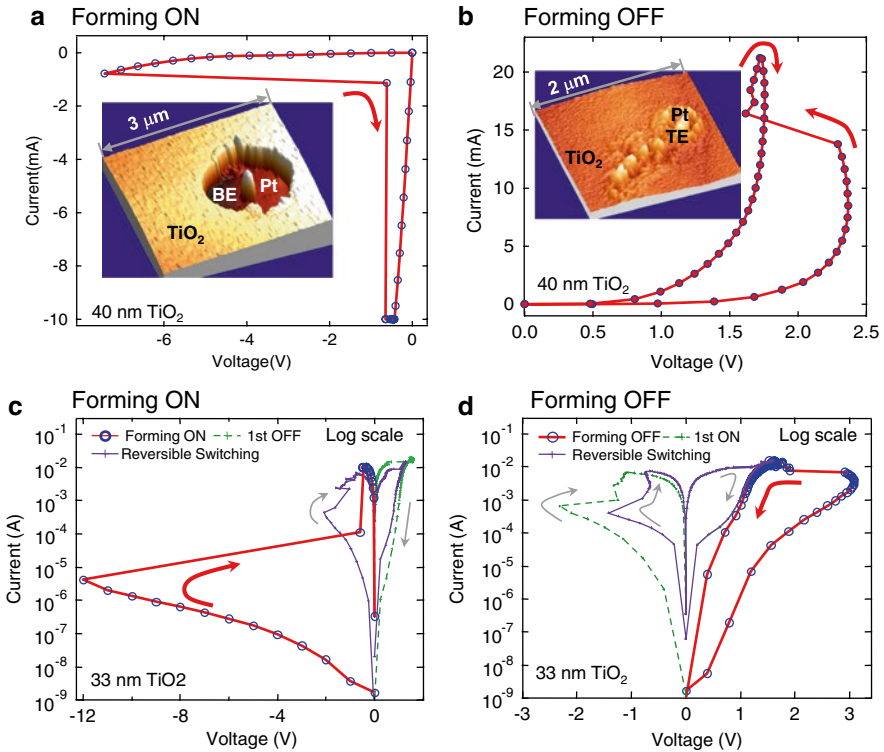


**Fig. 6.11** Conducting channel formation and dissolution adjacent to the bubble area, as observed with the Local Pressure-modulated Conductance Microscopy (LPCM) technique (*schematic*). (*top*) AFM image of a micron-size device with a bubble created in the center of the junction area during the forming step (negative bias on TE in this case). *Dashed lines* indicate the electrode edges. (*left*) LPCM conductance image of the bubble region in the low resistance state (LRS), where a conductance peak indicates the existence of a local conducting channel at the periphery of the bubble area. (*right*) After switching back to the high resistance state (HRS) the conducting channel disappears (IOP Publishing Ltd)

interface (the top interface for our devices) (see Fig. 6.9a inset). We next investigate the polarity dependence of the electroforming process to reveal the role of electric field and electrical heating.

Opposite polarity electroforming produces different final junction states, as shown in Fig. 6.12 (see also Fig. 6.9a). Two devices from the same sample (40 nm TiO<sub>2</sub> with a resistivity of 120 Ω-cm) are formed by either a negative voltage to the ON state (Fig. 6.12a) or a positive voltage to the OFF state (Fig. 6.12b). The forming process is typically too fast to be recorded and only a jump between two data points (before and after forming) is seen in the  $I$ - $V$  curves. Importantly, the field strength for these two cases is very different. Positive voltage forming apparently requires a much smaller (~one third) average electric field compared to negative voltage forming. The asymmetry of the two metal/oxide interfaces becomes critical here—the current level is much higher for positive voltages (the Schottky-like





**Fig. 6.12** Electroforming results depend strongly on bias polarity and TiO<sub>2</sub> resistivity. **(a, b)** Two devices from the same sample of 40 nm thick more (120 Ω cm) TiO<sub>2</sub>. Negative forming produces an ON state and requires high voltage but low current, positive forming yields the OFF state and requires lower voltage but higher current. (*inset*) Atomic force micrographics of the electroformed TiO<sub>2</sub> surface after the TE Pt layers were removed by delamination. -V electroforming yield a micron-size hole through the entire TiO<sub>2</sub> layer; in +V electroforming the film is intact with minor TE Pt layer residue. **(c, d)** two devices from a second sample of thinner (33 nm) but more resistive (2,300 Ω cm) TiO<sub>2</sub>, as evidenced by lower virgin-state currents. A significantly higher electric field required for both negative and positive forming (*thick solid lines with open cycles*). The first switching (ON or OFF) after forming is shown with the *dashed lines*. Subsequently reversible switchings are shown with *thin solid lines*. All the devices **(a, b, c, d)** are engineered to have more oxygen at the bottom electrode/TiO<sub>2</sub> interface, defining a switching polarity of ON for -V and OFF for +V on the top electrode (IOP publishing Ltd)

interface is forward-biased), meaning a larger electrical Joule heating effect is possible. Independent experiments suggest self-heating of several hundred degrees may be possible in these devices [93]. Oxygen vacancy mobility increases by about seven orders of magnitude from room temperature to 240 °C, as estimated by combining the Arrhenius law for the temperature dependence of diffusion and the Nernst–Einstein relation. Electroforming is not purely a heating effect, however, since it is highly polarity dependent and annealing the TiO<sub>2</sub> without bias did not produce gas bubbles. Instead, an electroforming process triggered by high electric

field and enhanced by electrical heating, where oxygen ions and vacancies are created in the region of high field and then drift towards the anode (cathode), is most consistent with these data.

In this process, a negative voltage on the top electrode produces a large voltage drop at the reverse-biased Schottky-like top interface (Fig. 6.12a). Positively charged oxygen vacancies would likely be produced here and stay at the top interface until their doping effect reduces the electronic barrier to a conductive, and hence low electric field, state. Junction currents will then increase and be limited by the insulating bulk film, now the high electric field region of the device. Creation and drift of more  $V_{\text{O}_s}$  across the bulk film quickly creates a conducting channel and low resistance ON state where *both* the resistive bulk film and resistive Schottky-like interface have been penetrated by a conducting channel.

The devices were further examined after removing the top electrode layer with a delamination technique. [94, 95] A round hole in the oxide layer is usually observed (inset to Fig. 6.12a) after electroforming with a negative voltage, indicating the  $\text{O}_2$  gas bubbles likely formed under the oxide layer to weaken the bottom electrode/oxide.

In the case of a positive voltage on the top electrode, the forward-biased Schottky-like top interface is relatively conductive and the voltage drop is instead concentrated across the bulk film. The  $\text{O}^{2-}$  anions would drift toward the positively biased top electrode and discharge there to form  $\text{O}_2$  gas on top of the  $\text{TiO}_2$  layer but under the electrode. Oxygen vacancies would drift via high diffusion paths (e.g., defects, grain boundaries) away from the top interface towards the bottom electrode to form conducting channels through the oxide film. The electric field polarity repels the growing vacancy channels from touching the top electrode—the Schottky-like barrier oxide material is not heavily reduced after forming and the post-forming state is OFF. In other words, the conducting channel penetrates the bulk film but *not* the Schottky-like interface region. In addition, the  $\text{TiO}_2$  layer is much less physically deformed by gas bubbling and eruption, since the  $\text{O}_2$  has formed on top of the  $\text{TiO}_2$  film. The inset in Fig. 6.12b shows that the  $\text{TiO}_2$  is essentially intact after delaminating the top Pt, indicating that the deformation has preferentially weakened the oxide/top electrode interface in this case. This type of electroforming is preferred and the switching behavior has been empirically observed to be more repeatable with longer device lifetimes.

This model of vacancy creation and drift is supported by the electroforming and subsequent switching  $I$ - $V$ s of devices with a thinner (33 nm) but more resistive (2,300 ohm cm) oxide layer (Fig. 6.12c, d). These devices exhibit similar behavior to the previous 40 nm oxide devices. Counterintuitively however, an even larger voltage and electric field is required to form these thinner devices. This can be rationalized by considering the possible enhancement from Joule heating, which could yield a several hundred degree temperature increase for these thicker but more conductive and thus higher current devices (Fig. 6.12a, b).

In this section, we have demonstrated that electroforming of metal/oxide/metal switches is an electro-reduction and drift process triggered by high electric fields



and enhanced by electrical Joule heating. Oxygen vacancies are created and drift towards the cathode forming localized conducting channels in the oxide film. Simultaneously,  $O^{2-}$  ions drift towards the anode and are discharged there, evolving  $O_2$  gas and causing physical deformation of the junction. The gas eruption, physical deformation, and electroformation are bias polarity dependent. Electroforming with the polarity that effects “OFF” switching typically results in a more repeatable switch performance. The switching polarity of the junction is usually dominated by the as-fabricated asymmetry of the two interfaces and thus remains independent of the forming bias polarity. The understanding of electroforming provides the basis for device engineering as shown in Sect. 6.4.

## 6.4 Section 4: Device Engineering

### 6.4.1 Introduction

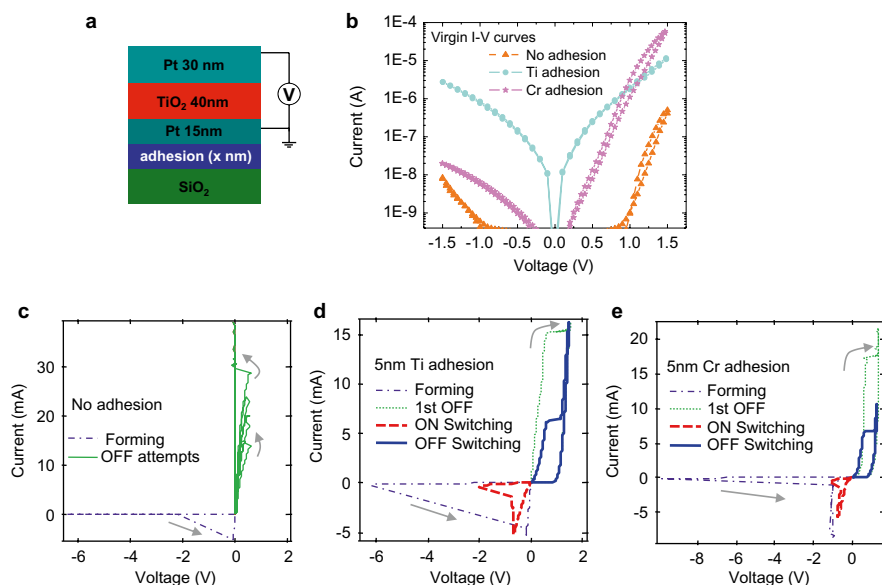
In order to make these switches useful in electrical circuits, a high device yield and an engineering control over device properties, such as switching polarity, are needed. In addition to issues created by the electroforming process in increasing the variance of the device operating parameters for consecutive cycles, the yield has historically been low. The conductance channels created during an electroforming step are the sites for the subsequent switching. As pointed out above, the electroforming process is poorly controlled leading to a broad distribution of post-forming states for the devices, including a significant resistance variance, but most importantly, uncontrolled switching polarity and even unswitchable failed devices as a result of excessive forming damage.

Here we show that electroforming and thus the subsequent switching of  $TiO_2$  metal oxide switches can be controlled by the diffusion of trace “adhesion layer” reactive metal atoms through the contact electrodes to the metal oxide switching layer. Many previous studies have focused on the as-deposited metal/oxide/metal tri-layer that nominally defines the device. However, an adhesion layer is often used to help the bottom electrode better adhere to a substrate, and the possible influence of that layer on device properties has been ignored. For a multilayered material stack that is only tens of nanometers thick, the final structure is usually different from what is nominally deposited because of strong chemical and/or physical interactions among the layers [94]. Therefore, the entire device stack should be considered as a single material system. We show that the adhesion layer material and anneal history plays a critical role in determining switching device properties, including switchable device yield, initial state conductance, and switching polarity.

Finally, based on the understanding of the switching and electroforming mechanisms, electroforming-free devices can be obtained with a bi-layer structure of the switching oxide.

## 6.4.2 Device Engineering by Seeding the Switching Centers

Devices with a junction area of  $5\ \mu\text{m} \times 5\ \mu\text{m}$  were built to demonstrate the role of the adhesion layer on device behaviors, since such large devices have adequate junction areas for some typical material characterization techniques. Three multilayered samples were fabricated on Si/SiO<sub>2</sub> wafers: a sample with a 5 nm Ti adhesion layer, a sample with a 5 nm Cr adhesion layer, and a control sample without any adhesion layer. Next, a tri-layer of Pt (15 nm)/TiO<sub>2</sub> (40 nm)/Pt (30 nm) was deposited in the same experimental run to complete these three samples and ensure that the “active layers” of the devices were identical, as illustrated schematically in Fig. 6.13a. The TiO<sub>2</sub> layer was deposited at 250 °C and then transferred in air to an evaporation chamber for the 30 nm Pt top electrode deposition at ambient temperature. Figure 6.13b presents typical  $I$ - $V$  curves of the virgin states for these three samples, which display significant differences among the three samples. Again, the measurement convention is that voltages were applied on the top electrode and the bottom electrode was grounded during the four-probe DC electrical measurements.



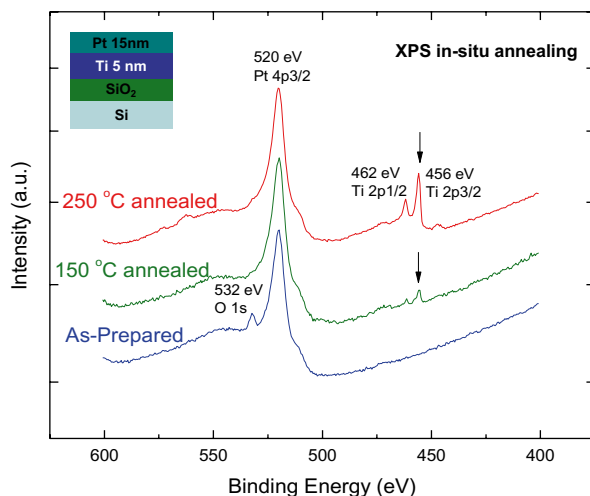
**Fig. 6.13** The effect of an adhesion layer on the electrical behavior of Pt/TiO<sub>2</sub>/Pt crosspoint junctions. (a) Schematic of the junction structure and the electrical configuration during the measurement. (b) The virgin state  $I$ - $V$  curves from three identical devices with different adhesion layer. (c–e) Electroforming and switching  $I$ - $V$  loops for the three devices. The junction with no adhesion layer was formed, but could not be switched OFF even with very high current level. This device was shorted after experiencing a high current level ( $>30$  mA). In contrast, the devices with a 5 nm Ti or Cr adhesion layer were formed and then readily switched OFF by an opposite bias (Copyright Wiley-VCH Verlag GmbH & Co. KGaA. Reproduced with permission)

The device with no adhesion layer had the lowest conductance and the one with the Ti adhesion layer had the highest conductance in the virgin state. Figure 6.13c–e present the typical electroforming and switching  $I$ – $V$  curves for these three samples. The devices with a 5 nm Ti or Cr adhesion layer were electroformed by a negative voltage sweep (magnitude >6 V) and then switched OFF with a positive 1 V bias (<20 mA). Devices with no adhesion layer were also electroformed by a negative voltage, but they could not be switched OFF, as illustrated by several OFF switching attempts in Fig. 6.13c. These devices were electrically shorted after experiencing a large current (~40 mA). Approximately 50 devices of each type were measured. The switchable device yield for the samples with either a 5 nm Ti or Cr adhesion layer was 98 %. In sharp contrast, the no adhesion layer device yield was less than 10 %.

The electrical results of these devices agree with the scenario that Ti or Cr can diffuse through the 15 nm bottom Pt electrode to react with the  $\text{TiO}_2$  at the bottom interface during hot deposition of  $\text{TiO}_2$  and form a locally reduced oxide, denoted as  $\text{TiO}_{2-x}$  (i.e., an oxide characterized by significant oxygen vacancies). We propose this diffusion creates the seeds for subsequent growth of conducting channels during the electroforming process, significantly improving the post-electroforming switchable device yield and reducing the device variance compared to the samples prepared with no adhesion layer. This asymmetric diffusion-created oxygen vacancy profile also dictates the switching polarity of the device: switching ON typically occurs by applying a negative bias and OFF via a positive bias on the top electrode, independent of the subsequent electroforming process [96].

As shown in Sect. 6.1, the device electronic transport can be understood by considering the asymmetry of the top and bottom metal/oxide interfaces. The top interface can be described by a Schottky-like barrier while the bottom interface is typically much more electrically conductive due to the diffusion-created oxygen vacancy dopants. During switching, the conductive bottom interface sees a much smaller electric field than the Schottky-like top interface does and thus remains essentially unchanged. Since Cr metal has a weaker reducing capability to  $\text{TiO}_2$  than Ti metal due to a smaller free energy of formation for the Cr oxide, it produces fewer vacancies at the bottom interface and a more resistive virgin state than the device with a Ti adhesion layer. The enthalpies of formation for  $\text{TiO}_2$  and  $\text{Cr}_2\text{O}_3$  are about 316 J/mole-atom and 226 J/mole-atom, respectively [97]. Therefore, Cr can reduce  $\text{TiO}_2$  to a certain Ti sub-oxide but not Ti metal. The device with no adhesion layer is the most resistive one in the virgin state because of the absence of oxygen vacancies created by the diffusion of an adhesion metal.

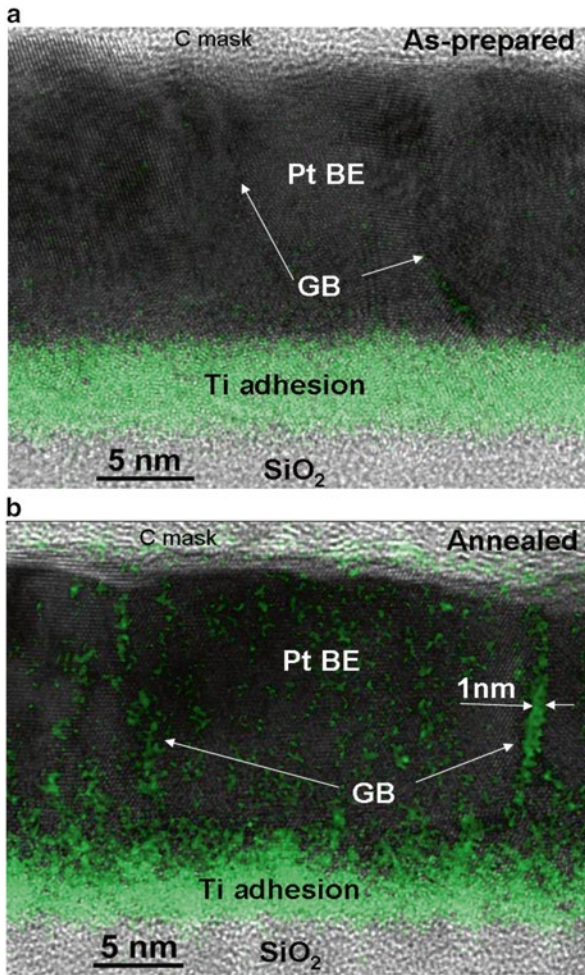
While the electrical results demonstrate the impact of the adhesion layer on the device properties, physical evidence is essential to confirm any diffusion of the adhesion metal. The interdiffusion of Ti and Pt layers has been studied over large areas at high temperatures of ~600 °C typical for ferroelectric device processing [98, 99], since this effect significantly degrades the electrical device properties in many cases [100]. We seek instead to understand diffusion effects with nanometer resolution for memristive Ti/Pt/oxide devices processed at low temperatures 150–250 °C, and thereby better exploit these effects to control and improve the performance of nanoscale memristive switches.



**Fig. 6.14** XPS spectra of Si/SiO<sub>2</sub>/5 nm Ti/15 nm Pt in the as-prepared, post 150 °C annealed and post 250 °C annealed states. The photoemission peak from Pt 4p 3/2 at 520 eV suggests a metallic Pt before and after annealing. The annealing was done in-situ in the XPS UHV chamber. The small amount oxygen adsorbed at the Pt surface disappeared after annealing. Ti 2p peaks started to be visible after 1 h annealing at 150 °C and became significant after 1 h annealing at 250 °C. The energy of Ti peaks corresponds to Ti with some degree of oxidation (Copyright Wiley-VCH Verlag GmbH & Co. KGaA. Reproduced with permission)

As a final experiment to corroborate the above points, X-ray photoelectron spectroscopy (XPS) combined with ultra-high vacuum (UHV) sample annealing showed the appearance of buried adhesion layer Ti on top of an upper Pt film after annealing. A 5 nm thick Ti and then a 15 nm thick Pt films were evaporated on a Si/SiO<sub>2</sub> substrate. The sample was then transferred into an XPS chamber equipped with in-situ annealing capability. In the annealing process, the temperature was set to ramp up in 10 min, remain at the annealing temperature for 20 min and cool down in 30 min, duplicating as closely as possible the temperature conditions experienced by the Ti/Pt bottom electrode during TiO<sub>2</sub> sputtering for memristive device fabrication. XPS spectra shown in Fig. 6.14 were collected before and after in-situ annealing at different temperatures. The photoemission peak from Pt 4p<sub>3/2</sub> at 520 eV corresponds to metallic Pt before and after annealing. The small amount of adsorbed oxygen on the Pt surface disappeared after annealing. No Ti peak was seen on the as-prepared sample. However, the Ti 2p peaks were visible after annealing at 150 °C, indicating diffusion of the Ti adhesion layer through the 15 nm Pt layer. Further annealing of the sample at 250 °C resulted in a significant diffusion of Ti, as evidenced by the intense Ti 2p peaks. The binding energy of the Ti peaks (2p<sub>3/2</sub> at 456 eV and 2p<sub>1/2</sub> at 460 eV) corresponds to Ti with some higher oxidation state, rather than metallic Ti.

Atomic level mapping of the diffused Ti via transmission electron microscopy (TEM) confirms inhomogeneous grain-boundary mediated diffusion of the Ti through the Pt electrode. In order to unambiguously identify the source of the diffused Ti



**Fig. 6.15** EFTEM maps of Ti overlaid on HTEM images for the as-prepared (a) and 250 °C 1 h UHV in-situ annealed (b) samples. The sample structure was Si/SiO<sub>2</sub> 100 nm/Ti 5 nm/Pt 15 nm and the C mask for TEM sample preparation with Focused ion beam (FIB) can also be seen on top of the Pt layer. The 5 nm Ti layer diffused through the Pt grain boundaries (GBs) after annealing. The width of the diffused Ti atom channels is about 0.5–1 nm (Copyright Wiley-VCH Verlag GmbH & Co. KGaA. Reproduced with permission)

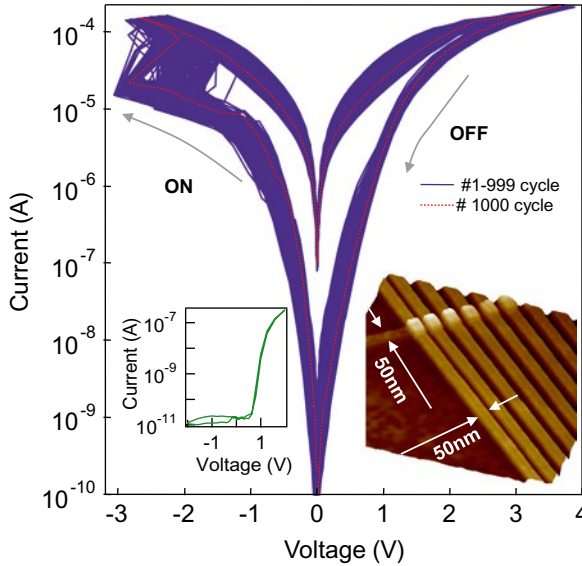
atoms in the TEM sample, the Ti/Pt bottom electrode was annealed without sputtering TiO<sub>2</sub> on top of it. Cross-sectional energy-filtered transmission electron microscopy (EF-TEM) characterization was carried out for both as-prepared and 250 °C annealed samples. Similar to electron energy loss spectroscopy (EELS), EF-TEM filters transmitted electrons by energy, enabling chemical selectivity when the energy filter is modulated near a strongly absorbing element-specific ionization energy. EF-TEM maps were overlaid on high resolution TEM (HR-TEM) images shown in Fig. 6.15, where the dots represent the Ti-specific signal. As expected, the

15 nm Pt is a polycrystalline film with grain boundaries (GBs) visible in the HRTEM images. The grain size of the ambient temperature e-beam evaporated thin Pt layer (15–30 nm) is typically 5–10 nm. For the as-prepared Ti/Pt bi-layer shown in Fig. 6.15a, the 5 nm Ti layer is uniformly distributed under the Pt layer with almost no Ti observed in the Pt layer. In sharp contrast, after annealing at 250 °C the thickness of the Ti adhesion layer is significantly reduced and many channels consisting of Ti are seen along the GBs of the Pt layer (Fig. 6.15b). GB diffusion is typically 4–8 orders of magnitude faster than volume diffusion depending on the temperature, primarily due to the difference in the diffusion activation energies [101–103]. This results in nanoscale channels of diffused Ti atoms, which are about 0.5–1 nm in diameter in Fig. 6.15b, consistent with GB width in diffusion theory [104].

The fact that the Ti channels are as small as ~1 nm in diameter makes thermal diffusion a very interesting approach for engineering the switching seed creation. The reasons are twofold: (1) this approach remains effective when the devices are scaled down to a few nanometers and (2) ultra-small switching channels consume ultra-low power for switching operations. The density of the switching channel seeds may be manipulated by varying the grain size and thus density of grain boundaries in the Pt layer (or other bottom electrode material). Deposition conditions can control the grain size of a pure Pt layer to some degree. The grain size can also be efficiently controlled by co-depositing a second element [105]. Direct lithographic patterning of the Ti adhesion layer would offer control over the switching site position. Selection of the adhesion layer material and annealing parameters further offers a large parameter space for device optimization, which may eventually lead to electroforming-free devices.

Engineered nanodevices validate the switching seed creation approach. Junctions of area  $50 \times 50 \text{ nm}^2$  and a nominal structure of Si/SiO<sub>2</sub> (100 nm)/Ti (2 nm)/Pt (9 nm)/TiO<sub>2</sub> (40 nm)/Pt (11 nm) were fabricated by nanoimprint lithography. Ti metal from the underlying 2 nm Ti layer was diffused through the 9 nm Pt bottom electrode during the hot deposition of the TiO<sub>2</sub> layer at 250 °C. The electrical measurement results are given in Fig. 6.16, where 1,000 consecutive switching *I*–*V* loops were obtained with fixed ON and OFF switching voltage sweeps. After the 1000th switching loop (shown in dashed line in Fig. 6.16), no obvious degradation was observed and the ON/OFF conductance ratio remained  $\sim 10^3$ . The forming and switching voltages from device to device had narrow distributions with a spread of less than 1 V around their average values. A highly rectifying *I*–*V* curve was observed in the virgin state (inset) and the rectification direction and subsequent switching polarity both support the model of a top interface Schottky-like contact and a bottom interface Ohmic-like contact, consistent with the bottom interface heavily doped by Ti diffusion-created oxygen vacancies (VOs). These data highlight the unexpectedly important role that metal “adhesion layers” can play in these oxide switches, which needs to be well understood in some medium or high temperature processes, such as the integration of resistance switches in a CMOS process. This engineering control may be expected to scale to devices as small as a few nanometers without significant difficulty, and may also transfer to other nitride- or sulfide-based memristive devices.

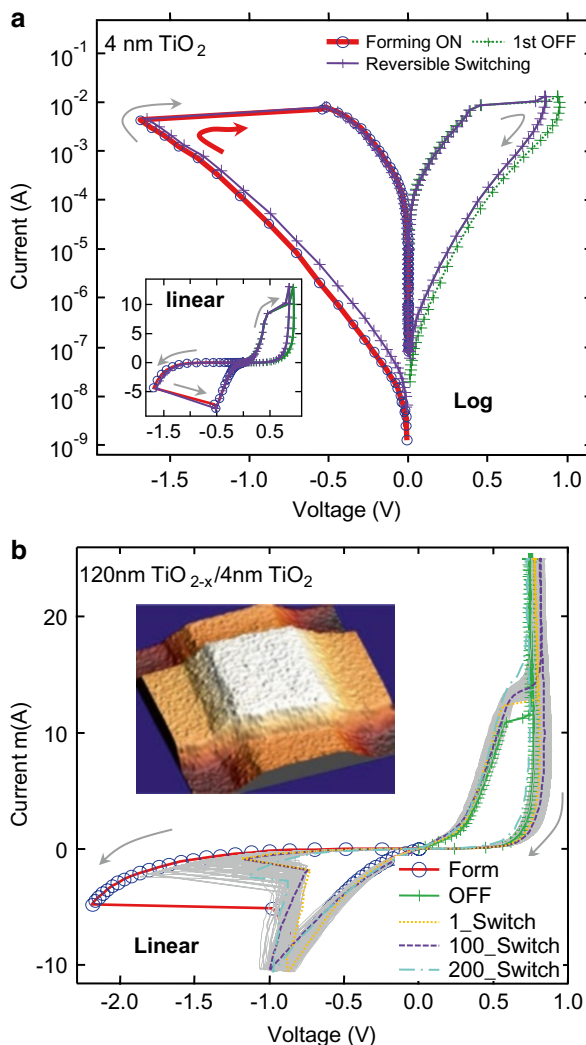




**Fig. 6.16** 1000 consecutive reversible bipolar non-volatile switching  $I$ - $V$  loops from an Si/SiO<sub>2</sub>/Ti (5 nm)/Pt (15 nm)/TiO<sub>2-x</sub> (40 nm)/Pt (30 nm) nano crosspoint device. OFF/ON resistance ratio remains about 10<sup>3</sup> and no obvious degradation is observed after the 1000th switching loop (*dotted line*). The *inset on right* presents the AFM image of 6 nano-junctions with the junction area of 50 nm×50 nm. The virgin state  $I$ - $V$  is highly rectified (*inset on left*) and this rectification orientation dictates the switching polarity of the junction. Voltages are applied on the top electrode and the bottom electrode is grounded for all these measurements (Copyright Wiley-VCH Verlag GmbH & Co. KGaA. Reproduced with permission)

### 6.4.3 Electroforming-Free Devices with a Bi-layer Oxide

The above grain-boundary-mediated thermal diffusion approach enables a well-controlled switching polarity, a high device yield and a small device variance. However, electroforming step is still required in those devices. The electroforming process with bubble formation is potentially destructive and certainly difficult to control. Technologically, it is desirable to eliminate this device variance for computer circuit applications. We have postulated that electroforming by either positive or negative voltage creates a conductance channel(s) through the bulk oxide film, and subsequent ON/OFF switching is concentrated at one or both interface regions. One approach to engineer a device that obviates electroforming is to thin the oxide film, eliminate the “bulk” region, and just keep the “switching interface.” Figure 6.17 shows  $I$ - $V$  data from such a device. The TiO<sub>2</sub> for this device is only 4 nm thick and the  $I$ - $V$  curve for the initial electroforming step is essentially identical to the  $I$ - $V$ s of subsequent reversible ON switching. Significantly, the resistances for both ON and OFF states are comparable to the previous devices with the thick TiO<sub>2</sub> layers—supporting the postulate that electroforming primarily creates conductance



**Fig. 6.17** Engineering the device to eliminate the need for electroforming. Thinning the  $\text{TiO}_2$  insulator to 4 nm and just keeping the key electrode/ $\text{TiO}_2$  “switching interface” reveals that the electroforming is primarily a process of creating conductance channels across the bulk in insulator. (a) A Pt/4 nm  $\text{TiO}_2$ /Pt device. The forming  $I$ - $V$  (thick solid lines with open circles) is essentially identical to the subsequent ON switching  $I$ - $V$  (solid lines with crosses). The shape and amplitude of conductance switching is comparable to those devices with much thicker  $\text{TiO}_2$  layers. (b) The data from a Pt/120 nm  $\text{TiO}_{2-x}$ /4 nm  $\text{TiO}_2$ /Pt devices, showing 200 consecutive switching loops after the forming step. The thick  $\text{TiO}_{2-x}$  is already highly reduced during device fabrication and thus no electroforming is needed; the key interface is again the electrode/ $\text{TiO}_2$ . Neither sample a nor b show detectable physical deformation by AFM (IOP Publishing Ltd)



channels across the bulk oxide film. However, the device with a 4 nm oxide exhibits an increasing conductance in both ON and OFF states with switching cycling, probably due to the lack of an oxygen reservoir for the reversible migration of oxygen ions and vacancies. To solve this problem and also further verify the electroforming mechanism, we added a highly reduced, i.e. conductive, but thick (120 nm)  $\text{TiO}_{2-x}$  layer to otherwise identical 4 nm  $\text{TiO}_2$  devices during the fabrication process and found that the electroforming process in this new device with thick oxide is also eliminated. As shown in Fig. 6.17b, there is no obvious degradation observed in the device after 200 consecutive switching cycles. No detectable physical deformation can be seen by AFM in the device after electrical forming and switching either. Fine-tuning the thickness and composition of the reduced layer is of utmost importance for realistic device applications, since the selected thickness of 120 nm is prohibitively thick. Future experiments demonstrate that moderate thickness reproduces the desired behavior for an optimal stoichiometry.

## 6.5 Section 5: Summary

In this chapter, we have addressed several issues regarding oxide based memristive nanodevices, including the switching mechanism, the electroforming mechanism, the device engineering, and a family of memristive devices. The switching mechanism involves changes to the electronic barrier at the Pt/ $\text{TiO}_2$  interface due to the drift of positively charged oxygen vacancies under an applied electric field. Vacancy drift towards the interface creates conducting channels that shunt, or short-circuit, the electronic barrier to switch ON. The drift of vacancies away from the interface annihilates such channels, recovering the electronic barrier to switch OFF. The electroforming in a metal/oxide/metal switch is an electro-reduction process caused by electric field enhanced by Joule heating. The electroforming deformation in the junction is reduced to an undetectable level by shrinking the junction size to nanoscale. The forming process is essentially eliminated by using a thin oxide layer in the device. The device properties can be well controlled by engineering the devices. The understanding of these fundamental mechanisms enables a class of reconfigurable two-terminal electronic circuit elements behaving as networks of memristive switches and rectifiers in parallel and series combinations, which are based on the physical properties of a metal/oxide/metal system. These novel devices will enhance the toolkit of circuit designers and allow new nanoelectronic architectures for a variety of applications, including memory, logic, synaptic, and other circuits.

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# **Part III**

## **Probe Memories**

# Chapter 7

## Ferroelectric Probe Storage Devices

Seunghum Hong and Yunseok Kim

### 7.1 Introduction

An information storage device is a gadget that has a probe head and a medium, and uses them as means for recording (write) and retrieving (read) information (see Fig. 7.1).

As the world gets more and more connected and linked, the amount of information flow will drastically increase, which boosts the demand for storage devices. For example, people are using smartphones not only to make a phone call but also to take pictures, surf various web sites, watch movies, and write emails to name a few.

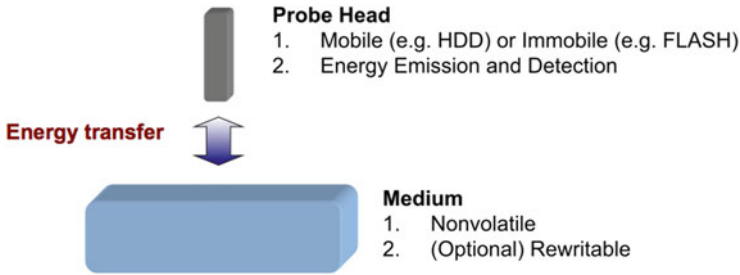
Then, why do we need to store more information in our gadgets? Is it not sufficient to use storage devices with current capacity for such gadgets? The answer to this question can be found by looking at the trends of necessary amount of information in four areas: display, medical, financial, and security information.

As the technology developed, the display device has evolved from black and white to color, and to 3D. It can be easily found that the amount of information needed to display 3D images is orders of magnitude larger than that for color images. For medical information, people are more interested in customized medication based on their own gene information and personal health history with all X-ray and MRI images included, which would need about 4 exabytes (EB) ( $4 \times 10^9$  GB) [1]. Another important trend can be found in financial sector, where people want to

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**Fig. 7.1** Schematic of an information storage device, which mainly consists of a probe head and a medium

**Table 7.1** Terminologies used for describing storage capacity in increasing order and their magnitudes

Storage capacity units	Equivalent storage capacity
1 TB (Terabyte)	1,000 GB (Gigabyte)
1 PB (Petabyte)	1,000 TB
1 EB (Exabyte)	1,000 PB
1 ZB (Zetabyte)	1,000 EB

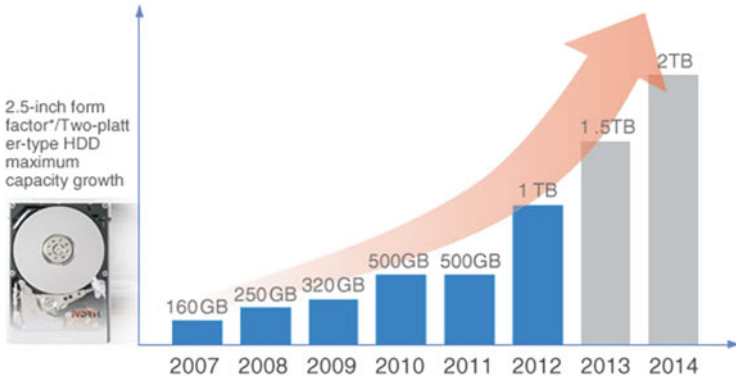
have customized financial advice based on their personal banking and investment history. For safety and security reasons, more and more surveillance cameras are being installed in major cities with better resolution, which drastically increase the demand for storage capacity.

In parallel with the increasing demands to store more information in our gadgets, the available information increases exponentially as well. The information floating on the Internet is estimated to be more than 530 PB [1]. The telephone calls worldwide produce information about 17.3 EB per year. New information produced by print, film, magnetic, and optical storage media is roughly 5 EB per year (see Table 7.1 for the storage capacity units) [1].

The driving force to meet the ever-increasing demands for more information and supplies of such information has pushed the capacity of mobile HDD from 160 GB in 2007 to 1 TB in 2012 as shown in Fig. 7.2 [2].

## 7.2 Principle and History of Information Storage Devices

In order to develop new technology to meet the needs of the end users, one has to think about the right science that he or she can apply to realize the technology. Surprisingly one can find the common science and technology implemented in various mechanically addressable storage devices from the example of a note-taking process.



**Fig. 7.2** Roadmap of mobile HDD embedded in laptops. Reprinted with permission from iVDR [2]

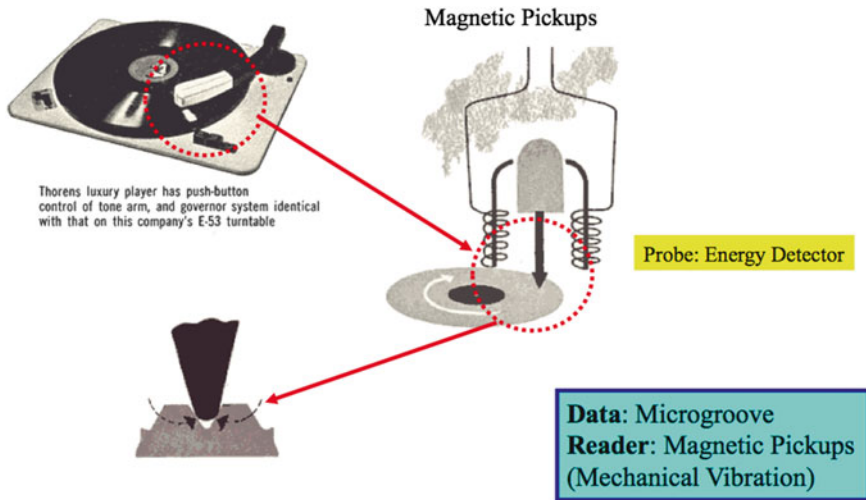
**Fig. 7.3** Schematic of note-taking process, where the pen is the information writer and the human eye is the reader



As shown in Fig. 7.3, when we take a note during a lecture or a seminar, the pen becomes the writer and deposits inks on the notebook in the form of characters that encode information transmissible to people who use the same character set. The eyes become the reader and our brains decode the image of characters into meaningful words that form sentences conveying the message recorded on the notebook.

Two important activities involved in this note-taking process are (1) locating the place to write the characters and (2) finding the place where to read. This process is similar to servo and tracking of information in HDD or ODD. We use indentations or tabs to mark the first sentence of each paragraph and align each sentence vertically with the lines preformatted in our notebook (Y marker in Fig. 7.3), and use either the edge of the notebook or additional vertical line (X marker in Fig. 7.3) as



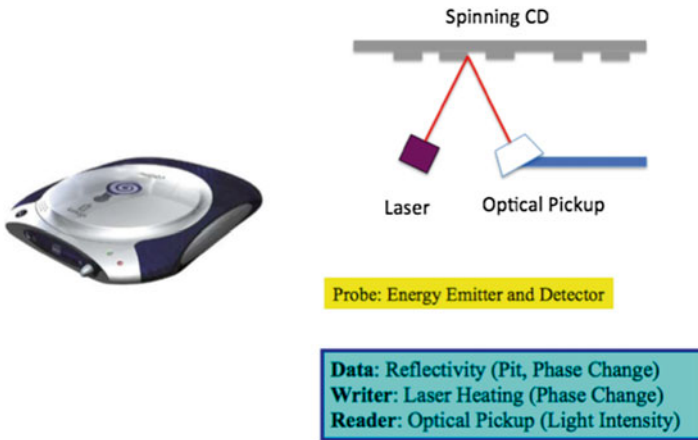


**Fig. 7.4** Schematic diagram of phonograph, which has a magnetic pickup as the information reader. In the case of LP turntable, the microgroove acts as the information that contains the music, and the mechanical vibration of the pickup is detected by the inductive current

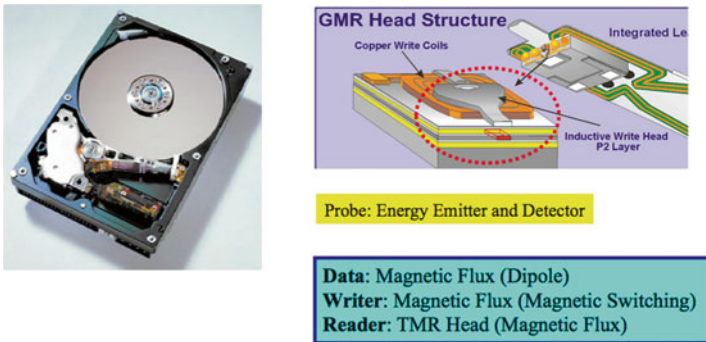
the reference to which we start our sentences. Likewise, when we want to find a specific sentence, we first identify the position by saying, e.g. the third line of the second paragraph. In this particular case, our eyes will quickly count the number of tabs of each paragraph from the top and locate the third line by counting again the number of lines from the top of the second paragraph.

We can learn more common science and technology embedded in mechanically addressable storage devices, or say probe storage devices by studying the prototypical turntables, optical disk drives, and hard disk drives. They all have similar mechanical structures when one considers the shape of media being circular, and the head moving in or close to the radial direction. The information is recorded sequentially along either one track or multiple tracks in the form of micron-size grooves for turntable, bits with different optical reflectivity using different phases for DVDs [3], and magnetic domains with different magnetization directions for HDDs. As such, the writing process would be imprinting the physical grooves for turntables (see Fig. 7.4), heating with laser source at different temperature and duration for DVDs (see Fig. 7.5) and applying focused magnetic fields with different polarity and duration for HDDs (see Fig. 7.6) whereas the reading process would be detecting the height of the grooves using magnetic transducers or piezoelectric transducers for turntables (see Fig. 7.4), detecting the intensity of reflected laser beam for DVDs (see Fig. 7.5) and measuring the current amount passing through magnetoresistance device which has different resistance depending on the direction of magnetic field emanating from the HDD media (see Fig. 7.6) [19, 20].

Moreover, the heads are located in the arm that has a balance mass on the opposite side of the pivot, which absorbs the lateral vibration and shock. Therefore, if one can conceive of a physical mechanism to write and read information using different



**Fig. 7.5** Image of DVD player and schematic diagrams of the media and the optical pickup. The optical head has a laser source that heats the media locally to induce a phase change, which can be detected by the laser reflected from the bit [3]

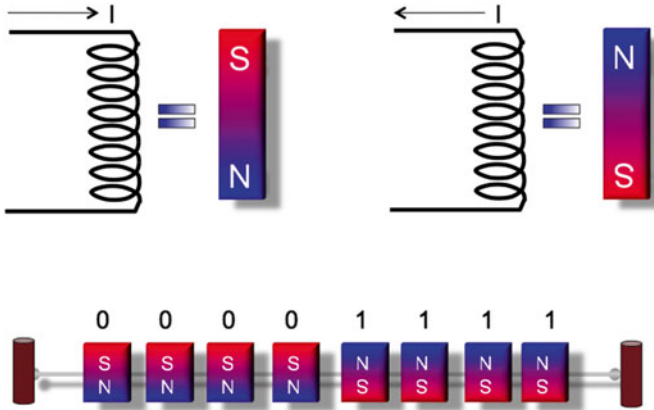


**Fig. 7.6** Image of a hard disk drive (HDD) along with a schematic of a HDD head composed of inductive copper write coils and giant magnetoresistance (GMR) reader. Courtesy of International Business Machines Corporation, ©2014 International Business Machines Corporation

transduction scheme, e.g. writing with electric field and reading back with a resistance change induced by electric field, then one can invent a new recording system based on the mechanically addressable framework.

### 7.3 Understanding Key Processes of Information Storage

In order to come up with a novel idea to increase the density and speed of information storage, one has to think about the key processes that govern the writing and reading of information in the device. Here we present three distinct processes that

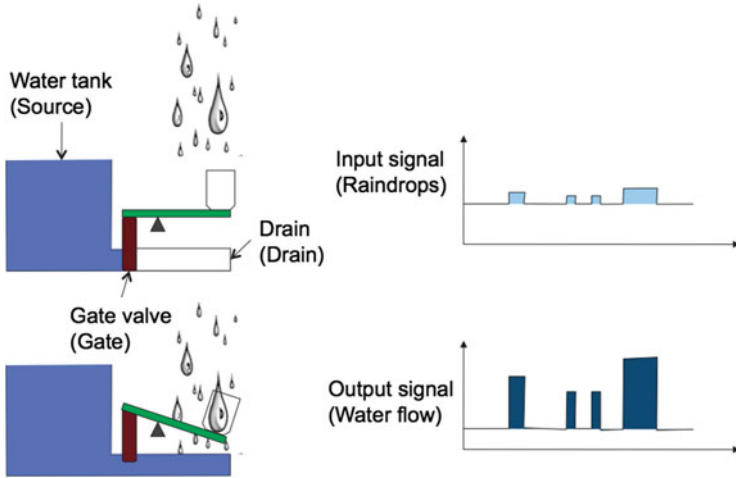


**Fig. 7.7** Schematic drawings of writer coils with current flowing from top to bottom (*left upper*) and current flowing from bottom to top (*right upper*)

are important to construct an information storage device. The first process is designing the writer with a transduction mechanism from electrical energy into magnetic energy in the case of HDD. Figure 7.7 shows the schematic representation of induction coils embedded in the HDD head that are equivalent of permanent magnets with opposite direction depending on the flow of current through the coil. The media can be envisioned as a row of magnets threaded through a string that hold those small magnets, which store the information bit by bit, and as the HDD head travel above each bit and exert magnetic field, the bit either flip or stay depending on the polarity of the head.

From Fig. 7.7, one can immediately understand the limitation of writing with induction coil. The speed of writing depends on how fast you can flow the current through the coil, and any damping in the circuit will impede the process. Moreover, any heat loss due to the joule heating of the coil will increase the power consumption of the magnetic write head. Therefore, spin or charge injection could be a faster write mechanism for future storage devices [18].

The second process is the amplification process of the read signal. As depicted in Fig. 7.8, we can understand the process with a cartoon of water tank equipped with a gate valve that opens upon the impingement of raindrops collected by a cup connected to the valve. People usually get confused about the concept of amplification, as it seems to violate the law of energy conservation. How can one design a device where the output energy is bigger than the input energy? In fact, we cannot violate the law of energy conservation, and we can only amplify signals using two independent stream of energy (or material) flow that are connected via three terminals called source, gate, and drain. As depicted in Fig. 7.8, the amount of water contained in one raindrop is very small, therefore the input signal is very small. However, as the signal defined by the change of flow can be manipulated by a lever connected to a gate valve that regulates the water flow from the tank, the signal can be amplified by orders of magnitude as shown in the output signal plot in Fig. 7.8.

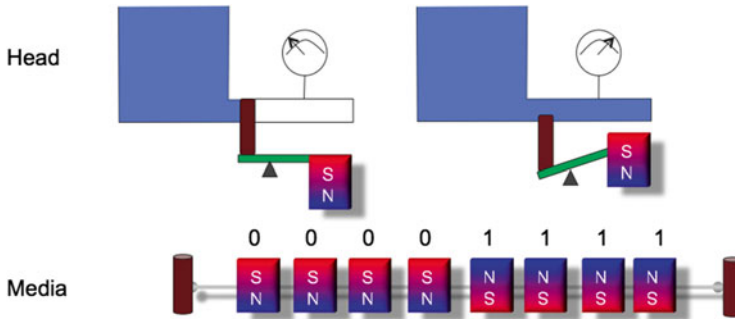


**Fig. 7.8** Schematic diagrams of signal amplification mechanism. The tank filled with water acts as a source of signal, and the gate valve connected to the cup via a lever supported by a pivot acts as the gate for the signal. Output signal in terms of water flow through the channel will replicate the raindrops collected in the cup with much amplified strength

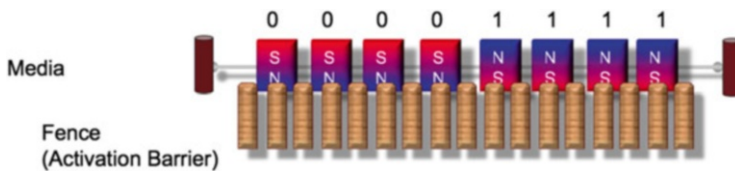
Therefore, it is important to invent a mechanism where the small field emanating from the information bit can trigger a large flow of current through a gate opened and closed by the field. One such a mechanism is magnetoresistance, where the stray magnetic field from the magnetic domain can either increase or decrease the resistance between the source and drain terminals of the giant or tunneling magnetoresistance devices as depicted in Fig. 7.9. The mechanism shown in Fig. 7.9 illustrates an example where the magnetic force is converted to mechanical force acting on the gate of the water tank. However, in reality, it is the magnetic force acting on the spins of the gate that increases or decreases the resistance of electrons with specific directions that flow through the tunnel junctions.

The last but not the least key component of information storage devices is the retention properties of written information. If the recorded data is not stable against environment, then the consumers cannot reliably use the device. Therefore, one has to make sure that each information bit has a proper barrier against flipping to the other state by thermal energy. Figure 7.10 depicts this idea by putting a fence or an activation barrier in the vicinity of the written information. One immediately sees a conflict here. If one wants to write the information easily, the fence should be low whereas if one wants to keep them stable against external perturbation, the fence should be high.

People have come up with an idea of raising the fence and increasing the writing energy. One way to accomplish this is to use both magnetic and heat energies when writing the bits, which is called heat-assisted magnetic recording (HAMR). However, this combined usage of two different energy sources complicates the device design. It should be noted that three major HDD companies have developed



**Fig. 7.9** Schematic diagram of reading process in hard disk drives where the polarity of dipole moments encoded as information bits can either open or close the gate valves to amplify the read signals



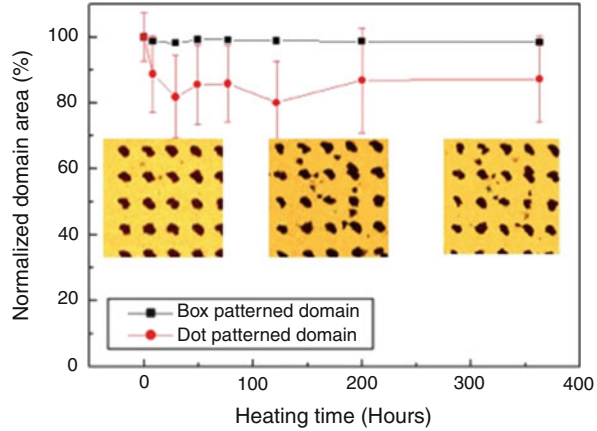
**Fig. 7.10** Schematic diagram of written information bits with an activation barrier that keep the bits stable against thermal energy

HAMR technology that can be implemented in 2016 [4, 5]. Others have come up with the patterned media where they can increase the signal to noise ratio by increasing the change between the information bits [6]. However, mass production of regularly aligned nanoscale bits is a big challenge in the industry.

## 7.4 Ferroelectric Materials as Storage Media

Fong et al. at Argonne National Laboratory have published a seminal work on the size limit of periodic stripe domains in  $\text{PbTiO}_3$  thin films grown epitaxially on  $\text{SrTiO}_3$  substrates [7]. They have found that down to three unit cells, one can sustain ferroelectricity at room temperature. As the domain size scales with the thickness of the film, this would mean that one can write information within a diameter less than a few nanometers leading to potential bit density larger than 10 terabits/in.<sup>2</sup> [8]. Regarding the thermal stability of written bits, Woo et al. have found that fully penetrated domains can retain its state [9], and Kim et al. have shown that so written bits can withstand the thermal energy at 200 °C for over 350 h as shown in Fig. 7.11, which translates into more than 10 years of retention even at 85 °C based on the assumption of thermally activated process with activation barrier of about 1 eV [10, 21].

**Fig. 7.11** Normalized area of written information (black dots) on ferroelectric thin films as a function of elapsed time at 200 °C. The sample was imaged using piezoresponse force microscopy (PFM) at each time



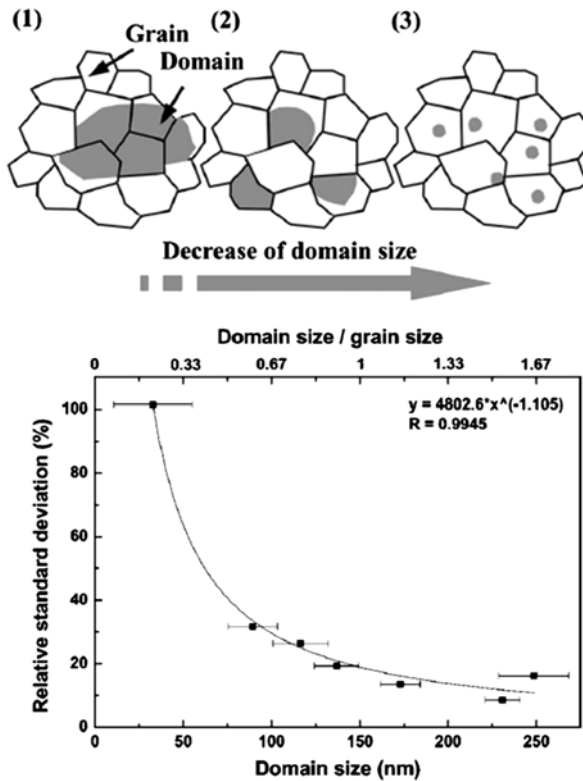
Another issue that should be identified is the uniformity in the size of bits written under the same condition. It has been known for a long time that the grain boundary interacts strongly with domain boundaries to influence the size of the domain written by the electric field from the probe head. In order to minimize such fluctuations, Kim et al. have explored the relationship between the grain size and the domain size and its fluctuation as shown in Fig. 7.12 [11]. They found that reducing the grain size, which is the same approach taken in the HDD industry for ferromagnetic media, will lead to higher uniformity in the bit size written under the same voltage magnitude and duration.

Therefore, so-called nano-grain ferroelectric media were initiated and developed by Buehmann et al., where he and his colleagues found that  $\text{TiO}_2$  thin films can be deposited to thickness below 10 nm in a continuous form, and by converting the film to  $\text{PbTiO}_3$  through gas phase reaction with  $\text{PbO}$ , they could obtain ferroelectric media with grain size below 5 nm as shown in Fig. 7.13 [12–14].

## 7.5 Ferroelectric Hard Disk Drive

One of the biggest challenges of ferroelectric probe storage device based on micro-electromechanical system (MEMS) is the wear of the probe [22]. As can be seen in Fig. 7.14a, the wear volume depends on the load we apply to the tip and the wear coefficient between the tip and the ferroelectric media among other factors. Figure 7.14b shows the scanning electron microscopy (SEM) images of the resistive tip before and after 10 mm sliding in contact mode with load of 17 nN and in tapping mode. One can clearly see the wear of the tip that leads to a significant change in the radius of the tip when operating in contact mode whereas such a wear is minimized when the tip is not in direct contact with the media surface.

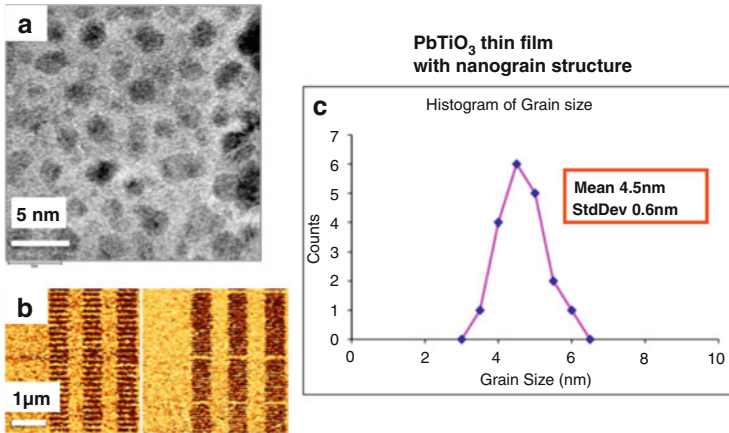
As such Hong et al. developed a concept of ferroelectric hard disk drive based on the resistive probe developed before [15], which utilizes the design of air-bearing



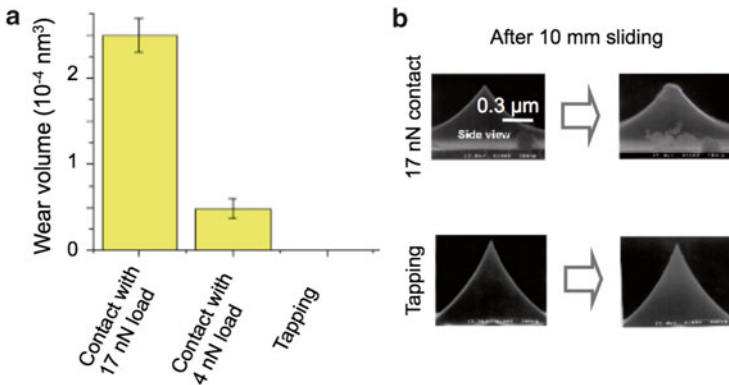
**Fig. 7.12** Schematic diagram of overlapped images of written domains and grain structure in polycrystalline ferroelectric media. The grain boundary interacts with the domain to increase the standard deviation of the size of the written domains as depicted in the graph of relative standard deviation of domain size vs. domain size/grain size (or domain size). Reproduced with permission from Appl. Phys. Lett. [11]. Copyright 2006, AIP Publishing LLC

slider to maintain an air-gap of about 8 nm between the head and the media. In order to realize this concept, there are three imminent challenges that need to be addressed. Firstly, one should design a method to write ferroelectric domains even when there is a significant voltage drop across the air-gap. Secondly, the slider materials of AITC used for magnetic HDD should be changed into Si to embed field effect transistor as the information reader. Thirdly, one should develop ferroelectric media based on a HDD platter in a doughnut shape (Fig. 7.15).

Hong et al. combined the front-end process of fabricating the resistive channel and conducting writer on a silicon wafer using a standard nanofabrication process and the assembly of sliders in a standard HDD head fabrication process as shown in Fig. 7.16 [15]. One can clearly see the boundary in the center region of the top-view optical microscopy image of the slider, which was created by the wafer bonding process.



**Fig. 7.13** (a) Transmission electron microscopy (TEM) image of PbTiO<sub>3</sub> thin film nanograin media, and (b) PFM phase images of written domains with line spacing of (left) 75 nm and (right) 38 nm. The pattern was written at voltages of ±3 V. (c) Histogram of the grain size measured from (a)

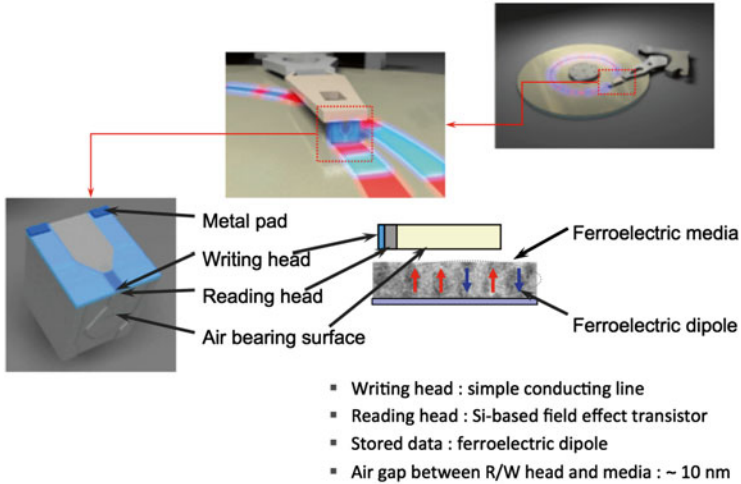


**Fig. 7.14** (a) Plot of wear volume when operating at contact mode with load of 17 nN and 4 nN and tapping mode. (b) Scanning electron microscopy (SEM) images of the resistive tip after 10 mm sliding in contact mode with load of 17 nN and in tapping mode

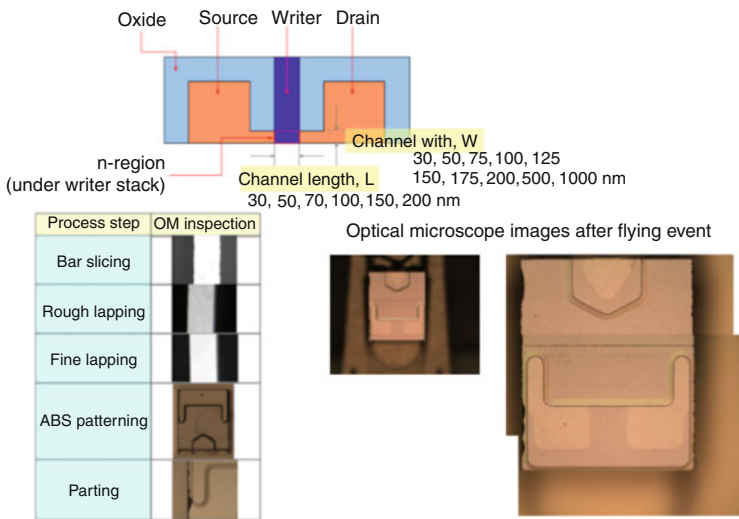
The slider showed no debris attached to it after the flying test as seen in the optical microscope image. The acoustic sensor detected no sound, which indicates that our newly developed slider could fly above the media rotating at 7,200 rpm. With our fabrication process, we could address the challenges of fabricating the head using silicon instead of AlTiC.

The first and third challenges we discussed were addressed by conducting a model experiment using atomic force microscopy as well as performing the prototype experiment using the HDD head and ferroelectric media, which was polished to have less than 0.5 nm roughness using chemical–mechanical polishing (CMP)

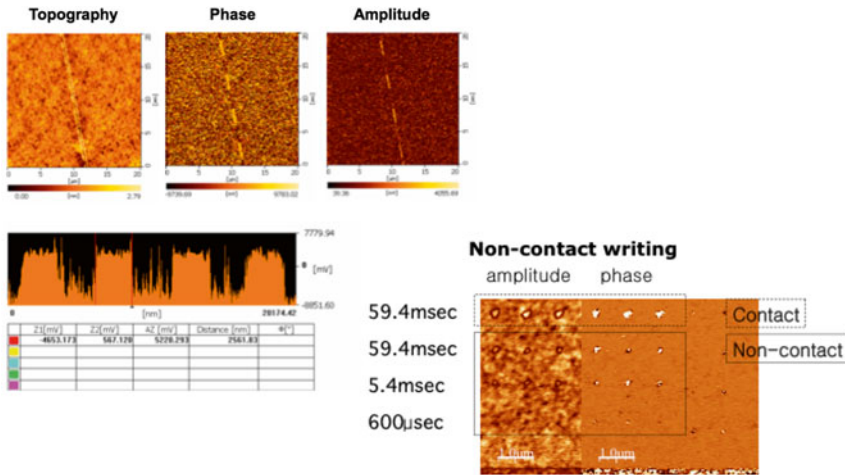




**Fig. 7.15** Schematic diagrams of ferroelectric hard disk drive (FE-HDD). The head consists of a metal pad as the writer and a resistive channel as the reader. The air-gap between the head and media is about 8–10 nm, which is sustained by the airflow under the air-bearing surface. The media is ferroelectric thin film deposited on a silicon wafer diced to fit the HDD platform



**Fig. 7.16** Schematic diagram of the front view of FE-HDD head (top) and the processing sequence of head assembly (left bottom). Optical microscopy image of bottom view of FE-HDD head showing the air bearing surface (right bottom)



The size of switched domains is smaller for non-contact mode than contact mode.

**Fig. 7.17** Topography, and PFM phase and amplitude images of a written track using a HDD head with bias voltage pulses of +10 and -10 V. Line profile along the track clearly shows the written ferroelectric domains. A comparative study using PFM shows that the bits formed in non-contact mode are smaller in size when compared to those formed in contact mode

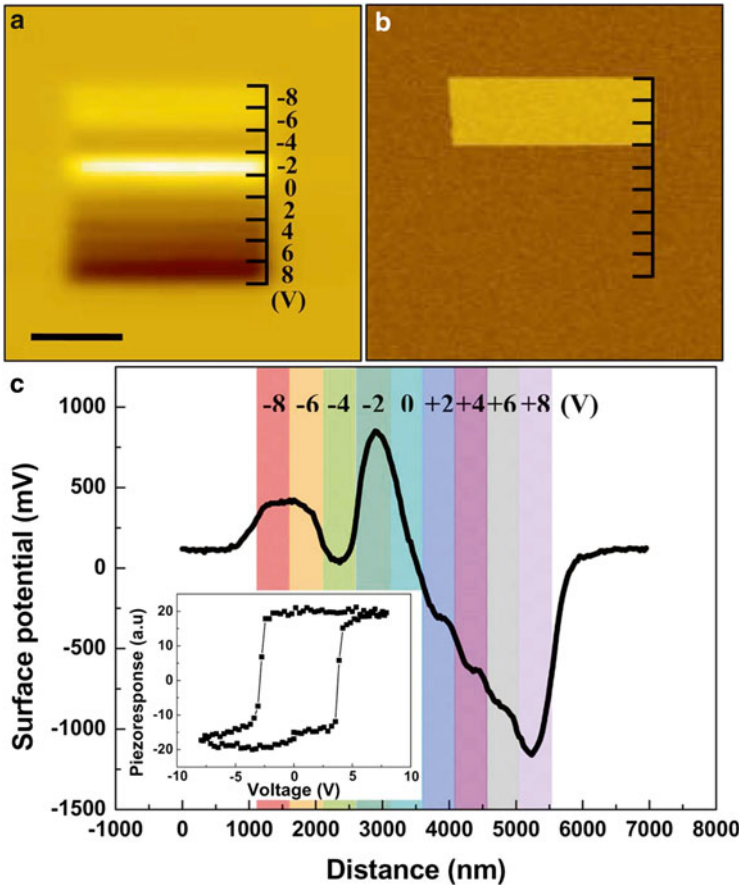
process (see Fig. 7.17). We used laser-dicing method to make a hole in the center of the ferroelectric media.

We confirmed that the HDD head could be used as a writer through which we apply bias voltage pulses of opposite polarities (+10 and -10 V) and write alternating ferroelectric domain patterns without damage to the surface of ferroelectric media as shown in Fig. 7.17. Furthermore, we compared the bit size of ferroelectric domains written by a biased AFM tip using the same duration of 59.4 ms using contact and non-contact tapping modes. As evident in the PFM phase images, the bit size is slightly smaller when written in non-contact mode than that written in contact mode.

Using PFM and Kelvin probe force microscopy (KPFM), Kim et al. found that the writing process consists of charge injection through the air-gap and polarization switching induced by the electric field exerted by the accumulated charges as shown in Fig. 7.18 [16]. This finding can explain the reason why we could write the domains even though we have an air-gap of 10 nm between the head and the media. The air-gap acts as tunneling barrier where the charges can flow as in the case of alumina capped ferroelectric thin films [17].

## 7.6 Conclusion

We have reviewed briefly the history of probe storage devices consisting of a probe and a medium, where the probe emits energy to the medium to write and read information and the medium store the information. The needs for ever-increasing



**Fig. 7.18** (a) KPFM surface potential distribution and (b) PFM phase image of the area scanned with the applied voltage biases from  $-8$  to  $8$  V with a  $2$  V step (*from top to bottom*) to the bottom electrode. The black scale bar presents  $2 \mu\text{m}$ . (c) Surface potential line profile obtained from (a). The *inset* shows piezoresponse hysteresis loop of PTO thin films. Reproduced with permission from Appl. Phys. Lett. [16]. Copyright 2009, AIP Publishing LLC

information storage density in the mobile gadgets have driven the research and development of probe storage devices to find read/write mechanism that can scale down to nanometer scale other than existing HDDs and ODDs as they are approaching their storage density limits. We proposed the ferroelectric materials as one of the candidates for media with very high information storage density, as the ferroelectric domain could be as small as a few unit cells or  $1.2$  nm in size. We showed that the writer is a simple conductor and the reader can be designed in the form of field effect transistors [23]. We envision that well-established hard disk drive system or newly developed micro-electromechanical system (MEMS) can be the candidates for realizing the ferroelectric probe storage device.

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