CHAPTER 5

3D Vertical NAND

Now, welcome to the exciting world of 3D vertical NAND! In this chapter, we will cover a cutting-edge technology that has revolutionized the way we store data. 3D vertical NAND is a remarkable advancement in NAND flash memory, allowing us to stack memory cells vertically to increase storage capacity and performance significantly.

You might be wondering how this technology works and what makes it so special. We will walk through the basics of 3D vertical NAND, explaining its unique architecture and how it overcomes the limitations of traditional 2D planar NAND. You'll discover the advantages and benefits of this innovative technology, along with its real-world applications and the impact it has on various industries.

By the end of this chapter, you will have a clear understanding of how 3D vertical NAND works and how it has transformed data storage, making it a technology crucial to modern electronic devices. So, let's dive in and explore the fascinating world of 3D vertical NAND!

Evolution of 3D Vertical NAND Technology

The rapid growth in data traffic globally is pushing the boundaries of NAND flash memory technology. The industry-standard 2D planar NAND technology has inherent limitations when it comes to expanding storage capacity without compromising performance and reliability. This has created a need for innovative solutions to meet the increasing demands for data storage.

G. Kuppan Thirumalai, *A Beginner's Guide to SSD Firmware*,
https://doi.org/10.1007/978-1-4842-9888-6_5

To address these challenges, the industry has introduced a groundbreaking approach known as 3D vertical NAND (V-NAND) flash memory technology. This innovation has revolutionized the design and architecture of NAND flash memory by stacking memory cells vertically in a three-dimensional structure, as opposed to the traditional two-dimensional planar arrangement. This vertical stacking allows for the creation of multiple layers of memory cells, resulting in significantly higher memory capacities (Figure 5-1).

By adopting a 3D V-NAND structure, the industry has overcome the limitations associated with capacity expansion in 2D planar NAND technology. This vertical stacking not only enables higher storage densities but also eliminates performance and reliability issues caused by capacity constraints. With more memory cells packed into each chip, the industry has achieved remarkable advancements in storage capacity while maintaining or even enhancing performance and reliability characteristics.

The vertical stacking of memory cells in 3D V-NAND technology offers several advantages. First, it allows for increased memory capacity within a smaller physical footprint, which is particularly beneficial in applications where space is a constraint. Additionally, the three-dimensional structure enables better control of electrical properties, resulting in improved performance and endurance.

This innovation in flash memory technology has had a significant impact on the storage industry, enabling the development of high-capacity solid-state drives (SSDs) that can handle the ever-growing volumes of data. The adoption of 3D V-NAND technology has facilitated advancements in areas such as cloud computing, data centers, mobile devices, and other storage-intensive applications.

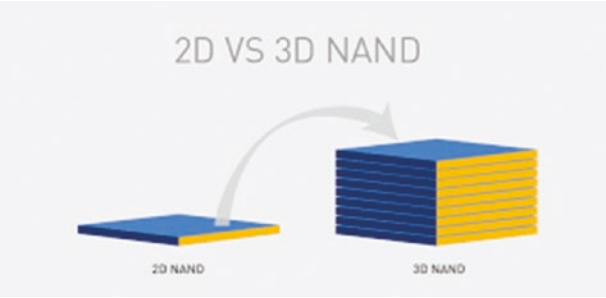

Figure 5-1. *2D vs. 3D NAND comparison block diagram*

Unlocking New Possibilities with Vertical NAND Architecture

Figure 5-2 compares the storage density of 2D planar NAND and 3D V-NAND flash memory. As shown, 3D V-NAND can achieve up to 10x greater storage density than 2D planar NAND. This is because 3D V-NAND stacks memory cells vertically on top of each other, while 2D planar NAND stacks memory cells horizontally on a silicon wafer.

The higher storage density of 3D V-NAND allows for larger capacity NAND chips to be produced. This has made it possible to create NAND flash memory devices such as solid-state drives (SSDs) and USB flash drives with capacities of several terabytes.

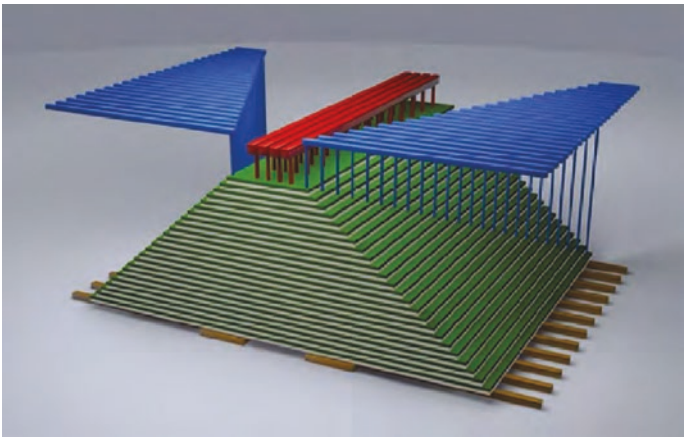

Figure 5-2. *Bird's-eye view of the V-NAND structure*

In the pursuit of fitting more memory cells into a smaller space, the limitations of 2D planar NAND flash memory become evident. The shrinking size makes it challenging for light to penetrate the mask and transfer the desired pattern onto the photoresist, ultimately hindering the patterning process. This inherent limitation restricts the widespread use of 2D planar NAND flash memory in today's demanding memory landscape.

However, 3D V-NAND overcomes these patterning limitations by adopting a vertical architecture. Unlike the close proximity of cells in 2D planar NAND, 3D V-NAND creates a wider gap between each cell, enabling efficient patterning. While the cell-to-cell spacing in traditional planar NAND typically ranges from 15 to 16 nanometers (nm), 3D V-NAND offers an impressive 30nm to 40nm of space between cells, revolutionizing NAND flash technology.

This vertical architecture has opened new doors for memory advancement, allowing for higher capacities and enhanced performance. By overcoming the constraints of patterning, 3D V-NAND flash memory has become a game-changer in the industry, meeting the demands of today's memory-intensive applications.

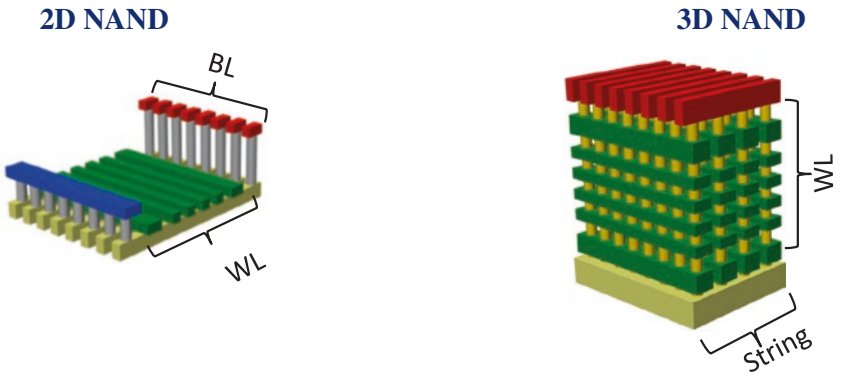

Figure 5-3. *2D planar NAND vs. 3D Vertical NAND*

Advantages of 3D Vertical NAND

3D vertical NAND has several advantages over traditional planar NAND, as follows:

a. Higher Storage Capacities: The vertical stacking of memory cells enables significant increases in storage capacities. With more layers of cells, 3D V-NAND offers the potential for greater memory densities, allowing for storage devices with larger capacities.

b. Improved Performance: 3D V-NAND can deliver enhanced read and write speeds compared to 2D planar NAND. The vertical structure reduces the distance that signals need to travel, resulting in faster data access and transfer rates.

c. Enhanced Endurance: Vertical NAND architecture improves the endurance of the memory cells. The increased space between cells reduces interference, leading to improved reliability and longevity.

d. Energy Efficiency: 3D V-NAND technology offers improved energy efficiency, allowing for longer battery life in portable devices and reduced power consumption in data centers.

Applications of 3D Vertical NAND

The advantages offered by 3D vertical NAND make it well suited for various applications, including the following:

a. Solid-State Drives (SSDs): SSDs equipped with 3D V-NAND deliver high-speed data storage and retrieval, making them ideal for use in laptops, desktops, and enterprise storage solutions. The increased storage capacity enables SSDs to meet the demands of modern data-intensive applications.

b. Mobile Devices: Smartphones, tablets, and other portable devices benefit from the compact size and high storage capacities of 3D V-NAND. These devices require reliable and fast storage solutions to handle multimedia content, applications, and operating systems.

c. Data Centers and Cloud Computing: The scalability and performance of 3D V-NAND make it a valuable technology for data centers and cloud computing environments. The increased storage densities and improved reliability contribute to efficient data management and faster processing speeds.

Understanding 3D Vertical NAND Architecture

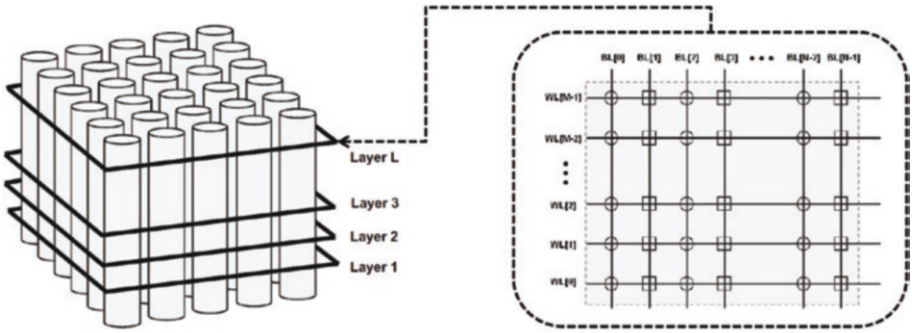

Figure 5-4. *3D vertical NAND layered architecture*

The unique architecture of 3D vertical NAND involves intricate vertical cell stacking and layering, which enables higher storage density and better performance. A block consists of vertically stacked layers of NAND flash cells, each consisting of grid of cells connected by Wordlines (WLs) and Bit Lines (BLs).

The vertical cell stacking approach ensures that more memory cells can be packed in a smaller space. This is achieved by placing multiple layers of memory cells on top of each other, making the most efficient use of available silicon area.

Each memory cell in 3D vertical NAND still consists of a transistor and a floating gate, just like in traditional NAND flash memory. However, the arrangement of these components is optimized for vertical stacking.

Layers and Pages

A 3D vertical NAND chip is composed of multiple layers, and each layer is divided into pages. Within a layer, pages are accessed individually for read and write operations. The vertical stacking of pages allows for greater memory capacity without increasing the chip's physical size.

Charge Trapping Technology

In 3D vertical NAND, memory cells use a charge trapping technology, unlike the floating-gate technology found in traditional NAND. Charge trapping stores charge in a non-conductive layer, preventing data loss due to electron leakage, which was a challenge in floating-gate technology. This enhanced data retention capability contributes to the reliability and longevity of 3D vertical NAND.

The 3D vertical NAND cell (also known as a V-NAND cell) is a type of NAND flash memory cell that is stacked vertically on top of other NAND flash memory cells. This allows for significantly greater storage density than traditional 2D planar NAND cells, which are stacked horizontally on a silicon wafer.

As shown in Figure 5-5, the 3D vertical NAND cell consists of three main components:

The charge storage film: This layer is made of a material that can trap electrons. The number of electrons trapped in this layer determines the state of the cell (0 or 1).

The control gate: This gate is used to control the flow of electrons into and out of the charge trap layer.

The channel layer: This layer is made of a semiconducting material that allows electrons to flow through it.

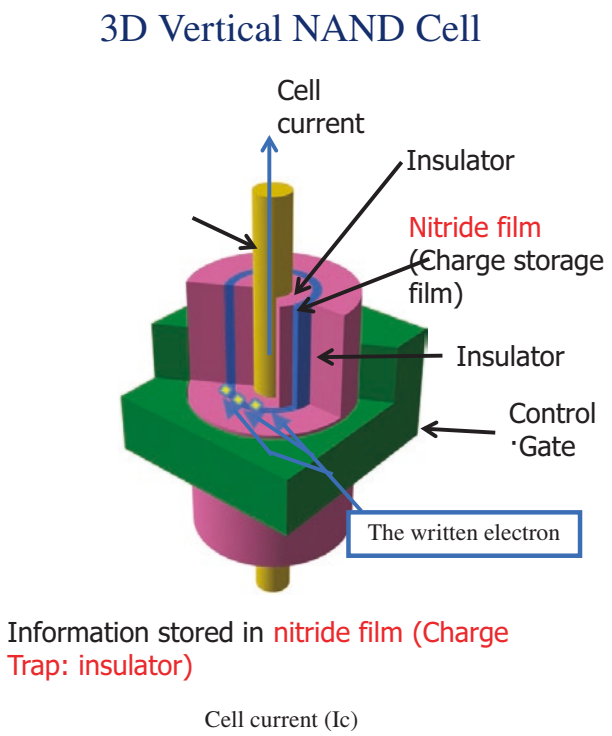

Figure 5-5. *3D NAND cell*

To store a bit of data in a 3D vertical NAND cell, a voltage is applied to the control gate. This causes electrons to flow into or out of the charge trap layer, depending on the desired state of the cell. Once the desired state has been achieved, the voltage is removed and the electrons are trapped in the charge trap layer.

The 3D vertical NAND cell is a highly efficient way to store data. It offers significantly greater storage density than traditional 2D planar NAND cells, while also being more energy-efficient. This makes it the ideal choice for a wide range of applications, including solid-state drives (SSDs), USB flash drives, and mobile devices.

Bit Line and Word Line Architecture

The bit lines and word lines form the essential structure of 3D vertical NAND. Bit lines run vertically through all layers, connecting the memory cells within a column. Word lines, however, run horizontally, connecting the memory cells across a row in each layer.

Control and Decoding Circuits

Control and decoding circuits are responsible for managing the flow of data in 3D vertical NAND. These circuits decode address inputs, control the selection of memory cells during read and write operations, and handle other essential functionalities.

Memory Cell Size and Density in 3D Vertical NAND Flash Memory Technology

3D vertical NAND (V-NAND) flash memory technology is a type of non-volatile memory that stacks memory cells vertically to increase storage density and capacity. One of the factors that affects the density and capacity of V-NAND chips is the size of the memory cells. As technology advances, manufacturers can reduce the size of the memory cells to fit more of them in a given area, resulting in higher density and larger capacity NAND chips. However, shrinking the cell size also poses some challenges, such as increased interference and reduced reliability. To overcome these challenges, V-NAND technology uses techniques such as charge trap flash (CTF) and tunnel field-effect transistor (TFET) to improve the performance and endurance of the memory cells. Moreover, V-NAND technology can also use different levels of charge to store multiple bits per cell, such as quad-level cell (QLC) or even higher, to further increase the storage capacity of NAND chips.

Understanding NAND Cell Types Supported: SLC, MLC, and TLC (QLC)

There are different types of memory cells, including SLC (single-level cell), MLC (multi-level cell), and TLC (triple-level cell). Each cell type comes with its own characteristics, influencing how data is stored, accessed, and managed. We'll discuss the principles of reading, writing, and erasing data from 3D vertical NAND flash.

SLC

3D vertical NAND SLC Vth distribution refers to the distribution of threshold voltages (Vth) of the memory cells in a 3D vertical NAND SLC flash memory device. Vth is a critical parameter that determines the performance and reliability of a NAND flash memory device. A narrow Vth distribution is desirable, as it indicates that all of the memory cells have similar Vth values. This makes it easier to read and write data to the memory cells, and it also reduces the risk of errors.

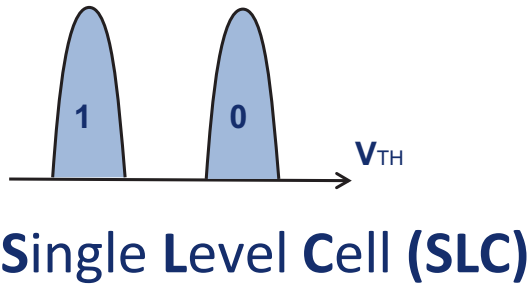

Figure 5-6. *3D vertical NAND SLC Vth distribution*

- 2 States (1 Erase + 1 Program) = 1 bit of information per cell

MLC

3D vertical NAND MLC Vth distribution refers to the distribution of threshold voltages (Vth) of the memory cells in a 3D vertical NAND MLC flash memory device. MLC NAND flash memory devices can store more than one bit (2-4) of data per memory cell, which requires a wider Vth range than SLC NAND flash memory devices. However, a narrow Vth distribution is still desirable for MLC NAND flash memory devices, as it improves performance and reliability.

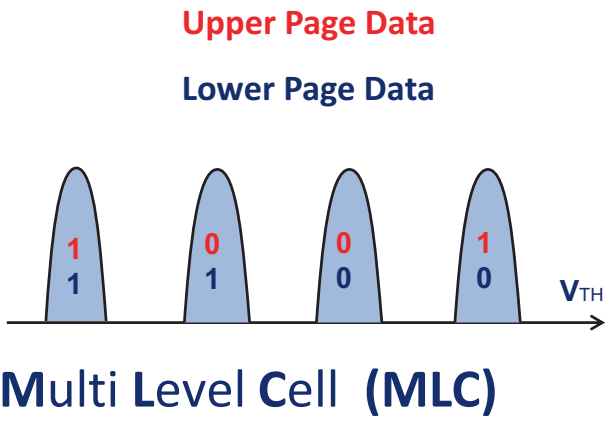

Figure 5-7. *3D vertical NAND MLC Vth distribution*

- 4 States (1 Erase + 3 Program)

  = 2 bits of information per cell

  = 2x capacity of SLC!

TLC

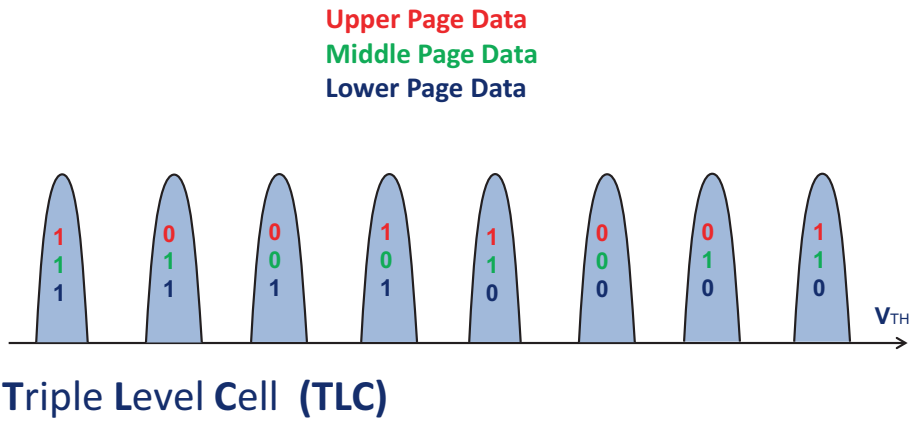

Figure 5-8. *3D vertical NAND TLC Vth distribution*

8 States (1 Erase + 7 Program)
= 3 bits of information per cell
= 1.5x capacity of MLC
= 3.0x capacity of SLC

Read and Write Operations in 3D Vertical NAND

3D vertical NAND exhibits remarkable read and write operations owing to its unique vertical architecture. During a read operation, the control gate voltage is adjusted, allowing the flow of current through the memory cell. The resulting current state is then sensed to determine the stored data. The vertical stacking of memory cells enables faster read operations by reducing the distance the current needs to travel, resulting in reduced read latency.

Write operations in 3D vertical NAND involve programming the memory cell to store data. The voltage applied to the control gate elevates the electron energy in the floating gate, causing the charge to be trapped, representing either a 0 or 1. The vertical architecture enhances write performance by reducing the parasitic capacitance between memory cells, enabling faster and more efficient write operations.

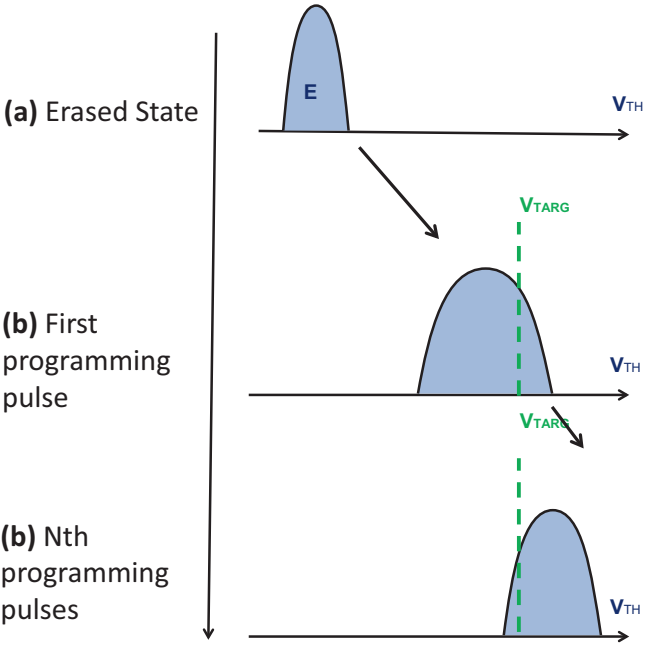

Figure 5-9. *3D vertical NAND SLC incremental programming pulse*

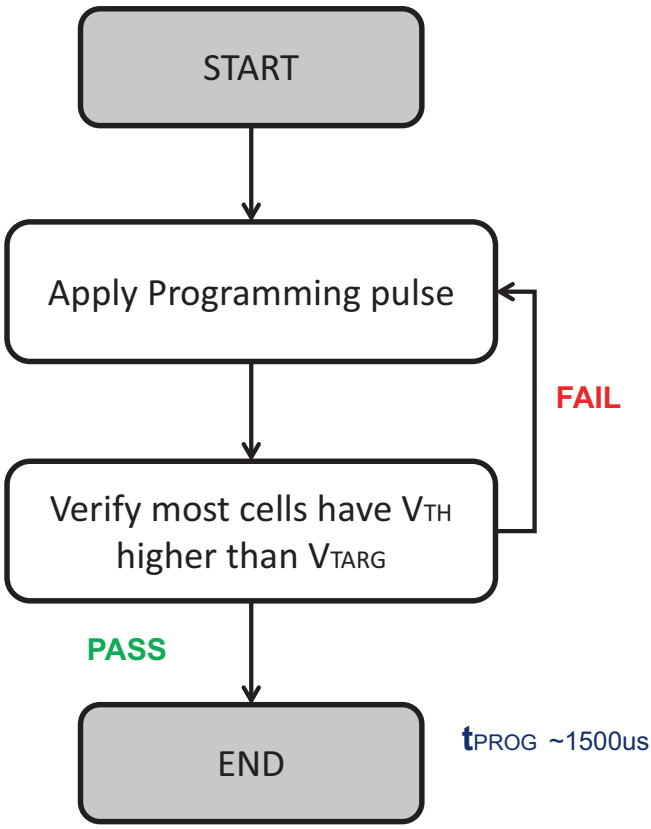

Figure 5-10. *3D vertical NAND SLC incremental programming pulse flow chart*

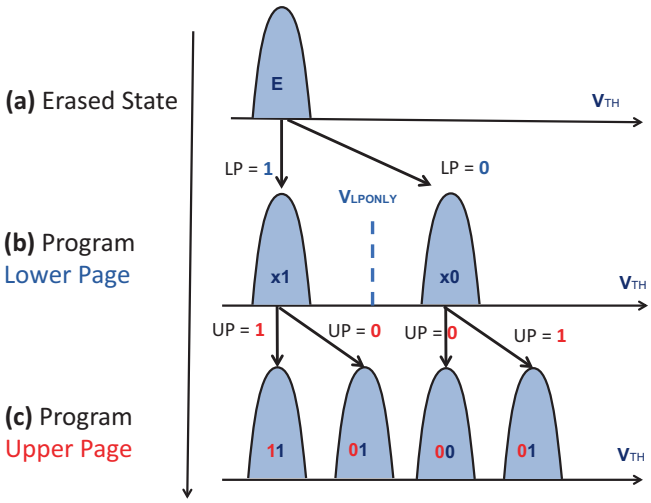

Figure 5-11. *3D vertical NAND MLC program sequence*

- Data is programmed to the device one page at a time.
- The cells are either left in the erased state or programmed to an intermediate state, depending on the lower page data.
- An intermediate read determines the previously programmed lower page data, and the cell distribution for the WL is "finalized" using the upper page data.

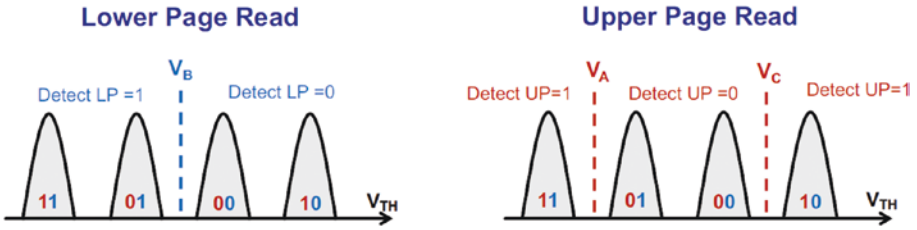

Figure 5-12. *Reading data from 3D vertical NAND MLC*

- Lower page can be read using a single read voltage (VB).
- Upper page can be read using a pair of read voltages (VA,VC).
- A page read (from NAND cell to NAND cache) typically takes up to 100us.

Erasing MLC 3D vertical NAND block

Erasing an MLC 3D vertical NAND block is the process of resetting all of the memory cells in the block to the same state. This is done by applying a high voltage to the block. The high voltage causes electrons to flow out of the charge trap layers in the memory cells, erasing the data.

Erasing MLC 3D vertical NAND blocks is more complex than erasing SLC NAND blocks because of the wider Vth range of MLC memory cells. To ensure that all of the memory cells in an MLC block are properly erased, the erase voltage must be carefully controlled.

There are a number of different methods for erasing MLC 3D vertical NAND blocks. One common method is to use a partial erase scheme. In a partial erase scheme, the erase voltage is gradually increased until all of the memory cells in the block are erased. This method is more energy-efficient than erasing the block at a single high voltage, but it takes longer.

Another method for erasing MLC 3D vertical NAND blocks is to use a full erase scheme. In a full erase scheme, the erase voltage is set to a high value for a fixed period of time. This method is faster than a partial erase scheme, but it consumes more energy.

The best method for erasing MLC 3D vertical NAND blocks depends on the specific application. For example, applications that require high performance may be willing to sacrifice some energy efficiency in order to achieve faster erase times.

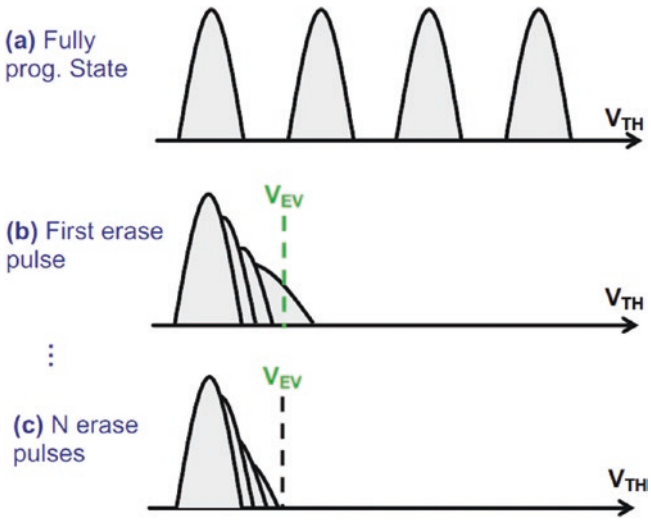

Figure 5-13. *Erasing MLC 3D vertical NAND block*

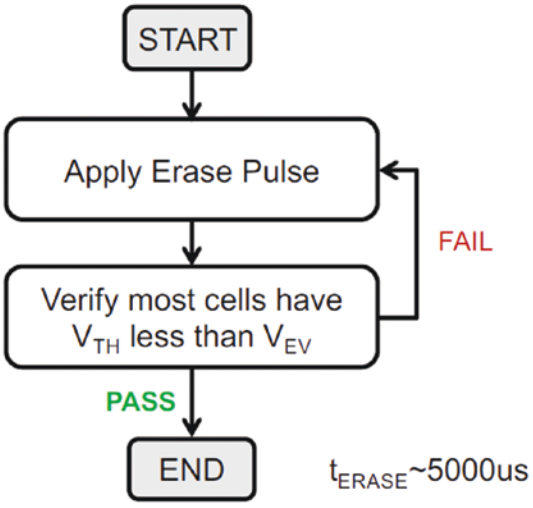

Figure 5-14. *Flow Diagram for 3D vertical NAND block erase MLC*

Endurance and Data Retention Capabilities

Endurance and data retention are crucial aspects of NAND flash memory. 3D vertical NAND excels in both areas due to its improved memory cell design and materials. The vertical structure reduces crosstalk and interference between memory cells, leading to improved data-retention capabilities. As a result, data stored in 3D vertical NAND remains intact for longer periods, even under challenging conditions.

Additionally, the vertical stacking design contributes to enhanced endurance by reducing wear on individual memory cells. This translates to a higher number of program-erase cycles before memory cell degradation, making 3D vertical NAND a reliable choice for data-intensive applications that require frequent read and write operations.

Speed and Efficiency Compared to 2D Planar NAND

Compared to traditional 2D planar NAND, 3D vertical NAND offers notable speed and efficiency advantages. The vertical stacking of memory cells results in shorter electrical pathways, reducing data access times and improving overall system performance.

With faster read and write operations, 3D vertical NAND outperforms 2D planar NAND in data access speed, making it an excellent choice for applications requiring real-time data processing. Moreover, the improved efficiency of 3D vertical NAND contributes to lower power consumption, leading to energy savings and prolonged battery life in portable devices.

Advancements in Storage Capacity with 3D Vertical NAND

One of the most significant achievements of 3D vertical NAND is the substantial advancement in storage capacity. The vertical cell stacking allows for a more efficient use of space, enabling the integration of multiple memory-cell layers within the same footprint.

As a result, 3D vertical NAND-based data storage solutions can achieve much higher capacities compared to traditional 2D planar NAND devices. This breakthrough has enabled the development of solid-state drives (SSDs) and memory modules with unprecedented storage capabilities, catering to the ever-growing demands of data-intensive applications.

Summary

With this very brief chapter on 3D Vertical NAND, we have covered the basics only. As you delve into this exciting field of advanced memory technology, you will gain a deeper understanding of how 3D vertical NAND is revolutionizing data storage and setting the stage for future innovations in the semiconductor industry. As engineers and developers, your expertise in harnessing the capabilities of 3D vertical NAND will be instrumental in creating next-generation storage solutions that cater to the evolving needs of our data-driven world. Embrace the power of 3D vertical NAND and unlock the endless possibilities it holds for shaping the future of storage technology from here.