CHAPTER 10

User Data Flow

In this chapter, we will discuss the user data flow in solid-state drive (SSD) firmware. We will start by discussing the write path, which is the process of writing data from the host to the NAND flash memory. We will then discuss the read path, which is the process of reading data from the NAND flash memory and transferring it back to the host.

Write Path

In SSD firmware, the *write path* refers to the process of writing data from the host to the NAND flash memory. When the host sends a write request command, the device allocates a cache buffer to receive the data. The data is then transferred from the host to the device cache, where it is transformed and prepared for writing to the NAND memory by the firmware translation layer (FTL). This process includes adding error-correcting codes (ECCs) to the data to ensure its integrity.

Once the data has been prepared for writing, the FTL programs it into the NAND memory. When the program is completed successfully, it updates the mapping table with the physical block address (PBA) for the corresponding logical block addresses (LBAs) that were successfully written. The goal of this process is to achieve the maximum write performance by ensuring that the NAND throughput is utilized to its full potential.

G. Kuppan Thirumalai, *A Beginner's Guide to SSD Firmware*,
https://doi.org/10.1007/978-1-4842-9888-6_10

To achieve this goal, the FTL arranges and performs independent tasks on the write path in parallel on different threads or CPUs, and sequences the NAND programming while preparing the next set of NAND programming. It also arranges the data for programming in a way that is most optimal for NAND operations, such as by using multi-plane and multi-die techniques to maximize channel and die capacity.

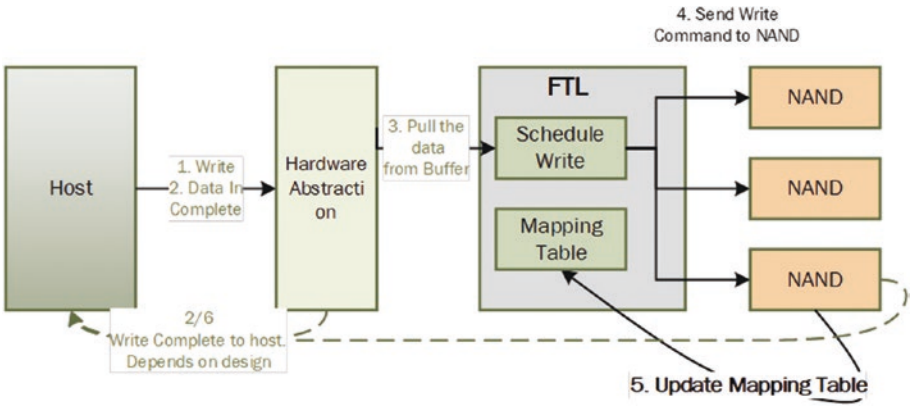

Figure 10-1. *Host write data path*

Read Path

The *read path* refers to the process of reading data from the NAND flash memory and transferring back to the host. This is a critical path in the system, as the host expects the device to read data with low latency.

The read process begins when the host issues a read command, which is processed by the FTL. The FTL translates the logical block address (LBA) of the requested data into a physical block address (PBA), and then sends a NAND read command to the PBA. The FTL monitors the progress of the read command and transfers the data from the NAND cache buffer to a read buffer inside the flash controller.

If the data is found to be error-free, it is transferred from the read buffer to the SSD cache. From there, it is transferred to the host. If the data needs to be corrected and is within the correction capability of the SSD firmware, it is corrected before being transferred to the host.

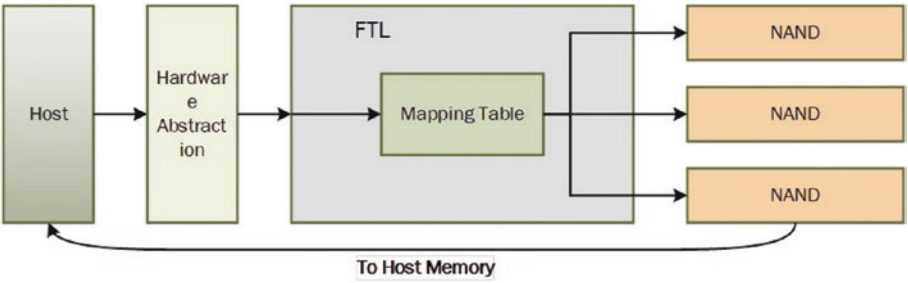

Figure 10-2. *Host data read path*

Overall, the write and read paths in SSD firmware are complex processes that involve a series of steps to ensure the efficient and reliable reading of data to and from the NAND memory. By optimizing these processes and carefully managing the data transfer, SSD manufacturers can improve the performance and reliability of their drives.

Summary

This chapter has discussed the user data flow in SSD firmware. We have seen how the write and read paths are two critical processes that ensure the efficient and reliable transfer of data between the host and the SSD. We have also seen how the SSD firmware can optimize these processes to improve the performance and reliability of the drive.