Chapter 6
Mechanical Stability and Performance

This chapter describes the reliability performance and failure mechanisms of Pb-free solder joints under various mechanical load conditions, including bending, cyclic bending fatigue, and mechanical shock. The structural stability of solder joint under such mechanical loads is an important consideration factor for the current and future solder interconnects because electronic devices are subjected to such loads during various parts of their production as well as in end-use conditions. Even more importantly, mechanical stability is emerging as critical reliability concern with a rapid expansion of mobile electronics. In order to properly apprehend their challenges to the reliability, this chapter describes the threat from each mechanical load and the mechanism by which the solder joint fails. We begin with the introduction of the failure in solder interconnect induced by the bending force on PCB. The source of the bending force and its test method are presented along with discussion on failure mechanism. It is shown that the failure by bending force occurs either in Cu trace in PCB or solder/Cu interface. Secondly, the influence of cyclic bending fatigue is introduced. It is discussed more in terms of its mechanics and its potential as a new reliability evaluation tool. Finally, the failure by mechanical shock is discussed with weighted emphasis on recent experimental observations showing a sensitivity of shock resistance to the microstructure of the SAC solder joint bulk structure.

Mechanical Stability of the Solder Joint: Introduction

Electronic devices experience various external forces in several different modes. From a portable smartphone to a stand-alone Internet router, all equipment experiences some level of vibration, cyclic bending, monotonic bending, cyclic shock or a single shock. For high-reliability electronic devices, the mechanical stability of solder interconnects during dynamic conditions is crucial [1–5]. To have a stable interconnect in a mechanical performance environment, the

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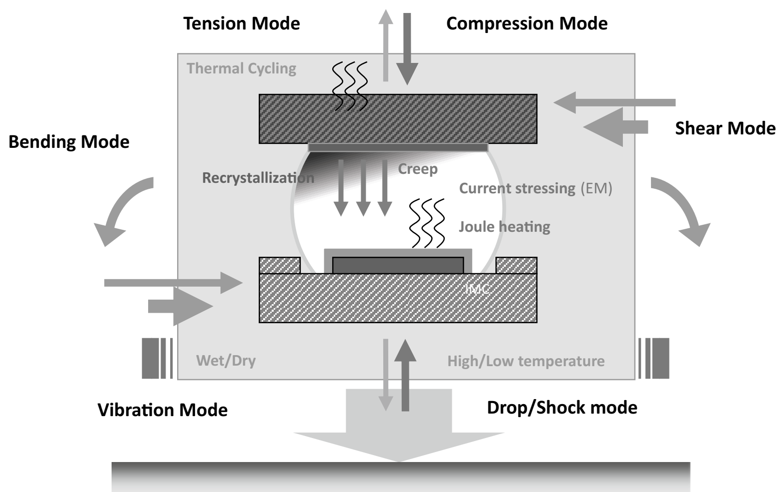

Fig. 6.1 Several factors need to be considered to predict the total lifetime of the solder joint including external forced from a variety of sources

interconnections need to tolerate mechanical strain, which develops in a particular way that depends on how the applied shock input reaches the particular component and particular joint [6–9].

Figure 6.1 shows a schematic of a solder joint, which experiences various external forces and challenges. All of these external or internal sources affect the stability of the solder joint. Mechanical bending can occur during use of the device or board, but even before assembly to the chassis, a large PCB can be easily bent by mishandling (grapping the board at one corner, etc.). The bend can produce a significant strain at certain component corner joints and potentially induce fracture to the joint even before it is deployed to the field. A continuous cyclic bending condition is a potential risk to the solder joint stability since high cycle fatigue failure develops during a long period of time, making it more difficult to identify and mitigate. Thus, knowing how monotonic and cyclic strains affect the solder joints and the associated deformation mechanisms that are activated is important to correctly assess and predict the lifetime of the joint and in order to identify potential mitigation strategies that can delay the failure [10].

In real products like running cars, for example, there are many types of energy inputs that lead to cyclic bending (or vibration), which can challenge the mechanical performance of the solder joint. An example of a 2.5 t truck is introduced in Steinberg's book [11, 12] that shows 15–19G peak acceleration at speeds above 10–15 mph with a frequency of about 15–40 Hz. Here we can see that there are two major factors, which need to be identified, the acceleration (G) and the frequency (Hz). The G level is an important factor, which is deeply correlated to the strain.

A higher G level can induce higher local strains, which will be examined in more detail in this chapter. Compared to vibration, mechanical shock usually has higher G levels per event and is a more single event-driven factor. It is easy to see the importance of shock performance by just looking at an everyday usage of a smartphone. Causing a total malfunction with just one general drop to the ground is not an expectation from a user. Fortunately various service programs and marketing programs exist that often can replace the malfunctioned device. But the problem is more serious if the mechanical shock-induced failure occurs on high-reliability products, where even a short interruption can cause unacceptable consequences and even endanger the safety of the users. In this case the frequency is not an important factor since the user just dropped the device one time, but once if the frequency increases, we will immediately see the effect of the interval time between the events, which ultimately will define the stability of the joint even in lower G level environments (e.g., cycling events like cyclic bending and vibration).

Facing these mechanical stability challenges, to correctly understand the mechanical performance of the device under certain user condition, simple questions need to be answered. For example, how many drops can a smartphone endure? Can the multi-chip module (MCM) under the hood in a car, which has an environmental temperature range of 200 °C, survive 10 years? After 5 years of functioning, can the router survive a general earthquake shock? To answer these questions, test methods and assessment tools based on mechanical shock-, bending-, and vibration-induced failure mechanism need to be established.

In this chapter, we will consider the mechanical stability of the solder joint by focusing on mechanical bending and shock for both monotonic and cyclic events. We will begin with monotonic bending and then consider cyclic bending, followed by mechanical shock to identify factors that affect their failure mechanisms. Figure 6.2 shows the failure modes observed in mechanically induced failures, whether by direct bending, vibration, or shock. Each external energy input induces a particular strain, and the localized strain is one of the direct sources that trigger failure in the solder joint structure. Representative failure modes are at the interface IMC for both package and board-side interface, inside the solder bulk joint, at the laminate region under the Cu pad, or at a combination of all three modes. It is often a competition between each failure location regardless of the crack initiation point, during further external energy input after initiation, the once dominating failure location can be shifted to a different failure location with faster crack propagation rate and ended up with a different final failure mode. So knowing the crack initiation and the propagation mechanism is crucial. Then how can we increase the stability in the mechanically challenged environment? An ideal system should consist of a flexible board and component that can absorb all the energy from the vibration, bending momentum, or shock, but given the fact that the silicon die is stiff, flexibility is limited; to endure the shock, the interconnects need to absorb or tolerate mechanical strain, which develops in a way that depends upon the interactions between the component location and applied mechanical source [6–9].

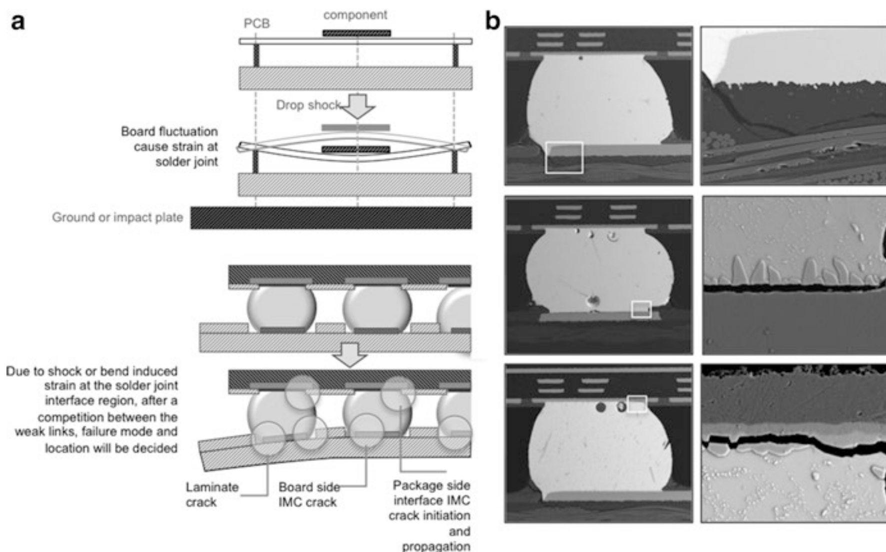

Fig. 6.2 Shock or bend eventually causes local strain which can affect the stability of the joint. (**a**) The corner solder joints experience a strain induced by the shock and bending mode. (**b**) Selected solder joints after shock test which show various types of failure modes and location

Given that the weakest interface changes with package design or even joint position in a package, identifying the methodology to improve the solder joint shock performance is a challenge. Three approaches can be proposed. With an example of a solder joint, which fails at the laminate, the first one is to either improve the strength of the laminate material or design the pad to shift the weakest link away from the laminate stress concentration point. The second approach is to directly strengthen the IMC layer so that the crack propagation is mitigated or delayed, and the third approach is to have the solder joint become able to absorb shock so that the shock wave does not transfer strain to the IMC layer or have the solder joint absorb strain by deformation so that the joint does not experience damage at the interfaces. We will discuss these approaches in the next section and identify methods that can elucidate how deformation mechanisms operate. What we will see in this chapter is that, at the end of the day, it is actually the capability of the solder joint, how much energy it can absorb, which defines ultimately the mechanical stability of the system.

Mechanical Bending

One form of mechanical force input is bending. Bending can be considered as an external mechanical source, but it can also be considered as an outcome that is induced by other external force and sources. For example, bending could be caused

by direct force input, but it can also be caused by shock and vibration that induce bending. But whatever the original source is, bending can induce strain in a particular region, and if the locally developed strain exceeds a certain damage limit, the energy released will develop an unstable damage site that will grow with further deformation.

Representative industry test standards exist. For monotonic bending, one of the standard documents is the IPC/JEDEC 9702 "monotonic bend characterization of board-level interconnects," and for cyclic bending there is an industry standard, JEDEC22-B113 "board level cyclic bend test method for interconnect reliability characterization of components for handheld electronic products" [13, 14]. The IPC/JEDEC 9702 on monotonic bend test is intended to characterize the fracture strength of a component's board-level interconnects and is applicable to surface-mount components attached to PCB. The characterization results provide a measure of fracture resistance to external loading that may occur during board assembly and test operations. A detailed test method is described in the document [13]. A universal tensile tester, with a four-point bending fixture is used to generate a controlled board deflection rate and apply a uniform-bending moment across the load span. Figure 6.3 shows a conventional four-point bending fixture and test configuration. To obtain valid results, a repeatable and well-controlled strain and strain rate are required. The crosshead travel distance and crosshead speed of a universal tester are approximately proportional to the test board assembly strain and strain rate, respectively. But as test boards have their own construction and geometry, interaction between a given component and board, a strain measurement is needed. Strain measurement equipment with a scan frequency of 500 Hz and a data signal resolution of 16 bits are necessary for the short-duration monotonic bend test (typically <5 s), allowing simultaneous recording of the daisy-chain resistance and strain based on the specification [13].

Since the interaction between the crosshead speed and the test board, the thickness and metal layer counts are important factors. The test board thickness and metal layer count should match the actual end-use device-printed circuit board. Table 6.1 provides recommended minimum test board thickness and metal layer counts. The recommended crosshead speed in the IPC/JEDEC 9702 is 5,000 µstrain/s. Testing conducted at crosshead speeds less will tend to overestimate the fracture strength of a component's board-level interconnects; hence, test equipment and test board configurations should be selected that meet the minimum crosshead speed to ensure getting the right value for an interconnect strength. The duration of the test is until the solder joint full fracture is detected, which is usually when the daisy chain has electrically failed, including the laminate crack which leads the Cu trace to be fractured/disconnected.

Figure 6.4 shows one bend test example with a large FCBGA mounted on a 2.36 mm (93 mil) thickness board. Strain gauges are located and applied to four different locations, and the board was bent to the point where the component daisy chain is broken. Shown in the figure, Ch1 and Ch2 strain gauges were attached to the backside of the board under the middle of the component edge and the corner of the component location, respectively. Ch3 strain gauge was placed on top of the

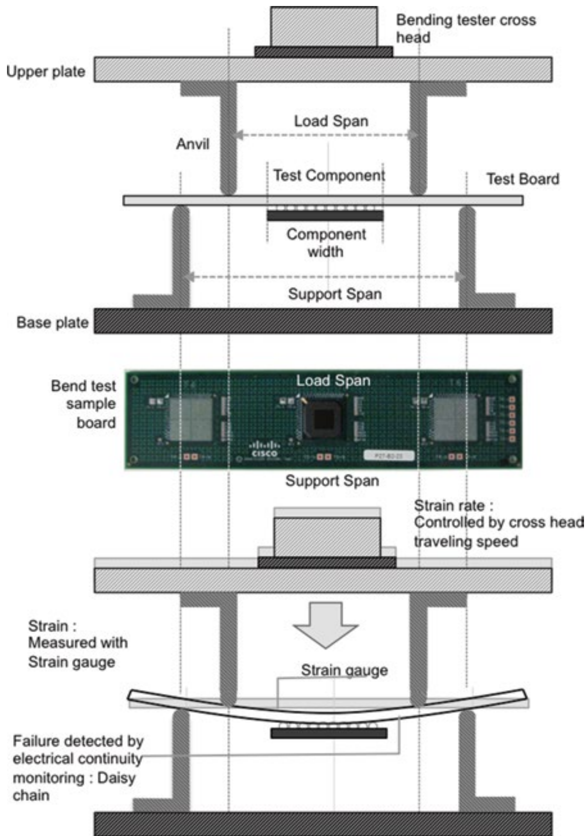

Fig. 6.3 Four point bending fixture and test configuration

component. A separate channel was attached to the daisy chain of the test component and board, so that the resistivity can be measured and detect the resistivity increase at the joint failure. With the crosshead pushing the backside of the test board, bending proceeds; Ch1 and Ch2 increased in negative microstrain value, since the component is facing downward. At the same time the component top also followed the bending with a positive microstrain until it reached the joint failure strain. When the Ch2 strain, the strain of the backside of the board under the component corner, reached (−)4,000 μstrain, Ch1, Ch2, and Ch3 all show a sudden step in the strain value measurement, which indicates the failure event followed with several continuous steps. With this measurement, we can assess the minimum strain to failure and use this data to set a process guideline or, if necessary, find a way to improve the minimum strain to failure for better mechanical reliability under bend-

Table 6.1 Recommended test board thickness and layer count

Maximum Package body size	PCB thickness (mm)	Minimum Cu layer count
Small : less or equal than 15 × 15 mm	1.0 mm (0.039 in.)	4
Medium : larger than 15 × 15 mm and less or equal than 40 × 40 mm	1.55 mm (0.062 in.)	6
Large : equal or larger than 40 × 40 mm	2.35 mm (0.093 in.)	8

ing condition. This example, in this case, monotonic bending, also shows that the various locations on the board show different strain responses, and each location shows a different stage and point of a joint failure. A certain incubation time or strain before reaching the strain level of failure exists. It is how much the component and board interaction and structure can endure, before a failure occurs. In other words, it is how much the solder joints and the interface bonding can hold on or absorb the strain caused by the bending before it releases the strength and fall apart. It is not hard to estimate that a larger component with a stiffer body is more riskier than a small and flexible component, but at the same time, other factors like the design of the Cu trace on the board side, the pad opening size, the height and diameter of the solder joint, the surface finish, etc., are equally important to derive a certain stability trend [15, 16].

Figure 6.5 shows the results of several components with different shapes and sizes that were bent to failure. The maximum strain at failure shows that the larger the component, the lower the strain level needed to break the solder joint, which is in most cases the corner solder joint. Of course, other factors than the component size are additional consideration factors, which influence the joint stability, like surface finish, solder alloy, solder ball size, and standoff heights. With all these combinations, the fracture mode is often strongly correlated to the board pad design. In non-solder mask-defined pads (NSMD) most of the cracks initiated and propagated through the laminate under the Cu pad, and most of the solder mask-defined pad (SMD) boards fracture in the IMC in the board-side interface. This effect of pad design performances will be discussed later in the shock performance results. Another interesting pint in the results in Fig. 6.5 is the failure strain difference between the electrical resistance measurement method and the acoustic event detection method. The acoustic event detection method is a nondestructive measurement method, which uses acoustic wave signal to identify fracture signatures during bending. As we can see in the figure, the failure strain levels are much lower compared to the electrical discontinuity measurement failure strains. This means that the laminate crack actually happens in a very low strain level. The strain needs to be built up to a certain level to break the Cu or solder interconnect to show the discontinuity in electrical measurements; thus a strain gap exists between two measurement methods.

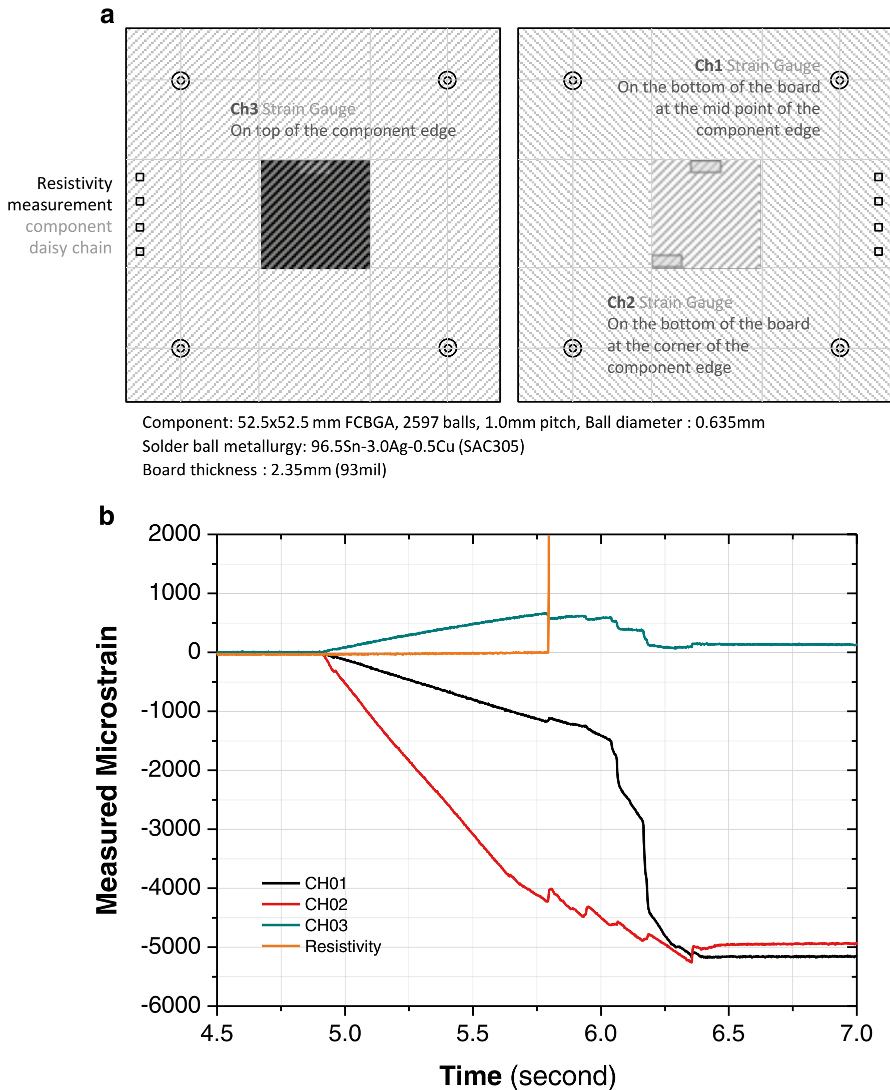

Fig. 6.4 Monotonic bend test example with a large FCBGA mounted on a 2.35 mm thickness board. (**a**) board layout and component info (**b**) strain value/data plot during bend test

Effect of Cyclic Mechanical Bending

Printed circuit board assemblies experience various mechanical loading conditions during assembly and use. Repeated flexing (cyclic bending) of boards during various assembly and test operations and in actual use can cause electrical failures due

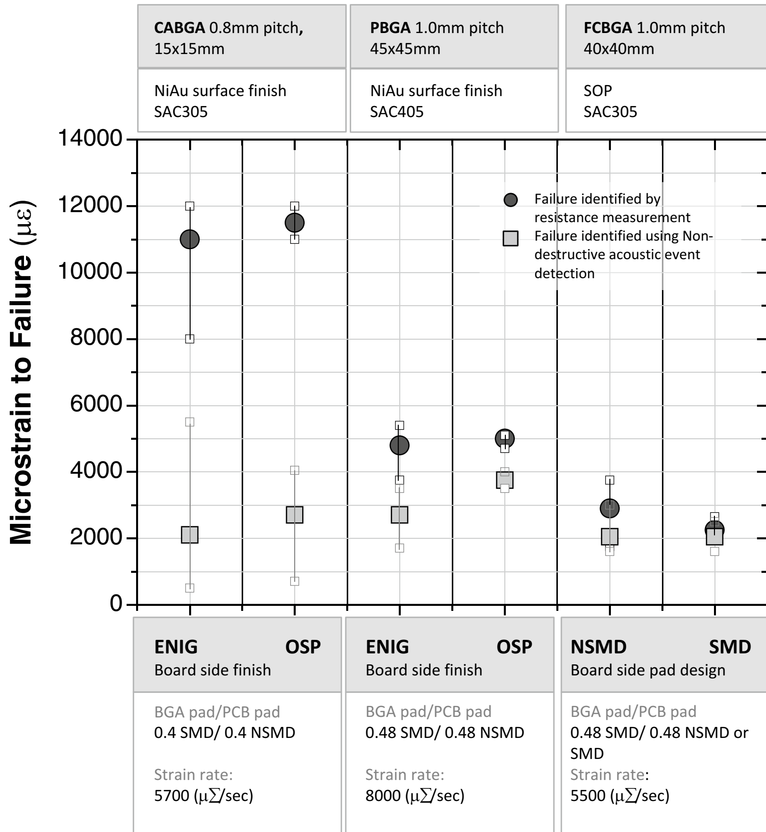

Fig. 6.5 Monotonic bend on CABGA, PBGA, and FCBGA sample with a 2.35 mm thickness board. Data points collected with electrical resistance measurement and Acoustic event detection method

to circuit board and trace cracks, solder interconnect cracks, and component cracks [17–23]. Although the number of repeated bend cycles is small during assembly (e.g., handling between various assembly operations, in-circuit testing, final assembly in product casing), the magnitude of flexure can be very significant. On the other hand, the actual-use conditions such as repeated key presses in mobile phones can result in a large number of repeated bend cycles during the life of the product, albeit at a lower magnitude. For example, the longitudinal and transverse strains that were measured on printed wiring board underneath the "9" and "8" keys show a maximum strain of about 400 microstrain and a duration of about 0.2 s for each key press [17]. A board-level test method is needed to evaluate the performance of the mounted parts against such failure and compare their performance with other components. Such evaluation is routinely conducted using cyclic bending tests.

In addition to the need for evaluating bending reliability of solder joints in normal-use conditions, the bend test has become more important in the packaging industry because it can reduce the reliability testing time. One of the most widely practiced reliability tests is temperature cycling. While it allows reliability evaluation of solder joints in normal-use conditions, it has a major drawback of taking an excessive long time. It often takes several months to induce failure, and multiple tests are required to enable reliability prediction with desired confidence. Because thermal cycling imposes significant time limitations on product development, there is growing interest to replace it with a faster but equally effective testing method. Cyclic bending fatigue testing may be one of the most promising methods with this potential. At the least, it has proved to be a quick way to identify failure-prone package designs or improper process conditions [18–25]. There is even greater interest to replace the temperature cycling test with the cyclic bending test if isothermal fatigue properties can be put into a predictive model that effectively predicts thermal fatigue reliability. However, because failure by thermal fatigue involves microstructural evolution, the model must include the dynamics of solder joint microstructure evolution and its influence on the thermal fatigue fracture mechanism. This poses a considerable modeling challenge that has not yet materialized. Nonetheless, the fact that fatigue testing can be done in a matter of days, if not hours, makes the bending fatigue test attractive for continuing considerable research and be used at least for product screening purposes. Industry standards on the cyclic bending test, for example, JEDEC22-B113, define boundary conditions for evaluating the whole assembly, but since they are intended for simulating failures at normal-use condition, they do not specify conditions for testing particular components on board and methods for analyzing the data. In order for it to be used for the study of solder fatigue properties, a few minor modifications of the system is needed, but more important is to understand its mechanics in inducing solder joint fatigue failure [25]. Also, the fact that cyclic fatigue bending performance varies significantly with chip design, materials, and process conditions makes discussion on fatigue performance of a particular system to be not so meaningful. Therefore, we focus more on the introduction of the fracture mechanics in cyclic bending fatigue and discussion on its merits as a potential reliability testing method.

The cyclic bending method builds on concepts developed from measurement of bending strength of structural materials [26]. In the case of bend-strength testing, the test piece is one piece of material that is subjected to bending strain by displacing the center of the sheet in reference to two pivot points. This action creates the uniform bending of the test piece between the two pivot points and allows the measurement of various material properties related to bending strength. The 3-point or 4-point bending configuration for assembled component packages is similar in that the stress imposed on the joint is induced and controlled by the bending of the substrate. However, the way that stress is induced at the solder joints is intrinsically different, and the difference can be seen in the example of 3-point bending of the PBGA assembly shown in Fig. 6.6. As shown, when the PCB board is bent, the test component is also forced to be bent. Because the bending force on the component

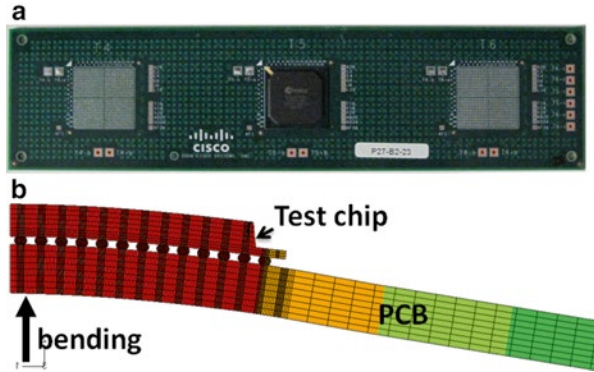

Fig. 6.6 A picture and diagram showing (**a**) PBGA board assembly designed for cyclic bending testing; (**b**) a schematic representation of the assembly at the bending condition

is transferred through the joints, the difference in the stiffness of the PCB and the chip creates a nonzero bending moment in the solder joint and thus exerts stress into the solder joints.

The fact that the stress at solder joint develops due to the difference in bending stiffness between the PCB and the chip creates several advantageous conditions for testing solder joint reliability. The first is the fact that the strain developed in an individual solder joint is not pure bending or shear but also has a significant tensile/compressive component perpendicular to the board. When the center of the PCB is pushed toward the chip, the joints at the outer edge of the array experience a force to separate the PCB and the chip, creating tensile strain. If the test were cycled fully about the neutral position, the opposite displacement would place the same joints under compressive strain. Such stress condition can simulate the stress induced by the thermal expansion mismatch between the chip and the substrate. The thermal mismatch causes the substrate to bend, resulting in the highest stress at the solder joints located at the outer edge or at corner of the assembly. It is therefore likely that the failure mechanism of the joint discovered by the bending fatigue is similar to the failure by thermal fatigue as long as the effect of microstructural evolution on the fatigue mechanism plays a minor role. This is the reason why the bending fatigue has gained considerable research interest.

Because the difference in bending stiffness between PCB and the test component is the very source of the stress in the solder joint, the level of stress is affected not only by the position of solder but also by the thickness (or local stiffness) of the molding compound where the joint is located. The variation in stress condition due to variation in molding thickness can be seen from the FEM (finite element method) strain simulation result of the PBGA package shown in Fig. 6.6. The result is shown in Fig. 6.7, where the shear, bending, and total plastic strain in the joints located at the outmost column of solder array as a function of their row position. This assembly contains a 26×26 array of 600 μm SAC305 solder ball joints, and the test component has a 2×2 cm base (labeled as BT) with an octagonal mold structure. The FEM simulation result shown in Fig. 6.7 is the case when bending displacement is 200 μm along the central axis. It is important to note that the joints experiencing the

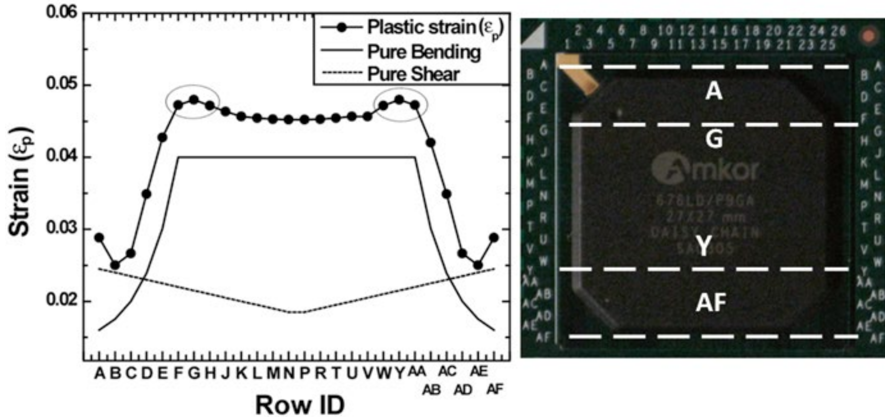

Fig. 6.7 A plot showing the shear, bending, and total plastic strain in the joints located at the outmost column of solder array as a function of their row position. The *left* is the image of the test chip with an inclusion on the key row positions of solder arrays. FEM analysis on the strain is conducted with an assumption of 200 **μ**m bending displacement at the central axis

maximum plastic strain is not located at two outer corners (A and AF) but is located inner side of the row (G and Y). This occurs because the joint at the G and Y rows is located at the boundary of low (thin) and high (thick) molding compound thickness. The schematic representation of the strain included in Fig. 6.7 presents a mechanistic explanation of this effect. As shown, there are two sources of the total strain upon bending. The first is the strain caused by the pure bending, and the other is pure shear. The bending strain comes mainly from the bending resistance of the chip, forcing the chip to separate from the solder, and therefore it is directly proportional to the local thickness of the molding. On the other hand, the chip also resists against the deformation in directions normal to the bending axis, that is, x- and y-axis, resulting in a shear strain. Consequently, the shear strain develops at the solder joint, and it will be the maximum at four corners of the molding, regardless of the thickness, and decreases with distance from the corner. The total strain is therefore the result of these two strain sources, making the G and Y joints to be at the maximum strain.

Figure 6.8, where the total plastic strain field within G and Y joints is shown, demonstrates that the cyclic bending testing is likely to induce crack initiation at the board side of the solder joint. In this colored diagram, the red represents the high total plastic strain while the blue represents low strain. It can be seen that there exist two maxima points, one at the solder/Cu trace interface corner of the joint and the other at the chip/solder interface. Detailed analysis reveals that the former experiences slightly higher plastic deformation than the latter. According to this result, the primary location for fracture is the interface between the solder and Cu trace in PCB substrate, unless the neck area in the solder created by the solder mask is mechanically weaker. Also predicted is that the joint that fails first is the one at G and

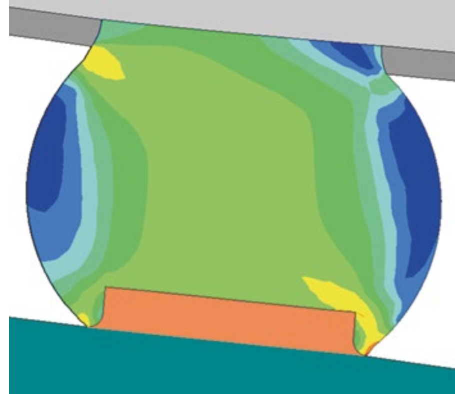

Fig. 6.8 A diagram showing the total plastic strain field in the solder joint G and Y under 200 **μ**m displacement at the central axis of the board. The red and blue colors represent the high strain and low strain, respectively. Note the presence two strain maxima, one at the right corner of the solder joint and the other at the solder neck area

Y. Cyclic bending testing of the as-reflowed solder assembly shows an exactly matching failure joint position and path. It was found that the failing joint under fatigue was located at G and Y position regardless of the level of displacement and cycle frequency. An example of the fatigue crack in a SAC305 joint (G position) following the interface of solder and Cu trace is shown in Fig. 6.9. Note that the crack propagates along the interface of solder/IMC but not inside the solder matrix. Also, the crack growth is very rapid, as evidenced by the resistance tracking data shown in Fig. 6.10. It can be seen that the number of cycles for the failure (C_f) after the damage initiation (C_i) is much shorter than C_i. It means that crack nucleation beyond the critical size takes much longer cycles than the crack growth. This is a result of crack growth under cyclic bending proceeding by the crack opening mode. Figure 6.11, where the FEM simulation of the solder joint deformation is shown, demonstrates the crack opening. In this simulation, a preexisting crack representing the embryonic crack is placed at the joint corner, and the deformation of the joint under bending displacement is calculated. The stress created at the crack tip due to bending results in opening of crack tip and causes the stress intensity factor (K_I) to increase. Such a level of crack opening is possible because nearly all applied strain is taken by the solder.

Early explorations of using cyclic bending in studying solder joint fatigue reliability indicate that it not only produces data that is reasonably repeatable but also a data that is consistent with normal fatigue theory. Figure 6.12 shows some of such data, which were gained from the bending fatigue testing of the same assembly in Fig. 6.6 with variation in frequency and bending displacement. Note that the failure cycle number increases with frequency but decreases with bending displacement. The result of decreasing fatigue life with increase in displacement is easy to understand because the plastic deformation per cycle at the joint increases with the bending displacement. Its dependence on the bending frequency may not be as intuitive, but it can be understood in the frame of work hardening. The frequency physically is related to the strain rate, meaning that high-frequency fatigue is equivalent to the fatigue at high strain rate. Since solder work hardens more at higher strain

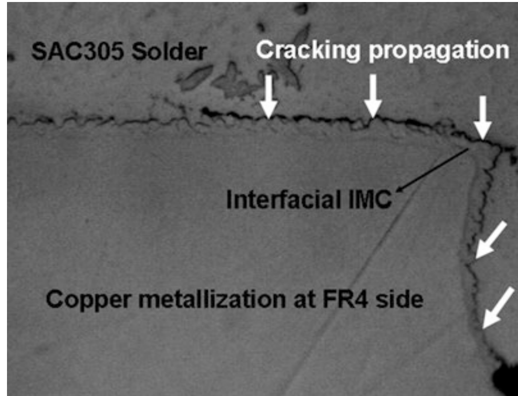

Fig. 6.9 A SEM micrograph showing the crack propagation path in SAC305 solder joint taken after the cyclic bending with 200 **μ**m displacement under 1 Hz frequency. Note that crack initiates at the corner of solder/IMC interface and grows following the solder side of the interface

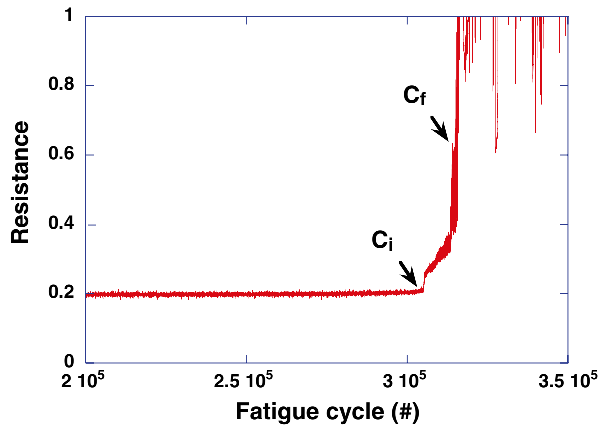

Fig. 6.10 A plot showing the typical resistance trace of solder joint taken during the cyclic bending. Note that it takes very large number of cycles to initiate crack (C_i) compared to the cycle number for its growth to failure (C_f)

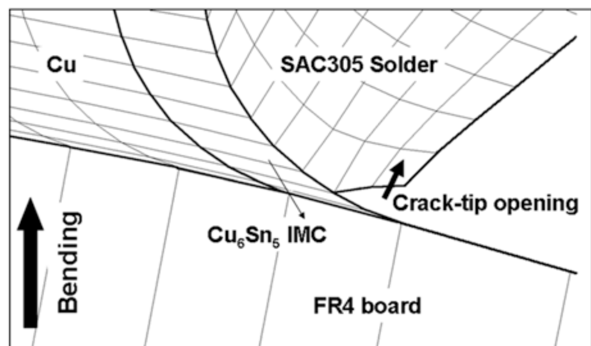

Fig. 6.11 A diagram showing the solder joint deformation configuration at the corner of solder joint near interfacial Cu_6Sn_5 IMC. This FEM analysis result evidences that the crack-tip opens due to plastic deformation in the solder by the bending of the PCB

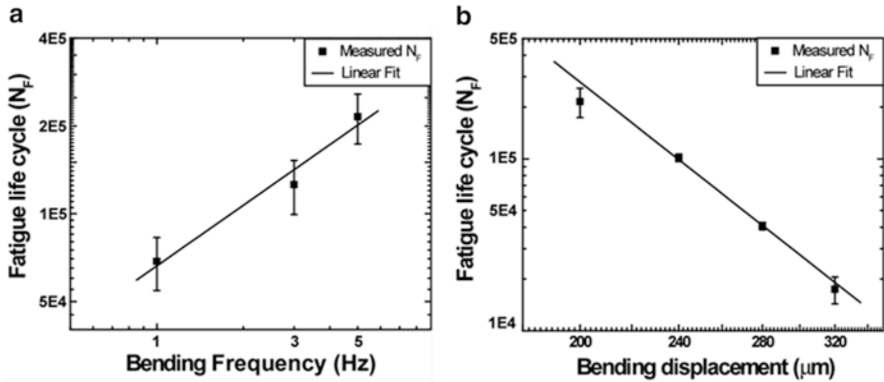

Fig. 6.12 Plots showing the fatigue life of SAC305 joints in PBGA assembly (shown in Fig. 6.6) as a function of bending displacement tested with variation in (**a**) bending frequency, and (**b**) bending displacement

rate, increasing its yield strength, the increase in the fatigue life with the bending frequency may be attributed to work-hardening property of the solder although other factors like deformation relaxation rate may play a role.

The results from the cyclic bending fatigue like the ones shown in Fig. 6.12 may provide an opportunity of investigating the fatigue properties and fatigue mechanism active in solder joints. There are two competing fatigue models suggested for the solder, and they are the total plastic strain and the total plastic strain energy models. The plastic strain model, known as the Coffin-Manson model, suggests that the fatigue life is determined by the amount of plastic deformation per cycle, while the energy model suggests that the fatigue life is related to the stored plastic energy. The level of plastic strain and strain energy can be calculated using FEM analysis and used for fitting of data to these models. The fit tried on the data in Fig. 6.12 is shown in Fig. 6.13. Note that the fatigue data gained from the displacement and frequency variation in Fig. 6.12 fit to one power law when they are plotted together as a function of the total plastic strain. On the other hand, those two fatigue data do not show such a correlation when they are plotted as a function of the total plastic energy. In this case, there exist two power law relations: one for the displacement and the other for frequency. This result may suggest that the Coffin-Manson model may be a more appropriate model for describing the fatigue behavior of the solder at isothermal condition, which may or may not be extended to the case of thermal fatigue, where stress relaxation is an important consideration.

Effect of Mechanical Shock

A mechanical shock to a device or board can occur from various sources. A direct hit to the device or a collision can transfer the impact energy directly to the device. This type of impact energy can also happen when the device is dropped to the

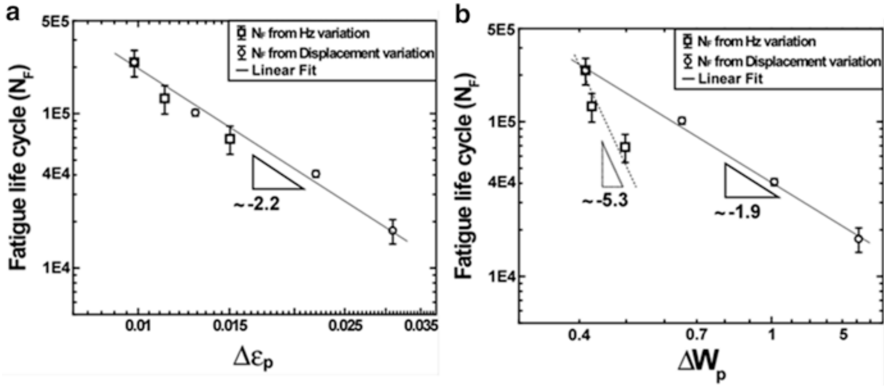

Fig. 6.13 Plots showing the fatigue life of SAC305 joint in PBGA assembly (Fig. 8.5) as a function of FEM calculated (**a**) total plastic, $\Delta\varepsilon_P$, and (**b**) total strain energy, ΔW_P

ground. With the impact energy transfer to the device, two important quantities can be measured, the acceleration (G) level and strain (ε). With a given impact energy input, to maintain its functionality, the device or the board needs to dissipate the impact energy before the energy impacts the joints or interconnects.

Figure 6.14 shows one example of a monotonic table drop shock impact applied to an electronic equipment board. The board size in this case, 6 × 6 in., was attached to the table with four standoffs at each corner of the board and lifted to a calibrated height to achieve a 200G acceleration or shock level at the table. With the impact, the table experienced a 200G level shock pulse; the accelerometer at the component corner on the test board measured a 300G maximum acceleration shock wave. At the same time, strain at the corner of the component measured by a strain gauge shows a sudden spike, a localized strain, which is a very high strain rate bending moment, followed by a high-frequency oscillating cyclic bending. In these series of events, we can see several factors, the input shock level based on the drop height, the shock wave travel from the table to the component via standoffs, the local strain, induced by the shock, and the frequency of the strain cycles to dissipate the shock energy.

But one very important factor among those various factors is the shock pulse duration and its correlation to the intensity of the shock wave, in other words the G level. For example, the pulse duration for the table shock input from the test above is 1 ms as shown in Fig. 6.14 and can be differed with using a different stopper material at the surface, where the table drops on. Simply it is a cushion, which defines the shape of the shock wave, the half-sine pulse duration as shown in Fig. 6.14b. Whether the stopper material is thin or thick (or different materials which absorb more shock than the other), the shape of the shock wave can be different with various pulse duration times. Figure 6.15 is a series of examples with the same test board with three different stopper materials. Shown in Fig. 6.15a the drop height was fixed to have a 200G table shock input with a thin stopper material. But

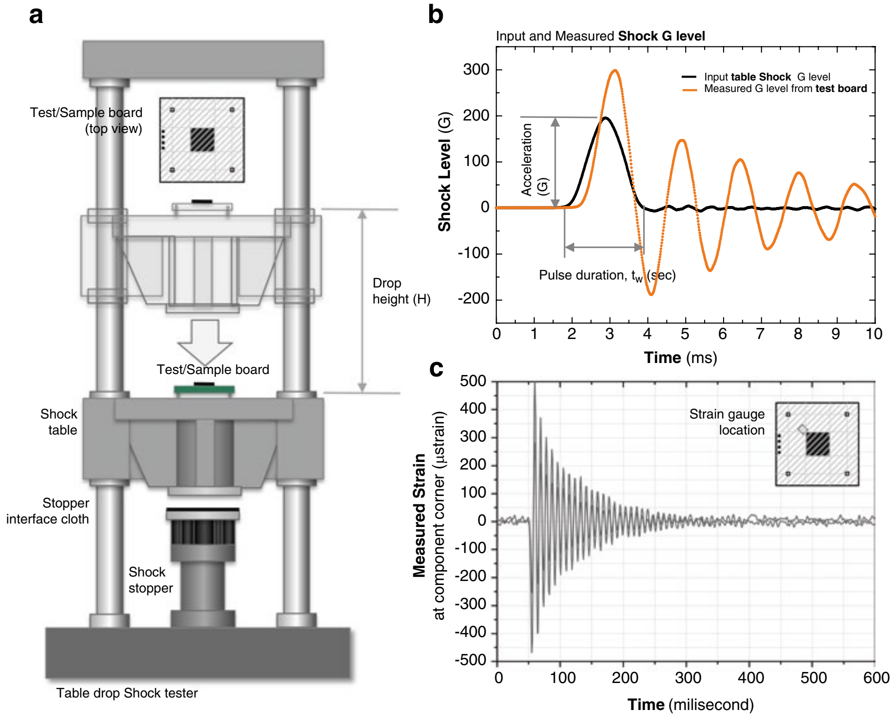

Fig. 6.14 (**a**) Schematic drawing of typical table drop tester. (**b**) Measured G level corresponds to a 200G half sine pulse input shock and (**c**) strain at the corner of the component during the 200G input shock. The acceleration (G) and the pulse duration time (t_w) are indicated in (**b**)

with the same drop height, and slightly thicker stopper (medium thick), the measured input table shock level decreased with further decrease using a thick stopper material. Figure 6.15b shows a slightly different comparison. This time we fixed the input table shock level to 200G. To have the G level reach 200G, the drop height needs to be increased, and at the same time we can see the pulse duration increased also. These two series of examples show the correlation between several factors. Figure 6.16 is the accumulated summary plot and correlations and interaction between those several factors. These correlations are important because it is the combination of the maximum shock level, the shock duration, the frequency, the localized strain, and also the cyclic fluctuation or cyclic fatigue that makes the solder joint degrade and, eventually, fail.

In this section we will begin with the industry standard test methods and understand the behavior of the test board, the strain and G level, and how these values depend on location on the board. The components' shock performance and the failure mode will be discussed followed by effects of pad design, isothermal aging, microalloy compositions, and cooling rate.

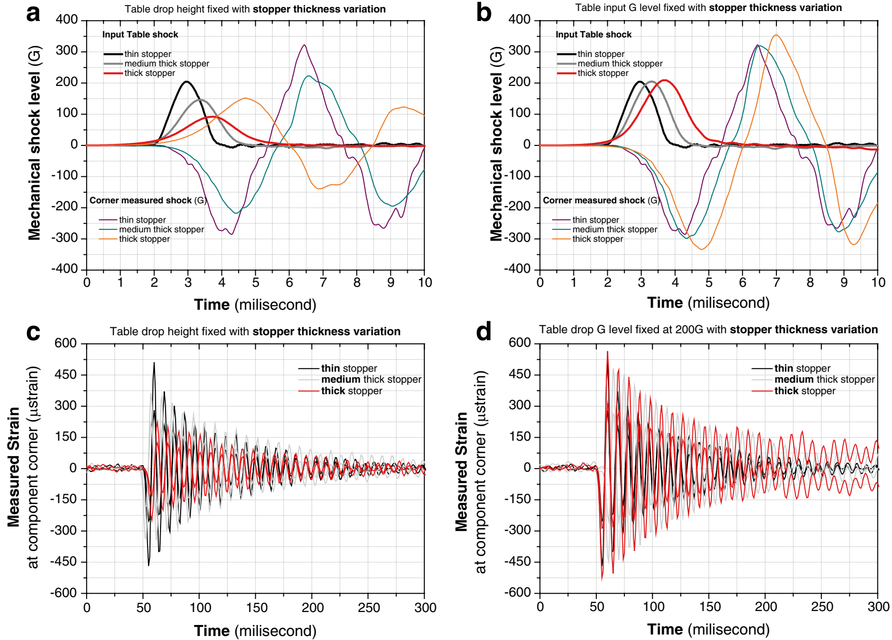

Fig. 6.15 Input shock, measured shock, and measured strain with different shock stopper material selection. (**a**, **c**) Shock G level and strain plot with fixed drop height with three different stopper thicknesses. (**b**, **d**) G level plot and strain plot with increased drop height to fix the input G level. The pulse duration increases with thicker stopper material but the G level decreases with a fixed drop height. To maintain the G level for higher pulse duration time, the height needs to be increased and the induced strain increases with increasing the drop height

Mechanical Shock Test-Related Industry Standards

Because there are various end-use conditions related to mechanical shock, there are a variety of industry standards. The IPC/JEDEC 9703 "Mechanical Shock Test Guidelines for Solder Joint Reliability" and the military spec are a few of the standard test method documents. The document explains the mechanical shock test guidelines for assessing solder joint reliability of PCB assemblies from system to component level. For more handheld devices a more focused standard is document JESD22-B111 "Board Level Drop Test Method of Components for Handheld Electronic Products," with an additional JEDEC standard JESD22-B110A "Subassembly Mechanical shock." The handheld and portable electronic products usually fit into the consumer market segments as handheld electronic products are more prone to being dropped during their service life. This dropping event cannot only cause mechanical failures in the housing of the device but also create electrical failures in the PCB assemblies mounted inside the housing due to transfer of energy through PCB supports. One of the primary drivers of these failures is localized strain exceeding the endurable limit induced by the input acceleration to the board,

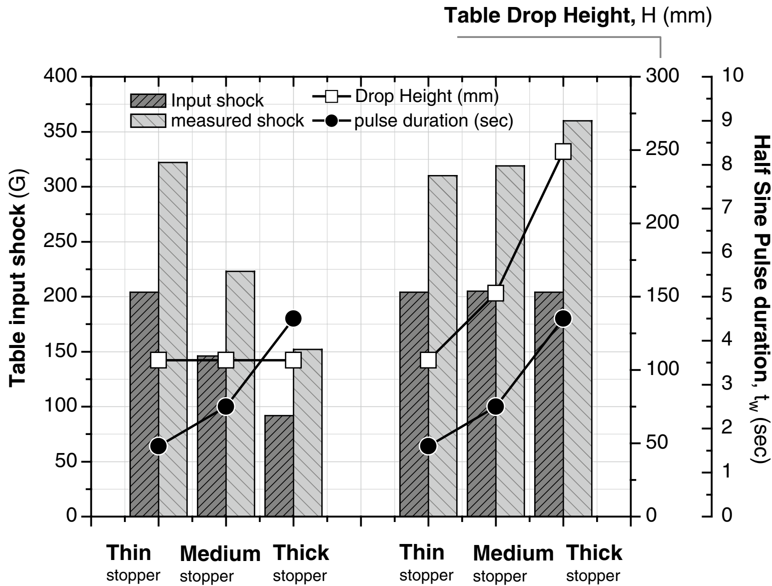

Fig. 6.16 Summary of Fig. 6.15. Input shock, measured shock, and measured strain with different shock stopper material selection. The pulse duration (t_w) increases with thicker stopper material but the G level decreases with a fixed drop height (H). To maintain the G level for higher pulse duration time, the height needs to be increased and the induced strain increases with increasing the drop height

resulting in component, interconnect, or board failure. The failure is a strong function of the combination of the board design, construction, material, thickness, and surface finish material, interconnect material, and component size, which we will address in this chapter.

Several test board designs and layouts are shown in Fig. 6.17, where Fig. 6.17a is a 132 mm × 77 mm (5 × 3 in.) JEDEC test board, with up to 15 components and maximum component size of 15 × 15 mm. For components larger than 15 × 15 mm, a square board (Fig. 6.17b) with hole locations of 5 or 6 in. (125–150 mm) apart is widely used, which usually accommodates one component. While the B111 board is a suitable board for a smaller package size and higher G level shock tests, which are typical of the consumer electronic product sector, the larger square board is for larger and heavier components like FCBGAs utilized in high-reliability product boards with a relatively lower G level test condition. The board in Fig. 6.17c is a modified test board based on the JESD22-B111 test board. The basic design concept for the JEDEC rectangular board was to imply various strain conditions in one board to test the component in variety of conditions. Due to that purpose, the failure cycle number varies by the location of the component on the board. But to reveal the effect of subtle changes in microstructure on the mechanical stability of the joint, an appropriately sensitive test method needed to be established, which can decouple the shockwave-induced failure from the strain-induced failure with a more simple

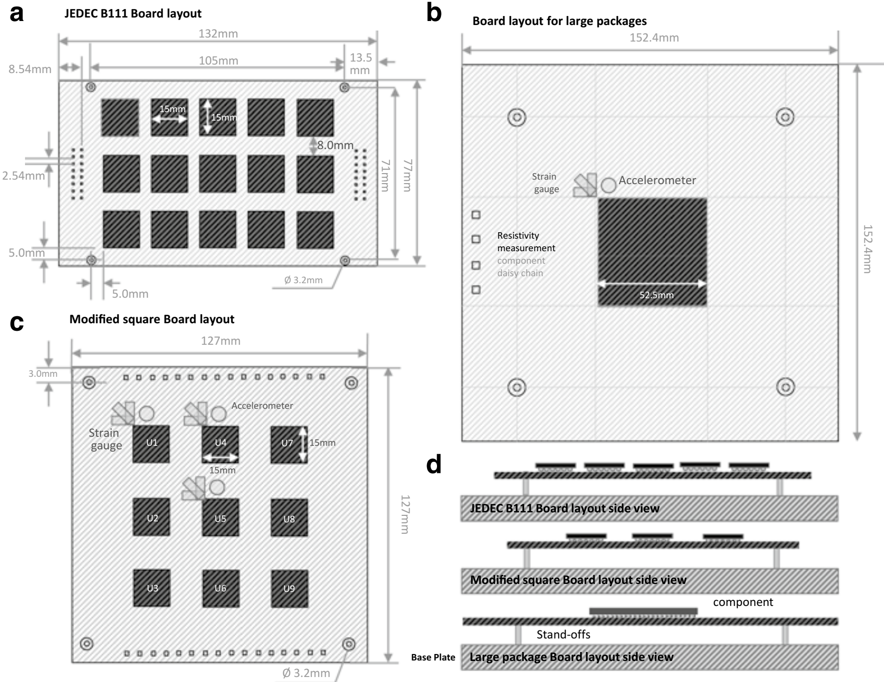

Fig. 6.17 Test size and layout. (**a**) JEDEC B111 board layout. (**b**) Large package shock board layout and (**c**) Modified square board layout. (**d**) side view for each board for shock testing

strain and G level combination test board. The modified 125 × 125 mm square board in Fig. 6.17c is designed to have a uniform condition on four corners and four edges with same strain and G level combination, which made it possible to evaluate the joint stability under various combinations of shock and strain level.

The drop shock test is performed by raising the shock table to the height specified according to JEDEC condition and dropping on the strike surface while measuring the G level, pulse duration, and pulse shape as we saw already in the earlier section. There are various shock conditions as shown in Table 6.2. The widely used test criteria for small packages used in portable and handheld electronics including the tablet computers is Condition B: 1,500 Gs, 0.5 ms duration, half-sine pulse as the input shock pulse to the printed circuit assembly (as listed in JESD22-B110 Table 1 or in JESD22-B104-B Table 1). This is the applied shock pulse to the base plate and is measured by an accelerometer mounted at the center of the base plate or close to the support posts for the board. Other shock conditions, such as Condition H (2,900 Gs, 0.3 ms duration), in addition to the required condition can also be used for more extreme end-use conditions. But for larger components like FCBGA, condition B with 1,500G is too high because larger components like FCBGAs are heavy and could not survive this level of shock unless it has additional support material. Thus

Table 6.2 Component test levels described in JEDEC22 B111

Service condition	Equivalent drop height (in./cm)	Velocity change (in./s)/(cm/s)	Acceleration peak (G)	Pulse duration (ms)
H	59/150	214/543	2,900	0.3
G	51/130	199/505	2,000	0.4
B	44/112	184/467	1,500	0.5
F	30/76.2	152/386	900	0.7
A	20/50.8	124/316	500	1.0
E	13/33.0	100/254	340	1.2
D	7/17.8	73.6/187	200	1.5
C	3/7.62	48.1/122	100	2.0

conditions C, D, and E with 100G, 200G, and 340G are used for larger component applications.

As we discussed earlier, the peak acceleration and the pulse duration are a function of not only the drop height but also the strike surface and the stopper material. Depending on the strike surface, the same drop height may result in different G levels and pulse duration. Theoretically, the drop height needed to achieve the appropriate G levels can be determined by an equation below where H is the drop height and C is the rebound coefficient (1.0 for no rebound, 2.0 for full rebound).

$$A(t) = A_o \sin\left(\frac{\pi t}{t_w}\right)$$

$$\sqrt{2GH} = \frac{2A_o}{C}\frac{t_w}{\pi}$$

However, this equation does not include the strike surface effect. The shock wave can be controlled by controlling the height of the drop table, and also the stopper material (or the thickness of the material), to adjust the shock wave duration. The level of shock and the duration are important factors because the same amount of energy can be achieved with a lower shock level and longer duration than a higher G level with very quick duration. That is the reason why the test standards define also the shock duration, to make it available for comparison.

Mechanical shock-induced failure is based on two major phenomena: a shock-induced strain and a shock wave (G). In general, one can think that with a higher level of shock, the board deflection is larger and producing larger strain and thus inducing solder joint crack at the weakest link. But the higher G level does not always mean a higher strain. The strain at a given shock level is strongly dependent on the component weight and the structure of the board. As shown in Fig. 6.18, the comparison between the JEDEC-B111 rectangular board and the modified square board reveals that the G level of each location shows a similar response, but the strain value is much higher for the rectangular board compared

to the square board, showing the effect of the board geometry and structure. The G level response and strain values are from 1,500G level peak acceleration, 0.5 ms half-sine shock pulse input to the drop table. Even though the JEDEC-B111 rectangular board is the industry standard test board, since the failure locations are too versatile, in this chapter we will mainly use the modified square board (Fig. 6.17c) test results to explain the mechanical shock properties of the solder joints based on the G level and the strain. The square board has a total of 9 components per board and is designed to provide three pairs of different strain and shock conditions: high shock/high strain, which occurred at the center location (U5); low shock/low strain, which occurred at the corner locations (U1, U7, U3, U9); and low shock/high strain, which occurred at the edge locations (U2, U4, U6, U8). With the 1,500G, 0.5 ms half-sine shock pulse, each location, edge, corner, and center shows a different maximum peak G level and response to time wave with the highest peak level at the center of the board. Like this, the G level and strain variation are affected by the geometry of the board and location; the thickness of the board is also an important factor. A series of measurements on three different thickness boards with different level of input shock is presented in Fig. 6.19. As shown in the figures, from a thinner board toward a thicker board, with a given shock input, the thicker board shows a higher peak G level response but lower maximum strain level at most of the locations compared to the thinner

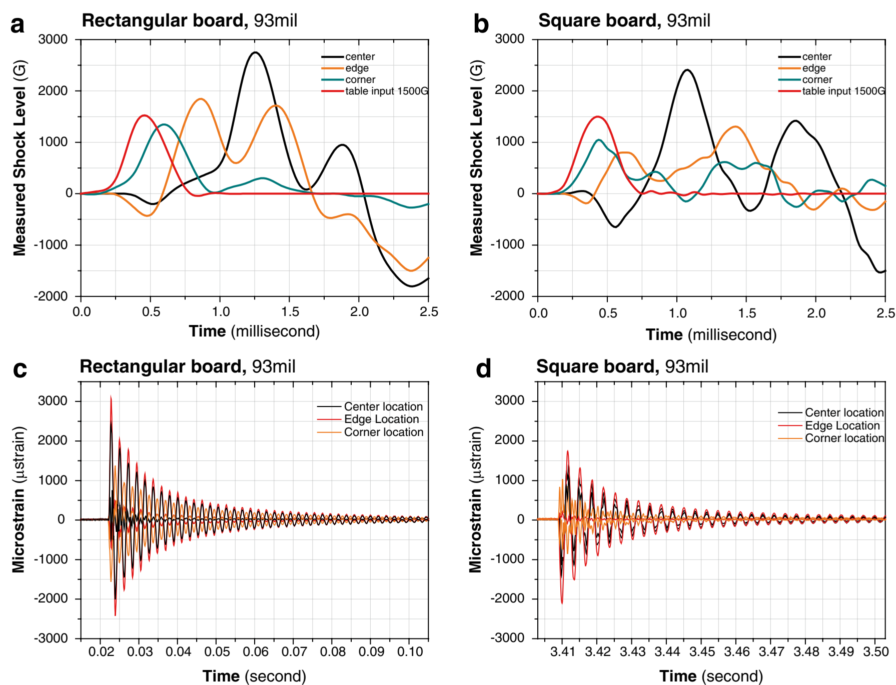

Fig. 6.18 Test size and layout. (**a**) JEDEC B111 board layout (**b**) Large package shock board layout and (**c**) Modified square board layout. (**d**) side view for each board for shock testing

board, which shows the opposite. But the maximum G and maximum strain values are not always the decision makers for the solder joint stability. As shown in Fig. 6.20, the strain response after the first maximum peak has a different fluctuation pattern, which ultimately affects the energy that needs to be consumed by the solder joint before it breaks, the cycle number per time (frequency), and the duration that affects the solder joint stability and determines whether joint failure occurs early or late. For example, the strain for the 31 mil board in Fig. 6.20d shows a higher peak strain compared to the 2.36 mm (93 mil) board strain response, but the strain fluctuation frequency for a given time frame is much less for 0.79 mm (31 mil) compared to the higher frequency of 2.36 mm (93 mil) strain response. Of course, the strain fluctuation and peak value differ with the component location, which is because the shock G level at each component location is different as shown in Fig. 6.20a–c. With these examples, we can see that it is not only the shock G level and the strain maximum peak value that impact the solder joint mechanical stability but also the location of the component and the interaction between the shock-induced strain and the board, which influence the fluctuation of the strain. But this is not all the factor which needs to be considered. The interaction between the strain and the solder joint itself is a critical factor, which we will see in the next sections.

Board-Side Pad Design Effect: NSMD Versus SMD

The failure induced by shock is “a strong function of the combination of the board design, construction, material, thickness, and surface finish; interconnect material and standoff height; and component size” [16]. One additional consideration is the pad design on the PCB side. As shown in Fig. 6.21, from a mechanical bonding point of view, a non-solder mask-defined pad (NSMD)-designed board is different than a solder mask-defined (SMD) board. The NSMD pad shown in Fig. 6.21a has more area of bonding between the Cu pad and the solder ball than the SMD pad. After reflow, the solder ball completely covers and grabs/surrounded the Cu pad; the solder therefore has a larger bonding interface area than the package-side interface. The SMD pad design solder joints are expected to be more directly affected by interface microstructure evolution than NSMD pad-designed boards. This is due to the balanced condition between the package and board-side interface. Both the board side and package side have the same interface bonding area and have no geometrical differences; thus, both the package side and board side have equal potential for local deformation and fracture. With a given shock wave, the potential failure initiation site for the NSMD pads are at the lower part of the Cu pad corner, the interface between the Cu pad, and the laminate on the board side. Compared to the NSMD, the SMD pads have their potential failure site at the interface between the solder and the Cu pad, where the solder bulk is exposed right above the IMC interface layer. We will see the influence of the board-side pad design in the following sections, where the pad design plays a crucial role deciding the failure mode per given isothermal aging preconditions and solder alloys.

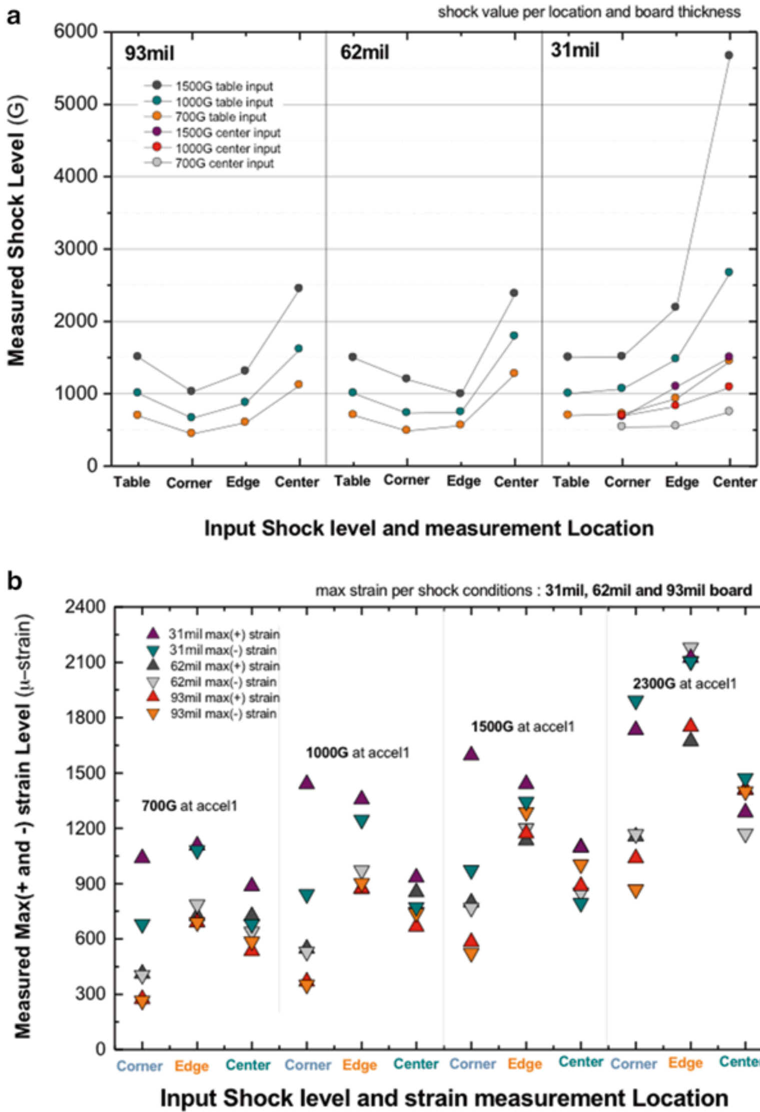

Fig. 6.19 Measured Maximum Shock G level and maximum (+ and −) strain per board thickness and component location. (**a**) Shock level per location and board thickness. (**b**) Strain per location and board thickness. It is interesting to see that the thinner board has lower strain due to the lower weight of the board

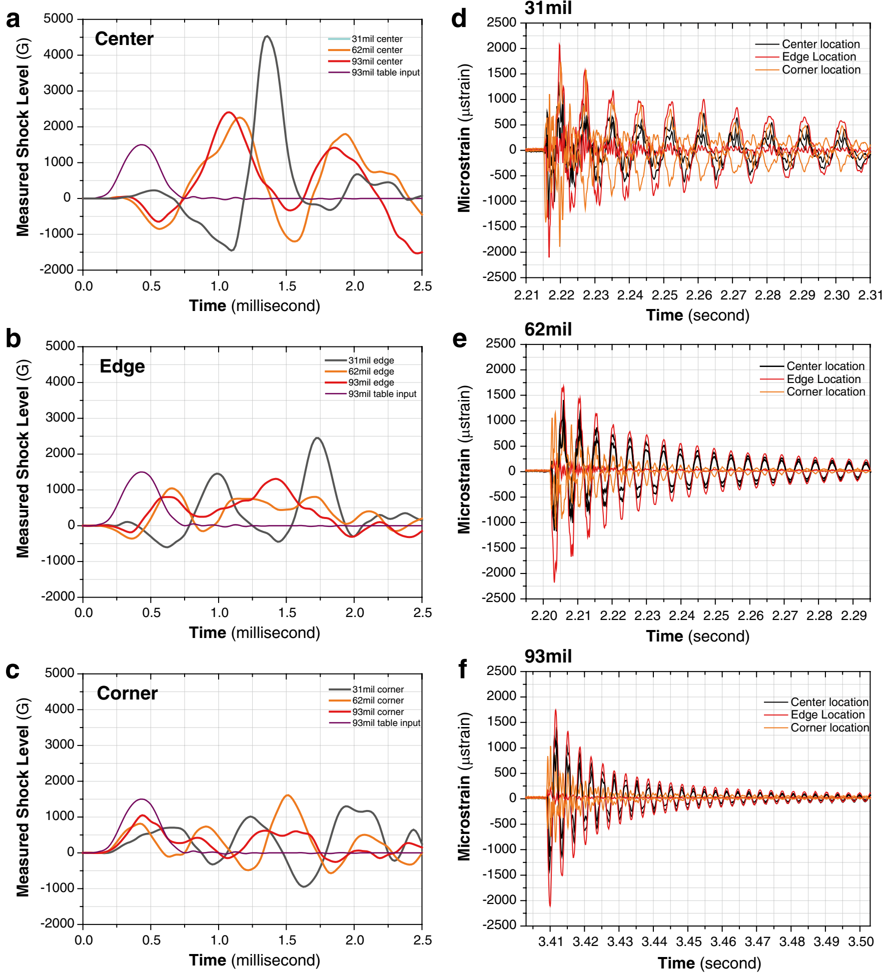

Fig. 6.20 Measured Shock G level plot and strain plot per board thickness and component locations. The shock G level at each component location is different as shown in (**a**–**c**). The strain response in (**d**–**f**) after the first maximum peak has a different fluctuation pattern, which ultimately affects the energy that needs to be consumed by the solder joint before it breaks. The strain fluctuation and peak value differs with the component location

Isothermal Aging Effect on Mechanical Shock

As addressed in Chap. 4 and the impact to thermal cycling performance addressed in Chap. 5, the isothermal aging brings the SAC305 solder microstructure to a transition at two regions. One is the solder bulk and the other one is the interface. The solder bulk become more soften with larger accumulated IMC precipitates, and

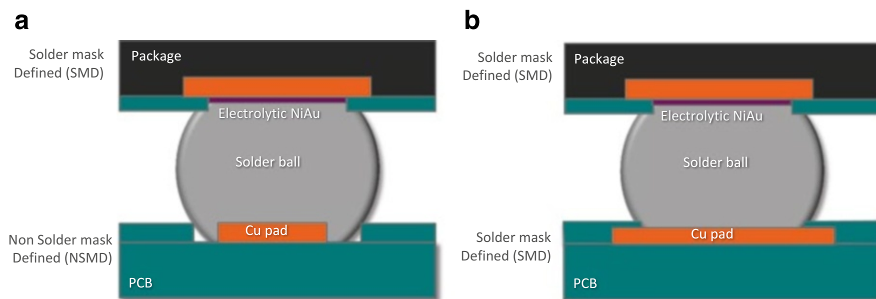

Fig. 6.21 Schematics of cross sections for (**a**) Non solder mask defined board pad design (NSMD) and (**b**) Solder mask defined board side pad design (SMD)

based on the surface finish, some local area near the interface show precipitation-free zones, and the once dendrite-shaped beta Sn with eutectic IMC decoration around it become a more equiaxed grain structure. At the same time IMC thickness increases and shape transformation occurs at the interface. The scallop-shaped IMC structure or a needle-shaped IMC structure are developed at the interface without Ni and with Ni element-contained surface finish and become thicker with a uniform thickness after isothermal aging. The effect of these microstructure evolutions before and after isothermal aging on shock performance can be seen in the following example with 17 × 17 mm FCBGA component shock performance on 2.36 mm (93 mil) thickness boards. The initial microstructure for both package- and board-side interfaces is shown in Fig. 6.22 before and after aging. The shock test was applied utilizing the standard standoffs and 1,500G shock level cycles at the center location of the board. The shock test results are shown in Fig. 6.23. The Weibull plots before and after isothermal aging at 100 and 150 °C for 500 h without regard to the component location on the boards showed a continuous degradation from corner to edge to center and also depending on aging throughout the samples. Focusing on the first failures, the 150 °C/500 h-aged samples failed first followed by 100 °C/500 h-aged and the no-aged samples, and the overall characteristic lifetime cycle number was around 100 cycles. Compared to the NSMD SAC305 samples, the SMD SAC305 samples showed a more isothermal aging-dependent result, as the Weibull curves are clearly separated based on the aging conditions, and the characteristic life cycle number showed a distinct degradation of characteristic life due to isothermal aging. The dye-and-pry analysis, to identify the failure location and failure mode, is shown in Fig. 6.24. It reveals that all the fractures in the NSMD pad test board before isothermal aging were laminate cracks at the board side, regardless of package position on the board. Figure 6.24b shows the dye-and-pry results for the 150 °C/500 h preconditioned components following shock testing. Laminate cracks at the board side were observed as the major failure mode in addition to some failures at the package-side interface. Compared to the mostly laminate crack failure mode in NSMD pad design board samples, the dye-and-pry results for the SMD pad

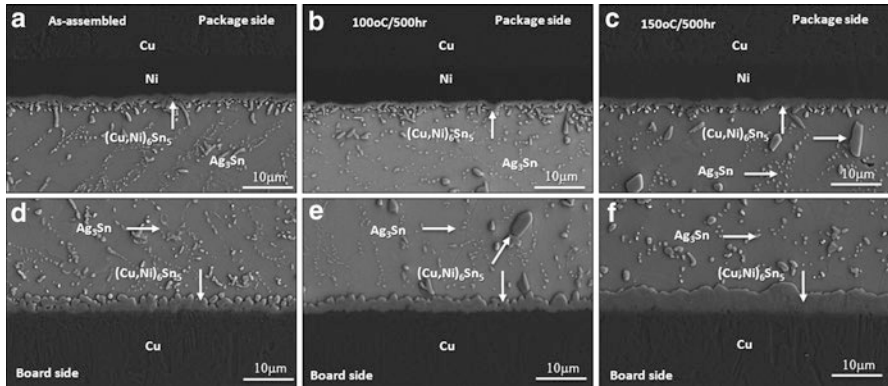

Fig. 6.22 Scanning electron microscopy cross section microstructure of package side (**a, b, c**) and board side (**d, e, f**) before aging (**a, d**), after isothermal aging at 100 °C/500 h 500 h (**b, e**) and after aging at 150 °C/500 h (**c, f**)

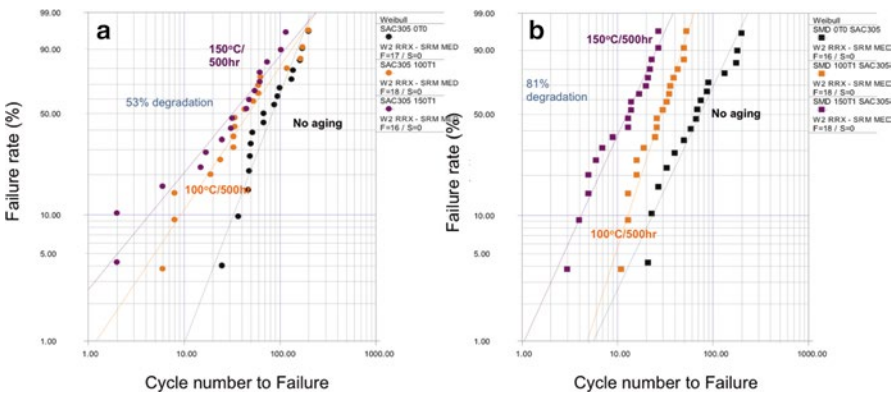

Fig. 6.23 Number of shock to failure Weibull plot before and after isothermal aging. (**a**) NSMD pad test board and (**b**) SMD pad test board results

test board showed different failure modes. As shown in Fig. 6.24c failure occurred primarily at the package- and board-side interfaces, and just a few failures occurred at the board laminate.

While the NSMD test board results showed a stronger joint configuration at the board side, the SMD pads had equal potential for crack development at both the package- and board-side interfaces. This competition between the major crack propagation paths can be seen in the cross-section images shown in Figs. 6.25 and 6.26. In Fig. 6.25, the cross-section SEM from an NSMD sample solder joint after shock

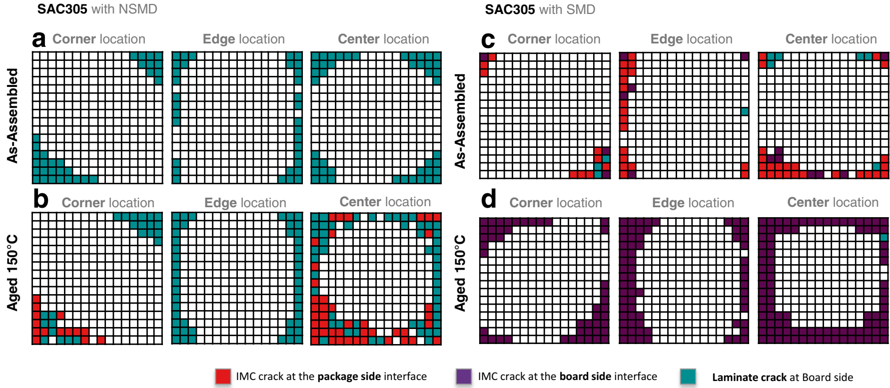

Fig. 6.24 Dye and pry fracture distribution maps after shock test: (**a**) SAC305 with NSMD pad design shock tested right after assembly and (**b**) shock tested after isothermal aging at 150 °C/500 h. (**c**) SMD pad design shock tested before aging and (**d**) tested after isothermal aging at 150 °C/500 h

shows the laminate crack propagated under the Cu trace and eventually cracked the Cu trace (as indicated with white arrows). With the isothermal aging at 150 °C/500 h, the sole failure mode at the laminate begins to show a mixed failure mode, both at the laminate- and the package-side IMC interfaces. On the other hand, Fig. 6.26 is the images from an SMD sample. This time, cracks were observed at both the package-side and board-side IMC interfaces, and after isothermal aging, the board-side IMC interface was the dominant failure mode. The cracks at the board-side interface, shown in Fig. 6.26c, f, were propagating through the (Cu, Ni)$_6$Sn$_5$ intermetallic compound (IMC). The crack propagation path for no-aged samples are more difficult to proceed because the crack needs to penetrate the bulk solder and the IMC, but for 150 °C/500 h-aged samples the crack propagation is much easier resulting in a shorter life cycle time than the no-aged samples. With the help of an EPMA analysis, we can see that the crack was actually propagated through a region between a higher Ni concentration region and a low Ni concentration region shown in Fig. 6.27. A crack propagation through the lower part of the Cu_6Sn_5 IMC can be observed often in other interfaces too. Figure 6.28 is a shock-induced crack propagation for a large FCBGA component before and after aging at 75,100 and 150 °C. With the shape/geometry change of the IMC, the crack path and the relatively ease or difficulty of the crack propagation rate are defined. In this case the 75 °C aged sample showed the lowest shock performance compared to the 150 °C aged sample, which showed the best performance. Unlike the no-aged interface, the 75 °C aged sample interface begins to have a continuous layer of Cu_6Sn_5, and this makes the joint more easy for crack propagation. For the no-aged sample interface, the crack needs to propagate partially through the bulk solder and then back to the IMC and then back to the bulk solder, etc. so the crack propagation is mitigated in some sense. With the same point of view, the 150 °C aged sample with a thicker IMC for both Cu_3Sn and Cu_6Sn_5, the crack propagation is much more difficult, due

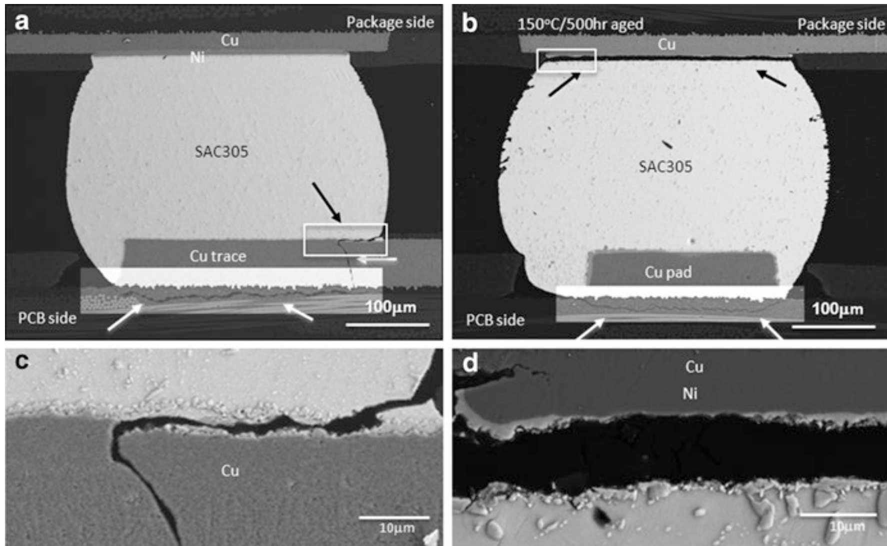

Fig. 6.25 Scanning electron microscopy cross section microstructure of an NSMD sample solder joint after shock shows the laminate crack propagated under the Cu trace and eventually cracked the Cu trace (as indicated with *white arrows*). (**b**) With the isothermal aging at 150 °C/500 h, the failure mode at the laminate begin to show a mixed failure mode, both at the laminate and the package side IMC interface

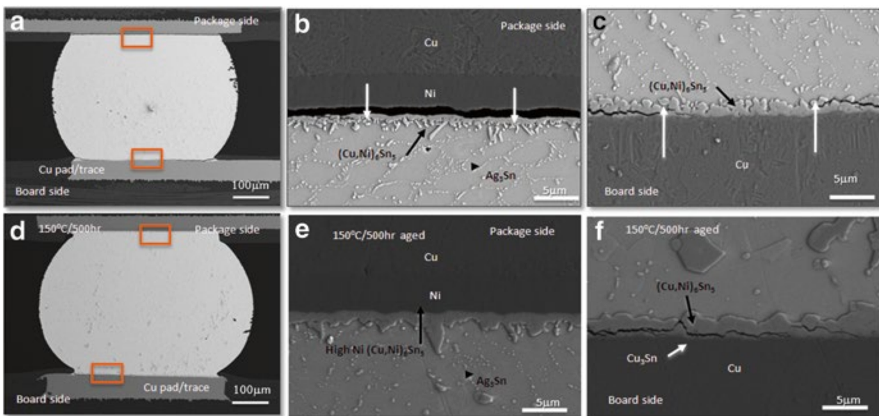

Fig. 6.26 Scanning electron microscopy cross section of shock tested microstructure for unaged package (**a–c**) and package aged at 150 °C/500 h (**d–f**) at low magnification (**a, c**), and at high magnification at locations shown in *boxes* in (**a, d**) along package side (**b, e**) and board side (**c, f**). Crack locations are indicated by *arrows*

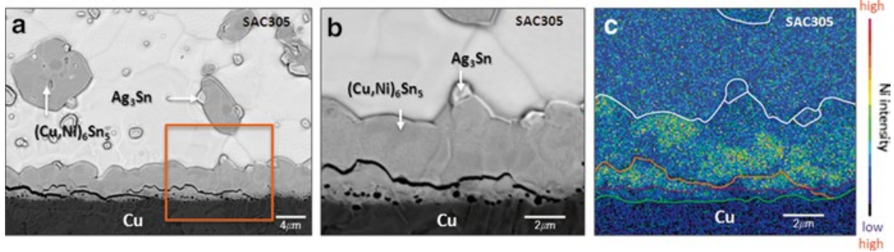

Fig. 6.27 EPMA mapping overlapped on SEM microstructure. Both are SMD pad design samples with (**a**) SAC305 after isothermal aging at 150 °C/500 h and shock tested. (**b**) Higher magnification area indicated in (**a**). (**c**) EPMA map overlayed on (**b**)

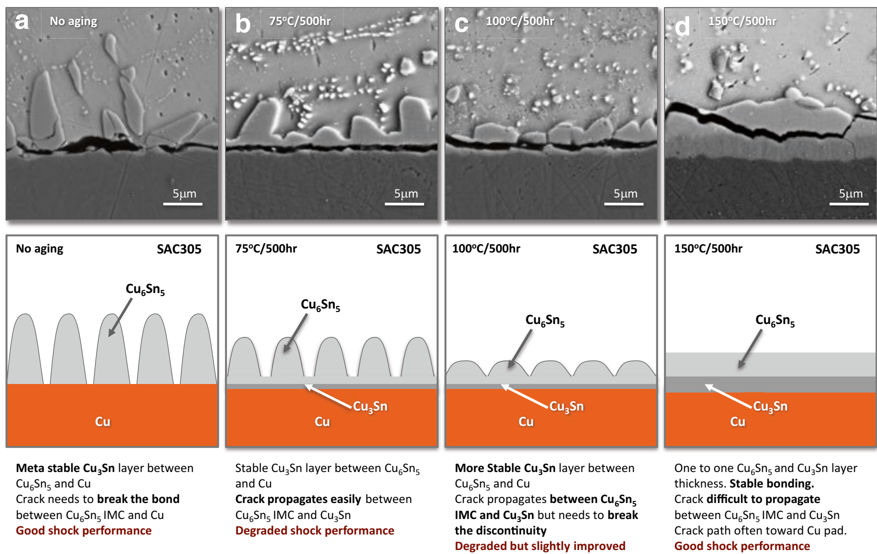

Fig. 6.28 Fracture path based on isothermal aging induced IMC geometry differences. Schematic drawing on the interface after isothermal aging associated with SEM structure after aging

to the irregular interface in between the Cu_6Sn_5 and the Cu_3Sn. The Cu_3Sn IMC layer is an equiaxed columnar grain structure, and the Cu_6Sn_5 covers several of the equiaxed Cu_3Sn grain, thus making the horizontal crack propagation difficult.

Like these examples, the IMC interface thickness, shape distribution, composition, and uniformity is closely related to the stability against shock and is crucial defining the shock performance. But even though IMC interface is often the path where the crack propagates, it is not the only factor which defines the shock performance. We will see another factor in the next section, which can degrade or improve the shock performance, the solder bulk itself.

Increasing the Capability of Absorption of Shock Energy

With the degradation phenomenon observed as above, the mechanical reliability and stability of the solder joint at higher temperature are challenging, because higher temperature environment means isothermal aging on the solder joint, which can transfer the microstructure of the solder and ultimately degrade the performance level. Then how can we improve the shock performance in these alloy systems. Based on the failure mode, the shock can be improved by enhancing two major regions, the IMC interface at the package and board-side interface and laminate area below the Cu pad.

Thus, adding some microalloy to the surface finish or bulk solder alloy is an active approach along with finding a way to strengthen the laminate with material enhancement or new pad designs. But maybe a more fundamental approach is to increase the capability of the solder joint to absorb the shock energy input caused by external loads. This is an important approach and direction since it can achieve two things at the same time, by not only strengthening the solder joint itself but also reducing the shock energy reaching the IMC interface and laminate area below the Cu pad by mitigating the energy transfer into adjacent weak interfaces. Given that failure locations vary from the package-side interface intermetallics to the laminate area right below the Cu pad or trace, mitigation or delay of crack initiation can be accomplished if a mechanism by which the solder joint bulk can absorb more shock energy [27, 28]. In the next sections, we will discuss about a few mechanisms and methodologies to improve the shock performance, including strengthening the IMC layer with microalloy, increasing the shock absorption with microalloyed bulk solder composition change and altering the initial internal buildup stress. But before going into the methodology, we will begin with a basic comparison between low and high Ag-contained solder joint shock performance and the mechanism which defines the difference.

Low Ag Alloy Versus High Ag Alloy

It is not a new finding that the lower silver content alloy performs better in mechanical shock performance than higher silver content Sn–Ag–Cu solder, which is demonstrated in several reported results [29, 30]. Most of the results were explained by a simple mechanism that less Ag content results in fewer Ag_3Sn IMC precipitates and thus a softer bulk solder compared to higher Ag solder alloys. This softer bulk material transfers less shock-induced strain at the interfacial stress concentration locations, resulting in a better shock performance, which is true and a valid explanation. With isothermal aging, the IMC particles coarsen into larger, fewer, and more widely spaced IMCs in the microstructure [29–31], which also provides a softer and more shock-tolerant microstructure. If we can explain the improved shock performance in lower Ag-contained SAC solder by only identifying the difference in hardness value, then we can also reach to a conclusion that isothermally aged SAC305

solder joints, which has lower hardness than no-aged SAC305, are expected to have better shock performance compared to no-aged SAC305 solder joints, which is actually not the results we see in SAC305 solder joint shock performances.

Then is there a different failure mechanism in SAC305, higher Ag content solder compared to SAC105, lower Ag content solder joints?

To explain and to understand the mechanism, we need to look into the microstructure evolution during shock test. We will compare SAC105 solder alloy with SAC305 solder alloy to assess the effect of isothermal aging and local recrystallization on high G board-level shock performance, observe and discuss the different shock-induced microstructure changes, and try to find the right mechanism, which defines the shock performance and solder joint stability.

The initial microstructure for both SAC105 and SAC305 is shown in Fig. 6.29. With lower Ag content (SAC105), the Ag_3Sn IMC precipitates are less in number thus overall showing a lower hardness value compared to SAC305, which has fine IMC precipitate distribution. Both SAC105 and SAC305 show an accumulation of these IMC precipitates after isothermal aging with interface IMC thickness increase. The shock test was performed with 12 × 12 mm CABGAs assembled on a 1.57 mm (62 mil) board with the test condition B (1,500G, 0.5 ms shock pulse).

Figure 6.30a, b shows the compiled shock test Weibull plots for each aging condition and solder alloy composition. Overall, there are higher numbers of cycles to failure for SAC105 than SAC305 before or after aging. In contrast, the SAC305 samples show a much lower unaged characteristic life cycle number of 42 cycles, but it degraded further to 12 cycles after aging at 150 °C for 500 h. Since the thickness of the IMC at both package and board-side interface increased, both SAC105 and SAC305 solder joints are expected to show degraded shock performance. But the shock performance of SAC105 solder joints improved with aging. The consolidated plot for each condition with regard to the component location on the board

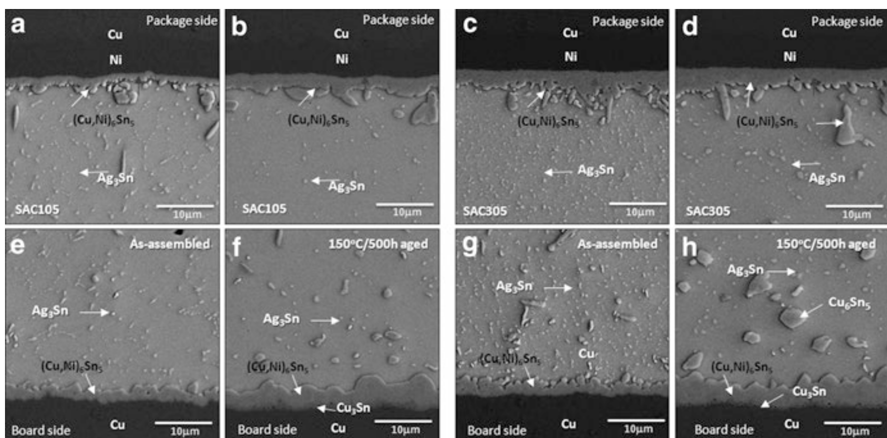

Fig. 6.29 Scanning electron microscopy cross section microstructure of SAC105 (**a**, **e**) before aging and (**b**, **f**) after aging at 150 °C/500 h. SAC305 before aging (**c**, **g**) and after aging at 150 °C/500 h (**d**, **h**)

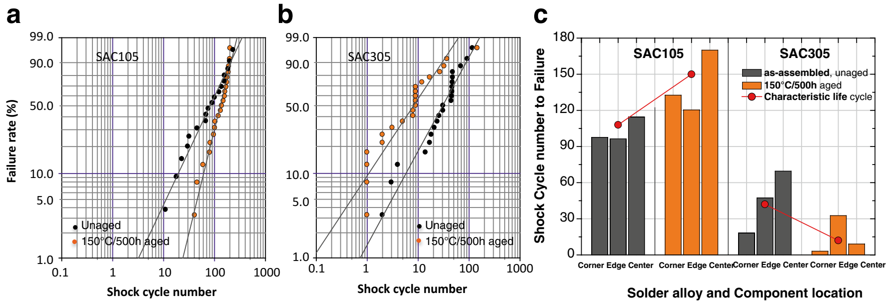

Fig. 6.30 Weibull plots for shock test results on the isothermal aged BGA samples: SAC105 (**a**) and SAC305 (**b**). (**c**) Number of cycles to failure and characteristic life cycle number based upon component location and isothermal aging conditions for SAC105 and SAC305

shows the trend more clearly in Fig. 6.30c, and this trend is consistent for every package location on the test board. The center component showed an especially high improvement rate compared to the corner and edge locations in SAC105. SAC305 on the other hand shows the highest degradation rate for the center-located components. Given that this opposite aging effect is greatest at the center location, which also has high strain level and shock level per test cycle, those solder joints at the center location are good joints to look into the microstructure and were selected for further observation. The cross-section-polarized light microstructure of the outermost five joints on each side of the outside edge is shown in Fig. 6.31. The crack locations are typically at the upper interface or in the laminate below the board-side copper pad, as indicated by an outlined box. Most of the unaged solder joints before shock test have single, bi-, or tri-crystal structure with a small number of grains per joint for both SAC105 and SAC305. However, after shock testing, the SAC105 microstructure revealed development of a fine grain (possibly recrystallized) microstructure that is much finer for isothermally aged than the unaged samples. This transformation from single or dual grains to multigrain or fine localized grain structure may account for better absorption of the shock-induced strain energy. The transformation from single to multigrains during shock cycling produced many additional grain boundaries. As there are elastic discontinuities at grain boundaries that cause local stress variations, dislocation generation at grain boundaries is likely. With this microstructural transformation, the shock strain energy can be absorbed in two ways: by motion of dislocations nucleated at grain boundaries and by grain boundary sliding so that the shock conveyed to the interface region is reduced. This form of energy consumption will increase in proportion to number of new grain orientations and/or grain boundary area. This transformation during the shock cycling thus can reduce or delay damage accumulation at the high stress concentration locations at the intermetallic interface layer or at the laminate and Cu pad interface. In contrast, SAC305 samples (Fig. 6.31d–f) show much less of a difference in the fine grain microstructure development. The initial grain structure

does not appear to have changed significantly even after isothermal aging and shock testing. This lack of change indicates that the SAC305 is less able to absorb the shock-induced strain energy, so it transfers the shock energy to the weakest interconnection interface, which in this case is the IMC layer at the package side or to the laminate and Cu pad interface, resulting in a much earlier full failure than the SAC105 samples.

Figure 6.32 shows four exemplary cross-section SEM and polarized light microstructures with and without 150 °C/500 h aging and then shock tested to failure for SAC105 and SAC305 joints. The SEM microstructure shows the crack location, and the polarized images show the grain structure associated with the crack. The SEM images revealed shock-induced crack propagation from the package-side interface corner into the bulk solder for SAC105 aged samples. The unaged joint showed a crack propagation initiated from the upper right corner into the bulk, and the aged joint shows crack propagation from both side corners. Also a laminate crack is shown below the Cu pad area in both solder joints, which are L1 joints from two different center components. The corresponding polarized light images show a fine grain structure development at the joint corner region.

In contrast to SAC105, in SAC305 joints, the crack propagated into the laminate region, and there are very few fine grains in the SAC305 joints. This contrast suggests that the fine grain structure provides much more energy-absorbing sites with

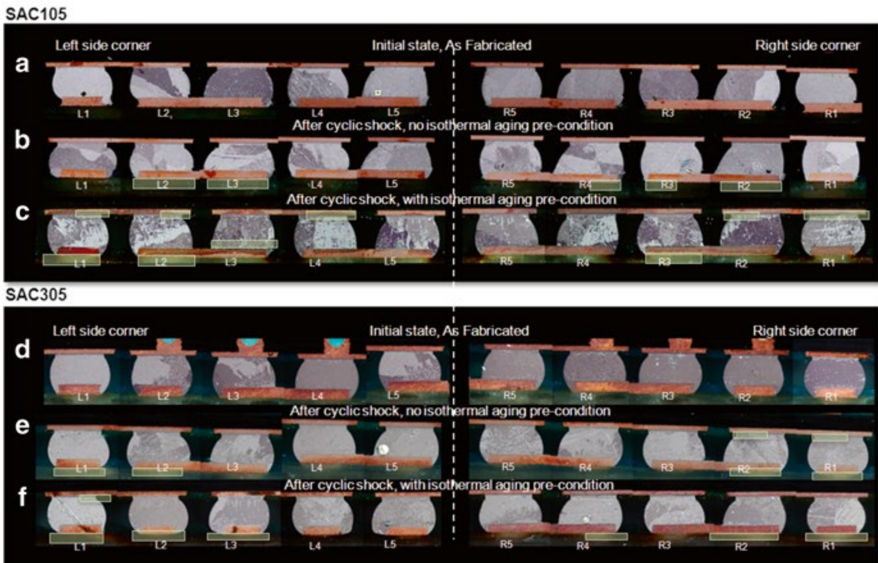

Fig. 6.31 Polarized light microstructure cross sections of the 10 joints marked in Fig. 1 before and after shock testing. (**a–c**) SAC105 and (**d–f**) SAC305. As assembled (**a, d**), after shock test (**b, e**), and after 150 °C/500 h aging and shock test (**c, f**). The crack locations are indicated by *boxes*

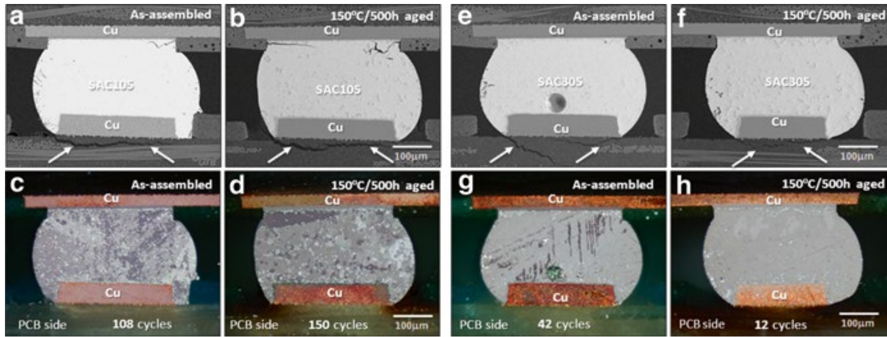

Fig. 6.32 Selected cross-section SEM and associated polarized image microstructure before (**a, c, e, g**) and after 150 °C/500 h aged (**b, d, f, h**) and then shock test to failure for SAC105 (**a–d**) and SAC305 (**e–h**). The SEM microstructure shows the crack location in the joint and laminate (*white arrows*) (**a, b, e, f**) and the polarized images show the grain structure associated with the characteristic life cycles to failure indicated (**c, d, g, h**)

the increase in the number of grain boundaries. The compliance and easier deformation of SAC105 bulk solder in the interconnects led to the better absorption of the shock-induced strain energy, which in turn resulted in multigrain or finer grain microstructure development, possibly through both dynamic and static recrystallization during and following each shock event. Without the fine grain structure development in SAC305, deformation of the bulk solder was difficult and little shock-induced strain was absorbed, which ultimately transferred the stress and strain directly to the IMC and the Cu trace laminate interfaces, resulting in an earlier crack initiation and propagation than the more shock-absorbing SAC105. In addition to the effect of the alloy composition and precipitate microstructure, isothermal aging increased the shock absorption capability and actually improved the shock performance in SAC105. After isothermal aging in the SAC105 joints, the bulk solder became softer, which further promoted bulk solder deformation and increased absorption of the shock-induced strain energy. Due to the increased strain energy absorbed, microstructure features such as IMC precipitates coarsening and consequently wider particle spacing occurred, which favored dislocation accumulation that enabled recrystallization. But in SAC305, isothermal aging degraded the shock performance. Even though the hardness decreased after aging, the ability to transform the single-grain structure to a much finer multigrain structure was not accelerated, thus the ability to absorb the shock energy was not increased, and the thicker IMC layer at the interface resulted in a weaker interface structure that ultimately resulted in a degraded shock performance after aging.

In this section, we learned that if the solder joint can absorb more shock energy by single to multigrain transformation or by developing more grain boundaries with recrystallization, we can have an improved shock performance. In this case we saw the difference between the low and high Ag solder alloy comparison, but is there any alternate method to increase the capability of the joint to absorb shock energy?

The Cooling Rate Effect

As we saw in the former section, if we can accelerate or trigger the single to fine multigrained structure during shock test, we can improve the shock performance. Then what kind of methodology can we bring into the solder joint to accelerate this phenomenon? One of the methods is by controlling the cooling rate. With fast cooling, the solder joint tended to build up more stress, which generated more dislocation activity, which can be released by recrystallization during shock impact. In contrast, slow cooling can lead to the development of mechanical twins, and these interfaces provided more locations for energy dissipation during shock and thus extended the lifetime (if there is no large-scale microstructure evolution to release the stress right after cooling). Once if the internal stress is maintained and then triggered to be released during shock test, then we can have a more accelerated fine grain structure transformation, which can absorb the shock energy and delay the crack initiation and propagation.

Figure 6.33 is the microstructure before and after shock testing, after applying three different variation cooling rates from slow to fast cooling. For the normal cooled samples, we can observe an overall grain number increase after shock testing, but compared to the normal cooled samples, the fast cooled sample shows a dramatic increase of fine multigrained microstructure right after shock test. This fine grain structure transformation can absorb a huge amount of shock energy, contributing to delay the crack initiation or propagation, which resulted in an improved solder joint shock performance. In this experiment, 12×12 mm CABGA with 0.5 mm pitch were used, and the fast cooled samples were cooled with a cooling rate of 75 °C/s. The shock result came out as we expected. A 140 % increase in cycle number to failure with the fast cooled samples as shown in Fig. 6.34. The slow cooled samples also show improved shock performance compared to normal cooled samples.

Microalloy Effect: Pd

An additional way to improve the shock performance is by shock absorption with facilitating mechanical twin formation. Like single to fine multigrained structure transformation, mechanical twins can form by shock-induced strain but also can be facilitated with microalloy addition to the solder joint composition. The effect from the microalloying can be also seen in higher Ag-contained SAC305 solder alloy. This is actually an interesting phenomenon from an industry application point of view because it is known that having a higher Ag content shows better thermal cycling performance than SAC105 solder alloy. But with maintaining the thermal cycling performance, if there is a method to facilitate the twin formation for improving the shock performance simultaneously, it will provide good practical applications.

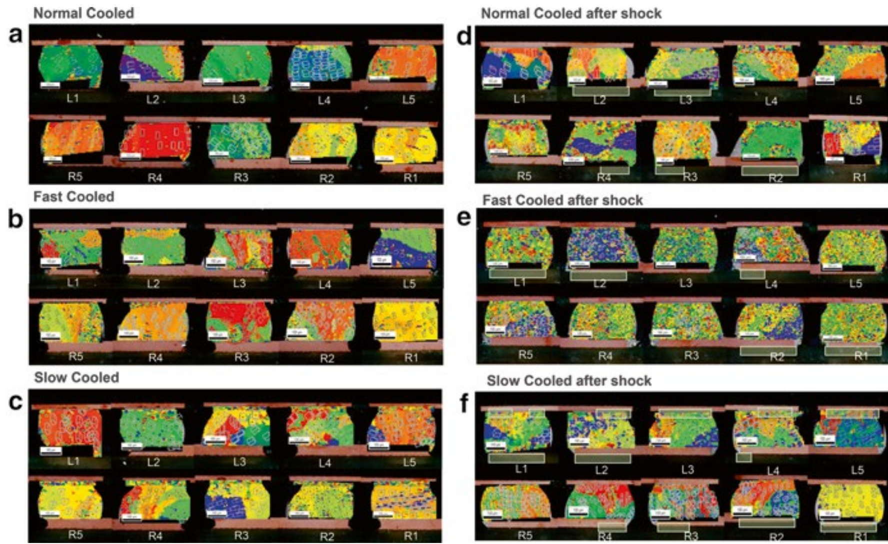

Fig. 6.33 OIM images for sample before and after shock test per three different cooling conditions. Before shock test (**a**) Normal cooled, (**b**) Fast cooled, (**c**) slow cooled. After shock testing (**d**) normal cooled, (**e**) fast cooled, (**f**) slow cooled. Fractured crack locations are indicated in *white box*

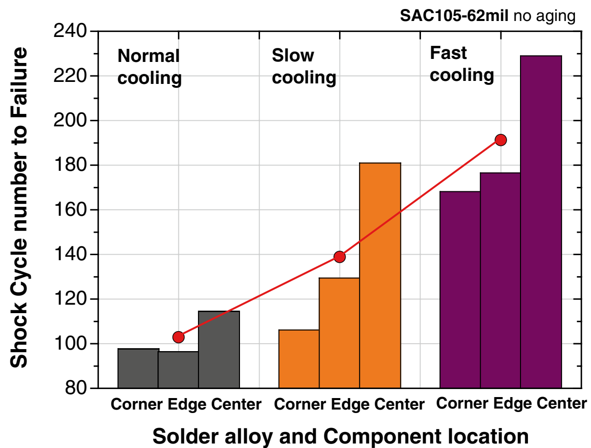

Fig. 6.34 Shock cycle to failure per cooling condition for each component location

Among the elements, which can induce accelerated twin formation is Palladium (Pd). As shown in Fig. 6.35, the SAC305 + Pd solder joints showed an overall higher cycle number in each location, which leads to a cumulatively higher characteristic life cycle number as summarized in Fig. 6.35c. The characteristic life cycle number for the unaged condition improved 65 % by adding Pd to NSMD pad samples, and the trend of improved shock performance was even greater for the 100 and 150 °C aged conditions, 132 % for 100 °C aged, and 102 % with 150 °C aging. However,

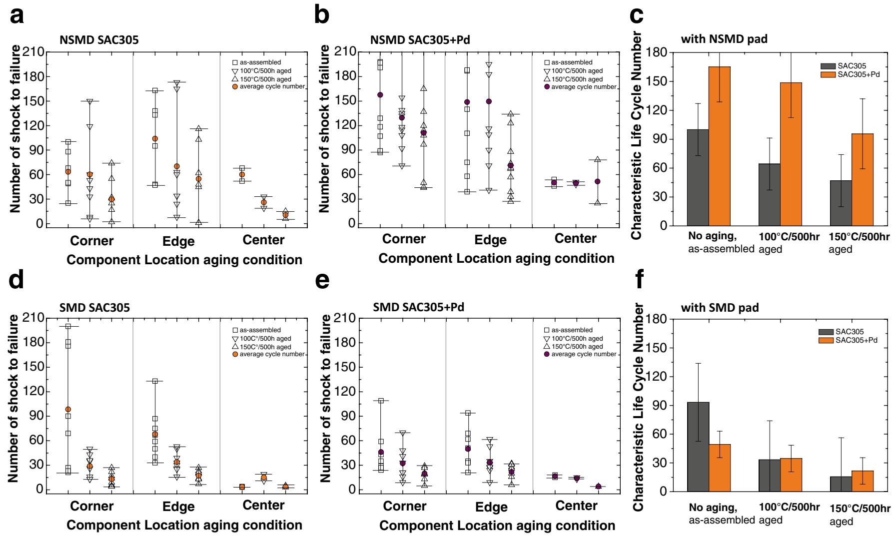

Fig. 6.35 Number of cycles to failure based upon component location and isothermal aging conditions for NSMD (**a**–**c**), and SMD (**d**–**f**) pad designs for SAC305 (**a, d**) and SAC305 + Pd (**b, e**). Characteristic life cycle number summary comparisons of aging conditions illustrate the strong benefits of Pd for the NSMD pad (**c**) but not for the SMD pad design (**f**)

with the SMD pad design, there was little to no improvement of shock performance, as shown in Fig. 6.35d, e, where the location-based cycle to failure numbers are similar for SMD SAC305 and SAC305 + Pd samples. To assess a potential explanation for the beneficial effects of Pd, the Sn grain microstructure was analyzed using OIM to examine how the microstructure changed before and after shock testing for NSMD SAC305 and SAC305 + Pd samples. OIM scans were performed, and the OIM images are overlaid on the cross section where the cracks are identified in a manner similar to that reported in [32]. As shown in Fig. 6.36, the SAC305 OIM microstructure after the shock test shows no obvious change in the microstructure from the as-solidified microstructure and shows joints containing mostly single-crystal orientations. In contrast, the Pd containing joints shown in Fig. 6.36b, d show many more interfaces and refinement features in the microstructure while retaining the as-solidified large grain features. Two particular SAC305 + Pd solder joints A16 and B16 show localized grain refinement or recrystallization and significant twin deformation inside the bulk solder joints, which are enlarged in Fig. 6.36e, f. The finer precipitate structure increases the hardness and, hence, raises the yield stress, which is a condition that is often necessary to stimulate deformation twinning in other materials [33]. In joints A16 and B16, active deformation twin structures are evident, which are rarely observed in SAC305 samples. Given the fact that the SAC305 + Pd solder joints exhibit more deformation twin grain refinement features following the shock test, activation of deformation twins may dissipate strain energy within the joint and thus may provide an explanation for why SAC305 + Pd can absorb more shock-induced impacts than SAC305, resulting in a high characteristic cycle number to failure.

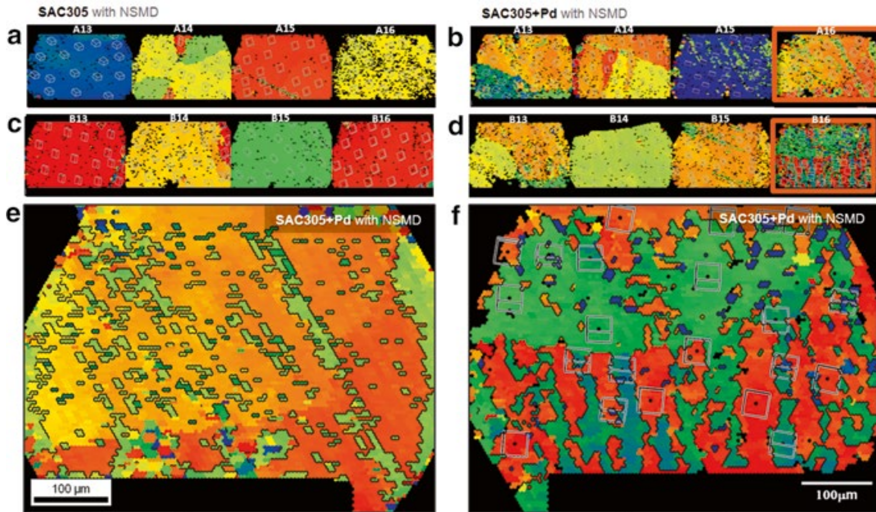

Fig. 6.36 OIM images from cross-section images for SAC305 (**a**) unaged and shock tested from U4 (Fig. 2) side B, (**c**) shock tested, from U6 side A. SAC305 + Pd (**b**) unaged and shock tested, from U4 (Fig. 2) side B, (**d**) shock tested, from U6 side A. (**e**) higher magnification of Fig. 10b joint A16, (**f**) higher magnification of Fig. 10e joint B16

Hence, the activation of deformation twinning has the most influence in conditions where the board interface strength is sufficient to sustain a higher stress (which may never be reached in the SMD geometry because IMC interface cracks can form at the maximum stress concentration location). The effect of the Pd to induce mechanical twinning to dissipate energy allows more cycles before essentially the same number of failure sites is achieved in the NSMD design without Pd. Also, it is evident that the mechanical twinning energy dissipation reduces the driving force for package-side interfacial cracks.

Summary

Mechanical stability is emerging as critical reliability concern with a rapid expansion but not limited to mobile electronics. In order to properly apprehend their risk factors to the reliability, this chapter described the threat from each mechanical load and the mechanism by which the solder joint fails. This chapter describes the reliability performance and failure mechanisms of Pb-free solder joints under various mechanical load conditions, including bending, cyclic bending fatigue, and mechanical shock. The structural stability of solder joint under such mechanical loads is an important consideration factor for the current and future solder interconnects because

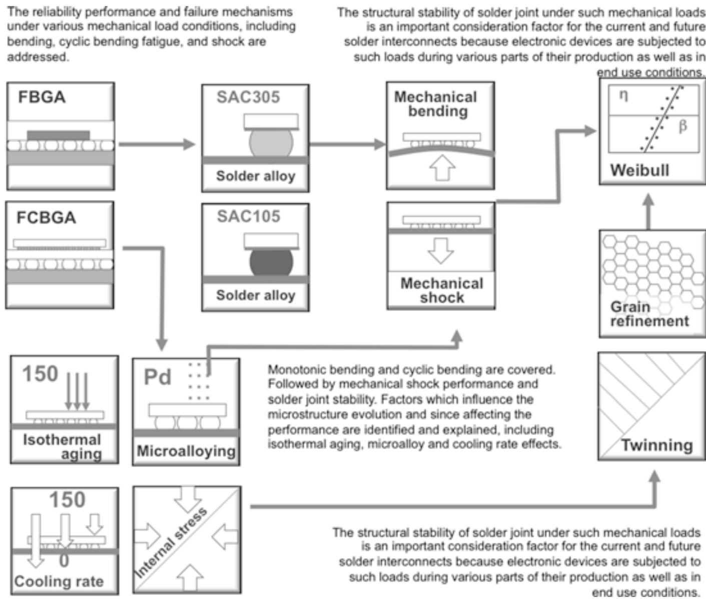

Fig. 6.37 Overall summary diagram of Chap. 6

electronic devices are subjected to such loads during various parts of their production as well as in diversified end-use conditions. As shown in Fig. 6.37, the summary of this chapter is presented schematically. As described in the earlier part of this chapter, the identified factors and approaches we discussed can elucidate how deformation mechanisms operate. The learning leads us to the thought process on how to emphasize and utilize the capability of the solder joint and how much energy it can absorb, which ultimately defines and improves the mechanical stability of the system.

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