Tae-Kyu Lee · Thomas R. Bieler
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Fundamentals of Lead-Free Solder Interconnect Technology

From Microstructures to Reliability

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ISBN 978-1-4614-9265-8 ISBN 978-1-4614-9266-5 (eBook)
DOI 10.1007/978-1-4614-9266-5
Springer New York Heidelberg Dordrecht London

Library of Congress Control Number: 2014949343

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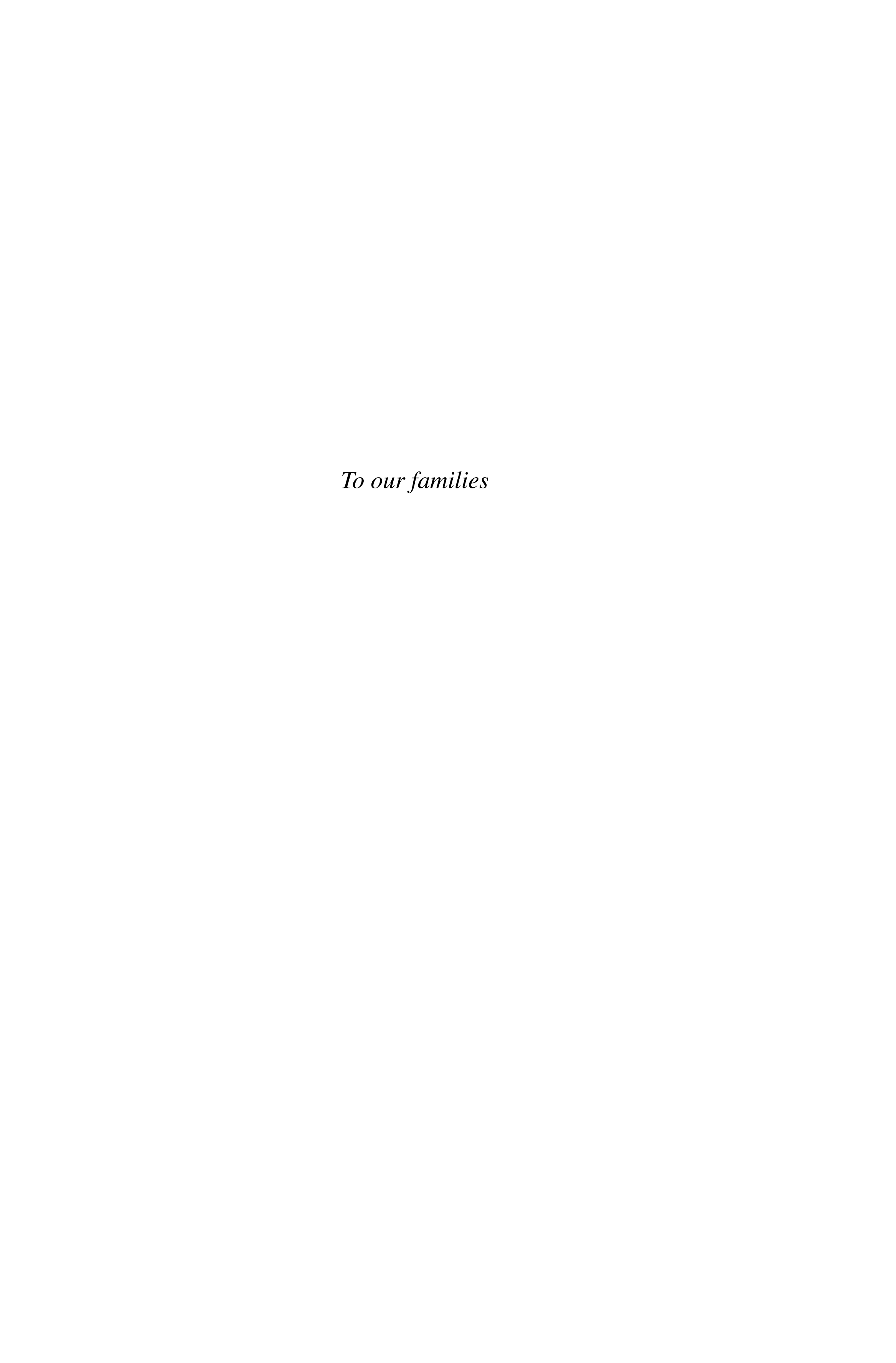

To our families

Preface

The wonders of modern technologies may seem to be achieved by the development of exotic materials such as Si and GaN single crystals, graphene, and nano-materials. However, what is not well known is the fact that those wonders exist simply because of seemingly benign-looking small piece of a metallic alloy known as solder. Without them effectively and cheaply carrying power and signals from one device to the other, all the technological advancements essential for modern and future life are likely to disappear. It must be a surprising experience to anyone to realize that what we enjoy is possible because of cheap Sn-rich solder. In essence, solder joints or solder interconnects connect the world and therefore are infrastructure essential for our daily life.

Tin itself, a long friend to human civilization as it enabled the Bronze Age (in a supporting but invisible though extremely important role), may have a higher ambition since it was shaped into a sphere-shaped solder ball that is connecting the world together. Maybe it saw over the years its friends, Si, a near neighbor just upstairs, and fellow metals Cu and Fe, become dominant players in bringing our civilized structure into the global village we live in together and decided to leave behind a supporting role to become one of the bigger elements.

This book is about lead-free solder technology based strongly on microstructure evolution and reliability in application perspective, but during the preparation of the book, the authors saw a more fundamental story, reflecting many aspects of the world of materials. Since the property and function of the interconnect is a combination of microstructure and chemical composition, it is surrounded by all possible phenomena that we can see in various metallic materials.

We will see the interaction between several interfaces and layers. The properties of these individual but connected layers have interesting relationships since if you strengthen just one layer, the failure layer just shifts to a different weaker link. So understanding the interconnect is to begin with individual layer and expanding the understanding to the whole system. Without understanding the whole system, it is hard to come up with a valuable assessment or reliability and further along to find a solution for a better and stable interconnect.

This book is the tip of the iceberg from the point of view of making the performance of solder joints and, thus, the performance of electronic systems predictable, as most designs are made so that the joint fails before other components do. Predictable performance of an electronic system depends on predictable performance of tin in solder joints. Making this prediction is challenging because tin has rather unusual properties for a metal, as it is very anisotropic. To make its performance predictable, effective material models are needed. To make a useful model, the mechanisms of deformation and damage nucleation and growth must be understood, and these mechanisms are becoming more and more clearly understood in the past few years.

One of the major challenges in the current decade is to predict microstructure evolution and hence property evolution from the beginning to end of life of an electronic product. When this becomes possible, design for reliability can be realized. In contrast to fluids, this challenge is especially large for solid materials, because the deformation and thermal history lead to irreversible changes in microstructural features that affect how the next incremental change occurs. Hence there is a history/memory effect that requires knowledge of all that has happened prior to a given point in time and space, all the way back to the point of formation of the crystal. This is in contrast to fluids where there is no long-term memory of past conditions, and only the most recent history is needed to predict the next incremental change.

So we will begin with the single bulk solder material, then consider what differs in solder joints, then interconnects, and then the thermal, mechanical, and chemical performances followed by future challenges in next-generation electronic devices.

We hope that our growing appreciation for the complexity of Sn and solders and, in particular, its ways of adapting to a continuously changing environment can support you in your efforts to improve the reliability and performance of the electronic systems that our modern culture depends on.

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Acknowledgments

The authors acknowledge the support of NSF funding for a GOALI grant (Grant Opportunities for Academic Liaison with Industry), which involved work by MSU faculty Thomas R. Bieler and Farhang Pourboghrat and PhD students Bite Zhou and Payam Darbandi. Also acknowledged is the grant and female graduate student fellowship support from Texas instruments in conducting research on solder joint reliability at UT Arlington. A number of PhD students and research staffs, including Huili Xu, Liangshan Chen, and WoongHo Bang, were supported from the grant, and their research work has greatly inspired critical discussions made in this book. The authors also want to acknowledge the valuable discussion between several university groups including Prof. Jeng-Gong Duh's group in National Tsing Hua University and Cisco interconnect technology team in the technology and quality group.

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Chapter 1
Introduction

The foundation of this book is that mechanical and functional properties are defined by microstructure, atomic bonding structure, and chemical composition [1]. This is approached by following the path of microstructure evolution and identifying the microstructure interaction with the external environmental factors. Before getting into these factors and their influence and effects, we will consider the interaction between the electronic device and our daily life. With the world covered with more electronic devices and the higher dependency on the signals into and out of these devices, identifying the elements that react to these external factors is crucial. In this chapter, we will briefly look into the overall landscape we are living in and the variety of design expectations of electrical components and devices in various end-use conditions. We will identify external factors and their relationship with the term "reliability."

Electronic Device in Our Lives

Electronic devices are used virtually everywhere. Since Ewald Georg von Kleist and Pieter van Musschenbroek invented the Leyden jar in 1745, an electrical storage device, considered as one of the first uses of electricity for an electric circuit [2], and after William Watson discharged the Leyden jar through a circuit in 1747 [3], electronic devices have been in our everyday lives ever since. Of course it needed several revolutionary milestones like the invention of the transistor, the personal computer, and the Internet, which ultimately connects revolutionary milestones to enable us to reach the entire world today. But it is clear that we are more attached to electronic devices than at any other time in history.

During this revolutionary transformation, electronic devices not only evolved in its internal function, but they have evolved in their ability to connect with other devices. First, the power grid dominated, by connecting houses and factories, and then the telephone transferred a very small amount of information compared to

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T.-K. Lee et al., *Fundamentals of Lead-Free Solder Interconnect Technology*,
DOI 10.1007/978-1-4614-9266-5_1

today's data capacity through copper lines. Today, it is the still evolving Ethernet cable that connects the world with high-speed information and streaming data input from virtually everywhere, from a personal electronic device to the massive traffic of information into and out of a "cloud" or in another term, an era of "Internet of everything (IoE)."

With this connectivity, data transport, and control over various electronic devices, the functionality of a device is becoming more versatile, and the end-use conditions are getting much broader. Areas once not reached by electricity now have massive current flowing through electric devices, serving as critical controllers, which are ultimately responsible for the safety of their users. Figure 1.1 depicts the overall relationships we live within with representative devices used in our daily life, directly or indirectly, from a simple handheld device to transportation control systems and energy monitoring devices.

A good example of the deep penetration of electronic components and devices into our daily life can be found in the automobile sector. Compared to a decade ago, we have many more electronic devices in our cars. There are basic on/off switches, brake control systems, electronically controlled shock absorbers, engine and transmission control systems, GPS and entertainment systems connected to the Internet, and so on. With the increasing variety of devices, the role of these electronics becomes crucial to assure the safety of the car and its occupants, while being more efficient, more fun, and more informed. Automobiles have become some of the most advanced electronic products on the market today. With the introduction of in-car instrumentation, navigation capabilities, safety features, and so-called infotainment technologies, the vehicle electronic systems become increasingly complex. As a result, the challenge to assure the reliable performance of automotive electronics

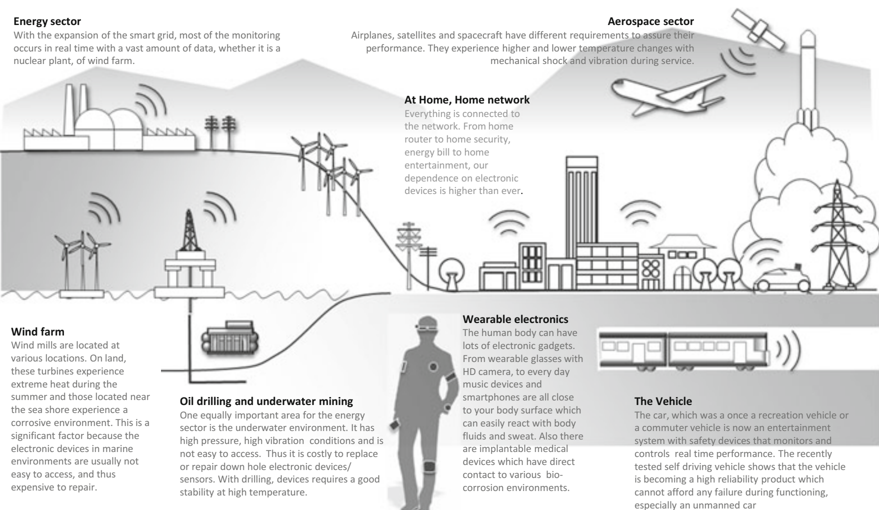


Fig. 1.1 Overall landscape of electronic use conditions from sea level to underground, vehicles, our bodies, and home

is greater than ever. Self-driving vehicles are in development, which ultimately need a very high level of reliability to assure that the vehicle and the adjacent vehicles on the road will be safe. A shift from a vehicle loaded with noncritical and independent electronic systems to a highly integrated and reliable system is becoming a reality.

A similar high-reliability level is required in other sectors such as Internet routers in the telecommunication industry. A vast amount of information and data need to be delivered with a high bandwidth and without interruption. The aerospace sector needs assured reliability both for airplanes and ground systems, because repairing a satellite is too expensive to be a viable option. The same is true for ocean wind turbines. Offshore wind farms are regions where the most wind exists, which are often a place on earth where extreme environmental and temperature fluctuations exist, from very cold static conditions with no wind to hot daytime temperatures with high wind. These wind turbines experience high vibration and corrosion environment, which are all challenges to the long-term reliability of devices. But one of the most severe thermal and mechanical shock and vibration environments for electronic systems is the oil drilling sector. Underground drilling sensors, like the satellites in space, cannot allow a reliability issue since it is too expensive to repair [4].

Given the demands and opportunities, how can we confidently say that an electronic device or system is acceptable and safe to use for an important safety-related end-use condition and be qualified as reliable? To make that assessment, the service conditions the device experiences need to be identified, define the important factors and boundary conditions that affect the stability of the device, and find the degradation mechanism(s). Using this approach, the expected lifetime of the device can be estimated.

Revisiting the automobile example in Fig. 1.2, a regular thermal cycling is expected if the vehicle is exposed to open air, with day and night thermal cycling, or during winter and summer, but a more direct thermal challenge comes from the engine itself.

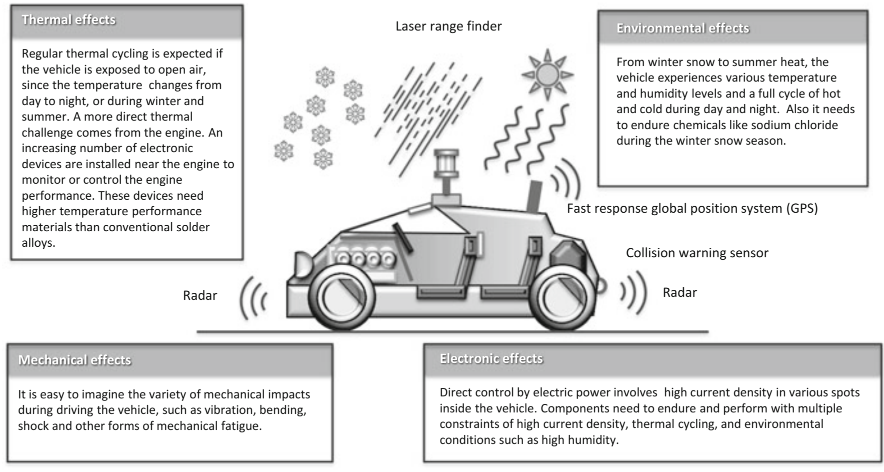


Fig. 1.2 An example, in this case a vehicle, what external factors can influence and impact the stability and functionality of the electronic device during service

An increasing number of electronic devices are installed near the engine to monitor or control the engine performance. These devices need higher temperature materials, where conventional solder materials are inadequate. From winter snow to summer heat, the vehicle also experiences various humidity levels and needs to tolerate chemicals like sodium chloride during the winter snow season. It is easy to imagine the variety of mechanical impacts like vibration, bending, shock, and other mechanical fatigue processes during driving the vehicle. The electric or hybrid vehicles, which are directly controlled by electric power, also have high-density currents in various locations inside the vehicle circuitry. An increasing number of components perform with high current density combined with severe environmental conditions. Thus, there are thermal, mechanical, electrical, and environmental challenges which need to be overcome in an electronic loaded car to be reliable for a long enough time. It is important to learn from the drastically failed components, to know the mechanisms responsible for electronic system degradation and failure, and it is often challenging to find a solution that will mitigate one mechanism, without facilitating another mechanism that can cause failures.

Expected Lifetime

The expected lifetime of a component varies with the character of the device and its purpose or end-use condition. Table 1.1 shows the general life expectancy based on several practical categories [5]. For example, the expected lifetime for a personal computer or a smart phone is not the same as a commercial aircraft. As shown in the table, the expected lifetime of a commercial aircraft is 10 years with a tolerable failure rate of 0.001 %, which is a very high expectation compared to a 2-year life expectancy with 1.0 % failure rate for consumer electronics. Then how can we insure that our products will meet these expected lifetimes for each electronic product category? What do we need to consider to make this product function safely? The answer can be found in the next section “Reliability.”

The Difference Between Quality and Reliability

As we have a variety of devices, we have also a variety of different reliability expectancies. Reliability can be defined in various ways, but a representative definition is the quality or state of being reliable or the extent to which an experiment, test, or measuring procedure yields the same results on repeated trials. There are also some expanded definitions, such as the idea that an item is fit for a purpose with respect to time; the capacity of a designed, produced, or maintained item to perform as required over time or the probability of an item to perform a required function under stated conditions for a specified period of time; or the durability of an object [6].

Table 1.1 Product categories and worst-case use environments for surface mounted electronics [5]

Product category (Typical application)	Worst-case use environment				
	T_{min} °C/°F	T_{max} °C/°F	ΔT °C/°F	Typical years of service	Approx. accept. failure risk, %
Consumer	0/32	60/140	35/63	1–3	1
Computers and peripherals	0/32	60/140	20/36	5	0.1
Telecomm	–40/–40	85/185	35/63	7–20	0.01
Commercial aircraft	–55/–67	95/203	20/36	20	0.001
Industrial and automotive-passenger compartment	–55/–67	95/203	20/36	10–15	0.1
Military (ground and shipboard)	–55/–67	95/203	40/72 and 60/108	10–20	0.1
Space	–55/–67	95/203	3/5.4	5–30	0.001

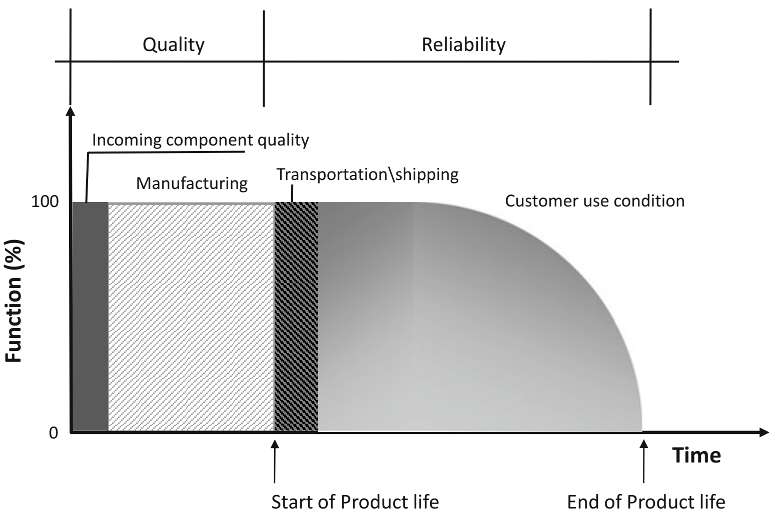


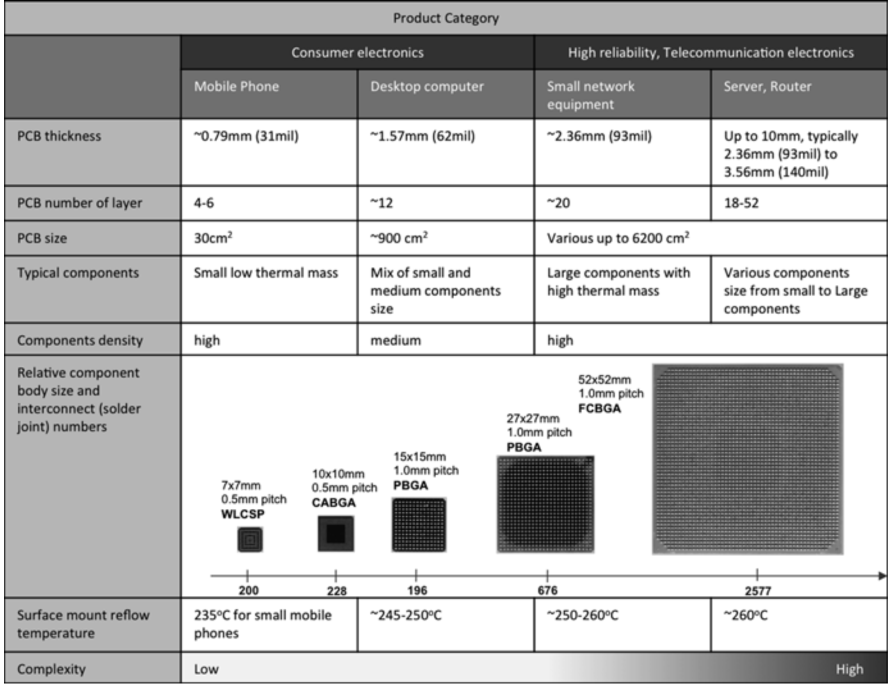
Fig. 1.3 The difference between quality and reliability schematically shown

Before we discuss reliability directly, we often face confusion between quality and reliability. As the definitions state, quality and reliability are different terms with a common ground. Quality is more related to the transition between manufacturing and the beginning of the device life cycle. As shown schematically in Fig. 1.3, a few factors among several that affect quality are the defect rate in the process during assembly and the component quality itself. For example, during assembly of an electronic circuit board with numerous components, either a highly defected group of components or a wrongly calibrated assembly temperature profile can cause a lot of defective boards, which are functionally failed even before sending out to the field. These are considered quality issues and not reliability issues.

Of course, a defective board can escape from the early filtering process and cause failure during early service, but once again this is a quality induced failure, not a reliability issue. Once the product is qualified to be released to the market by passing all the required tests, the life of the product or device begins. As the device functions and is used in their anticipated environment, various mechanisms occur to degrade the device and finally make it fail in a region where the weakest link begins to emerge near the end of life, which is expected by both the designer and the user. Reliability is the more natural behavior of the electronic device or the product if all the construction and quality expectations are met. Thus, it is important to understand the mechanisms that cause the device degradation, in other words, degrade the reliability. Also important is to identify what factors accelerate or decelerate the degradation mechanism to accurately estimate and predict the life and mitigate the unexpected failures.

The Scope of This Book: The Book in a Nutshell

We will go deeply into the fundamentals of the solder interconnect reliability from thermal, electrical, mechanical, and chemical aspects, but before that, we will discuss the details of various package types, the structure of the interconnect, and the character and properties of solders. As shown in Fig. 1.4, there are a variety of electronic components in various sizes and configurations. In Chap. 2 we will visit various package types, which face their own challenges whether thermal or mechanical. Small packages have fine pitch and small solder balls attached with a relatively large die to body size ratio, which can impact the thermal cycling performance. Large body size packages are heavy, potentially facing mechanical stability challenges, and some components can reach high temperatures at peak functions, which directly alters the microstructure and the properties of the system and hence, its reliability. Also, the base plane printed circuit board (PCB) in which the components will be assembled varies with size, thickness, and materials used. These impose all kinds of mechanical responses from external factors as shown in Fig. 1.5. As Fig. 1.4 shows, the layer count and the component density varies based on the product applications and thus varies in expected reliability levels. Consumer electronics usually need small form factors with high density to make the product thin, light, and portable. These consumer products actually don’t need a very long thermal cycling lifetime but need a very stable mechanical performance since it is portable. On the other hand, the telecommunication sector doesn’t need small components, but it needs to accommodate various high-density components in a very good signal integrity package to achieve a high-speed process capability. The thermal cycling needs a very long and reliable performance to function in the field usually for more than 10 years. These products are mostly not handy and portable, but because components are heavy, the product needs to endure shock impacts during transportation and handling. Then there are of course high-reliability products that need everything, like military and harsh environment electronics, with portability, high density, large



Product Category				
	Consumer electronics		High reliability, Telecommunication electronics	
	Mobile Phone	Desktop computer	Small network equipment	Server, Router
PCB thickness	~0.79mm (31mil)	~1.57mm (62mil)	~2.36mm (93mil)	Up to 10mm, typically 2.36mm (93mil) to 3.56mm (140mil)
PCB number of layer	4-6	~12	~20	18-52
PCB size	30cm^2	~900 cm^2	Various up to 6200 cm^2	
Typical components	Small low thermal mass	Mix of small and medium components size	Large components with high thermal mass	Various components size from small to Large components
Components density	high	medium	high	
Relative component body size and interconnect (solder joint) numbers	7x7mm 0.5mm pitch WLCSP: 200; 10x10mm 0.5mm pitch CABGA: 228; 15x15mm 1.0mm pitch PBGA: 196		27x27mm 1.0mm pitch PBGA: 676	52x52mm 1.0mm pitch FCBGA: 2577
Surface mount reflow temperature	235°C for small mobile phones	~245-250°C	~250-260°C	~260°C
Complexity	Low			High

Fig. 1.4 The difference between consumer electronic device and high-reliability devices/ equipment

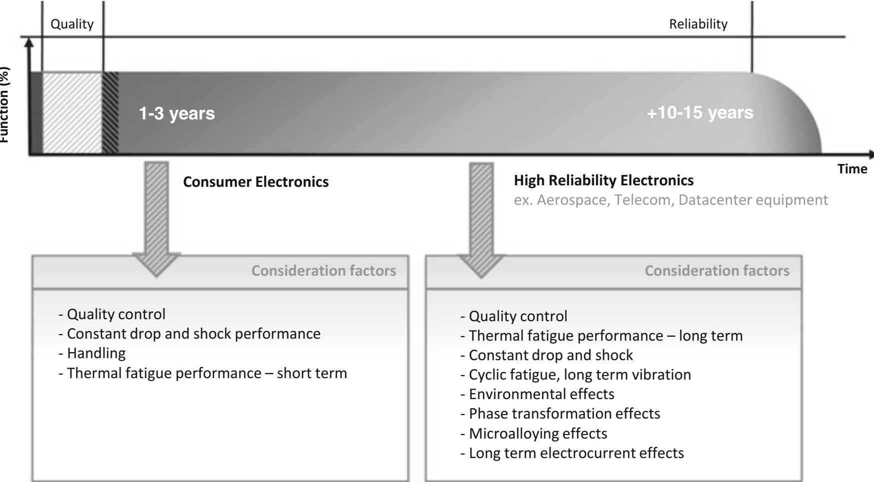


Fig. 1.5 Expected reliability for high-reliability products is higher and the expected lifetime is longer than typical consumer electronic products

components, shock performance, vibration performance, good thermal cycling performance, etc. Based on their reliability expectations and end-use conditions, there are factors that need to be considered at a higher priority than others. As shown in Fig. 1.5, the diagram shown in Fig. 1.3 can be modified and expanded to include the long-term reliability electronics. There are several additional factors which are not considered for short life electronics but crucial for long-term/high-reliability application products.

What Affects Reliability

Then what kind of factors affects the life of a certain product or component? The variety of end-use conditions, which imposes the external environmental factors, can be seen in a device exposed to an outside environment. The typical climatic weather and day to night cycles produce a characteristic thermal cycle. This external thermal fluctuation also occurs in devices in controlled environments. A server in a very good air-conditioned room also experiences thermal fluctuation because the components are constantly functioning with an on/off state and the junction temperatures increase and decrease based on the feedback control settings of a cooler, which keeps the temperature constant for better functionality. Another easily seen factor is in our everyday handheld devices, where a simple drop can impact the whole device with various shock waves and strain fluctuations, a mechanical factor. Mechanical shock and bend and vibration are a few representative factors that can directly affect the electronic device. More extreme environments can be found in moving vehicles and equipments, which have moving parts in it. Even the hard drive can produce vibration which can affect the mechanical stability of the nearby located interconnects. Another crucial factor, which is probably a core factor in this category, is the effect of current flow. For example, in an interconnect with a high current density, the joule heating occurs and brings the component into a higher temperature state. When combined with a moving vehicle, the complexity can be even more increased if it is, for example, winter outside. We can easily have a multifactor combination of thermal, electrical, mechanical, and even chemical factors that can all affect the reliability of the product or component (e.g., salt and defrost chemicals on the road during winter).

Figure 1.6 summarizes the major external factors in various application products in a few categories. For example, some of the portable consumer products have relatively short lifetime expectancy and are expected to be stable against a few mechanical drop/shock; thus, the thermal fatigue performance doesn't need to be so much improved as the long-term life expectancy products, in which expected lifetimes are more than 10 years. With the same thought path, a long-term high-reliability product, which sits in a controlled room, does not need an extremely high-shock performance. With these consideration factors and end-use conditions in mind, a design window can be defined. But most important, one should know the mechanisms of how the

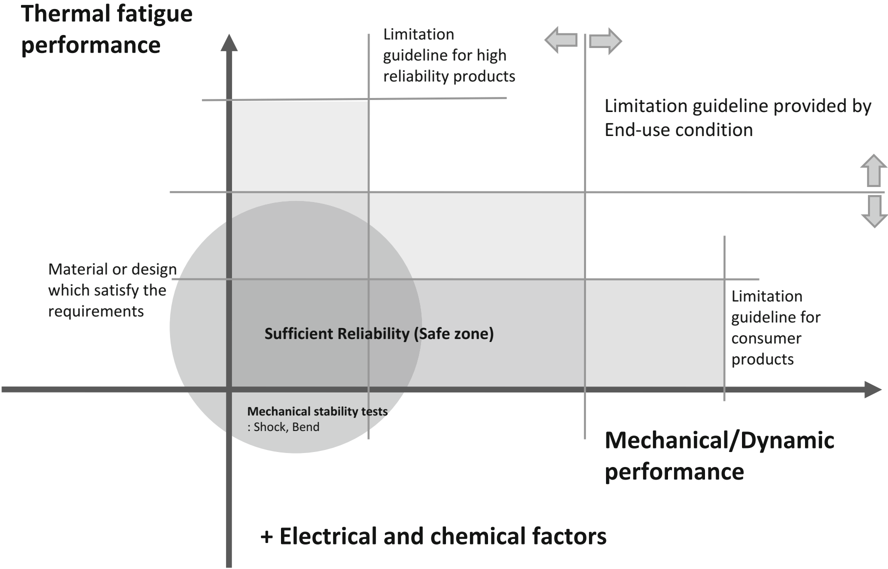


Fig. 1.6 External factors and categorized performance including thermal, mechanical, and electrical/chemical factors

performance interacts with the external end-use conditions. Knowing how and how fast the degradation to failure happens will lead us to the understanding of the degradation/failure mechanism, which ultimately leads us to the right methodology and solution mechanism, which can mitigate and improve the performance one desired.

Reliability Prediction and Improvement

Then how can we estimate or assess whether the reliability is acceptable or not and make improvements if needed? Reliability prediction is the combination of creating a proper reliability model together with estimating and identifying the mechanism, requiring the definition of the input parameters for the model (e.g., failure rates for a particular failure mode or event and the mean time to repair the system for a particular failure) and to provide a system or component interconnect level estimate for the output reliability parameters (e.g., system availability or a particular functional failure frequency). It is realistically impossible to wait until a target component fails and record the failure time to assess the lifetime of a certain device. A more effective and clever way to assess the lifetime in a reasonable manageable time frame is needed without sacrificing time and losing any meaningful data. Thus, accelerated tests are used to identify such parameters.

There are well-established methods and deep analytical strategies which provide various approaches to achieve what we need. One of the strategies is "qualitative tests" and the other is "quantitative test" methods. One additional method is environmental stress screening (ESS) [7]. The goal of ESS is to expose, identify, and eliminate latent defects which cannot be detected by visual inspection or electrical testing but which will cause failures in the field. ESS is performed on the entire product or component and does not involve sampling. A qualitative test method is an accelerated test. Because it shows the failure mode only, it is also called a shake and bake test or highly accelerated life test (HALT) [8]. These methods overstress products to obtain failures as quickly as possible, but the end of the test has no reliability information. Hence, the qualitative test is more commonly applied to a relatively small number of specimens subjected to a harsh environment. If the specimen survives, it passes the test. This test method can give the engineer a benefit of revealing the potential failure modes, but the reliability information is limited, and it is often not clear whether the failure mode observed in this test is really the failure mode that will occur in real service conditions.

Unlike qualitative testing, quantitative accelerated life testing is designed to provide reliability information on the product, component, or system. Time to failure can be in any quantitative measure, such as hours, days, cycles, miles, etc. The easiest and most common form of accelerated life testing is "continuous use acceleration." Accelerated tests can be performed at elevated temperature, humidity, voltage, pressure, vibration, etc., or in a combined manner in order to accelerate the failure mechanism. The stress level should be chosen to accelerate the failure modes under consideration, but the stress levels should be chosen so that they do not introduce failure modes that would never occur under real-use conditions. Also, the stress levels must be high enough so that enough failures are observed within the allowable timeframe. Of course the uncertainty is higher if the accelerated stress is higher than the usual operating stress, but the accelerated life test estimates the distribution of lifetimes in the product in a shorter time, which can identify wear-out periods (defined in the next section) resulting from actual product performance degradation.

How Do We Show and Express the Reliability Level: Weibull Distribution

An illustration on the difference between quality and reliability can be seen in the plot shown in Fig. 1.7, which is often used to describe the lifetime of a product or component called the "bathtub curve." The bathtub curve consists of three periods: an infant mortality period with a decreasing failure rate followed by a normal life period (also known as "useful life") with a low, relatively constant failure rate, concluding with a wear-out period that exhibits an increasing failure rate. The bathtub curve does not depict the failure rate of a single item but describes the relative failure rate of an entire population of products over time. Some individual units will fail relatively early (infant mortality failures), others will last until wear-out, and some will fail

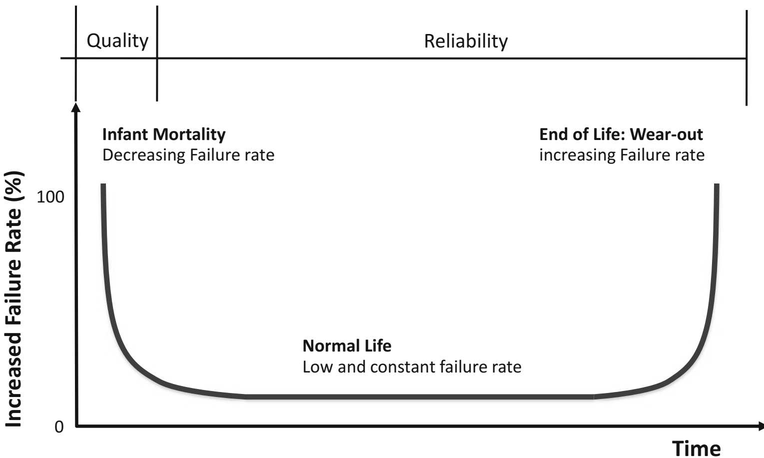


Fig. 1.7 Bathtub *curve*, which shows the three different regions related to infant Mortality, normal life, and wear-out region

during the relatively long, normal life period. Failures during infant mortality are highly undesirable and are always caused by defects and design flaws: material defects, design factors, process factors during assembly, etc., and are considered as quality issues [5]. The infant mortality period is a time when the failure rate is dropping but is undesirable because a significant number of failures occur in a short time. During normal life, it is desired to have the bottom of the bathtub to be as low as possible with a wear-out period long after the expected useful lifetime of the product.

One of the wonders of nature is that even twins have different lifetimes. Variation in unknown and subtle birth conditions as well as differences in lifestyle and specific experiences (such as an injury) makes two twins have different lifetimes. When we consider life expectancy of people, we evaluate it by using statistical analysis of the sample groups and extrapolate it to the entire population. The key to the success of such analysis is the choice of the statistical model that correctly captures lifetime variations among people and also to select sufficient sampling for extracting parameters defining the distribution. The reliability evaluation requires the same type of analysis. It is impractical to test all products under a normal-use condition. The reliability evaluation has to be conducted with a selected number of samples under highly accelerated but relevant conditions for the failure. The test result is then fitted to an appropriate statistical model for extraction of model parameters like a mean and standard deviation. Through extrapolation of the result to end-use condition and entire product population, reliability assessment is completed. The common industrial choice for the statistical analysis of failure is the Weibull model, known as Weibull distribution. Statistical theory behind the model is beyond the scope of this book, yet it can be mentioned that the Weibull distribution physically captures extreme boundary of lifetime rather than the nominal distribution. The choice of

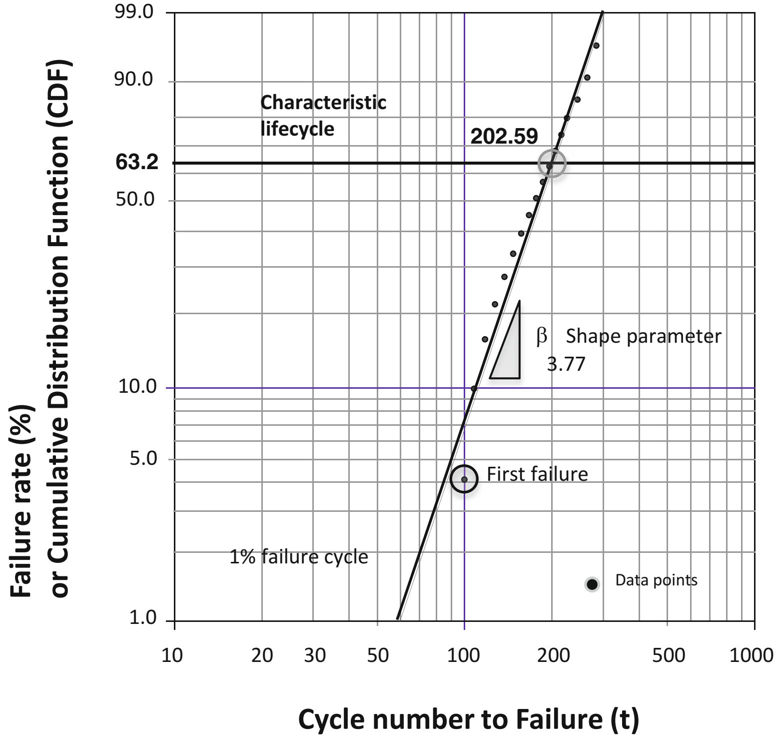


Fig. 1.8 Typical Weibull plot

Weibull may be correct and safe because many physical failure processes are dictated by the weakest link of potential failure sources. For example, fracture toughness of steel wire is known to follow the Weibull distribution because the fracture toughness is determined by the largest crack in the wire. Correlation to physical failure mechanics makes the Weibull distribution a correct choice and thus popular.

The Weibull distribution is a continuous probability distribution used in probability theory and statistics, but it is a useful way to show and see the performance of the device or system. The primary advantage of Weibull analysis is the ability to provide reasonably accurate failure analysis and failure forecasts with a small number of samples. Another advantage of Weibull analysis is that it provides a simple and useful graphical plot of the failure data. Figure 1.8 is a typical Weibull plot. The horizontal scale is a measure of life or aging. Start/stop cycles, mileage, operating time, landings, or mission cycles are examples of aging parameters. The vertical scale is the cumulative percentage failed. The two defining parameters of the Weibull plot are the slope, beta (β), and the characteristic life, eta (η). The slope of the line, β, is particularly significant and may provide a clue about the

physics of the failure process, determines which member of the family of Weibull failure distributions best fits or describes the data, and also indicates which class of failures is present:

$\beta < 1.0$ indicates infant mortality
$\beta = 1.0$ means random failures (independent of age)
$\beta > 1.0$ indicates wear-out failures

The characteristic life, η, is the typical time to failure in Weibull analysis. It is related to the mean time to failure.

The horizontal scale is the cycle or time (t) parameter to failure, with a logarithmic scale. The vertical scale is the cumulative distribution function (CDF) that defines the proportion of the parts that will fail up to cycle number (t) in percent. The statistical symbol for the CDF is $F(t)$, the probability of failure up to time t. The complement of $F(t)$ is reliability, the probability of not failing up to time t. $R(t) = 1 - F(t)$:

$$F(t) = 1 - e - (t/\eta)\beta$$
$$R(t) = e - (t/\eta)\beta$$

where
$F(t)$: fraction failing up to time (t) (CDF)
t: failure time
e: the base for natural logarithms
η: characteristic life or scale parameter
β: slope or shape parameter

The characteristic life η is defined as the age at which 63.2 % of the units will have failed (indicated on the plot with a red line). For β = 1, the mean time to failure and η are equal. For β > 1.0, the mean time to failure (MTTF) and η are approximately equal.

Two sets of example plots are shown in Fig. 1.9, where Fig. 1.9a is a data set, which has the same first failure condition but different failure interval after the first failure. The result shows that each data set has its own shape parameter (β), where different shape parameters produce a different characteristic lifetime. With a lower beta slope, the characteristic lifetime occurs at a much higher value than the higher beta slope data set. This means that even with the same first failure cycle number, it is important to see the following failure trend to accurately estimate the life expectancy. Figure 1.9b shows the same beta for each data set, but the first failure is well aligned with the characteristic life cycle number ranking. The meaning of the beta slope parameter is related to the physics of the failure. Thus, the beta differences in Fig. 1.9a represent different failure mechanisms. There are more Weibull plots in this book in the following chapters. Each Weibull plot will provide their unique stories about the test and the sample results. Different failure mechanisms arising from differently evolved microstructures will be discussed.

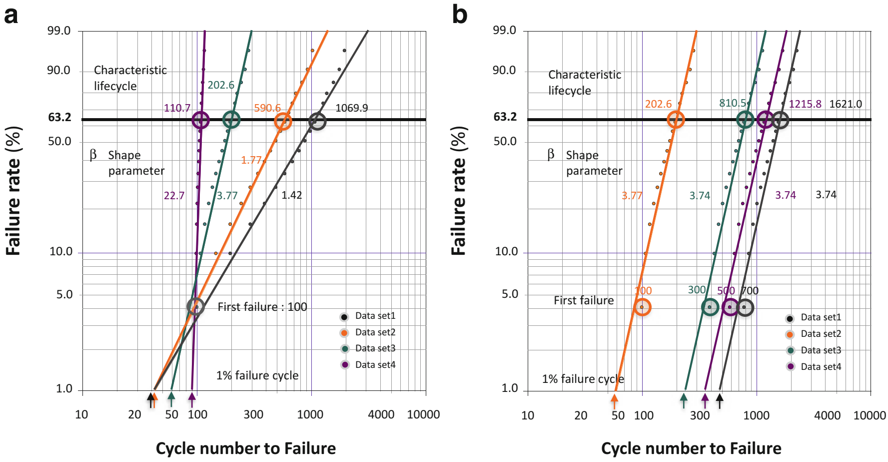


Fig. 1.9 Weibull plots with different data set presentation. (**a**) Fixed first failure but different failure cycle trend resulted in a variety of characteristic life cycle number. (**b**) Different first failure but the follow-up failure with a similar rate shows same beta value

The Role of Microstructure

One of the key questions and steps in the reliability analysis is to ask what makes failure to occur at different rate even within the same sample group. The answer to this question, when it comes to failure in materials, is usually found from what is known as the microstructure. Microstructure does not refer to any specific feature in a material, but rather it is a broadly defined term to include any microscopically distinctive feature that can affect the physical properties of materials. It includes many structural features commonly present in materials including interface, grains and their boundaries, phases, precipitates, crystal defects, and so on. Hence, it can be said that material is a collection of microstructural features, and they are the ones that respond to the environmental conditions such as the stress, temperature, current, etc. Because microstructural details have to vary from one component to the other with subtle variation in the process and chemical condition, materials are bound to have variation in their responses to the external loads and therefore exhibit different failure rates or, in an extreme situation, failure mechanisms. Since microstructure includes so many different elements, it is important to identify the specific element or elements that have direct connection to the failure mechanism under evaluation, which is a major part of reliability engineering. A classic example of such kind may be found from the development of Al alloys. Pure Al has such a low yield strength that it cannot be used for any structural applications. The low yield strength of Al stems largely from the fact that dislocations are highly mobile in pure Al when subjected to stress. Therefore, in order to increase the yield strength, a

small amount of alloying elements, most notably Cu and Ti, are added to Al. The addition of those elements results in a formation of small but hard precipitates densely dispersed in Al matrix. Impeded by them, dislocations cannot move very well unless stress is high enough for them to either cut through them or bypass around them. This enables Al alloys to withstand high stress beyond its limit in pure state and to be used for structural applications. In this case, therefore, the relevant microstructure may be the precipitates while their size and distribution can be included in the microstructure.

Sn-rich solder joints, the main topic of this book, is not an exception to this rule. Solder joints consist of various microscopic features, and they, either collectively or individually, participate in various types of known failure mechanisms. Either their presence or absence is responsible for rapid failure or slow failure, and, in some cases, precipitates become a source of failure mechanism. It is therefore important to identify the very features associated with the failure mechanisms, to learn how they evolve and interact with the failure process, to find where and when they form, and to understand the contributing factors to their formation. Such knowledge is essential not only for achieving accurate reliability assessment of the solder joints in electronic products but also for enabling development of more reliable solder interconnects. Even with complexity, there are a few key microstructural features that are known to interact with failure mechanisms such as the constitutional phases and their distribution in the solder matrix, grain structure, and interface structure at the adjoining interfaces. These microstructural features interact with common failure mechanisms including thermal fatigue, mechanical fatigue and shock, and corrosion. This book describes such microstructural features, their origin and evolution, and their interaction with their associated failure mechanisms.

Chapter Summary and the Structure of This Book

As mentioned in the abstract of this chapter, the foundation of this book is that mechanical properties are defined by microstructure and chemical composition [1]. This fundamental approach follows the path of the microstructure evolution and identifies the microstructure interaction with the external environmental factors. With the world covered with more electronic devices and the higher dependency on the signals and output that these devices provide, identifying the elements that react to these external factors is crucial. Since we need to know the degradation mechanism to find the mechanism that causes failures, simultaneously gaining and understanding of microstructural evolution phenomena can lead to improvements in reliability of the solder interconnect and ultimately the device or product. In this chapter we briefly looked into the overall landscape we live in and the electrical components and devices in various end-use conditions we use in our daily lives. In the next chapters, we will start with covering the initial formation of the microstructure and the evolution during time and temperature. Further on, we will identify the factors and explain the mechanisms associated with various end-use conditions and

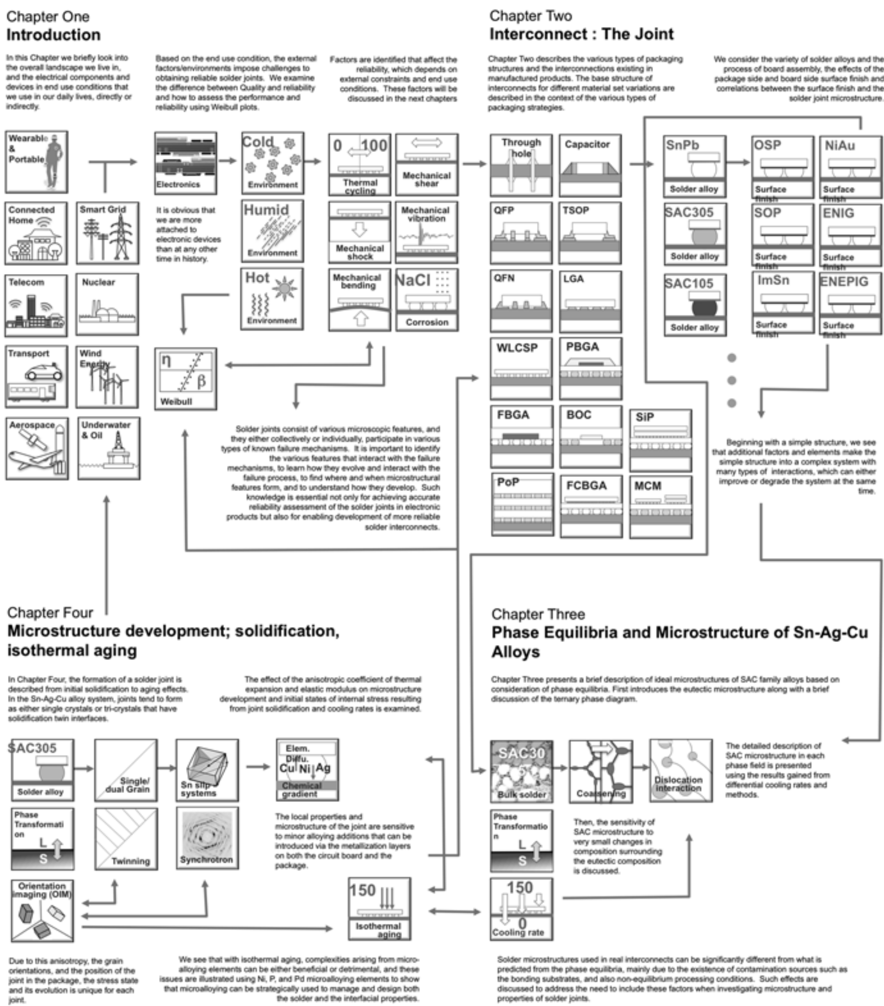


Fig. 1.10 The whole book in a nutshell. Schematically summarized book outline and content

external factors, which includes thermal, mechanical, and chemical performances. Figure 1.10 shows the overall structure of this book schematically in a very brief and simplified format.

Chapter 2 describes the various types of packaging structures and the interconnections present in industrial products. It also provides the basic structure of interconnects for each material set variation and describes the various types of packaging structures and the interconnections. We will examine the variety of solder alloys and the process of board assembly, the effect of the package-side and board-side surface finish, and the correlation between the surface finish and the solder joint microstructure.

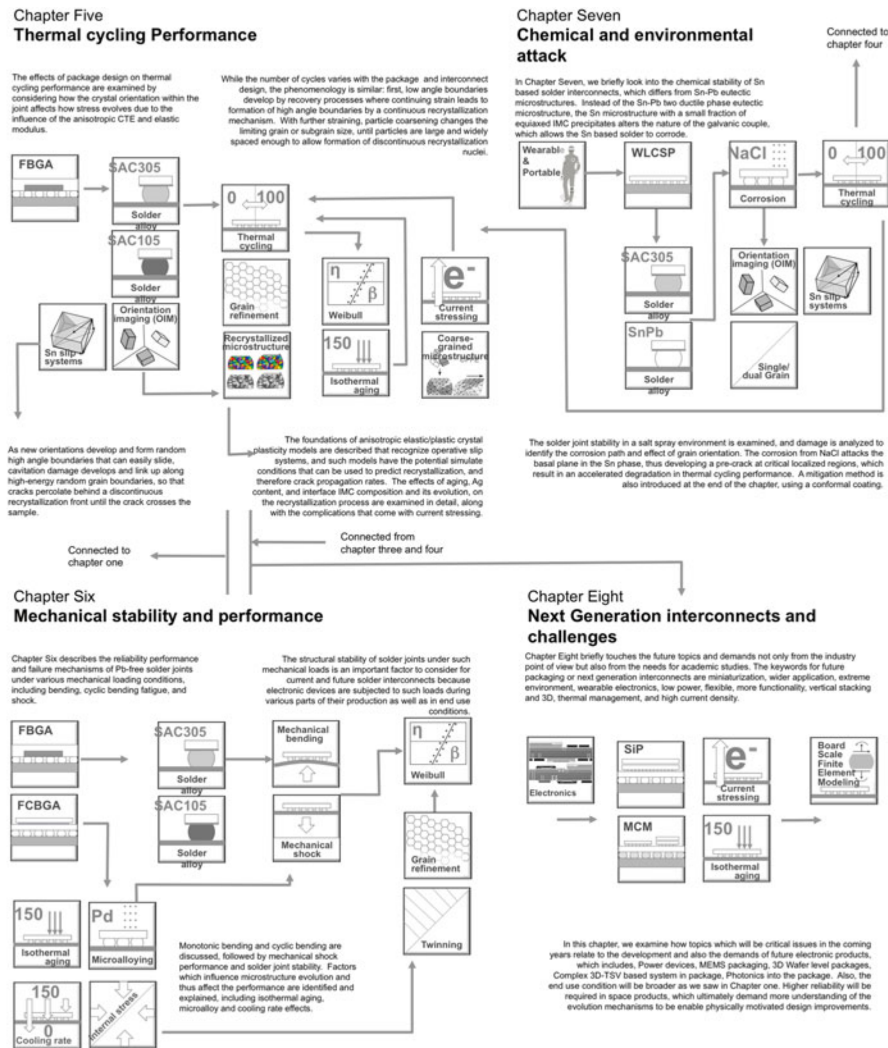


Fig. 1.10 (continued)

Beginning with a simple structure, we will see that additional factors and elements make the simple structure into a complex system with various interdependencies, which can improve or degrade the joint at the same time.

Chapter 3 presents a brief description of ideal microstructures of Sn–Ag–Cu family alloys based on consideration of phase equilibria. It first introduces the eutectic microstructure along with a brief discussion of the ternary phase diagram. Then, the sensitivity of Sn–Ag–Cu microstructure on very small changes in composition surrounding the eutectic composition is discussed. The microstructural sensitivity of the alloy composition stems from the fact that there are six possible phase

fields for the primary phase formation. The primary phase refers to the phase that is in equilibrium with the liquid phase at off-eutectic composition and is the phase that forms prior to the eutectic reaction during solidification. A detailed description of Sn–Ag–Cu microstructure in each phase field is presented using the results gained from the differential cooling method. Solder microstructures used in real interconnects can be significantly different from what is predicted from the phase equilibria mainly due to the existence of many contamination sources, including the joining substrates and nonequilibrium processing conditions. Such effects are discussed to address the need for their inclusion in investigating microstructure and properties of solder joints of interest. This chapter sets the foundation on which nonequilibrium microstructures that form in practical joints can be understood in Chap. 4.

In Chap. 4, the formation of a solder joint is described from initial solidification to aging effects. In the Sn–Ag–Cu alloy system, joints tend to form as either single crystals or tri-crystals that have twin interfaces that ideally form a "beach ball" orientation relationship of 60° sections about a common crystal [100] axis. The effect of the anisotropic coefficient of thermal expansion and elastic modulus on microstructure development and initial states of internal stress as the joint solidifies and cools is examined. Due to this anisotropy and the grain orientations, the position of the joint in the package, the stress state, and its evolution are unique for each joint. The local properties and microstructure of the joint are sensitive to minor alloying additions that can be introduced via the metallization layers on both the circuit board and the package. We will see that with isothermal aging, complexities arising from microalloying elements can be either beneficial or detrimental, and these issues are illustrated following Ni, P, and Pd microalloying elements to show that microalloying can be strategically used to manage and design both the solder and the interfacial properties.

In Chap. 5, the effects of package design on thermal cycling performance are examined by considering how the crystal orientation within the joint affects how stress evolves due to the influence of the anisotropic CTE and elastic modulus. With low-stress designs such as plastic ball grid arrays (PBGA, larger balls with a large pitch), it takes thousands of cycles before cracks are prevalent, while direct chip attachment designs such as wafer-level chip-scale packages (WLCSP) will fail in a few hundred cycles. While the number of cycles varies with design, the phenomenology is similar: first, low-angle boundaries develop by recovery processes where continuing strain leads to the formation of high-angle boundaries by a continuous recrystallization mechanism. With further straining, particle coarsening changes the limiting grain or subgrain size, until particles are large and widely spaced enough to allow discontinuous recrystallization nuclei to form. As these new orientations develop and form random high-angle boundaries that can easily slide, cavitation damage develops which links up along high-energy random grain boundaries, so that cracks percolate behind a discontinuous recrystallization front until the crack crosses the sample. The foundations of anisotropic elastic/plastic crystal plasticity models are described that recognize operative slip systems, and such models have the potential simulate conditions that can be used to predict recrystallization. The effects of aging, interface IMC composition and evolution, and Ag content on the

recrystallization process are examined in detail, along with the complications that come with current stressing.

Chapter 6 describes the reliability performance and failure mechanisms of Pb-free solder joints under various mechanical load conditions, including bending, cyclic bending fatigue, and shock. The structural stability of solder joints under such mechanical loads is an important factor for the current and future solder interconnects because electronic devices are subjected to such loads during various parts of their production as well as in end-use conditions. Even more importantly, mechanical stability is emerging as critical reliability concern with a rapid expansion of mobile electronics. In order to properly apprehend their threats to the reliability, this chapter describes the threat from each mechanical load and the mechanism by which the solder joint fails. We begin with failure in solder interconnects induced by bending forces on a PCB. The source of the bending force and its test method is presented along with the discussion on failure mechanism. It is shown that the failure by bending force occurs either in the Cu trace in PCB or solder/Cu interface. Secondly, the influence of cyclic bending fatigue is introduced. It is discussed more in terms of its mechanics and its potential as a new reliability evaluation methodology. Finally, failure by mechanical shock is discussed with weighted emphasis on recent experimental observations showing a sensitivity of shock resistance to the microstructure of SAC solder joint.

In Chap. 7, we will briefly look into the chemical stability of the Sn-based solder interconnects. Sn itself is considered as a good corrosion-resistant material. In early use of the eutectic Sn–Pb alloy in electronics, not much research was performed since there was no specific corrosion concern. But with the microstructure change from a dual-phase eutectic structure to a Sn microstructure with equiaxed IMC precipitate islands, a potential galvanic couple is formed, which enables Sn-based solder to corrode. The solder joint stability in a salt spray environment is examined, and damage is analyzed to identify the corrosion path and effect of grain orientation. The corrosion due to NaCl attacks the basal plane in the Sn, thus developing a pre-crack at critical localized regions, which results in an accelerated degradation in thermal cycling performance. A mitigation method is also introduced at the end of the chapter, using conformal coating.

Finally in Chap. 8 we will briefly touch the future topics and demands not only from the industry point of view but also from the perspective of academic research opportunities. The keywords for future packaging or next-generation interconnects are miniaturization, wider application, extreme environment, wearable electronics, low power, flexible, more functionality, vertical stacking and 3D architecture, thermal management, and high current density. In this chapter, we will go through a list of topics which will be critical issues in the coming years related to the development and demands of future electronic products, which includes power devices, MEMS packaging, 3D wafer-level packages, complex 3D-TSV-based system in package, and photonics in the package. Also, the end-use condition will be broadened as we saw in this chapter. Higher reliability will be required in consumer space products, which ultimately demands more understanding of the solder joint evolution mechanisms to enable rational strategies for improvement.

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Chapter 2
Interconnection: The Joint

From power cord to the printed circuit board (PCB), from the PCB to components via each solder joint, from solder joints to substrate through silicon chips via wire or flip-chip solder bump, and then to another adjacent chip with a chip on top connected with microbumps, electronic devices are constructed with various interconnects through various material sets and thus various interfaces that are called interconnections. Chapter 2 describes the various types of packaging structures and the interconnections existing in industry products. Also, the base structure for each interconnect material set is described.

What Is an Interconnect in Electronic Device

As with many words, the definition of interconnection varies according to the context in which the word is used. The overall general definition is a connection (physical or logical) between multiple things [1, 2]. In a more detailed sense for the telecommunication sector, it is the linking of two networks for the mutual exchange of traffic, as defined by the US Code of Federal Regulations [3]. In a smart grid sector, it means connecting renewable-energy systems to the power grid. But when thinking about the meaning of "interconnection," it may also sound political and social because it connects not only physically different things but also needs to deal with different characteristics, sometimes a strong bond or weak link between two different physical or social groups. In any of these situations, an interface connects the whole, and a system is built (Fig. 2.1).

The bonding between different things, in the context of electronic devices, involves layers that are crucial because it provides structure stability to the component and, in a bigger picture, the stability of the system. An interesting phenomenon occurs once an interconnect or a joint is formed. If the bonding between the two material sets is strong, it may be stable, or it may cause a shift from one weak link to another weak interface. For example, an electric device can have very strong

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T.-K. Lee et al., *Fundamentals of Lead-Free Solder Interconnect Technology*,
DOI 10.1007/978-1-4614-9266-5_2

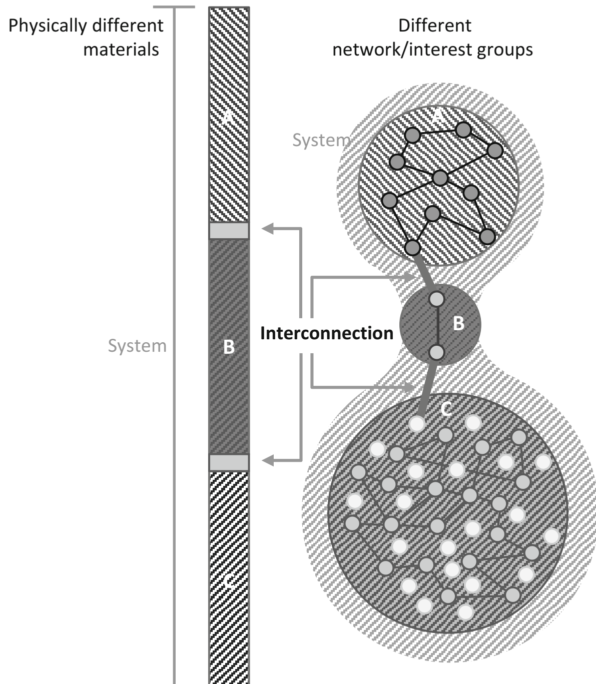


Fig. 2.1 Interconnection, a contact point for different material sets or different networks

solder joints, but the system can be unstable because fracture can occur *near* the solder joint interface inside the package substrate or in the dielectric material within the silicon die or even cause laminate cracking in the circuit board. Therefore, increasing strength in only one section of the interconnect is not enough, and strengthening the whole system is not simple, as a careful design that absorbs the distributed stress and shifts the excessive stress or strain to a place where it can be sustained is needed. This is a crucial design factor, which ultimately improves the stability of the interconnect as well as the whole system.

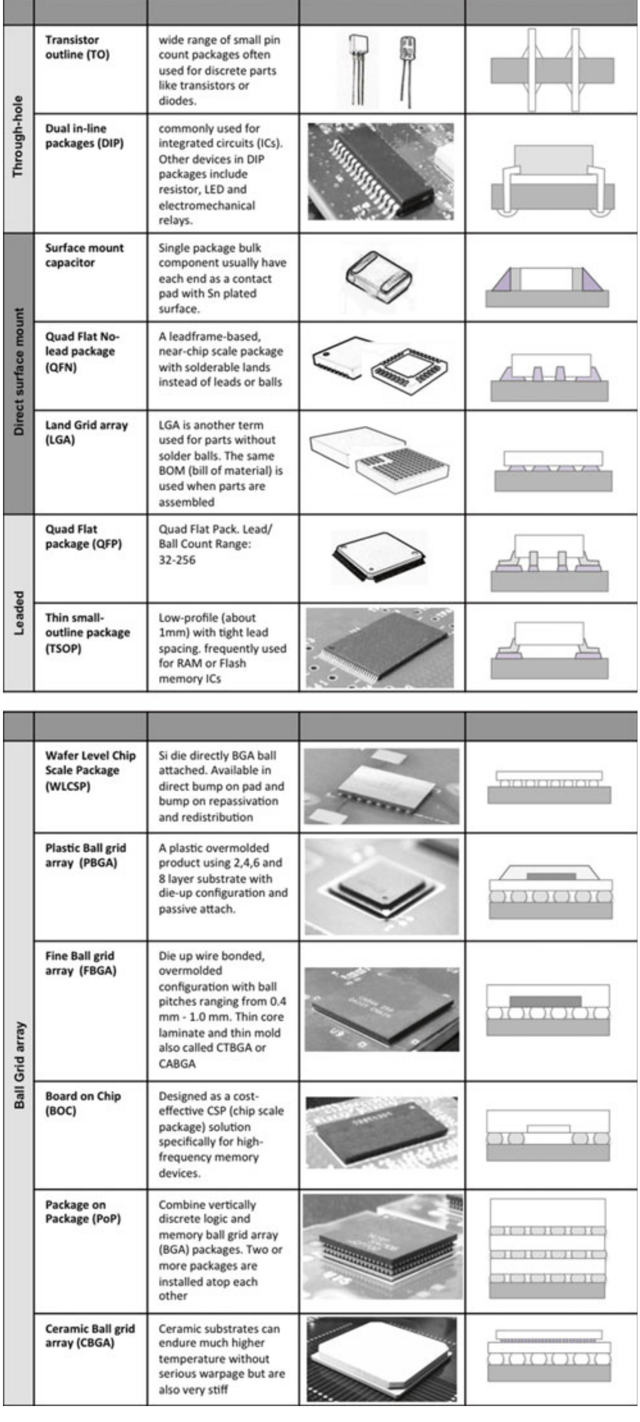
There are many types of interconnections in electronic systems: Starting from the electronic plug-in cord, there are pin connectors and solder joints between the PCB and modules, solder joints from modules to a component, wire bond interconnects or solder bumps (on a flip-chip joint) from the component substrate to the Si chip, and microbumps from a Si chip to another stacked Si chip. Each of the interconnection types has their own functionality and configuration within electronic systems.

To cover all of these interconnects, one book is definitely insufficient, not only because of the variety of interconnects, but also because interconnect technology is a fast moving technology, where every quarter year, a new technology is introduced to improve the functionality and the form factor. Thus, to identify the foundation for this fast moving technology sector, this book will focus on the structural interconnect between the PCB and the component. We will further consider the next-generation (smaller and more highly stressed) interconnects briefly in Chap. 8.

Figure 2.2 shows an overall diagram of what types of electronic packages exist. There are several approaches to connect the component to the board to make a system. One of the simplest ways is drilling a hole into the PCB and inserting the lead of the component for bonding, known as through-hole components. Capacitors or resistors are simple components with two or three channels to connect to the PCB circuitry. Such components with through-hole leads are soldered to the board using a wave soldering process. Another package type using through-hole leads are dual in-line packages (DIPs). DIPs are classic electronic packages, which are still widely used for memory or in a variety of IC devices. They are directly soldered to the board or sometimes placed into a socket, which is another type of connection to the board. But with increasing functionality and IO density, more and more leads are needed with a demand of smaller and thinner package size with more input and output channels to and from a single Si die. Thus, the DIPs are being changed to denser package types such as a quad flat no-lead (QFN), ball grid array (BGA), or board on chip (BOC) type packages. Since it is not efficient to drill hundreds of through holes in the PCB, the higher-density packages use smaller pads with solder paste or solder balls to make connections to the board. These components can also be attached to the PCB by simply using solder paste. A small amount of solder paste is printed using a stencil at the Cu pad location, and the component is placed on top of the solder paste right before going through a solder reflow process oven. This approach is defined as surface-mount technology (SMT). Designs that use only paste are QFNs and land grid arrays (LGA), and solder balls are used for FBGAs, PBGAs, and the FCBGAs (acronyms are defined in Fig. 2.2).

The surface-mount components can be as versatile as the function of each component requires. Packages that do not need a lot of signal pins have a lead package like the quad flat package (QFP) or thin small-outline package (TSOP), but when the number of signal pins needs to be increased, BGA components are needed. Among the BGA components, maybe the simplest component package with solder balls attached might be the wafer-level chip-scale package (WLCSP) since the silicon die is directly bonded to the PCB via solder balls. But having the bare silicon die on a board is often a risk since it can be easily damaged by external factors and the interconnects must be under the die area. The CTE mismatch between the silicon and the PCB is also a challenge to overcome, thus having a very large WLCSP is problematic. Due to these limitations, various electronic packaging technologies were introduced to place these silicon chips onto the board. Electronic packaging not only protects the silicon die but also provides the connection from the Si to the substrate and to PCB and other components to form an electronic system. The package types vary by the component function, and it is hard to categorize the whole packaging family into well-distinguished categories. Thus, in this book, we have selected a few representative package types (Fig. 2.2).

Within the component package there are also various methods of connecting the Si die to the substrate. As shown in Fig. 2.3, one of the novel connection methods is using thin metal wire. Gold wire was used in components for a very long time, but with the increasing price of gold, recently Cu and Ag alloy wires have been developed [4–6]. Each material has its own advantages and disadvantages, so the



Through-hole	Transistor outline (TO)	wide range of small pin count packages often used for discrete parts like transistors or diodes.
	Dual in-line packages (DIP)	commonly used for integrated circuits (ICs). Other devices in DIP packages include resistor, LED and electromechanical relays.
Direct surface mount	Surface mount capacitor	Single package bulk component usually have each end as a contact pad with Sn plated surface.
	Quad Flat No-lead package (QFN)	A leadframe-based, near-chip scale package with solderable lands instead of leads or balls
	Land Grid array (LGA)	LGA is another term used for parts without solder balls. The same BOM (bill of material) is used when parts are assembled
Leaded	Quad Flat package (QFP)	Quad Flat Pack. Lead/ Ball Count Range: 32-256
	Thin small-outline package (TSOP)	Low-profile (about 1mm) with tight lead spacing. frequently used for RAM or Flash memory ICs
Ball Grid array	Wafer Level Chip Scale Package (WLCSP)	Si die directly BGA ball attached. Available in direct bump on pad and bump on repassivation and redistribution
	Plastic Ball grid array (PBGA)	A plastic overmolded product using 2,4,6 and 8 layer substrate with die-up configuration and passive attach.
	Fine Ball grid array (FBGA)	Die up wire bonded, overmolded configuration with ball pitches ranging from 0.4 mm - 1.0 mm. Thin core laminate and thin mold also called CTBGA or CABGA
	Board on Chip (BOC)	Designed as a cost-effective CSP (chip scale package) solution specifically for high-frequency memory devices.
	Package on Package (PoP)	Combine vertically discrete logic and memory ball grid array (BGA) packages. Two or more packages are installed atop each other
	Ceramic Ball grid array (CBGA)	Ceramic substrates can endure much higher temperature without serious warpage but are also very stiff

Fig. 2.2 Selected package designs

Ball Grid array with Area array	**Flip Chip ball grid array (FCBGA)**	Flip Chip technology use array interconnect of die to substrate as a replacement for wire bonding. The entire die surface is used for electrical connections to the substrate, exponentially increasing the I/O per unit area vs. perimeter interconnect technologies.		
	Multi chip module (MCM)	A fully functional system or subsystem in an IC package format. Multiple dies are placed onto a single substrate, boosting functionality and signal speed.		
	System on package (SoP)	System-On-Package (SOP) provides all the system functions in one single module, have multiple integrated ICs for analog, digital and optical functions		
	System in package (SiP)	A system-in-a-package (SiP), also known as a Chip Stack MCM (multi-component module). SiP dies are stacked vertically, compared to the horizontally placed MCMs		

Fig. 2.2 (continued)

material properties required for each use condition need to be carefully considered. But with an increasing number of connections to be made, the available space around the perimeter of the die for wire bonding is getting denser and denser. Even with two rows of wire connections, space is limited, and a different interconnect technology is needed for higher density and more interconnection per unit area. In the early 1980s, a technology was developed, and it became well adopted by the industry called flip-chip technology. As shown in Fig. 2.4, instead of using wire, a miniaturized solder joint is placed between the Si die and the substrate. Since the joint, which is called a solder bump, can be small and is also placed under the die with a very fine pitch, this technology makes it possible for the electronic device to be more densely packed with more functions available, leading to much higher computing speeds, resulting from a shorter connection distance than wire connections. Flip-chip solder bumps are small and must endure the high CTE mismatch between the silicon and the organic or ceramic substrate, so to assist the accommodation of the CTE mismatch, a polymer underfill is injected after the solder bumps are formed to strengthen the interface. This underfill process is also used in WLCSP assembled boards, where additional strengthening is needed for both thermal and mechanical performance improvement. Recently a modified process technology called thermal compression bonding (TCB) was introduced, which combines the reflow of the solder bump and the underfill into one operation.

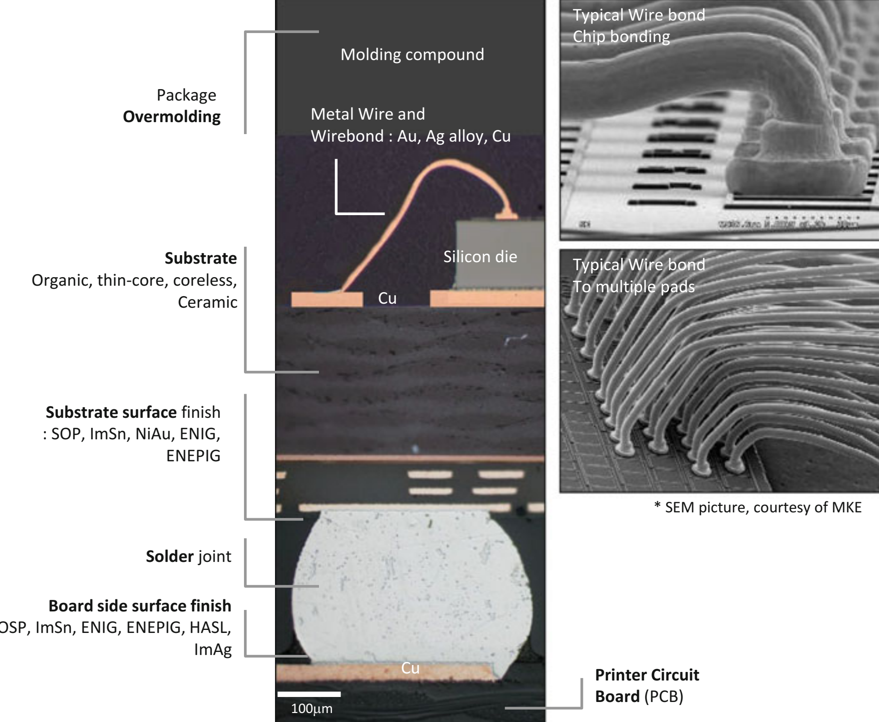


Fig. 2.3 Wire bond package interconnections

With all of the above package types, there are also packages with multiple combinations of technologies. For example, two or three silicon die can be stacked up with Au wire connecting not only the Si die and the substrate but also providing connection between multiple Si dies, which are called multi-chip components (MCC). This concept can be also applied to a single substrate with several silicon die or components in parallel and are called multi-chip modules (MCM). Another type of package is the package on package (PoP), a stack-up of several independent BGA components.

The most recent new technologies need even higher density and functionality in a single device or component. Since the signal speed needs to be faster without sacrificing any signal loss, the distance between the silicon chips needs to be closer than ever, with not only one application-specific integrated circuit (ASIC) chip but with central processor unit (CPU) and memory chips installed together on one single substrate. This came to be possible with drilling a hole into the Si chip itself and connecting the top and bottom of the silicon chip. While it is conceptually simple, drilling a small hole into the Si and filling it with conductive metal like Cu, the technology itself, through-silicon via (TSV) technology, is a huge challenge, and

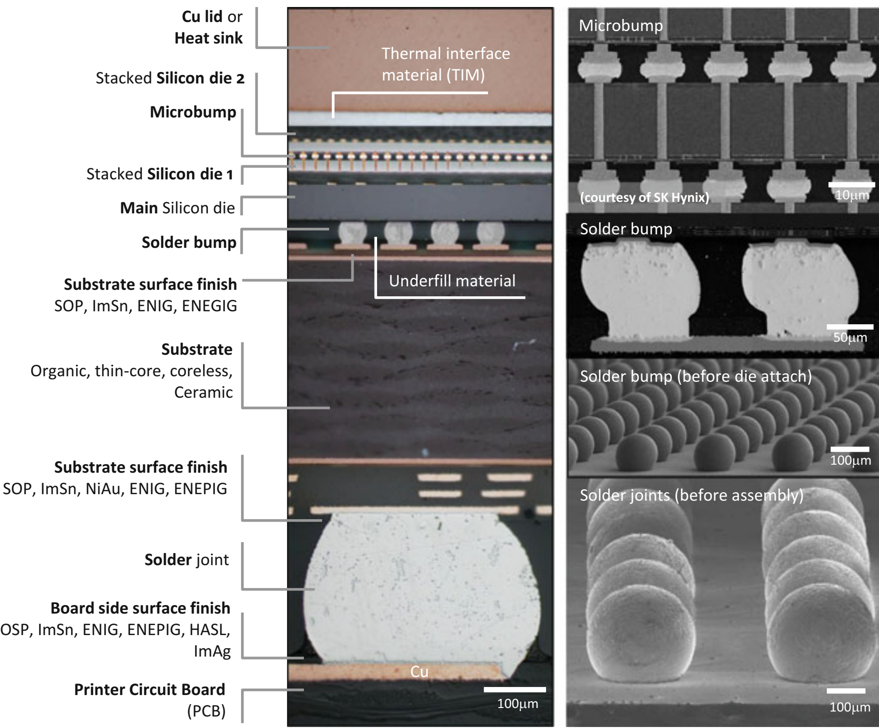


Fig. 2.4 Flip-chip connected package with Silicon die stack-up with through silicon via (TSV) and microbump connection

the industry is still in the process of fine tuning. But with developing the process and assessing the reliability of these devices, these will appear in a wide range of high-function components. This technology enables a new form of package and interconnect, which is the interconnect between one Si die and another using an even more miniaturized solder joint, called microbumps.

With a roadmap for a design concept for a new technology, a new package category came to the industry, the MCM, system on chip (SoC), system on package (SoP), and system in package (SiP). All of these concepts are similar, but small differences between these terms exist based on structural aspects. SoC, for example, seeks to integrate numerous system functions on one silicon chip, meaning that the package remains the same among different SoC, because they are built on the same Si die. Fabricating one perfect Si chip with all the different component functions inside is a challenge and still a costly option. This technology will be revisited in Chap. 8 after the challenges for existing interconnect technology are discussed, to anticipate future challenges. An SiP is a fully functional system or subsystem in an IC package format. It contains one or more IC chips, plus other components traditionally found on the system board. These components may include passive components, RF shields, prepackaged ICs, connectors, antennas,

camera lenses, or other mechanical parts required to achieve full system functionality. This package type is also known as a chip stack MCM. SiP dies are stacked vertically, unlike a slightly less dense MCM, which places dies on the same plane alongside one another. It is considered an intermediate solution on the path to the SoC. The definitions of the MCM and the SiP overlap, but if the Si die are stacked, it is usually called an SiP, and if those components are placed horizontally, it is called an MCM.

From the power cord to microbumps, electronic devices are constructed with various interconnects through various material sets and thus various interfaces that are called interconnections.

Printed Circuit Board

As illustrated in Figs. 2.3 and 2.4, the interconnection from the Si to the substrate, whether it is via Au wire or a solder bump, needs to be connected to the board to connect the component functionality to the system. A PCB is used to mechanically support and electrically connect electronic components using conductive pathways, tracks, or signal traces etched from copper sheets laminated onto a nonconductive substrate [7, 8]. When the board has only copper tracks and features, and no circuit elements such as capacitors, resistors, or active devices have been manufactured into the actual substrate of the board, it is more correctly referred to as printed wiring board (PWB) or etched wiring board [8, 9]. Although more accurate and distinct from what would be known as a true printed circuit board, use of the term PWB or printed wiring board has generally fallen by the wayside for many people as the distinction between circuit and wiring has become blurred. Today, PCBs are used in virtually all but the simplest commercially produced electronic devices and allow fully automated assembly processes that were not possible or practical in the past. A PCB populated with electronic components is called a printed circuit assembly (PCA), printed circuit board assembly, or PCB assembly (PCBA). In informal use, the term "PCB" is used both for bare and assembled boards, the context clarifying the meaning [9].

A schematic presented in Fig. 2.5 shows the construction of a PCB. Circuit board materials available for multilayer construction are primarily of two types: core material that has copper laminated to both sides (cured laminate) and pre-preg material (uncured resin treated glass) used to fill the space between cores and out-layer foils that are used to bond all of the layers together. Copper foil of various weights (half ounce or greater) is available as well for outer layer construction. Pre-preg is a term for "pre-impregnated" composite fibers, where a material, such as epoxy, is already present. These usually take the form of a weave or are unidirectional. They already contain an amount of the matrix material used to bond them together and to other components during manufacture. The resin is only partially cured to allow easy handling.

The core material is the basis for the construction of the multilayered board. It is etched with the required circuitry and oxide treated to promote proper adherence to

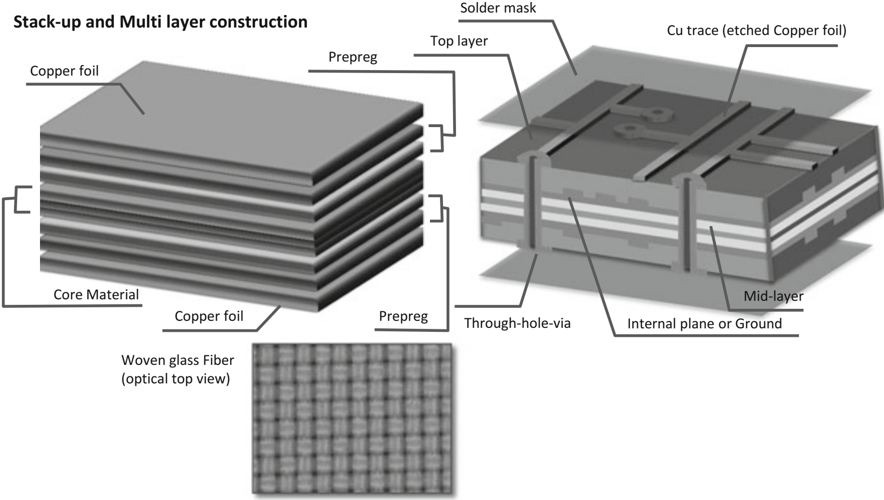
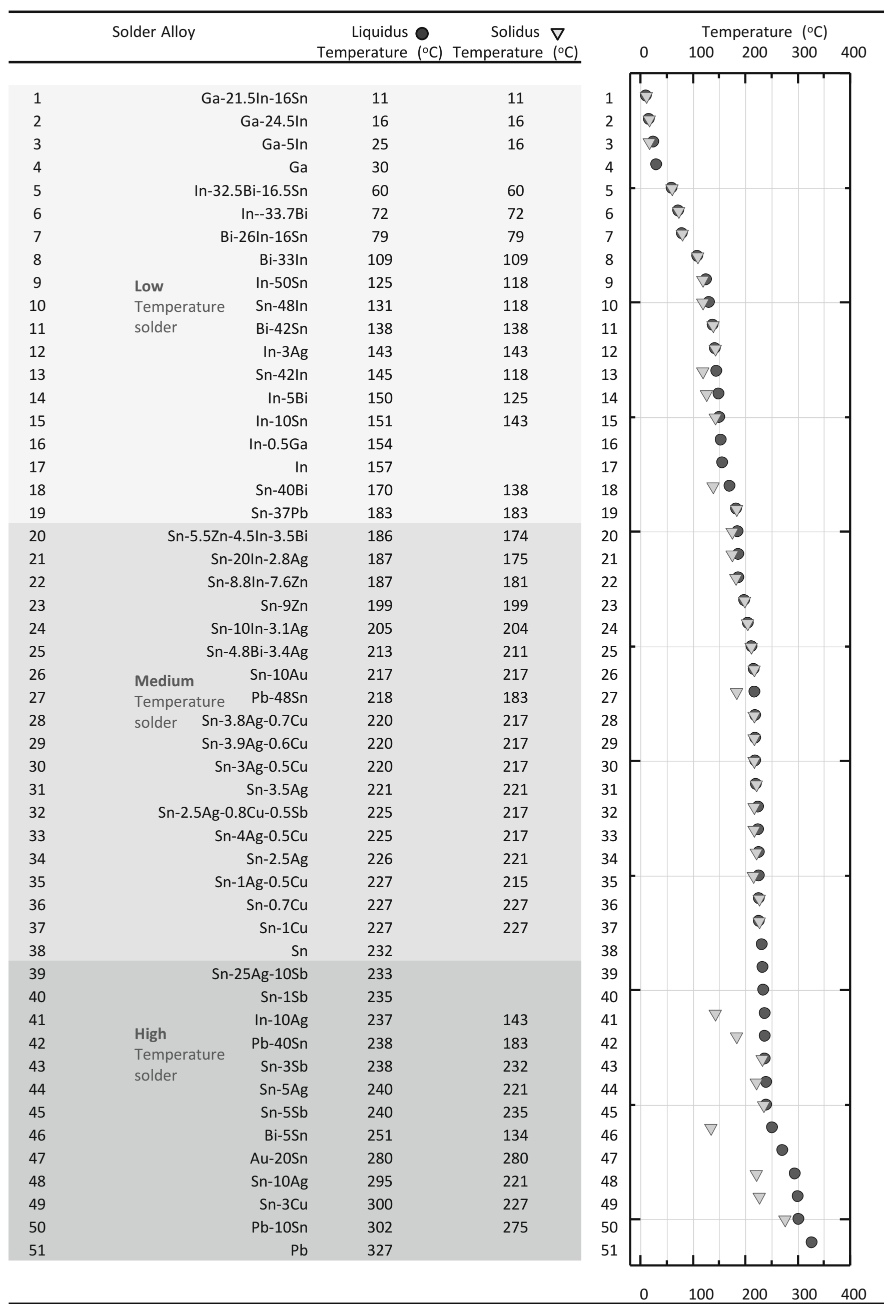


Fig. 2.5 Printed Circuit board stack-up and multilayer construction

the pre-preg layers that will be applied in the subsequent stack-up. Regarding the material for the core, for example, FR-4 is commonly used for PCBs. The abbreviation "FR4" means: F (for flame) and R (for retardant), and the 4 is a # 4 epoxy. FR4 features high-flexural, impact, and mechanical bond strength at temperatures up to 130 °C, which is the glass transition temperature (T_g) for this material. With this T_g, it is possible to pass through two or three reflow processes. While FR4 is common, there are various T_g material options available for applications that require different properties.

Solder Alloys

The components need to be mounted on the PCB. Connecting different materials at a very fine scale is a challenge because bonding needs to be made between components with different physical properties. Soldering is a process in which two or more metal items are joined together by melting a lower melting temperature solder alloy into the joint. There are numerous solder alloy compositions in the industry, which serve specific purposes. Figure 2.6 shows a span of alloy compositions based on their liquidus and solidus temperatures. Some are eutectic (have one low melting temperature), and some have a gap between the liquidus and solidus temperature that results in a mushy zone between being fully liquid and fully solid during cooling (based on the equilibrium assumptions). In reality, undercooling is required to solidify, which will be discussed in depth in Chaps. 3 and 4. Pb-based solder alloys have been used for at least 2,500 years (dating to the ancient Egyptians) or earlier during the early Bronze age. It was relatively easy to extract and form a good alloy with other elements at that time. Pb-based solders were used for jewelry and making



		Solder Alloy	Liquidus ● Temperature (°C)	Solidus ▽ Temperature (°C)
1	Low Temperature solder	Ga-21.5In-16Sn	11	11
2		Ga-24.5In	16	16
3		Ga-5In	25	16
4		Ga	30	
5		In-32.5Bi-16.5Sn	60	60
6		In--33.7Bi	72	72
7		Bi-26In-16Sn	79	79
8		Bi-33In	109	109
9		In-50Sn	125	118
10		Sn-48In	131	118
11		Bi-42Sn	138	138
12		In-3Ag	143	143
13		Sn-42In	145	118
14		In-5Bi	150	125
15		In-10Sn	151	143
16		In-0.5Ga	154	
17		In	157	
18		Sn-40Bi	170	138
19		Sn-37Pb	183	183
20	Medium Temperature solder	Sn-5.5Zn-4.5In-3.5Bi	186	174
21		Sn-20In-2.8Ag	187	175
22		Sn-8.8In-7.6Zn	187	181
23		Sn-9Zn	199	199
24		Sn-10In-3.1Ag	205	204
25		Sn-4.8Bi-3.4Ag	213	211
26		Sn-10Au	217	217
27		Pb-48Sn	218	183
28		Sn-3.8Ag-0.7Cu	220	217
29		Sn-3.9Ag-0.6Cu	220	217
30		Sn-3Ag-0.5Cu	220	217
31		Sn-3.5Ag	221	221
32		Sn-2.5Ag-0.8Cu-0.5Sb	225	217
33		Sn-4Ag-0.5Cu	225	217
34		Sn-2.5Ag	226	221
35		Sn-1Ag-0.5Cu	227	215
36		Sn-0.7Cu	227	227
37		Sn-1Cu	227	227
38		Sn	232	
39	High Temperature solder	Sn-25Ag-10Sb	233	
40		Sn-1Sb	235	
41		In-10Ag	237	143
42		Pb-40Sn	238	183
43		Sn-3Sb	238	232
44		Sn-5Ag	240	221
45		Sn-5Sb	240	235
46		Bi-5Sn	251	134
47		Au-20Sn	280	280
48		Sn-10Ag	295	221
49		Sn-3Cu	300	227
50		Pb-10Sn	302	275
51		Pb	327	

Fig. 2.6 Selected solder alloy compositions and liquidus/solidus temperature

bonds between metals including the ancient pipes in aqueducts [10–15]. Hence, in the periodic table, element symbol Pb comes from a Latin origin "plumbum" which is also the origin of plumbing, so it was natural to use Pb as an interconnect material. But since the ban on hazardous materials in consumer electronics since 2006, and beyond consumer electronics in the whole electronics industry nowadays, Sn-based solder alloys have replaced Pb-bearing solders in most applications [10–22]. Sn was also used in an alloy form since the Bronze Age, as it was the metal that made bronze. But replacing the Pb with Sn was not sufficient for solder joints, so alloying elements such as Cu and Ag to make Sn–Ag–Cu (SAC) alloys have brought performance necessary to meet requirements [23–36].

There are a number of SAC alloy compositions in current use, and many more have been developed in the past. The first recommendation for SAC family was made by both Soldertec and iNEMI in 2000, as a result of the IDEALS project in Europe. There are 33 alloys chronicled in the ELFNET/COST 531 database, but the property variation among these 33 alloys does not seem to be significant. The large variation in alloy compositions may be largely motivated by patenting and commercial issues. The IPC Solder Products Value Council studied the effect of this variation in a large collaborative program and concluded that there was very little performance difference between commonly used formulations. Low-silver alloys have nevertheless been an important new development, initially aiming at reducing costs of Ag but later for cultivating beneficial properties such as shock resistance, which will be discussed in depth in Chaps. 4–6 [37–39].

It is expected that more SAC alloys will be added to the existing family. Unlike previous motivations to win the market by differentiation, future development will be driven more by technology demand for tailored performance. While SAC solder is quickly replacing Pb–Sn solder in electronic packaging, packaging technology itself is rapidly changing with new directions. Overall miniaturization of existing packaging structure, such as flip-chip and BGA, is one direction, but another direction is 3D packaging where unusually small solder interconnects are essential. In such cases, as the solder amount is small compared to joining substrates, control of the intermetallic (IMC) bond layer growth is necessary. Excessive reaction with Cu in microbumps, for example, can result in a joint that is prone to failure by shock or fatigue. One notable development in this area is the microalloyed SAC system. SAC alloys containing a minute amount of Ni, Co, Mn, or Ge are now used as ball materials for BGA applications [27–32, 34, 36–44]. Similar alloys with Pd and Fe are also under investigation [30–45]. The beneficial effects of microalloying are becoming known, but the links between microstructure and reliability are not fully understood. Further, they may not provide enough protection against reliability issues stemming from excessive IMC growth. More ideal alloys may contain higher Cu to reduce reactivity with Cu without increasing brittleness of the solder alloy itself. Another reason for needing new SAC alloys for 3D packaging technology may be related to the process itself. The small volume of solder with large joint surface increases the likelihood of trapping cavities. This demands fluxless soldering or the use of flux that does not produce cavities. This will inevitably require different SAC solder alloys because existing alloys may not be compatible with a fluxless process or do not well work with new fluxes [46, 47].

The fact that SAC alloys prevail for present electronic packaging technology doesn't mean that alloy development is completed. There are continuing efforts to develop other alloy systems. Some of these efforts are motivated to adjust the strength (to lower it in many cases) of SAC alloys to improve reliability, while the other efforts will enable new packaging technologies. One of the most serious challenges to removing the Pb–Sn alloy system from the solder materials is the lack of suitable alloys for high-temperature applications. Many of the electronics used for automobile applications, for example, require solder alloys that can withstand operating temperatures near 150 °C [18, 19]. For such applications, solder alloys with melting temperature close to 300 °C or higher are essential. Previously, 95Pb–5Sn provided a reasonably high melting temperature as well as mechanical and chemical stability. Currently, there is no suitable Pb-free solder alloy that can provide such high-temperature application needs. One solder alloy that is qualified for such application is Sn–Au eutectic solder, but it is too expensive to be practical [48, 49]. A number of alloys currently considered and being developed include Sn–Sb and high Ag–Sn, but none of them provide properties comparable to 95Pb–5Sn [50]. Therefore, high-temperature solder is one area that is seeing an explosion of alloy development.

At the opposite end of the spectrum from high-temperature solders is low-temperature solder. There are two desired temperature levels for a low-temperature solder. The first is a melting temperature near 180 °C (the temperature of eutectic Sn–Pb), and the second is with 150 °C or lower. The purpose of the first type of alloy is to directly replace Sn–Pb eutectic alloy from the reflow temperature consideration. Since these alloys enable lower reflow temperatures than SAC alloys, they may look more eco-friendly and presumably provide a more reliable joint with lower residual thermal stress. These types of alloys include Sn–Zn, Sn–Bi, Sn–Zn–Bi alloys and their derivatives [37, 42, 51–55]. In fact, Sn–Zn alloys have been used in some applications but mainly in Japan. However, these alloys have one major weakness, that is, that they are prone to oxidation. Furthermore, for the same reason, they require the use of a strong flux and thus are not necessarily as eco-friendly as they appear. There are many studies in this area, but progress has been slow [56]. It is highly unlikely that this type of alloy will be as widely used as SAC alloys. Solder alloys with a melting temperature lower than 150 °C have also been pursued in the past. The need for low-temperature solder has risen mainly with the interest for solder-based 3D packaging and the die attachment. In order to enable 3D solder packaging process, it is necessary to have solder alloys with different reflow temperatures, so that already packaged interconnects are not disturbed by the subsequent reflow process. To this end, a handful of alloys have been investigated and developed, such as In–Sn, Sn–Bi and In–Sn–Bi. However, these alloys have multiple problems retarding their use for solder application, and their use is still very limited. One clear problem of low-temperature alloys is the fact that they are not stable against mechanical and chemical loads. Furthermore, the majority of them contain In, which is far more expensive than any other solder alloy element. This high cost also hinders their speedy adoption by the packaging industry.

Table 2.1 provides a summary of the mechanical properties in the current research database of the major lead-free solders [57]. All the data in the table were recorded at

Table 2.1 Tensile properties of SAC alloys

Solder alloy	Elastic modulus, E (GPa)	UTS (MPa)	Yield strength (MPa)	Strain rate (s^{-1})	Specimen preparation	Testing method	References
Sn-3.9Ag-0.5Cu	50.3	36.2	31.9	4.2×10^{-5}	Machined, cylindrical	Compression	[58, 59]
	54				Machined, cylindrical	Dynamic/ acoustic	[58, 59]
		60		1.78×10^{-3}	Cast, dog-bone, water quenched	Tension	[60, 61]
		41		1.78×10^{-3}	Aged 35 days at 25 °C	tension	[60, 61]
Sn-3.8Ag-0.7Cu	43.1				Solder joints	Nano indentation	[62]
	45	40	35	6.68×10^{-4}	Cast, cylindrical	Tension	[63]
	50	45		1.67×10^{-3}	Cast, cylindrical	Tension	[64]
	44.4	39.6	35.1	5.6×10^{-4}	Cast, dog-bone	Tension	[65]
	46			4-Oct	Cast, dog-bone	Tension	[66, 67]
	44.9				Solder joints	Nano indentation	[68]
	41	39	32	3-Oct	Cast, dog-bone	Tension	[69]
	46		47.1		Solder joints	Dynamic analyzer	[70]
Sn-4.1Ag-0.5Cu	43	36	33	6.86×10^{-4}	Cast, cylindrical	Tension	[63]
Sn-4.0Ag-0.5Cu	40				Cast, dog-bone	Tension	[66]
	48.3				Solder joint	Nano indentation	[71]
	45				Bulk solder	Nano indentation	[72, 73]
		51		3-Oct	Cast, dog-bone	Tension	[74]
Sn-3.0Ag-0.5Cu	54	41.8	25.3	4×10^{-3}	Machined, cylindrical	Tension	[75]
	37.4	43	37	5×10^{-4}	Cast, dog-bone	Tension	[76]
Sn-3.1Ag-0.5Cu	45	49	40	6.68×10^{-4}	Cast, cylindrical	Tension	[63]
Sn-3.2Ag-0.8Cu		32	28		Cast, cylindrical, quenched	Tension	[77]
		30	20		Air-cooled		
Sn-3.5Ag-0.7Cu		46.6			Cast, dog-bone	Tension	[66, 78]

Table 2.2 Tensile properties of Sn-37Pb eutectic solder

Solder alloy	Elastic modulus, E (GPa)	UTS (MPa)	Yield strength (MPa)	Strain rate (s^{-1})	Specimen preparation	Testing method	References
Sn–Pb eutectic	33.5	33.9	30.2		Cast, cylindrical	Tension	[79]
	27	47	41	6.86×10^{-4}	Cast, cylindrical	Tension	[63]
	32	39		1.67×10^{-3}	Cast, cylindrical	Tension	[64]
	32		32.5		Solder joints	Dynamic analyzer	[70]
	36	54		2×10^{-2}	Lap joints	Tension/shearing	[80]
	35	26		3-Oct	Machined, cylindrical	Tension	[81]
	29		29				[82]
	15.7	30.6	27.2				[83]
	32.1						[84]
		31–46					[85]

room temperature. There are large discrepancies in the tensile property values as well as the specimen preparation and testing approaches. The elastic modulus for SAC ranges from 30 to 54 GPa, although the majority of the values lie in the range of 40–50 GPa. The UTS values vary from 30 to 60 MPa, with the majority in the range of 35–45 MPa. The yield stresses range from 20 to 47 MPa, with the majority in the range of 25–35 MPa. All the differences in testing conditions, such as specimen geometry, testing methods, and testing strain rates, are likely to contribute to the variations.

Table 2.2 gives a summary of the mechanical properties of Sn–Pb eutectic solders, which also show large variations in the published mechanical properties [57]. The elastic modulus ranges from 16 to 36 GPa, the UTS values from 26 to 47 MPa, and the yield stress from 27 to 41 MPa. The large differences are reportedly due to the contribution of the inelastic deformation (plastic) from the slope of the stress–strain curve arising from the high homologous temperature of solders. The slope of the stress–strain curve therefore does not represent the true elastic modulus.

As the above data show, there are large discrepancies in the current database of mechanical properties for both lead-free and Sn–Pb solders. These discrepancies may have been caused by the lack of accepted standards for testing methods, specimen preparation, and testing conditions. However, none of the typical resources discuss the effect of room temperature aging, which may also lead to variations even for the same testing conditions due to the high homologous temperature of solder alloys. The room temperature aging effects have been known for decades, yet they may have played a significant role in the discrepancies in the published data.

Further assessment of details of selected solder alloys are found in Chap. 3 discussion of phase diagrams and the development of the microstructure in a joint in Chap. 4. Since the reliability of these interconnections are important in a product level configuration, it is important to have the system function as a whole and not to be concerned about each component, so the property and stability of the joint are crucial to understand. Chapters 5 and 6 will examine the evolution of thermal and mechanical performance, deformation mechanisms, and microstructure of these solder joints.

Board Assembly

To assemble the component to the PCB, as shown in Fig. 2.7, solder balls are first attached to the component. Usually a flux is applied on top of the Cu pad surface then solder balls are placed on top of it, using a fixture, followed by a thermal reflow. After the component has the solder balls attached, the components are brought to an assembly station. A solder paste is placed on top of each Cu pad on the PCB, and the component is precisely placed on top of each Cu pad footprint using a component placing machine. Then the board goes through a reflow oven which has several heating zones set at different temperature to have a specific reflow temperature profile, as shown in Fig. 2.8.

The reflow profile is defined by the relationship of temperature versus time during heating. A typical profile consists of three heating slopes (the time vs. temperature relationship or rate of heating). Each solder paste has recommended heating slopes and time and temperature limits within each slope. The three-step heating profile slopes are called preheat, dryout, and reflow, but usually the word reflow is used to cover the whole process. For a good quality assembly process (and ultimately a reliable solder joint formation), the optimum temperature profile must be found. The heating and cooling rates must be compatible with the solder paste, components, and the overall PCB. The duration of time that the assembly is exposed to certain temperatures is a crucial factor in order to have a defect-free solder joint.

In the preheat section, the goal is to fully preheat the entire SMT assembly to temperatures between 100 and 150 °C in the case of Pb-free assembly. The most critical parameter in the preheat section is to control the heating rate to 1–4 °C/s, avoiding a thermal shock that can cause defects during reflow. The second heating section, referred to as the dryout, soak, or preflow zone, is used primarily to ensure that the solder paste is fully dried with full activation of the flux before reaching the reflow temperatures between 140 and 170 °C for a 60–120-s time period. Dryout also provides thermal stabilization of large and small components to ensure uniform heating as the assembly enters the reflow zone. Once the boards reached the reflow temperature heating section, the solder paste and the solder ball melt, forming a solder joint. The cooling section following the solidification of the joint is also a crucial section since it is important to have a suitable cooling rate to reduce the residual stress which was built during solidification. Convection ovens have reduced the need for the thermal stabilization, as

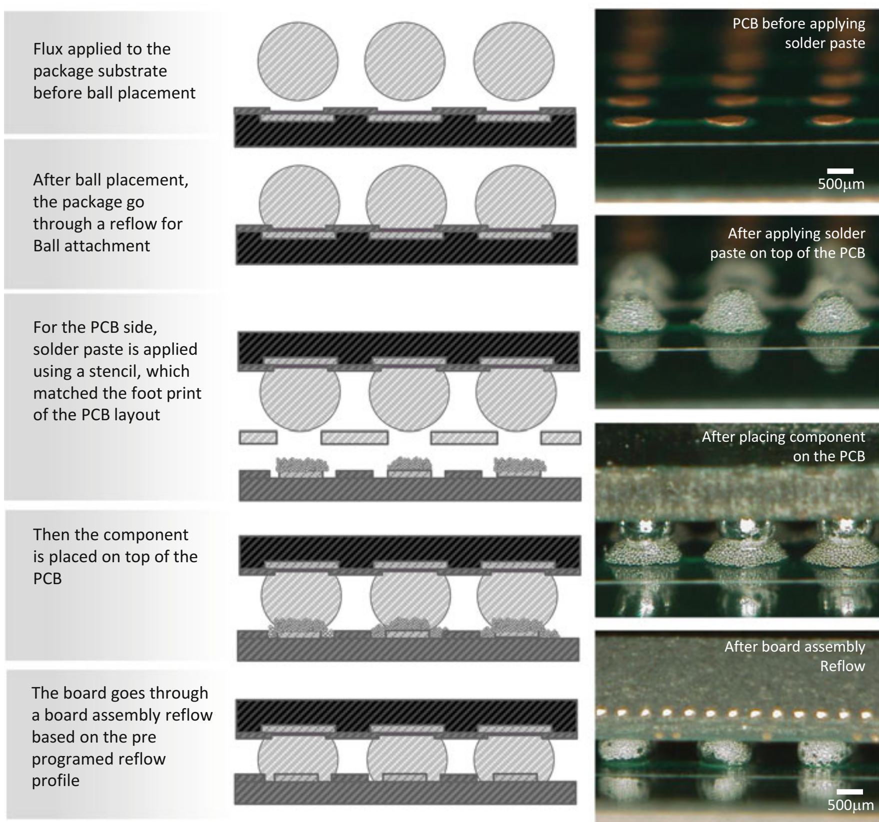


Fig. 2.7 Ball attachment and board assembly process diagram

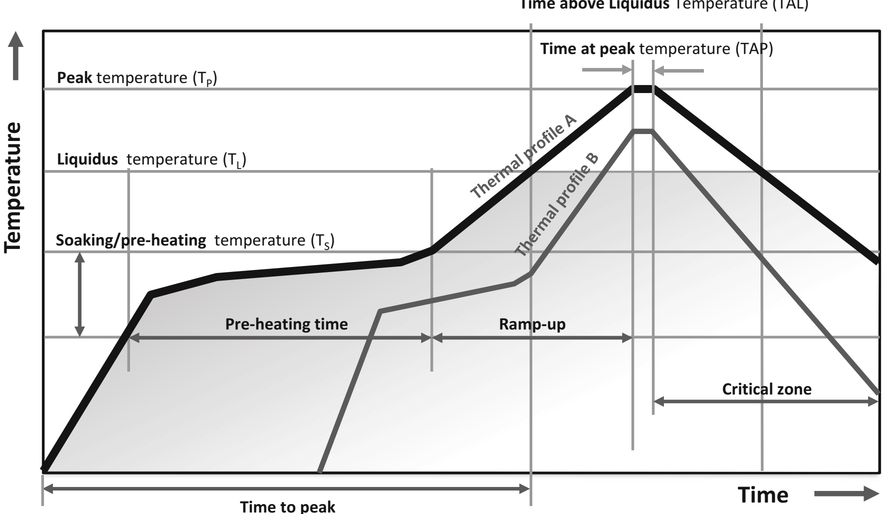


Fig. 2.8 Board assembly reflow profile

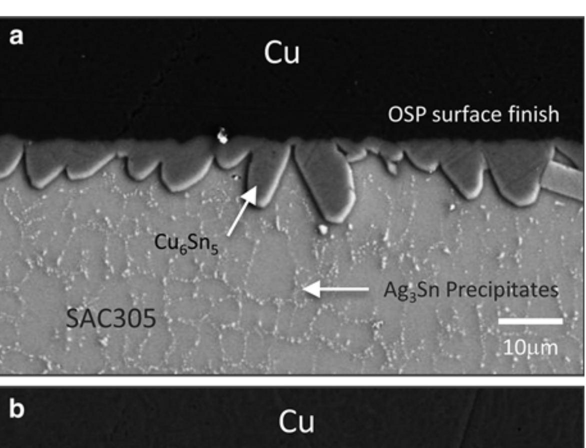
the temperature at all locations on the board tends to be uniform. Each component and board has its own unique design and hence, its own temperature distribution, so finding the right reflow profile for each product board is crucial to have a good quality board. A lot of defects can be produced when the profile is not right, as described in various publications with valuable information on SMT-related issues and defects [86].

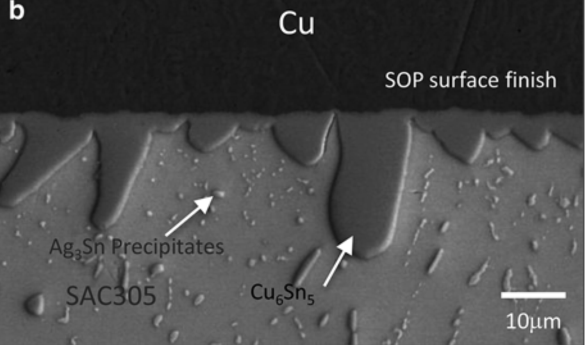
Package Side and Board-Side Surface Finish

Cu is used for both package-side pads and the board-side PCB pads. Although it reacts well with Sn and forms a strong intermetallic compound bonding layer, exposure of Cu pads to air can easily oxidize the Cu and cause dewetting/solderability problems [87]. So, to prevent oxidation and provide a relatively long shelf life before assembly, a coating layer is applied on top of the Cu pads, which is called a surface finish. Surface finish is an important material layer for both board-side and package-side interfaces, not only because it prevents oxidation, but also because it provides a diffusion barrier between the Cu pad and solder and sometimes accelerates the wetting. As shown in Fig. 2.4, the surface finish at both interfaces of the solder joints has a variety of options. A few selected surface finishes, which are widely used in the industry, are listed below, which includes organic solderability preservatives (OSP), solder on pad (SOP), immersion Sn (ImSn), electrolytic Ni gold (NiAu), electroless nickel immersion gold (ENIG), and electroless nickel/electroless palladium/immersion gold (ENEPIG).

OSP contain an azole compound and are applied on top of copper pads to protect the copper surface from oxidation. The OSP is transparent and has angstrom range thickness. OSP is widely used on the board-side interface surface finish and also at the package-side interface in BGA components. Another common surface finish is SOP surface finish. SOP is more widely used at the package-side interface pads. A thin layer of solder is pre-applied to cover the exposed Cu via printing or using a microball followed with a reflow. The solder alloys used for SOP are the alloy, which is matched with the solder ball alloy to be attached later. For example, if the solder alloy for ball attachment is Sn–Pb, then the SOP is Sn–Pb; if the Sn–Ag–Cu solder ball is the target alloy then the SOP is Sn–Ag–Cu. This means that after ball attachment and reflow, the SOP layer is fully mixed into the solder alloy, resulting in only the Cu and solder interface.

A similar but different surface finish is ImSn surface finish. Instead of using a certain solder alloy composition as used for SOP, ImSn surface finish is simply Sn plated on Cu. The Sn layer is consumed into the bulk solder material right after ball attachment reflow and results in the same interface structure as the SOP or OSP. But, slightly different interface properties result, since the plated Sn often has a minor dopant in the system to mitigate Sn whiskers during storage (usually a few 100 ppm level of Ag).





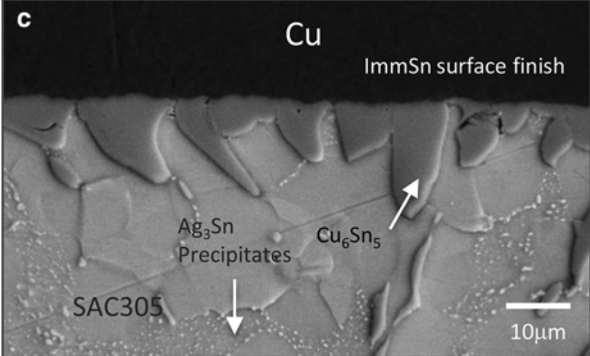


Fig. 2.9 Package side interface after board assembly using SAC305 solder with (**a**) OSP, (**b**) Solder on Pad (SOP), and (**c**) Immersion Sn surface finish (ImSn)

The bonding between the Cu and the solder alloy, such as SAC305, results in formation of an IMC compound layer. The thermodynamics between the formation of the IMC layer and the solder alloy itself will be thoroughly examined in Chaps. 3 and 4. Several good references are published which explain the details of the shape of the IMC layer [88–92], but as shown in Fig. 2.9, the IMC layer typically has a scallop-shaped interface. Between the Cu and the Cu_6Sn_5 IMC, a second IMC layer of Cu_3Sn forms, though it is not always thick enough to see right

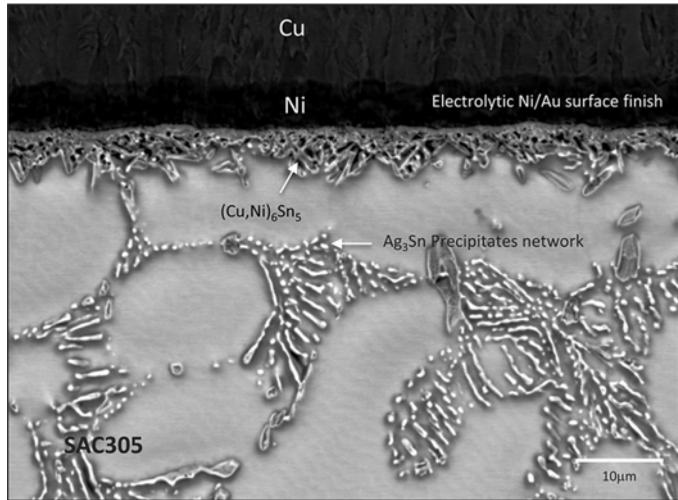


Fig. 2.10 Package side interface after board assembly using electrolytic NiAu surface finish

after assembly. The difference between two IMC layers is more clearly shown in samples after isothermal aging, discussed further in Chap. 4. The continuous diffusion of Cu into the solder and the Sn diffusion into the Cu region lead to a thicker Cu_3Sn layer and an evenly thickened Cu_6Sn_5 layer.

Another purpose of the surface finish is to prevent the Cu diffusion into the bulk solder. Since Cu is a fast diffuser, a prolonged exposure at high temperature during reflow can result in rapid consumption of the Cu pad that weakens the interface. One of the surface finish material options that reduce the consumption of Cu is a diffusion barrier layer of Ni. However, Ni has poor wettability for solder alloys, thus to facilitate wetting, a thin layer of Au is plated on top of the Ni surface. Applying the Ni on top on the Cu pad can be done using several different approaches. One is electrolytic plating and another is the electroless Ni plating method. Each surface finish has its own property and influence on the solder joint.

Electrolytic nickel gold (NiAu) surface finish is a widely used surface finish for package-side surface finish interfaces. Through an electrolytic process, a layer of around 3–5 μm nickel and a flash of gold layer (usually less than 0.75 μm of gold) are applied. The Au provides a good wettability and also a good corrosion protection of the Ni layer beneath. Most of the Au is consumed into the solder during the reflow process, and the Ni layer directly interfaces with the solder alloy by forming an intermetallic layer in between. With Ni in the surface finish composition, the interfaces show a different IMC layer morphology and composition than the OSP, SOP, and ImSn surface finish. Figure 2.10 shows a typical interface at the package-side

interface with NiAu surface finish and SAC305 solder alloy. Unlike the scallop type IMC for SOP and ImSn surface finish, the IMC here shows needle-shape IMC structure. These are $(Cu,Ni)_6Sn_5$ IMCs.

The Cu_6Sn_5-based intermetallic compound (IMC) containing Ni is the primary phase at the Sn–Ag–Cu/Ni interface with Cu content higher than 0.5 wt.% in the solder joint [93]. Ni exhibits significant solubility in Cu_6Sn_5, occupying the Cu atom sublattice to form $(Cu,Ni)_6Sn_5$ with up to 27 wt.% Ni. Thermodynamic calculations demonstrate that Ni additives can stabilize the $(Cu,Ni)_6Sn_5$ structure. The Gibbs free energy of $(Cu,Ni)_6Sn_5$ decreases by 9 kJ/mol as the Ni content increases to 20 wt.%, confirming that $(Cu,Ni)_6Sn_5$ is a more stable phase than Cu_6Sn_5 in solder joints [94]. In fact, Cu_6Sn_5 exists in two types of crystal structures and transforms from the monoclinic η′ Cu_6Sn_5 at temperatures below 186 °C to a more stable hexagonal η Cu_6Sn_5, which causes a volume expansion that generates internal stresses. With 5 wt.% Ni, $(Cu,Ni)_6Sn_5$ is stable in the hexagonal η structure at all temperatures [95, 96].

ENIG is another nickel-based surface finish. ENIG is formed by the deposition of electroless nickel–phosphorus (Ni–P) layer on a catalyzed copper surface followed by a thin layer of immersion gold. It provides a good diffusion barrier against reaction with Sn-based solders, has relatively low cost, and provides good wettability/solderability. The immersion gold protects the underlying nickel from oxidation/passivation in the same way as the electrolytic NiAu surface finish. The ENIG surface finish is used on the both package-side and board-side surfaces. The historical drawback was that the electroless nickel layer is brittle and has been found to break up during mechanical stress. Also, a galvanic hypercorrosion occurs on the Ni–P surface layer caused by the immersion Au solution, which is usually called "black pad" [97], due to the formation of Ni oxide that degrades the interfacial strength. These drawbacks can be avoided with better process control and are now less problematic. Although the processes in the industry are well tuned and controlled, the fundamental risk for black pads can be overcome by using ENEPIG surface finish. Pd prevents corrosion of the Ni–P layer that occurs before the immersion Au plating solution is used. ENEPIG is very similar to ENIG and is formed by the deposition of electroless nickel followed by 0.2 μm of electroless palladium with an immersion gold flash (~0.03 μm). The palladium is plated on the electroless nickel by chemical reduction instead of a displacement reaction, which prevents attack on the electroless nickel layer.

Figure 2.11 shows a schematic diagram comparing ENIG and ENEPIG. Also, the growth behavior of Cu_6Sn_5 and $(Cu,Ni)_6Sn_5$ in ENIG and ENEPIG joints in Fig. 2.12 shows differences in the interfacial reaction of ENIG and ENEPIG solder joints. Irregular-shaped IMCs formed after reflow on both metallizations. During the early stage of soldering, the thin Pd finish as well as the Au finish dissolves into the solder within a few seconds [98]. Pd was dissolved into the solder matrix since very low Pd concentration (about 0.01 wt.%) was detected by FE-EPMA. On the other hand, a slightly higher amount of Pd (0.3 wt.%) was found in the

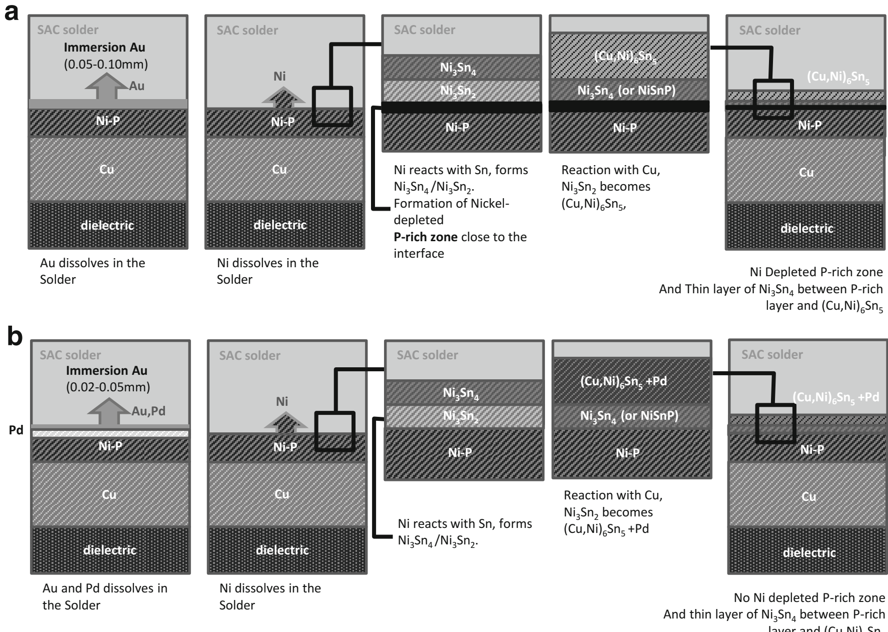


Fig. 2.11 Schematic comparison between (**a**) ENIG and (**b**) ENEPIG reflow process and layer evolution on the package side

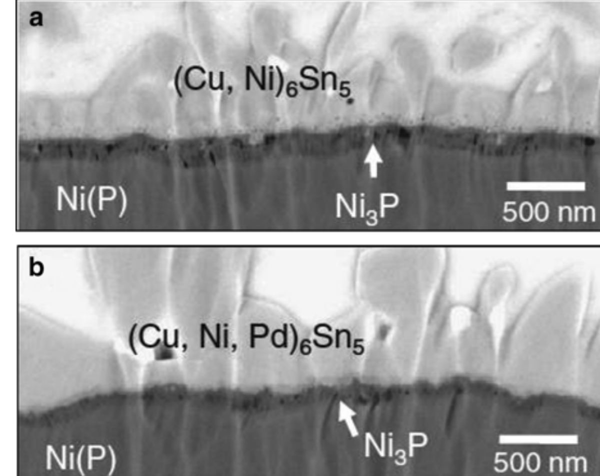


Fig. 2.12 Cross-sectional images of reflowed joints with columnar voids after thermal aging: (**a**) ENIG surface finish, (**b**) ENEPIG surface finish [100]

$(Cu,Ni,Pd)_6Sn_5$, implying that Pd was likely to dissolve into the IMC. Pd may refine the grain structure of $(Cu,Pd)_6Sn_5$ and also inhibit its grain growth [99]. The refinement of grain size may be attributed to lattice strain arising from the different atomic radii of Cu (128 pm) and Pd (137 pm), which causes slower grain growth in Cu_6Sn_5 [100].

Other than the surface finishes stated above, there are immersion silver (ImAg) and hot air solder leveling (HASL) surface finish. Silver is deposited directly on the copper surface by a chemical displacement reaction for the ImAg surface finish. The reaction is fast and does not require the relatively high-temperature exposure usually associated with ENIG, and the contrasting color makes it easier to inspect than OSP. While there is some consideration related to silver migration, anti-migration agents have been added to minimize the effect. Hot air solder leveling (HASL) was a widely used surface finish before lead-free solders for board-side surface finish. The process consists of immersing circuit boards in a solder alloy (the alloy is composed of tin (Sn) 99.7 % and copper (Cu) 0.3 % with traces of nickel (Ni)), and the excess solder is then removed by so-called air knives, which blow hot air across the surface of the board. The increased complexity of boards and finer pitches has exposed many limitations with the HASL finish, but with recent efforts to prevent Cu pad corrosion in harsh environments, HASL can serve as an option for some end-use conditions because it usually covers all exposed metal pads.

The Correlation Between the Surface Finish and the Solder Joint

One important factor related to the Ni-containing surface finish is that not only the region where the surface finish is applied but that the other end of the solder joint is also affected by the introduction of Ni into the solder joint. As illustrated in Fig. 2.7, the schematic drawing on the process from ball attachment to board assembly, the surface finish at the package side affects the board-side interface composition. The case for OSP, SOP, or ImSn might be minimal because the main compositions are simply Sn and Cu, but for surface finish containing Ni or Pd, the board-side interface IMC is mostly affected and getting into a relatively complex structure. One example for electrolytic NiAu surface-finished samples in Fig. 2.13 compares two package side surfaces: one is the OSP surface finish and the other is the NiAu surface finish. The interface at the board side, even though it is OSP for both cases, is affected by the surface at the package side. The series of EPMA maps in Fig. 2.14 after reflow also show that the board interface IMC has Ni in it. This indicates that elements in the surface finish at the package side actually affect the opposite board side by first dissolving into the molten solder and then forming/

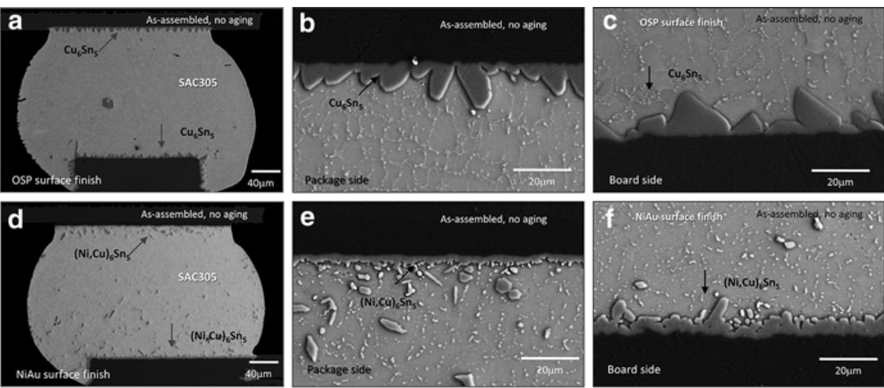


Fig. 2.13 SEM microstructure after board assembly (unaged) of OSP (**a**–**c**) and NiAu (**d**–**f**) surface finishes: (**a, d**) Overall view of the joint, (**b, e**) higher magnification of the package side interface, and (**c, f**) board side interface

solidifying at the board interface. Thus, the surface finish composition is an important factor that directly influences the solder alloy composition and also the property of the joint. It is an additional source of elements, which can alter the composition of the solder alloy and at the same time affect the ultimate property of the material.

The additional Ni present on the board-side interface IMC during reflow occurs due to the diffusion of the Ni through the molten Sn and the formation of IMC at the time of solidification as shown in Fig. 2.15. At the ball attachment process reflow, a limited amount of Cu forms the Cu_6Sn_5 IMC at the interface, and Ni from the surface finish diffuses into the IMC formation resulting in a $(Cu,Ni)_6Sn_5$ IMC composition. Once the component is assembled to the board, a sufficient source of Cu is typically available from the board-side Cu pad. So, the IMC at the package-side interface forms additional IMC in the form of $(Cu,Ni)_6Sn_5$. Because after a certain thermal exposure, additional IMC formation or growth happened, but this time the composition is slightly different. After aging, the IMC became layer-like at the solder/Ni interface, and two kinds of $(Cu,Ni)_6Sn_5$ with different Ni contents were detected as shown in Fig. 2.15c. The elemental map analysis using EPMA indicates that a continuous L-$(Cu,Ni)_6Sn_5$ layer with a lower Ni content formed above the H-$(Cu,Ni)_6Sn_5$ IMC, proving that the Ni is distributed nonuniformly in $(Cu,Ni)_6Sn_5$. This phenomenon will be further examined following isothermal aging in Chap. 4 and its effect on thermal and mechanical performance in Chaps. 5 and 6.

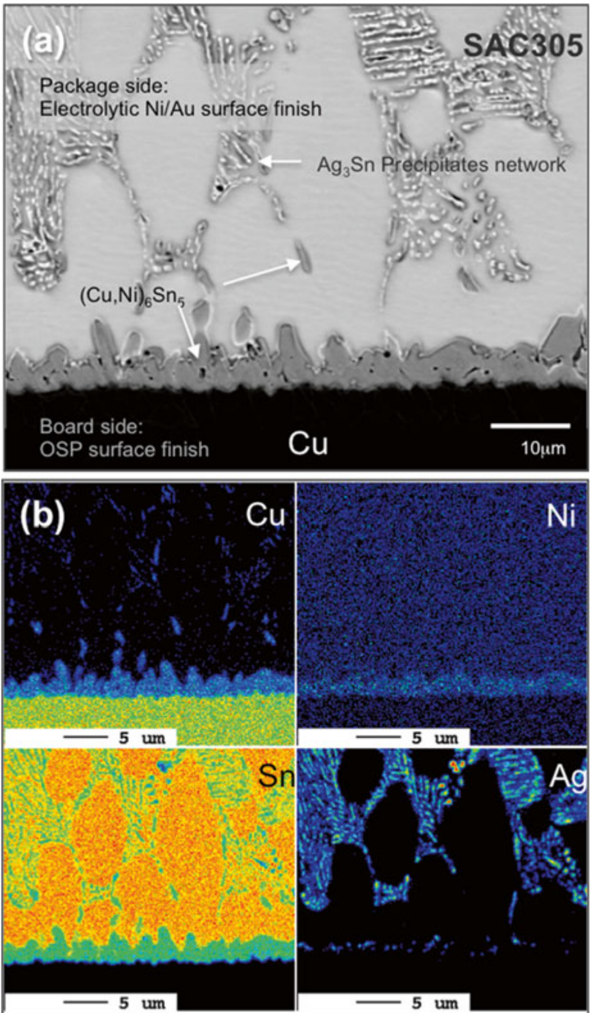


Fig. 2.14 Board side interface and bulk region SEM image after board assembly with NiAu surface finish on the package side. (**a**) SEM, (**b**) Cu, Ni, Sn, and Ag EPMA maps

Summary

In this chapter, we described interconnects at three scales: at the largest scale of connecting components, the structure of the package and boards, and then the microstructure of the interfaces between the solder and the package and board. We considered the variety of solder alloys and the process of board assembly and the importance of the package-side and board-side surface finish. Also, we

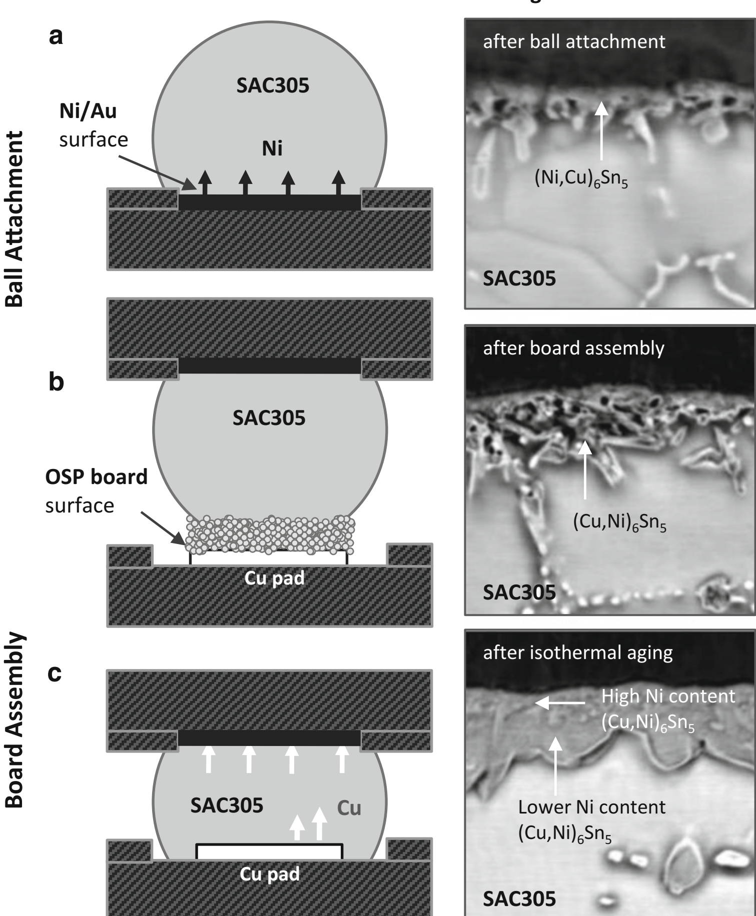


Fig. 2.15 Interface microstructure development and IMC formation in the joint formation process. (**a**) Ball attachment to the package substrate reflow, (**b**) package placement on top of solder paste applied onto PCB, and (**c**) board assembly reflow

considered how the surface finish affects the microstructure and phases present in the intermetallic layer between the solder and package or board. Several additional factors and elements that make a simple structure into a complex system with various interactions have different roles that can improve one aspect of the interconnect and degrade another. In the next chapters, we will examine the mechanisms that govern the thermal and mechanical performance. Figure 2.16 shows the chapter summary.

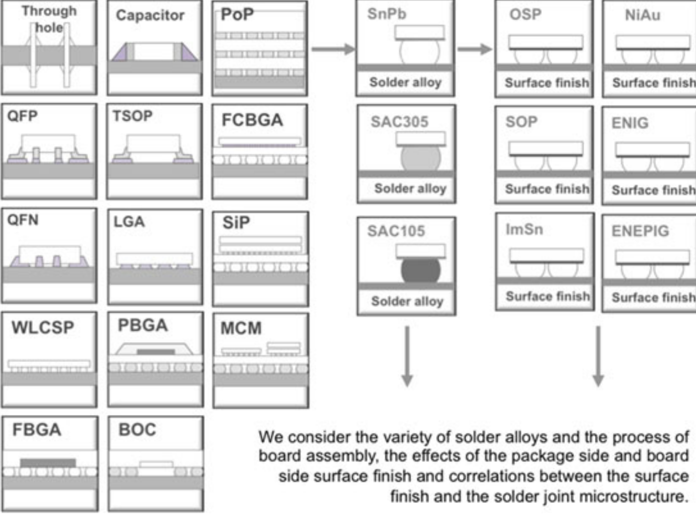


Fig. 2.16 Overall summary diagram of Chap. 2

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Chapter 3
Phase Equilibria and Microstructure of Sn–Ag–Cu Alloys

This chapter presents a brief description of ideal microstructures of the SAC family alloys based on consideration of phase equilibria. It first introduces the eutectic microstructure along with a brief discussion of the ternary phase diagram. Then, the sensitivity of SAC microstructure on very small changes in composition surrounding the eutectic composition is discussed. The microstructural sensitivity of the alloy composition stems from the fact that there are 6 possible phase fields for the primary phase formation. The primary phase refers to the phase that is in equilibrium with the liquid phase at off-eutectic composition and is the phase that forms prior to the eutectic reaction during solidification. A detailed description of SAC microstructure in each phase field is presented using the results gained from the differential cooling method. Solder microstructures used in real interconnects can be significantly different from what is predicted from the phase equilibria, mainly due to the existence of many contamination sources such as the joining substrates and also due to nonequilibrium cooling. Such effects are discussed to assist interpretation of microstructure and properties of solder joints. This chapter sets the foundation on which nonequilibrium microstructures that form in practical joints can be understood, as discussed further in Chap. 4.

Why Phase Equilibria Matter

Studies on phase equilibria of the SAC solder system have been extensive ever since its introduction, and those experimental and theoretical studies have resulted in a reasonably accurate phase diagram [1–11]. Nevertheless, misinterpretation of SAC microstructure often occurs in this field mainly due to the fact that its eutectic microstructure consists of a small fraction of Ag_3Sn and Cu_6Sn_5 phases embedded in large fraction of β-Sn phase [12–16]. This creates considerable difficulty in distinguishing the phases formed by the primary phase and the later eutectic reaction. An added difficulty is related to the fact that solder alloys are subjected to a highly

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T.-K. Lee et al., *Fundamentals of Lead-Free Solder Interconnect Technology*,
DOI 10.1007/978-1-4614-9266-5_3

nonequilibrium cooling process because nonequilibrium cooling can skew the size and fraction of the constitutional phases [14]. In order to control the solder joint microstructure, it is important to understand the equilibrium microstructure, as the system will move in this direction after it has solidified in a nonequilibrium manner. Any microstructural deviation from the ideal can then be related to the influence of process conditions, external factors such as contamination, and changes in the composition by interface reactions with the interface substrates [17–19].

The aim of this chapter is not to present a theoretical description of the phase equilibria in the SAC system as it is beyond the scope of this book. Rather, our intention is to provide a sufficient description of the SAC microstructure at equilibrium condition so that engineers and scientists can understand how microstructure of SAC alloys develops and identify the factors affecting the solder joint microstructure. To this end, this chapter describes (1) the ideal ternary eutectic microstructure of SAC system, (2) the microstructure of off-eutectic compositions, (3) the influence of nonequilibrium cooling, and (4) the changes in microstructure caused by a few typical contaminants.

Eutectic Microstructure of Sn–Ag–Cu Eutectic

The ternary phase for the entire Sn–Ag–Cu system is complex due to the existence of many binary intermetallic and intermediate phases. The binary phase diagram of the Ag–Cu system shows that Ag–Cu forms a simple eutectic. However, in the cases of Sn–Cu and Sn–Ag, there are multiple binary phases that make the phase equilibria complex. As shown in Fig. 3.1a, where the liquidus surface projection

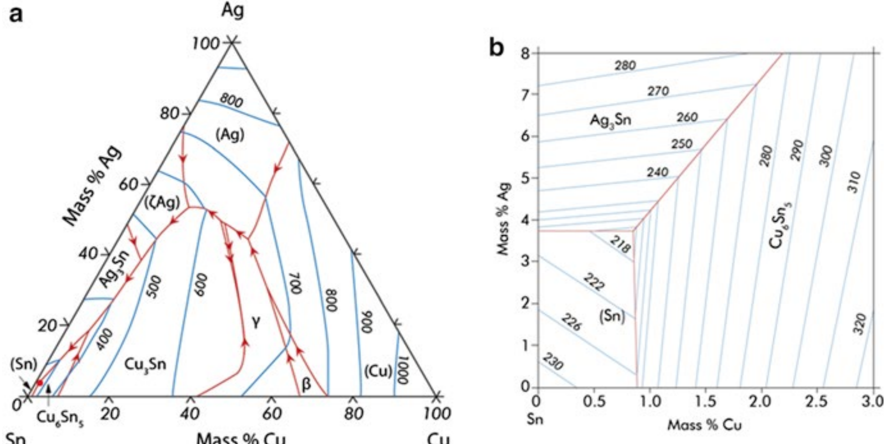


Fig. 3.1 (**a**) Ternary phase diagram of Sn–Cu–Ag system showing liquidus surface projection, (**b**) liquidus surface project of Sn–Ag_3Sn–Cu_6Sn_5 ternary eutectic system. (These diagrams are reconstructed using the data in Moon et al. [4])

of the entire ternary system is shown, there are several invariant reactions. Fortunately, the ternary eutectic system of primary interest, consisting of β-Sn, Ag_3Sn, and Cu_6Sn_5 phases, exists at the Sn-rich corner. Because Ag_3Sn and Cu_6Sn_5 phases are thermodynamically independent phases, a reduced ternary diagram consisting of β-Sn, Ag_3Sn, and Cu_6Sn_5 can be constructed, meaning that other binary phases do not need to be included in the phase equilibrium considerations at the Sn-rich corner. Figure 3.1b shows this corner in the established diagram, which displays the liquidus surface projected in a Cartesian plot where x- and y-axis represent the Cu and Ag concentration, respectively, with scales that are not the same. The liquidus surfaces merge at one point with decreasing temperature to the point where eutectic reaction occurs. Binary and ternary invariant reactions existing in this Sn-rich ternary system are listed in Table 3.1. The compositions relevant to the eutectic reaction in binary systems, namely, Ag–Cu, Sn–Ag_3Sn, and Sn–Cu_6Sn_5, are very well known. On the other hand, the composition and temperature for ternary eutectic reaction is not consistent among existing studies.

The first study on the SAC eutectic point was conducted by Gebhardt and Petzow [9] and later followed by Miller [10] who carried out compositional and differential thermal analysis (DTA) of the eutectic microstructure found in Sn-3.6Ag-1.5Cu alloys. Miller's analysis of the eutectic microstructure suggested that the eutectic composition of SAC system is Sn-4.7Ag-1.7Cu. However, Loomans and Fine [11] reexamined the Sn-4.7Ag-1.7Cu alloy using differential scanning calorimetry (DSC) and concluded that the eutectic is Sn-3.5Ag-0.9Cu. Moon et al. [4] carried

Table 3.1 Eutectic reactions existing in binary and ternary alloy of Sn–Ag–Cu

Alloy system	Reaction	*T* (°C)	Composition (wt.%)	Note
Ag	$L \rightarrow$ FCC Ag	961.93	100Ag	
Cu	$L \rightarrow$ FCC Cu	1084.67	100Cu	
Sn	$L \rightarrow$ BCT Sn (b-Sn)	221.67	100Sn	
Ag–Cu	$L \rightarrow$ Ag + Cu	779.1	28.4Cu	43
Ag–Sn	$L \rightarrow$ b-Sn + Ag_3Sn	220.9	3.5Ag	44, 45
Cu–Sn	$L \rightarrow$ b-Sn + Cu_6Sn_5	227.0	0.89Cu	46
Sn–Ag–Cu	$L \rightarrow$ b-Sn + Ag_3Sn + Cu_6Sn_5	225	4Ag-0.5Cu	9
		218	4Ag-0.5Cu	47
		217	4.7Ag-1.7Cu	10
		217	3.5Ag-0.9Cu	11
		217.7	3.24Ag-0.57Cu	7, 8
		217.2	3.5Ag-0.9Cu	4
		217.3	3.63Ag-0.85Cu	48

The phases and the eutectic reactions in ternary alloy system are limited to those at the high Sn side

out both theoretical and experimental studies on the phase equilibria of SAC system and found that the two approaches led to two different eutectic compositions. Their experimental study found that the Sn-3.5Ag-0.9Cu is close to a eutectic composition, but a theoretical calculation of the phase equilibrium predicted Sn-3.66Ag-0.91Cu to be the eutectic composition. While a microstructure study led by Lewis et al. supports the experimental conclusion of Moon et al., the study of phase equilibria by Ohnuma et al. [7] disagrees as it finds Sn-3.24Ag-0.57Cu to be a eutectic alloy. Also inconsistent among studies is the eutectic temperature; however, recent studies tend to agree that it is near at 217 °C [2].

The difficulty in finding the eutectic point of the ternary SAC system probably originates from the fact that the ternary eutectic microstructure is overwhelmed by the β-Sn phase as the fraction of Cu_6Sn_5 and Ag_3Sn phase is very small. It is not so easy to separate the primary phases (phase solidifying by an off-eutectic solidification event) and phases in the eutectic microstructure in such circumstances. Identification of the eutectic alloy using DTA or DSC analysis is equally difficult because the peak associated with the eutectic reaction can overwhelm the small peaks from the off-eutectic reactions. The best way of finding the eutectic point is to grow a pure eutectic alloy and then characterize its composition and melting temperature. A research team led by one of the authors of this book, Kim, used this approach by growing a pure eutectic SAC alloy in a Bridgman furnace. Although not yet published, this research reveals that the eutectic point is located at 217.3 °C with 3.63 % Ag and 0.85 % Cu (all weight percent), which is very close to the one suggested by Moon et al.

A common use of the Bridgeman technique is to grow single crystals. Since it is simple and inexpensive to operate, it is one of the most popular techniques of growing single crystals for research purposes. This method is very similar to the method of directional cooling in that it induces solidification under an extreme temperature gradient. The difference is that the Bridgman method induces solidification at an extremely slow rate, a few millimeters per day. In this method, the target material is encapsulated in an inert container with a pointed end followed by placing it in a furnace for melting. By slowly advancing the pointed end of the melt into the area where a temperature gradient exists, an embryonic solid forms when the end reaches the position for the solidification temperature. This embryo acts as a seed for subsequently growing a single-crystal solid by a slow and steady advancement of the whole container.

Although not well known, this method is also effective in growing pure eutectic crystal from the off-eutectic alloy. This is possible because the eutectic is at the lowest melting temperature of all possible phases in the phase equilibria. When the starting alloy has an off-eutectic composition, the first solid phase forms from the melt are the first primary phase because it has the highest melting temperature at the given condition. Slow and directional crystal growth provides sufficient time for the remaining liquid to achieve compositional uniformity through diffusion and convection. Continued crystal growth in this manner removes the off-eutectic phase from the melt, making the liquid to be enriched with eutectic liquid. The pure eutec-

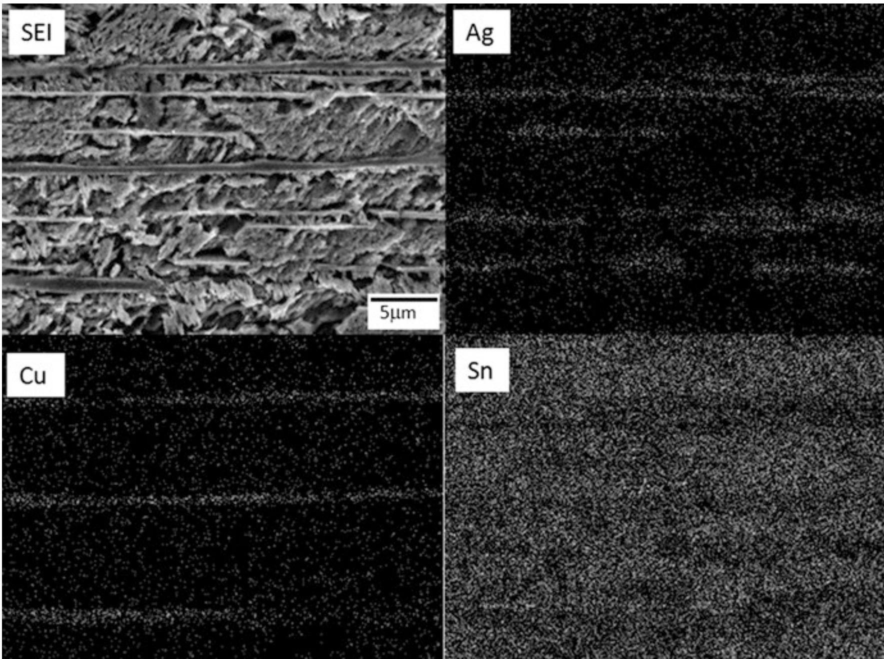


Fig. 3.2 A SEM micrograph and elemental mapping images showing the eutectic microstructure of Sn–Ag–Cu solder alloy. This single crystal eutectic alloy is produced using the Bridgeman method. Note the presence of Ag_3Sn and Cu_6Sn_5 phases with continuous secondary phases. The images were taken after slight etching of the Sn matrix to reveal the IMC phases. The *top left image* displays the SEM image, and the other show X-ray elemental mapping image for Ag, Cu, and Sn

tic alloy then can be acquired by analyzing a piece of the sample from the last part of the crystal to solidify.

SEM micrographs in Fig. 3.2 present the microstructure of pure eutectic SAC alloy grown by the Bridgman method. Since this sample was grown with an extremely slow rate, ~3 mm/day, the sample was in fact found to be a eutectic single crystal. Compositional analysis of this sample using WDX (wavelength dispersive x-ray spectroscopy) indicated that the final solidifying alloy contained 3.63 % Ag and 0.85 % Cu. This can be taken as the eutectic composition with greater confidence than the other studies. Considering the accuracy limitation inherent to WDX, composition analysis using other methods such as atomic absorption appears to be necessary to confirm the result. Also visible is the presence of Cu_6Sn_5 and Ag_3Sn IMC phases that grow together in the direction of crystal growth. It was found that Ag_3Sn grew as a plate and Cu_6Sn_5 as a flat bar with facets. The shape of Ag_3Sn is consistent with its equilibrium shape in eutectic microstructure suggested by others. However, the shape of Cu_6Sn_5 is somewhat different from other investigations.

A commonly observed shape of Cu_6Sn_5 phase in eutectic microstructure is either a hollow short rod or a hollow blocky particle with facets. Because the Bridgman furnace induces growth of eutectic phases near or at equilibrium conditions, the rod-shape Cu_6Sn_5 found in other studies may be a result of nonequilibrium cooling. On the other hand, because the Bridgman method forces IMC phases to grow in the direction of the temperature gradient, there is a possibility that the shape developed by the Bridgman method may be a result of directional growth. However, considering the fact that both shapes share commonality in a sense that one axis is longer than the other, it is probable that a flat bar is an ideal shape for Cu_6Sn_5 in SAC eutectic. The short rod can form when the cooling rate is less ideal because surface energy anisotropy is to play a role. The widely dispersed blocky particles in solder microstructure are probably not the part of eutectic but a primary phase. Since the eutectic growth demands tight maintenance of phase equilibrium among all four phases (liquid and three solid phases), the growth of IMC phases has to be coordinated. If not, phase equilibria at the growth front of the eutectic, especially on the liquid side, will be distributed. It is difficult to imagine that widely dispersed Cu_6Sn_5 particles can satisfy the needed phase equilibrium condition. It is more reasonable to conclude that the equilibrium microstructure of SAC eutectic consists of Ag_3Sn plates and Cu_6Sn_5 flat bars (or rods) embedded in the β-Sn matrix.

Off-Eutectic Microstructure

All commercial SAC solder alloys have an off-eutectic composition. A SAC alloy containing 3.8 % Ag and 0.7 % Cu (Sn-3.8Ag-0.7Cu) has been marketed as a eutectic solder alloy. However, even if it was the alloy with eutectic composition, it is more likely to have an off-eutectic composition because mass production of an alloy without compositional variation is impossible. All SAC alloys therefore should be treated as off eutectic, so then it is necessary to understand how solidification proceeds in an off-eutectic condition.

Unlike binary alloys, the off-eutectic solidification in a ternary system is more complex to describe due to the presence of several different solidification paths. In principle, there are six different solidification paths that a SAC alloy can take, and the path is determined by the composition of the alloy. If we denote α, β, and γ as solid phases in the ternary eutectic, the off-eutectic solidification sequence can be described by three reaction equations:

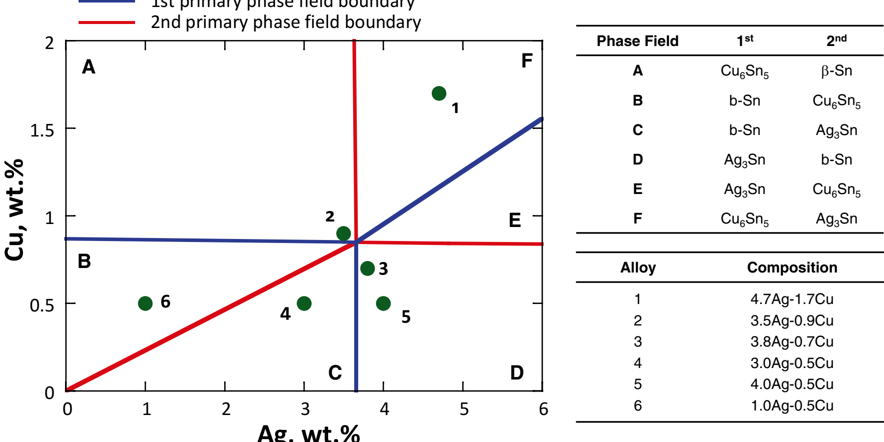
$$L \rightarrow L + \alpha \tag{3.1}$$

$$L + \alpha \rightarrow L + \alpha + \beta \tag{3.2}$$

$$L + \alpha + \beta \rightarrow \alpha + \beta + E(\alpha + \beta + \gamma), \tag{3.3}$$

where E represents the eutectic reaction. As indicated in (3.3), any alloy in a simple ternary eutectic system passes through three different phase fields during its solidification. Since there are two primary phase fields and three solid phases, there are six variations. Figure 3.3 shows the diagram for the first and second primary phase field as a function of composition. Also shown is the position of a few commercial SAC alloys in the phase field diagram. The phase field sequence for those alloys is confirmed through microstructural analysis described later. Note that a seemingly minor compositional difference in alloys places them in completely different phase fields. For example, the Sn-3.5Ag-0.9Cu alloy may seem similar to the Sn-3.8Ag-0.7Cu alloy in terms of composition. However, these two alloys are located in different phase fields. The first and second primary reactions of the Sn-3.5Ag-0.9 alloy involve Cu_6Sn_5 and β-Sn, respectively. On the other hand, the Sn-3.8Ag-0.7Ag is in the section where Ag_3Sn is the first primary and β-Sn is the second primary phase. This illustrates the fact that the phase equilibria of SAC alloys are very sensitive to the alloy composition and emphasizes the need for careful characterization of the phases present in a given alloy.

The phase field diagram shown in Fig. 3.3 may suggest that the alloy simply produces two primary phases, α and β precipitates, prior to the eutectic reaction. However, this is not the case and is more complex. When the temperature of the melt crosses the liquidus surface of the alloy, the α phase forms. With phase separation, the liquid phase composition moves toward that of the binary $(\alpha+\beta)$ eutectic liquidus line, which starts from the binary $\alpha+\beta$ eutectic point and ends at the ternary eutectic point. The solidification at this phase field is not a simple formation of β phase but a formation of $(\alpha+\beta)$ binary eutectic. Continuation of binary eutectic



Phase Field	1st	2nd
A	Cu_6Sn_5	β-Sn
B	b-Sn	Cu_6Sn_5
C	b-Sn	Ag_3Sn
D	Ag_3Sn	b-Sn
E	Ag_3Sn	Cu_6Sn_5
F	Cu_6Sn_5	Ag_3Sn

Alloy	Composition
1	4.7Ag-1.7Cu
2	3.5Ag-0.9Cu
3	3.8Ag-0.7Cu
4	3.0Ag-0.5Cu
5	4.0Ag-0.5Cu
6	1.0Ag-0.5Cu

Fig. 3.3 Phase diagram showing the first and second primary phase field as a function of Cu and Ag content. Table shows the phase field sectors and corresponding phases that form during solidification process. The *numbered dots* shown in the figure represent the composition of a few commercially available SAC alloys

solidification shifts the liquid composition toward that of the ternary eutectic until the tertiary reaction, that is, ternary eutectic reaction, completes the solidification. Equation (3.3) can be rewritten to include this sequence:

$$L \rightarrow L + \alpha_P \tag{3.4}$$

$$L + \alpha_P \rightarrow L + \alpha_P + \beta_P + E(\alpha + \beta)_P \tag{3.5}$$

$$L + \alpha_P + E(\alpha + \beta)_P \rightarrow \alpha_P + \beta_P + E(\alpha + \beta)_P + E(\alpha + \beta + \gamma), \tag{3.6}$$

where subscript P is used to represent the phases formed by the primary reaction. Whether the binary eutectic reaction occurs or not as a part of the second primary reaction depends on the starting composition of the alloy. If the alloy composition is in close proximity to the binary eutectic line, the binary eutectic reaction would eventually occur at the later part of the second primary reaction. In that case, the final microstructure would consist of α phase formed by the first primary reaction, β and $(\alpha+\beta)$ binary eutectic by the second primary reaction, and then the $\alpha+\beta+\gamma$ ternary eutectic by the tertiary reaction. This phase formation sequence explains why a proper characterization of SAC microstructure is a challenging task even in slowly cooled bulk alloys. The phases existing in Sn-3.8Ag-0.7Cu, for instance, are $(Ag_3Sn)_P$, β-Sn_P, E$(Ag_3Sn+\beta\text{-}Sn)_P$, and E$(Ag_3Sn+\beta\text{-}Sn+Cu_6Sn_5)$ as its composition is close to the $(Ag_3Sn+\beta\text{-}Sn)$ binary eutectic line. With a microstructure having a small total volume fraction of Ag_3Sn and Cu_3Sn, it will be difficult to distinguish the $E(Ag_3Sn)_P$ from $(Ag_3Sn)_P$, because E$(Ag_3Sn)_P$ is embedded in $E(\beta\text{-}Sn)_P$ matrix. Note that the $E(\beta\text{-}Sn)_P$ phase would be almost indistinguishable from the β-Sn in the ternary eutectic. The situation would be the same when the binary eutectic in the microstructure is $(Cu_6Sn_5+\beta\text{-}Sn)$. The microstructure of the $(Cu_6Sn_5+Ag_3Sn)$ eutectic mixture in the ternary eutectic can exist if the alloy has a composition located at E and F in the phase diagram of Fig. 3.3. It can exist as a particle with a core-shell structure, that is, one phase at the core and the other at the shell. Nevertheless, such particles would be difficult to locate because they exist in small numbers, and the core may not be identifiable.

Evidently, tracking the phase equilibria of a SAC alloy based on the microstructure is nearly impossible. One can overcome the difficulty by using a “differential cooling” technique. The principle idea behind this technique is to induce prolonged growth of primary phases by holding the target alloy at temperature where the presence of the primary phase field is suspected. By quenching the alloy after the hold, the remaining melt is forced to solidify in a fine microstructure. This enables easy and error-free identification of the primary phase. Figure 3.4 shows a schematic representation of a temperature profile used for differential cooling. As shown, two holding temperatures are needed to identify the first and the second primary phases. Park et al. [2] investigated the phase equilibria of Sn-3.8Ag-0.7Cu by using differential cooling to prove that the alloy is not a eutectic alloy as generally believed.

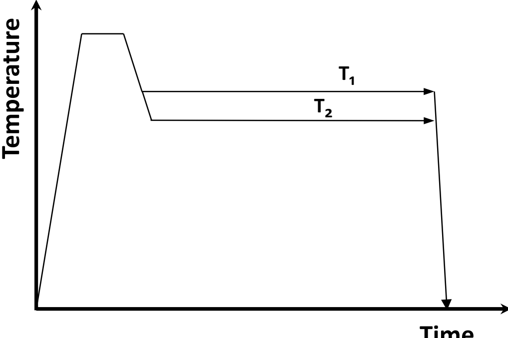


Fig. 3.4 A schematic diagram showing the temperature–time profile used in the differential cooling method. Samples are kept at temperatures where the primary phase formation is suspected to induce preferential growth of the phases. In this way, the primary phases and their formation sequence (1st and 2nd) for a given alloy system can be correctly identified

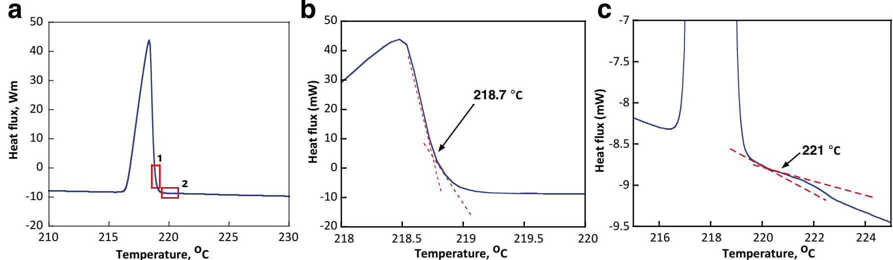


Fig. 3.5 Plots showing a DSC result of Sn-3.8Ag-0.7Cu (alloy 3 in Table 3.2). The data are taken from the heating run with a rate of 5 °C/min. The result appears to show a single reaction peak at 217.3 °C (**a**) but close inspection of the 1 and 2 area suggests that there exist two additional reactions (**b, c**) occurring near at 218.7 and 221 °C

Figure 3.5a presents a representative DSC curve of the alloy tested at a heating rate of 5 °C/min. Since the melting of an alloy is an endothermic reaction, the DSC curve shows a corresponding peak that begins at 217.3 °C and ends roughly at 219 °C. The plot shown in Fig. 3.5a appears to show only a single peak and suggests that the alloy is indeed a eutectic alloy. If it were a single peak, it would indicate that the alloy melts through a eutectic reaction. However, a closer inspection of the peak using expanded scales suggests the possibility of multiple reactions. Notice that there exists a small plateau right after the major peak at the marked position in Fig. 3.5c. Also noticeable is the curvature change near 218.7 °C (Fig. 3.5b). These results suggest that the peak might be a result of combining several closely spaced peaks. Also, close inspection of the DSC result suggests that those peaks begin at 217, 218.7, and 221.9 °C, respectively. Holding the sample at 219.5 and 218 °C, therefore, would result in a preferential growth of the first primary and second primary phases.

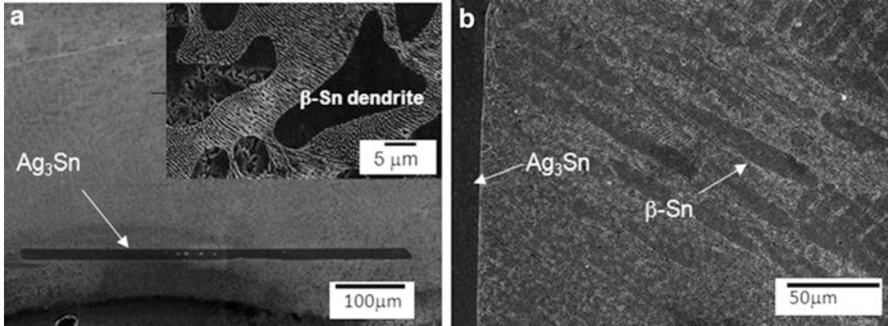


Fig. 3.6 SEM micrographs showing the microstructure of Sn-3.8Ag-0.7Cu solder alloys after 1,000 min holding at 219.5 (**a**) and 218 °C (**b**). After 1,000 min of holding at each temperatures, these samples were quenched to induce rapid cooling. The inset image shown in (**a**), which was quenched from 250 °C, and the microstructure of the solder matrix outside of the large Ag_3Sn precipitate, shows evidence of Sn-dendrite and ternary eutectic phase

Figure 3.6a presents the microstructure of a differentially cooled sample with a holding treatment at 219.5°C for 1,000 min. Note the presence of a rod-shaped Ag_3Sn phase with an abnormal size of a few millimeters. This result alone proves that the alloy is not a eutectic and that Ag_3Sn is the first primary phase of the alloy. The inset in this figure shows the quenched microstructure of the same alloy after holding at 250 °C. The presence of β-Sn dendrites can easily be taken as evidence that β-Sn is the first primary phase. As evidenced by differential cooling, such an interpretation is not correct. The formation of β-Sn dendrites should be attributed to the result of nonequilibrium cooling. Figure 3.6b shows the microstructure of the same alloy after 1,000 min holding at 218 °C, which is in between 217.3 and 218.7 °C. This is the temperature where the second primary phase should develop, and Fig. 3.6b suggests that it is β-Sn. This β-Sn is a pro-eutectic phase of ($Ag_3Sn+\beta$-Sn) binary system. This result suggests that the first primary phase is $(Ag_3Sn)_P$ and the second primary is $(\beta\text{-Sn})_P$, consistent with the prediction made in the phase field diagram in Fig. 3.3. It is not clear whether the binary eutectic reaction for $E(Ag_3Sn+\beta\text{-Sn})_P$ occurs in this alloy. With the composition being close to the ternary eutectic, it is likely that a small amount of the reaction for $E(Ag_3Sn+\beta\text{-Sn})_P$ reaction happens, but if it did, its fraction would be negligibly small to be visible in the microstructure.

The SEM micrographs shown in Figs. 3.7 and 3.8 present the results of differential cooling experiments conducted on Sn-4.7Ag-1.7Cu (Fig. 3.7) and Sn-3.0Ag-0.5Cu (Fig. 3.8). It can be seen that the first primary phase of Sn-4.7Ag-1.7Cu is Cu_6Sn_5, while the second primary is Ag_3Sn. On the other hand, Fig. 3.8 shows that the first and the second primary phases for Sn-3.0Ag-0.5Cu are β-Sn and Ag_3Sn, respectively. These results are also in agreement with the phase field diagram in Fig. 3.3. Note that two overgrown Ag_3Sn plates shown in Fig. 3.8b are in coexistence with β-Sn. This large β-Sn phase is situated in between two parallel Ag_3Sn plates, which may be the result of the (β-Sn$+Ag_3Sn$) binary eutectic reaction that occurred above the eutectic temperature. Again, this result is in excellent agreement with the microstructure prediction based on the phase equilibria of the alloy.

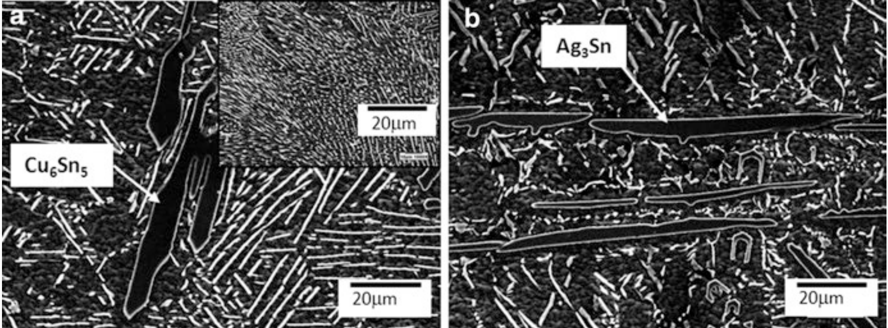


Fig. 3.7 SEM micrographs showing the microstructure of Sn-4.7Ag-1.7Cu solder alloys after 1,000 min holding at 262 (**a**) and 225 °C (**b**). The inset image shown in (**a**) shows the typical microstructure of the solder microstructure when the alloy quenched from 250 °C without holding treatment

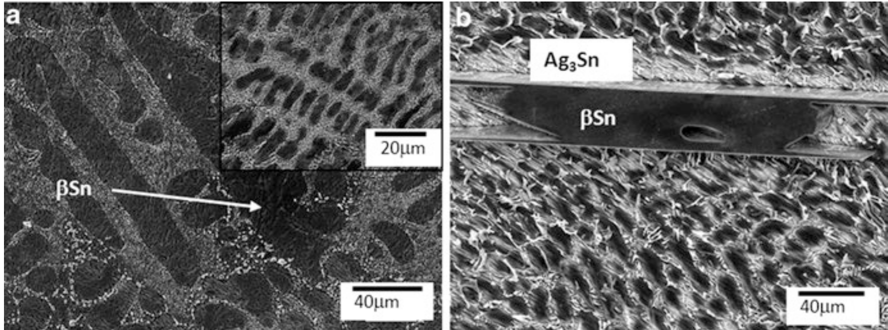


Fig. 3.8 SEM micrographs showing the microstructure of Sn-3.0Ag-0.5Cu solder alloys after 1,000 min holding at 220 (**a**) and 218 °C (**b**). The inset image shown in (**a**) shows the typical microstructure of the alloy that was cooled from 250 °C without holding treatment. In (**b**), primary beta Sn is enclosed between two thin Ag_3Sn plates

Microstructure with Undercooling

The cooling rate used in a solder joint reflow process is a few degrees per minute, which is too fast for SAC solder alloys to maintain ideal phase equilibria during solidification. This highly nonequilibrium cooling process can result in a solder microstructure that is substantially different from that expected from the phase diagram. Nonequilibrium cooling affects the solder microstructure because it introduces undercooling effects into the solidification process [16–23]. In order for a solid embryo to form, liquid must be cooled below its solidification temperature to attain sufficient free energy for solidification to overcome the interface energy required for creation of the liquid–solid interface. The influence of undercooling on solidification is complex and is not fully understood. There are many different ways that undercooling affects the phase equilibria, the solidification sequence, and thus

the final microstructure. It can expand one or both primary phase fields by lowering the eutectic temperature, which also changes the composition for the eutectic reaction. In an extreme case, either the primary reaction sequence is switched or one of two primary reactions is suppressed. All of these depend on which phase requires more undercooling to solidify. There are three solid phases in a ternary eutectic system, and they generally don't have the same interfacial energy. When any of these phases has far higher interfacial energy than the others or is more uncooling prone, this phase will dictate the whole solidification sequence that results in microstructures where the phase fraction and the type of phases are different from the phase diagram, and hence, metastable. Surprisingly, SAC solder alloys appear to behave in this way due to difficulty in nucleating the β-Sn phase.

The degree of undercooling in SAC alloys depends highly on many factors including size and purity of the melt, cooling rate, and substrate types, because they all affect the nucleation process. Because of this, it is difficult to generalize the influence of undercooling on the solder joint microstructure. In fact, the influence of undercooling on the SAC microstructure is not very well understood. Further detail on its influence on solder joint microstructure is presented in Chap. 4 with an emphasis on experimental observations. A brief yet excellent review on undercooling effect on solder joint microstructure is also available in a paper published by Borgesen et al. [21]. Thus, our purpose here is to bring a general understanding of its role by considering a few typical scenarios and the related phase equilibria of SAC system.

Typically, 20–30 °C of undercooling is reported in SAC solder alloys during reflow process [17, 22]. Considering their low melting temperature, undercooling in excess of 20 °C is unusually high. Such an extreme level of undercooling in SAC alloys is generally attributed to the difficulty of forming a stable β-Sn nucleus. Evidence for β-Sn dictating the undercooling may be seen from the DSC result shown in Fig. 3.9, where the 5 °C/min cooling scan curve of Sn-3.8Ag-0.7Cu is shown (the heating scan result of the same alloy is shown in Fig. 3.5). According to Fig. 3.5, the alloy is supposed to form the $(Ag_3Sn)_P$ at 221.9, $(\beta\text{-Sn})_P$ at 218.7, and ternary eutectic at 217.3 °C. The corresponding reaction temperature measured during cooling run is found to be ~217 for $(Ag_3Sn)_P$, ~205.7 for $(\beta\text{-Sn})_P$, and 205.5 °C for the ternary eutectic. The undercooling for $(Ag_3Sn)_P$ formation is ~5 °C, while it is in excess of 12 °C for both $(\beta\text{-Sn})_P$ and the ternary eutectic. This means that the $(Ag_3Sn)_P$ phase requires less undercooling than $(\beta\text{-Sn})_P$ and the ternary eutectic microstructure. The phase common to the $(\beta\text{-Sn})_P$ and the ternary eutectic microstructure is β-Sn, indicating that β-Sn is the phase that controls the second primary and ternary eutectic reactions. The eutectic reaction has to occur with compositional coordination among constitutional phases. If one phase does not form due to the undercooling requirement, then the other phase or phases cannot form in the eutectic reaction. This is the reason why both the second primary and ternary eutectic reactions are suppressed until undercooling exceeds 12 °C. It also explains why the temperature separation between the second primary and the ternary eutectic reaction is in such a close proximity, less than 1 °C, which is evident in the ~205 °C peak in Fig. 3.9a. Close inspection shows that it consists of two peaks, but an arrow

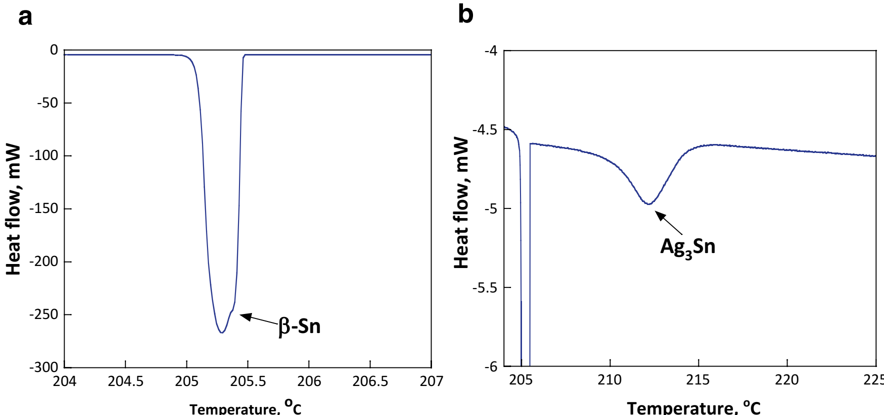


Fig. 3.9 Plots showing a DSC result of Sn-3.8Ag-0.7Cu (alloy 3 in Table 3.2). The data are taken from the cooling run with a rate of 5 °C/min. Comparison to the result shown in Fig. 3.3, which is from the heating run of the same alloy, shows the occurrence of super cooling to a significant level and change in fraction of the 1st and 2nd primary phase. The peak near at 205 °C (**a**) appears to show a single peak but as indicated with an arrow there exists a change in peak curvature. It means that the 205 °C peak consists of two peaks, and the peak intensity of these two peaks is almost comparable. On the other hand, the undercooling for (Ag_3Sn)p reaction is found to be ~5C (**b**). Non-equilibrium cooling clearly increases the fraction of the primary phases

identifies a point where the curvature of the peak changes. Deconvolution of the peak indicates that these two peaks are separated by very small difference in temperature. Figure 3.9 also shows that the phase fraction in the final microstructure can be significantly altered by undercooling. Note that the peaks for $(Ag_3Sn)_P$ and $(\beta\text{-Sn})_P$ melting (Fig. 3.5) is almost absent, but their solidification produces the noticeably intense peaks. Because the peak intensity represents the reaction amount, an increase means more reaction energy for $(Ag_3Sn)_P$ and $(\beta\text{-Sn})_P$ formation than the phase equilibrium demands. The SEM micrograph in the inset of Fig. 3.6a shows such a microstructure with a large volume fraction of β-Sn dendrite. While it is not visible in the micrograph, large $(Ag_3Sn)_P$ rods are found in other areas. Since this alloy was quenched from the melt at 250 °C, it was subjected to an extreme level of undercooling. This led to microstructure containing abnormally large amount of β-Sn dendrite as well as $(Ag_3Sn)_P$ even if the alloy composition is near the ternary eutectic. Borgesen et al. analyzed the effect of undercooling on the phase type and fraction of SAC alloy microstructure using the case of the Sn-3.9Ag-0.6Cu alloy and a 3D phase diagram displaying liquidus surfaces of β-Sn, Cu_6Sn_5, and Ag_3Sn as a function of temperature and composition. The 3D phase diagram they used is presented in Fig. 3.10. In this plot, the liquidus surfaces for β-Sn, Cu_6Sn_5, and Ag_3Sn are extrapolated below the eutectic temperature to consider effects of undercooling. The red trajectory superimposed on the liquidus surfaces represents the change in composition and temperature of the liquid under equilibrium cooling. The white trajectory represents the case of more realistic cooling where a sizable degree of undercooling occurs during the solidification process.

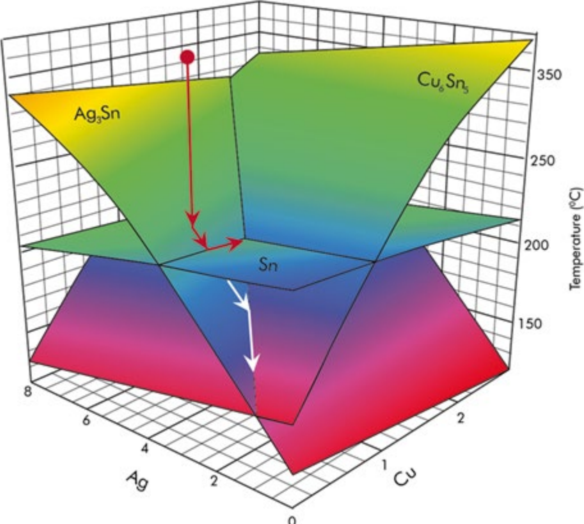


Fig. 3.10 A 3D phase diagram showing the liquid surface projection of Sn-rich side Sn–Ag–Cu ternary system published by Borgesen et al. To reflect the undercooling effect, liquidus surfaces of Sn, Ag_3Sn, and Cu_6Sn_5 are extrapolated below the equilibrium. The *red* (equilibrium) *trajectory* follows the compositional and temperature trajectory of Sn-3.9Ag-0.6Cu alloy when the solidification proceeds without undercooling, while the *white trajectory* corresponds to the case with a sizable undercooling (This diagram is reconstructed from the plot used in Lehman et al. [21])

The alloy composition considered in the plot is very close to the alloy in Fig. 3.6. As shown in the equilibrium red trajectory, the liquid composition of the alloy follows the Ag_3Sn liquidus surface and moves toward the binary eutectic liquidus line where the liquid is at equilibrium with ($Ag_3Sn + \beta$-Sn) binary eutectic. The compositional shift toward this monovariant liquidus line continues by Ag_3Sn solidification, followed by the pro-eutectic *β-Sn* solidification as a part of the second primary reaction. The liquid composition eventually reaches and follows that of binary ($Ag_3Sn + \beta$-Sn) eutectic liquid until the ternary eutectic reaction. When undercooling exists, however, the liquid composition continues to follow the Ag_3Sn liquidus surface because the undercooling requirement for β-Sn lowers the subsequent reaction temperatures. This makes the liquid to be enriched with Sn because continued growth of Ag_3Sn drains Ag as indicated by the white trajectory. This trajectory suggests that the liquid composition reaches and eventually follows the composition of the ($Cu_6Sn_5 + Ag_3Sn$) binary eutectic prior to ternary eutectic reaction. If the solidification occurs in this manner, the microstructure of the alloy will contain a (Cu_6Sn_5+ Ag_3Sn) eutectic microstructure. However, this is not the only likely solidification scenario. Alternatively, the liquid composition could change its direction and move toward the ternary eutectic point along a suppressed (undercooled) Sn

surface (not shown) before it reaches the ($Ag_3Sn + \beta$-Sn) binary eutectic liquidus line. This could occur because Sn enrichment in the liquid may force nucleation of pro-eutectic (binary) β-Sn dendrites through the second primary reaction. The removal of Sn from the liquid restores compositional balance in the melt, making its composition move toward the ternary eutectic point (which is at a different composition in the undercooled state) along the Ag_3Sn-Sn liquidus intersection. This is the path that disturbs the phase equilibrium the least under the condition of undercooling. In fact, this path is consistent with the microstructure of the quenched alloy (inset of Fig. 3.6a).

The effect of undercooling on other SAC alloy microstructures can be understood using similar considerations of the phase equilibria. In the case when Cu_6Sn_5 is the first primary and β-Sn is the second primary phase, the microstructure will be similar to what is discussed above except that Ag_3Sn is replaced with Cu_6Sn_5. When both the first and second primary phases are IMC phases, the microstructure will be a simple combination of large IMC phases and the ternary eutectic. The Ag_3Sn and Cu_6Sn_5 phases require a lesser degree of undercooling (and, hence, have a lower interfacial energy) so that the first and second IMC phases will solidify with little disturbance of the phase equilibria. Suppression of the ternary eutectic reaction by undercooling provides those phases with time to grow. Therefore, the resulting microstructure would be more or less similar to what the phase diagram predicts but IMCs could be abnormally large; this is often observed with the presence of large tubular Cu_6Sn_5 precipitates when the solder is enriched in Cu due to dissolution of the Cu substrate.

Alloys with β-Sn as the primary phase (such as SAC305 and SAC 105) are a more complex case, and the microstructure is not simple to predict. With β-Sn dictating the undercooling, there is a possibility that β-Sn formation is delayed to a degree where the IMC phase solidifies first. Whether this occurs or not in reality will depend on the degree of uncooling required for given alloy, which is affected by various factors including the cooling rate. When the undercooling requirement is mild, then the solidification path would follow the same sequence suggested by the phase diagram. Solidification will proceed with the formation of the β-Sn dendrite, the IMC phase, and/or the (IMC + β-Sn) eutectic, and then the ternary eutectic. The phase fraction may not differ much from that for equilibrium because the IMC and the ternary eutectic should form almost as soon as β-Sn growth occurs. Also, the IMC phases formed as a part of the second primary reaction is likely to be tiny due to lack of time for their growth for the same reason. This may be a common microstructure for SAC solder joints as their cooling rate, and thus the degree of undercooling is moderate. On the other hand, in the case when the IMC phase precipitates first, due to a fast cooling rate, for example, the resulting microstructure is impossible to predict because a variety of different solidification paths are possible depending on the location of the alloy composition in the phase field diagram and the degree of uncooling. In the most complex cases, the microstructure will contain an unexpected IMC primary phase. Therefore, this is the condition that demands more studies.

Contamination, Microalloying, and Microstructure

Solder joints in electronic devices are bound to be contaminated with foreign elements. The word "contamination" is used here to distinguish the intentional alloying elements from the unintentionally introduced elements during soldering process. In fact, some of the "contaminants" considered here are often introduced to the solder for alloying purposes. Regardless of their origin, inclusion of such elements in the SAC solder alloy can alter the phase equilibria and the joint microstructure. In prior solder technology, whether Pb-free or not, the contamination effect was not a subject of serious concern and usually ignored. It was reasonably safe to do so because the total volume of solder in the joint was too large compared to a small amount of contaminants to significantly affect the microstructure and properties of solder joint. Unfortunately, miniaturization reduces the volume of solder, so more modern and future solder interconnects are much more sensitive to such effects. For example, contaminants in microbumps can become a major constituent of the alloy and substantially alter its microstructure and properties. The importance of understanding contamination effects will only increase in the future with the continuing thrust toward miniaturization of electronic devices and their packaging infrastructure.

There are several common contaminants in solder joints. They can originate from the flux and chemicals used during the reflow process, but the major source is the metallization layer. Since the purpose of soldering is to join two metallization layers, solder alloys are always subjected to contamination by the interfacial reaction [23–27, 29, 32]. While Cu is the most common metallization layer, since it can be deposited from aqueous solutions, other elements can enter into the solder. These elements include Ni, Au, Pd, Pb, and Sn [23–42]. A metallization layer coated with Pb and Sn used to be very popular as they are cheap yet provide reasonably robust protection against oxidation. With Pb-free technology, their use, especially Pb, is declining and will eventually be removed from the list. However, there still exist a number of devices with those layers in the market. Until complete exhaustion of those devices, the concern on Pb and Sn contamination will continue. Also, the Cu metallization layer itself may not be contamination-free. The lead frame is not made of pure Cu but is alloyed with a small amount of Co and Fe. When solder reacts with the lead frame, those elements react together with solder. Therefore, the elements under consideration in relation to contamination issue should include at least Cu, Sn, Ni, Pd, Au, Fe, Co, and Pb. Among these, the effect of Cu and Sn on the phase equilibria is simple to analyze because they are constituents of SAC alloys. Their addition only changes the composition of the SAC alloy in the joint, and the change in the microstructure can be determined by using the phase field diagram shown in Fig. 3.3. One possible complication in this case is that the interface reaction also drains the constituents of SAC alloys. For example, Cu_6Sn_5 growth at the Cu interface occurs by consuming Sn in SAC alloys. Such influence should be included in the composition estimation. Hence, the problematic elements in terms of figuring out the change in phase equilibria are Ni, Pd, Au, Fe, Co, and Pb.

Clearly, some of these elements, most notably Ni, Pd and Co, are also considered to be alloying elements for SAC solder alloys as they are known to provide several benefits. Some of those benefits are discussed in Chaps. 5 and 6 in relation to the interface IMC structure and the mechanical properties of solder joints. The scope of this section is not to discuss how those elements change solder properties but to explain the possible change in the phase equilibria and microstructure resulting from inclusion of those elements in solder alloys. In this regard, whether they produce beneficial effect or not, all these elements will be treated as the contaminants.

The effect of the listed contaminants on the SAC alloy phase equilibria is quite complex to predict as it requires phase equilibrium consideration on quaternary alloy systems and beyond. At the present moment, while quaternary phase diagrams with some of the listed elements are actively investigated, our understanding is still limited so that we can't describe their effect with confidence. Nevertheless, by extending the understanding made in the phase equilibria of SAC system and with a help of limited but existing results in the field, we can arrive at some generalizations. At the minimum, it would be possible to predict the direction of change in the phase equilibria and microstructure, which is attempted in this section. Three key factors must be identified in order to make a reasonably reliable prediction, and they are the (1) level of contamination, (2) element's affinity to metallization materials at interface, and (3) type of phase created by the element.

The level of contamination is an important factor because it determines whether the contaminant results in a major change in the phase equilibria or not. Strictly speaking, regardless of the amount, a quaternary phase system must be considered in order to make an accurate analysis. However, when the level of contamination is small, its influence on the phase equilibria can be negligibly small to a degree to treat the contaminated alloy as a ternary system. When the solubility of the contaminant in β-Sn phase is sizable, then this approach makes the most sense because the total phase fraction of β-Sn in SAC alloys is overwhelmingly large and effective in absorbing contaminant. Pb is the element that belongs to this category. The solubility of Pb in β-Sn is as high as ~2 % at binary (Pb–Sn) eutectic temperature, meaning that SAC alloys can take considerable amount of Pb before creating a new phase field. Therefore, when the level of Pb is low, SAC solder alloys can be treated as ternary system with a minor change in the melting temperature in so far as microstructure is concerned.

For other elements, namely, Ni, Au, Pd, Fe, and Co, the solubility in β-Sn is fairly low. For Ni, Au, and Pd, there is an anticipation that Ag_3Sn and Cu_6Sn_5 can absorb them as β-Sn does for Pb because the binary phase diagram for these elements with either Cu or Ag shows complete mutual solubility at high temperature. However, experimental observations indicate that such an effect does not exist, as evident in Figs. 3.11 and 3.12. The sample used for Fig. 3.11 was made by mixing Sn-4.7Ag-1.7Cu with 2.5 wt.% Ni (in reference to the total weight of the sample) followed by a slow cooling from 250 °C. Because a large quantity of Ni that was added to the alloy produces all possible IMC phases, the phase equilibria and thus the microstructure of the sample changed somewhat from the original SAC alloy. These micrographs show that Ni is present where Cu-_bearing IMCs exist. X-ray diffraction

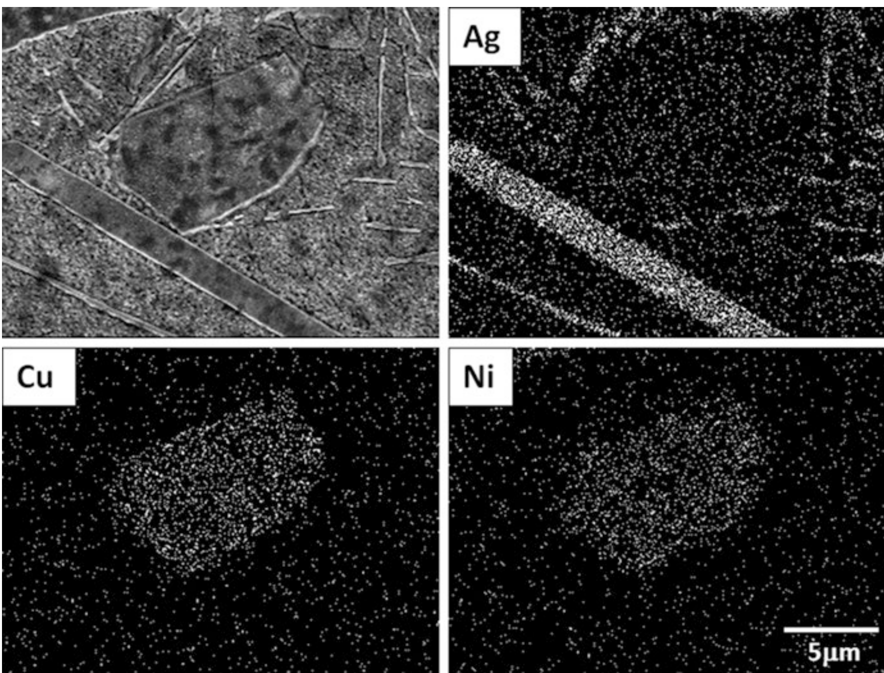


Fig. 3.11 SEM micrographs displaying the microstructure of the Sn-3.8Ag-0.7Cu with an addition of 2.5wt. Ni in reference to the total weight of the sample. This sample was prepared by mixing the alloy at 500 °C followed by a slow cooling to 250 °C and subsequent cooling to room temperature, The Ni rich phase is determined to be $(CuNi)_4Sn_4$

analysis of the alloy revealed that the Cu-bearing phase has the same structure to Ni_3Sn_4, meaning that Ni_3Sn_4 forms by absorbing Cu in its structure. Also, Ni was not present in either Cu_6Sn_5 nor Cu_3Sn, even at low amounts. Because Ni is observed in Cu_6Sn_5 phases (see discussion in Chaps. 4 and 5) apparently the Ni exceeded the capacity to be absorbed in Cu_6Sn_5 and instead, it formed a Ni-based IMC phase with Cu absorbed. Also noticeable is the absence of Ni in regions with the Ag_3Sn phase, indicating that the solubility of Ni in other phases in SAC alloys is negligibly small, at least below the limit of its detection using EDX (electron energy dispersive x-ray spectroscopy). Figure 3.12 shows the microstructure of the same alloy but mixed with 1 wt% Pd. Note that Pd is absent in places where Ag_3Sn and Cu_6Sn_5 phases exist. According to the result, the solubility of Pd is small in Cu_6Sn and Ag_3Sn, and it forms its own IMC phase that was found to be $PdSn_4$. The alloy mixed with Au showed a similar behavior, that is, to form $AuSn_4$ IMC phase with negligible dissolution in Cu_6Sn and Ag_3Sn. Therefore, it is fair to assume that a small amount of Ni, Pd, and Au added to SAC alloys would change their phase equilibria by introducing a new phase field.

In the case of Co and Fe, having HCP and BCC crystal structure, their solubility in β-Sn, Ag_3Sn, and Cu_6Sn_5 is extremely low, a few thousand ppm at best, such that

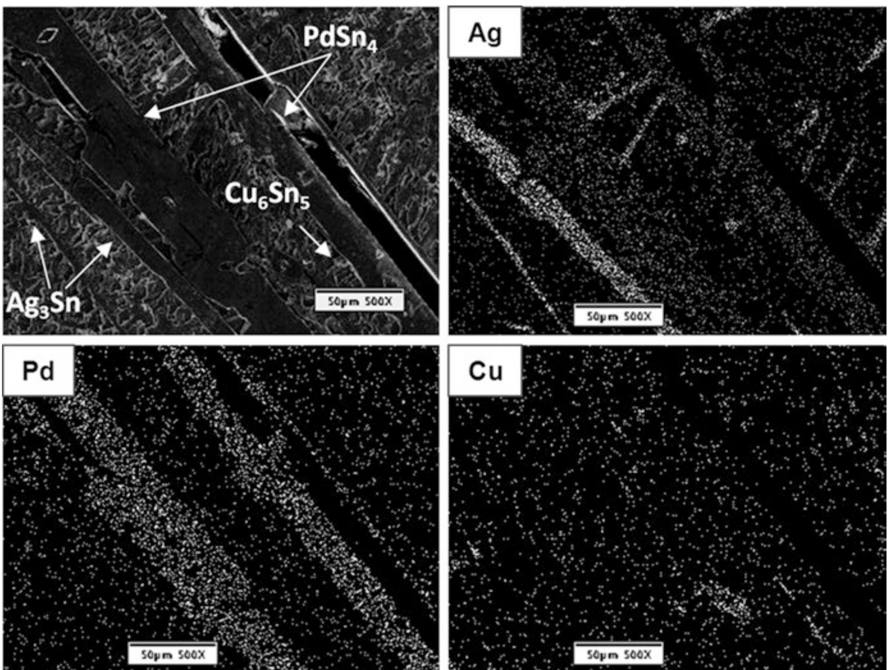


Fig. 3.12 SEM micrographs displaying the microstructure of the Sn-3.8Ag-0.7Cu with an addition of 1.5 wt. Ni in reference to the total weight of the sample. This sample was prepared by mixing the alloy at 500 °C followed by a slow cooling to 250 °C and subsequent cooling to room temperature, The Pd rich phase is determined to be $PdSn_4$

creation of new phase field is anticipated regardless of the added amount. Fortunately, they are already in low concentration in the Cu lead frame, and therefore the level of contamination in SAC alloys is likely to be close to their solubility limit in phases present in SAC alloys. Therefore, unless they are intentionally added to SAC alloys to a sizable amount, their effect on the phase equilibria of SAC solder alloys can be safely assumed to be small. However, this doesn't mean that the microstructure of SAC solder would not be changed. Due to their low solubility, even a minute amount addition by solder reacting with the lead frame can produce Fe–Sn ($FeSn_2$) and Co–Sn ($CoSn_2$) IMC phases. They must be small in size because low level of concentration prevents growth but large in population because their high melting temperature (above 500 °C) prevents their coarsening or dissolution in solder melt. The large quantity of microscopic IMC phases dispersed in liquid can act as nucleation sites for solid phases in SAC alloys during solidification. Hence, their presence may refine the solder microstructure, which may be one of the reasons why they are being considered as microalloying elements for improving mechanical properties of solder joints.

The second factor to consider in terms of evaluating the contamination effect is the contaminant's affinity to the adjoining metal substrate that is mostly Cu and Ni. On one hand, this factor affects the contamination level in SAC alloys, but on the

Table 3.2 A list showing IMC phases that were found to present in bulk of SAC and Cu interface when the Sn-3.8Ag-0.7Cu alloyed was alloyed with 1 wt.% of listed elements

Element	Solder IMC phases	Cu Interface IMC
Au	$AuSn_2$, $AuSn_4$	$(CuAu)_6Sn_5$
Ni	$(CuNi)_3Sn_4$	$(CuNi)_6Sn_5$
Co	$CoSn_2$	$(CuCo)_6Sn_5$
Fe	$FeSn_2$	$(CuFe)_6Sn_5$
Pb	No IMC	Cu_6Sn_5
Pd	$PdSn_4$	Cu_6Sn_5

This characterization was done after reacting the solder with Cu on PCB at 250 °C

other hand, it can affect the microstructure of interfacial IMC phases. In the case when the contaminant has a strong affinity to solder, the whole amount added to the melt would stay in the SAC alloys and take part in the solidification process. In the opposite situation where the contaminant reacts with interfacial IMC layers, a good portion of them would be drained away from SAC alloys and return back to the interface. In that case, the actual amount of contaminant remaining in SAC alloy is lower than the anticipated. Elements having preference to reside in the interface are Au, Ni, Co, and Fe. Table 3.2 lists experimentally observed IMC phases in bulk SAC alloy and its interface with Cu substrate with addition of these elements to Sn-3.8Ag-0.7Cu. Note that Au, Ni, Co, and Fe can be absorbed in Cu_6Sn_5 IMC at interface, while Pb and Pd were not. This means that the former gradually returns back to solder/Cu interface by taking part in the growth of interfacial IMC. The latter prefers to stay in SAC alloys probably because of extremely low solubility in interfacial IMC or low reactivity with Cu. Evidence that strongly suggests the preference of Au, Ni, Co, and Fe in interfacial IMC can be seen in micrographs shown in Fig. 3.13, where SEM images of the interface IMC layer seen from the top (after etching of the SAC solder) and in cross section. The interfacial Cu_6Sn_5 IMC has strikingly different forms depending on the presence or absence of Au in SAC alloys. In the SAC alloy, the observed interface IMC has scallop-shaped IMC, but with 1 wt.% Au the IMC grows more evenly without creating the scallop shapes. Also, Sn was present in the middle of IMC layer as dispersed islands. The mechanism for IMC shape change, which also traps Sn during its growth, is not well understood and is beyond the scope of this section. However, it clearly shows that Au becomes an active part of interfacial IMC growth mechanism, and in doing so, Au is removed from SAC alloys. The IMC layers formed with other contaminants, Ni, Fe and Co, also show the similar IMC growth pattern. The formation of such interfacial IMC layers may be the reason why some of these elements are found to improve aging-induced embitterment of solder joint, including resistance against the fatigue, and shock-induced interface fracture, which is discussed further in Chaps. 5 and 6.

Table 3.1 contains one interesting yet mysterious result, that is, elements showing good solubility in interface IMCs are not necessarily soluble in the same Cu_6Sn_5

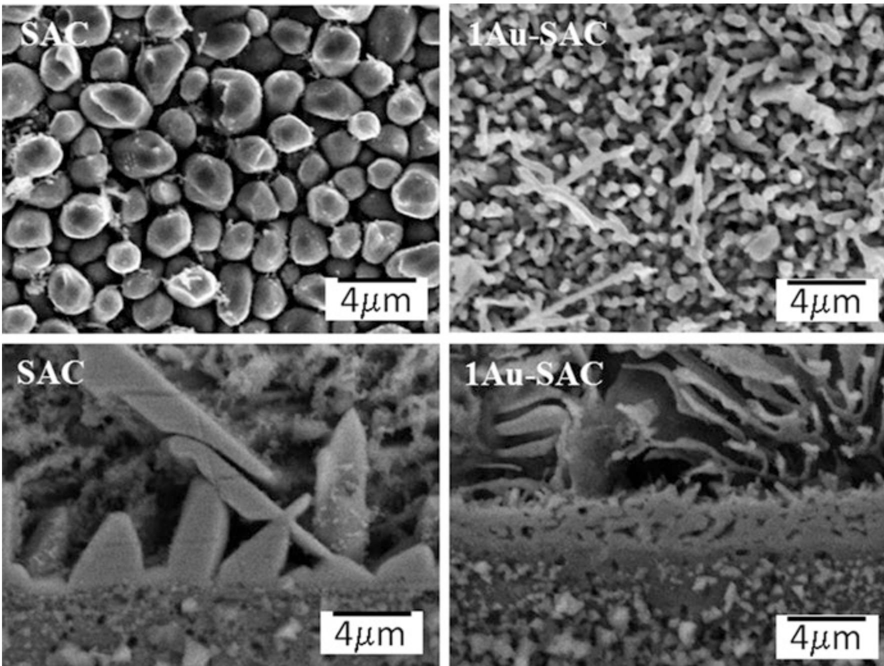


Fig. 3.13 SEM micrographs comparing IMC phase formed at Cu/SA solder interface with and without addition of Au. The *top micrographs* are the *top view* of the interface IMC, obtained after removal of Sn, while *bottom micrographs* are the cross-sectional view of the Cu/solder interface. The alloy used for this characterization was Sn-4.7Ag-1.7Cu with an addition of 1 wt.% Au. The reflow process for soldering was conducted at 250 °C

phase in the bulk. For example, Au was found to dissolve well into Cu_6Sn_5 interfacial layer, forming $(CuAu)_6Sn_5$, yet it did not show such solubility away from the interface. The Au-bearing phase in the bulk SAC solder was found to be $AuSn_4$ and $AuSn_2$, not Cu_6Sn_5. The same was found to be true for Ni, Fe, and Co. Presently, it is not clear what makes Cu_6Sn_5 IMC to interact with these elements so differently at interface. One probable cause of such difference may be found from the temperature where Cu_6Sn_5 phase forms. Interfacial Cu_6Sn_5 IMC formed mostly at the reflow temperature of 250 °C, while the formation temperature of the same IMC within the solder should have been well below ~220 °C, the melting temperature of the alloy. With the high temperature as well as a strong preference to react with Cu, these elements may be easily incorporated into the Cu_6Sn_5 at interface. On other hand, significantly lower formation temperature of Cu_6Sn_5 in SAC alloys, taking undercooling into account, prohibited it from accommodating those elements into its structure. Furthermore, and perhaps more critically, the melting temperatures of Sn bearing IMC phases with those elements, namely, Ni_3Sn_4, $AuSn_4$, $FeSn_2$, and $CoFe_2$, are relatively higher than typical SAC IMC phases. Consequently, the additional liquid–solid equilibrium phase field created by these IMC phases is likely to exist at higher

temperature. This would result in the solidification of those IMC phases prior to Cu_6Sn_5, limiting incorporating of those elements into Cu_6Sn_5. This may explain why the Ni addition creates $(NiCu)_3Sn_4$ in the SAC alloy, rather than creating $(CuNi)_6Sn_5$, because if Ni_3Sn_4 was the phase formed at higher temperature, it would form while taking Cu into its structure with its high solubility to Cu.

The type of phase that the contaminant produces when added to SAC alloys is related to the degree that it exceeds its solubility limit in Sn or alloy IMCs, because this determines the number and type of new phase fields to consider in the contaminated system. This is quite complex and a challenging topic to discuss because there are a number of factors to consider. However, if we keep the same boundary condition as above, that is, the low level of contamination, fairly reasonable and simple predictions can be made. The first is to determine if the addition of the contamination element creates a ternary compound with SAC alloys. Available database for compounds combined with experimental observations in the field suggests that none of the elements forms a ternary compound with any binary combination of Sn, Ag, and Cu at least at the Sn-rich corner of the alloy. This eliminates the need for considering the ternary or quaternary compound phase field. If no ternary compound exists, then the next step is to find the type of possible phases with the contaminant at Sn-rich side. Such phases can be found from binary phase diagrams consisting of the contaminant and Sn. According to the binary phase diagram, Pb exists as Pb, and Ni resides in Ni_3Sn_4, Au in $AuSn_4$, Pd in $PdSn_4$, Fe in $FeSn_2$, and Co in $CoSn_2$. Then it must be determined if a quaternary eutectic reaction is possible when these phases are added to the SAC alloy systems. In order for four phases to form a eutectic system, all binary combinations of the four phases are desirably eutectic systems. Of these elements, Pb can form a quaternary eutectic system, because Pb–Sn, Pb–Cu, and Pb–Ag are all eutectic systems. Therefore, it is likely that the addition of Pb (1) creates Pb-bearing liquid phase field and (2) makes a liquidus surface in the alloy move toward a lower temperature. The addition of a new phase field occurs because there are four independent solid phases, Pb, Sn, Ag3Sn, and Cu_6Sn_5. Therefore, there will be four corresponding liquidus surfaces that meet at the quaternary eutectic reaction point. When we consider the low concentration limit of Pb, the composition of the quaternary alloy is likely to be at the pro-eutectic regime of the quaternary system along the Pb axis. Because of this, adding a small amount of Pb to SAC makes the melting temperature of the alloy to be lower than the uncontaminated. The solidification path would vary depending on the SAC alloy composition and Pb content, but it is likely that Pb formation occurs either as the second or third primary reaction if Pb content again is assumed to be at the low limit. Experimental exploration of the Pb effect made in Kim's internal research, a part of which is shown in Fig. 3.12, confirmed that Pb added to Sn-3.8Ag-0.7Cu indeed decreased the melting temperature and induced formation of the Pb phase at the third primary reaction, that is,

$$L + Cu_6Sn_5 + Ag_3Sn \rightarrow L + Cu_6Sn_5 + Ag_3Sn + Pb. \tag{3.7}$$

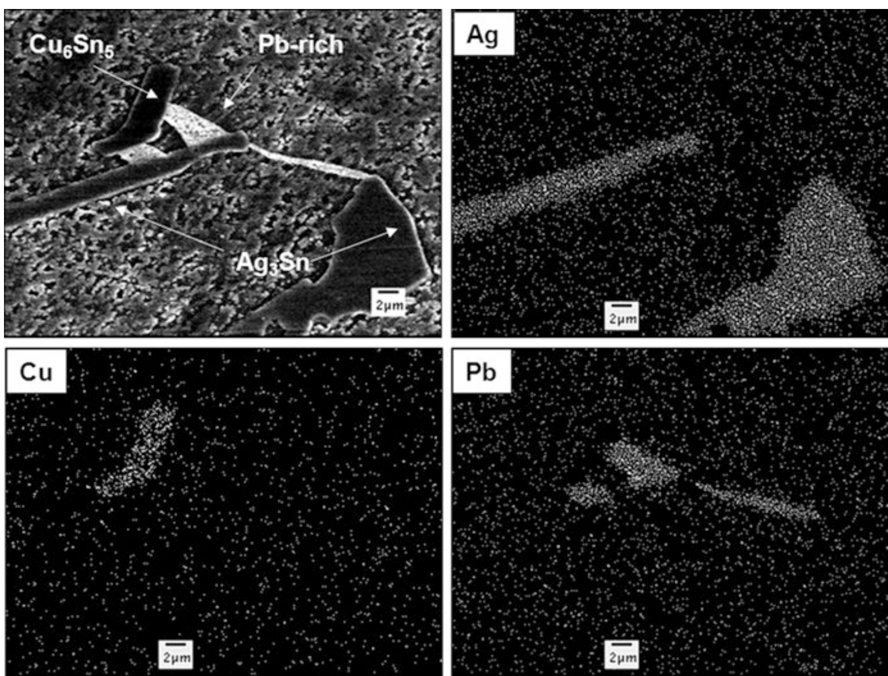


Fig. 3.14 SEM micrographs displaying the phases present in eutectic Sn-3.8Ag-0.7Cu alloy with an addition of 1.5wt. Pb. The sample was prepared by mixing the SAC alloy with Pb at 500 °C followed by slow cooling to 250 °C for holding and subsequent cooling to room temperature

As shown in SEM micrographs of Fig. 3.14 for Sn-4.7Ag-1.7Cu alloy with 1.5 % added Pb, Pb forms as a primary phase.

The next system to consider is the $AuSn_4$ and Ni_3Sn_4 phases because they are known to produce a ternary eutectic with Sn and Cu_6Sn_4. Huh et al. reported that $AuSn_4$ forms a ternary eutectic with Cu_6Sn_5 and Sn at 212 °C, $AuSn_4$, which is ~6 °C lower than the SAC eutectic temperature [35]. The composition for the eutectic is not well determined but is located at ~15%Au and ~2%Cu. The Ni effect on the SAC phase equilibria is somewhat controversial. There are conflicting reports about Ni forming ternary IMC phase with Sn and Cu, and also debated is if Ni_3Sn_4 forms a eutectic with Cu_6Sn_5 and Sn. According to the phase equilibrium study conducted by Duh et al. [29, 31] and also by Felberbaum et al. [33], it is likely that they form a ternary eutectic at the Sn-rich corner. Felberbaum suggests that the eutectic composition is probably at 0.7Cu and 0.03Ni, which is far closer to the Sn-rich corner than the SAC alloy. In this case, the change in phase equilibria can be tracked by considering the alloy as a system where two ternary eutectic systems are in competition. Since the eutectic temperature of Sn-$AuSn_4$-Cu_6Sn_5 is lower than that of SAC system and its composition is far away from Sn-rich corner, the addition of Au to SAC alloy is likely to decrease the liquidus temperature, while $AuSn_4$

becomes the part of the primary phase. In the Ni_3Sn_4-bearing eutectic, having its composition at far end of Sn corner, the Ag content in SAC alloys would dictate how the Ni addition affects the phase equilibria. In low-Ag SAC alloys, such as SAC101, the phase equilibria can quickly move to the SnCuNi ternary field with the addition of Ni. In that case, the SAC microstructure would consist of SnCuNi eutectic and Ag_3Sn as primary phase, which would generally lower the melting temperature of the alloy. For high Ag SAC alloys, the effect would be the opposite.

The final category is the element that doesn't form a ternary eutectic with any binary combination of phases in SAC alloys, and its IMC phase with Sn has a high melting temperature. These elements are Pd, Fe, and Co. Because all these phases have a high melting temperature, their inclusion will increase the liquidus temperature of the SAC alloys. Further, their phase field boundary is likely to be located at the first primary, meaning that they are the ones that should form first upon solidification. An example case is shown in Fig. 3.15, where a pseudo-binary SAC phase diagram is shown as a function of Pd weight percent when added to the Ag-3.8Ag-0.7Cu. It can be seen that the liquidus surface increases with Pd content, and the first field near the Ag-3.8Ag-0.7Cu corner is L + $PdSn_4$. Therefore, contamination with these elements would increase the melting temperature of the SAC alloys, and the resulting microstructure would contain the contamination-bearing IMCs as the first primary phase. Incidentally, all these elements are considered for alloying element for SAC alloys because they are reported to reduce undercooling and refine the

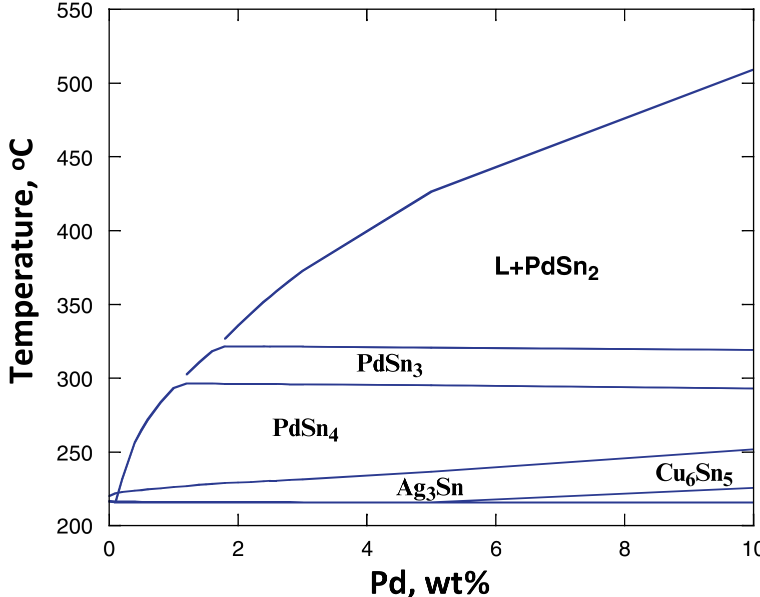


Fig. 3.15 A phase diagram showing the change in the phase field when Pd is added to Sn-4.7Ag-1.7Cu alloy. Note that there are multiple Pd–Sn IMC phases possible in the SAC alloy microstructure, and the liquidus temperature increases with Pd addition

microstructure of SAC solder joint. Such effect may result from their ability to form nuclei for SAC phases.

It is important to realize that the contamination effect described in this section is highly simplified and may lead to erroneous interpretation in some cases if not careful. The exact change in phase equilibria and microstructure with contamination needs much more careful and in-depth investigation of the quaternary phase system. Such studies are being extensively carried out in many laboratories [5, 6, 16, 28, 35–39, 42]. Because the underlying objective of those studies is to find potentially beneficial alloying elements, the list of element under research is extensive. The list includes not only the ones discussed in this section but also other elements such as Ge, In, Bi, and rare earth elements. Nevertheless, complexity in phase equilibria of quaternary system and beyond and inconsistencies among studies make the results difficult to use. The simplified view on the contamination effect discussed in this section may be helpful in properly understanding those results. Conversely, those results can be useful in gaining knowledge on specifics and thus reduce potential errors stemming from oversimplification. In doing so, one factor to be careful about is that contaminants are introduced during soldering, while alloy elements are present in SAC alloys from the beginning. The change in phase equilibria with contamination is dynamic and sensitive to process conditions. While lacking details, therefore, simplification made here should be useful as a way to make a quick assessment on the given situation because predictions made from it are reasonably accurate at least at the limit of low concentration.

Summary

In this chapter, we reviewed developing understanding about phase equilibria in the SAC alloy system by firstly inspecting the ternary eutectic and secondly off-eutectic alloy compositions. Understanding phase equilibria is important because it provides fundamental knowledge about how the microstructure of SAC alloys must evolve when the microstructure does not realize an equilibrium structure. The phase equilibria identify the ideal solidification path, but external factors such as the undercooling and contaminants cause deviation from the ideal path. Even under highly nonequilibrium process conditions, however, the driving force for restoring phase equilibrium persists, so the path for microstructural development is identified by equilibrium phase diagram. Minor changes, such as the phase fraction as well as fraction of eutectic microstructure, result from nonequilibrium solidification. In general, the solder microstructure is likely to reflect what phase diagram predicts unless the alloy is contaminated with foreign elements. A very brief summary chart is presented in Fig. 3.16.

With the help of the Bridgman growth technique, the eutectic composition and temperature for SAC alloys was determined with a high confidence, yielding 3.63Ag-0.85Cu at 217.3 °C, which is close to results from a few recent studies on the same system. It is further shown that the ideal eutectic microstructure consists

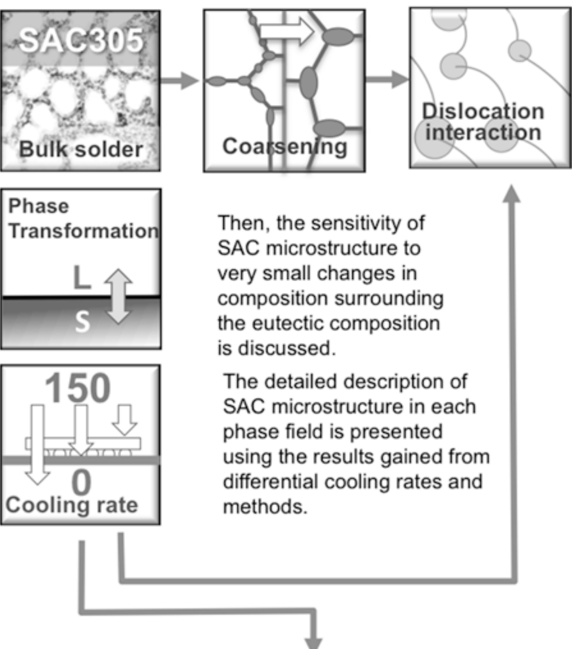


Fig. 3.16 Overall chapter three summary

of the β-Sn matrix, Ag_3Sn plates, and short Cu_6Sn_5 flat bar phases. With an overwhelming fraction of β-Sn in the eutectic microstructure, Ag_3Sn and Cu_6Sn_5 appear as embedded particles in β-Sn matrix. Nonetheless, the requirement for compositional coordination among phases in the eutectic structure makes them easily distinguished from the pro-eutectic primary phases.

In the case of off-eutectic compositions, the essential outcome of the phase equilibrium analysis was to show that there are six different phase fields for primary

phase formation, because there is a first primary and a second primary solidification phase. The six different fields exist because there are three solid phases to form and two reactions, i.e., the first and second primary, to occur prior to the eutectic reaction. As shown in Fig. 3.3, the six different fields have narrow composition ranges of Ag and Cu. This is the source of confusion and misinterpretation of SAC solder microstructures, particularly when the second primary reaction can include the binary eutectic reaction if the alloy composition is close to the binary eutectic monovariant liquidus composition. To resolve such complications, the "differential cooling" technique is effective, because it induces preferential growth of the targeted primary phase by storing the alloy at suspected temperature of reaction for extended period of time. Clearly, a combination of many experimental techniques is necessary to avoid misinterpretation of SAC alloy microstructures.

While the overall direction of the solidification path of given SAC alloy tends to follow what phase equilibria dictate, it can be derailed from its path by two major factors. The first is the substantial undercooling required to form β-Sn, and the other is the change in the phase field by contamination introduced during reflow process. Since β-Sn is the most prone to undercooling, it is the phase that controls the entire solidification process and thus dictates the final microstructure. This characteristic of Sn is especially dramatic when the second primary phase is β-Sn, because undercooling requires the second primary reaction and the eutectic reaction to occur at a temperature well below the eutectic.

The change in the phase equilibria due to the addition of contaminants from the reacting substrate with SAC solder is discussed to emphasize the possibility that SAC solder alloys are prone to the changes in phase equilibria and the resulting microstructure due to contaminants. Therefore it is important to consider this outcome in any microstructure analysis to reduce misinterpretation and to efficiently track the source of problematic features of microstructure.

It may seem that this tortuous journey to understanding solder joint microstructure might be over with the conclusion of this chapter. Sadly, it is far from the end, and it has just started. One decisive part of SAC microstructure affecting mechanical properties as well as other relevant properties of SAC solder joint is the grain structure. Here, we call it the "grain," while most metallurgists define differing orientation of eutectic microstructures as a "colony." Although it may appear odd, there is a good reason why the term "grain" is used in this book. In the case of SAC alloy, due to overwhelming phase fraction of β-Sn, β-Sn entirely surrounds the all-Ag3Sn and Cu_3Sn phases even in the eutectic microstructure. Therefore, the orientation of the β-Sn phase is responsible for the creation of microstructure (which could be described as having multiple colonies). The grain structure, especially its orientation, plays an important role in determining the joint resistance against various reliability failure mechanisms, from well-known fatigue failure to less well-known electromigration voiding. The grain structure in solder joints is often a single crystal or a multi-crystal and, in some cases, polycrystalline. The solder joint contains a few grains which are commonly not in a mixture of random orientations but in specific orientation relationships. Therefore, they can behave like a single crystal or as a multi-crystal, depending on how they are oriented with respect to imposed stress, thermal, or electrical fields.

The fact that β-Sn is a material with highly anisotropic properties that are explored in the next chapter makes the responses of solder to thermal, electrical, and mechanical loads to be surprisingly (or frustratingly) variable. There are multiple solder joints in a packaging structure, and the grain orientation of each joint differs. Therefore, many of the concerns about reliability failure mechanisms depend on how the failure mechanism interacts with the grain orientation, which implicitly varies with the joint location in the assembly. This is the very reason why process/reliability engineers in industry are constantly struggling with reliability issues whenever a new packaging design or process needs to be developed. It is therefore of utmost importance to understand how grain structure of solder develops in solder joints during the reflow process, what affects its development, and how it defines solder joint properties. This will start with discussion of the origins of β-Sn orientations in solder joints in Chap. 4, their influence on the thermal fatigue mechanism in Chap. 5, and their response to mechanical fatigue and shock resistance in Chap. 6.

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Chapter 4
Microstructure Development: Solidification and Isothermal Aging

The formation of a solder joint is described from initial solidification to aging effects. In the Sn–Ag–Cu alloy system, joints tend to form as either single crystals or tri-crystals that have twin interfaces that form a "beachball" orientation relationship of 60° sections about a common [100] axis. The effect of the anisotropic coefficient of thermal expansion and elastic modulus on microstructure development and initial states of internal stress as the joint solidifies and cools is examined. Due to this anisotropy, the grain orientations and the position of the joint in the package and the stress state and its evolution are unique for each joint. The local properties and microstructure of the joint are sensitive to minor alloying additions that can be introduced via the metallization layers on both the circuit board and the package. With isothermal aging, complexities arising from microalloying elements can be either beneficial or detrimental, and these issues are illustrated following Ni, P, and Pd microalloying elements to show that microalloying can be strategically used to manage and design both the solder and the interfacial properties.

The Beginning: The Initial Microstructure

Chapter three identified how sensitive solidification microstructures are to alloy composition and cooling rate, noting especially how forming a β-Sn nucleus often requires substantial undercooling. Additional complications arise from dissolution of interfacial metals into the melt, which introduce concentration gradients into the liquid solder. The composition of the liquid will depend on all that happens in the liquid during the minute or so of the reflow event. Because solder joints solidify in a nonequilibrium manner, the solidification process depends strongly on the concentration and temperature gradients just before solidification commences. The free surfaces associated with the shape of the joint provide an additional boundary condition that affects solidification of the joint. In addition, if there are large intermetallic phases present in the solder, it takes time for them to dissolve. If the IMC

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T.-K. Lee et al., *Fundamentals of Lead-Free Solder Interconnect Technology*,
DOI 10.1007/978-1-4614-9266-5_4

phases are not dissolved before solidification commences or if they form in the liquid before the tin starts to solidify, they can affect the solidification process and hence, the microstructure that develops. As long as there are no unmelted phases in the liquid solder prior to solidification in the reflow event, then any prior history before melting has minimal importance on the future microstructural evolution of the joint.

Given that the reflow process has a strong influence on the solidification process (especially the concentration and thermal gradients present in the liquid) [1–4], this will be the starting point for describing the evolution of the microstructure of a solder joint. In this chapter, the conditions that affect formation of the initial solidification microstructure will be the primary focus. As the solidification microstructure forms in a highly nonequilibrium manner, driving forces for continued changes remain in the microstructure. However, if the joint does not melt completely, the implications of this, as well as the potential for fabricating joints without complete melting (i.e., semisolid joint formation), will be discussed first.

Solid-State and Semisolid Joint Formation

While Sn-based solders are heavily used, there is a growing need for higher-temperature interconnection materials. One approach in making higher-temperature joints is to use solid-state diffusional (sintering) processes. An important area of current research involves the use of nanoscale particles to form a joint capable of high-temperature performance [5–7]. The nanoscale particle size has a high surface-to-volume energy ratio, and this surface energy is a form of stored free energy that can cause incipient melting far below the normal melting temperature. The surface energy is high enough to enable rapid sintering of nanoscale powders to form a structural joint once the temperature is high enough to initiate incipient melting, where the liquid greatly accelerates the sintering process. Once this starts, the transport distances are nanoscale in the interfacial liquid, so the formation of a nearly fully dense joint can happen in a short time at a temperature more than 100 °C below the equilibrium melting temperature. A major challenge with this approach is to keep the nanoscale powder from becoming oxidized prior to the sintering operation and to insure that protective coatings are removed. Subsequent remelting of joints made in this manner require heating to the normal melting temperature because the surface energy present in the nanoscale powder was used and dissipated to form the joint and is no longer available to lower the thermal energy needed to melt.

The approach just described is similar to a more general approach called transient liquid phase bonding or solid–liquid interdiffusion (TLPB, SLID) [8, 9]. This semisolid approach involves making a paste of powders that can form a low melting temperature eutectic composition at the interfaces (even though the overall composition can be far from the eutectic composition). Once the eutectic temperature is reached, the interfacial regions on the powder particle surfaces melt, and the liquid then spreads into the interfacial regions, partially dissolving the solids on either side

of the liquid. It is not necessary to fully melt the two phases in the powder, as long as there is enough liquid formed to facilitate mass transport to eliminate most of the porosity. When this process is well designed it is possible to have less shrinkage porosity than normal melting, because only a fraction of the material goes through the liquid to solid phase transformation [10]. It is important to decide whether a homogeneous composition is needed, as composition gradients generate a chemical potential that can affect further evolution of the microstructure in desirable (e.g., composition homogenization) or undesirable ways (e.g., galvanic potential that enhances corrosion).

Yet another approach to making a high-temperature interconnect is to start with a low melting temperature solder joint using a Sn-based solder to connect two copper substrates. With time and temperature, the Sn will be slowly consumed to make Cu_6Sn_5 and Cu_3Sn intermetallic phases. These two intermetallic phases have a much higher melting temperature than Sn, but they are not very ductile. This approach is most useful if the two copper pieces to be joined are not needed to mitigate differential thermal expansion requirements, so this strategy can be considered for joining components with the same expansion properties. However, if differential expansion needs to be accommodated, maintaining a softer solder joint may be necessary to prevent cracking of the joint or the components to be joined. Issues regarding consumption of Sn to form intermetallics, and thermal fatigue of Sn-based joints in settings where Sn is consumed by Cu will be discussed further in later sections.

Intrinsic Anisotropy of Sn

One of the most important fundamental issues with Sn-based solders was hidden from view in Sn–Pb alloys; Sn is one of the most anisotropic metals in the periodic table. The crystal structure of Sn is illustrated in Fig. 4.1, where its body-centered tetragonal structure shows a central atom with tetrahedral bonding to the atoms on

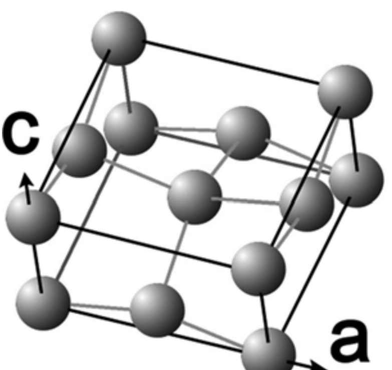

Fig. 4.1 Crystal structure of pure Sn (A5, tI4, space group 141, I41/amd) with lattice parameters a =5.8315 Å, c =3.1814 Å; c/a=0.5456

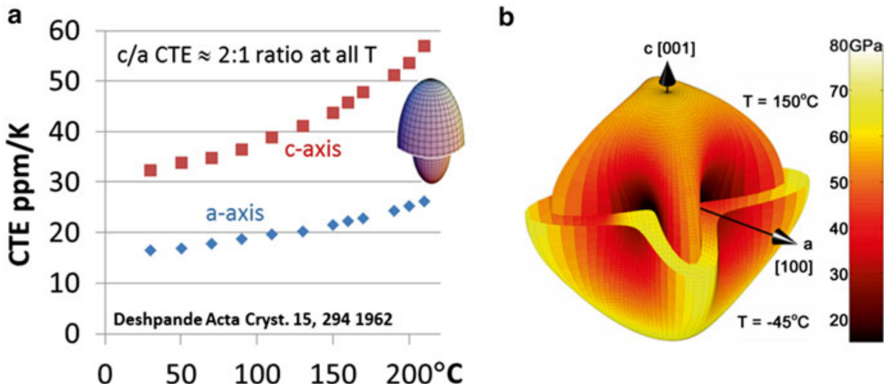

Fig. 4.2 (**a**) Temperature dependence of the coefficient of thermal expansion (CTE) with temperature in the directions the half- (*ellipses* show relative difference in CTE magnitude at 25 and 210 °C). (**b**) Anisotropy of Young's Modulus at −40 and 150 °C

the four faces. The Sn structure is essentially a squashed diamond cubic structure.[1] When Sn is combined with Pb, which is much softer than Sn and has more isotropic plastic properties, the Pb accommodates the anisotropic deformation of Sn. As Sn-based joints often form large or single-crystal joints, the anisotropic properties of Sn provide an important driving force for heterogeneous microstructural evolution, and hence the properties of solder joints evolve in a complex manner. Figure 4.2 and Table 4.1 illustrate and summarize the physical properties of Sn [11–13]. Of particular importance is the anisotropy of the coefficient of thermal expansion (CTE) plotted in Fig. 4.2a. The CTE increases with a slight upward curvature with temperature, and it is twice as large in the *c* direction than the *a* direction, at all temperatures. The 3-dimensional CTE surface that describes this property with respect to the crystal directions has the appearance of an ellipsoid. Hence, the CTE is isotropic in the x–y plane and shows the maximum anisotropy in any plane containing the z axis.

The elastic anisotropy is greater than the CTE anisotropy and is illustrated as a surface of Young's modulus values in 3 dimensions in Fig. 4.2b. This figure is shown at two temperatures, the upper half at 150 °C and the lower half at −45 °C, which bounds the typical range of application temperatures for most electronic systems. Sn is most compliant in the <100] directions and stiffest in the [001] direction and almost as stiff in the <110] directions (hence, Sn is nearly isotropic on <110) planes). At low temperatures, the maximum anisotropy ratio is about 2, but this ratio increases to about 5 at the highest temperatures. An important non-intuitive outcome of the stiffness and CTE is that Sn is stiffest in the direction that the CTE is

[1] While there are only four atoms in the Sn unit cell and eight in the diamond cubic unit cell, the connectivity of the tetrahedral bonding arrangement is the same. More atoms are required in the diamond cubic unit cell to describe the symmetry than the tetragonal Sn unit cell.

Table 4.1 Important anisotropic physical properties of Sn

Property	Direction[a]			Reference
	<100]	<110]	[001]	
Young's Modulus at −45 °C	28.7	65.9	71.4	11, 12
Young's Modulus at 22.5 °C	23.5	62.4	66.6	11, 12
Young's Modulus at 150 °C	13.3	54.5	57.7	11, 12
CTE at 30 °C	16.5	16.5	32.4	13
CTE at 160 °C	22.3	22.3	45.9	13
Diffusivity[b] of Sn	10.7, 105.1	10.7, 105.1	7.7, 107.2	72
Diffusivity of Ag in Sn	0.018, 77.0	0.018, 77.0	7.1e-3, 51.5	73
Diffusivity of Cu in Sn	2.4e-3, 33.1	2.4e-3, 33.1	*D* = 2e-6	74
Diffusivity of Ni in Sn	1.87e-2, 54.2	1.87e-2, 54.2	1.92e-2, 18.1	75
Electrical resistivity	ρ_0	ρ_0	$1.48\rho_0$	76

[a]Use of mixed braces <*uvw*] and <*hkl*) represents the symmetry of the tetragonal crystal structure; the first two indices are permutable, to be in the same family. Crystal directions *[uvw]* and plane normal directions *(hkl)* in a crystal based Cartesian coordinate system are *[ua va wc] and (h/a k/a l/c)*
[b]Diffusivity values are D_o in cm^2/s and activation energy Q in kJ/mol

highest, and this implies that there will be profound disagreements at grain boundaries where dislocations are generated, leading to localized plastic deformation of the crystal. Hence, the amount of diffusion or dislocation generation required will be in proportion to the magnitude of the disorientation[2] between the two crystals and the change in stress or temperature.

Nonequilibrium Solidification

Solidification of alloys in practical time scales always involves nonequilibrium solidification processes that result in metastable microstructures, but the equilibrium phase diagram is useful to anticipate the direction of evolution of Sn–Ag and Sn–Cu phases as shown in Fig. 3.1. The Sn-rich corner of the ternary Sn–Ag–Cu phase diagram in Fig. 3.1b shows that the ternary eutectic temperature is lower than the eutectic temperatures of the binary alloys identified on the X and Y axes. As solder joints spend most of their lives above half their melting temperature (i.e. 0.5 $\times (220+273)-273=-26.5$ °C), there is sufficient thermal energy for nonequilibrium microstructures to evolve into a state that is closer to equilibrium. Thus, understanding of solder joint property evolution depends on the starting nonequilibrium state of the solidification microstructure. Alloys such as SAC105 and SAC305 are

[2]The word misorientation is used loosely in the materials field and is often used to refer to "disorientation" too. Disorientation describes the angle of mismatch between two grains at a grain boundary. The word misorientation is used to refer to the difference in orientation between two locations within a grain and hence is descriptive of lattice curvature and low-angle boundaries.

hypoeutectic alloys, so primary solidification of Sn is expected to occur first (see table in Fig. 3.3). As the solidification of Sn commonly takes place at temperatures significantly lower than the eutectic temperature, the liquidus lines are projected below the eutectic temperature in Fig. 3.9. This implies that initial precipitation of Ag_3Sn or Cu_6Sn_5 could occur before Sn solidifies, even in a hypoeutectic alloy. An example of a nonequilibrium solidification path is illustrated for a Sn-3.8Ag-0.7Cu alloy in Fig. 3.9 and discussed in depth in the associated text. Solidification microstructures are greatly dependent on the solidification path that is actually followed, which depends on the details of nucleation of the Sn phase.

Typically, undercooling of 20–30 °C occurs in Sn-based solder joints. This is most commonly investigated using differential scanning calorimetry experiments. Figure 3.5 shows an example of a heating curve and Fig. 3.9 shows a cooling curve, where 15 °C undercooling is apparent before solidification started. Most other metals and alloys solidify with heterogeneous nucleation of the solid with only a few °C undercooling. At least two factors contribute to the need for much undercooling; firstly, the small volumes of solder joints reduce the probability of finding a critical nucleus. Secondly, the entropy of fusion of Sn is about 50 % larger than most other metals, implying that formation of a Sn unit cell/nucleus requires a larger amount of coordinated atomic positioning than other metals. The crystal structure[3] shown in Fig. 4.1 is body-centered tetragonal with 4 atoms per unit cell in a fairly open structure with tetrahedral bonding similar to diamond cubic (note the bonding arrangement of the central atom). The tetrahedral bonding (which may exist to some degree in the liquid) and the more open structure may account for a larger entropy change associated with crystallization than is found in other close-packed metals.

The larger entropy of fusion also leads to a larger-than-average release of heat with solidification, such that when solidification commences, recalescence can be significant. This effect is illustrated in the enthalpy diagram in Fig. 4.3a where the microstructure of a Sn–Ag solder ball shows a dendritic solidification microstructure. In the plot, an 80 °C undercooling condition is shown for illustrative convenience (which has occasionally been observed in isolated balls, but 30 °C is more typical), indicating that an 80 °C temperature increase is needed to bring the undercooled two phase solid + liquid into an equilibrium condition at the melting temperature. That is, the heat released by the enthalpy of fusion resulting from solidification reheats the sample to the melting temperature in a nearly adiabatic (constant enthalpy) process. Once the melting temperature is reached, a certain fraction of the Sn is solid, about 1/3 in the plot. It is likely that the fraction that solidifies adiabatically will occur quickly, and that once the two phase equilibrium temperature is reached, then the rest of the solder ball would solidify at the rate

[3] The density of α Sn in the diamond cubic structure is 5.769 g/cm^3 and β Sn in the body-centered tetragonal structure is 7.365 g/cm^3. If Sn atoms were in a face-centered cubic arrangement like Pb, then based upon the atom diameter defined by the closest spacing in the c direction, the density would be 8.75 g/cm^3, 19 % higher. Thus the BCT Sn crystal structure is more open than a close-packed lattice but denser than α Sn.

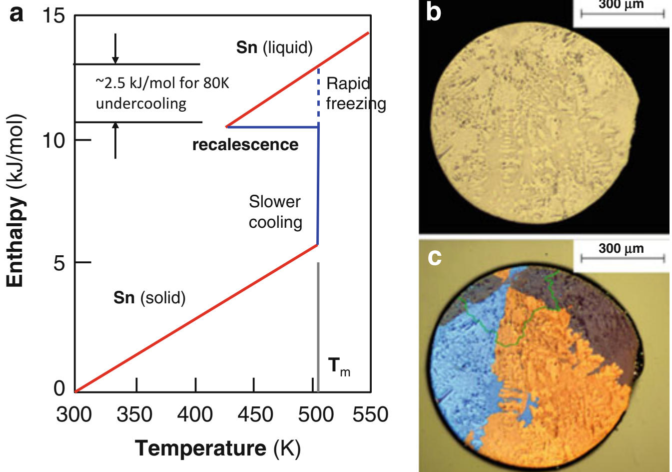

Fig. 4.3 (**a**) Enthalpy plot of Sn showing an exaggerated undercooling-recalescence path, and (**b**) a polished bright field optical image of a Sn-3.9Ag-0.6Cu solder ball polished through the center to illustrate a location close to the probable nucleation site. (**c**) Polarized light image of the same image showing a typically beachball microstructure, with an *overlaid line* illustrating a change in scale of solidification microstructure features that can be seen without distraction in (**b**)

imposed by the environment. Figure 4.3b, c illustrates a region near the pole that has much finer dendritic features than the rest of the solder ball. A green line in the polarized light image in (c) delineates the boundary between two scales of microstructural features [this boundary is easier to see in the bright field micrograph in (b)]. As finer microstructural features are a consequence of faster solidification rates, this boundary suggests that if solidification started at the pole of the beachball, a spherical cap with a diameter of about 1/2 of the diameter of the ball itself may have solidified much more quickly than the rest of the ball. This provides a way to correlate the recalescence event with the enthalpy plot. Using the formula for the volume of a spherical cap, this volume is about 4 % of the volume of the ball, which implies that this ball started to solidify after it undercooled at least 10 °C below the melting temperature (and hence, 4 % of the of the ball solidified adiabatically).

The solidification process has been monitored in situ in a synchrotron X-ray beam to identify some important features of the solidification process [14]. Figure 4.4 illustrates a sequence of 4 diffraction pattern images taken prior to melting, during the liquid state, at the moment of solidification and just after solidification, with integrated diffraction patterns overlaid. This solder joint was at the corner of a wafer-level chip-scale package (WLCSP) sample, so upon cooling, considerable strains developed as the sample cooled. Four important observations from these measurements are (1) the orientations of the crystal(s) before and after solidification are different (compare Fig. 4.4a, d), which implies that there is no obvious influence from the substrate on the orientation of the solidified joint; (2) the solidification took

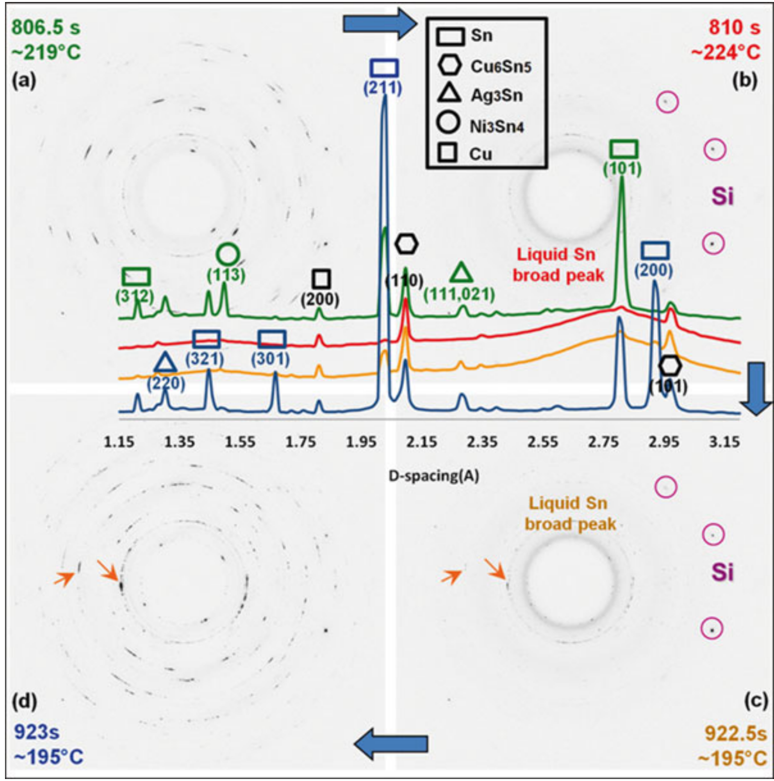

Fig. 4.4 In situ diffraction patterns during melting and solidification, illustrating how the Sn and Ag_3Sn peaks disappeared after melting and reappeared upon solidification. The *broad ring* indicates the liquid Sn phase. The Cu_6Sn_5 phase in the interface remained solid, as did Si (the Si chip was oriented to a nonsymmetric orientation in order to have few peaks). Solidification occurs within 1 s

place about 25 °C below the melting temperature; (3) the solidification process took place within 1 s, as images were taken at the rate of 2 per second; and (4) the orientations present just after solidification remained unaltered during the subsequent cooling process (not shown).

Figure 4.5 illustrates features of the beachball microstructure that are often seen in SAC solder joints, to compare different characterization methods and perspectives. In the top half of the figure, a series of polarized light images illustrate how the appearance is altered when the sample is oriented differently with respect to the polarized filters. Even a difference of 1.3° makes a noticeable change in the contrast of the different orientations, as the negatively sloped boundary is visible in the image marked 0° but only visible with knowledge that it is there in the image labeled −1.3°. The contrast reversed with a 90° rotation. This beachball structure has also been observed in other minerals such as aragonite and chrysoberyl and described as cyclic twins, owing to the repetition of interface disorientations about a common axis that

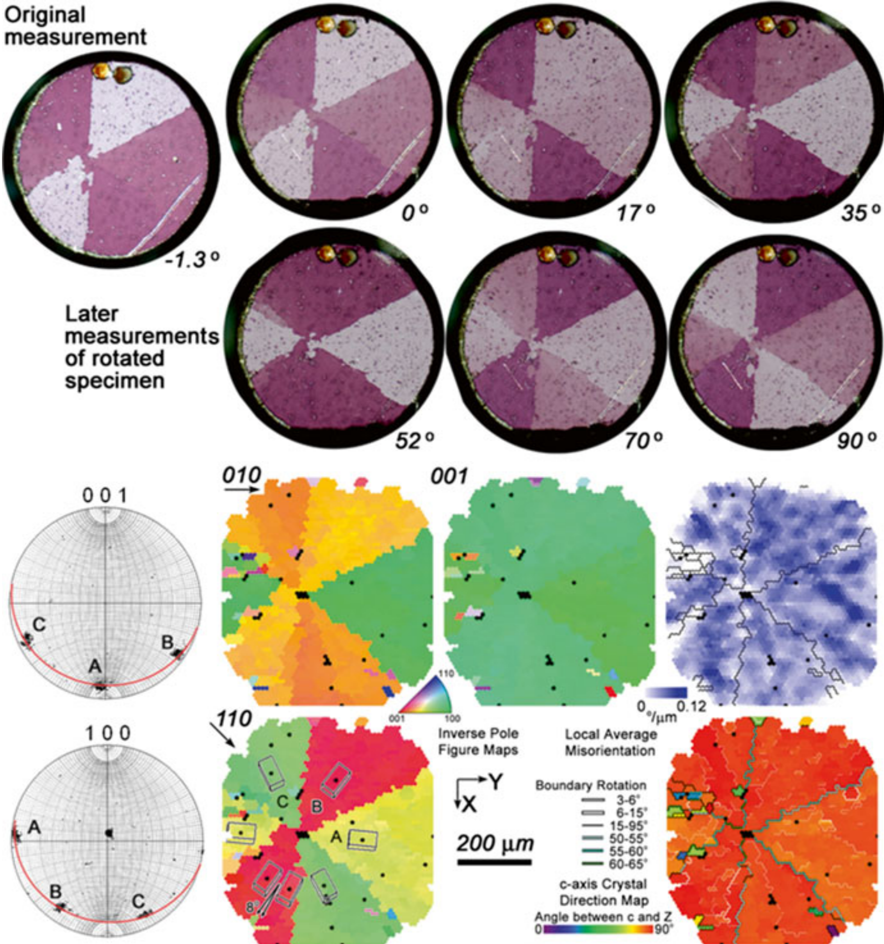

Fig. 4.5 The beachball microstructure of one particular SAC solder joint, showing three orientations arranged in six sections. It is characterized using several different polarized light filter orientations (the sample was rotated with a fixed filter condition, and then the images were rotated to have the ball in the same orientation on the page), and with different types of maps and pole figures made using an EBSP data set

sums to 360°. In the ideal beachball microstructure, there are six sections with three orientations, where the orientation on the opposite side has the same orientation and contrast, as illustrated in the figure. The beachball microstructure is more effectively characterized using scanning electron microscopy with electron backscattered diffraction pattern mapping (aka orientation imaging microscopy or OIM™), as illustrated in the lower part of Fig. 4.5. The left three maps are based upon inverse pole figure directions, where the color key is interpreted with respect to the sample [100], [001], and $[1\bar{1}0]$ directions, which give very different appearances. When the map

is referenced to the beachball axis direction (close to the [001] sample orientation), all sections have the same color, and hence the joint could appear as a single crystal. In order to clearly interpret the crystal orientations, at least two maps need to be made. The two orientation maps on the right illustrate other insightful ways to represent OIM data. Orientation gradient maps such as the local average misorientation show regions of greater and lesser lattice curvature, which varies spatially in every section, which will be discussed further below. Given the anisotropy related to the *c*-axis orientation, *c*-axis maps are often effective. In the lower right map, all three sections have a similar *c*-axis orientation with respect to the board, and hence, their color is similar, but minority orientations appear (small green grains) in a way that could be missed in other maps.

Depending on how the joint is cross-sectioned, the appearance of the beachball microstructure can vary significantly (sometimes hiding the threefold orientation relationship). In many cases, distortions in the shape of the three beachball orientations can be so strong, that only the pole figure will reveal that there are only three orientations having the beachball orientation relationship. Nevertheless, the orientation relationship between the three orientations exhibits a particular set of characteristics easily observed in pole figures.[4] The (001) and {100) pole figures in Fig. 4.5 illustrate the characteristic signature of a beachball orientation relationship. The three orientations present have a common [100] axis, which is near the center of the {100) pole figure for this ball (this common axis can have any orientation in a given joint). The other {100) poles show up three times for the other three orientations on a great circle 90° from the common (100) pole. The three (001) poles in the other pole figure are on the same great circle, at positions between the (010) poles.

A major concern about using 2-D sections is that nothing is known about the rest of the volume (though it can be inferred in many cases). Thus high-energy X-ray (synchrotron) measurements are useful because diffracted beams penetrate all the way through the sample. Figure 4.6 shows diffraction patterns for two balls out of a one row slice from a PBGA package [15]. Indexation of the pattern confirms that the full volume of many joints have one dominant orientation, and sometimes two orientations that are close to the same, indicating the presence of low-angle boundaries or a tri-crystal, as illustrated Fig. 4.7 shows a 14x14 plastic ball grid array in the as-solidified and aged state, sectioned parallel to the board interface. There are 38 joints (19 %) that are apparently single crystals this is an upper bound, see Fig. 4.5 which illustrates the limitations of this 2-dimensional cross-section method). This statistical analysis shows that SAC-type alloys tend to solidify as either single or tri-crystals [16–18].

[4] Pole figures show the orientation of crystal directions in the sample coordinate system. There is only one (001) pole in each crystal and two {100) poles, which are 90° apart, so that viewing the (001) pole figure allows the number of crystals to be identified, and with the {100) pole figure, one or a few orientations can be visualized.

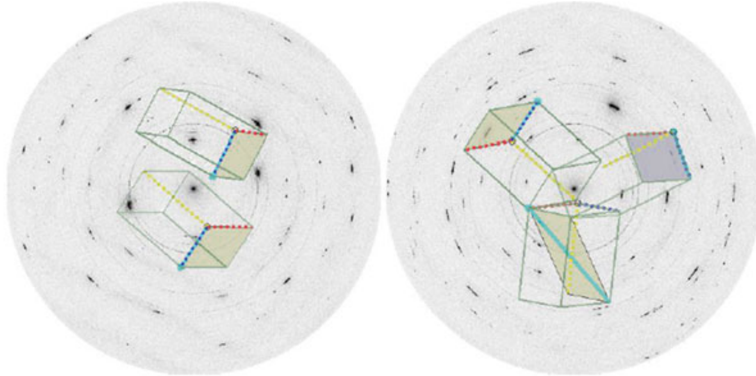

Fig. 4.6 Synchrotron diffraction pattern measurements of two different balls from a slice out of a package, illustrating one joint with two orientations that are close to each other, and another having a tri-crystal orientation relationship (slip planes with high Schmid factors in the vertical direction are illustrated)

Fig. 4.7 A 14×14 array of joints illustrating the variety of orientations of single and tri-crystal orientations. The *color code* is based upon the *c*-axis orientation with respect to the substrate. Ball D13 (4th row, 13th column) is examined in detail in Fig. 4.5

Sn Nucleation

From the discussion above, important factors that affect formation of a Sn nucleus were identified, so the actual nucleation process will be considered next. The fact that many joints solidify as single crystals implies that one nucleus forms and solidification takes place through the entire joint volume before another stable nucleus can form. Even if another stable nucleus does form in the joint prior to completion of solidification, the recalescence front at the solid–liquid interface is likely to remelt or destabilize it, such that the first growing nucleus will establish the orientation of the entire joint.

Given the strong driving force for rapid solidification arising from significant undercooling, the origin of the beachball orientation relationship described above must involve a nucleus that brings about all three orientations at the same time. Hence, a Sn-beachball nucleus requires formation of the nominally 60° interfaces at the time that a nucleus becomes stable. Recent investigations of this phenomenon in Sn have led to the hypothesis that a pseudo-hexagonal nucleus can form around an Ag atom at the center of a hexagonal unit cell, which enables growth to a size that is stable enough to then force three distinct Sn tetragonal orientations to develop radially [19]. Figure 4.8 shows how the {101)<101] twin system can form a 6-sided pseudo-hexagonal nucleus, such that Sn [100] directions radiate from the center, but this twin has a disorientation of 57.2°, not 60° [19]. Thus, misfit dislocations are required to compensate for the imperfect closure.

The fastest-growing crystal direction is <110], and these directions are illustrated on the related planar surfaces of the pseudohexagonal nucleus in Fig. 4.8 [20]. This shows that once this pseudohexagonal nucleus starts growing, the beachball

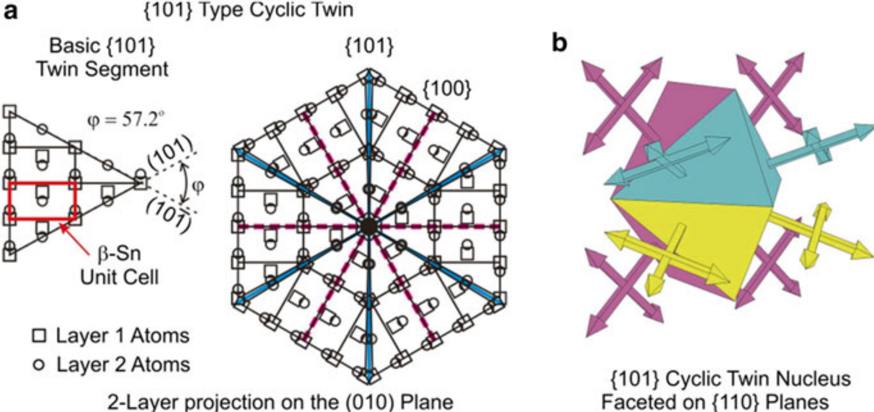

Fig. 4.8 Pseudo-hexagonal unit cell based on {101} cyclic twins made from tetragonal unit cells that form the basis of the beachball microstructure, and schematic arrangement of fast growing <110] planes that lead to stable growth of a cyclic (beachball) twin. [19]

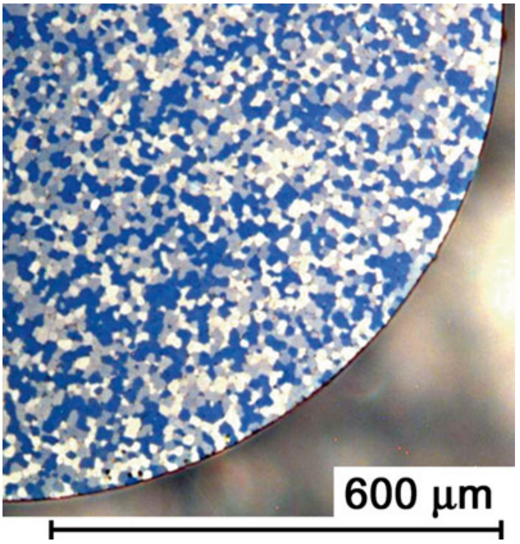

Fig. 4.9 Examples of joints in which solidification commenced at lower than usual temperatures, leading to an interlaced microstructure consisting of only there orientations

morphology will be maintained. With decreasing temperature, the most rapidly growing direction can shift to other directions, which has been documented in other crystal structures. Fast growth in directions other than (110) would not provide the stable growth of the same orientation in space, and hence, dendrites growing in other directions could intersect. This leads to interlaced microstructures, which still only have three orientations, but the cross section of this type of microstructure appears to have a fine polycrystalline appearance (example in Fig. 4.9). As the solidification rate slows down, conditions favoring normal [110] growth will often take over partway through the solidification process, and microstructures that show both the interlaced and beachball type microstructures signify that the initial solidification process occurred with greater undercooling. Also, with greater undercooling, it is more likely to obtain two nuclei, leading to rare examples of microstructures with 4 or 6 orientations, but these tend to occur about 1 % of the time.

It is common for these beachball twins to exhibit disorientations between 55 and 65° in EBSP maps such as the one shown in Fig. 4.5. Clearly, a 57° twin interface with periodic misfit dislocations could lead to a disorientation of 60°, but this boundary would have a higher energy than a perfect twin. Alternatively, some boundaries could have the lower energy 57° twin disorientation, but in order to close the cyclic twin, other boundaries would need to have a compensating 63° disorientation, and this has been observed in some locations in many joints, showing up as a double peak in the disorientation histogram. On the other hand, lattice curvature within each section of the cyclic twin could also allow *all* of the interfaces to have the 57° disorientation, such as the one shown in Fig. 4.5. As illustrated in the lower right c-axis crystal direction map the disorientation between the sections of the twinned grains are closer to 55°, as indicated by a blue line on a thicker black boundary line. There are only a couple of short segments near the center where a disorientation greater than 60° is present, and a disorientation just below 50° in the lower center

boundary. To compensate for the lack of closure of 57° twin boundaries, there are many low-angle boundaries present in large Sn grains (white boundaries in the lower right map). In some joints, there is a disorientation peak at 7°, which is an especially stable low-angle boundary that has a coincidence site lattice [21]; such a boundary is illustrated in Fig. 4.5 in the lower left section of the beachball, with a thicker white boundary. Inspection of the pole figures in Fig. 4.5 shows that all of the peaks are spread out by almost 10° along the great circle, indicating that each grain orientation is full of geometrically necessary dislocations, that allows the low energy 57° twin interfaces to exist. Consistent with the need to maintain 57° boundaries, the peak that is the least spread out is the common [100] rotation axis peak.

Twin Systems in Sn

There are two twin systems in tin [22]; the {101)<101] system that is involved with beachball nucleation, and the {301)<103] that is a mechanical twin system. Figure 4.10 illustrates the geometrical arrangement of one layer in the (010) plane

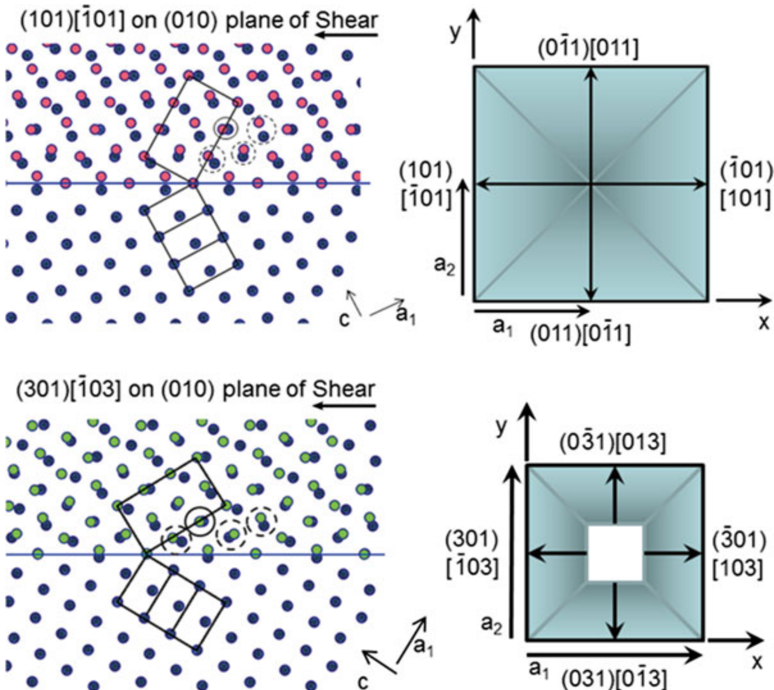

Fig. 4.10 Geometrical arrangement of Sn unit cells that lead to the {101} and {301}twin planes. Shear from the *dark to lighter* orientations could lead to the twin symmetry about the {101} or {301} plane. The *circled atom* positions illustrate the sense of shear and shuffles for each of the four repeating atom positions in the unit cell needed to generate the twin. Unit cells are plotted to show the four possible plane orientations and twin directions for each system

of shear (plane of the page). The second layer of the repeating crystal structure has atoms in the same arrangement but shifted in space from the corner to the body center position (see Fig. 4.8). Shear in the direction of the arrow is needed to generate either the pink {101) or green {301) atomic positions from the parent dark-blue positions. In both images, three parent unit cells are outlined to show the atom positions on a (010) face and to show the symmetric twin orientations in the twinned lattice. In both cases, only one out of 4 atoms is displaced in the direction of shear (circled with solid line), and 3 other atoms must shuffle to move to a new lattice position in the twinned crystal structure (circled with dashed lines). It is apparent that the shuffles are much larger in the {101) twin shear than in the {301) shear, and this may account for the fact that only {301) mechanical twins are observed. The geometrical arrangement of the four twin systems in each family are illustrated in the representations of 001 projections of the unit cell, showing the orientation of four sloped twin planes; the twin plane has a shallow slope from the basal plane for the {101) family and a steep slope for the {301) twins. The associated twin dislocation direction is shown on each plane (the magnitude of the twin Burgers vector is much smaller than the arrows). The presence of the {101) twins arises from the pseudo-hexagonal solidification nucleus. Thus, it is not likely that the twin interfaces that form on {101) planes are mobile, so their low energy makes these boundaries very stable. The {301) twins are commonly found in shock-deformed samples, and are not commonly observed in deformation conditions at lower strain rates.

Porosity

Solidification of metals always requires shrinkage, and there is a 2.3 % shrinkage from liquid to solid in Sn. The presence of a free surface on all sides of the solder ball provides a natural means for solidification shrinkage to be accommodated. However, larger pores often develop, particularly when solder paste is used, when pores containing flux are occasionally found at locations far from the outer surface. The associated outgassing caused by the flux evaporation are sometimes trapped inside the solder joint and are not able to escape during reflow process. The size of these pores varies from micron scale voids to sometimes a diameter of about ¼ the joint size. As solidification often commences at one of the two interfaces, and because the solidification front travels quickly, pores can be readily trapped in the solidified Sn, often near the substrate interface. Thus, it is important to control flux melting and flowing properties and a hold time below 200 °C allow for flux melting and activation, which accounts for the importance of the right reflow profile for each surface-mount and board assembly (see more detail in Chap. 2).

Porosity in solder joints also occurs at the scale of dendrites (a few microns), and this scale of porosity is occasionally observed on the surface of solder joints [23–26]. Surface porosity features near the interconnect on either side of the joint can lead to a local stress concentration due to the higher stress at the reduced diameter at the interconnect. In a recent study of porosity, X-ray tomographic reconstruction was

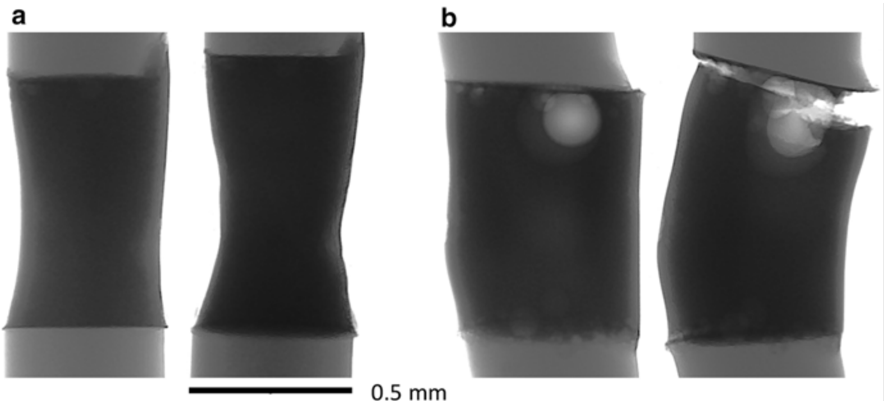

Fig. 4.11 Two radiographs of tensile samples of single crystal solder joints showing porosity on one interface in one joint (**b**) and none in the other (**a**). After tensile deformation to just past maximum load, the joint with pores developed a crack and a corresponding sudden load drop, while the one without pores deformed uniformly and did not exhibit a load drop

used to identify the locations of pores in a simple shear lap sample. In this investigation, computational simulation of the measured geometry including internal pores showed that large pores at the interface provided stress concentrations that facilitated damage development and crack initiation at the solder–substrate interface [23, 24]. However, microporosity arising from trapped voids in the interdendritic regions had no impact on properties. The effect of macroporosity is also visible in Fig. 4.11, which compares radiographs of two single-crystal cylinder type tensile solder joint (verified using X-ray diffraction). In the joint with several pores on one interface (Fig. 4.11b), the crack developed along the interface, while solder deformed more uniformly in the other joint with no pores (Fig. 4.11a).

The Effect of Microalloying

Microalloying of solder alloys (i.e., alloy additions less than 1 wt.%) provides a means to modify the properties of solder joints in beneficial ways [27–29]. One of the main motives for microalloying is to reduce the amount of undercooling that occurs prior to solidification, in order to obtain more homogeneous microstructures with less segregation of intermetallic phases. The IMC phases can grow quickly in the liquid state if they precipitate before Sn. In addition, microalloying to stimulate nucleation can lead to a polycrystalline microstructure, which is desirable for improved resistance to electromigration damage discussed later. A strategy for stimulating nucleation is with inoculants, i.e., to precipitate small compounds in the liquid that have a lattice spacing and surface energy that facilitates nucleation on Sn on this interface. The list of microalloying elements that have been investigated is

growing, but additions of Mn, Co, Cr, Al, Zn, Ni, Ge, RE elements, and POSS macromolecules have seen significant attention [27–38]. Some of these alloy additions have demonstrated significantly less undercooling but have not been necessarily effective in nucleating Sn. Many of these elements dissolve into the Cu_6Sn_5 intermetallic and alter the lattice parameters so that they have some effect on nucleation of Sn. For example, microalloying addition of Ni facilitates formation of fine $(Cu,Ni)_6Sn_5$ intermetallic particles that are effective in pinning grain boundaries and hence delay or prevent recrystallization (discussed in more detail later). Also, Ni additions alter the composition and growth rate of the intermetallic layer between the solder and the circuit attachment interfaces. Reduction of the IMC interfacial layer growth rate has generally been shown to be desirable because thicker brittle intermetallic materials are prone to cracking (also true with IMC particles within the Sn).

In addition to altering undercooling and the formation of precipitates with desirable characteristics, microalloying can affect the evolution of the interfacial intermetallic layers both during the melting stage and during joint service lifetime [39]. The small amount of microalloying from the surface finish can also affect the overall joint microstructure, as discussed in Chap. 2. The beneficial effects of Pd deposited in a thin layer on the interfacial metallurgy layers will be discussed later and also in Chap. 6. One of the most significant effects of the Cu in SAC alloys, in contrast to the binary Sn–Ag solder, is that the initial presence of Cu in the liquid solder alters the chemical potential of the liquid, so that there is less of a driving force for dissolution of Cu from the interfaces. This results in a smaller thickness of the brittle interfacial intermetallic layers, and when these layers are thinner, they are less prone to forming cracks. With less of a driving force for dissolution of Cu, there is less Cu in the liquid during the liquid stage, and consequently there is less supersaturation of the liquid with Cu that facilitates formation of large rods of Cu_6Sn_5, which can facilitate formation of cracks in the joint.

A third major effect of addition of Cu into the alloy in the first place is that it facilitates formation of cyclic twin tri-crystals. The presence of tri-crystals reduces the fraction of extreme values of the CTE among a population of joints. Figure 4.12 illustrates how formation of tri-crystals affects the average CTE from a population

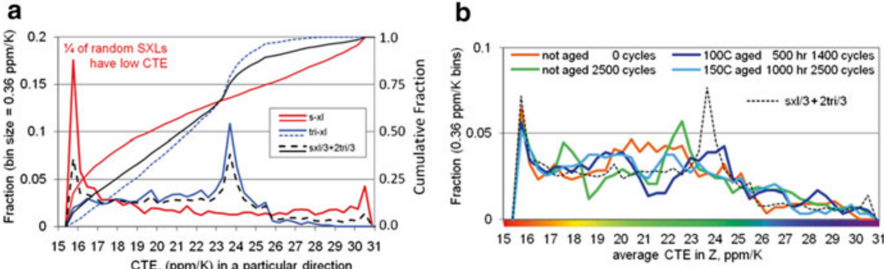

Fig. 4.12 Distribution of CTE values in a specified direction based upon a random number generated set of orientations. (**b**) Comparison with experimentally measured CTE values from a population of 200 joints. The experimental simulation is close to that expected when there is about 1/3 single crystal and 2/3 tricrystal joints

of about 2,000 simulated orientations based upon the assumption of a random orientation nucleation assumption, and many observations have shown that this assumption is close to what is observed in reality, as illustrated with several data sets with similar distributions [18].

This topic is in its infancy, and much more research and discovery are anticipated in the next decade. There is the opportunity and a general goal to identify microalloying elements that can truly make a random polycrystalline microstructure, or to assist in forming controlled crystal orientations that take advantage of the anisotropy of Sn in intentional ways.

The Effects of Isothermal Aging

The microstructure, mechanical response, property, and failure mechanisms of Sn-based solder joints are constantly changing due to the effects of isothermal aging. The observed variation in material behavior during thermal aging is universally detrimental to reliability and includes reductions in stiffness, yield stress, ultimate strength, and strain to failure, as well as highly accelerated creep. The reduction of tensile strength even with room temperature aging was identified in 1956 by Medvedev [40] in Sn–Pb solder, followed by many other publications in both Sn–Pb solder alloys and Sn–Ag and Sn–Ag–Cu alloy systems [41–50].

As the solidification microstructure is metastable, thermal activation will lead to microstructural evolution into structures with less interfacial energy and possibly changes in crystal structure of the IMCs. For example, Cu_6Sn_5 has a monoclinic microstructure in its equilibrium structure, but it initially forms in a metastable hexagonal structure that can transform into the monoclinic structure, depending on microalloying present in the alloy and thermomechanical history. Also, microalloying elements can stabilize the hexagonal structure [38].

Figure 4.13a, c illustrates the initial dendritic microstructure present after solidification on a finer scale than illustrated in Fig. 4.3. This microstructure has two constituents, particle-free Sn and regions surrounding it that contain dispersions of fine particles that are effective in pinning dislocations, leading to a composite material having hard regions and soft regions defined by the shapes of the primary β-Sn dendrites and the final liquid to solidify. Within the β dendrites, low-angle boundaries are commonly observed, which are visible in the backscattered electron image shown in Fig. 4.13c, (small orientation differences lead to large differences in the backscattered electron intensity). With optimized tilting conditions, individual dislocations or dislocation subgrain walls can be visualized. In the midst of the nanoscale Ag_3Sn precipitates, some of the larger particles have other compositions, depending on the initial solder composition and the time and temperature history in the liquid state. There are many variations on this microstructure, depending on the Ag content and the rate of solidification. With a slower solidification rate, such as in larger sample volumes (e.g., cast bulk tensile samples), the Ag_3Sn particles are larger and more cylindrical than spherical, and the dendritic structure is more clearly defined [51].

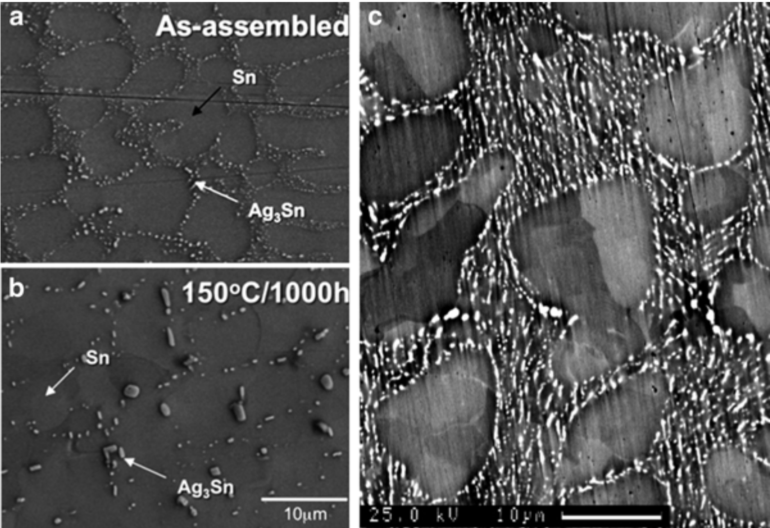

Fig. 4.13 Secondary electron image of as-fabricated SAC305 solder microstructure (**a**), and the coarsened microstructure after aging (**b**). Backscattered electron micrograph of as-solidified eutectic Sn–Ag solder (**c**) illustrating subgrain boundaries within β tin dendrites, which are only slightly visible in the secondary electron images in (**b**) [Photo credit Tae-kyu Lee (**a, b**) and Boon-Chai Ng (**c**)]

Effect of Aging on Precipitate Morphology

It is common to simulate the microstructure that develops with years of service conditions by aging an as-fabricated sample to transform the eutectic microstructure regions into Sn with roughly evenly distributed larger particles (Fig. 4.13b). The presence of dislocations within the β-Sn dendrite provide dislocation pipes that facilitate coarsening of Ag_3Sn particles. This coarsening process results in an increase in the spacing between particles and hence a reduction in the stress needed to cause dislocation motion throughout the joint. In thermal cycling experiments on as-fabricated samples, this drop in the stress occurs exponentially over the first several hundred cycles, and it depends on the magnitude of strain. While aging can also cause coarsening similar to that observed in thermal cycling experiments, the significant difference is that during thermal cycling, the stress changes continually, leading to dislocation generation and recovery, and the temperature change facilitates the dissolution of precipitates at high temperature and re-precipitation of dissolved elements in solution back onto existing precipitates, which is a process that does not occur during long-term aging. Hence, interpretation of outcomes of experiments with an isothermally aged microstructure needs to be interpreted with these differences in mind.

The strength degradation and the increase in creep rate with the isothermal aging temperature are interrelated. The underlying mechanism for the reduction in strength

in SAC solder alloys after aging is due the microstructure coarsening and also the IMC precipitate coarsening. With the temperature increase that starts the aging process, there is stress relaxation arising from CTE and anisotropic stiffness effects, resulting in an exponentially decreasing creep rate. Creep is strongly dependent on dislocation nucleation, mobility, and grain size. Finer grains will cause more grain boundary sliding facilitated by absorption of dislocations into boundaries, which accelerates grain boundary diffusion and thus leads to faster creep deformation and stress relaxation. Particle coarsening results in larger distances between particles, which enables more shear strain by bowing of dislocations that are pinned by particles. With fewer and larger particles, the pinning effect of particles on grain boundary motion is reduced. The contribution of dislocation motion to the apparent elastic modulus will therefore increase with increasing grain and particle size. This explains why isothermal aging can cause a reduction in the apparent elastic modulus [50]. The interrelationships between particle spacing, dislocation density and grain boundary mobility will be discussed in more depth in Chap. 5.

Isothermal aging results also show that after an initial tensile strength drop, Sn–Pb eutectic solder reaches a relatively stable condition after about 200 h of aging. However, for SAC, both the tensile and creep properties continuously change with increasing aging time. It is noteworthy that the creep deformation of SAC is only lower (better than) Sn–Pb at room temperature and shorter aging times. There is a crossover point at about 50 h of aging at 125 °C (Fig. 4.14) where the creep resistance of SAC becomes lower than Sn–Pb [49, 52]. The associated microstructure comparison between the Sn–Pb and the SAC305 alloy is shown in Fig. 4.15. But we must note that these results were based on bulk solder samples. The situation becomes more complex when we consider the joint as an interconnect with different interface materials.

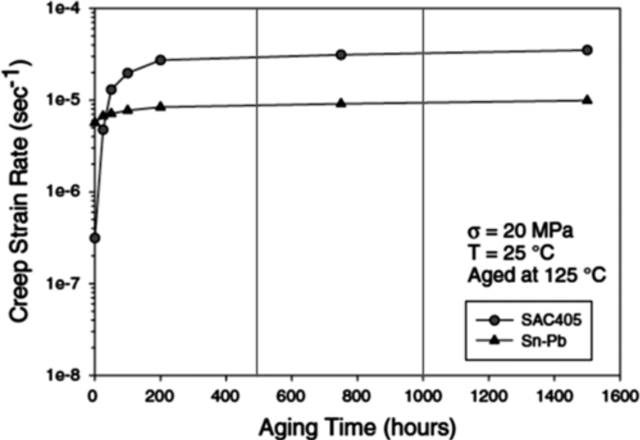

Fig. 4.14 Comparison of Sn–Pb and SAC405 creep rates for aging at 125 °C

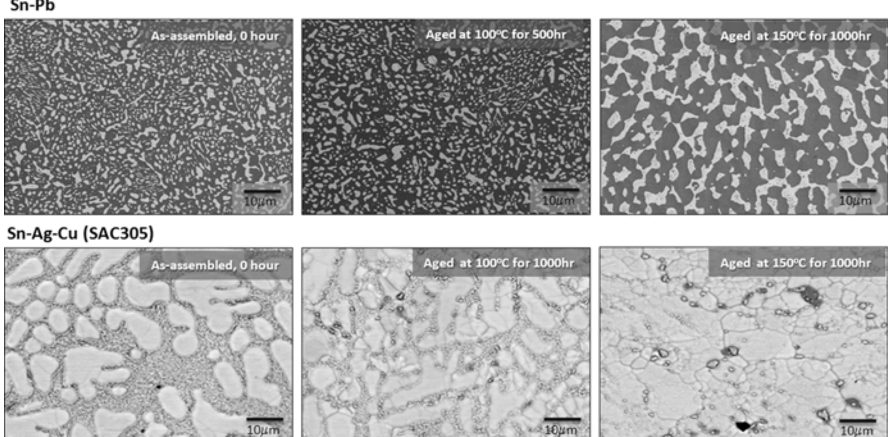

Fig. 4.15 Microstructure comparison of Sn–Pb and SAC305 before and after aging at 100 and 150 °C for 500–1,000 h

Interfacial Composition and Property Evolution with Aging

Isothermal aging is also affected by alloying element concentration gradients. The rate of particle growth depends on the precipitation and coarsening kinetics, which in turn depend on the local concentration gradients. In thermal cycling conditions, coarsening is also affected by dislocation generation and stress states, but in either case, variability is expected because diffusivity in Sn is anisotropic (Table 4.1). As each joint has its own orientation, the details of particle coarsening vary according to the crystal orientation and the stress state boundary conditions arising from the interactions between the crystal orientation, the package design, and the position of the joint in the package.

As electronic components evolve to smaller and higher functionality with higher-density packages, the solder ball diameter needs to shrink [53, 54]. This technological trend is associated with several challenges because as the solder joints become smaller, the thickness and morphology of the solder joint interface intermetallic compounds (IMC) will become a larger fraction of the volume of the interconnect. The related concentration gradients will depend more sensitively on the composition of the bulk solder alloy, the microstructure, and the surface finish of the packages and boards [55–57]. One of the main sources for the alloy element concentration gradient is the package and board-side surface finish. Since the component and board experience a liquid–solid diffusion interface during reflow, a significant amount of elements from the surface finish flow into the bulk liquid solder and sometimes produce a localized element concentration, which can be observed by identifying the IMC precipitate composition and location. The influence of these surface-preserving layers on joint properties is stronger with smaller joints.

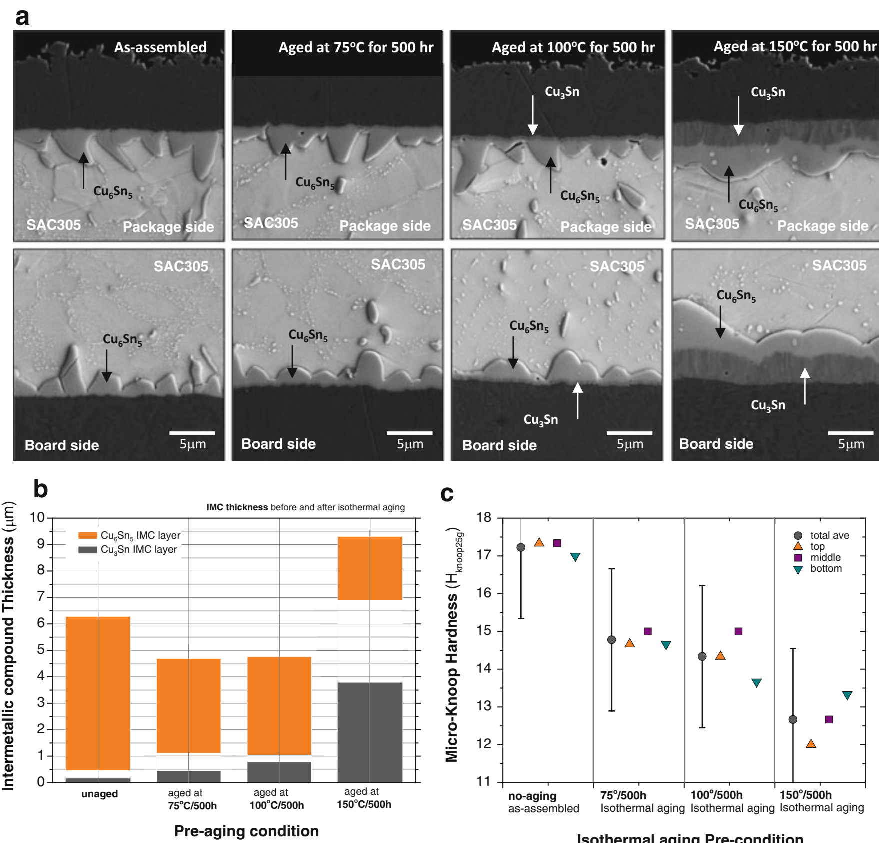

Fig. 4.16 Effect of temperature on SEM microstructure, IMC thickenss, and hardness before and after isothermal aging in a joint with Immersion Sn surface finish on the package side and Cu–OSP on the board side (**a**). Package side (*top*) and board side (*bottom*) interfaces have similar microstructures after aging for 500 h at 75, 100, or 150 °C. The IMC thickness increases (**b**) and Micro Knoop hardness decreases (**c**) with increasing temperature

As discussed in Chap. 2, various surface finish combinations can exist on either side of a joint. For example, when both sides of the joint use organic solderability preservative (OSP) on Cu, Fig. 4.16 shows the same features on both sides of the joint. As explained in Chap. 2, OSP is an organic layer and dissolves into the solder joint during reflow, leaving the joint interface with a simple Cu/IMC/solder interface. When the composition is similar on both sides but made with different methodologies, such as immersion Sn surface finish on Cu and OSP surface finish on the other side, with SAC305 solder between, the feature characteristics are the same on both sides of the joint (compare with Fig. 2.9). While the morphology of the Cu_6Sn_5 differs, a relatively balanced elemental gradient will exist on both sides of the joint; a scallop-shaped IMC develops with a finely distributed IMC precipitate network in the bulk. With isothermal aging, as shown in Fig. 4.16, the scallop shaped IMC layers

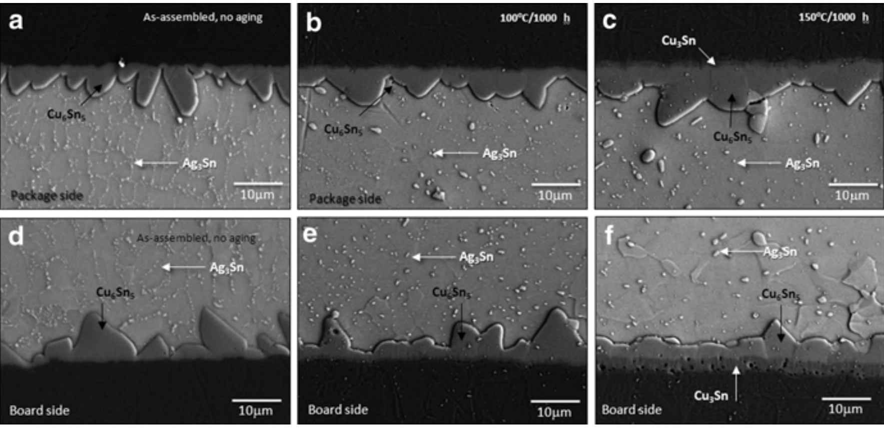

Fig. 4.17 Effect of aging time on SEM microstructure for Cu–OSP surface finished package side (a,b,c) and Cu–OSP on the board side (d,e,f) before and after isothermal aging. Package side interface (**a, d**) as-assembled (**b, e**) after 100 °C/1,000 h aging and (**c, f**) after 150 °C/1,000 h aging [13]

on the package-side and board-side interface change from at the initial state to develop a more uniform thickness after aging at 150 °C. This smoothing is also shown in the IMC thickness plot in Fig. 4.16b, and in Fig. 4.17b, e, where the gap between the maximum and minimum thickness of the Cu_6Sn_5 layer becomes narrower after aging at 150 °C for 500. With increasing time, the overall thickness variation becomes less and a uniform thickness develops. The growth of the Cu_3Sn layer is also observed with a gradual growth rate, but the growth is accelerated with higher aging temperature. Because both package and board side have a sufficient source of Cu, the microstructure and hardness difference between the package side and board side is minimal. Figure 4.16c shows similar hardness values at different positions in the joint, but an overall decrease of hardness occurs due to the bulk microstructure evolution with larger IMC precipitates. Figure 4.17 also shows the same kind of interface microstructure development when both joints have the same Cu-OSP surface preparation.

Unlike Cu/solder/Cu structures, when one surface has Ni/Au surface finish, (either electrolytic Ni/Au or electroless Ni/Au (ENIG)), a more complicated structure develops with aging. The formation and the growth mechanisms of IMCs that form between the solder and the interfacial metallization have been extensively studied in various solder alloy systems and alloy compositions [58–62]. During thermal aging, the IMC on the Ni side will grow with a substantial morphology change from $(Cu,Ni)_6Sn_5$ needles to a smoother continuous morphology while suppressing the growth of the Cu_3Sn layer.

One example with electrolytic Ni/Au surface finish is shown in Fig. 4.18, where the microstructure of two different solder alloys, Sn-1.0Ag-0.5Cu (wt.%) (SAC105) and Sn-3.0Ag-0.5Cu (wt.%) (SAC305), are compared. SAC305 shows finer and

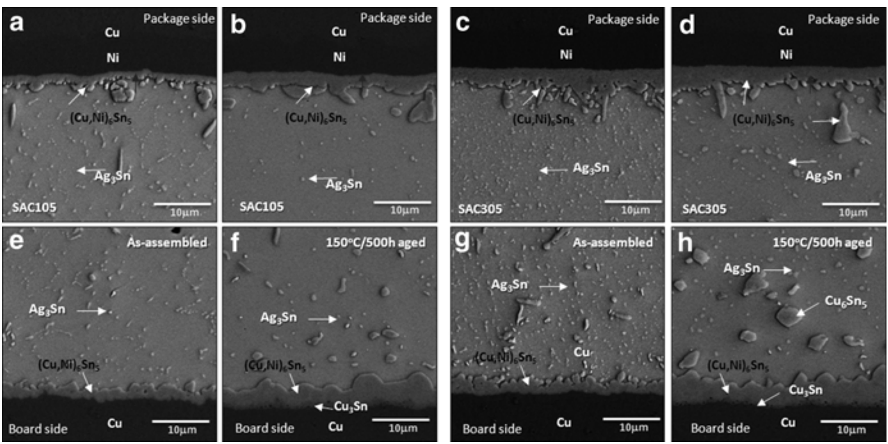

Fig. 4.18 Effect of alloy composition on SEM cross-section microstructure on the package side (**a, b, c, d**) and board side (**e, f, g, h**) of SAC105 (**a, b, e, f**) and SAC 305 (**c, d, g, h**) before aging (**a, e, c, g**) and (**b, f, d, h**) after aging at 150 °C/500 h

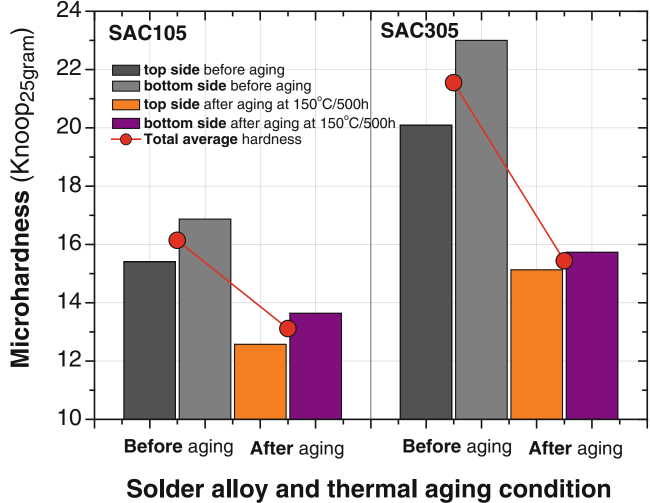

Fig. 4.19 Micro knoop hardness data for SAC105 and SAC305 before and after aging at 150 °C/500 h

more abundant Ag_3Sn precipitates in the solder β-Sn matrix than SAC105, which eventually makes SAC305 harder compared to SAC105 joints. The measured hardness in Fig. 4.19 shows how much the hardness drops after isothermal aging, which is based on 12 solder joints per condition with two indentations per joint inside the solder bulk region, near-package-side interface, and board-side interface. The IMC precipitates grew larger, and the number of precipitates decreased, resulting in a

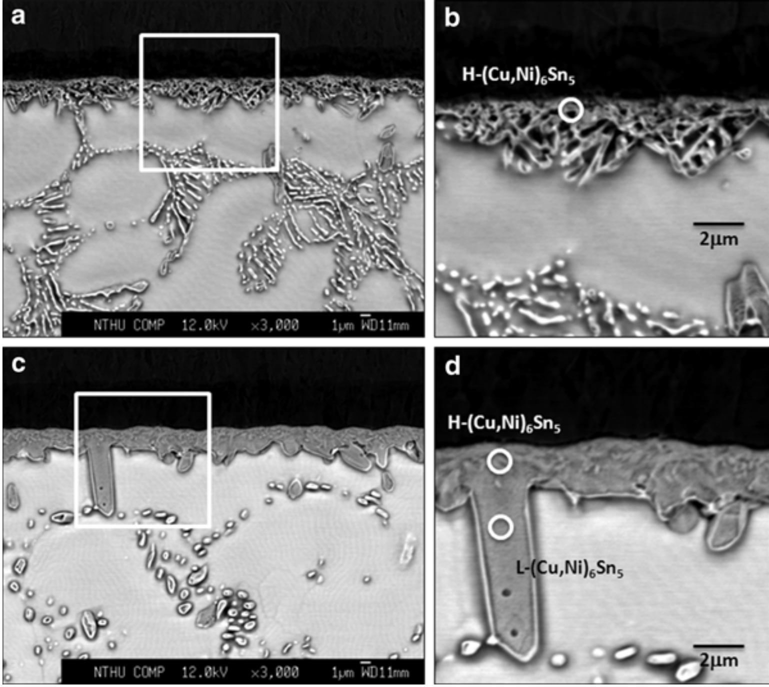

Fig. 4.20 Package side interface after board assembly (**a, b**) and after isothermal aging (**c, d**). Electrolytic NiAu surface finish

lower hardness value after aging. The drop in hardness is smaller in SAC105 since the initial amount of Ag_3Sn is lower than SAC305. Also, the interface IMC layer becomes smoother after aging compared to the Cu/solder/Cu joint configuration, but with a closer look at the interface structure, there are actually two distinguishable layers discussed next.

Figure 4.20 shows an interface between SAC305 solder and electrolytic Ni/Au surface after assembly and after isothermal aging at 150 °C for 500 h. Actually Fig. 4.20a is the same interface which was shown in Fig. 2.9. As explained in Chap. 2 already, during reflow, a reaction between the solder alloy SAC305 and the Ni/Au interface occurred with Ni diffused from the substrate side into the solder alloy, leading to the formation of needle-like $(Cu,Ni)_6Sn_5$ at the solder/Ni interface. The composition analysis using EPMA shows that the average Ni concentration was ~20.0 at.% in $(Cu,Ni)_6Sn_5$, represented as H-$(Cu,Ni)_6Sn_5$ in Fig. 4.20b. After aging, an additional layer covered the initial IMC layer at the solder/Ni interface, and two kinds of $(Cu,Ni)_6Sn_5$ layers with different Ni content were detected. Figure 4.20d shows that a continuous L-$(Cu,Ni)_6Sn_5$ layer with a lower Ni content formed above the H-$(Cu,Ni)_6Sn_5$ IMC, proving that the Ni is distributed nonuniformly in $(Cu,Ni)_6Sn_5$ and maintains a sharp interface between those two. In H-$(Cu,Ni)_6Sn_5$,

the average Ni concentration was similar to the as-assembled interface with ~16.7 at.% Ni while after aging it was ~6.4 at.% in L-$(Cu,Ni)_6Sn_5$. The $(Cu,Ni)_6Sn_5$ IMC formation is attributed to the redistribution of Ni and Cu atoms as the Ni substrate reacts with SAC305 solder. As $(Cu,Ni)_6Sn_5$ is more stable than Cu_6Sn_5 [4], apparently the H-$(Cu,Ni)_6Sn_5$ cannot be diluted with subsequent aging, which resulted in an interface between the H-$(Cu,Ni)_6Sn_5$ and L-$(Cu,Ni)_6Sn_5$. During aging, the solubility of Cu in Sn decreases from 1.23 wt.% to approximately 0.001 wt.% as temperatures change from 250 to 150 °C [9]. This quantitative analysis shows that the Cu content near the solder/Ni interface decreased from 1.17 wt.% as reflowed to 0.46 wt.% after aging. Thus, the supersaturated Cu gradually migrated toward the interface and precipitated as L-$(Cu,Ni)_6Sn_5$ at the interface to decrease the energy of the system. Hence, L-$(Cu,Ni)_6Sn_5$ formed a substantial layer above the H-$(Cu,Ni)_6Sn_5$ IMC during aging [31]. In addition, H-$(Cu,Ni)_6Sn_5$ is as an effective diffusion barrier to block the Ni migration into solder, and retarding Ni diffusion into L-$(Cu,Ni)_6Sn_5$.

ENIG Versus ENEPIG After Isothermal Aging

An even more subtle example of the importance of microalloying can be illustrated by adding an additional element into consideration to show how it causes differences in the evolution of the IMC layer that can significantly affect interfacial properties. As reviewed in Chap. 2, electroless nickel immersion gold (ENIG) is aformed by the deposition of electroless nickel–phosphorus on a catalyzed copper surface followed by a thin layer of immersion gold. The immersion gold protects the underlying nickel from oxidation/passivation like the electrolytic Ni/Au surface finish [63, 64]. One of the drawbacks with ENIG is the potential risk of galvanic hypercorrosion in the Ni–P layer caused by the immersion in the Au solution, which is usually called the “black pad” issue [65]. To overcome, an additional layer was introduced, and the ENIG becomes electroless nickel/electroless palladium/immersion gold (ENEPIG) surface finish. The insertion of the Pd layer is believed to prevent corrosion underneath the Ni–P layer that exists before the immersion Au plating solution is used.

The growth behavior of Cu_6Sn_5 in ENIG and ENEPIG joints in Fig. 2.12 shows differences in the interfacial reaction of ENIG and ENEPIG solder joints. Irregular-shaped IMCs formed after reflow on both metallizations. During the early stage of soldering, the thin Pd finish as well as the Au finish was dissolved within a few seconds into solder [66].

Figure 4.21 shows the interfacial reaction of ENIG and ENEPIG solder joints followed by thermal aging. After a 1,000 h 150 °C thermal age, the morphology of the IMC became layer-like in both joints. After aging, a thin dark layer formed between the Ni–P and Cu–Sn IMC in both samples (Fig. 4.21a, b). The composition of this phase was 75.4 at.% Ni and 24.6 at.% P, (Ni_3P) that precipitated from amor-

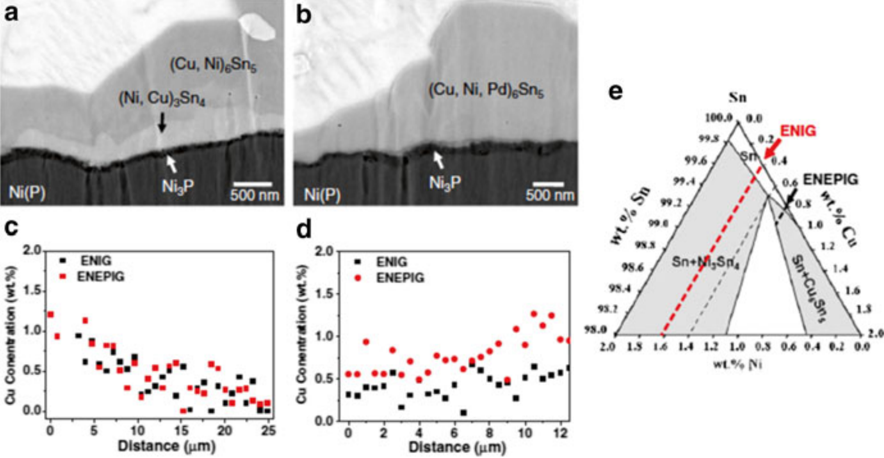

Fig. 4.21 Detailed cross-sectional images. (**a**) ENIG and (**b**) ENEPIG after 1,000 h aging; concentration profiles of Cu trace line near the solder/IMC diffusion zone in (**c**) vertical and (**d**) parallel directions and (**e**) enlarged Sn corner of Sn–Cu–Ni ternary isotherm [31]

phous electroless Ni–P during the reflow process [63, 64, 67, 68]. The formation of an IMC layer on the Ni–P layer would motivate the Ni_3P crystallization. Interestingly, an additional IMC formed between Ni_3P and $(Cu,Ni)_6Sn_5$ in the ENIG joint with a bright phase in Fig. 4.21a but not in the aged ENEPIG joints. The composition of the bright IMC was 36.4 at.% Ni, 10.7 at.% Cu, and 53.0 at.% Sn, which is close to the stoichiometry of $(Ni,Cu)_3Sn_4$. The inclusion of Cu in this compound that normally forms on Ni sites comes from the Cu in the solder. From the Sn–Cu–Ni ternary isotherm [69–71], the $(Cu,Ni)_6Sn_5$ IMC is stable when the Cu concentration in the Sn–Cu–Ni alloy is greater than 0.6 wt.%. This implies that the bright layer formed when the Cu content was less than 0.6 wt.%. Figure 4.21c shows the concentration of the Cu with distance from the interface toward the solder side in a direction perpendicular to the interface. It is evident that the concentration of Cu decreased from interface into the solder, indicating that Cu migrated to the solder/IMC interface during thermal aging to grow Cu_6Sn_5. The other Cu composition trace in Fig. 4.21d was measured at distance of 2 μm above interface, indicating fairly constant values for both conditions, yielding an average Cu concentration of 0.4 ± 0.2 wt.% and 0.8 ± 0.5 wt.% for ENIG and ENEPIG joints, respectively. As indicated in Fig. 4.21e, only $(Cu,Ni,Pd)_6Sn_5$ formed at the solder/ENEPIG interface due to the higher Cu concentration, and the smaller Cu concentration (0.4 wt.%) required $(Ni,Cu)_3Sn_4$ to form between $(Cu,Ni)_6Sn_5$ and Ni_3P layer. The higher Cu concentration in the ENEPIG joint can be attributed to less growth of interfacial $(Cu,Ni,Pd)_6Sn_5$. This difference provided the ENEPIG, a potentially tougher mechanical interface than ENIG joint structures, which can show improved mechanical stability. The example of the effect of microalloying Pd in the solder via surface

finish illustrates how composition and chemical reaction evolution is a crucial factor to consider in order to assure the stability of the joint in thermal, mechanical, and chemical performance. Clearly, the structure of the IMC geometry can affect the performance, the elemental distribution, as shown in this case where the local Cu concentration affects the stability of the interface, which then affects the overall property of the joint.

Summary

The formation of a solder joint involves complex nonequilibrium conditions resulting from many factors. First, the reluctance of β Sn to generate a stable nucleus leads to formation of single-crystal or tri-crystal (twinned) joints in the SAC alloy system and a solidified state that has a high defect density due to the fast growth rate of the solid. This characteristic is sensitive to both alloy and microalloying chemistry, and the details of solidification will differ according to details of the alloy additions. Secondly, once solidified, which occurs within a second, there is not much time for equilibrating complex internal stress states arising from the anisotropic CTE and elastic moduli of Sn. Thus, dislocation activity is substantial, resulting in orientation gradients and some generation of subgrains. Thirdly, the intermetallic precipitate and interface structure is heterogeneous, and it evolves with aging to weaken the microstructure. These are important issues that affect the performance of the joint in thermal and mechanical fatigue conditions that are discussed further in Chaps. 5 and 6.

Aging also causes complex restructuring and growth of the IMC layer that depends on the history and chemistry of joint formation with the metallization layers on either side of the joint. The necessary and complex metallization includes thin layers that result in localized microalloying. When strategically managed, this form of microalloying can lead to desirable IMC properties that are important, as its strength and toughness significantly affect joint properties discussed further in Chap. 6. However, before considering the importance of IMC properties, Chap. 5 examines how the very unstable solidification microstructure evolves under the influence of thermal cycling. With thermal cycling, the effects of aging discussed in the last part of this chapter take place, but it is further complicated by temperature changes that also introduce energy into the microstructure by elastic and plastic straining coupled with changes in solubility and diffusivity. These compositional and strain energy changes create driving forces for atomic transport that promotes significant changes in the microstructure, and hence, significant changes in joint properties that are explored in the next chapters. An illustrated overall summary chart is shown in Fig. 4.22.

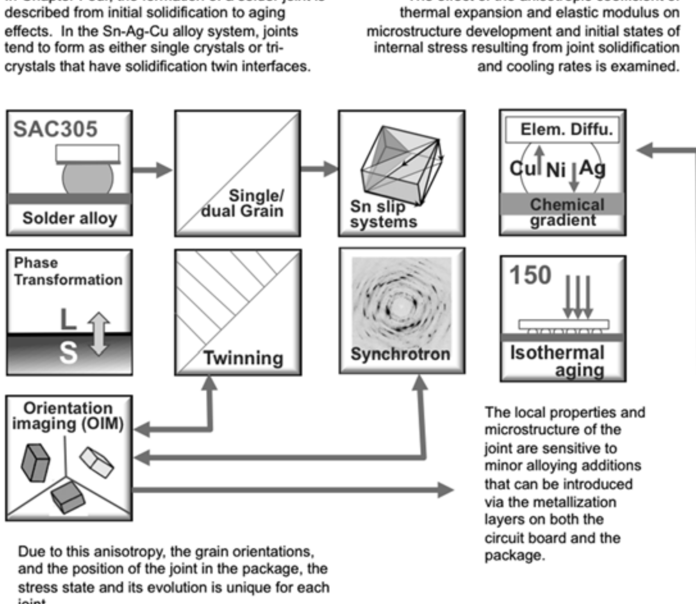

Fig. 4.22 Overall summary chart of Chap. 4

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Chapter 5
Thermal Cycling Performance

The effects of package design on thermal cycling performance are examined by considering how the crystal orientation(s) within the joint affects stress evolution due to the influence of the anisotropic CTE and elastic modulus. With low-stress designs such as plastic ball grid arrays (larger balls with a large pitch), it takes thousands of cycles before cracks are prevalent, while direct chip attachment designs such as wafer-level chip-scale packages will fail in a few hundred cycles. While the number of cycles to failure varies with design, the microstructural evolution is similar: First, low-angle boundaries develop by recovery processes where continuing strain leads to their conversion to high-angle boundaries by a continuous recrystallization mechanism. Concurrently, particle coarsening changes the limiting grain or subgrain size, until particles are larger and more widely spaced, and discontinuous recrystallization nuclei form due to mechanical twin formation or particle-stimulated nucleation at the larger particles. As these new orientations develop and form random high-angle boundaries that can easily slide, cavitation damage develops, which link up along high-energy random grain boundaries, so that cracks percolate behind a discontinuous recrystallization front until the crack crosses the sample. The foundations of anisotropic elastic/plastic crystal plasticity models are described, which recognize operative slip systems, and by combining such models with particle coarsening prediction, they have the potential to predict recrystallization. The effects of aging, interface IMC composition and evolution, and Ag content on the recrystallization process are examined in detail, along with the complications that come with current stressing.

Thermal Cycling Performance: Introduction

Chapters 3 and 4 identified how unstable a solder joint is from a thermodynamic perspective when it is formed. Introduction of cyclic thermal energy provides the means for the nonequilibrium microstructure to move closer to equilibrium. While

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T.-K. Lee et al., *Fundamentals of Lead-Free Solder Interconnect Technology*,
DOI 10.1007/978-1-4614-9266-5_5

this happens, the evolving solder microstructural state must be sufficiently strong and ductile to hold the electronic system together to enable it to function. A functioning device can experience thermal fluctuation from both internal and external sources. The Joule heating due to high current through a solder interconnect will increase the temperature of the component itself or adjacent components, which will cause steep temperature gradients during on–off transients. Recent advanced packages can reach over 125 °C in the joint during function. External inputs add additional temperature fluctuations to the functioning device temperature, such as day and night cycles (e.g., heat generation due to higher use or lesser activity) as well as environmental temperature cycles such as portable or transportation-related devices, where on/off cycles in winter produce an even wider temperature fluctuation.

In addition to thermal cycling, electronic devices experience additional external forces or fields including mechanical stress, electric fields, chemical corrosion, and complex thermal fluctuation-induced thermomechanical elastic and plastic deformation resulting from the anisotropy of the CTE and elastic modulus. Hence, a device or an electronic product can be placed in various environments with different boundary conditions that need to be examined for the effect they have on the reliability of the electronic system. Some form of metric is needed to identify the risk level or factor, whether the product or device can function until the end of expected life without failure. To assess whether it can accomplish lifetime expectations, two approaches are common. One approach is preliminary testing to see if the system survives with a sufficient statistical certainty to allow business planning and costing, which is time consuming and may not represent actual-use conditions. The other approach is accelerated thermal cycling tests (ATC) that are more aggressive than expected-use conditions, commonly used to determine how robust a prototype system is. Also, finite element computational models of boards are used to assess survivability before anything is built. However, these models are only as good as the ability of material models to sufficiently represent the material behavior. Ultimately, identification of the failure mechanisms and properly installing them into the material models will make computational design for reliability possible in the future.

In this chapter, the effect of these temperature fluctuations on component stability and life will be examined first, followed by industry standards regarding thermal cycling test methods, which are used to assess the performance. Then, the general trend of microstructural evolution that is typical for different package types is described, based on subgrain evolution mechanisms that precede development of high-angle boundaries. The heterogeneity of microstructure evolution with respect to crystal orientations is a major consideration. This evolving heterogeneity develops in response to the level of local strain/stress conditions that depend on the detailed design of components. Microstructure evolution by isothermal aging occurs concurrently and precedes localized recrystallization that often leads to crack nucleation and propagation. The combined effects of isothermal aging on thermal cycling performance and current stressing effect will be examined.

Thermal Expansion

Materials react and respond to temperature changes at different rates. The expansion and contraction happens in a volumetric manner that is described as the volumetric coefficient of thermal expansion (CTE). For simple geometries, a linear approximation can be sufficient, but due to the anisotropy of Sn, the linear CTE is not very accurate. The linear coefficient is commonly used for design, because materials with a cubic crystal structure have isotropic expansion behavior. However, non-cubic materials such as Sn or most ceramics have an anisotropic (volumetric) CTE that complicates how stresses develop in response to a temperature change.

As discussed in Chap. 4, Sn is a complex material with a CTE that depends on the crystal orientation. In addition to that, the materials being connected through various material layers in the interconnection have their own CTE values, some of which are also anisotropic. Thus, a design that accommodates all the strain and stress evolution during fabrication as well as during operation of the component on the board is crucial. Figure 5.1 shows how differential CTE effects lead to warpage for two examples of package interconnects, from a simple capacitor to a multilayered flip-chip BGA

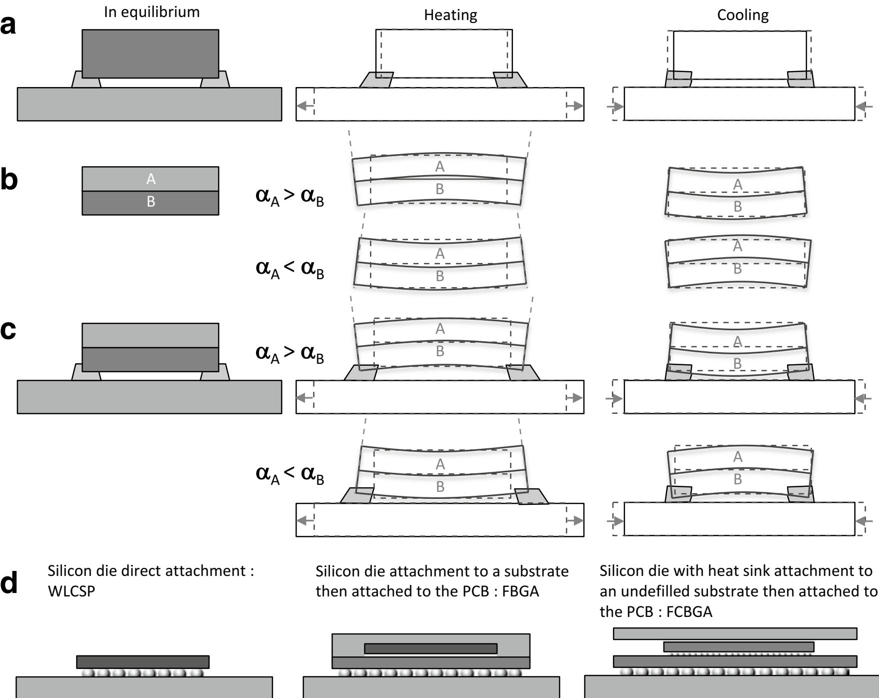


Fig. 5.1 Effects of a temperature change on stress and strain in solder joints; (**a**) single component attached on ends, (**b**) warpage in a two layer assembly, (**c**) effect of bilayer warpage on stress in attachments on the end, and (**d**) practical geometries with these effects

(FCBGA) component. Considering even a simple geometry and material set, such as a chip capacitor on a PCB, the continuous on and off conditions can heat and cool the component, causing stress buildup at the interconnect. Among BGA packages, WLCSPs are one of the simplest structures since the silicon die has a single well-defined and isotropic CTE. But once it is put on the substrate or circuit board, especially with a larger body size, the design calculation needs to consider not only the linear shear caused by the difference in CTE between Si and the PCB but also tension and compression caused by component warpage. Figure 5.1a shows an example of thermal cycling-induced shear imposed on the joints at both ends. Since the component is a bulk material (although it has multiple layers inside the component), the expansion happens horizontally. Compared to the single bulk component, if there are two (or more) bonded layers with different thermal expansion coefficients, the heating will cause warping to cause either a smiling or crying face shape as shown in Fig. 5.1b. The situation is further complicated when that component is assembled to a board. The combination of the board expansion and heating (and cooling) can cause several strain/stress deformation modes at the joint at different times, with smiling and crying faces (Fig. 5.1c). The effect of warping of the component results in various deformation modes within joints, depending on the material layer properties. A selected material property list is shown in Table 5.1, which shows the modulus, Poisson's ratio, and CTE for silicon, bismaleimide–triazine (BT) substrate, Cu pad, die adhesive and molding compound, and three examples of package designs that cause smiling/crying warpage effects are illustrated in Fig. 5.1d. While the diagram is simplified to show only two joints in Fig. 5.1a and c, joints in the middle will experience more axial cyclic deformation than shear/bending deformation, and joints in between will experience complex mixtures of shear, bending, and axial deformation.

The component/package design affects how joints deform in several ways. For example, thinner substrate components can experience more strain during thermal cycling compared to thicker substrate designs. Of course the substrate material and the metal layer distribution will affect the overall CTE of the substrate, but larger body size components are more likely to experience warping and thus impose more compression and tension force on joints during thermal cycling, especially at the cornermost joints and the joints at the center of the component. As these large body size components also have thicker substrates with a higher Cu layer count, this reduces the amount of bending, such that a longer thermal cycling life cycle number can be obtained. Thus, there is no general rule on what size of package is better in thermal cycling performance because a combination of many factors affect how the joints deform and hence, the reliability.

Table 5.1 Mechanical properties for selected materials commonly used in packaging

Material	Modulus (GPa)	Poisson's ratio	CTE (ppm/°C)
Silicon die	129.5	0.28	2.6
Substrate—BT	14.5	0.11	12.7
Pad—copper	128.7	0.34	17
Die adhesive	16	0.11	17.7
Molding compound	3	0.45	107

Thermal Cycling Test

The thermal cycling-induced degradation mechanism resulting from differential CTE strains is a crucial process that must be understood to accurately predict the reliability of the component. Because each component has its own temperature and function environment interacting with the board design and the material set, the industry has worked together to identify a standard test method that is useful for assessing the performance and use the resulting data to assure the reliability of the component in some defined conditions. JEDEC standard JESD22-A104D "Thermal cycling" [1] is one of these standards.

The test methods explained in JESD22-A104D are designed to determine the ability of components and solder interconnects to withstand mechanical stresses induced by alternating high- and low-temperature extremes. Permanent changes in electrical and/or physical characteristics can result from plastic deformation caused by cyclic thermomechanical stresses.

There are a few ways to impose temperature fluctuations on the component and solder interconnections, including single-, dual-, and triple-chamber temperature cycling systems. The simplest is single-chamber cycling, where the test boards are placed in a stationary chamber and are heated or cooled by introducing hot or cold air into the chamber. In dual-chamber cycling, the load is placed on a moving platform that shuttles between chambers maintained at fixed temperatures. In triple-chamber temperature cycling, the test boards are physically moved between them. Whatever the heating and cooling chamber configuration is, the test boards are brought to a maximum temperature with a controlled heating rate (also called ramp rate) and then held at the peak temperature for a given time and then cooled to the minimum temperature with a controlled cooling rate such as the schedule shown in Fig. 5.2, which defines the parameters of a typical thermal cycling cycle.

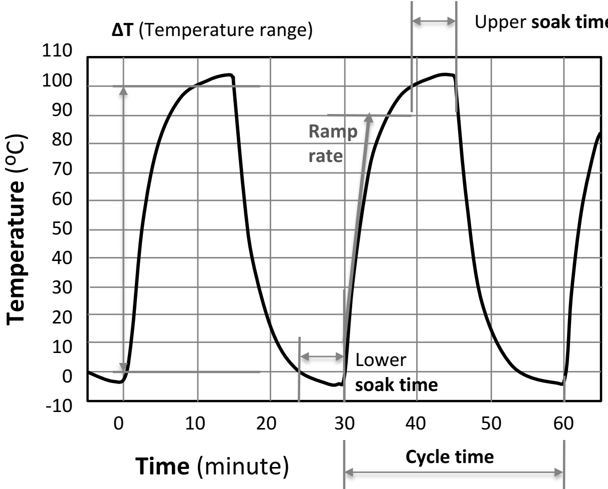


Fig. 5.2 Representative temperature profile of an accelerated thermal cycling test; ramp rates are defined by the initial linear part of the ramp

Table 5.2 Temperature cycling test conditions

Test condition	Nominal T_s (min) with tolerance (°C)	Nominal T_s (min) with tolerance (°C)	ΔT (°C)
A	−55 (+0, −10)	+85 (+10, 0)	140
B	−55 (+0, −10)	+125 (+15, 0)	170
C	−65 (+0, −10)	+150 (+15, 0)	215
G	−40 (+0, −10)	+125 (+15, 0)	165
H	−55 (+0, −10)	+150 (+15, 0)	205
I	−40 (+0, −10)	+115 (+15, 0)	155
J	0 (+0, −10)	+100 (+15, 0)	100
K	0 (+0, −10)	+125 (+15, 0)	125
L	−55 (+0, −10)	+110 (+15, 0)	165
M	−40 (+0, −10)	+150 (+15, 0)	190
N	−40 (+0, −10)	+85 (+10, 0)	125

The maximum and minimum temperatures for thermal cycling are important factors that need to be selected based on the end-use condition. As shown in Table 5.2, there are several combinations of test conditions with different minimum and maximum temperature and ΔT. These test conditions are based on typical end-use conditions, so that a particular test condition can be chosen that best represents the anticipated end-use condition. Use of these standard conditions will develop a database that can help identify commonalities in the failure mode and failure/degradation mechanisms. The effect of ΔT on the overall thermal cycling performance will be addressed later in this chapter. In addition to maximum and minimum temperature, ΔT, the ramp rate, and the holding time is also a crucial parameter, which ranges from 1 to 15 min (even up to 60 min for some laboratory test conditions). For example, test conditions B or G are for harsh environments such as aerospace, aircraft, and automobile under the hood use condition. Test condition *J* is a general temperature range for long-term reliability products in non-portable conditions, which are expected to run for a long time without the mechanical challenges required for a portable or mission-critical device.

Thermal Cycling Performance of Different Package Types

While it is difficult to identify the thermal cycling performance for a particular package type, a trend for several types of packages is shown in Fig. 5.3, indicating that the characteristic life drops with joint size and pitch for a variety of package types with different board configurations and package body sizes. More detailed information on each package type configuration can be found in Chap. 2, Fig. 2.2. QFPs live longer than QFNs in thermal test conditions, and a BGA shows lower performance than

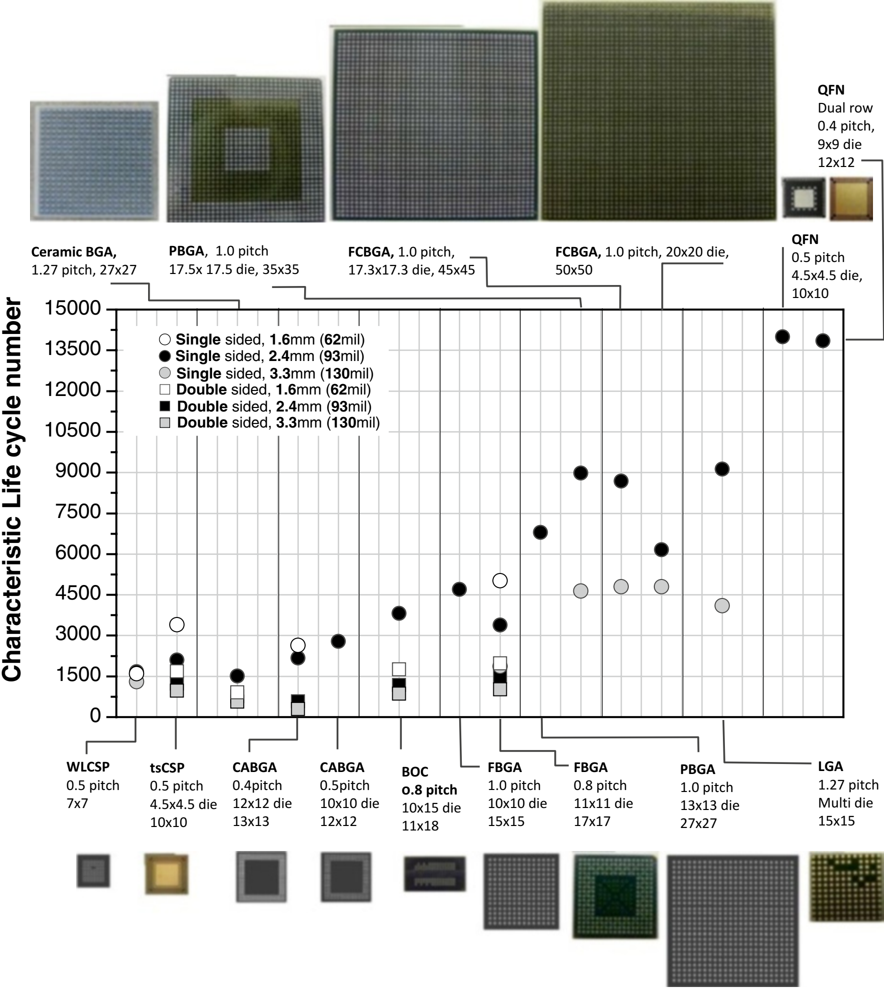


Fig. 5.3 Characteristic thermal cycling life cycle number depends on the package design. Solder alloy for all packages are SAC305. These data are for 0–100 °C with 10 min ramp rate and 10 min dwell

QFNs but with a very wide performance spread because of many factors such as component body size, die size, die to body size ratio, substrate thickness, alloy composition and geometrical ball arrangements, etc. For example, the WLCSP shows a variation of characteristic life cycle based on PCB thickness, with a life cycle from 3,700 cycles to less than 1,000 cycles as the board becomes thicker. The same board thickness effect is apparent in PBGA, FCBGA, and LGAs. There is also an effect from single-side vs. double-side configurations (i.e., a clamshell configuration), as the cycle number is degraded by more than 1,000 cycles with the double-side configuration with a same board thickness. The same single- to double-side comparison

is clearly shown in other package types, such as CABGA, BOC, and FBGAs. Another important detail is that the substrate material effect is stronger than the body size dependency in CABGA packages. Since the CTE of a ceramic substrate is much different than organic substrates, even a small body size package with a relatively large pitch (1.0 mm) shows a much lower life cycle number compared to other package types. All of these factors complicate the ability to predict. It is important to recognize that simple consideration of material property and structure to estimate the lifetime expectancy is not sufficient, since the interconnect itself is a complex anisotropic moving target with different characteristics from one joint to another, so that performance depends on many detailed internal and external factors.

As noted in the array of OIM maps in Fig. 4.7, each solder joint has different crystal orientations, and when this is combined with the complex CTE, chemical composition effects, and elastic property interactions, every joint becomes unique within its environment. The effect that crystal orientation has on variability in deformation is illustrated in Fig. 5.4a for a sample with four joints that had the same shear deformation condition. These four joints are from one row of a 4×4 solder joint sample cut from a PBGA, which was pre-cross-sectioned on one side, so that it could be polished before and observed after shear deformation. The sample was shear deformed by

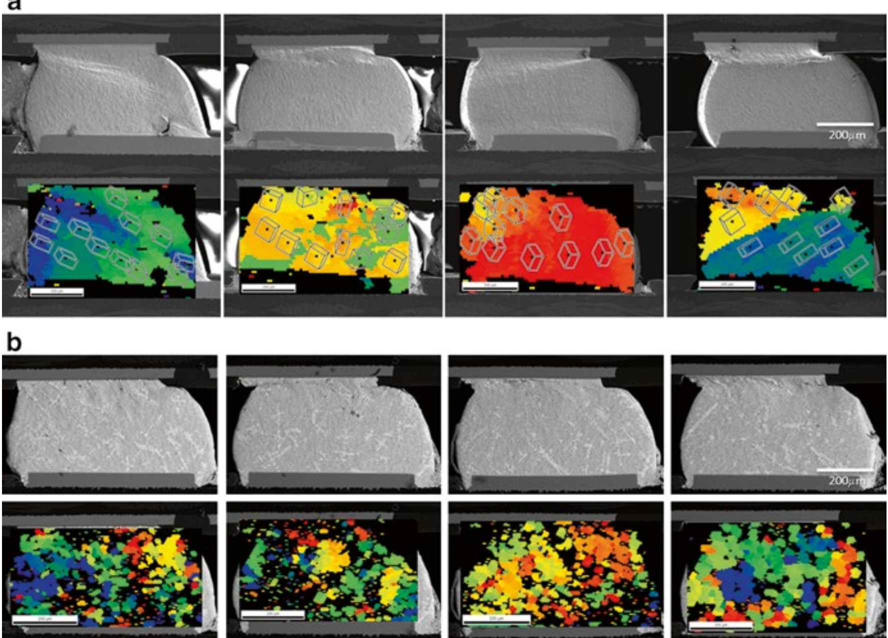


Fig. 5.4 (**a**) Scanning electron microstructure on initially polished and then shear deformed (**a**) SAC305 adjacent solder joints in a PBGA cross section with the corresponding OIM maps based upon Sn c-axis orientation (micron bars are 200 **μ**m). (**b**) SEM image and OIM surface normal direction map overlap showing the microstructure of shear deformed Sn–Pb solder joints taken after shear deformation with 0.01 mm/min. displacement rate

approximately 0.4 mm displacement, and they are expected to have the same amount of deformation for each joint. But after shear deformation, they show different slip deformation patterns, which make simple modeling inappropriate. Thus, modeling of the deformation of Sn-based solder joints is a very complex challenge.

In contrast, the modeling of Sn–Pb solder joints is easier because they solidify as polycrystals and deform more consistently, as illustrated in a similar shear deformed sample with Sn–Pb joints in Fig. 5.4b. There was considerable grain boundary sliding in the zone of highest deformation near the top right corners, but these features are also evident throughout the joint. This consistency in deformation features can be explained by interphase (or grain boundary) sliding that provides additional deformation modes beyond the slip systems in Pb or Sn. In addition, orientation imaging microscopy (OIM) maps show that Sn has various grain orientations that have irregular grain shapes with sizes from 30 to 50 μm. This deformation is much more similar in each joint in contrast to the very different deformation patterns in the SAC solder joints after shear deformation shown in Fig. 5.4a. This means that in Sn–Pb eutectic solder joints, the same overall deformation mechanism operates homogeneously in all joints, but with SAC solder, there are different combinations of operating slip systems in each joint.

An example of different deformation responses from thermal cycling is shown in Fig. 5.5a, which shows polarized light images of the corner ball of three different package on package (PoP) samples, in the as-fabricated, 2,000-, and 3,000-cycle conditions. The as-fabricated joint shows no contrast in polarized image, indicating that it is probably a single crystal. In the polarized image of the joint after 2,000 cycles, many additional orientations were found along the upper left diagonal direction, which is the eventual crack location, but the right side of the joint is not so much affected. The joint after 3,000 cycles shows many new orientations, which make it difficult to identify the original initial orientation (assuming it was also once a single crystal, which is likely from statistical studies on as-fabricated samples). In this solder joint, there is a continuous development of a recrystallized microstructure roughly along the joint diagonal before the crack initiated and grew to final failure, but the specific crack direction differs in different joints, presumably due to different crystal orientations (note arrow directions). Clearly, the solder joint microstructure does not evolve uniformly, but microstructure changes develop along the eventual crack path in a way that depends on the joint stress–strain history and the initial crystal orientation.

Another example is shown in Fig. 5.5b, in a solder joint thermal cycled to failure in a 0.4 mm pitch CABGA with a 13×13 mm body size. In this joint, a localized recrystallization area near the package-side interface developed, but there was no obvious change in the main body of the solder joint, suggesting that it experienced much less strain. The microstructure evolution took place mainly at the upper corner of the solder structure and then propagated throughout the near-interface region on the package side. A less developed degree of orientation change also occurred in the lower left corner. The nature and cause of the recrystallization mechanisms need to be identified and expressed in a model so that stochastic model calculations can be done to predict a distribution of life cycle times for a set of joints with different

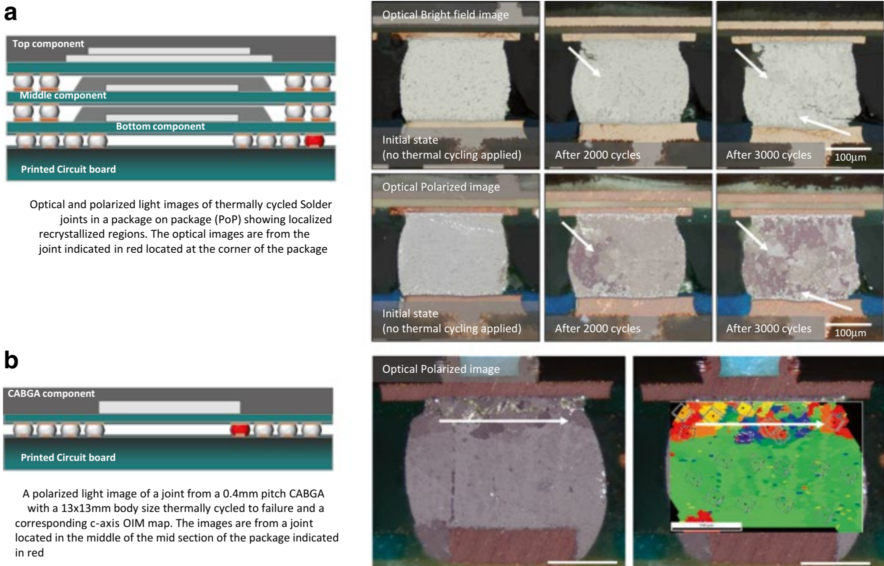


Fig. 5.5 Optical and polarized light images of thermally cycled Solder joints in (**a**) a package on package (PoP) and (**b**) a 0.4 mm pitch CABGA thermally cycled to failure. Arrows identify how cracks follow localized recrystallized regions

initial crystal orientations. Understanding of the failure mechanism that caused these localized microstructure changes is crucial in order to enable solutions to be developed that improve the structural stability.

Sn Grain Orientation Effects on Strain Hysteresis

From Fig. 5.1, it is clear that the package generally expands and contracts less than the board, due to the influence of the silicon die. Neglecting warping effects, a differential shear strain will increase with distance from the neutral point at the center of the package. Thus, balls near the corner under the die shadow area should experience the greatest shear strain, and it is well established using isotropic Sn–Pb balls that failures consistently occur at these corner locations. However, early assessment of failures in packages with Sn-based solder showed that though there is a higher chance of failure at corner or die edge locations, failures occurred in any position in a package [2, 3].

The cause of failures where there is little shear strain is due to strain hysteresis in the direction normal to the board arising from anisotropic CTE of large Sn crystals. Given that the CTE can differ from 15 to 30 ppm/K normal to the board, Fig. 4.12 [4] considers the likelihood of having joints with the extreme values of the CTE

normal to the board. The distribution for single crystals (red curve) shows a high likelihood of finding joints where the c-axis is parallel to the board, such that the CTE perpendicular to the board is at the lowest value; the cumulative distribution plot shows that 25 % of the total population of single-crystal joints can have such a low value. In contrast, only 5 % of the population will have the highest CTE value close to the board normal direction, and the median value of the CTE is near 20 ppm/K for single crystals. Thus, a joint with the lowest CTE in the normal direction will experience a delta CTE value of 5 ppm/K from the average CTE of all joints. With a temperature difference of 100 °C, this imposes a cyclic strain of 0.5 %. Using a modulus value of 50 GPa (Fig. 4.12) results in a stress of 25 MPa, which is sufficient to cause creep or plastic yielding. Thus, joints that have extreme values of the CTE will experience significant plastic strain hysteresis even at the neutral point.

Figure 4.12 also shows how tri-crystals reduce the likelihood of finding orientations with extreme values of CTE (assuming that there are equal volumes of the three orientations). The median CTE is higher, 22 ppm/K, because the fraction of orientations with the lowest CTE is about 10 %, and the maximum possible CTE drops to about 28 ppm/K (dashed blue curve). Experimentally, there are about 2/3 tri-crystals and 1/3 single crystals in packages investigated in reference [5], and the distribution of CTE values extracted from measured orientations and area fractions from OIM scans in several packages with different histories shows distributions that are similar to the computed random distribution. The effect of beachball microstructure may be one of the primary reasons for the greater success of SAC305 solder over other lead-free alloys, as beachball microstructures are readily formed using this alloy system.

Thus, the primary effect of the anisotropic character of Sn is that the strain hysteresis in the normal direction is as important as shear direction. Given that warping also imposes a significant normal direction cyclic strain, which varies with position, it is clear that the interaction between the imposed boundary conditions at each ball location coupled with the random orientations of solder joints leads to the reality that the stress–strain history of every joint is unique.

Phenomenology of Thermal Cycling Microstructure Evolution

From statistical studies of microstructures on plastic ball grid arrays (PBGA), chip array ball grid arrays (CABGA), and wafer-level chip-scale packages (WLCSP), thermally cycled for various times, with and without pre-aging, an overall sequence of microstructural evolution is commonly observed [4–11]:

1. The solidification process leads to large grains with orientation gradients and low-angle boundaries.
2. Thermal cycling causes dislocation activity and motion of low-angle boundaries that increase their misorientations.
3. Absorption of dislocations into low-angle boundaries leads to continuous recrystallization, which causes subgrain rotation, so that low-angle boundaries gradually develop into high-angle boundaries.

4. Discontinuous recrystallization develops in high-stress locations leading to high-angle disorientations.
5. Grain boundary sliding and differential CTE effects across high-angle/high-energy boundaries facilitate crack nucleation in some boundaries.
6. The stress concentration near a crack tip accelerates discontinuous recrystallization and crack percolation follows the discontinuous recrystallization path until failure.

The variability in the rate of microstructure evolution in solder joints arises from the combination of crystal orientations and joint location (boundary conditions). The 6-step process identified above was identified using a combination of destructive statistical measurements on packages cycled for particular times and from non-destructive characterization of particular joints after different numbers of thermal cycles from fabrication through failure. While the above sequence is generally descriptive of the process that takes place in any joint in any package, the rate of this evolution depends strongly on the design of the package and the specific starting initial microstructure. This is evident in the numbers of cycles to a characteristic life (defined using Weibull plot parameters) presented in Fig. 5.3. In the middle range of package/joint sizes, there is a distinct effect of pre-aging that is not significant for larger or smaller packages, which will be discussed further below. Thus, in any characterization of features described above, joints with different crystal orientations and boundary conditions will be at different stages of the overall process at a particular sampled time. In the sections that follow, specific examples of different stages of the process will be illustrated using joints from a variety of different packages cycled for various times. This description will close with some distinctions that arise based on different package designs [12–14].

Solidification and First Thermal Cycles

Upon solidification, rapid dendritic growth leads to formation of many defects, as low-angle boundaries are commonly observed within a given dendrite (e.g., Fig. 4.12). In tri-crystals, particularly those that form with greater undercooling, dendrites growing in non-<110] directions will bump into each other, which can bend them, and introduce low-angle boundaries (the orientation histogram of interlaced microstructures shows a spread of 10° on either side of 60° [15–17]). Upon solidification and subsequent cooling, the complex stress imposed by boundary conditions will introduce deformation, which can introduce additional dislocations that can arrange themselves into lower energy sub-boundaries. Figure 5.6a illustrates one example of a solder joint where the diffraction pattern exhibits a subtle change during the cooling process immediately following solidification. At 150 °C, the strong {420) peak shows a dominant peak and a few smaller peaks indicating the presence of a few subgrain boundaries. Upon cooling to 98 °C, a new peak just to the left of the dominant peak appeared, indicating that significant dislocation motion and

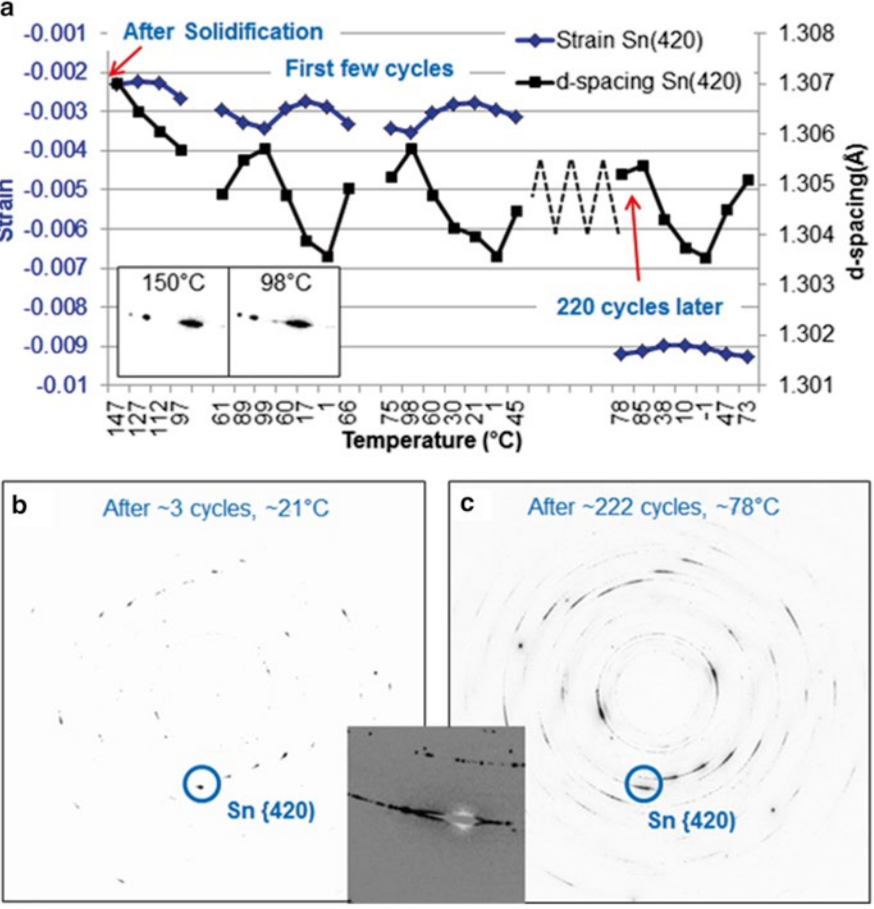


Fig. 5.6 Strain evolution from solidification to the first few thermal cycles in a WLCSP corner ball is correlated with temperature. After 222 cycles, the compressive strain on the Sn (420) plane became more negative after 222 thermal cycles. The inset between the diffraction patterns shows the difference between the two patterns, 222 cycles—3 cycles

recovery occurred as the sample cooled, resulting development of a sub grain [18]. During the first couple of thermal cycles, the internal strain on the (420) plane, tilted less than 15 degress from the interface, looked similar but the initial compressive strain became noticeably more negative and after 220 cycles.

Similarly, OIM maps from as-solidified joints show that there are significant orientation gradients within a given grain. Typically there are spreads of 5–10° in discrete pole figures and in diffraction spots (Figs. 4.4a, d, 4.6, and 5.6), which implies the existence of substantial lattice curvature or many differently oriented subgrains. With aging, the lattice curvature does not change in the overall sense,

though OIM maps show that after pre-aging, there are fewer sub-boundaries with higher misorientations, but this does not undo the overall spread in orientations present upon solidification (see pole figures for an aged joint in Fig. 4.5).

Subgrain Boundary Evolution

The X-ray diffraction pattern evolution shown in Fig. 5.6b, c shows that after 222 cycles from 0 to 100 °C with a 10 min dwell time, the peaks initially present are still the only peaks in the diffraction pattern, but they are much more spread out. The inset between the two diffraction patterns shows the initial <420] peak subtracted from the pattern measured after 222 cycles. The black spots represent new peaks resulting from thermal cycling. Close inspection shows that the apparent streaked peak is actually composed of discrete spots (see also the peaks in the next ring inside the main peak). This implies the presence of many well-defined subgrains with slightly different orientations.

Continuous and Discontinuous Recrystallization

The distribution of boundary disorientations with increasing number of cycles is illustrated in Fig. 5.7a for a low-stress 15 × 15 mm PBGA package with 1.0 mm pitch, but the evolution of low angle boundaries observed in Fig. 5.6 requires many more thermal cycles to obtain a similar level of microstructural change. The three curves indicate the evolution of the average disorientation from an OIM analysis of

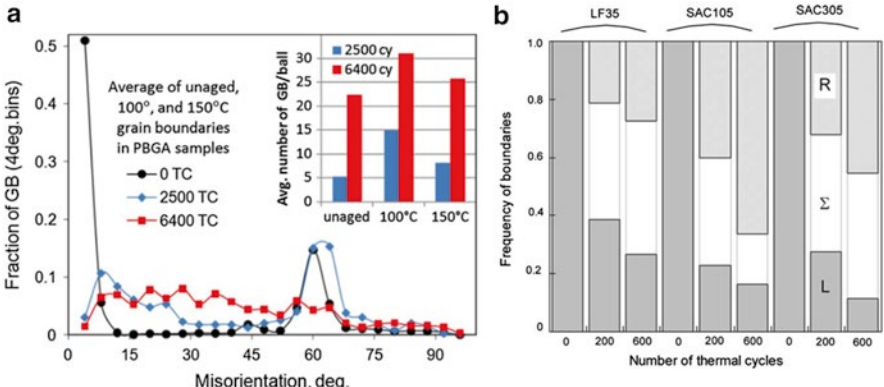


Fig. 5.7 The as-solidified disorientation histogram changes completely as continuous recrystallization develops in (**a**) PBGA package with 1 mm pitch [19], and (**b**) frequency of low (L), CSL (**Σ**), and random (R) boundaries on a WLCSP with 0.5 mm pitch [20]

14 balls in the middle two rows of a package. Initially, there is only a large fraction of low-angle misorientations indicated by the rapidly dropping black curve and solidification twin-related disorientations shown by the peak at 60°. After 2,400 thermal cycles, there are much fewer low-angle misorientations (none at the lowest angles, but a peak at 7°) and a broad spread of disorientations between 15° and 30°. The peak at 60° is more spread out (as the measurements are on different samples, the larger area under the 60° curve implies that there was either more twins present initially or that more twins formed during cycling). There is also a small peak near 80°, indicating that some highly misoriented grains formed by a discontinuous nucleation of a significantly different orientation. While the process of forming large disoriented grains is not clear, there is a strong elastic energy driving force to form grains with the opposite CTE behavior, to help mitigate the local stress state, and this can give a minority new orientation a driving force to grow [19]. After 6,500 cycles, the 60° twin peak spreads out significantly, and there are many high-angle disorientations over the full range of possible values. The number of grain boundaries increased with increasing thermal cycles, yet the number of low-angle misorientations diminished further. A study on a 10×10 mm WLCSP with 0.5 mm pitch on a 0.7 mm FR-4 board showed similar outcomes, as illustrated in Fig. 5.7b, where there were an increase in random boundaries and a reduction of special boundaries with increasing number of thermal cycles [20].

Continuous and Primary Recrystallization Mechanisms

The process of gradual increase in misorientations to become low-angle disorientations can be visualized in Fig. 5.8, where the new grains are clearly similar to the parent grain orientation in the center of the joint (where less strain hysteresis took place) [2]. With increasing distance from the interior toward the corner, the disorientation increases, and these rotations are typically about a <100] or a <110] axis. Such a rotation is a likely outcome of 001 direction slip, which is a facile slip direction that readily occurs on both {010) and {110) planes (see further discussion below). The presence of gradually changing orientations is a characteristic of continuous recrystallization, where dislocation absorption into a low-angle boundary gradually increases the disorientations until they become high-angle boundaries. This process clearly requires dislocation generation during the thermal cycling process, and from the simple analysis given above, there is sufficient strain to generate dislocations. Figure 5.8 also shows evidence for a discontinuous recrystallization process in the blue grains, where the stress concentration was largest at the location where the crack nucleated. There is no gradual difference in orientation between these blue grains and the surrounding green and orange grains. The mechanism of nucleation is not obvious from this sample but particle-stimulated nucleation of new orientations is a well-established mechanism to generate new orientations arising from localized lattice reorientation at dislocation pileups adjacent to particles [6]. Because this discontinuous process occurs later in the life of a solder joint, long

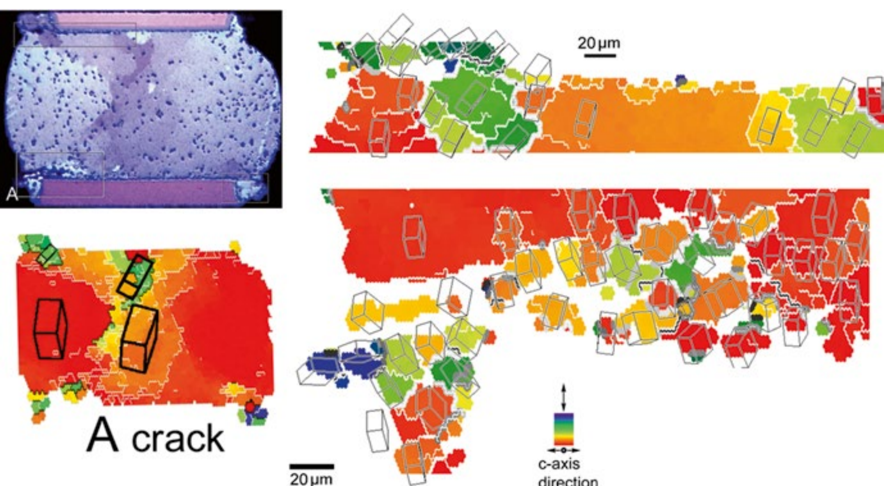


Fig. 5.8 Continuous recrystallization orientation gradients are commonly observed showing rotations about a 100 or 110 axis, related to slip in 001 directions [2]

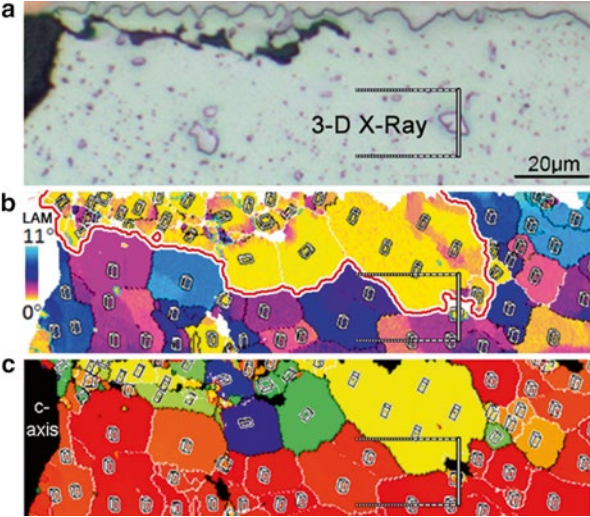


Fig. 5.9 Comparison of local average misorientation and c-axis maps in a regions where discontinuous and continuous recrystallization took place (the *red line* separates the two types of recrystallization) [8]

after continuous recrystallization is well established, enough time elapsed for significant coarsening of intermetallic particles. The coarsening rate of particles varies with distance from interfaces, as illustrated in Fig. 5.9a, where larger and more widely spaced particles are observed where microstructural evolution (and strain) occurs at higher rates [8].

Coarsening of precipitates is assisted by grain boundaries and dislocation pipes that connect particles. Temperature cycling also changes the solubility of Ag and Cu

in the Sn matrix, so at high temperature, precipitates will dissolve to some extent and put Ag and Cu into solution, and their transport is accelerated along dislocation pipes (diffusivity is also very fast along the Sn c-axis). With a decrease in temperature, the solubility decreases, and these solute atoms must reprecipitate. As the interfacial chemical potential of larger particles is lower due to the smaller curvature, they grow preferentially. With wider particle spacing, the mean free path of dislocations increases, so the likelihood for developing dislocation pileups against larger precipitates also increases with time.

Figure 5.9 illustrates the process of microstructural evolution at an advanced stage, where the crack is well established, and many discontinuously recrystallized grains are present. The boundary between the continuous and discontinuous recrystallization processes is made obvious in the c-axis map and the local average misorientation (LAM) maps. In the c-axis map, the parent red orientation shows crystal prisms with orientations that are similar to the parent red orientation at the bottom of the map. Some of the grains have an orange color, where the prism is rotated more than the surrounding subgrains delineated by white boundaries. The discontinuously recrystallized grains have distinctly different colors separated by black high-angle boundaries, indicating large misorientations from the parent red orientation.

In the LAM map, the gold/yellow color indicates that the deviation of any pixel in a grain is very small compared to the average value within the grain, and this implies that these grains have few defects and hence no defect content arising from geometrically necessary dislocations that cause lattice curvature. Thus, these grains are truly recrystallized. In contrast, the subgrains of the parent orientation have a variety of colors, due to the fact that the basis for comparison is the average of all of the subgrain orientations, so every subgrain has a distinct color. In both the discontinuous and continuous recrystallized grains, there are some locations with orientation (color) gradients. The gradients in the discontinuously recrystallized regions are close to the crack path locations. This implies that the grain recrystallized before the crack approached, so the intense straining just ahead of the crack tip was retained once the stress was relieved due to the passing of the crack.

Figure 5.10a shows the larger context of this joint in a CABGA package; this joint is the fifth ball from the corner. The green joint to the left also shows recrystallized grains that are not as well developed, probably due to the fact that a "green" orientation has a CTE in the vertical direction similar to the average CTE, so there is less driving force for microstructural evolution. A small subsurface part of the OIM scanned area identified in Fig. 5.9 in the red joint is examined in Fig. 5.10b and a "slice" of material tilted 45° from the surface was investigated using differential aperture X-ray microscopy (DAXM). This slice includes the interfacial region between the discontinuous and continuous recrystallization boundary. From the detailed analysis of the diffraction peaks, both orientation information and lattice strains arising from the internal stress state are quantified. The recrystallized (yellow) grain did not have much elastic strain present within, while the sub-boundaries in the continuously recrystallized (red) regions had much higher internal strains associated with them. Clearly, this elastic strain energy provides a driving force for migration of the discontinuously recrystallized grain to consume the "red" subgrains.

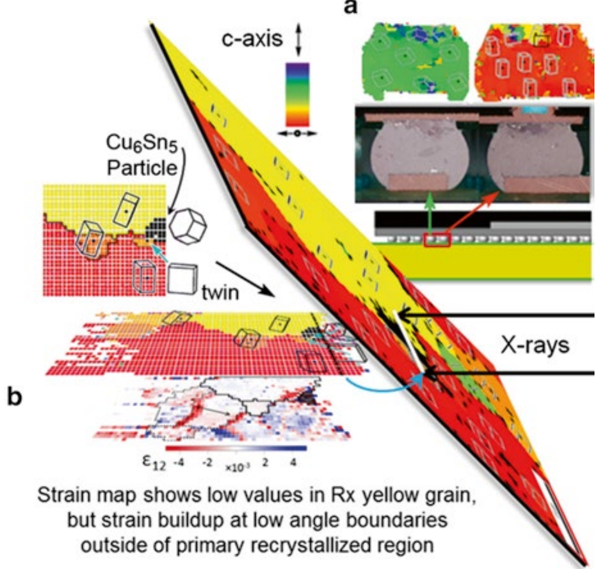


Fig. 5.10 (**a**) Two adjacent joints show differing magnitude of discontinuous recrystallization in solder joint in a CABGA package cycled to failure; (**b**) detailed investigation of the interface between discontinuous (*yellow*) and continuous (*red*) grain orientations shown in Fig. 5.9(**c**)

A portion of the 45° tilted plane in Fig. 5.10b focuses on the neighborhood around the large Cu_6Sn_5 particle (see Fig. 5.9a), which is at the triple junction between three grains (and is probably pinning grain boundary motion). A twinned orientation is adjacent below and to the left of the particle, which suggests one possible mechanism for forming a discontinuous recrystallization nucleus. As it is usually difficult to find the origin of discontinuously recrystallized grains or the particles that may have stimulated them, it is still unclear whether twinning plays a role in forming recrystallization nuclei.

Figure 5.11 shows a series of schematic diagrams indicating three stages of recovery/recrystallization that lead to crack nucleation and growth, which can be understood in the context of the descriptions above and similar discussion in [20–23]. At early time, strains are larger near the interface, and dislocations recover to form low-angle grain boundary networks. As precipitates coarsen with the aid of dislocation networks, smaller particles disappear, leading to less pinning of subgrain boundaries, which assists coalescence. As dislocations are pumped into the boundaries, they gradually become high-angle boundaries. In regions with the greatest strain energy, faster coarsening occurs, leading to conditions that facilitate particle-stimulated nucleation (or other processes) to form discontinuous nuclei. These nuclei are randomly oriented with respect to the parent grain due to the highly localized nucleation conditions, and these new grains grow to meet each other, forming grain boundaries with high-angle and high-energy disorientations. During thermal cycling, the differential CTE mismatch conditions at high-energy boundaries leads to sliding and formation of cavities in boundaries particularly at triple lines. Cracks form along high-energy boundaries to connect damaged locations between the discontinuously recrystallized boundaries.

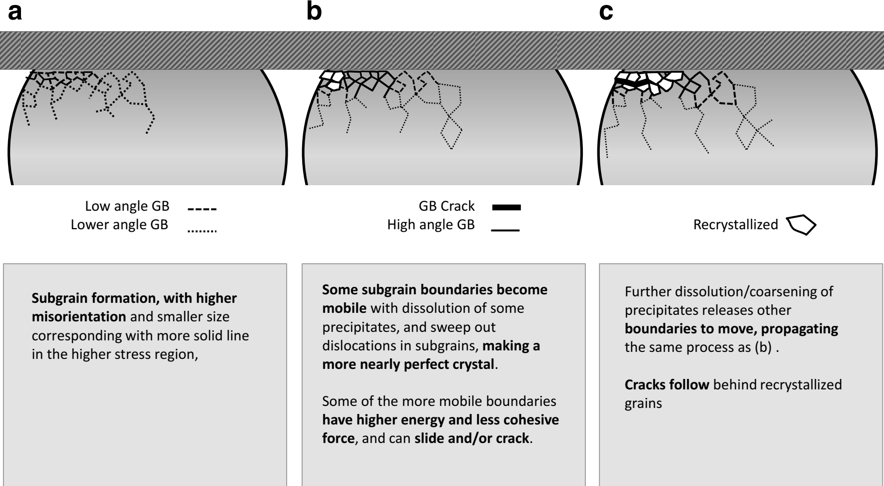


Fig. 5.11 Stages of continuous and discontinuous recrystallization in a single crystal solder joint

Low-Strain Versus High-Strain Packages Thermal Cycling Performance

The mechanism leading to crack initiation and propagation by subgrain boundary development can be observed as a general trend in various solder joints. However, the rate that this process occurs depends on the package design and configuration. It is not clear if the process outlined above is sufficiently general to account for very low and very high-stress package designs. Hence, the effect of package design microstructural evolution needs to be considered.

The correlation between the crack propagation, localized recrystallization area, and grain orientation is assessed in the four packages illustrated in Fig. 5.12, which shows the die size information and solder joint arrangement. A series of cross-section analyses are presented in Fig. 5.13 to identify. Crack propagation and orientation on the joints marked in red. The extent of crack propagation is directly correlated with the grain refinement or recrystallization area. The selected joints are also categorized into several stress–strain levels. For example, the two WLCSP corner joints experience the highest stress–strain during thermal cycling compared to the joints next to the corner. The joint position number is identified in Fig. 5.12 with respect to the magnitude of the shear strain, with position 1 having the highest amount of shear strain and 5 the lowest. The same categorization approach was used for the CABGAs with different die sizes and also the PBGA, which represents the lowest stress–strain package of the four. In the PBGA, the highest shear stress–strain joints are not at the package corners but under the edge of the die shadow, and hence they are labeled as position 1.

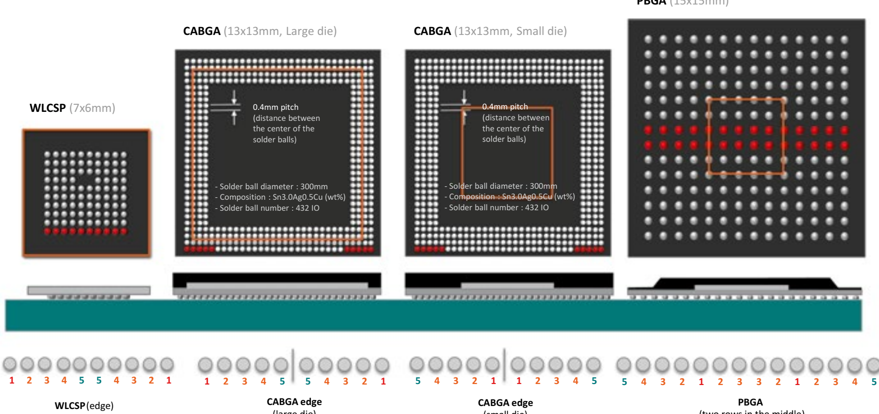


Fig. 5.12 Locations of joints examined with optical, electron, and orientation characterization in packages with high stress (WLCSP) to low stress (PBGA) designs. The position of the die is indicated with an *orange line*. The numbers beneath the ball positions that were investigate provides qualitative measure of CTE induced strain where 1 indicates highest strain and 5 lowest

After thermal cycling these samples to failure, samples that failed at cycle numbers close to the characteristic life were cross-sectioned for optical, SEM, and orientation imaging to document the existence and extent of cracks, the associated grain structure around the crack, and the grain orientation in the middle of the joints where less orientation change occurred. The thermal cycling lifetime is indicated in Fig. 5.3, and microstructural features are quantified in Fig. 5.13. The extent of cracking is identified using the red markers, which is consistent with the fact that the WLCSP samples have the highest stress–strain package design, and that the crack propagation at the corner solder joints is well developed. The associated recrystallized regions indicated in orange are also well distributed with a slightly larger recrystallized region in the corner joints (joints on the left side), which is expected since those are the most strained joints. With the CABGA samples, the larger die CABGA shows a higher crack propagation rate at the outer edge solder joints compared to the smaller die CABGA sample. Based on the test results using these sample configurations, the smaller die samples show the most extensive (and hence, first) failures at the inner edge row (location closest to the die edge) but with a longer life cycle number [12–14]. Compared to the WLCSPs and either large or small die CABGAs, the PBGA has a much smaller shear stress–strain condition during thermal cycling. Given the fact that PBGA samples have a larger solder ball size and pitch length (1.0 mm), the affected zones for both recrystallization and crack propagation were much more localized. Most of the solder joints in the middle of the package (rightmost columns) appear to be undeformed, as they maintained the original single- or triple-grain structure even after a high number of thermal cycles.

The grain orientation information (indicated by colors) from the comparison analysis shown in Fig. 5.13 is compared with the crack propagation length and the

Fig. 5.13 Selected joints examined after thermal cycling to failure close the characteristic cycle number with OIM and corresponding characterization of observed crack length (indicated by *red bars* on corresponding *grids*) and locations of recrystallized grains (indicated by *orange cells* on corresponding grids) for four different package designs with low (WLCSP) to high (PBGA) stress designs. The joint positions are presented in order from most stressed on the left to least stressed on the right for samples having three different aging conditions

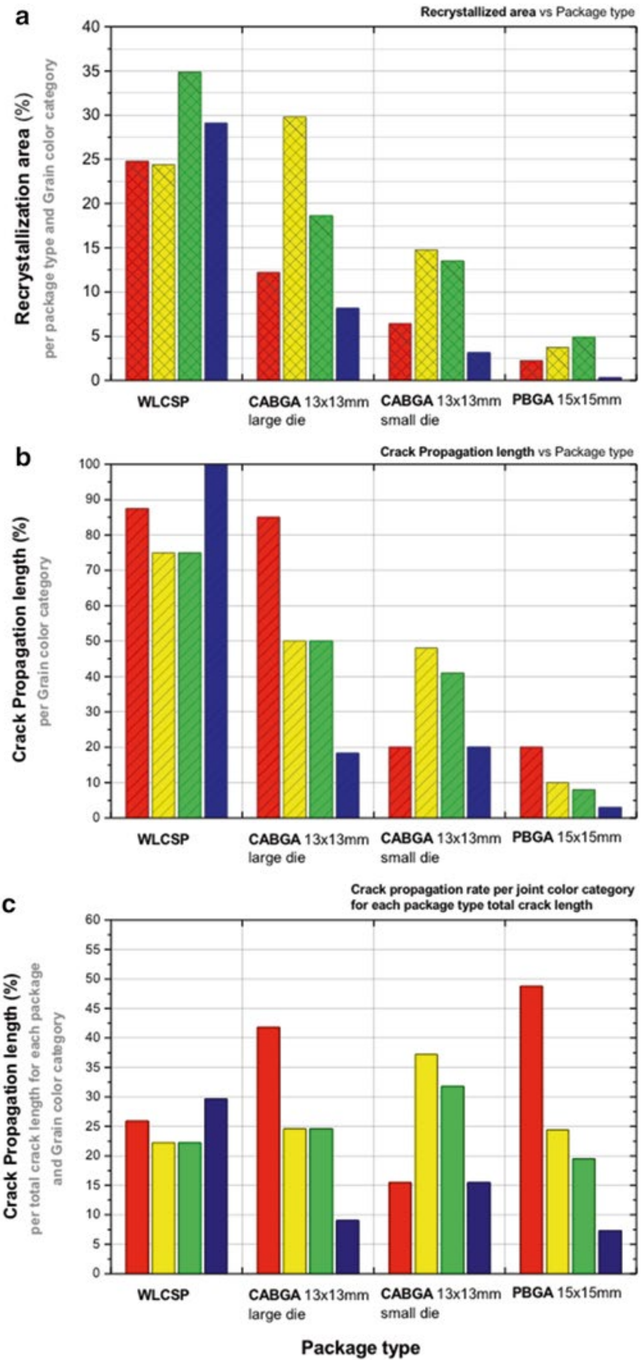


Fig. 5.14 Statistics from Figs. 5.12 and 5.13 for (**a**) area recrystallized and (**b**) cumulative crack length, and (**c**) the crack propagation rate per joint for each c-axis orientation group (color category) for each package design. The *bar colors* refer to approximate c-axis orientation in the dominant (parent) orientation in the joint

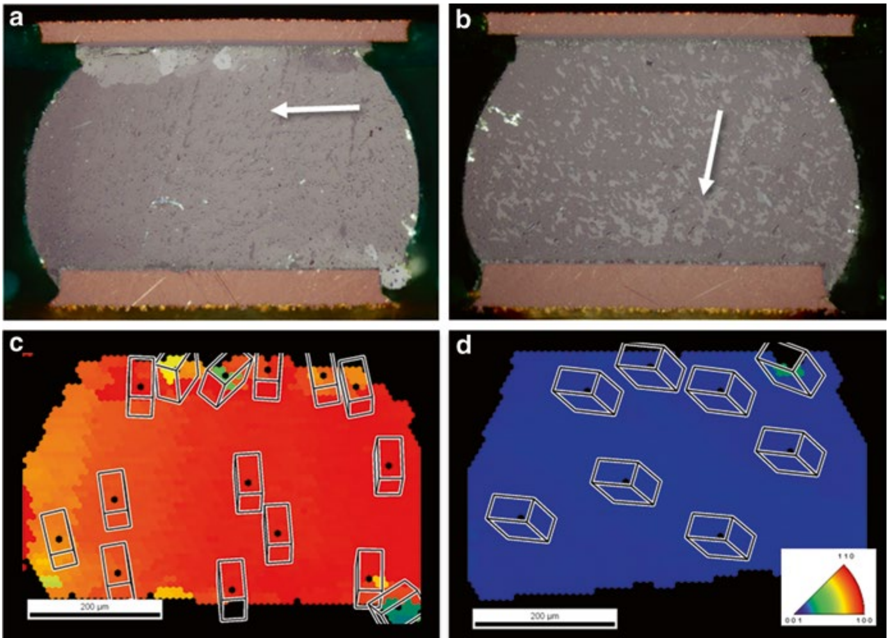


Fig. 5.15 Cross section of PBGA solder joints after 6,400 thermal cycles from 0 to 100 °C with 10 min dwell time and 10 min ramp times. Polarized light microscopy microstructure (**a**, **b**) and OIM orientation maps (**c**, **d**) associated with (**a**, **b**) respectively. (**a**) shows the crystal structure with the Sn grain c axis parallel to the package plane. (**b**) shows a crystal grain which has the c axis close to the package and board plane normal direction

recrystallized area in Fig. 5.14a, b. For the PBGA samples cycled 6,400 times from 0 to 100 °C, none of the blue single-grain solder joints show any indication of partial crack or crack initiation, and all cracks are formed in red, yellow, or green orientation solder joints [12–14]. Two solder joints in Fig. 5.15 from Fig. 5.13 show that the red joint shows crack initiation and propagation through the solder near the package-side interface, whereas the blue joint does not show any indication of crack development. The reason for this difference can be explained beginning with the linear coefficient of thermal expansion (CTE) along the [0 0 1] axis (c-axis), which is about twice the value along the [1 0 0] and [0 1 0] a-axes as shown in Fig. 4.2. As the coefficient of thermal expansion (CTE) is very anisotropic (Fig. 4.2), the color code used in Fig. 5.15 is correlated with the magnitude of the CTE perpendicular to the board. When the c-axis is parallel to the package plane, it is referred to as a "red-oriented" joint. If the c-axis is highly inclined to the package plane, as shown in Fig. 5.15d, it is a "blue-oriented" joint. For the red-oriented joints, the CTE in the interfacial plane is ~30 ppm/K in one direction and ~15 ppm/K in the other (perpendicular) direction. This causes a small CTE normal to the board but a highly varying CTE parallel to the substrate. On the other hand, blue-oriented joints have an isotropic low CTE of ~15 ppm/K in the interfacial plane, which is close to the CTE of

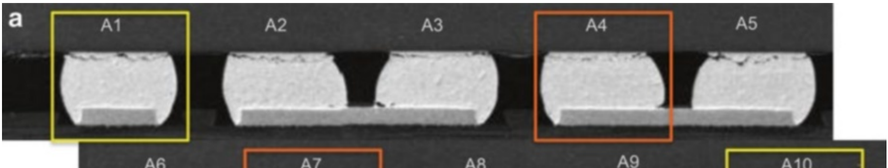


Fig. 5.16 Cross-sectioned SEM images of WLCSP joints with corresponding OIM maps. (**a**) SAC305 solder joint as-assembled and thermally cycled, (**b**) OIM images overlaid on cross-sectional SEM images in Fig. 5.16a. A1 and A10 are the corner solder joints of the WLCSP

board, but the CTE perpendicular to the board is very high. Similarly, the Young's modulus along the c-axis is about three times larger than that along the a- and b-axes (Fig. 4.2). If all of the joints in a package have random crystal orientations, then the thermal displacement of the package follows the average CTE of Sn. Compared to the average CTE, the red-oriented joints are in tension and the blue-oriented joints in compression at high temperature, and the high stiffness of the blue joints push up on the package with more force than the red joints. Hence, due to the high compliance of red joints, there is a greater magnitude of elastic strain in tension in red joints than compression in blue joints. As cracks are often observed in red-oriented orientations, such as the upper left corner of the joint in Fig. 5.15a, it is apparent that damage is generated preferentially in conditions of tension at high temperature. The large CTE difference in the interface plane of red joints also causes a Mode II stress state that is combined with the normal tensile stress.

In contrast to the low stress–strain conditions on PBGA samples, the recrystallized area develops in a larger area in the higher stress–strain CABGA packages. The larger die sample shows more active recrystallization at the corners when the dominant orientation is red and the crack propagation is the greatest. But in the recrystallization and grain orientation correlation plots in Fig. 5.14, the red joints show less recrystallized area than the yellow/orange and green joints. This implies that red joints do not need to have large area of recrystallization to facilitate crack propagation, whereas green and yellow/orange joints require a larger extent of recrystallization to generate a crack. Hence, crack propagation during thermal cycling is easier in red joints than other orientation joints.

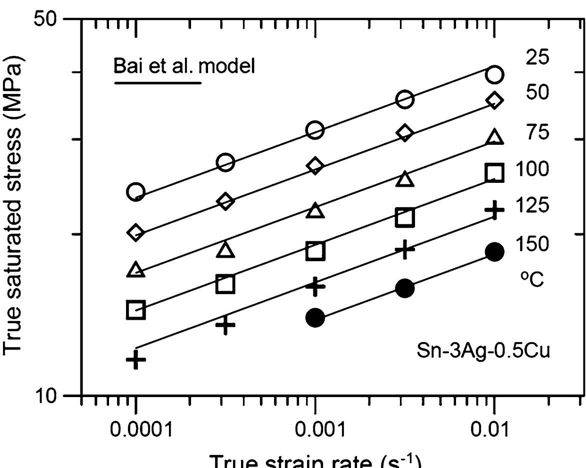
The same red versus blue joint phenomenon can be observed in the high-strain WLCSP samples. The WLCSP samples show very active recrystallization development and also a fast crack propagation rate. WLCSPs are considered a relatively short lifetime package during thermal cycling because of the high CTE mismatch [12]. The images in Fig. 5.16 are selected joints taken with optical microscopy overlaid with OIM scanning images. Joints A1 and A10 (marked by yellow boxes), which are the corner joints for the edge row in Fig. 5.12, can be considered joints that experienced the same strain during thermal cycling due to their location. Both solder joints are located at the corner, but, as shown in Fig. 5.16, they have a full crack and partial crack, respectively. The OIM maps shown in corresponding positions with the optical images reveal that the Sn grain orientation for joint A1 is a "red-oriented" structure and A10 a "blue-oriented" structure. Combined with the

crack propagation level in each joint, it is possible to determine that the red-oriented grain structure has a faster crack propagation rate compared to blue-oriented grain structures. The same comparison can be established between joints A4 and A7 in Fig. 5.16 (highlighted by orange boxes). Both joints are located near the middle of the package, four joints inward from the corner. Again, the red-oriented joint showed the full crack compared to the green-oriented joint, which showed a partial crack near the package-side interface inside the solder. Consistent with observations in other package designs, the red-oriented joint is more sensitive to crack initiation and propagation. Compared to these red-oriented joints, green- and blue-oriented joints need to reorient their c-axis to propagate the crack, which requires grain rotation or recrystallization during the process. If the internal stress developed during thermal cycling is not enough to deform the solder joint, the process of crack initiation and propagation will be very slow or may not even occur. For example, if the blue joint at A10 experienced a stress that is not sufficiently high to generate plastic deformation that can locally rotate the subgrains to become recrystallized near the package-side interface bulk solder, the crack will not develop.

The resistance of blue joints to deform suggests that blue joints will not fail during thermal cycling. Compared to the PBGA samples, which have no crack propagation in blue joints, the WLCSP has a high rate of crack propagation even in blue joints. Regardless of the grain orientation, the crack propagation and recrystallized area show a fast development, due to a higher amount of deformation during thermal cycling compared to other package types. This means that the strain produced during thermal cycling of the WLCSP is already over a threshold that causes crack initiation and propagation for any joint. Thus, the relationship between grain orientation and stress will also depend on the strain rate, and these relationships will be examined for high strain rate deformation in Chap. 6. In Fig. 5.14b, in conditions where the grain orientation matters, the rate of recrystallization is faster for green and yellow joints than red and blue joints, but this reverses for the WLCSP condition where a strain threshold is exceeded. Thus, a model that describes this process is not quickly identifiable.

Simulating Deformation of Solder Joints with Crystal Plasticity-Based Constitutive Models

From the prior discussion, it is clear that different package designs impose different stress–strain histories on solder joints and that the history varies with position in the package. Therefore, the only practical way to develop predictive capabilities is to develop material models capable of simulating realistic boundary conditions on the two joint interfaces, with constitutive models that incorporate the temperature-dependent anisotropic elastic, CTE, and plastic properties. Further refinements of such models would include effects of Joule heating arising from current stressing superposed with the thermomechanical displacement history. However, material models that have these capabilities are computationally expensive, so that only a



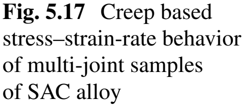


Fig. 5.17 Creep based stress–strain-rate behavior of multi-joint samples of SAC alloy

few joints can be practically modeled concurrently. Thus, practical modeling requires two steps of analysis, the first simulation at the overall board level, where each joint in the package is modeled with a very simple material model representing average solder properties. From this result, the temperature–displacement history can be extracted for selected joints and then be used as a boundary condition for a more detailed model with full anisotropic properties [24]. The former part is routinely done by manufacturers during the final design process for a mass-produced circuit board. The latter part at the individual joint level requires development of a crystal plasticity constitutive model that has properties that can evolve.

An evolving crystal plasticity model does not yet exist for Sn-based alloys, although components necessary for such a model are available in the literature, such as the evolution of stress with aging of precipitates [e.g., 25, 26]. One aspect of a comprehensive model is well established for average properties, to identify the temperature–strain rate relationships, such as shown in Fig. 5.17 [27] for creep data. Such data can be modeled with the Norton equation,

$$\dot{\varepsilon} = A\sigma^{n} \exp\left(-\frac{Q}{RT}\right) \tag{5.1}$$

where $\dot{\varepsilon}$ is the strain rate after the primary transient is exhausted, σ is the applied stress, n is the stress exponent, and Q is the activation energy of the rate-limiting mechanistic process that limits deformation (RT is the gas constant and temperature in K). This equation is commonly used for interpreting deformation mechanisms in uniaxial or shear tests where stress does not need to be expressed as a tensor. It is also common to express the stress in terms of strain and strain rate in the following equation, which is related to Eq. 5.1 with variables having the same meaning,

$$\sigma = K \exp\left(\frac{Q}{nRT}\right)\dot{\varepsilon}^{1/n}\varepsilon^{h} \tag{5.2}$$

which also includes the evolution of strain ε raised to the power h to describe how hardening develops with strain, where h is a hardening exponent. Furthermore, the constants A and K represent microstructural state functions which evolve in Sn-based solders, and such functions are complex, as the changing resistance to dislocation motion due to coarsening of precipitates requires A to increase with time/temperature history [25, 26], (and K must correspondingly decrease) as the solder microstructure becomes softer.

While these equations provide a means to express mechanism-based knowledge (specific values for Q and n are indicative of particular mechanisms), they are scalar expressions, which cannot express the tensorial nature of what really occurs in a solder joint. In a real solder joint, the stress state varies with position, and thus the rate of microstructural evolution at each position within a joint varies according to the specific local stress–strain history. Thus, Eq. 5.2 needs to be expressed in an incremental way for a given element in a finite element formulation, and the increment of strain must be the sum of shears on each of the slip systems that operate. This is accomplished with the following expression that describes how the slip resistance τ on a given slip system β evolves with the shear strain rate (increment):

$$\dot{\tau}^{\beta} = \sum_{\beta=1}^{N} h_0 \left|1 - \tau_y^{\beta} / \tau_s^{\beta}\right|^{a} \left|\dot{\gamma}^{\beta}\right| \qquad (5.3)$$

where there are N slip systems to consider. The variable h_0 is the initial hardening rate, a is an exponent that defines the curvature of the hardening rate, τ_s^{β} is a saturation value for the shear stress, τ_y^{β} is the current yield stress. The stress tensor σ is then a function of the convolution of each of the increments of $\dot{\tau}^{\beta}$ on each slip system, which depends on the amount of shear that occurred on each of the slip systems $\dot{\gamma}^{\beta}$. For a useful model, the shear strain rate in Eq. 5.3 needs to be a function of the prior stress and temperature expressed in a manner similar to Eq. 5.1. This simple

Table 5.3 Slip systems of interest in deformation of Sn [44]

Mode	Slip system	Number in family
1	{100)<001]	2
2	{110)<001]	2
3	{100)<010]	2
4	{110)<1-11]/2	4 (like BCC)
5	{110)<1-10]	2
6	{100)<011]	4
7	{001)<010]	2
8	{001)<110]	2
9[a]	{011)<0-11]	4
10	{011)<100]	4
11	{011)<1-11]/2	8
12[a]	{211)<0-11]	8
13[a]	{211)<–111]/2	8

{hkl)<uvw] recognizes tetragonal crystal symmetry
[a]Opposite directions are not equivalent [44]

hardening model does not consider latent hardening effects, where a slip on one system hardens another. Further description of a suitable modeling strategy can be found in [28–35].

The effectiveness of such models depends on knowledge of the slip resistance on different slip systems. Table 5.3 lists 13 families of slip systems that have been discussed in the literature. They are arranged in an order that roughly indicates their likelihood of operation. For example, slip systems having a slip vector along the c-axis (e.g., on {110) planes, denoted as {110)[001]) are known to be easily activated. This table is based upon single-crystal experiments on pure Sn discussed by Fujiwara, Düzgün, and others [36–41]. However, solder alloys have additional microstructural constituents such as intermetallic particles and alloying elements in solution, so this list is not necessarily sufficient for solder alloys, but it provides a starting place for comparative work. In examinations on solder joints by Zhou and Darbandi [34, 35, 42], slip systems 3, 6, and 9 seem to be less facile, particularly if other slip systems are able to operate more easily. In shear, the number of slip systems that have been observed to be active depends on the c-axis inclination as described by Darbandi [43]. These tentative outcomes result from analysis of previously polished sample surfaces after shear deformation, where slip bands can be observed and compared with Schmid factor analysis and crystal plasticity simulations [43].

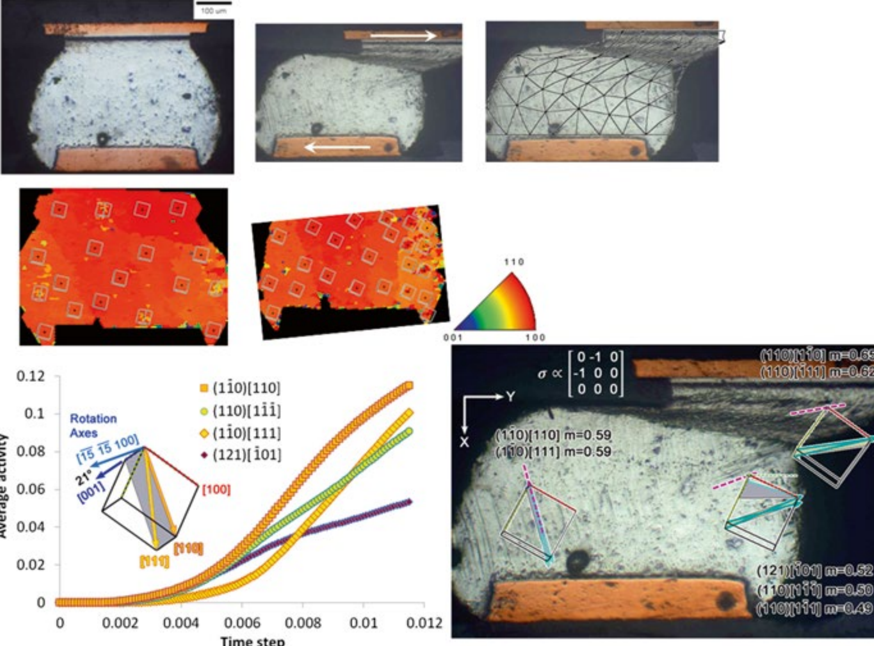


Fig. 5.18 Experimental characterization of shear deformation of a single crystal joint, showing how is localized at the *top*. Orientation analysis shows that slip on the most active slip systems modeled account for the observed rotations. Schmid factors were computed based upon simple shear boundary conditions

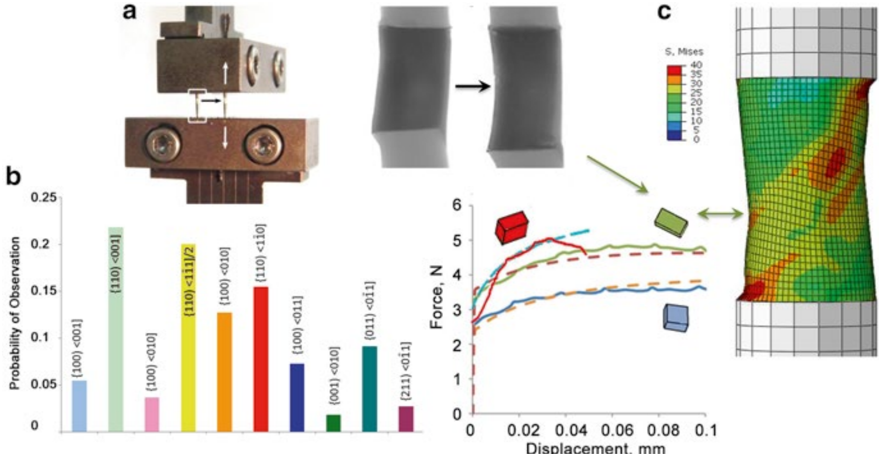


Fig. 5.19 Tensile tests on 0.5 mm diameter SAC305 single crystal joints (**a**) were combined with observations of slip systems in shear samples (**b**) were used to constrain calibration of a crystal plasticity finite element model against the *blue* and *green* orientations (**c**). The simulation of the *red orientation* was made with the model based upon the other two. *Dashed lines* are FEM model based on values in Table 5.2, and *solid lines* are experiment. Radiographs (**a**) show shape before and after deformation

Figure 5.18 shows how a crystal plasticity based finite element model can accurately represent the heterogeneous strain that develops in solder balls during room temperature deformation, where dislocation slip dominates the deformation process. The slip systems active in the simulation are the same as those observed by slip traces on the surface. While the kinematic agreement is good, optimization of the stress evolution in the model is a currently active topic. A recent estimation was made using two stress–strain tension experiments on 0.5 mm diameter single-crystal SAC305 joints deformed at room temperature at a strain rate of ~0.001/s (Fig. 5.19a). The critical resolved shear stress and hardening parameters for Eq. 5.3 in Table 5.4 were obtained by constraining the relative amounts of slip activity by quantitative observations in 32 shear test joints similar to Fig. 5.4a in the histogram in Fig. 5.19 [43]. Based upon the fit from two samples, the stress–strain behavior was adequately predicted for a third joint (until instability set in, solid red line in Fig. 5.19c). These critical resolved shear stresses have a similar relative rank of ease of operation as that obtained from first principles density functional theory simulations of slip systems described in [44] for computationally pure Sn; though fewer slip systems were considered in the experimental study, only two slip systems show significant differences from the theoretical study (noted in bold in the rank lines of the table). These differences could arise from alloying elements in the experiment and potentially incomplete assessment of slip system activity in a limited set of experimental data. Nevertheless, this shows that mesoscale modeling within the joint can be accomplished effectively.

Table 5.4 Critical resolved shear and saturation stress values (MPa) with $a = 2$ and $h_0 = 75$ in equation p3

Slip system	1 {100)<001]	2 {110)<001]	3 {100)<010]	4 {110)<1-11]/2	5 {110)<1-10]	6 {100)<011]	7 {001)<010]	8 {001)<110]	9 {011) <0-11]	12 {211)<0-11]
rank	7	**1**	8	2	4	**3**	6	10	5	9
[44]	7	**9**	12	2		**13**	5	10	1,15	6,14
τ_0	8.5	4.3	10.4	4.5	5.6	5.1	7.4	15	6.6	12
τ_S	11	9	11	9	10	10	10	16	9	13

Note Slip systems 10, 11, and 13 were not considered in the experimental analysis

Isothermal Aging Effect on Thermal Cycling

In recent studies, it was reported that the thermal aging effects are more severe for Sn-based Pb-free solders than for eutectic Sn–Pb solder alloys because the microstructure changes dramatically during thermal aging [45–47]. As shown earlier in Fig. 4.14, the Sn+Ag_3Sn eutectic solidification zones begin to coarsen, forming Ag_3Sn precipitates that grow from an average size of 0.6 μm to around 3 μm after 1,000 h of aging at 150 °C, and cause a hardness decrease from 17.5 H_{Knoop} to 12.5 H_{Knoop}. This decrease of hardness alters the mechanical and thermal stability of the joint. Along with the bulk solder microstructure evolution, the interface IMC layer also grows (see Figs. 4.14–4.17), implying that aging mechanisms take place in the interfacial region too.

The experimental and analytical findings show that the aging effect on the thermal cycling life depends on the package type, pitch size, and solder alloy metallurgy (Fig. 5.3). The internal stress in each package design is an additional crucial factor. Higher stress package designs show a more severe aging degradation in fatigue; however, with increasing stress in the package design, there seems to be a threshold window outside of which no isothermal aging effects are apparent, as suggested by the data in Fig. 5.13. Also, the grain structure evolution from single to multigrain development and its influence on thermal cycling performance has been investigated. As SAC105 and SAC305 have different amounts of Ag_3Sn, the structure transformation can affect the individual joint stress state in addition to the chemical gradient and IMC precipitation effects. The combination of various factors that occurs during thermal cycling microstructure evolution will be examined further. The correlations between microstructure evolution and thermal cycling performance are examined first, by following the structure development during aging, and the role of the interface region on thermal cycling performance will be considered next.

Effect of Isothermal Aging on Grain Structure Distribution

Solder joints composed of Sn–Pb alloys deform in a relatively uniform manner as illustrated in two joints deformed in shear (Fig. 5.20). The shear deformation was uniform regardless of aging conditions as indicated by the similar shape of joints in Fig. 5.20a for the unaged and Fig. 5.20d for the aged condition. In contrast, SAC305 joints deformed in the same way, shown in Fig. 5.4, have distinctly different deformation characteristics, because unlike Sn–Pb solder joints, lead-free solder alloys tend to be mostly single crystals with strongly anisotropic thermal expansion and plastic deformation characteristics. Solder joints with different crystal orientations will have significantly different tensile, compressive, and shear characteristics, giving each lead-free solder joint in a given package unique mechanical properties.

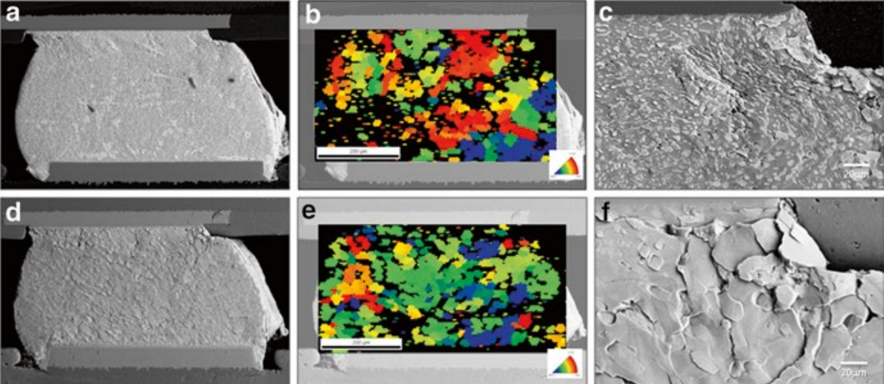


Fig. 5.20 SEM images of (**a**–**c**) Sn–Pb solder joints after shear in the unaged (**a**–**c**) and aged (**d**–**f**) conditions. The OIM c-axis maps show that the Sn grain orientations tend to be random

With aging, the properties of the joint will change. A relatively simple approach to reveal patterns in the grain structure evolution is to categorize each solder joint based on its polarized image. As shown in the key of Fig. 5.21, each solder joint was assigned to one of five categories: (1) single-grain structure, (2) nearly two-grain structures (mainly a single grain with small fractions of a second grain orientation structure), (3) two-grain structures, (4) nearly three-grain orientation structures (two strong grain orientations with an additional small fraction of a different grain orientation structure), and (5) three-grain orientations (either a clear beachball structure or more than three grains). Figure 5.21 presents a spatial presentation of how the categorized grain structure distribution differs after thermal cycling on unaged and aged samples. The fraction of single crystals is smaller in the samples with higher aging temperature and more thermal cycling. Figure 5.22 shows how the fraction of single crystals changes for several conditions, which generally implies that single crystals are likely to change into multi-crystals with time, temperature, and thermal cycling. Even aging of as-assembled samples without thermal cycling resulted in a decrease in the fraction of single-grain solder joints by about 10 %.

The decrease in the fraction of single-grained joints is related to the accumulation and coarsening of precipitates within the bulk solder, which are less effective in pinning the Sn subgrain boundaries as they grow larger. The coalescence of unpinned, low-angle grain boundaries leads to low-angle boundaries with larger crystallographic misorientations, which precedes the formation of higher angle mobile grain boundaries that brings the transformation of single-grained structures to multigrained structures. Also, depending on the stress state and change in crystal orientation, a minority orientation can grow into the larger grains by an incremental recrystallization and grain growth mechanism driven by the release of elastic strain energy [19], where a minority grain with lower elastic energy with respect to the more globally imposed stress state has an energy advantage that promotes it growth.

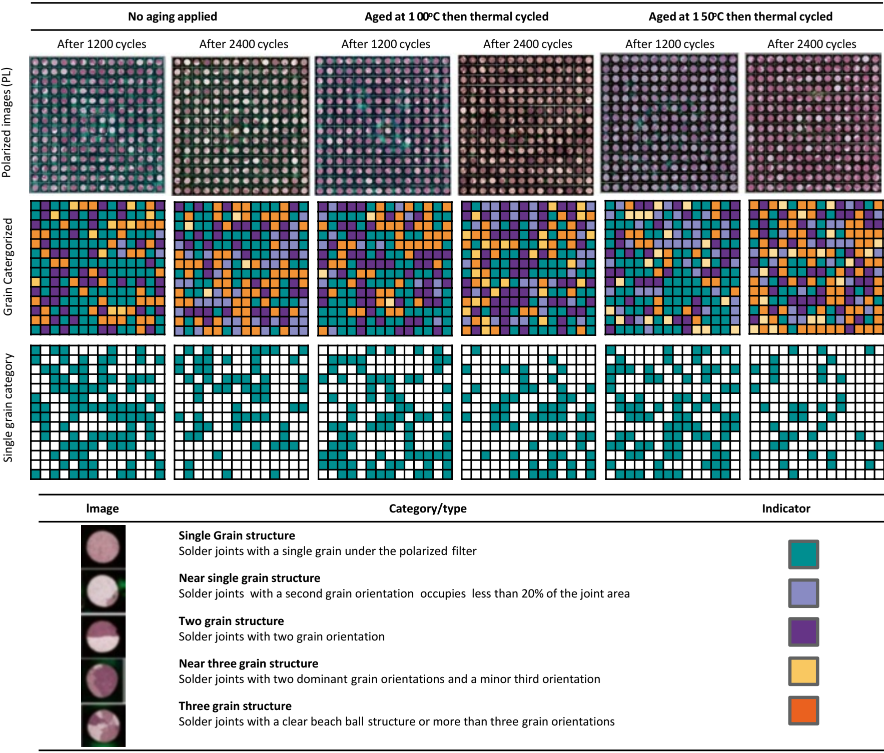


Fig. 5.21 Distribution of solder joint grain structure types with respect to pre-aging and number of thermal cycles in a PBGA package design. The single grain fraction decreases in numbers, indicating how cycling favors breakup of single crystal joints, especially in highly aged microstructures

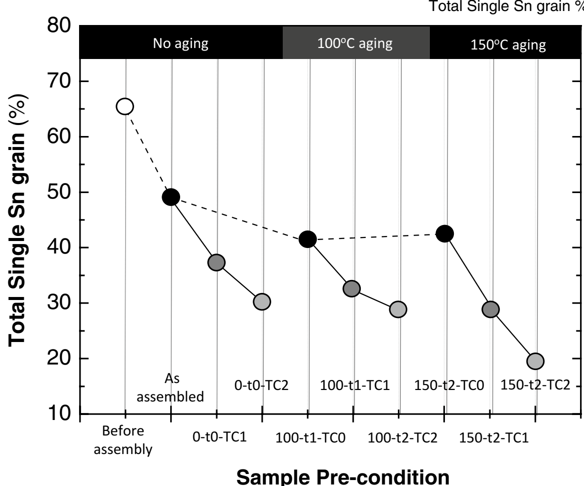


Fig. 5.22 Distribution of solder joint grain structure types with respect to pre-aging (and number of thermal cycles in a PBGA package design based on the data in Fig. 5.21. The abbreviations 100-t1-TC1 refers to aging at 100 C for 500 h, and cycled 1,200 times. Similarly 150-t2-TC2 refers to aging at 150 °C for 1,000 h, and cycled 2,400 times

Effect of Aging on Thermal Cycling Damage Generation

The effect of developing of larger grains with higher misorientations in aged microstructures on thermal cycling damage generation is assessed in PBGA damaged regions in samples with different amounts of aging shown in Fig. 5.23. The moderate 100 °C aging condition led to the greatest amount of crack propagation, about twice that in the unaged or overaged conditions, indicating that the size and spatial distribution of precipitates have a large effect on damage generation. This can be understood in that the unaged sample had finer particles that restricted boundary motion, and hence, recrystallization. With very large particles, recrystallized grains became large, and hence, fewer boundaries were susceptible to cracking. The intermediate particle size distribution had sufficient pinning power to make recrystallized grains smaller, so that with more boundaries available, more cracking could occur. Also, this shows that different c-axis orientations have different sensitivity to crack propagation tendencies, where "red" joints with the c-axis nearly parallel to the substrate had a smaller fraction of intact boundary length than green and yellow orientations, so red orientations are the most vulnerable to cracking.

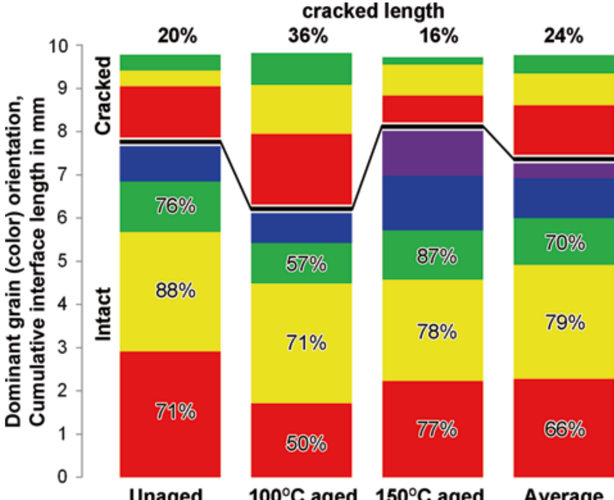
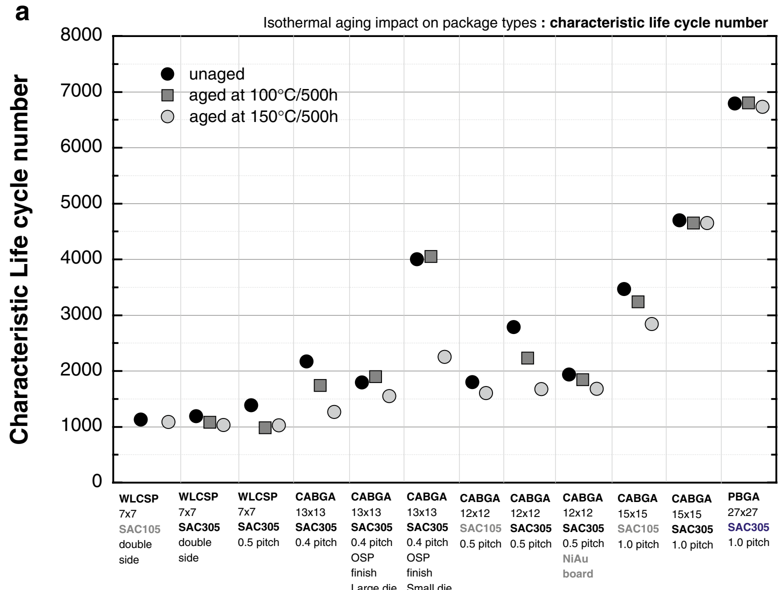


Fig. 5.23 Effect of aging and particle size on development of recrystallized grains and crack length in thermally cycled PBGA samples sectioned to show the cross section (28 joints; see also the data in Fig. 5.7). The 100 °C age led to the greatest amount of cracking. The cracked length percentages above indicate the fraction of the cumulative interface cracked length, and the percentages within the *colored bars* indicate the fraction of the intact length for all color orientations in the group; *red* always has the smallest fraction of intact interface length (i.e. largest cracked fraction) and *yellow* the largest (least cracked)

Isothermal Aging Effect in Various Package Designs

The effects of isothermal aging on the characteristic lifetimes for the samples described in the prior sections are presented in Fig. 5.24, showing various levels of degradation ranging from 0 to 40 %. A general trend can be seen when various package types are compared. The highest percentage of degradation due to aging occurred in mid-stress CABGA packages. In contrast, the low-stress PBGA and high-stress WLCSPs with SAC305 show almost no effect of aging on degradation. To gain understanding of why the mid-range design is sensitive to prior aging, the microstructural evolution in samples with and without isothermal aging is examined in more detail in Fig. 5.25. The initial microstructure state shows typical single- and tri-grain structure. By comparing thermally cycled samples, the amount of active grain refinement and recrystallization differs with and without aging. The unaged samples show only two solder joints from the corner region with well-established recrystallization, but the aged and thermal-cycled sample shows overall recrystallization in all five solder joints. Based on these observations, the degree of coarsening of precipitates, a variation that existed prior to thermal cycling, affects the rate of recrystallization during thermal cycling (and it also depends on crystal orientation). All CABGA packages in this series show the same phenomena: After aging, a higher creep rate will occur with coarsened IMC precipitates [5, 12] that do not pin the dislocations or grain boundaries as effectively. The higher creep rate in aged (softer) solder joints allows more strain or plastic deformation for a given stress, and strain accumulation provides the driving force for recrystallization (by either continuous or discontinuous mechanisms) that causes grain rotation during thermal cycling.

In contrast, with a high stress and strain package design such as the WLCSP, all of the solder joints experience a rapid transition to multigrain structure and recrystallization, showing little variation between the most highly stressed corner and lower but still highly stressed solder joints along the edge. In contrast, for the low-stress PBGA design, the aging process proceeded faster than the transformation into recrystallized regions, so the advancing crack stimulated recrystallization more than recrystallization stimulated cracking. Thus, microstructural evolution conditions that led to the critical failure condition of a nearly completed crack were similar even if the accumulated crack length varied with aging conditions. But with an intermediate level of stress design, the difference in the stress needed to generate sufficient strain for recrystallization to take place can be strongly affected by aging preconditions.



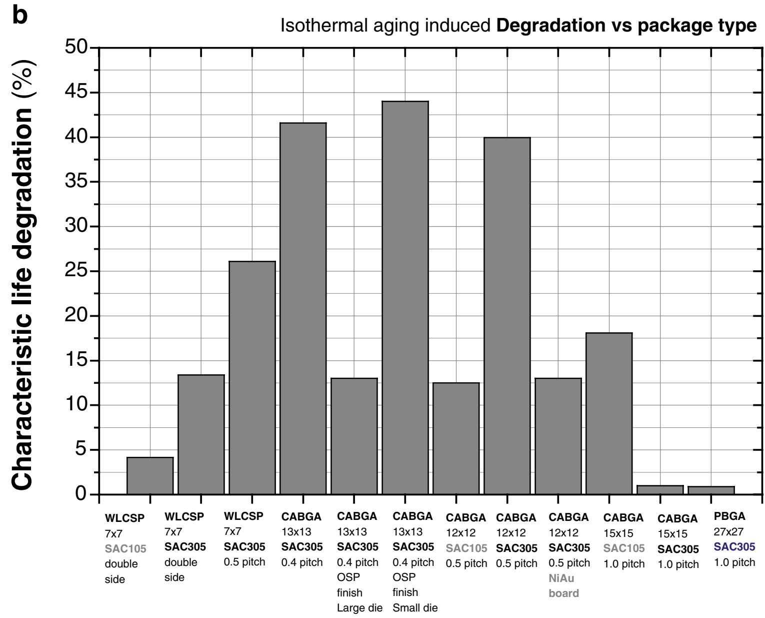


Fig. 5.24 (**a**) The effect of package size and design on characteristic life during accelerated thermal cycling tests. (**b**) The maximum degradation percentage per package type. Aging has little effect on life times for the highest stress and lowest stress designs. When the lifetime is between 1,000 and 4,000 cycles, then the prior aging degrades the lifetime by as much as a factor of 2. All components were board-assembled on 2.4 mm thick (93 mil), high glass transition temperature (T_g), FR4-printed circuit boards featuring Cu pads with organic surface preservative (OSP) surface finishes, unless noted otherwise

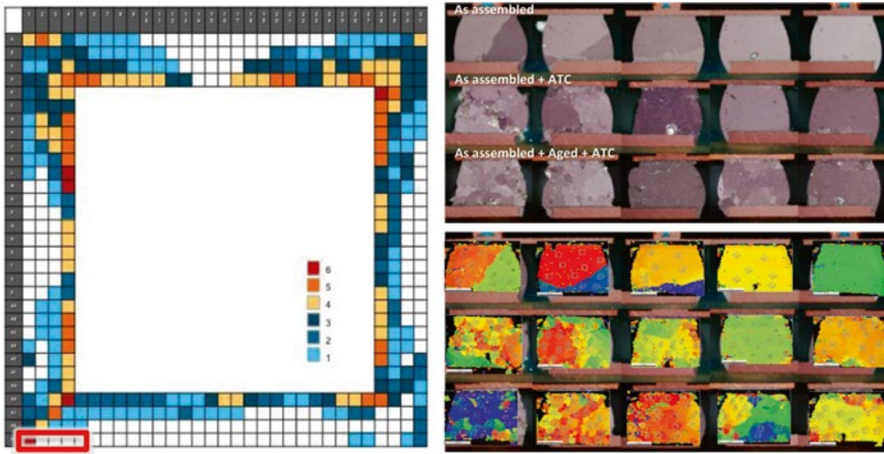


Fig. 5.25 Large die 13×13 CABGA package with 0.4 mm pitch showing the frequency of failure at each position from dye and pry assessment due to accelerated thermal cycling (ATC) of 6 samples, and the microstructure state in the five *balls* close to the outer corner

Effects of Aging and Interface Metallurgy on Thermal Cycling Performance

A series of experiments with different chemical gradients inside solder joints and different aging conditions were examined after thermal cycling to failure to assess the effect of surface finish on the thermal cycling performance. As discussed in Chap. 4, different solder alloy reactions with the surface finish and the presence of chemical gradients lead to different interface layer microstructures, as illustrated in Fig. 5.26. A 13×13 mm 0.4 mm fine-pitch CABGA component was used to compare OSP/SAC305/OSP and NiAu/SAC305/OSP interface combinations, and a 12×12 mm 0.5 mm pitch CABGA component was used for comparing NiAu/SAC305/OSP and NiAu/SAC305/NiAu interfaces. Both test vehicles used 2.36 mm (93 mil) boards. In Fig. 5.26, the initial and after aging microstructures for each selected interface combination are shown for these SAC305 joints. Figures 5.27 and 5.28 consider how these different conditions affect thermal cycling performance.

Figure 5.26 shows the OSP/SAC305/OSP as-assembled typical scallop-type IMC morphology, which grew to a thicker smooth IMC layer with a thicker developed Cu_3Sn layer after aging, due to the abundant source of Cu flowing into the bulk solder during reflow and during aging (left column). There are a smaller number and larger size IMC precipitates after aging near the interface, with a similar distribution on both the board and package sides. As Cu can flow into the joint system freely from both sides, a balanced Cu concentration joint structure develops.

For the NiAu/SAC305/OSP combination structure shown in the middle column of Fig. 5.26, the Ni changes the IMC geometry to a finer needle shape for both the package- and board-side interface. As the solder joint diameter is around 300 μm,

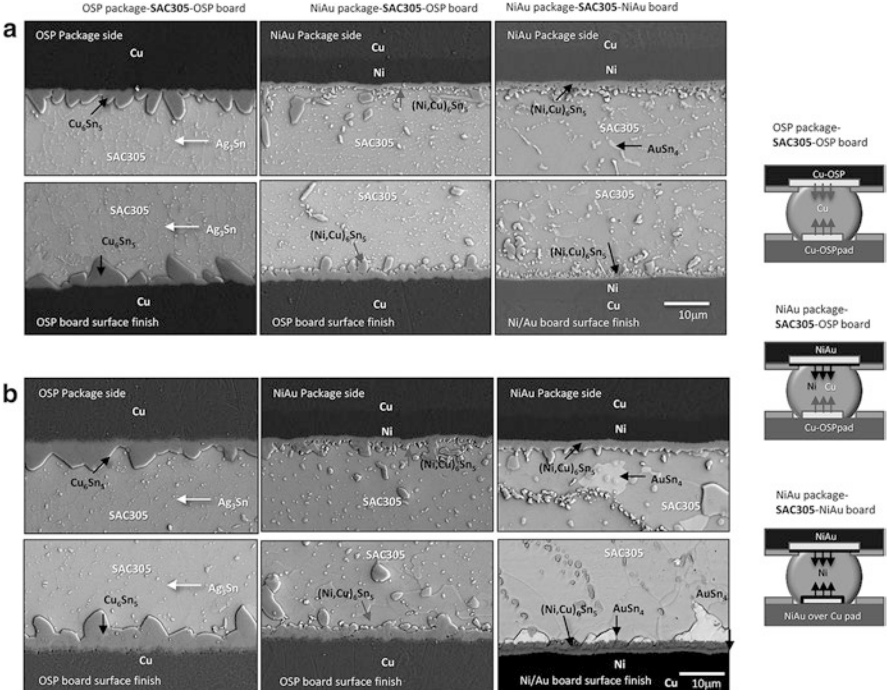


Fig. 5.26 Interfacial IMC structure in fine-pitch CABGA components assembled solder joints before (**a**) and after aging (**b**) with different interface metallurgy combinations, for OSP/SAC305/OSP, NiAu/SAC305/OSP, and NiAu/SAC305/NiAu, with aging condition of 150 °C/500 h (see data in Fig. 5.27)

the travel distance from the package-side interface to the board Cu pad is about half the diameter, and thus affects the IMC geometry more than is observed with larger solder ball diameter components. Because the package-side interface has a Ni diffusion barrier layer, the Cu source was limited to the board-side Cu pad. With this unbalanced condition, the preexisting Cu in the solder has a chemical potential to be driven to the package-side interface to form $(Cu,Ni)_6Sn_5$, which results in a Cu-depleted zone near the package-side interface. On the board side, large $(Cu,Ni)_6Sn_5$ intermetallic compounds are present just above the IMC interface, suggesting that a large flux of Cu came from the Cu source and that the package side provided a source of fast diffusing Ni.

On the other hand, with balanced Ni diffusion barriers on both sides (the NiAu/SAC305/NiAu joint configuration), in the right column of Fig. 5.26, the chemical potential gradient was not present. Since this structure has more Ni, the IMC geometry shows a more needle-shaped interface IMC with a few locations where $AuSn_4$ IMC phases formed and coalesced with aging. But after isothermal aging, both the board- and package-side interfaces show a smoother IMC surface with a lesser number of IMC precipitates nearby. This is due to the fact that the existing Cu in the solder near the interface formed $(Cu,Ni)_6Sn_5$ IMC, which consumed the Cu near the

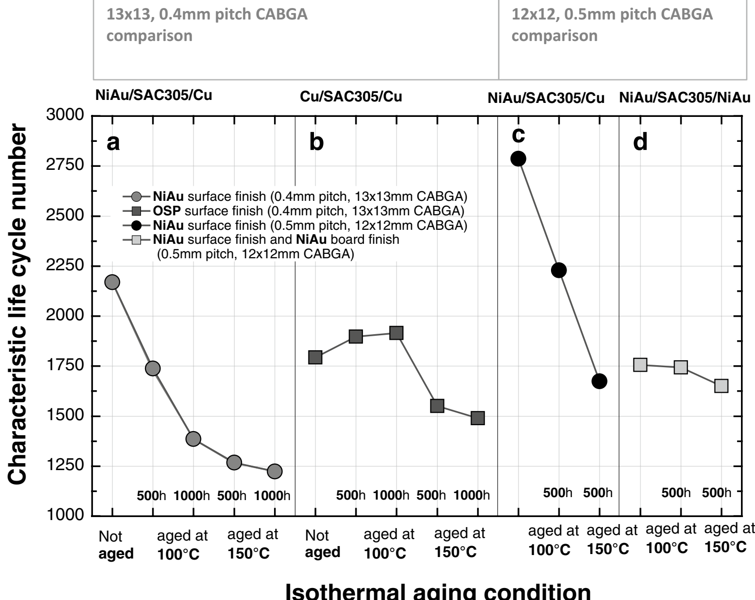


Fig. 5.27 Characteristic lifetime cycle number summary plot for Ni/Au samples and OSP sample interface preparations with different aging times and temperatures

interface at both sides, because Cu favors formation of the $(Cu,Ni)_6Sn_5$ crystal structure as discussed in Chaps. 3 and 4.

First, the thermal performance of OSP/SAC305/OSP and NiAu/SAC305/OSP joints in the 13×13 mm 0.4 mm pitch packages is compared. The black data points in Fig. 5.27 show the characteristic lifetime cycle numbers for the NiAu/SAC305/OSP samples. These samples have the highest cycle numbers for the unaged state, but there is a rapid decrease with aging (22 % with 100 °C, or 41 % with 150 °C 500 h). Compared to the NiAu/SAC305/OSP data, the OSP/SAC305/OSP samples showed a slightly lower cycle number in the unaged state but maintained a similar life cycle number even with aging at 100 °C for 1,000 h. There was greater degradation for the 150 °C aging temperature (17 % drop), but they still had a higher characteristic cycle number than samples with the NiAu/SAC305/OSP joint configuration. All cracks were located in the package-side solder bulk region near the interface. The cracks initiated at the upper corner of the package side and propagated through the upper part of the solder joint. As shown in Fig. 5.28a–d, there are different IMC precipitation distributions associated with the different interface conditions after aging and thermal cycling. The Ni/Au surface shows a reduced precipitate zone near the interface, whereas the OSP/SAC305/OSP interface region shows evenly distributed IMC precipitates with uniform size near the interface. The depletion of IMC precipitates in Ni/Au surface-finished samples can be related to the continuous formation of $(Cu,Ni)_6Sn_5$ at the package interface. It is known that the free energy of forming $(Cu,Ni)_6Sn_5$ is more favorable than Cu_6Sn_5 [48], and thus the Cu was

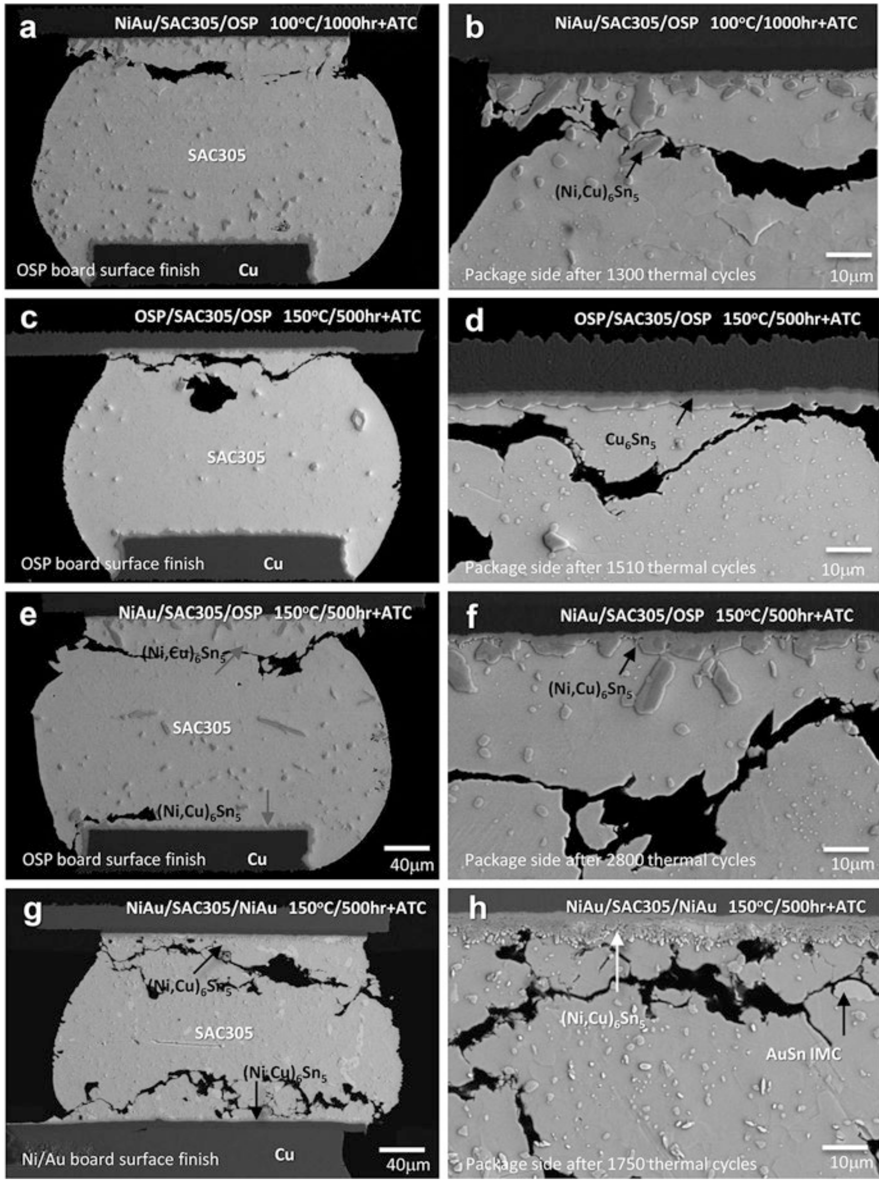


Fig. 5.28 The effect of isothermal aging on precipitates in the fractured region caused by thermal cycling of: 13 × 13 mm CABGA with 0.4 mm pitch (**a**, **b**) NiAu/SAC305/OSP with prior aging at 100 °C/1,000 h aging, (**c**, **d**) OSP/SAC305/OSP with prior aging at 150 °C/500 h. 12 × 12 mm CABGA with 0.5 mm pitch (**e**, **f**) NiAu/SAC305/OSP with prior aging at 150 °C/500 h, (**g**, **h**) NiAu/SAC305/NiAu with prior aging at 150 °C/500 h

consumed near the interface. Similar to the phenomenon observed with aging discussed in Chap. 4, the secondary $(Cu,Ni)_6Sn_5$ IMC formed during thermal cycling has lower Ni content in the $(Cu,Ni)_6Sn_5$ [49]. Nevertheless, the formation of this lower Ni-containing IMC at the interface requires consumption of Cu, which leads to fewer precipitates that can pin boundaries and, hence, greater grain boundary mobility as the microstructure recrystallizes, and this ultimately accelerates cracking. In contrast, the OSP/SAC305/OSP samples have a balanced Cu/solder/Cu structure and no resulting chemical gradient. The IMC precipitates near the interface grew in size but showed no specific change in their volume fraction, which is indirect evidence for the lack of a concentration gradient. Thus, the rate of degradation due to precipitate coarsening was slower, and the aged samples lasted for a larger number of cycles.

The observations of a reduced precipitate zone using the NiAu/solder/OSP surface finish are also observed in the other package design having a slightly smaller size and slightly larger pitch, as shown in Fig. 5.28e–f. In this smaller package, the number of cycles to failure was higher than for the larger package with the same conditions, but the rate of decreased life with aging was similar for 100° aging (24 %) and greater for 150 °C aging (41 %) for a 500 h aging time. In this smaller package, the condition of having Ni/Au on both sides of the joint was evaluated, and for the 150 °C 500 h aging condition, the lifetime dropped by 17 %. When there is a Ni/Au surface finish on both the package and the board side, the precipitate size is smaller and arranged similarly as the sample with OSP on both sides in Figs. 5.28g–h and 5.26. In the NiAu/SAC305/NiAu solder joint, there is only a small amount of Cu present, and the IMC chemical composition at the interface is Ni_3Sn_4, and the bulk solder has IMC precipitates with Ag_3Sn and $(Cu,Ni)_6Sn_5$. Little degradation was observed in NiAu/SAC305/NiAu joints with isothermal aging. The initial characteristic cycle number from the unaged sample showed a lower cycle number compared to the NiAu/SAC305/OSP samples, which results from Ni_3Sn_4 IMCs and more abundant Au in the bulk solder. The Ni_3Sn_4 IMC has a larger CTE mismatch with SAC and can facilitate crack initiation sites during thermal cycling [50]. Also, Au in the solder, which can form Sn–Au IMC precipitates, often reduces the performance, causing the lower thermal cycling performance. To summarize, in both package sizes, when there is a balanced chemical gradient, it reduces the life in the as-fabricated condition, but with isothermal aging, the lack of a chemical gradient is advantageous, as it slows the rate of subsequent degradation.

Comparison Between High-Ag Solder Alloy and Low-Ag Solder Alloy

A lower amount of silver in solder alloy is known to have better mechanical shock performance compared to higher-Ag solder alloys. The mechanism behind that will be addressed in Chap. 6. The amount of Ag also affects the grain structure development during thermal cycling. As shown in the previous section, aging can produce chemical gradients at the crucial region near the package-side interface. An alloy

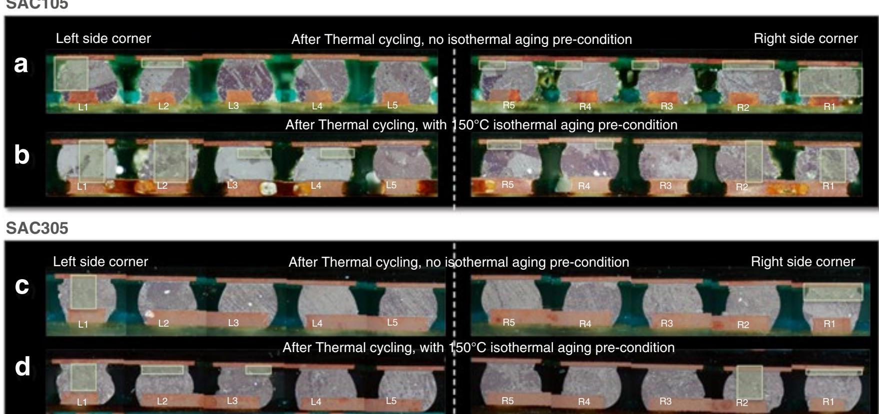


Fig. 5.29 Cross section optical polarized image microstructure for unaged and aged 12 × 12 mm 0.5 mm pitch CABGA samples after thermal cycling to failure with SAC105 (**a, b**) and SAC305 (**c, d**) joints. Observed crack locations are indicated in a *box*, indicating that unaged samples show less crack damage (**a, c**) than the 150 °C/500 h pre-aging samples (**b, d**). Cross section joints locations are indicated in Fig. 5.24

that initially has a low number of IMC precipitates will be less able to resist deformation and defect accumulation, so the joint will fail earlier than similar alloys with higher Ag content. This may be one of the main reasons why low-Ag solder alloys have a lower characteristic life cycle number for thermal cycling. But this is not all of the story, as illustrated in Fig. 5.24, which compares package designs and the influence of isothermal aging. For 15 × 15 mm CABGA packages, the SAC105 alloy performed more poorly than SAC305, and aging affected the lifetime of SAC105 but not SAC305. For 12 × 12 mm packages, the aged condition for both alloys gave similar performance, but in small 7 × 7 mm WLCSP packages, neither aging nor alloying affected the lifetime. Reducing the Ag content causes a lifetime dropping effect in larger package sizes with lower stress designs. As shown in the polarized light microstructures of the thermally cycled samples in Fig. 5.29, overlaid boxes show the locations of cracks that developed near the package-side interface (or through the diagonal of the joint if the box is larger). Due to the effect of the large die size, most of the damage occurred at the cornermost joints (Fig. 5.12), which show full crack propagation in each condition. There was more crack damage in the 150 °C-aged samples, and in SAC105, full and partial cracks were observed over a wider range of positions (indicated with boxes).

The reason for faster damage accumulation in SAC105 than SAC305 joints is that recrystallization occurs more uniformly and quickly in SAC105 joints. This can be quantified by identifying the number of grain boundaries per joint in the regions close to the interface. Based on ASTM-E112 [51], a linear intercept line was used to count the number of grain boundaries near the package-side interface and the board-side interface as illustrated in Fig. 5.30 in a 12 × 12 mm 0.5 mm pitch CABGA package with a large die. The cumulative number of boundaries for all 10 joints (the

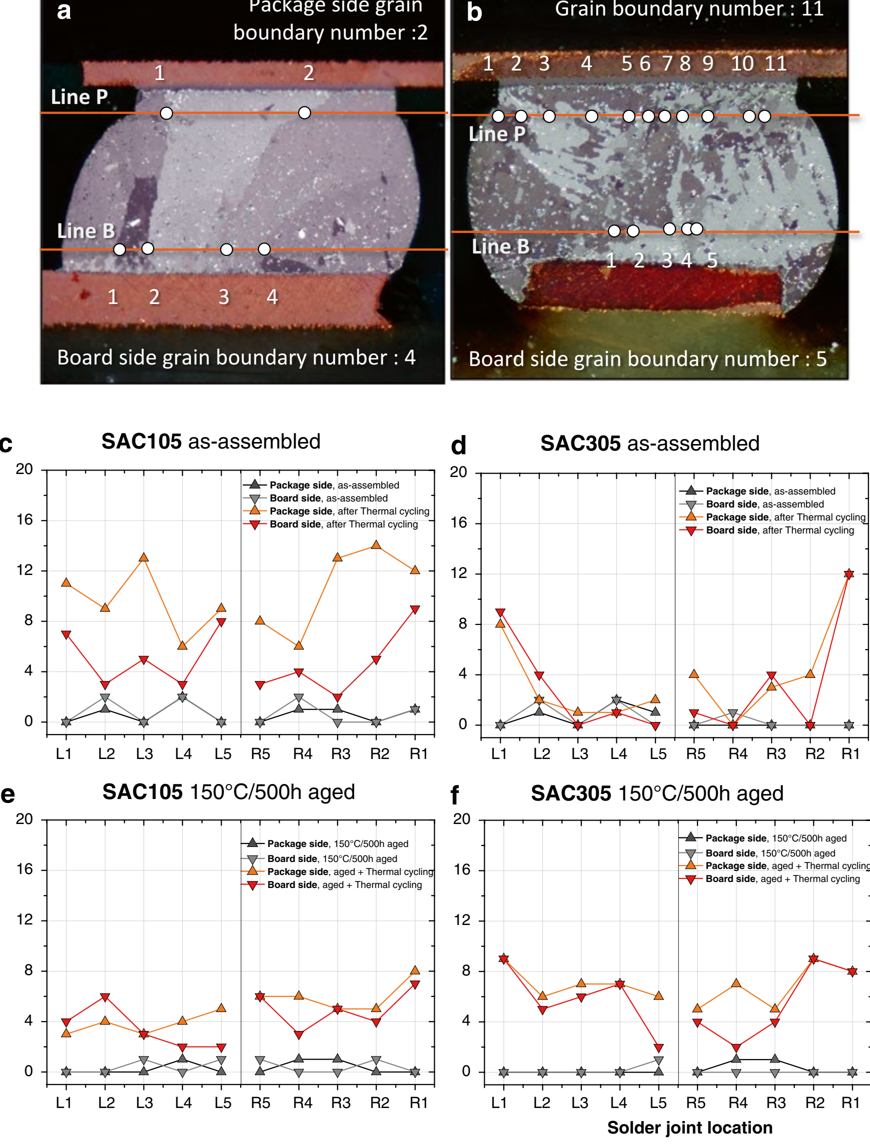


Fig. 5.30 Grain boundary counting in 12 × 12 mm 0.5 mm pitch CABGA packages with a large die along a line 50 μm from the package (P) and Board (B) for two sample joints (**a, b**). The number of boundaries at each joint location from left (L1–L5) and right (R1–R5) corner, (see data in Fig. 5.24) are shown before and after thermal cycling for unaged (**c, d**) and aged (**e, f**) SAC105 (**c, e**) and SAC305 (**d, f**)

five solder joints from each corner) per condition along the upper (and lower) line of each joint is marked with an up (or down) pointing triangle and plotted with joint position in Fig. 5.30. In each plot, the effect of thermal cycling (orange and red symbols) is shown with respect to the distribution prior to thermal cycling (black

and gray; these data are all measured from different packages). By comparing the grain boundary number distribution in SAC105 and SAC305 unaged and aged conditions, the number of grain boundaries increased substantially in all four conditions with thermal cycling, and the greatest increase was in SAC105 for the unaged condition. The SAC305 joints show a more uniform change in the unaged condition, with the greatest change occurring in the corner joint, indicating the effect of an extreme stress condition at the corner. The aged samples show similar changes in the number of grain boundaries in both alloys, implying that aging led to a similar spatial distribution of particles that govern the size of recrystallized grains. In general, the recrystallized grain structure development changed more uniformly in aged samples than aged samples [52].

The Effect of ΔT

As mentioned in the first section of this chapter (Table 5.2), the industry standards have several thermal cycling profiles, with various minimum and maximum temperature values, ΔT, and holding times, representing different end-use conditions. A larger ΔT will damage solder joints faster due to the CTE factor, which produces more mismatch strain. In this section, the effect of the ΔT on the thermal cycling performance will be compared on sample sets consisting of three different package designs and four different thermal cycling profiles shown in Table 5.5 [53]. The Weibull plots in Fig. 5.31 show that the temperature profiles consistently affect the thermal cycling performance for the conditions shown. For the large PBGA packages with SAC305 solder joints, the extreme ΔT condition with −60 ~ 150 °C thermal cycle reduced the life by a factor of 5 compared to the 0–100 °C thermal cycle (Fig. 5.31a). The thermal cycling results for 0.5 mm pitch CABGA with SAC105 and SAC305 also show consistent thermal cycling performance degradation with greater ΔT, with a drop in life by a factor of 4 for SAC305 and 3 for SAC105 (Fig. 5.31b, c). In the summarized plot in Fig. 5.32a, the 0.8 mm CABGA package showed very similar characteristics as the 0.5 mm pitch CABGA, suggesting that the package design has a larger role than the pitch.

With the thermal cycling damage discussed in this chapter so far, almost all the failures occurred at the package side, but as Fig. 5.32b shows, the more severe thermal cycling profiles show a shift of failure mode from only the package-side interface to a mixed failure mode including laminate crack propagation. Comparing test conditions

Table 5.5 Thermal cycling ATC Temperature profile and matrix

ATC condition	Temperature profile(°C)	Max–min temperature gap (ΔT) (°C)	Ramp rate (°C/min)	Dwell time (min)
1	0 ~ 100	100	10	10
2	−40 ~ 125	165	15	10
3	−55 ~ 125	180	15	10
4	−60 ~ 150	210	15	10

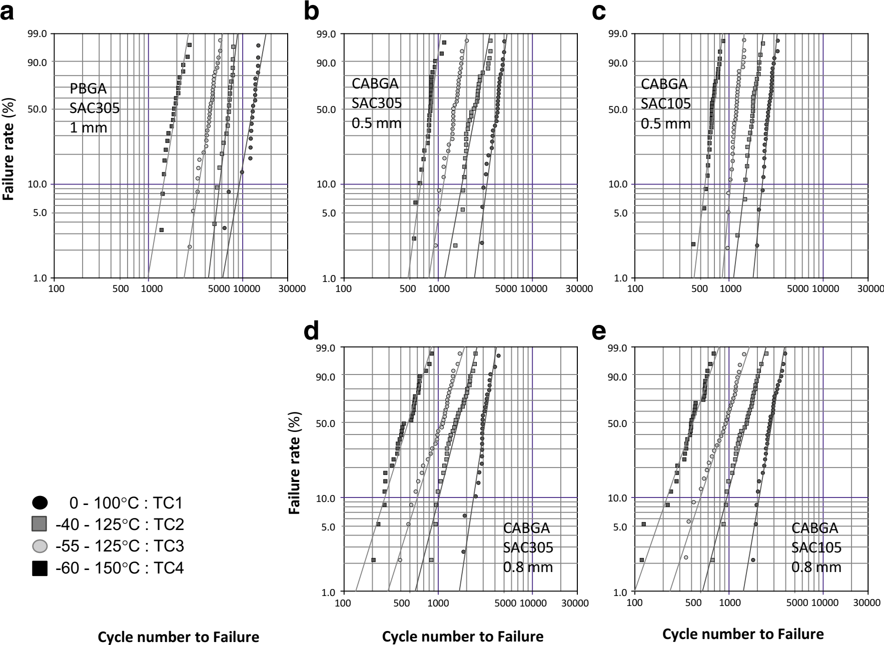


Fig. 5.31 Weibull plots for each package and alloy composition with four **Δ**T thermal cycling conditions. (**a**) PBGA with SAC305 solder, (**b, c**) 0.5 mm pitch CABGA with SAC105 and SAC305, (**d, e**) 0.8 mm CABGA with SAC105 and SAC305

with −40 and −55 °C and the same 125 °C high temperature, the failure mode shift may be caused by the extreme low-temperature excursion. The tensile properties of SAC solders are approximately linear with temperature, $\sigma = -\alpha T + \beta$ [54], where the tensile strength of SAC alloy is 20 % higher at −40 °C than at 0 °C, and α is temperature strengthening coefficient, and β is the strength at 0 °C in MPa, and T is in °C. The elastic modulus (E) ultimate tensile strength, the yield stress follow this trend. Thus, the solder joints become stiffer at lower temperature, and absorbs less energy with an increase in the yield stress. Also, the creep resistance increases with lower temperature [e.g., 29, 55], which makes the board laminate become the weakest link, so cracks propagate under the copper pad to cause failure. This mixed mode effect can account for the observation that solder joint alloy differences have less significance with wider thermal cycling temperature ranges. As the interconnect as a whole consists of several layers of materials, strengthening one layer may cause the shift of the weakest link to a different layer. To improve the system reliability, strong bonds are needed, but tough layers are also needed that can absorb strain without passing it to an adjacent layer are needed. An extremely low-temperature condition adds additional factors that make failure prediction more complex.

Other studies of thermomechanical fatigue have examined the effects of temperature range, mean temperature, dwell times, and heating and cooling rates. In a comprehensive study using a 12×12 mm BGA package with 0.8 mm pitch and

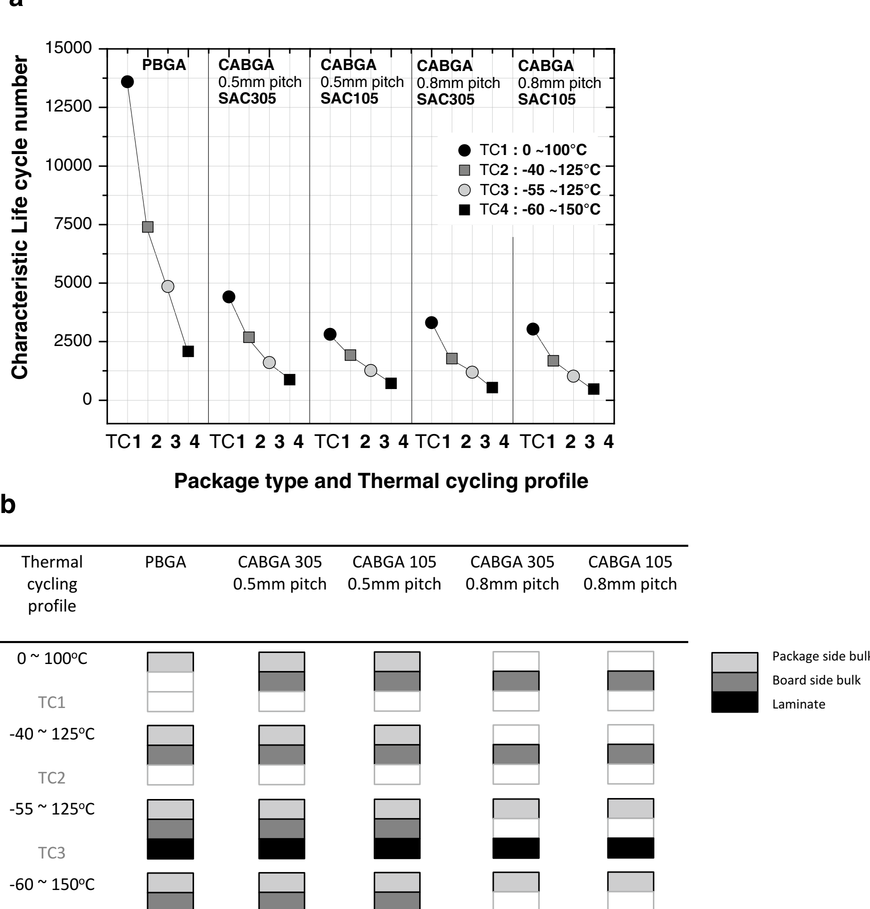


Fig. 5.32 Increasing **ΔT** reduces the number of cycles to failure in three different package size/alloy types. (**a**) Characteristic life cycle number per package type, solder alloy, and **ΔT** thermal cycling condition (**b**) failure mode per condition

SAC305 solder on a 1 mm board, considerable differences in lifetime resulted from variations in the thermal cycle [56, 57]. In general, the larger the temperature range, the shorter the life, and fast heating rates or high mean temperatures accelerate recrystallization/damage generation, due to generation of more strain inside a hysteresis loop. In a study using single-shear lap specimens, so that strength of the joint could be assessed with time/number of cycles, asymmetric dwell times were examined; longer cold dwell times led to a larger decrease in strength than longer hot dwell times [58]. The damage process reported consisted largely of generation of small grains near the solder/copper interface; and the greater the topography that

developed, the lower the strength. A rapid heating rate also led to lower strength and more generation of smaller grains in the solder/copper interface. While these results were not interpreted on the basis of recrystallization-limited damage generation discussed above, these prior results are consistent with this mechanism.

Thermal Cycling with In Situ Current Stressing

Up to this point, all of the studies described did not involve flowing current, but the flow of current is the primary source of heating that leads to thermomechanical cycling stress evolution. As electronic components are incorporated into smaller, higher-functionality, and higher-density packages, they will lead to increased power dissipation within a given volume, and consequently, larger temperature changes will result in shorter lifetimes [59–61]. With increasing current density, there is also an increasingly significant effect of electromigration [62–64], where rapid Cu transport assisted by the electron wind of current flow leads to depletion of Cu and voiding on one side of a joint and a buildup of Cu_6Sn_5 on the other. Although several failure mechanisms have been identified, the topic is under active investigation to find ways to mediate this problem.

Several factors affect the diffusion induced by electrical current flow through a solder joint. This includes not only the back stress caused by electrical current flow but also the Joule heating from localized hot spots [65], phenomena that lead to vacancy formation and migration that eventually cause void formation and current crowding, all of which strongly affect the lifetime of the solder interconnect [66]. However, the current stressing effect of relatively low current densities on the long-term solder joint stability and reliability is also important for systems that require long life. Figure 5.33 shows how the current density varies with input current for

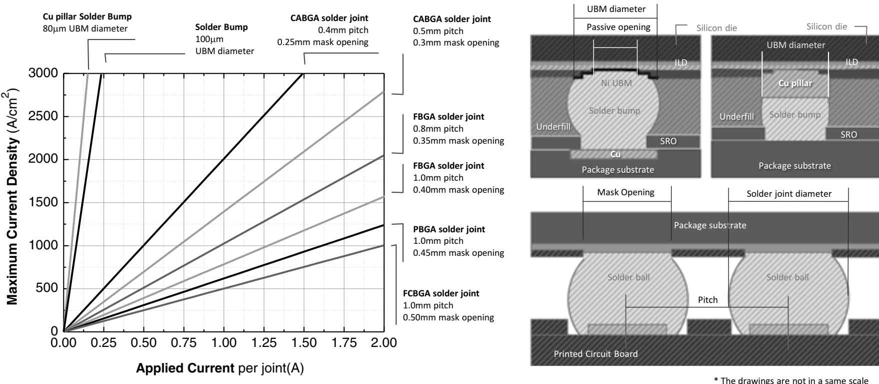


Fig. 5.33 The current density is directly related to the contact area and depends on the input current

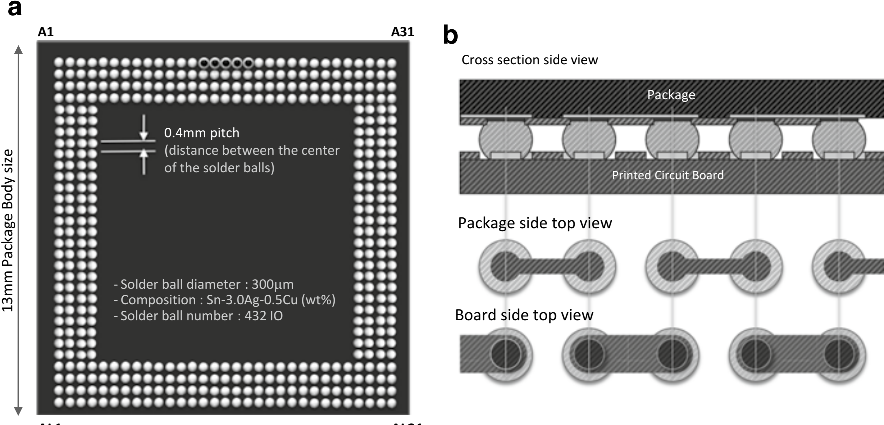


Fig. 5.34 (**a**) Fine pitch BGA sample configuration and (**b**) schematic side, package, and board views after board assembly

several solder interconnect sizes. With small solder bumps, it is obvious that the current density increases dramatically with current, resulting in a higher Joule heating and diffusion rates. Steady-state Joule heating causes conditions similar to isothermal aging, for which there is known degradation of the microstructure stability and thermal cycling performance. One potential mechanism for degraded life was linked to localized Cu depletion in asymmetric metallization on one side of the joint. Because current stressing causes an asymmetric distribution of Cu, it is also expected to cause degraded life.

Figure 5.34 illustrates a 0.4 mm pitch ball grid array (BGA) with 300 μm SAC305 solder joints on 13 × 13 mm components with a 10.05 × 10.05 mm silicon die using the daisy-chain wiring pattern that was used for a current stressing study. All BGA samples had either electrolytic Ni/Au surface finish or organic surface preservative (OSP) surface finish on top of the Cu package substrate, and the board had OSP surface preparation. During thermal cycling tests, daisy-chained solder joints were subjected to different levels of constant current density to reveal the effect of long-term current stressing and to investigate the effect of Cu migration driven by current stressing [67]. The internal circuit was connected so that the applied current flowed with a density of 2,000 A/cm^2 at the interface between the board and the package side through each solder joint as shown in Fig. 5.34. This level of current produced Joule heating due to the Cu trace and interconnect resistivity, which was compensated with the accelerated thermal cycling (ATC) test profile to cause a temperature change of 0 °C to 100 °C so that comparisons could be made for the same temperature range with and without current stressing.

Figure 5.35 shows Weibull plots for thermal cycling on unaged NiAu and OSP surface-finished BGA samples with and without in situ current stressing. Without current, the NiAu provided a significantly higher lifetime, but with current stressing, the characteristic life was 19 % lower, but nearly the same for the OSP specimen,

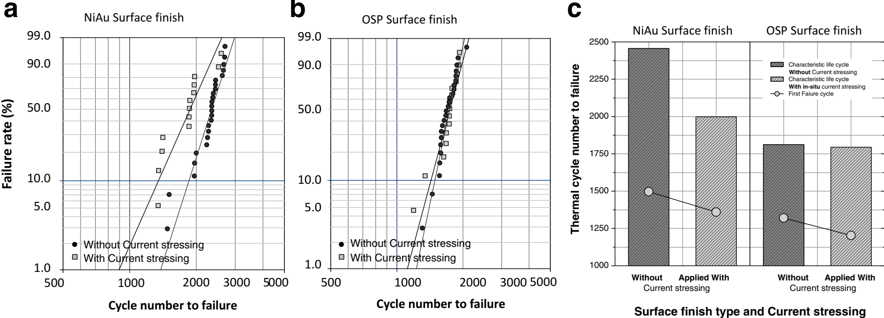


Fig. 5.35 Weibull chart plot for the thermal cycling results on BGA samples with and without in-situ current stressing with (**a**) NiAu surface finished samples, (**b**) OSP surface finished samples and (**c**) a summary plot which shows both the characteristic life cycle and first failure cycle number for each condition

which was nearly insensitive to current stressing. Figure 5.36 compares the different IMC precipitate arrangements in solder joints (A15-A19) after thermal cycling. Full cracks were observed in joints A17 and A19, in which the current was applied from the package side toward the board side. In contrast, joints A16 and A18, where the current moved electrons from the board to the package side, showed only partial cracks or no crack propagation. This shows that the fatigue crack propagation rate depends on the current flow direction inside the solder joint for NiAu interface-finished samples. Similar observations have been made by others [67, 68].

In OSP surface-finished samples, no accelerated crack propagation was observed, though there was significant microstructure evolution at the package and board-side IMC interface. In joint A15, a thicker IMC layer was developed during thermal cycling with in situ current stressing from the package to the board side, which was associated with Cu pad consumption at the package side. The same phenomenon, but in the opposite direction, occurred in joint A18, in which the current flow was from the board side toward the package side. The difference in the thickness of the Cu_6Sn_5 in A16 and A18 may be related to the crystal orientation, where the lack of IMC interfacial growth is a consequence of the c-axis being nearly perpendicular to the current flow that has been identified by others [69, 70].

The enlarged parts of insets in Fig. 5.36a and c left column for joint A15 show microstructural details where the current stressing moved electrons (and Cu) toward the package side. A locally IMC-depleted zone was observed near the board-side interface and an increased IMC ($(Ni,Cu)_6Sn_5$) thickness was observed at the package-side interface. The fine Ag_3Sn IMC precipitate distribution was also not present near the board side, which differs from the microstructure after thermal cycling without current stressing (Fig. 5.26 middle column). This difference in microstructure softened the board-side microstructure, but as the larger stress is present at the package side, there was no significant degradation of the joint performance. However, in joints such as A16 and A18 that experienced a current stress from the package side toward the board side, the Ag_3Sn IMC precipitate zone is

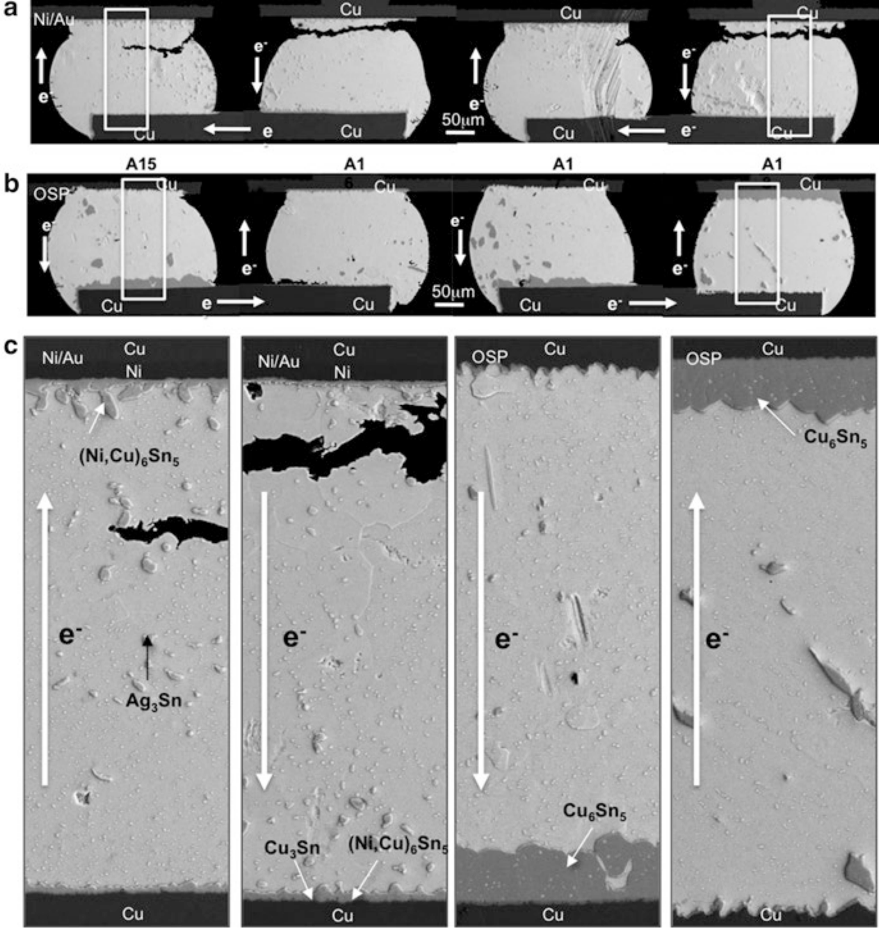


Fig. 5.36 SAC305 SEM microstructure after in-situ electro-current stressing during thermal cycling with 2,000 A/cm^2 current density (**a**) NiAu surface finished package samples (**b**) OSP surface finished package samples. The electron flow current direction is indicated with the arrow. (**c**) higher magnification areas indicated in (**a**, **b**)

maintained on the board side, and the volume fraction of ((Ni,Cu)$_6$Sn$_5$) is larger, and the IMC interface layer is thicker due to the transport of Cu to the board interface. The Ag$_3$Sn precipitates were depleted on the package side, and there are fewer ((Ni,Cu)$_6$Sn$_5$) precipitates, leading to an IMC-depleted and thus softened zone near the package interface. Because the package-side surface finish was NiAu, no Cu can diffuse into the solder bulk from the package-side Cu pad, resulting in a Cu depletion zone near the interface. A similar IMC and Cu depletion due to isothermal aging was also observed in earlier test results (Fig. 5.28), which accelerated the

crack propagation. Thus, the package side is further weakened (which is the most vulnerable side), and the board side is strengthened (which is not needed).

Figure 5.36b shows SEM microstructures that illustrate the effects of current stress on package-side OSP surface-finish samples. There are large ($(Ni,Cu)_6Sn_5$) IMC precipitates throughout all four of the joints, which are not present in the NiAu joints in Fig. 5.35a. In joint A15, in the enlarged image below in the third column of (c), the package Cu pad interface shows Cu dissolution into the solder bulk, as the IMC interface at the top is very thin, and an aggressive IMC thickness growth developed on the board side. Although the microstructure evolution happened aggressively at the interface IMC, the Ag_3Sn IMC precipitates inside the solder bulk exhibited little change in their distribution. Other than the differences in the ($(Ni,Cu)_6Sn_5$) thickness, the microstructures are similar to the unstressed microstructures shown in Fig. 5.26. Unlike the NiAu surface-finished samples, the OSP surface-finished samples have sufficient Cu sources at both the package- and board-side Cu pads to maintain a constant Cu concentration within the joint, which can feed the large ($(Ni,Cu)_6Sn_5$) precipitates, or the IMC at the interface on the downwind side.

Joint A16 in Fig. 5.36b differs from the other three in that there is no thickened ($(Ni,Cu)_6Sn_5$) interface at the package side, which is present in joint A18. Furthermore, there is a much smaller population of large ($(Ni,Cu)_6Sn_5$) IMCs within the joint, indicating that there is a much smaller flux of Cu passing through this joint, which is probably related to the crystal orientation, as the diffusivity is several orders of magnitude faster in the c direction than the a direction. This joint is probably a “red” joint, which prevents rapid transport of Cu through the joint because the fast path is parallel to the interface. In contrast, “blue” joints allow rapid transport of Cu through the bulk. While there was little or no effect on the characteristic lifetime during current stressing with OSP surface-finished components, stating that OSP surface-finished components are more stable than NiAu surface-finished components with in situ current stressing during thermal cycling is only valid if the Cu layer can sufficiently supply Cu into the solder joint system without degrading the joint structure itself. This is problematic because joint reliability is generally known to be degraded with increased interfacial IMC thickness.

Summary and Further Challenges

Thermal cycling provides a driving force to evolve the nonequilibrium solidification microstructures toward equilibrium conditions at rates that vary according to the package design and crystal orientation. This process evolves uniquely for each joint according to the combined effects of the joint position in the package and crystal orientation(s). With time, both continuous and discontinuous recrystallization processes occur, first in the most highly stressed location at corners or in some package designs, along diagonals between opposite corners. Some grain orientations evolve

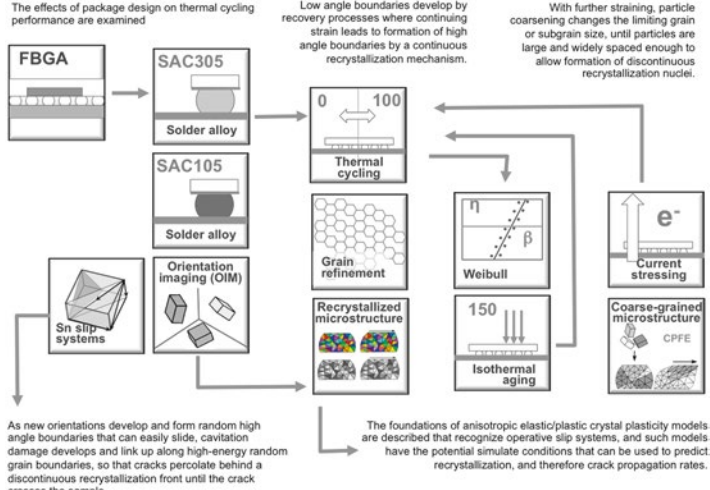


Fig. 5.37 Chapter five summary diagram

faster, such as red to yellow orientations (where the c-axis is parallel or within about 30° of the package interface). Other orientations are more resistant to this process, such as “blue” and “purple” orientations, where the c-axis is inclined by more than 60° from the interface. However, in packages with a low-stress design, recrystallization may never occur in the most resistant (blue–purple) orientations, and cracks can nucleate and percolate in some “red” orientations without the recrystallization process. These features are illustrated schematically in Fig. 5.37.

The interaction between aging and stress significantly affects the details of the recrystallization-limited crack percolation process; cracking is most quickly facilitated when conditions favor continuous recrystallized grains that are smaller but develop in a manner that stimulates more discontinuously recrystallized grains. Both recrystallization mechanisms depend on the rate of particle coarsening that governs the pinning of dislocations and grain boundaries. The influence of microalloying on IMC layer evolution and the stress state significantly affects the local particle coarsening (and related pipe diffusion) processes that control the discontinuous recrystallization mechanism. Thus, it is possible to envision dislocation slip-based models combined with evolving particle size evolution as a way to generate information from which the rate of crack nucleation and propagation can be predicted for a particular initial grain orientation and externally imposed boundary conditions. Once such models are developed, it may be possible to predict the failure process based upon physically based models. Once such models are validated, they have the potential to assist in designing accelerated testing strategies that can

assess the survivability of package designs without requiring time-consuming thermal cycling tests, which are a significant limit on the rate of design innovation.

Complicating cofactors that affect the microstructure evolution process include effects of electromigration that cause local Joule heating at rates that specifically depend on the function of the joint in the wider system. Electromigration also introduces additional chemical potentials that affect the growth rate and coarsening kinetics of particles and IMC layers and thereby alter the recrystallization mechanisms in specific ways relevant to the particular joint. The "blue" joints that are resistant to thermomechanical fatigue are particularly susceptible to electromigration damage due to the extremely high diffusivity of Cu and Ni along the crystal c-axis. Also, the superposition of externally imposed mechanical stress conditions caused by shock/drops and vibration fatigue must also be considered as important energy inputs into the microstructural evolution models. These inputs are examined in detail in the next chapter.

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Chapter 6
Mechanical Stability and Performance

This chapter describes the reliability performance and failure mechanisms of Pb-free solder joints under various mechanical load conditions, including bending, cyclic bending fatigue, and mechanical shock. The structural stability of solder joint under such mechanical loads is an important consideration factor for the current and future solder interconnects because electronic devices are subjected to such loads during various parts of their production as well as in end-use conditions. Even more importantly, mechanical stability is emerging as critical reliability concern with a rapid expansion of mobile electronics. In order to properly apprehend their challenges to the reliability, this chapter describes the threat from each mechanical load and the mechanism by which the solder joint fails. We begin with the introduction of the failure in solder interconnect induced by the bending force on PCB. The source of the bending force and its test method are presented along with discussion on failure mechanism. It is shown that the failure by bending force occurs either in Cu trace in PCB or solder/Cu interface. Secondly, the influence of cyclic bending fatigue is introduced. It is discussed more in terms of its mechanics and its potential as a new reliability evaluation tool. Finally, the failure by mechanical shock is discussed with weighted emphasis on recent experimental observations showing a sensitivity of shock resistance to the microstructure of the SAC solder joint bulk structure.

Mechanical Stability of the Solder Joint: Introduction

Electronic devices experience various external forces in several different modes. From a portable smartphone to a stand-alone Internet router, all equipment experiences some level of vibration, cyclic bending, monotonic bending, cyclic shock or a single shock. For high-reliability electronic devices, the mechanical stability of solder interconnects during dynamic conditions is crucial [1–5]. To have a stable interconnect in a mechanical performance environment, the

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T.-K. Lee et al., *Fundamentals of Lead-Free Solder Interconnect Technology*,
DOI 10.1007/978-1-4614-9266-5_6

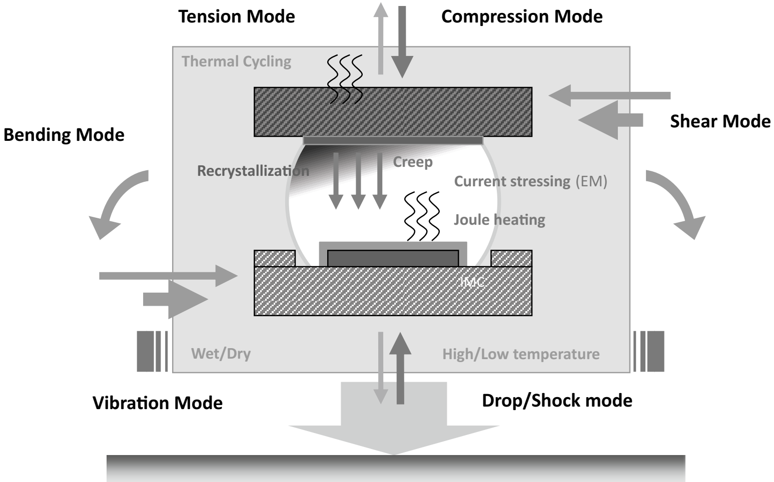


Fig. 6.1 Several factors need to be considered to predict the total lifetime of the solder joint including external forced from a variety of sources

interconnections need to tolerate mechanical strain, which develops in a particular way that depends on how the applied shock input reaches the particular component and particular joint [6–9].

Figure 6.1 shows a schematic of a solder joint, which experiences various external forces and challenges. All of these external or internal sources affect the stability of the solder joint. Mechanical bending can occur during use of the device or board, but even before assembly to the chassis, a large PCB can be easily bent by mishandling (grapping the board at one corner, etc.). The bend can produce a significant strain at certain component corner joints and potentially induce fracture to the joint even before it is deployed to the field. A continuous cyclic bending condition is a potential risk to the solder joint stability since high cycle fatigue failure develops during a long period of time, making it more difficult to identify and mitigate. Thus, knowing how monotonic and cyclic strains affect the solder joints and the associated deformation mechanisms that are activated is important to correctly assess and predict the lifetime of the joint and in order to identify potential mitigation strategies that can delay the failure [10].

In real products like running cars, for example, there are many types of energy inputs that lead to cyclic bending (or vibration), which can challenge the mechanical performance of the solder joint. An example of a 2.5 t truck is introduced in Steinberg's book [11, 12] that shows 15–19G peak acceleration at speeds above 10–15 mph with a frequency of about 15–40 Hz. Here we can see that there are two major factors, which need to be identified, the acceleration (G) and the frequency (Hz). The G level is an important factor, which is deeply correlated to the strain.

A higher G level can induce higher local strains, which will be examined in more detail in this chapter. Compared to vibration, mechanical shock usually has higher G levels per event and is a more single event-driven factor. It is easy to see the importance of shock performance by just looking at an everyday usage of a smartphone. Causing a total malfunction with just one general drop to the ground is not an expectation from a user. Fortunately various service programs and marketing programs exist that often can replace the malfunctioned device. But the problem is more serious if the mechanical shock-induced failure occurs on high-reliability products, where even a short interruption can cause unacceptable consequences and even endanger the safety of the users. In this case the frequency is not an important factor since the user just dropped the device one time, but once if the frequency increases, we will immediately see the effect of the interval time between the events, which ultimately will define the stability of the joint even in lower G level environments (e.g., cycling events like cyclic bending and vibration).

Facing these mechanical stability challenges, to correctly understand the mechanical performance of the device under certain user condition, simple questions need to be answered. For example, how many drops can a smartphone endure? Can the multi-chip module (MCM) under the hood in a car, which has an environmental temperature range of 200 °C, survive 10 years? After 5 years of functioning, can the router survive a general earthquake shock? To answer these questions, test methods and assessment tools based on mechanical shock-, bending-, and vibration-induced failure mechanism need to be established.

In this chapter, we will consider the mechanical stability of the solder joint by focusing on mechanical bending and shock for both monotonic and cyclic events. We will begin with monotonic bending and then consider cyclic bending, followed by mechanical shock to identify factors that affect their failure mechanisms. Figure 6.2 shows the failure modes observed in mechanically induced failures, whether by direct bending, vibration, or shock. Each external energy input induces a particular strain, and the localized strain is one of the direct sources that trigger failure in the solder joint structure. Representative failure modes are at the interface IMC for both package and board-side interface, inside the solder bulk joint, at the laminate region under the Cu pad, or at a combination of all three modes. It is often a competition between each failure location regardless of the crack initiation point, during further external energy input after initiation, the once dominating failure location can be shifted to a different failure location with faster crack propagation rate and ended up with a different final failure mode. So knowing the crack initiation and the propagation mechanism is crucial. Then how can we increase the stability in the mechanically challenged environment? An ideal system should consist of a flexible board and component that can absorb all the energy from the vibration, bending momentum, or shock, but given the fact that the silicon die is stiff, flexibility is limited; to endure the shock, the interconnects need to absorb or tolerate mechanical strain, which develops in a way that depends upon the interactions between the component location and applied mechanical source [6–9].

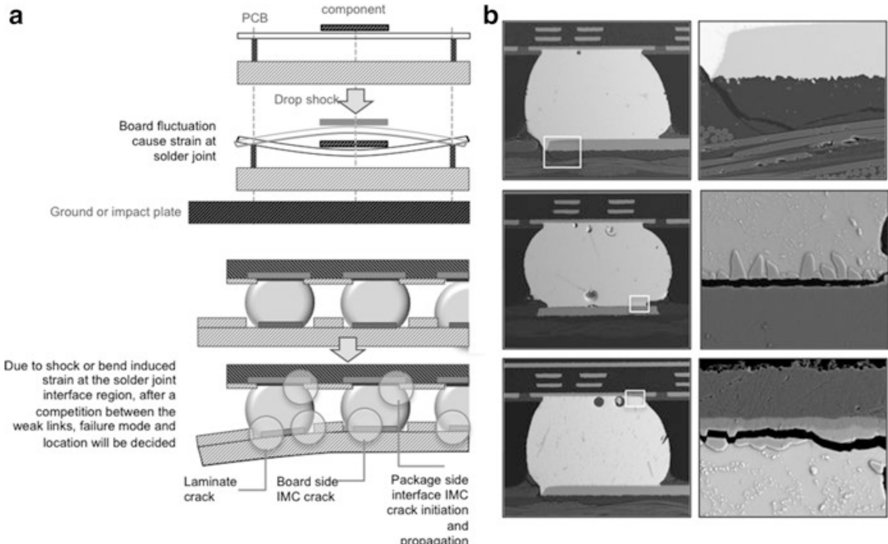


Fig. 6.2 Shock or bend eventually causes local strain which can affect the stability of the joint. (**a**) The corner solder joints experience a strain induced by the shock and bending mode. (**b**) Selected solder joints after shock test which show various types of failure modes and location

Given that the weakest interface changes with package design or even joint position in a package, identifying the methodology to improve the solder joint shock performance is a challenge. Three approaches can be proposed. With an example of a solder joint, which fails at the laminate, the first one is to either improve the strength of the laminate material or design the pad to shift the weakest link away from the laminate stress concentration point. The second approach is to directly strengthen the IMC layer so that the crack propagation is mitigated or delayed, and the third approach is to have the solder joint become able to absorb shock so that the shock wave does not transfer strain to the IMC layer or have the solder joint absorb strain by deformation so that the joint does not experience damage at the interfaces. We will discuss these approaches in the next section and identify methods that can elucidate how deformation mechanisms operate. What we will see in this chapter is that, at the end of the day, it is actually the capability of the solder joint, how much energy it can absorb, which defines ultimately the mechanical stability of the system.

Mechanical Bending

One form of mechanical force input is bending. Bending can be considered as an external mechanical source, but it can also be considered as an outcome that is induced by other external force and sources. For example, bending could be caused

by direct force input, but it can also be caused by shock and vibration that induce bending. But whatever the original source is, bending can induce strain in a particular region, and if the locally developed strain exceeds a certain damage limit, the energy released will develop an unstable damage site that will grow with further deformation.

Representative industry test standards exist. For monotonic bending, one of the standard documents is the IPC/JEDEC 9702 "monotonic bend characterization of board-level interconnects," and for cyclic bending there is an industry standard, JEDEC22-B113 "board level cyclic bend test method for interconnect reliability characterization of components for handheld electronic products" [13, 14]. The IPC/JEDEC 9702 on monotonic bend test is intended to characterize the fracture strength of a component's board-level interconnects and is applicable to surface-mount components attached to PCB. The characterization results provide a measure of fracture resistance to external loading that may occur during board assembly and test operations. A detailed test method is described in the document [13]. A universal tensile tester, with a four-point bending fixture is used to generate a controlled board deflection rate and apply a uniform-bending moment across the load span. Figure 6.3 shows a conventional four-point bending fixture and test configuration. To obtain valid results, a repeatable and well-controlled strain and strain rate are required. The crosshead travel distance and crosshead speed of a universal tester are approximately proportional to the test board assembly strain and strain rate, respectively. But as test boards have their own construction and geometry, interaction between a given component and board, a strain measurement is needed. Strain measurement equipment with a scan frequency of 500 Hz and a data signal resolution of 16 bits are necessary for the short-duration monotonic bend test (typically <5 s), allowing simultaneous recording of the daisy-chain resistance and strain based on the specification [13].

Since the interaction between the crosshead speed and the test board, the thickness and metal layer counts are important factors. The test board thickness and metal layer count should match the actual end-use device-printed circuit board. Table 6.1 provides recommended minimum test board thickness and metal layer counts. The recommended crosshead speed in the IPC/JEDEC 9702 is 5,000 μstrain/s. Testing conducted at crosshead speeds less will tend to overestimate the fracture strength of a component's board-level interconnects; hence, test equipment and test board configurations should be selected that meet the minimum crosshead speed to ensure getting the right value for an interconnect strength. The duration of the test is until the solder joint full fracture is detected, which is usually when the daisy chain has electrically failed, including the laminate crack which leads the Cu trace to be fractured/disconnected.

Figure 6.4 shows one bend test example with a large FCBGA mounted on a 2.36 mm (93 mil) thickness board. Strain gauges are located and applied to four different locations, and the board was bent to the point where the component daisy chain is broken. Shown in the figure, Ch1 and Ch2 strain gauges were attached to the backside of the board under the middle of the component edge and the corner of the component location, respectively. Ch3 strain gauge was placed on top of the

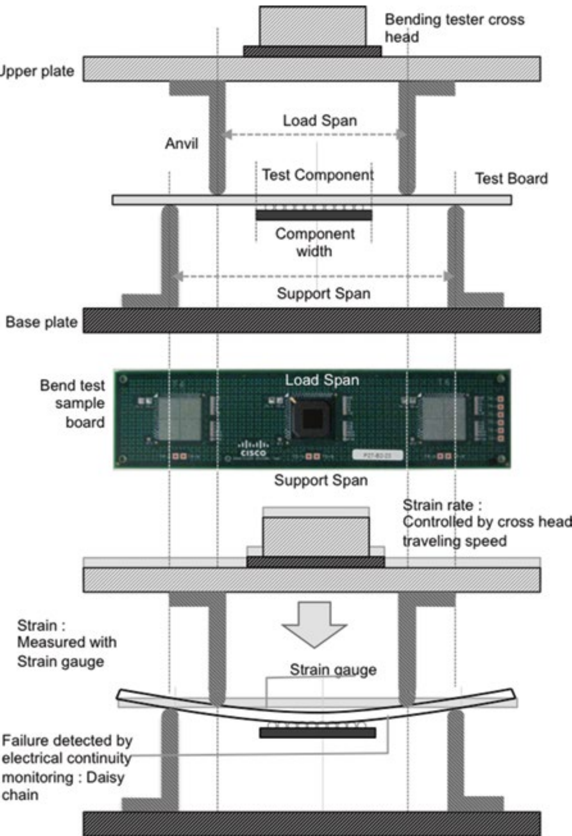


Fig. 6.3 Four point bending fixture and test configuration

component. A separate channel was attached to the daisy chain of the test component and board, so that the resistivity can be measured and detect the resistivity increase at the joint failure. With the crosshead pushing the backside of the test board, bending proceeds; Ch1 and Ch2 increased in negative microstrain value, since the component is facing downward. At the same time the component top also followed the bending with a positive microstrain until it reached the joint failure strain. When the Ch2 strain, the strain of the backside of the board under the component corner, reached (−)4,000 μstrain, Ch1, Ch2, and Ch3 all show a sudden step in the strain value measurement, which indicates the failure event followed with several continuous steps. With this measurement, we can assess the minimum strain to failure and use this data to set a process guideline or, if necessary, find a way to improve the minimum strain to failure for better mechanical reliability under bend-

Table 6.1 Recommended test board thickness and layer count

Maximum Package body size	PCB thickness (mm)	Minimum Cu layer count
Small : less or equal than 15 × 15 mm	1.0 mm (0.039 in.)	4
Medium : larger than 15 × 15 mm and less or equal than 40 × 40 mm	1.55 mm (0.062 in.)	6
Large : equal or larger than 40 × 40 mm	2.35 mm (0.093 in.)	8

ing condition. This example, in this case, monotonic bending, also shows that the various locations on the board show different strain responses, and each location shows a different stage and point of a joint failure. A certain incubation time or strain before reaching the strain level of failure exists. It is how much the component and board interaction and structure can endure, before a failure occurs. In other words, it is how much the solder joints and the interface bonding can hold on or absorb the strain caused by the bending before it releases the strength and fall apart. It is not hard to estimate that a larger component with a stiffer body is more riskier than a small and flexible component, but at the same time, other factors like the design of the Cu trace on the board side, the pad opening size, the height and diameter of the solder joint, the surface finish, etc., are equally important to derive a certain stability trend [15, 16].

Figure 6.5 shows the results of several components with different shapes and sizes that were bent to failure. The maximum strain at failure shows that the larger the component, the lower the strain level needed to break the solder joint, which is in most cases the corner solder joint. Of course, other factors than the component size are additional consideration factors, which influence the joint stability, like surface finish, solder alloy, solder ball size, and standoff heights. With all these combinations, the fracture mode is often strongly correlated to the board pad design. In non-solder mask-defined pads (NSMD) most of the cracks initiated and propagated through the laminate under the Cu pad, and most of the solder mask-defined pad (SMD) boards fracture in the IMC in the board-side interface. This effect of pad design performances will be discussed later in the shock performance results. Another interesting pint in the results in Fig. 6.5 is the failure strain difference between the electrical resistance measurement method and the acoustic event detection method. The acoustic event detection method is a nondestructive measurement method, which uses acoustic wave signal to identify fracture signatures during bending. As we can see in the figure, the failure strain levels are much lower compared to the electrical discontinuity measurement failure strains. This means that the laminate crack actually happens in a very low strain level. The strain needs to be built up to a certain level to break the Cu or solder interconnect to show the discontinuity in electrical measurements; thus a strain gap exists between two measurement methods.

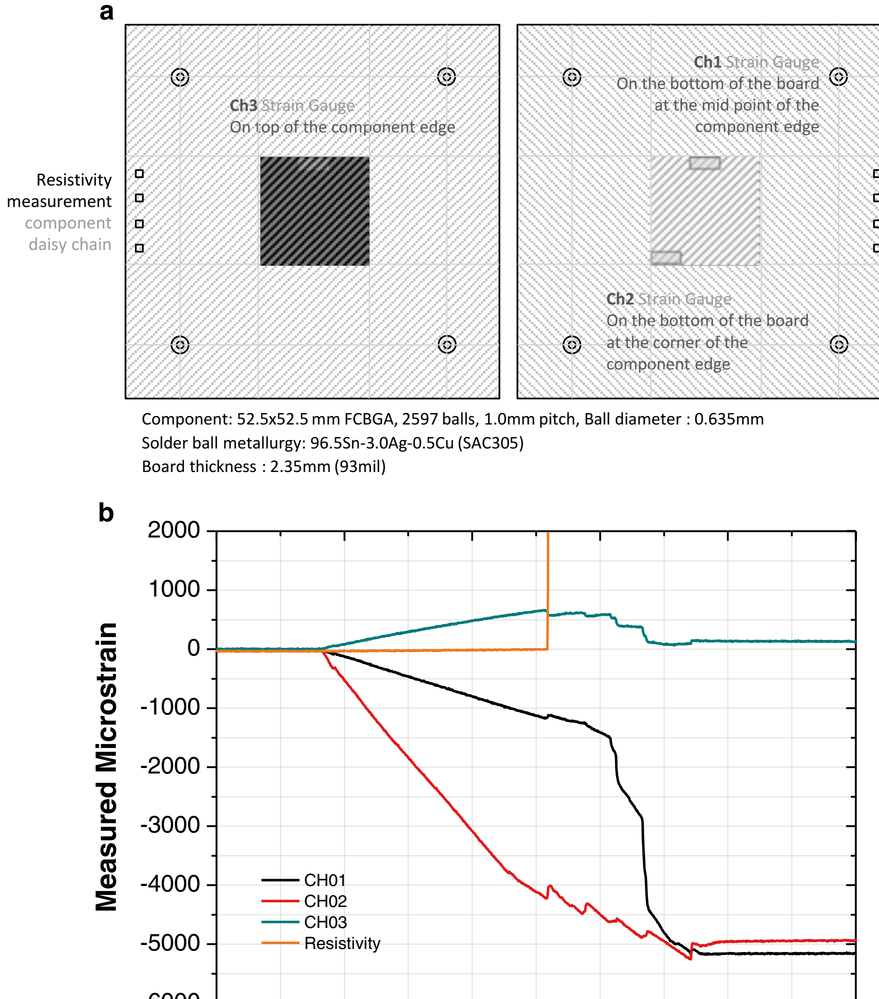


Fig. 6.4 Monotonic bend test example with a large FCBGA mounted on a 2.35 mm thickness board. (**a**) board layout and component info (**b**) strain value/data plot during bend test

Effect of Cyclic Mechanical Bending

Printed circuit board assemblies experience various mechanical loading conditions during assembly and use. Repeated flexing (cyclic bending) of boards during various assembly and test operations and in actual use can cause electrical failures due

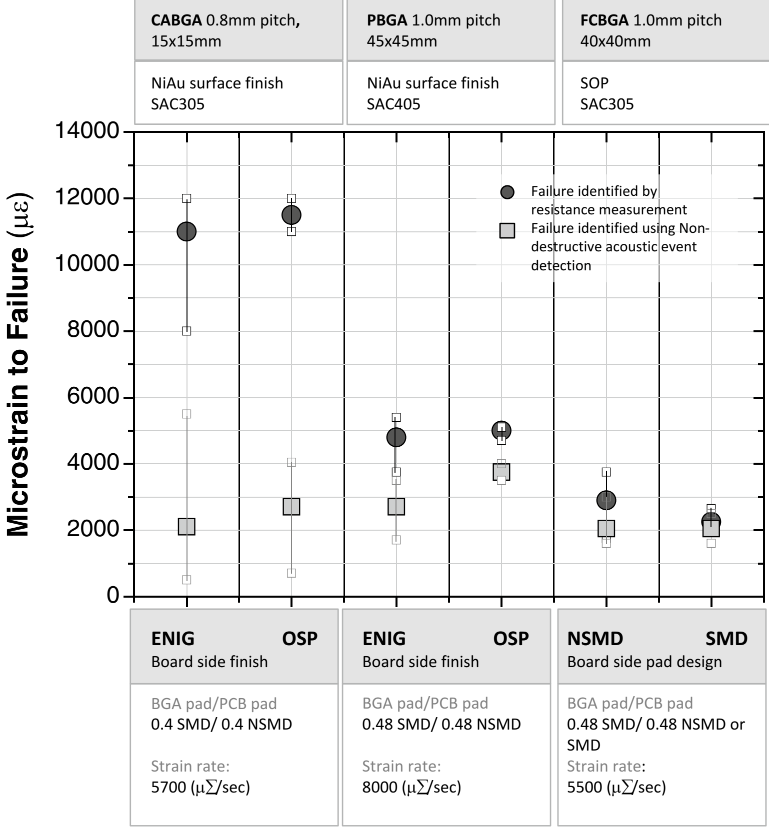


Fig. 6.5 Monotonic bend on CABGA, PBGA, and FCBGA sample with a 2.35 mm thickness board. Data points collected with electrical resistance measurement and Acoustic event detection method

to circuit board and trace cracks, solder interconnect cracks, and component cracks [17–23]. Although the number of repeated bend cycles is small during assembly (e.g., handling between various assembly operations, in-circuit testing, final assembly in product casing), the magnitude of flexure can be very significant. On the other hand, the actual-use conditions such as repeated key presses in mobile phones can result in a large number of repeated bend cycles during the life of the product, albeit at a lower magnitude. For example, the longitudinal and transverse strains that were measured on printed wiring board underneath the “9” and “8” keys show a maximum strain of about 400 microstrain and a duration of about 0.2 s for each key press [17]. A board-level test method is needed to evaluate the performance of the mounted parts against such failure and compare their performance with other components. Such evaluation is routinely conducted using cyclic bending tests.

In addition to the need for evaluating bending reliability of solder joints in normal-use conditions, the bend test has become more important in the packaging industry because it can reduce the reliability testing time. One of the most widely practiced reliability tests is temperature cycling. While it allows reliability evaluation of solder joints in normal-use conditions, it has a major drawback of taking an excessive long time. It often takes several months to induce failure, and multiple tests are required to enable reliability prediction with desired confidence. Because thermal cycling imposes significant time limitations on product development, there is growing interest to replace it with a faster but equally effective testing method. Cyclic bending fatigue testing may be one of the most promising methods with this potential. At the least, it has proved to be a quick way to identify failure-prone package designs or improper process conditions [18–25]. There is even greater interest to replace the temperature cycling test with the cyclic bending test if isothermal fatigue properties can be put into a predictive model that effectively predicts thermal fatigue reliability. However, because failure by thermal fatigue involves microstructural evolution, the model must include the dynamics of solder joint microstructure evolution and its influence on the thermal fatigue fracture mechanism. This poses a considerable modeling challenge that has not yet materialized. Nonetheless, the fact that fatigue testing can be done in a matter of days, if not hours, makes the bending fatigue test attractive for continuing considerable research and be used at least for product screening purposes. Industry standards on the cyclic bending test, for example, JEDEC22-B113, define boundary conditions for evaluating the whole assembly, but since they are intended for simulating failures at normal-use condition, they do not specify conditions for testing particular components on board and methods for analyzing the data. In order for it to be used for the study of solder fatigue properties, a few minor modifications of the system is needed, but more important is to understand its mechanics in inducing solder joint fatigue failure [25]. Also, the fact that cyclic fatigue bending performance varies significantly with chip design, materials, and process conditions makes discussion on fatigue performance of a particular system to be not so meaningful. Therefore, we focus more on the introduction of the fracture mechanics in cyclic bending fatigue and discussion on its merits as a potential reliability testing method.

The cyclic bending method builds on concepts developed from measurement of bending strength of structural materials [26]. In the case of bend-strength testing, the test piece is one piece of material that is subjected to bending strain by displacing the center of the sheet in reference to two pivot points. This action creates the uniform bending of the test piece between the two pivot points and allows the measurement of various material properties related to bending strength. The 3-point or 4-point bending configuration for assembled component packages is similar in that the stress imposed on the joint is induced and controlled by the bending of the substrate. However, the way that stress is induced at the solder joints is intrinsically different, and the difference can be seen in the example of 3-point bending of the PBGA assembly shown in Fig. 6.6. As shown, when the PCB board is bent, the test component is also forced to be bent. Because the bending force on the component

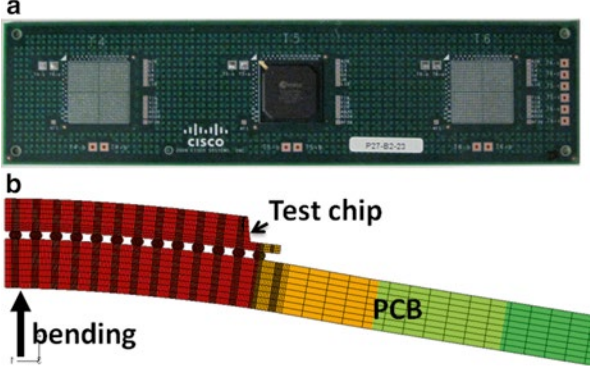


Fig. 6.6 A picture and diagram showing (**a**) PBGA board assembly designed for cyclic bending testing; (**b**) a schematic representation of the assembly at the bending condition

is transferred through the joints, the difference in the stiffness of the PCB and the chip creates a nonzero bending moment in the solder joint and thus exerts stress into the solder joints.

The fact that the stress at solder joint develops due to the difference in bending stiffness between the PCB and the chip creates several advantageous conditions for testing solder joint reliability. The first is the fact that the strain developed in an individual solder joint is not pure bending or shear but also has a significant tensile/compressive component perpendicular to the board. When the center of the PCB is pushed toward the chip, the joints at the outer edge of the array experience a force to separate the PCB and the chip, creating tensile strain. If the test were cycled fully about the neutral position, the opposite displacement would place the same joints under compressive strain. Such stress condition can simulate the stress induced by the thermal expansion mismatch between the chip and the substrate. The thermal mismatch causes the substrate to bend, resulting in the highest stress at the solder joints located at the outer edge or at corner of the assembly. It is therefore likely that the failure mechanism of the joint discovered by the bending fatigue is similar to the failure by thermal fatigue as long as the effect of microstructural evolution on the fatigue mechanism plays a minor role. This is the reason why the bending fatigue has gained considerable research interest.

Because the difference in bending stiffness between PCB and the test component is the very source of the stress in the solder joint, the level of stress is affected not only by the position of solder but also by the thickness (or local stiffness) of the molding compound where the joint is located. The variation in stress condition due to variation in molding thickness can be seen from the FEM (finite element method) strain simulation result of the PBGA package shown in Fig. 6.6. The result is shown in Fig. 6.7, where the shear, bending, and total plastic strain in the joints located at the outmost column of solder array as a function of their row position. This assembly contains a 26×26 array of 600 μm SAC305 solder ball joints, and the test component has a 2×2 cm base (labeled as BT) with an octagonal mold structure. The FEM simulation result shown in Fig. 6.7 is the case when bending displacement is 200 μm along the central axis. It is important to note that the joints experiencing the

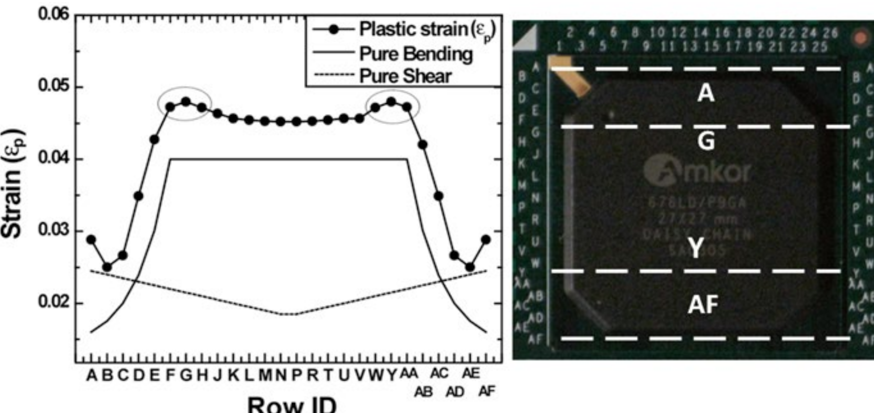


Fig. 6.7 A plot showing the shear, bending, and total plastic strain in the joints located at the outmost column of solder array as a function of their row position. The *left* is the image of the test chip with an inclusion on the key row positions of solder arrays. FEM analysis on the strain is conducted with an assumption of 200 **μ**m bending displacement at the central axis

maximum plastic strain is not located at two outer corners (A and AF) but is located inner side of the row (G and Y). This occurs because the joint at the G and Y rows is located at the boundary of low (thin) and high (thick) molding compound thickness. The schematic representation of the strain included in Fig. 6.7 presents a mechanistic explanation of this effect. As shown, there are two sources of the total strain upon bending. The first is the strain caused by the pure bending, and the other is pure shear. The bending strain comes mainly from the bending resistance of the chip, forcing the chip to separate from the solder, and therefore it is directly proportional to the local thickness of the molding. On the other hand, the chip also resists against the deformation in directions normal to the bending axis, that is, x- and y-axis, resulting in a shear strain. Consequently, the shear strain develops at the solder joint, and it will be the maximum at four corners of the molding, regardless of the thickness, and decreases with distance from the corner. The total strain is therefore the result of these two strain sources, making the G and Y joints to be at the maximum strain.

Figure 6.8, where the total plastic strain field within G and Y joints is shown, demonstrates that the cyclic bending testing is likely to induce crack initiation at the board side of the solder joint. In this colored diagram, the red represents the high total plastic strain while the blue represents low strain. It can be seen that there exist two maxima points, one at the solder/Cu trace interface corner of the joint and the other at the chip/solder interface. Detailed analysis reveals that the former experiences slightly higher plastic deformation than the latter. According to this result, the primary location for fracture is the interface between the solder and Cu trace in PCB substrate, unless the neck area in the solder created by the solder mask is mechanically weaker. Also predicted is that the joint that fails first is the one at G and

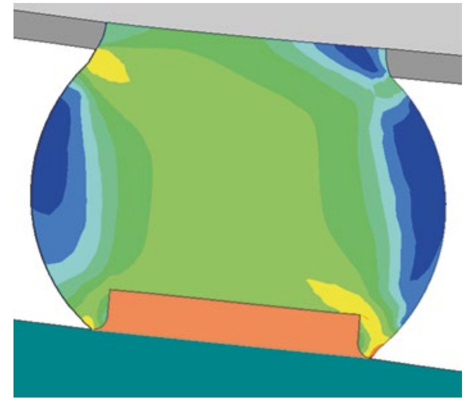


Fig. 6.8 A diagram showing the total plastic strain field in the solder joint G and Y under 200 **μ**m displacement at the central axis of the board. The red and blue colors represent the high strain and low strain, respectively. Note the presence two strain maxima, one at the right corner of the solder joint and the other at the solder neck area

Y. Cyclic bending testing of the as-reflowed solder assembly shows an exactly matching failure joint position and path. It was found that the failing joint under fatigue was located at G and Y position regardless of the level of displacement and cycle frequency. An example of the fatigue crack in a SAC305 joint (G position) following the interface of solder and Cu trace is shown in Fig. 6.9. Note that the crack propagates along the interface of solder/IMC but not inside the solder matrix. Also, the crack growth is very rapid, as evidenced by the resistance tracking data shown in Fig. 6.10. It can be seen that the number of cycles for the failure (C_f) after the damage initiation (C_i) is much shorter than C_i. It means that crack nucleation beyond the critical size takes much longer cycles than the crack growth. This is a result of crack growth under cyclic bending proceeding by the crack opening mode. Figure 6.11, where the FEM simulation of the solder joint deformation is shown, demonstrates the crack opening. In this simulation, a preexisting crack representing the embryonic crack is placed at the joint corner, and the deformation of the joint under bending displacement is calculated. The stress created at the crack tip due to bending results in opening of crack tip and causes the stress intensity factor (K_I) to increase. Such a level of crack opening is possible because nearly all applied strain is taken by the solder.

Early explorations of using cyclic bending in studying solder joint fatigue reliability indicate that it not only produces data that is reasonably repeatable but also a data that is consistent with normal fatigue theory. Figure 6.12 shows some of such data, which were gained from the bending fatigue testing of the same assembly in Fig. 6.6 with variation in frequency and bending displacement. Note that the failure cycle number increases with frequency but decreases with bending displacement. The result of decreasing fatigue life with increase in displacement is easy to understand because the plastic deformation per cycle at the joint increases with the bending displacement. Its dependence on the bending frequency may not be as intuitive, but it can be understood in the frame of work hardening. The frequency physically is related to the strain rate, meaning that high-frequency fatigue is equivalent to the fatigue at high strain rate. Since solder work hardens more at higher strain

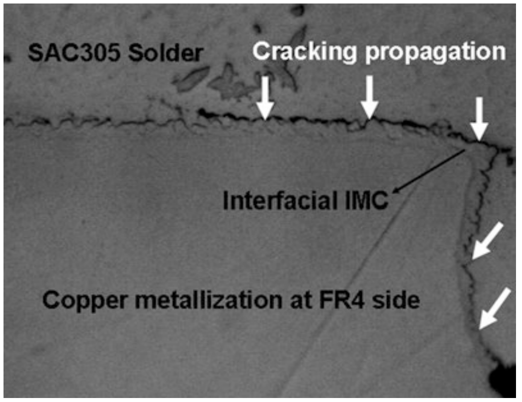


Fig. 6.9 A SEM micrograph showing the crack propagation path in SAC305 solder joint taken after the cyclic bending with 200 μm displacement under 1 Hz frequency. Note that crack initiates at the corner of solder/IMC interface and grows following the solder side of the interface

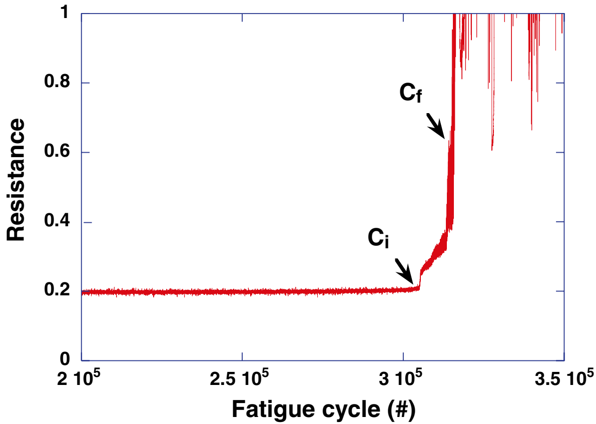


Fig. 6.10 A plot showing the typical resistance trace of solder joint taken during the cyclic bending. Note that it takes very large number of cycles to initiate crack (C_i) compared to the cycle number for its growth to failure (C_f)

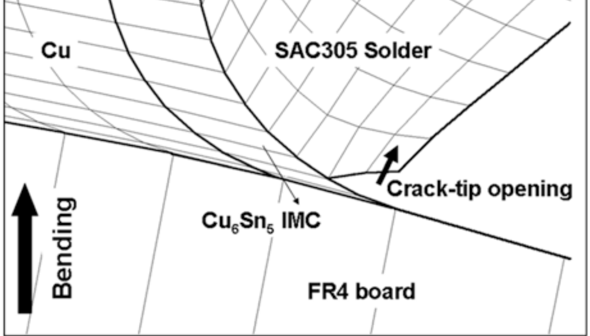


Fig. 6.11 A diagram showing the solder joint deformation configuration at the corner of solder joint near interfacial Cu_6Sn_5 IMC. This FEM analysis result evidences that the crack-tip opens due to plastic deformation in the solder by the bending of the PCB

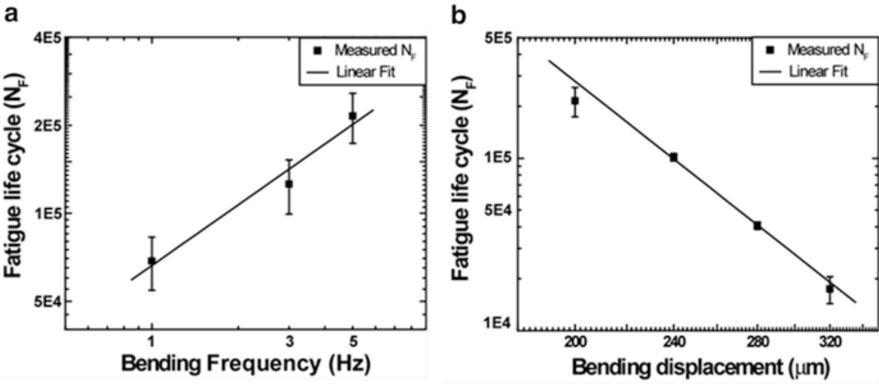


Fig. 6.12 Plots showing the fatigue life of SAC305 joints in PBGA assembly (shown in Fig. 6.6) as a function of bending displacement tested with variation in (**a**) bending frequency, and (**b**) bending displacement

rate, increasing its yield strength, the increase in the fatigue life with the bending frequency may be attributed to work-hardening property of the solder although other factors like deformation relaxation rate may play a role.

The results from the cyclic bending fatigue like the ones shown in Fig. 6.12 may provide an opportunity of investigating the fatigue properties and fatigue mechanism active in solder joints. There are two competing fatigue models suggested for the solder, and they are the total plastic strain and the total plastic strain energy models. The plastic strain model, known as the Coffin-Manson model, suggests that the fatigue life is determined by the amount of plastic deformation per cycle, while the energy model suggests that the fatigue life is related to the stored plastic energy. The level of plastic strain and strain energy can be calculated using FEM analysis and used for fitting of data to these models. The fit tried on the data in Fig. 6.12 is shown in Fig. 6.13. Note that the fatigue data gained from the displacement and frequency variation in Fig. 6.12 fit to one power law when they are plotted together as a function of the total plastic strain. On the other hand, those two fatigue data do not show such a correlation when they are plotted as a function of the total plastic energy. In this case, there exist two power law relations: one for the displacement and the other for frequency. This result may suggest that the Coffin-Manson model may be a more appropriate model for describing the fatigue behavior of the solder at isothermal condition, which may or may not be extended to the case of thermal fatigue, where stress relaxation is an important consideration.

Effect of Mechanical Shock

A mechanical shock to a device or board can occur from various sources. A direct hit to the device or a collision can transfer the impact energy directly to the device. This type of impact energy can also happen when the device is dropped to the

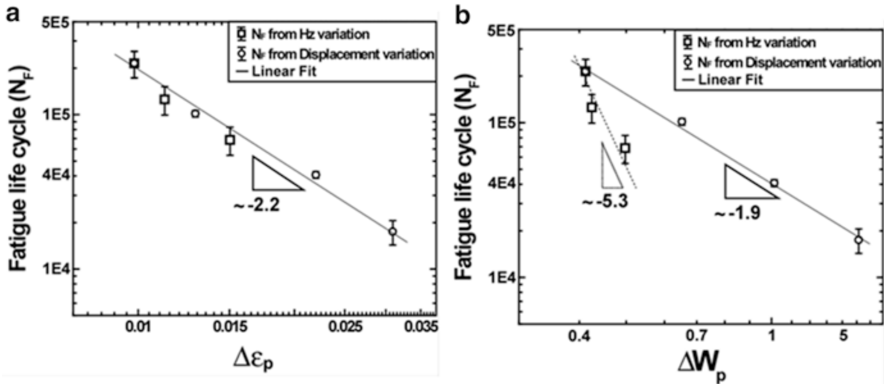


Fig. 6.13 Plots showing the fatigue life of SAC305 joint in PBGA assembly (Fig. 8.5) as a function of FEM calculated (**a**) total plastic, $\Delta\varepsilon_P$, and (**b**) total strain energy, ΔW_P

ground. With the impact energy transfer to the device, two important quantities can be measured, the acceleration (G) level and strain (ε). With a given impact energy input, to maintain its functionality, the device or the board needs to dissipate the impact energy before the energy impacts the joints or interconnects.

Figure 6.14 shows one example of a monotonic table drop shock impact applied to an electronic equipment board. The board size in this case, 6×6 in., was attached to the table with four standoffs at each corner of the board and lifted to a calibrated height to achieve a 200G acceleration or shock level at the table. With the impact, the table experienced a 200G level shock pulse; the accelerometer at the component corner on the test board measured a 300G maximum acceleration shock wave. At the same time, strain at the corner of the component measured by a strain gauge shows a sudden spike, a localized strain, which is a very high strain rate bending moment, followed by a high-frequency oscillating cyclic bending. In these series of events, we can see several factors, the input shock level based on the drop height, the shock wave travel from the table to the component via standoffs, the local strain, induced by the shock, and the frequency of the strain cycles to dissipate the shock energy.

But one very important factor among those various factors is the shock pulse duration and its correlation to the intensity of the shock wave, in other words the G level. For example, the pulse duration for the table shock input from the test above is 1 ms as shown in Fig. 6.14 and can be differed with using a different stopper material at the surface, where the table drops on. Simply it is a cushion, which defines the shape of the shock wave, the half-sine pulse duration as shown in Fig. 6.14b. Whether the stopper material is thin or thick (or different materials which absorb more shock than the other), the shape of the shock wave can be different with various pulse duration times. Figure 6.15 is a series of examples with the same test board with three different stopper materials. Shown in Fig. 6.15a the drop height was fixed to have a 200G table shock input with a thin stopper material. But

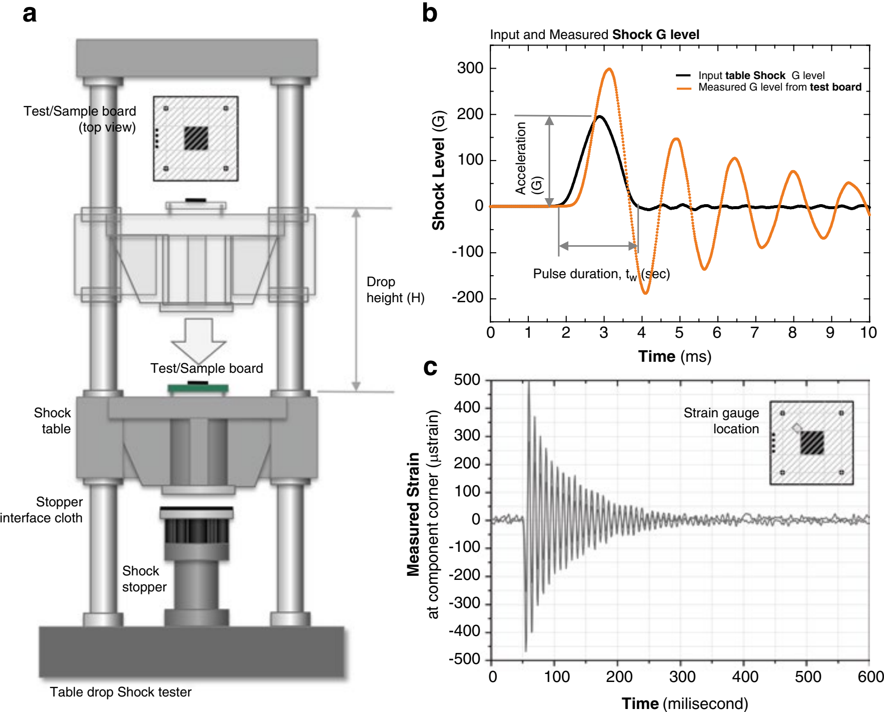


Fig. 6.14 (**a**) Schematic drawing of typical table drop tester. (**b**) Measured G level corresponds to a 200G half sine pulse input shock and (**c**) strain at the corner of the component during the 200G input shock. The acceleration (G) and the pulse duration time (t_w) are indicated in (**b**)

with the same drop height, and slightly thicker stopper (medium thick), the measured input table shock level decreased with further decrease using a thick stopper material. Figure 6.15b shows a slightly different comparison. This time we fixed the input table shock level to 200G. To have the G level reach 200G, the drop height needs to be increased, and at the same time we can see the pulse duration increased also. These two series of examples show the correlation between several factors. Figure 6.16 is the accumulated summary plot and correlations and interaction between those several factors. These correlations are important because it is the combination of the maximum shock level, the shock duration, the frequency, the localized strain, and also the cyclic fluctuation or cyclic fatigue that makes the solder joint degrade and, eventually, fail.

In this section we will begin with the industry standard test methods and understand the behavior of the test board, the strain and G level, and how these values depend on location on the board. The components' shock performance and the failure mode will be discussed followed by effects of pad design, isothermal aging, microalloy compositions, and cooling rate.

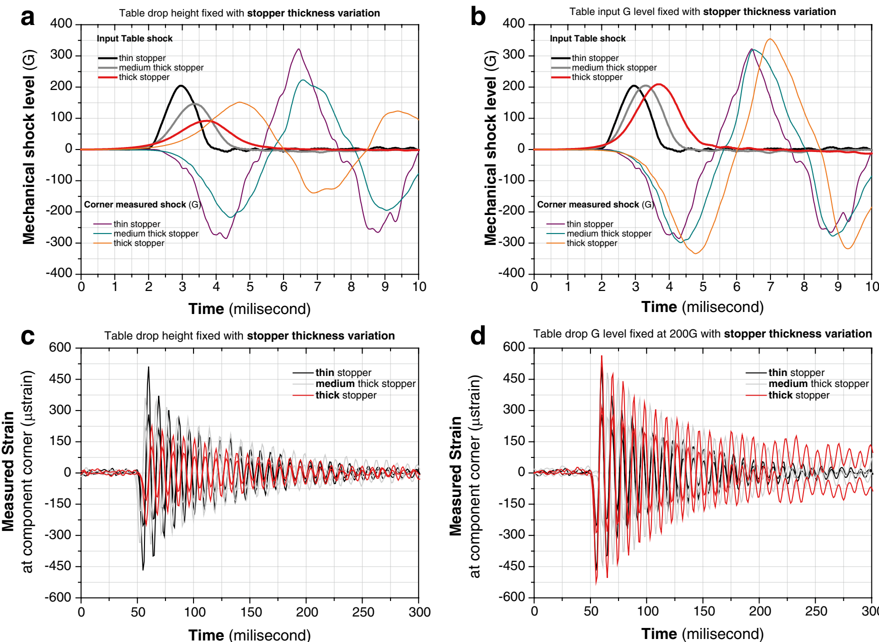


Fig. 6.15 Input shock, measured shock, and measured strain with different shock stopper material selection. (**a**, **c**) Shock G level and strain plot with fixed drop height with three different stopper thicknesses. (**b**, **d**) G level plot and strain plot with increased drop height to fix the input G level. The pulse duration increases with thicker stopper material but the G level decreases with a fixed drop height. To maintain the G level for higher pulse duration time, the height needs to be increased and the induced strain increases with increasing the drop height

Mechanical Shock Test-Related Industry Standards

Because there are various end-use conditions related to mechanical shock, there are a variety of industry standards. The IPC/JEDEC 9703 "Mechanical Shock Test Guidelines for Solder Joint Reliability" and the military spec are a few of the standard test method documents. The document explains the mechanical shock test guidelines for assessing solder joint reliability of PCB assemblies from system to component level. For more handheld devices a more focused standard is document JESD22-B111 "Board Level Drop Test Method of Components for Handheld Electronic Products," with an additional JEDEC standard JESD22-B110A "Subassembly Mechanical shock." The handheld and portable electronic products usually fit into the consumer market segments as handheld electronic products are more prone to being dropped during their service life. This dropping event cannot only cause mechanical failures in the housing of the device but also create electrical failures in the PCB assemblies mounted inside the housing due to transfer of energy through PCB supports. One of the primary drivers of these failures is localized strain exceeding the endurable limit induced by the input acceleration to the board,

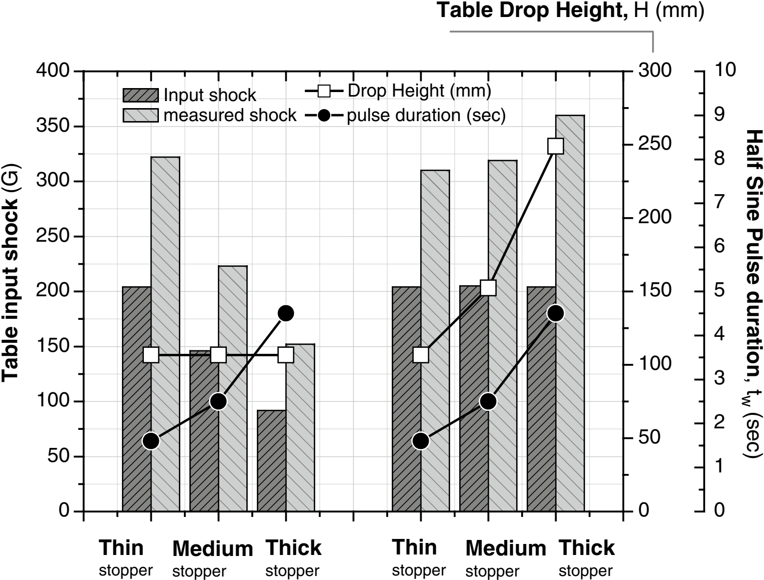


Fig. 6.16 Summary of Fig. 6.15. Input shock, measured shock, and measured strain with different shock stopper material selection. The pulse duration (t_w) increases with thicker stopper material but the G level decreases with a fixed drop height (H). To maintain the G level for higher pulse duration time, the height needs to be increased and the induced strain increases with increasing the drop height

resulting in component, interconnect, or board failure. The failure is a strong function of the combination of the board design, construction, material, thickness, and surface finish material, interconnect material, and component size, which we will address in this chapter.

Several test board designs and layouts are shown in Fig. 6.17, where Fig. 6.17a is a 132 mm × 77 mm (5 × 3 in.) JEDEC test board, with up to 15 components and maximum component size of 15 × 15 mm. For components larger than 15 × 15 mm, a square board (Fig. 6.17b) with hole locations of 5 or 6 in. (125–150 mm) apart is widely used, which usually accommodates one component. While the B111 board is a suitable board for a smaller package size and higher G level shock tests, which are typical of the consumer electronic product sector, the larger square board is for larger and heavier components like FCBGAs utilized in high-reliability product boards with a relatively lower G level test condition. The board in Fig. 6.17c is a modified test board based on the JESD22-B111 test board. The basic design concept for the JEDEC rectangular board was to imply various strain conditions in one board to test the component in variety of conditions. Due to that purpose, the failure cycle number varies by the location of the component on the board. But to reveal the effect of subtle changes in microstructure on the mechanical stability of the joint, an appropriately sensitive test method needed to be established, which can decouple the shockwave-induced failure from the strain-induced failure with a more simple

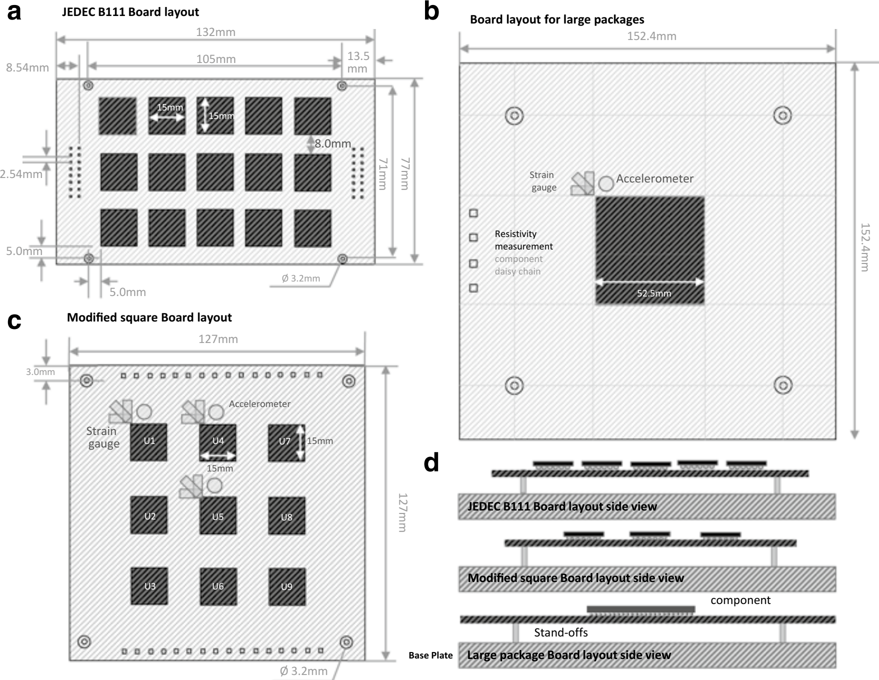


Fig. 6.17 Test size and layout. (**a**) JEDEC B111 board layout. (**b**) Large package shock board layout and (**c**) Modified square board layout. (**d**) side view for each board for shock testing

strain and G level combination test board. The modified 125 × 125 mm square board in Fig. 6.17c is designed to have a uniform condition on four corners and four edges with same strain and G level combination, which made it possible to evaluate the joint stability under various combinations of shock and strain level.

The drop shock test is performed by raising the shock table to the height specified according to JEDEC condition and dropping on the strike surface while measuring the G level, pulse duration, and pulse shape as we saw already in the earlier section. There are various shock conditions as shown in Table 6.2. The widely used test criteria for small packages used in portable and handheld electronics including the tablet computers is Condition B: 1,500 Gs, 0.5 ms duration, half-sine pulse as the input shock pulse to the printed circuit assembly (as listed in JESD22-B110 Table 1 or in JESD22-B104-B Table 1). This is the applied shock pulse to the base plate and is measured by an accelerometer mounted at the center of the base plate or close to the support posts for the board. Other shock conditions, such as Condition H (2,900 Gs, 0.3 ms duration), in addition to the required condition can also be used for more extreme end-use conditions. But for larger components like FCBGA, condition B with 1,500G is too high because larger components like FCBGAs are heavy and could not survive this level of shock unless it has additional support material. Thus

Table 6.2 Component test levels described in JEDEC22 B111

Service condition	Equivalent drop height (in./cm)	Velocity change (in./s)/(cm/s)	Acceleration peak (G)	Pulse duration (ms)
H	59/150	214/543	2,900	0.3
G	51/130	199/505	2,000	0.4
B	44/112	184/467	1,500	0.5
F	30/76.2	152/386	900	0.7
A	20/50.8	124/316	500	1.0
E	13/33.0	100/254	340	1.2
D	7/17.8	73.6/187	200	1.5
C	3/7.62	48.1/122	100	2.0

conditions C, D, and E with 100G, 200G, and 340G are used for larger component applications.

As we discussed earlier, the peak acceleration and the pulse duration are a function of not only the drop height but also the strike surface and the stopper material. Depending on the strike surface, the same drop height may result in different G levels and pulse duration. Theoretically, the drop height needed to achieve the appropriate G levels can be determined by an equation below where H is the drop height and C is the rebound coefficient (1.0 for no rebound, 2.0 for full rebound).

$$A(t) = A_o \sin\left(\frac{\pi t}{t_w}\right)$$

$$\sqrt{2GH} = \frac{2A_o}{C}\frac{t_w}{\pi}$$

However, this equation does not include the strike surface effect. The shock wave can be controlled by controlling the height of the drop table, and also the stopper material (or the thickness of the material), to adjust the shock wave duration. The level of shock and the duration are important factors because the same amount of energy can be achieved with a lower shock level and longer duration than a higher G level with very quick duration. That is the reason why the test standards define also the shock duration, to make it available for comparison.

Mechanical shock-induced failure is based on two major phenomena: a shock-induced strain and a shock wave (G). In general, one can think that with a higher level of shock, the board deflection is larger and producing larger strain and thus inducing solder joint crack at the weakest link. But the higher G level does not always mean a higher strain. The strain at a given shock level is strongly dependent on the component weight and the structure of the board. As shown in Fig. 6.18, the comparison between the JEDEC-B111 rectangular board and the modified square board reveals that the G level of each location shows a similar response, but the strain value is much higher for the rectangular board compared

to the square board, showing the effect of the board geometry and structure. The G level response and strain values are from 1,500G level peak acceleration, 0.5 ms half-sine shock pulse input to the drop table. Even though the JEDEC-B111 rectangular board is the industry standard test board, since the failure locations are too versatile, in this chapter we will mainly use the modified square board (Fig. 6.17c) test results to explain the mechanical shock properties of the solder joints based on the G level and the strain. The square board has a total of 9 components per board and is designed to provide three pairs of different strain and shock conditions: high shock/high strain, which occurred at the center location (U5); low shock/low strain, which occurred at the corner locations (U1, U7, U3, U9); and low shock/high strain, which occurred at the edge locations (U2, U4, U6, U8). With the 1,500G, 0.5 ms half-sine shock pulse, each location, edge, corner, and center shows a different maximum peak G level and response to time wave with the highest peak level at the center of the board. Like this, the G level and strain variation are affected by the geometry of the board and location; the thickness of the board is also an important factor. A series of measurements on three different thickness boards with different level of input shock is presented in Fig. 6.19. As shown in the figures, from a thinner board toward a thicker board, with a given shock input, the thicker board shows a higher peak G level response but lower maximum strain level at most of the locations compared to the thinner

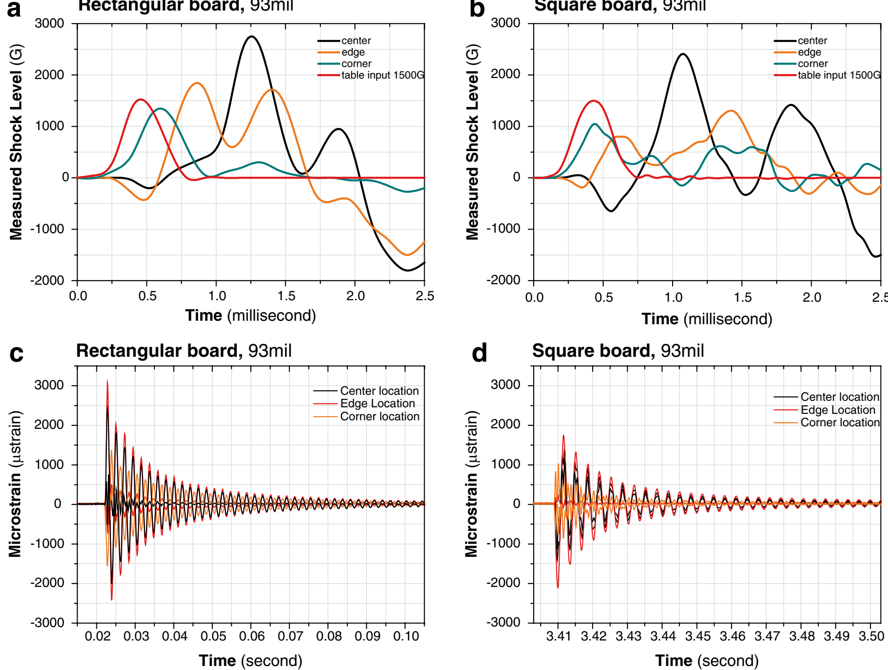
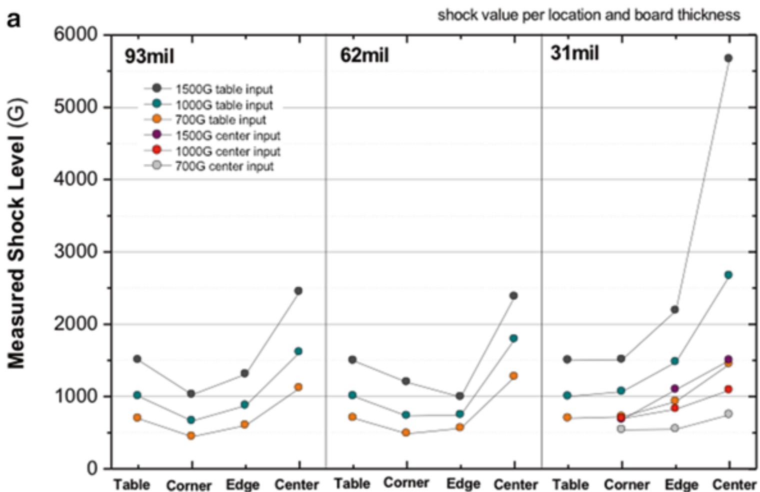


Fig. 6.18 Test size and layout. (**a**) JEDEC B111 board layout (**b**) Large package shock board layout and (**c**) Modified square board layout. (**d**) side view for each board for shock testing

board, which shows the opposite. But the maximum G and maximum strain values are not always the decision makers for the solder joint stability. As shown in Fig. 6.20, the strain response after the first maximum peak has a different fluctuation pattern, which ultimately affects the energy that needs to be consumed by the solder joint before it breaks, the cycle number per time (frequency), and the duration that affects the solder joint stability and determines whether joint failure occurs early or late. For example, the strain for the 31 mil board in Fig. 6.20d shows a higher peak strain compared to the 2.36 mm (93 mil) board strain response, but the strain fluctuation frequency for a given time frame is much less for 0.79 mm (31 mil) compared to the higher frequency of 2.36 mm (93 mil) strain response. Of course, the strain fluctuation and peak value differ with the component location, which is because the shock G level at each component location is different as shown in Fig. 6.20a–c. With these examples, we can see that it is not only the shock G level and the strain maximum peak value that impact the solder joint mechanical stability but also the location of the component and the interaction between the shock-induced strain and the board, which influence the fluctuation of the strain. But this is not all the factor which needs to be considered. The interaction between the strain and the solder joint itself is a critical factor, which we will see in the next sections.

Board-Side Pad Design Effect: NSMD Versus SMD

The failure induced by shock is “a strong function of the combination of the board design, construction, material, thickness, and surface finish; interconnect material and standoff height; and component size” [16]. One additional consideration is the pad design on the PCB side. As shown in Fig. 6.21, from a mechanical bonding point of view, a non-solder mask-defined pad (NSMD)-designed board is different than a solder mask-defined (SMD) board. The NSMD pad shown in Fig. 6.21a has more area of bonding between the Cu pad and the solder ball than the SMD pad. After reflow, the solder ball completely covers and grabs/surrounded the Cu pad; the solder therefore has a larger bonding interface area than the package-side interface. The SMD pad design solder joints are expected to be more directly affected by interface microstructure evolution than NSMD pad-designed boards. This is due to the balanced condition between the package and board-side interface. Both the board side and package side have the same interface bonding area and have no geometrical differences; thus, both the package side and board side have equal potential for local deformation and fracture. With a given shock wave, the potential failure initiation site for the NSMD pads are at the lower part of the Cu pad corner, the interface between the Cu pad, and the laminate on the board side. Compared to the NSMD, the SMD pads have their potential failure site at the interface between the solder and the Cu pad, where the solder bulk is exposed right above the IMC interface layer. We will see the influence of the board-side pad design in the following sections, where the pad design plays a crucial role deciding the failure mode per given isothermal aging preconditions and solder alloys.



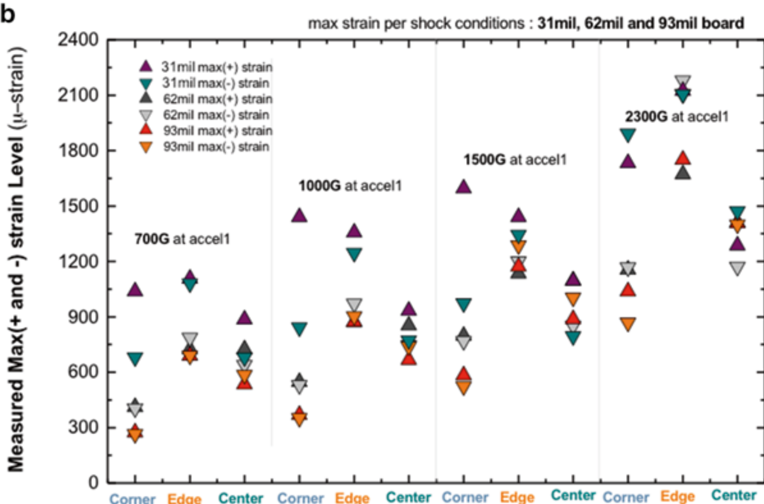


Fig. 6.19 Measured Maximum Shock G level and maximum (+ and −) strain per board thickness and component location. (**a**) Shock level per location and board thickness. (**b**) Strain per location and board thickness. It is interesting to see that the thinner board has lower strain due to the lower weight of the board

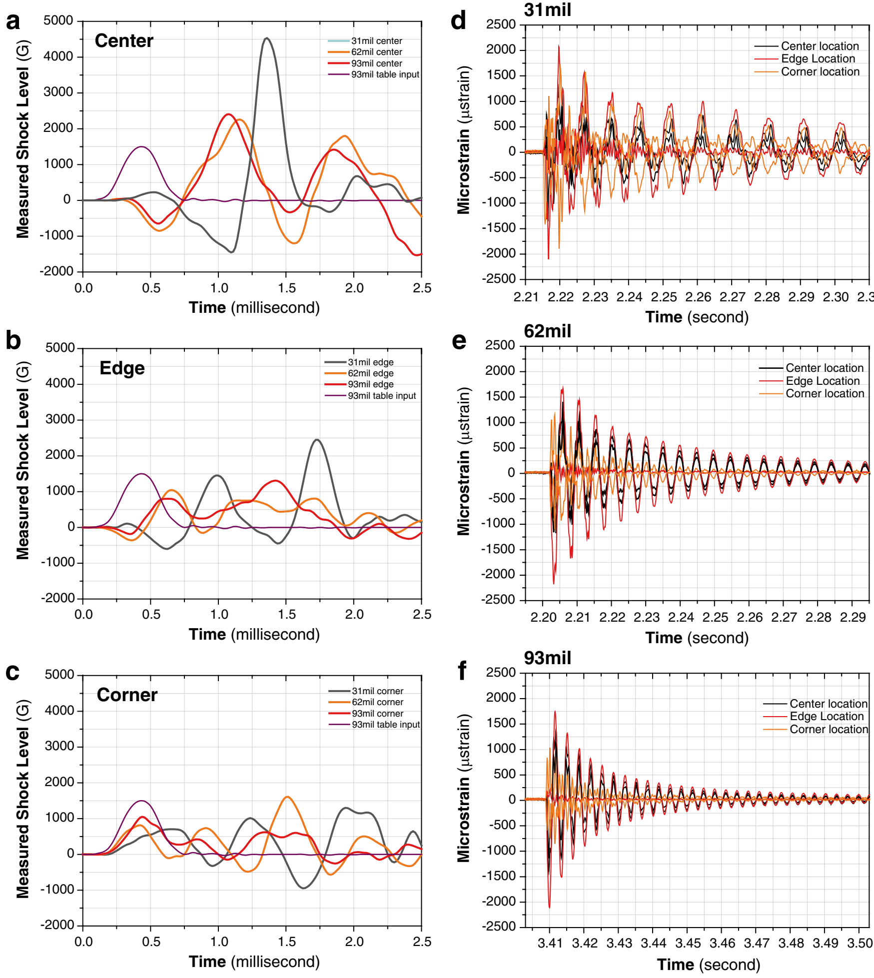


Fig. 6.20 Measured Shock G level plot and strain plot per board thickness and component locations. The shock G level at each component location is different as shown in (**a**–**c**). The strain response in (**d**–**f**) after the first maximum peak has a different fluctuation pattern, which ultimately affects the energy that needs to be consumed by the solder joint before it breaks. The strain fluctuation and peak value differs with the component location

Isothermal Aging Effect on Mechanical Shock

As addressed in Chap. 4 and the impact to thermal cycling performance addressed in Chap. 5, the isothermal aging brings the SAC305 solder microstructure to a transition at two regions. One is the solder bulk and the other one is the interface. The solder bulk become more soften with larger accumulated IMC precipitates, and

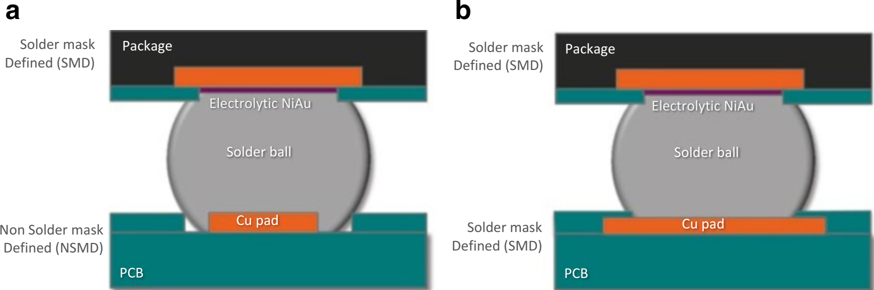


Fig. 6.21 Schematics of cross sections for (**a**) Non solder mask defined board pad design (NSMD) and (**b**) Solder mask defined board side pad design (SMD)

based on the surface finish, some local area near the interface show precipitation-free zones, and the once dendrite-shaped beta Sn with eutectic IMC decoration around it become a more equiaxed grain structure. At the same time IMC thickness increases and shape transformation occurs at the interface. The scallop-shaped IMC structure or a needle-shaped IMC structure are developed at the interface without Ni and with Ni element-contained surface finish and become thicker with a uniform thickness after isothermal aging. The effect of these microstructure evolutions before and after isothermal aging on shock performance can be seen in the following example with 17 × 17 mm FCBGA component shock performance on 2.36 mm (93 mil) thickness boards. The initial microstructure for both package- and board-side interfaces is shown in Fig. 6.22 before and after aging. The shock test was applied utilizing the standard standoffs and 1,500G shock level cycles at the center location of the board. The shock test results are shown in Fig. 6.23. The Weibull plots before and after isothermal aging at 100 and 150 °C for 500 h without regard to the component location on the boards showed a continuous degradation from corner to edge to center and also depending on aging throughout the samples. Focusing on the first failures, the 150 °C/500 h-aged samples failed first followed by 100 °C/500 h-aged and the no-aged samples, and the overall characteristic lifetime cycle number was around 100 cycles. Compared to the NSMD SAC305 samples, the SMD SAC305 samples showed a more isothermal aging-dependent result, as the Weibull curves are clearly separated based on the aging conditions, and the characteristic life cycle number showed a distinct degradation of characteristic life due to isothermal aging. The dye-and-pry analysis, to identify the failure location and failure mode, is shown in Fig. 6.24. It reveals that all the fractures in the NSMD pad test board before isothermal aging were laminate cracks at the board side, regardless of package position on the board. Figure 6.24b shows the dye-and-pry results for the 150 °C/500 h preconditioned components following shock testing. Laminate cracks at the board side were observed as the major failure mode in addition to some failures at the package-side interface. Compared to the mostly laminate crack failure mode in NSMD pad design board samples, the dye-and-pry results for the SMD pad

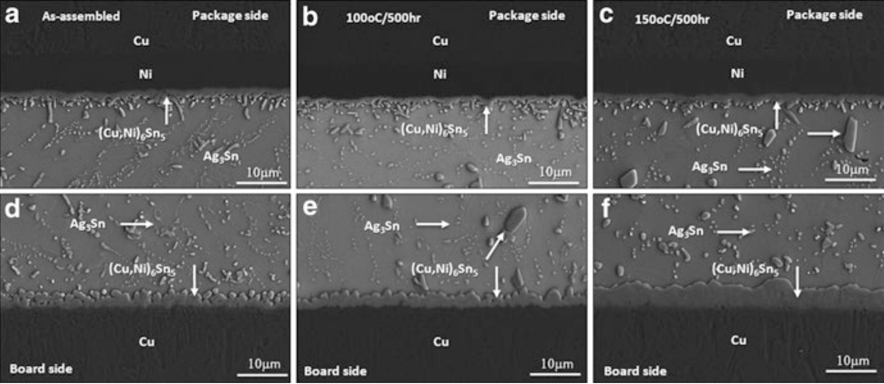


Fig. 6.22 Scanning electron microscopy cross section microstructure of package side (**a, b, c**) and board side (**d, e, f**) before aging (**a, d**), after isothermal aging at 100 °C/500 h 500 h (**b, e**) and after aging at 150 °C/500 h (**c, f**)

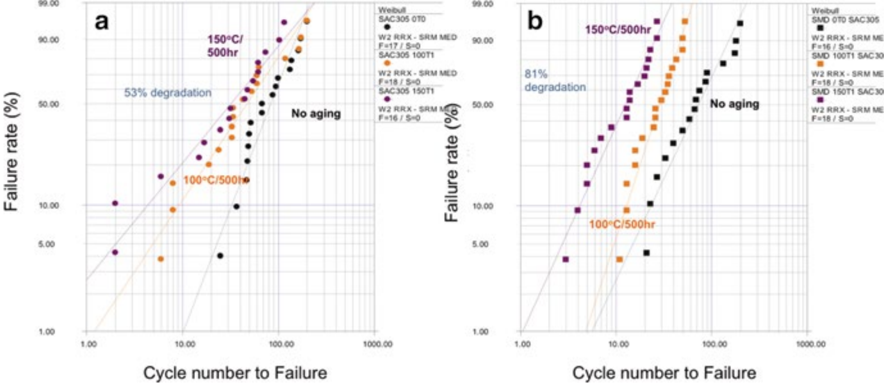


Fig. 6.23 Number of shock to failure Weibull plot before and after isothermal aging. (**a**) NSMD pad test board and (**b**) SMD pad test board results

test board showed different failure modes. As shown in Fig. 6.24c failure occurred primarily at the package- and board-side interfaces, and just a few failures occurred at the board laminate.

While the NSMD test board results showed a stronger joint configuration at the board side, the SMD pads had equal potential for crack development at both the package- and board-side interfaces. This competition between the major crack propagation paths can be seen in the cross-section images shown in Figs. 6.25 and 6.26. In Fig. 6.25, the cross-section SEM from an NSMD sample solder joint after shock

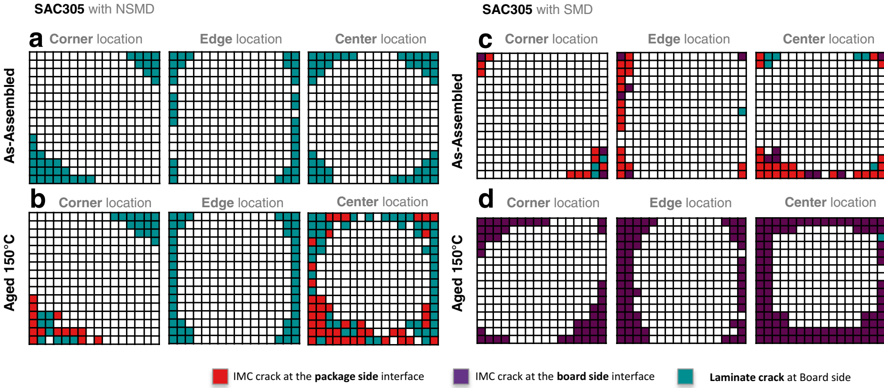


Fig. 6.24 Dye and pry fracture distribution maps after shock test: (**a**) SAC305 with NSMD pad design shock tested right after assembly and (**b**) shock tested after isothermal aging at 150 °C/500 h. (**c**) SMD pad design shock tested before aging and (**d**) tested after isothermal aging at 150 °C/500 h

shows the laminate crack propagated under the Cu trace and eventually cracked the Cu trace (as indicated with white arrows). With the isothermal aging at 150 °C/500 h, the sole failure mode at the laminate begins to show a mixed failure mode, both at the laminate- and the package-side IMC interfaces. On the other hand, Fig. 6.26 is the images from an SMD sample. This time, cracks were observed at both the package-side and board-side IMC interfaces, and after isothermal aging, the board-side IMC interface was the dominant failure mode. The cracks at the board-side interface, shown in Fig. 6.26c, f, were propagating through the $(Cu, Ni)_6Sn_5$ intermetallic compound (IMC). The crack propagation path for no-aged samples are more difficult to proceed because the crack needs to penetrate the bulk solder and the IMC, but for 150 °C/500 h-aged samples the crack propagation is much easier resulting in a shorter life cycle time than the no-aged samples. With the help of an EPMA analysis, we can see that the crack was actually propagated through a region between a higher Ni concentration region and a low Ni concentration region shown in Fig. 6.27. A crack propagation through the lower part of the Cu_6Sn_5 IMC can be observed often in other interfaces too. Figure 6.28 is a shock-induced crack propagation for a large FCBGA component before and after aging at 75,100 and 150 °C. With the shape/geometry change of the IMC, the crack path and the relatively ease or difficulty of the crack propagation rate are defined. In this case the 75 °C aged sample showed the lowest shock performance compared to the 150 °C aged sample, which showed the best performance. Unlike the no-aged interface, the 75 °C aged sample interface begins to have a continuous layer of Cu_6Sn_5, and this makes the joint more easy for crack propagation. For the no-aged sample interface, the crack needs to propagate partially through the bulk solder and then back to the IMC and then back to the bulk solder, etc. so the crack propagation is mitigated in some sense. With the same point of view, the 150 °C aged sample with a thicker IMC for both Cu_3Sn and Cu_6Sn_5, the crack propagation is much more difficult, due

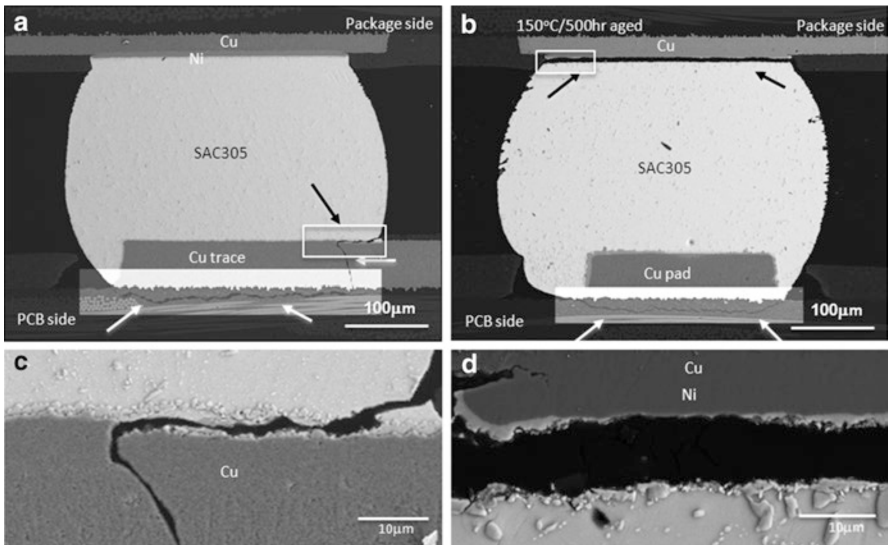


Fig. 6.25 Scanning electron microscopy cross section microstructure of an NSMD sample solder joint after shock shows the laminate crack propagated under the Cu trace and eventually cracked the Cu trace (as indicated with *white arrows*). (**b**) With the isothermal aging at 150 °C/500 h, the failure mode at the laminate begin to show a mixed failure mode, both at the laminate and the package side IMC interface

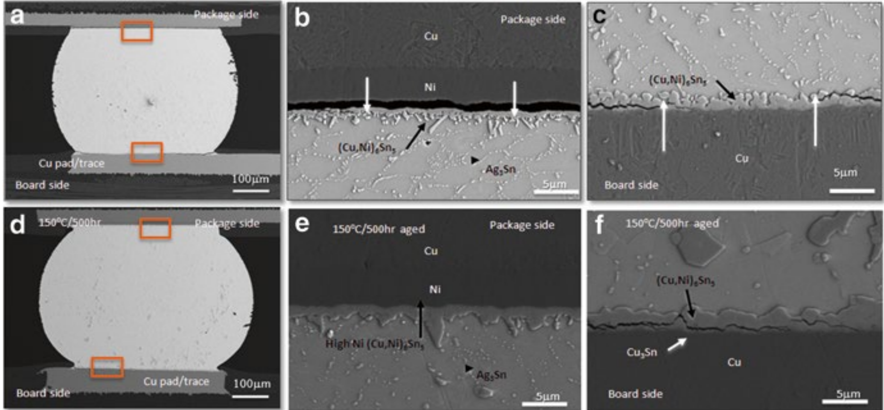


Fig. 6.26 Scanning electron microscopy cross section of shock tested microstructure for unaged package (**a–c**) and package aged at 150 °C/500 h (**d–f**) at low magnification (**a, c**), and at high magnification at locations shown in *boxes* in (**a, d**) along package side (**b, e**) and board side (**c, f**). Crack locations are indicated by *arrows*

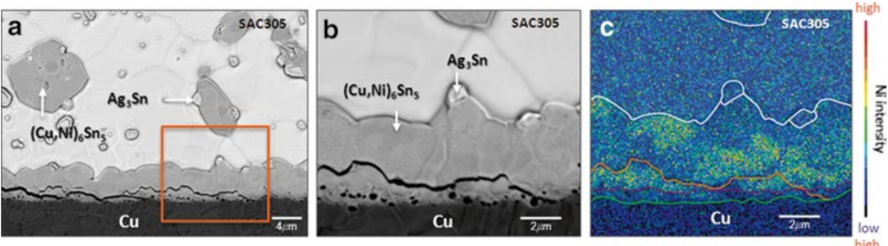


Fig. 6.27 EPMA mapping overlapped on SEM microstructure. Both are SMD pad design samples with (**a**) SAC305 after isothermal aging at 150 °C/500 h and shock tested. (**b**) Higher magnification area indicated in (**a**). (**c**) EPMA map overlayed on (**b**)

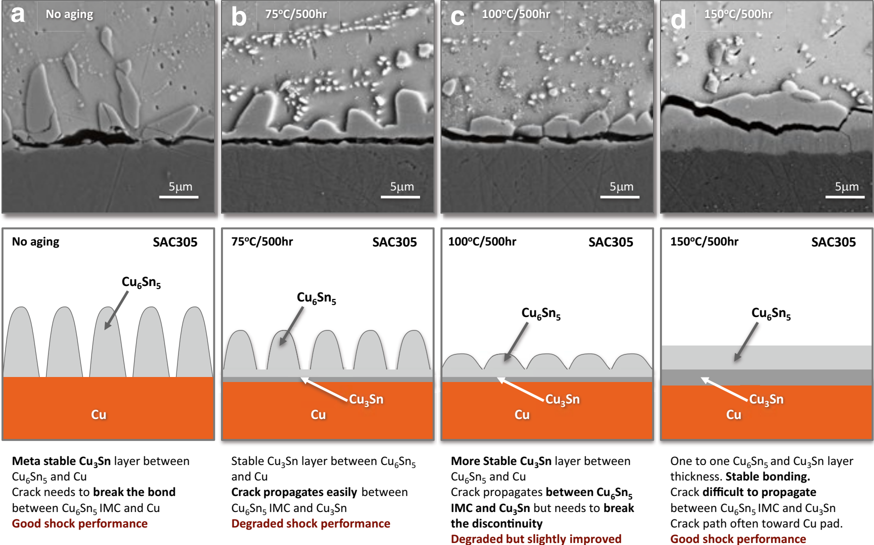


Fig. 6.28 Fracture path based on isothermal aging induced IMC geometry differences. Schematic drawing on the interface after isothermal aging associated with SEM structure after aging

to the irregular interface in between the Cu_6Sn_5 and the Cu_3Sn. The Cu_3Sn IMC layer is an equiaxed columnar grain structure, and the Cu_6Sn_5 covers several of the equiaxed Cu_3Sn grain, thus making the horizontal crack propagation difficult.

Like these examples, the IMC interface thickness, shape distribution, composition, and uniformity is closely related to the stability against shock and is crucial defining the shock performance. But even though IMC interface is often the path where the crack propagates, it is not the only factor which defines the shock performance. We will see another factor in the next section, which can degrade or improve the shock performance, the solder bulk itself.

Increasing the Capability of Absorption of Shock Energy

With the degradation phenomenon observed as above, the mechanical reliability and stability of the solder joint at higher temperature are challenging, because higher temperature environment means isothermal aging on the solder joint, which can transfer the microstructure of the solder and ultimately degrade the performance level. Then how can we improve the shock performance in these alloy systems. Based on the failure mode, the shock can be improved by enhancing two major regions, the IMC interface at the package and board-side interface and laminate area below the Cu pad.

Thus, adding some microalloy to the surface finish or bulk solder alloy is an active approach along with finding a way to strengthen the laminate with material enhancement or new pad designs. But maybe a more fundamental approach is to increase the capability of the solder joint to absorb the shock energy input caused by external loads. This is an important approach and direction since it can achieve two things at the same time, by not only strengthening the solder joint itself but also reducing the shock energy reaching the IMC interface and laminate area below the Cu pad by mitigating the energy transfer into adjacent weak interfaces. Given that failure locations vary from the package-side interface intermetallics to the laminate area right below the Cu pad or trace, mitigation or delay of crack initiation can be accomplished if a mechanism by which the solder joint bulk can absorb more shock energy [27, 28]. In the next sections, we will discuss about a few mechanisms and methodologies to improve the shock performance, including strengthening the IMC layer with microalloy, increasing the shock absorption with microalloyed bulk solder composition change and altering the initial internal buildup stress. But before going into the methodology, we will begin with a basic comparison between low and high Ag-contained solder joint shock performance and the mechanism which defines the difference.

Low Ag Alloy Versus High Ag Alloy

It is not a new finding that the lower silver content alloy performs better in mechanical shock performance than higher silver content Sn–Ag–Cu solder, which is demonstrated in several reported results [29, 30]. Most of the results were explained by a simple mechanism that less Ag content results in fewer Ag_3Sn IMC precipitates and thus a softer bulk solder compared to higher Ag solder alloys. This softer bulk material transfers less shock-induced strain at the interfacial stress concentration locations, resulting in a better shock performance, which is true and a valid explanation. With isothermal aging, the IMC particles coarsen into larger, fewer, and more widely spaced IMCs in the microstructure [29–31], which also provides a softer and more shock-tolerant microstructure. If we can explain the improved shock performance in lower Ag-contained SAC solder by only identifying the difference in hardness value, then we can also reach to a conclusion that isothermally aged SAC305

solder joints, which has lower hardness than no-aged SAC305, are expected to have better shock performance compared to no-aged SAC305 solder joints, which is actually not the results we see in SAC305 solder joint shock performances.

Then is there a different failure mechanism in SAC305, higher Ag content solder compared to SAC105, lower Ag content solder joints?

To explain and to understand the mechanism, we need to look into the microstructure evolution during shock test. We will compare SAC105 solder alloy with SAC305 solder alloy to assess the effect of isothermal aging and local recrystallization on high G board-level shock performance, observe and discuss the different shock-induced microstructure changes, and try to find the right mechanism, which defines the shock performance and solder joint stability.

The initial microstructure for both SAC105 and SAC305 is shown in Fig. 6.29. With lower Ag content (SAC105), the Ag_3Sn IMC precipitates are less in number thus overall showing a lower hardness value compared to SAC305, which has fine IMC precipitate distribution. Both SAC105 and SAC305 show an accumulation of these IMC precipitates after isothermal aging with interface IMC thickness increase. The shock test was performed with 12 × 12 mm CABGAs assembled on a 1.57 mm (62 mil) board with the test condition B (1,500G, 0.5 ms shock pulse).

Figure 6.30a, b shows the compiled shock test Weibull plots for each aging condition and solder alloy composition. Overall, there are higher numbers of cycles to failure for SAC105 than SAC305 before or after aging. In contrast, the SAC305 samples show a much lower unaged characteristic life cycle number of 42 cycles, but it degraded further to 12 cycles after aging at 150 °C for 500 h. Since the thickness of the IMC at both package and board-side interface increased, both SAC105 and SAC305 solder joints are expected to show degraded shock performance. But the shock performance of SAC105 solder joints improved with aging. The consolidated plot for each condition with regard to the component location on the board

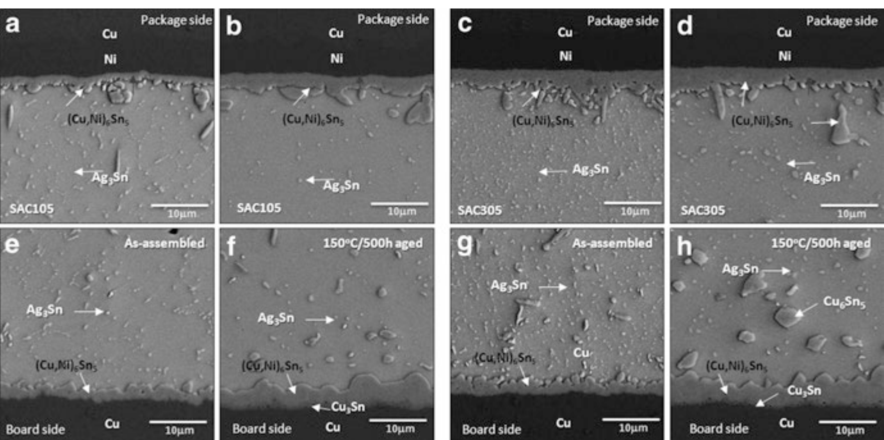


Fig. 6.29 Scanning electron microscopy cross section microstructure of SAC105 (**a**, **e**) before aging and (**b**, **f**) after aging at 150 °C/500 h. SAC305 before aging (**c**, **g**) and after aging at 150 °C/500 h (**d**, **h**)

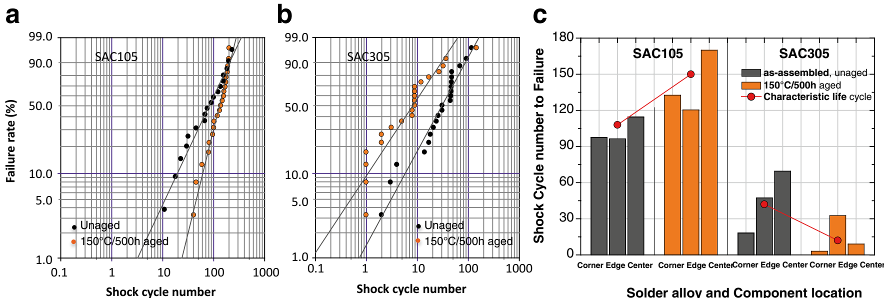


Fig. 6.30 Weibull plots for shock test results on the isothermal aged BGA samples: SAC105 (**a**) and SAC305 (**b**). (**c**) Number of cycles to failure and characteristic life cycle number based upon component location and isothermal aging conditions for SAC105 and SAC305

shows the trend more clearly in Fig. 6.30c, and this trend is consistent for every package location on the test board. The center component showed an especially high improvement rate compared to the corner and edge locations in SAC105. SAC305 on the other hand shows the highest degradation rate for the center-located components. Given that this opposite aging effect is greatest at the center location, which also has high strain level and shock level per test cycle, those solder joints at the center location are good joints to look into the microstructure and were selected for further observation. The cross-section-polarized light microstructure of the outermost five joints on each side of the outside edge is shown in Fig. 6.31. The crack locations are typically at the upper interface or in the laminate below the board-side copper pad, as indicated by an outlined box. Most of the unaged solder joints before shock test have single, bi-, or tri-crystal structure with a small number of grains per joint for both SAC105 and SAC305. However, after shock testing, the SAC105 microstructure revealed development of a fine grain (possibly recrystallized) microstructure that is much finer for isothermally aged than the unaged samples. This transformation from single or dual grains to multigrain or fine localized grain structure may account for better absorption of the shock-induced strain energy. The transformation from single to multigrains during shock cycling produced many additional grain boundaries. As there are elastic discontinuities at grain boundaries that cause local stress variations, dislocation generation at grain boundaries is likely. With this microstructural transformation, the shock strain energy can be absorbed in two ways: by motion of dislocations nucleated at grain boundaries and by grain boundary sliding so that the shock conveyed to the interface region is reduced. This form of energy consumption will increase in proportion to number of new grain orientations and/or grain boundary area. This transformation during the shock cycling thus can reduce or delay damage accumulation at the high stress concentration locations at the intermetallic interface layer or at the laminate and Cu pad interface. In contrast, SAC305 samples (Fig. 6.31d–f) show much less of a difference in the fine grain microstructure development. The initial grain structure

does not appear to have changed significantly even after isothermal aging and shock testing. This lack of change indicates that the SAC305 is less able to absorb the shock-induced strain energy, so it transfers the shock energy to the weakest interconnection interface, which in this case is the IMC layer at the package side or to the laminate and Cu pad interface, resulting in a much earlier full failure than the SAC105 samples.

Figure 6.32 shows four exemplary cross-section SEM and polarized light microstructures with and without 150 °C/500 h aging and then shock tested to failure for SAC105 and SAC305 joints. The SEM microstructure shows the crack location, and the polarized images show the grain structure associated with the crack. The SEM images revealed shock-induced crack propagation from the package-side interface corner into the bulk solder for SAC105 aged samples. The unaged joint showed a crack propagation initiated from the upper right corner into the bulk, and the aged joint shows crack propagation from both side corners. Also a laminate crack is shown below the Cu pad area in both solder joints, which are L1 joints from two different center components. The corresponding polarized light images show a fine grain structure development at the joint corner region.

In contrast to SAC105, in SAC305 joints, the crack propagated into the laminate region, and there are very few fine grains in the SAC305 joints. This contrast suggests that the fine grain structure provides much more energy-absorbing sites with

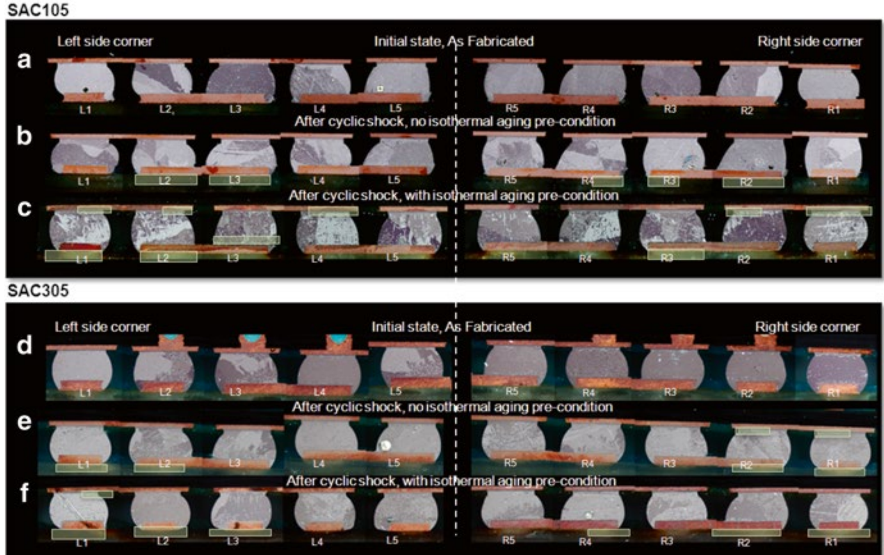


Fig. 6.31 Polarized light microstructure cross sections of the 10 joints marked in Fig. 1 before and after shock testing. (**a–c**) SAC105 and (**d–f**) SAC305. As assembled (**a, d**), after shock test (**b, e**), and after 150 °C/500 h aging and shock test (**c, f**). The crack locations are indicated by *boxes*

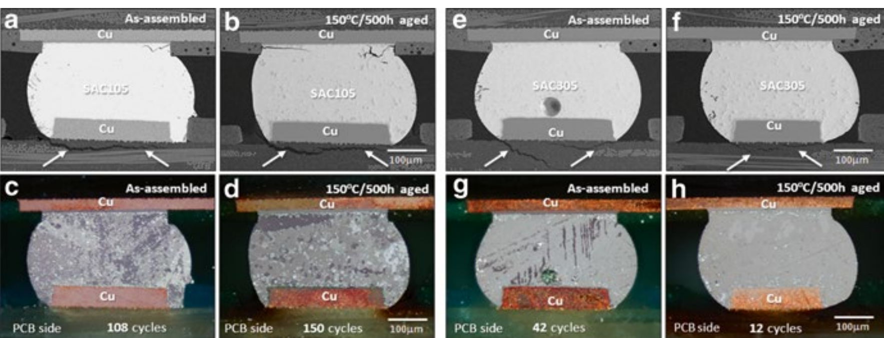


Fig. 6.32 Selected cross-section SEM and associated polarized image microstructure before (**a, c, e, g**) and after 150 °C/500 h aged (**b, d, f, h**) and then shock test to failure for SAC105 (**a–d**) and SAC305 (**e–h**). The SEM microstructure shows the crack location in the joint and laminate (*white arrows*) (**a, b, e, f**) and the polarized images show the grain structure associated with the characteristic life cycles to failure indicated (**c, d, g, h**)

the increase in the number of grain boundaries. The compliance and easier deformation of SAC105 bulk solder in the interconnects led to the better absorption of the shock-induced strain energy, which in turn resulted in multigrain or finer grain microstructure development, possibly through both dynamic and static recrystallization during and following each shock event. Without the fine grain structure development in SAC305, deformation of the bulk solder was difficult and little shock-induced strain was absorbed, which ultimately transferred the stress and strain directly to the IMC and the Cu trace laminate interfaces, resulting in an earlier crack initiation and propagation than the more shock-absorbing SAC105. In addition to the effect of the alloy composition and precipitate microstructure, isothermal aging increased the shock absorption capability and actually improved the shock performance in SAC105. After isothermal aging in the SAC105 joints, the bulk solder became softer, which further promoted bulk solder deformation and increased absorption of the shock-induced strain energy. Due to the increased strain energy absorbed, microstructure features such as IMC precipitates coarsening and consequently wider particle spacing occurred, which favored dislocation accumulation that enabled recrystallization. But in SAC305, isothermal aging degraded the shock performance. Even though the hardness decreased after aging, the ability to transform the single-grain structure to a much finer multigrain structure was not accelerated, thus the ability to absorb the shock energy was not increased, and the thicker IMC layer at the interface resulted in a weaker interface structure that ultimately resulted in a degraded shock performance after aging.

In this section, we learned that if the solder joint can absorb more shock energy by single to multigrain transformation or by developing more grain boundaries with recrystallization, we can have an improved shock performance. In this case we saw the difference between the low and high Ag solder alloy comparison, but is there any alternate method to increase the capability of the joint to absorb shock energy?

The Cooling Rate Effect

As we saw in the former section, if we can accelerate or trigger the single to fine multigrained structure during shock test, we can improve the shock performance. Then what kind of methodology can we bring into the solder joint to accelerate this phenomenon? One of the methods is by controlling the cooling rate. With fast cooling, the solder joint tended to build up more stress, which generated more dislocation activity, which can be released by recrystallization during shock impact. In contrast, slow cooling can lead to the development of mechanical twins, and these interfaces provided more locations for energy dissipation during shock and thus extended the lifetime (if there is no large-scale microstructure evolution to release the stress right after cooling). Once if the internal stress is maintained and then triggered to be released during shock test, then we can have a more accelerated fine grain structure transformation, which can absorb the shock energy and delay the crack initiation and propagation.

Figure 6.33 is the microstructure before and after shock testing, after applying three different variation cooling rates from slow to fast cooling. For the normal cooled samples, we can observe an overall grain number increase after shock testing, but compared to the normal cooled samples, the fast cooled sample shows a dramatic increase of fine multigrained microstructure right after shock test. This fine grain structure transformation can absorb a huge amount of shock energy, contributing to delay the crack initiation or propagation, which resulted in an improved solder joint shock performance. In this experiment, 12×12 mm CABGA with 0.5 mm pitch were used, and the fast cooled samples were cooled with a cooling rate of 75 °C/s. The shock result came out as we expected. A 140 % increase in cycle number to failure with the fast cooled samples as shown in Fig. 6.34. The slow cooled samples also show improved shock performance compared to normal cooled samples.

Microalloy Effect: Pd

An additional way to improve the shock performance is by shock absorption with facilitating mechanical twin formation. Like single to fine multigrained structure transformation, mechanical twins can form by shock-induced strain but also can be facilitated with microalloy addition to the solder joint composition. The effect from the microalloying can be also seen in higher Ag-contained SAC305 solder alloy. This is actually an interesting phenomenon from an industry application point of view because it is known that having a higher Ag content shows better thermal cycling performance than SAC105 solder alloy. But with maintaining the thermal cycling performance, if there is a method to facilitate the twin formation for improving the shock performance simultaneously, it will provide good practical applications.

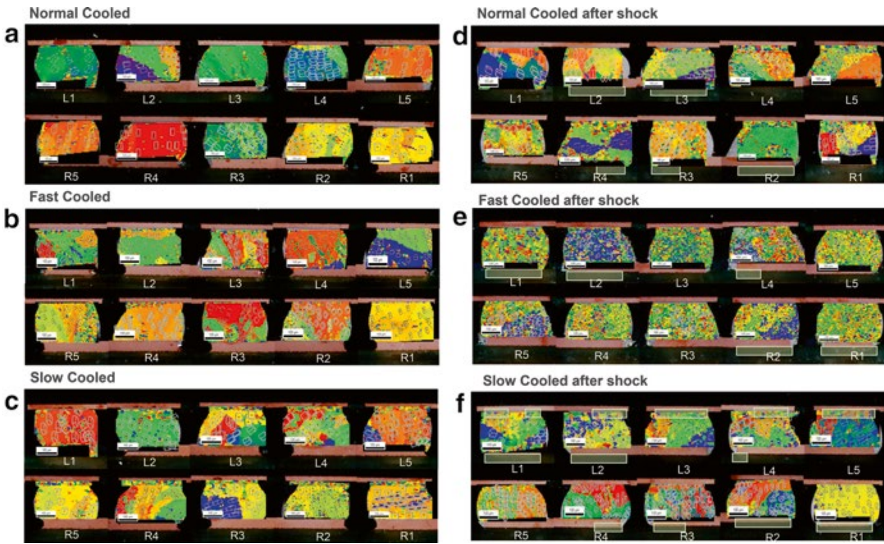


Fig. 6.33 OIM images for sample before and after shock test per three different cooling conditions. Before shock test (**a**) Normal cooled, (**b**) Fast cooled, (**c**) slow cooled. After shock testing (**d**) normal cooled, (**e**) fast cooled, (**f**) slow cooled. Fractured crack locations are indicated in *white box*

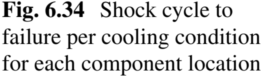
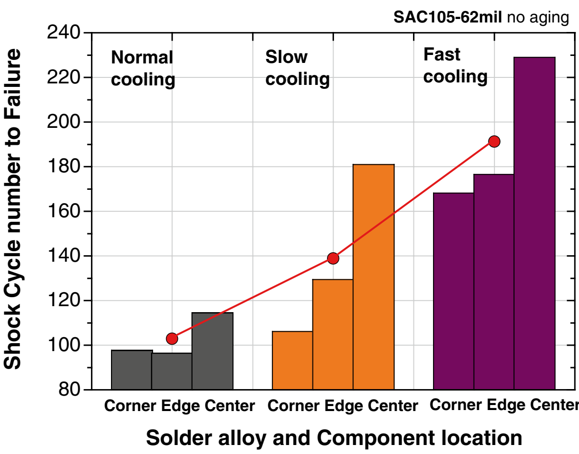


Fig. 6.34 Shock cycle to failure per cooling condition for each component location



Among the elements, which can induce accelerated twin formation is Palladium (Pd). As shown in Fig. 6.35, the SAC305 + Pd solder joints showed an overall higher cycle number in each location, which leads to a cumulatively higher characteristic life cycle number as summarized in Fig. 6.35c. The characteristic life cycle number for the unaged condition improved 65 % by adding Pd to NSMD pad samples, and the trend of improved shock performance was even greater for the 100 and 150 °C aged conditions, 132 % for 100 °C aged, and 102 % with 150 °C aging. However,

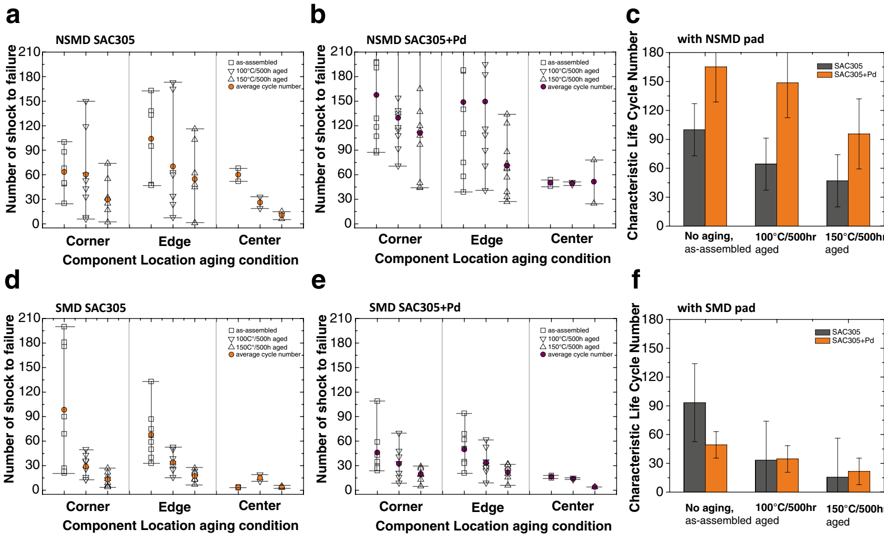


Fig. 6.35 Number of cycles to failure based upon component location and isothermal aging conditions for NSMD (**a–c**), and SMD (**d–f**) pad designs for SAC305 (**a, d**) and SAC305 + Pd (**b, e**). Characteristic life cycle number summary comparisons of aging conditions illustrate the strong benefits of Pd for the NSMD pad (**c**) but not for the SMD pad design (**f**)

with the SMD pad design, there was little to no improvement of shock performance, as shown in Fig. 6.35d, e, where the location-based cycle to failure numbers are similar for SMD SAC305 and SAC305 + Pd samples. To assess a potential explanation for the beneficial effects of Pd, the Sn grain microstructure was analyzed using OIM to examine how the microstructure changed before and after shock testing for NSMD SAC305 and SAC305 + Pd samples. OIM scans were performed, and the OIM images are overlaid on the cross section where the cracks are identified in a manner similar to that reported in [32]. As shown in Fig. 6.36, the SAC305 OIM microstructure after the shock test shows no obvious change in the microstructure from the as-solidified microstructure and shows joints containing mostly single-crystal orientations. In contrast, the Pd containing joints shown in Fig. 6.36b, d show many more interfaces and refinement features in the microstructure while retaining the as-solidified large grain features. Two particular SAC305 + Pd solder joints A16 and B16 show localized grain refinement or recrystallization and significant twin deformation inside the bulk solder joints, which are enlarged in Fig. 6.36e, f. The finer precipitate structure increases the hardness and, hence, raises the yield stress, which is a condition that is often necessary to stimulate deformation twinning in other materials [33]. In joints A16 and B16, active deformation twin structures are evident, which are rarely observed in SAC305 samples. Given the fact that the SAC305 + Pd solder joints exhibit more deformation twin grain refinement features following the shock test, activation of deformation twins may dissipate strain energy within the joint and thus may provide an explanation for why SAC305 + Pd can absorb more shock-induced impacts than SAC305, resulting in a high characteristic cycle number to failure.

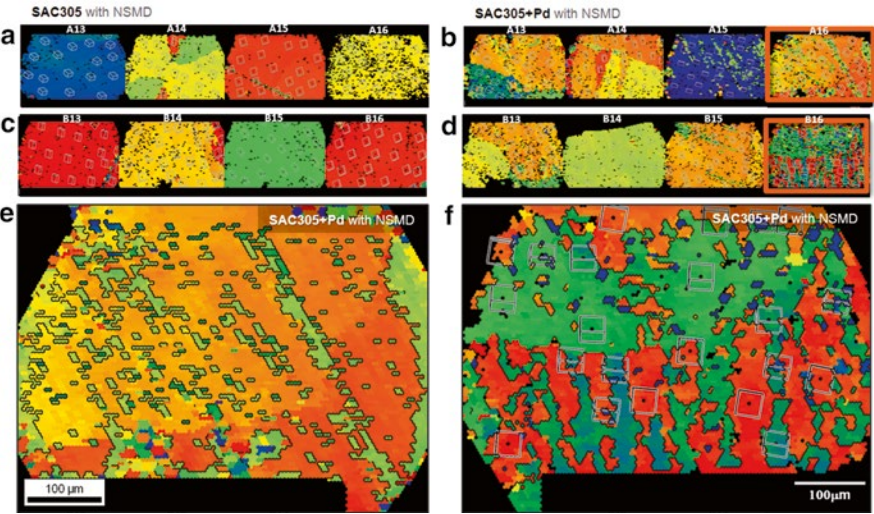


Fig. 6.36 OIM images from cross-section images for SAC305 (**a**) unaged and shock tested from U4 (Fig. 2) side B, (**c**) shock tested, from U6 side A. SAC305 + Pd (**b**) unaged and shock tested, from U4 (Fig. 2) side B, (**d**) shock tested, from U6 side A. (**e**) higher magnification of Fig. 10b joint A16, (**f**) higher magnification of Fig. 10e joint B16

Hence, the activation of deformation twinning has the most influence in conditions where the board interface strength is sufficient to sustain a higher stress (which may never be reached in the SMD geometry because IMC interface cracks can form at the maximum stress concentration location). The effect of the Pd to induce mechanical twinning to dissipate energy allows more cycles before essentially the same number of failure sites is achieved in the NSMD design without Pd. Also, it is evident that the mechanical twinning energy dissipation reduces the driving force for package-side interfacial cracks.

Summary

Mechanical stability is emerging as critical reliability concern with a rapid expansion but not limited to mobile electronics. In order to properly apprehend their risk factors to the reliability, this chapter described the threat from each mechanical load and the mechanism by which the solder joint fails. This chapter describes the reliability performance and failure mechanisms of Pb-free solder joints under various mechanical load conditions, including bending, cyclic bending fatigue, and mechanical shock. The structural stability of solder joint under such mechanical loads is an important consideration factor for the current and future solder interconnects because

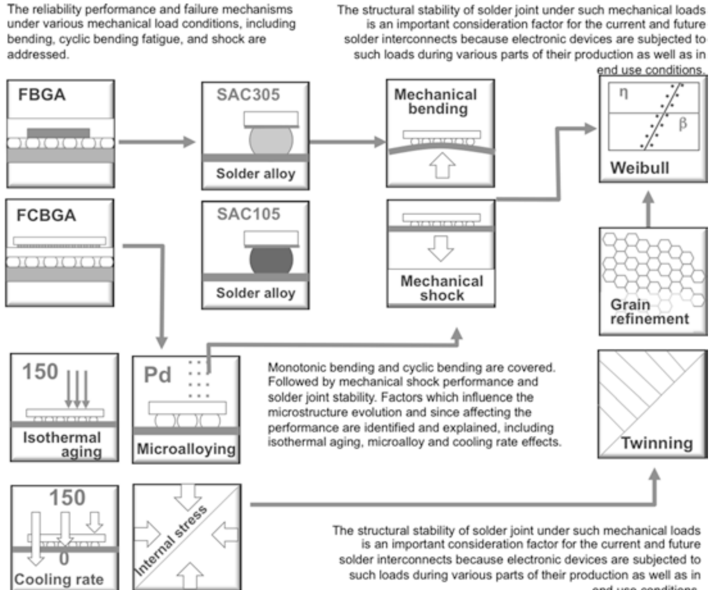


Fig. 6.37 Overall summary diagram of Chap. 6

electronic devices are subjected to such loads during various parts of their production as well as in diversified end-use conditions. As shown in Fig. 6.37, the summary of this chapter is presented schematically. As described in the earlier part of this chapter, the identified factors and approaches we discussed can elucidate how deformation mechanisms operate. The learning leads us to the thought process on how to emphasize and utilize the capability of the solder joint and how much energy it can absorb, which ultimately defines and improves the mechanical stability of the system.

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Chapter 7
Chemical and Environmental Attack

With wider application and installation environments of electronic devices, the influence of the external environment on the reliability of the device is an increasingly important factor. For example, the expanding market for wearable electronics exposes the device to human sweat and related biochemical environments. Also, more equipment is being placed in industrial regions with increased air pollution components such as H_2S combined with humidity, which can cause corrosion on exposed Cu and Ag in some end-use conditions. As for the solder joint itself, Sn is considered as a corrosion-resistant material. In early adaptation of Sn–Pb eutectic alloys in electronics, not much research was performed since there was no specific corrosion concern. But with the microstructure change from a dual phase eutectic structure to a Sn microstructure with equiaxed IMC precipitate islands, a potential galvanic couple is formed, which allows the Sn-based solder to corrode. Solder joints exposed in a saltwater fog environment reveal that Sn–Ag–Cu solder joints can be degraded and that corrosion can occur along the basal plane of the Sn grain structure. This localized pre-crack development at critical localized regions can accelerate degradation in thermal cycling performance. Mitigation methods such as conformal coating will be briefly described at the end of the chapter.

Corrosion in Solder Joints: Introduction

As noted in Chap. 1, electronic products and assemblies are deployed in a wide range of environments for a variety of applications and can be subjected to a diverse array of extreme conditions [1, 2]. Given the fact that Pb-free solder has not been in use in the field for a long time, the amount of data concerning corrosion properties of Pb-free products are limited. Because Sn has shown good corrosion resistance for hundreds of years in the food industry (e.g., tin can), aggressive chemical environments have not been high on the priority list during the conversion from Sn–Pb to lead-free solder. But along with the wider application and installation environments

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T.-K. Lee et al., *Fundamentals of Lead-Free Solder Interconnect Technology*,
DOI 10.1007/978-1-4614-9266-5_7

of electronic devices and with higher density circuits and systems that need higher power consumption and thus more airflow for cooling, the effect of the outside air quality and the end-use environment have become important factors.

Another recent major driver is the expanding market for wearable electronics. Holding a smartphone or portable devices in hand and health-related mobile devices exposes the device continuously to human sweat and related biochemical environments. These applications are significant because phone manufacturers encourage users to carry their phone while exercising [3]. If a phone is not protected in a waterproof case during exercise, it can be exposed to a considerable amount of moisture and humidity. Perspiration can enter the phone through the USB port, the microphone, the headset port, or the keypad and ultimately provide chances to corrode metals inside the phone. Exposure to moisture can occur while regularly operating a mobile phone, but perspiration from exercise is more corrosive [4–7].

One of the most common reasons for electronic failure for industrial equipment is from environmental contaminants. The list of contaminants includes fine and coarse particles of chlorides, sulfates, sodium, ammonium, potassium, magnesium, and calcium. The single most important environmental condition affecting corrosive behavior (such as sulfur dioxide and nitrogen oxides) is relative humidity. The contaminants vary in size depending on their origin. Coarse particles (2.5–15 μm) are typically formed as a result of human activity [8] or originate from soil. Fine particles (0.1–2.5 μm) come from the combustion of fossil fuels and, at times, from volcanic and geological activity and are the main source of contaminants in industrial fields. In electronic devices, coarse particles may cause malfunctions by interrupting electrical contact between mating pairs of contacts on connectors or relays but typically require higher relative humidity conditions to cause problems than the fine particles. Among all the potential contaminants, sulfidation of copper and silver has been a problem since antiquity and is well known in museum and conservation studies, especially with silver corrosion [9–11]. Sulfidation (or sulfuration) is the corrosion of elemental metal (e.g., silver, copper, etc.) in the presence of sulfur compounds in a liquid or gaseous phase with high relative humidity condition. Figure 7.1 shows an example of corrosion due to sulfur contained air on an electronic device in an industrial field. The exposed Cu pad shows an extended area of corrosion, and the cross section examined using both SEM and EDX shows the distribution of several elements including Cu, which is the base material, with oxygen and sulfur. The initiation of the sulfidation reaction is through the reduction of H_2S to HS^-. In an aqueous solution, HS^- can either react directly with silver ions that have oxidized or they can adsorb onto the surface, subsequently reacting to form a sulfide salt. The presence of an oxidizing species, such as Cl, has been shown to increase the corrosion rate.

Of course the time to failure is dependent on many variables such as: sulfur levels, product type, surface finish type, amount of exposed area, and possibly temperature and humidity levels, air flow, flux residues, etc. In general, as shown in Table 7.1, according to the International Society for Automation (ISA) standard, there are four classes of industrial atmospheres with respect to copper reactivity, which are summarized from G1 to G4 depending on the area and depth of the corrosive region [12].

To test or evaluate the electronic device performance against these corrosive environments, several test methods are used in industry. Among them, the mixed flowing gas (MFG) test is a laboratory test, in which the temperature, relative

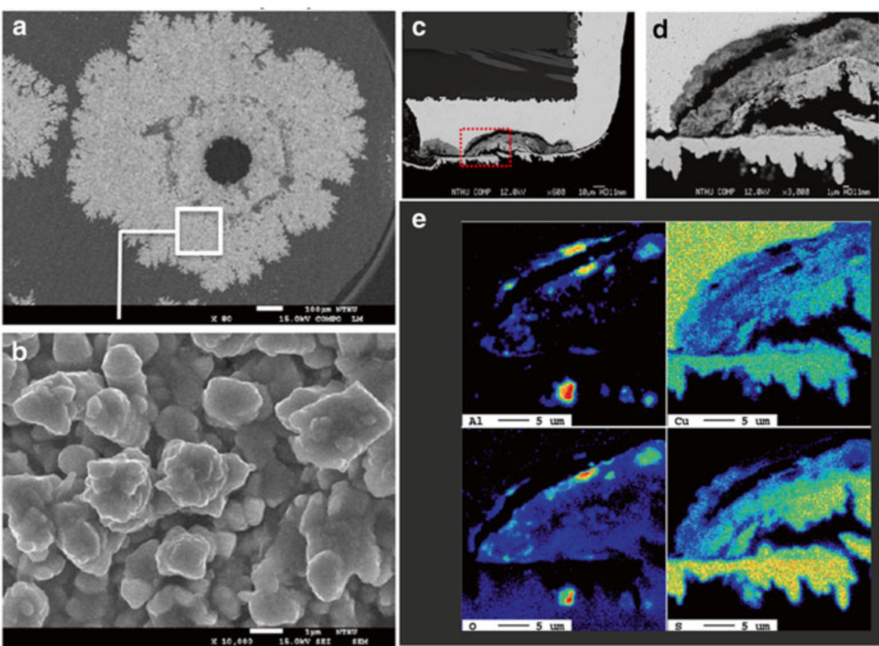


Fig. 7.1 SEM image of a corroded Cu pad after service in a high Sulfur environment. (**a**) *Top view* of the reacted Cu pad. (**b**) Higher magnification of the corroded area. (**c**) Component corner, which was tested in a high Sulfur environment. (**d**) A higher magnification of the interface area between the component metal pad and PCB. (**e**) EPMA map which reveal the high concentration of Sulfur at the reacted interface

Table 7.1 Classification of industrial atmosphere's corrosivity to copper [12]

Class	Description	Expected time to failure
G1 (mild)	Corrosion is *not a factor* (less than 300 Å per month)	No corrosion related failures
G2 (moderate)	Corrosion is *measurable* (less than 1,000 Å per month)	Failure within 3–4 years
G3 (harsh)	*High probability of corrosion* (less than 2,000 Å per month)	Failure within 1–2 years
G4 (severe)	*Considerable corrosion* (less than 3,000 Å per month)	Failure within 1 year

humidity, concentration of gaseous pollutants (ppb level), and other critical variables (such as volume exchange rate and airflow rate) are carefully defined, monitored, and controlled. The purpose of this test is to simulate corrosion phenomenon due to atmospheric exposure [13]. Since there are several elements that can cause corrosion, a mixture of several elements in various concentration levels are used. It is not easy to fix the concentration to one formula to cover all existing industry conditions, so various laboratories and industries identified several representative test formulas. Battelle Labs, Telcordia (previously Bellcore), and IBM are among the groups who used several MFG formulas to accelerate atmospheric corrosion and its effect on electronic applications [14–17]. Later, several organizations developed standardized test methods and guidelines. Among them, ASTM provides a wide review of existing MFG practices summarized in Table 7.2 [18].

Table 7.2 Test conditions of mixed flowing gas tests [18]

ASTM Method	H_2S (ppb)	SO_2 (ppb)	Cl_2 (ppb)	NO_2 (ppb)	Temperature (°C)	Relative humidity (%)	Air changes (#/h)	Air velocity (m/h)	Duration (days)	References
A		25,000 ± 5,000			25 ± 2	75 ± 5		20-60	4,10,21	[19]
B	12,500 ± 2,500				25 ± 2	75 ± 5	5-Mar	20-60	4,10,21	[20]
C		500 ± 100			25 ± 1	75 ± 3	5-Mar	60	4,10,21	[21]
D	100 ± 20				25 ± 1	75 ± 3	5-Mar	60	4,10,21	[21]
E	100 ± 20	500 ± 100			25 ± 1	75 ± 3	10-Mar	60	4,10,21	[21]
G	10 + 0/−4		10 + 0/−2	200 ± 25	30 ± 2	70 ± 2	8-Mar			[14, 22, 23]
H	100 ± 10		20 ± 5	200 ± 25	30 ± 2	75 ± 2	8-Mar			[14, 22, 23]
K	200 ± 10		50 ± 5	200 ± 25	50 ± 2	75 ± 2	8-Mar			[14, 22]
L	40 ± 5 %	350 ± 5 %	3 ± 15 %	610 ± 5 %	30 ± 2	70 ± 2		1,832		[25]
M	10 ± 5	200 ± 20	10 ± 5	200 ± 20	25 ± 1	75 ± 3	10-Mar			[21, 25, 26]
N	10 + 0/−4	200 ± 25	10 + 0/−2	200 ± 25	30 ± 2	70 ± 2	ASTM B827	ASTM B827	30-May	[27]
O	10 ± 5	100 ± 20	10 ± 3	200 ± 50	30 ± 1	70 ± 2	ASTM B827	ASTM B827	10,20	[23]
P	100 ± 20	200 ± 50	20 ± 5	200 ± 50	30 ± 1	70 ± 2	ASTM B827	ASTM B827	20	[23]

Various forms of corrosion or corrosion-induced degradation mechanism exist in electronics, including anodic or cathodic corrosion, corrosion-induced ion migration, fretting corrosion on various surface finishes, and galvanic coupling corrosion. Of course, corrosion itself can bring the device to total failure, but in most cases, it is the combination of corrosion and thermal or mechanical fatigue that accelerates degradation, which is reached earlier than the expected failure. In other words, it is mostly a corrosion-induced degradation that we are looking into [28–35].

Corrosion in Marine Environment

The main failures with sulfur or the MFG occur on Cu and Ag, but not much reaction is observed at solder joints with Sn–Pb or SAC [36]. But other elements actively react with solder joints, which are Cl- ions, which are abundant in salt water. As explained in earlier chapters, electronic devices and equipment are increasingly placed on seashores, cruise ships, and marine rescue vehicles. In these environments the equipment is continuously exposed to salt water or vapor, even in enclosed casings. Due to the high reliability requirement for some devices with long lifetime expectations, the influence of salt water and vapor on the reliability of the products in those environments needs to be quantified and closely monitored. It has been shown in various publications that corrosion-related phenomena depend on the material property and also upon cross functional phenomena with the base microstructure [36–51].

It is well established that tin-based Pb-free alloys are less problematic because of their relatively strong corrosion resistance [5, 36, 37]. It has been reported that the main component of solder alloys, tin (Sn), resists corrosion because of the passivity of the film that forms on its surface [52]. Both Sn–Pb and SAC alloys have a thin oxide layer on the surface, which protects the solder from corrosion. Sn–Pb solder joints have SnO films less than 2 nm thick and are Pb oxidized only if there is no Sn at the surface [41, 42]. Of course, the same SnO layer is present on SAC305 solder joints where the amount of Sn is much greater than that of Sn–Pb, i.e., >96.5 %. Measurement by FE-Auger has revealed a 5 nm thick layer of SnO on the surface of solder joints [53].

By comparing the corrosion resistance of Sn–Pb and several Pb-free solders in 3.5 wt.% NaCl solution, SAC solders show better corrosion resistance due to these passive thin layers. In addition to the thin passivation film, SAC solders were more resistant to corrosion than Sn–Pb solder in a NaCl solution, due to their lower passivation current density, more stable surface passivation film, and lower corrosion current density after breakdown of the passivation film [45]. Various studies show that SAC305 solder exhibits better corrosion resistance than other Sn-based alloy compositions due to its high content of noble or inert elements (Ag and Cu) and its stable structure, in addition to the thin oxide film on the surface [52, 54]. As discussed earlier in Chaps. 3 and 4, Ag and Sn in SAC305 solder react with each other to form a fine network of Ag_3Sn evenly distributed in the matrix and the Cu and Sn

in SAC305 to form Cu_6Sn_5. Since these IMCs are chemically stable, they are nearly insoluble in etchants, making them stable against corrosion.

With these statements and published results, one might reach a conclusion that SAC solders are resistant to corrosion, so that with the conversion from Sn–Pb to Pb-free, we are actually getting into a safer situation because there is more Sn in the solder joint. This is partially true. However, most of the test samples are bulk solder not in a joint configuration. When test conditions are imposed on the whole system (package and PCB), there are potentially different mechanisms that can cause corrosion and affect the joint reliability. One potential risk factor comes from the intermetallic phases at the interface region for both package- and board-side interface. With existing IMCs, which are noble and not corrosive, the nearby Sn region can be affected by forming a galvanic couple with a large difference in electrochemical potential. The same can happen within the bulk solder. Intermetallic precipitates, after growing to a larger size, in addition to functioning as noble materials, may also react with the base material Sn to form galvanic couples. It is already reported that the dissolution of Sn from the Sn–Ag alloy can be accelerated by the presence of Ag [54]. Thus, assessing the environmental impact from an interconnection point of view is important and considered in the following sections.

Salt Spray Test

The salt spray test exposes samples in an enclosed environment to a 5 % sodium chloride (NaCl) aqua solution (or fog) to simulate the effects of a severe marine atmosphere [13]. A standardized 5 % solution of NaCl is known as neutral salt spray (NSS). The chamber setup, testing procedure, and testing parameters are standardized under ASTM B117-09 and ISO 9227, defining parameters such as temperature, air pressure of the sprayed solution, preparation of the spraying solution, concentration, pH, etc. However, these standards do not indicate the test duration because the duration varies with the test product and agreements between the customer and manufacturer. Tests can be as long as 720 h, but in the electronic industry, a test duration of 48 or 96 h is common.

Packages attached to boards were exposed in a salt spray environment with 5 % sodium chloride (NaCl) aqua solution (or fog) according to the ASTM B117-09 standard, at 35 °C for 96 h. The sample salt residue was removed by a gentle rinse of deionized water at room temperature and dried in a dry chamber. As shown In Fig. 7.2, even though Sn is protected by a stable passivation layer of SnO and exhibits relatively good resistance to corrosion, it is still possible for localized corrosion to occur. Indeed a minimal amount of corrosion occurred because of the protective oxide layer, but the location of this corrosion can pose a significant risk to the long-term reliability of the joint. Figure 7.2a, b shows scanning electron microscopy (SEM) images of the same solder ball attached to a ball grid array (BGA) package, before and after salt spray pretreatment. After 96 h of treatment, the surface of the joint showed some degree of surface roughness but no serious corrosion pits or

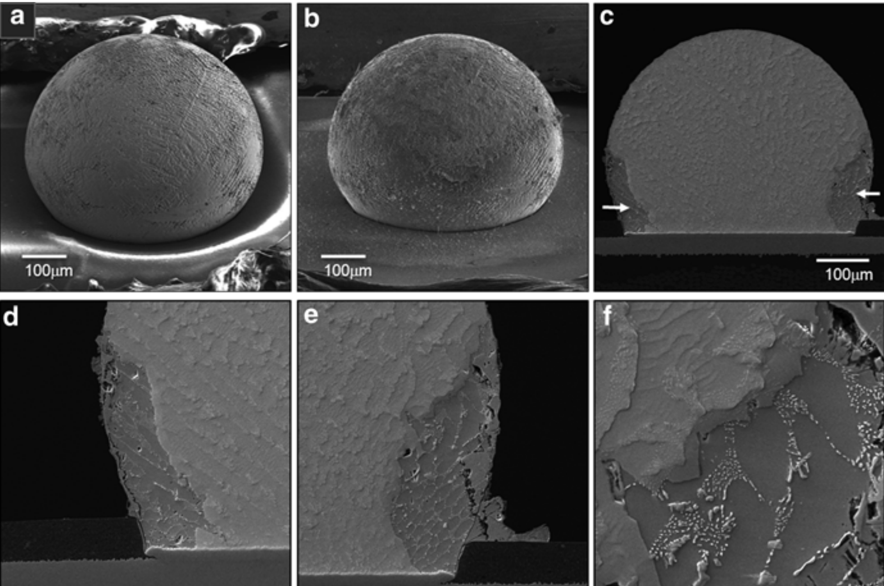


Fig. 7.2 SEM image of a SAC305 Solder ball attached to a ball grid array package (**a**) before 5 % NaCl aqueous salt spray treatment and (**b**) after 96 h salt spray treatment. (**c**) Cross-section SEM image from another SAC305 solder joint treated in 5 % NaCl aqueous solution for 96 h. The *arrows* indicate the corroded area

penetrated areas, as shown in Fig. 7.2b. Compared with the outside surface, the cross section shown in Fig. 7.2c revealed a few localized areas near the corner of the bulk solder joint that showed corrosion damage. A higher magnification SEM image (Fig. 7.2d–f) reveals that the Ag_3Sn remains in the matrix where it was initially located and is not attacked, as they act as noble material islands while the Sn is removed. An SEM-EDX analysis of the corrosion by-product phases at the corner of the solder ball identified a complex oxide chloride hydroxide of tin, $Sn_3O(OH)2Cl_2$ [45, 55]. As the electrochemical potential of Ag is much higher than Sn [39, 55], the existence of Ag, Ag_3Sn, and Cu_6Sn_5 IMCs decorating the Sn grain boundaries may induce the dissolution of Sn into the electrolyte solution. Previous studies have shown that the electrode potential of Ag_3Sn is nearly the same as that of pure Ag, suggesting that the presence of Ag_3Sn in SAC305 solders may accelerate the dissolution of Sn due to galvanic coupling [5]. But, even though the corroded area caused by the galvanic reaction is relatively small and limited to the corner of the solder joint, the thermal cycling performance is more highly affected because of the critical location of such localized corrosion.

Based on this observation, the overall impact of a 5 % NaCl salt spray treatment did not produce a serious or imminent challenge to the reliability of the joint. However, given the fact that the corroded areas were near the interface between the package surface and the bulk solder, such localized corrosion could pose a potential

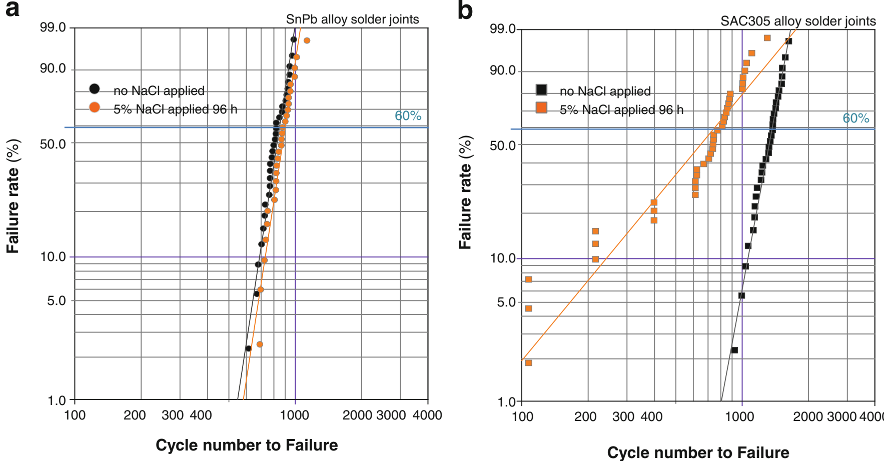


Fig. 7.3 Weibull chart plot for the thermal cycling results on 5 % NaCl aqueous solution (salt spray) treated WLCSP: (**a**) SnPb solder alloy samples and (**b**) SAC305 solder alloy samples

risk to the long-term reliability of the solder joint. Even if the overall solder joint did not experience severe corrosion, the joint can suffer accelerated thermal fatigue crack initiation due to the reduced load-carrying area of the joint and brittle corrosion products in stress concentration locations, which, in this case, is at the corner of the solder joint.

Weibull plots for both Sn–Pb and SAC305 alloy samples before and after pretreatment in a 5 % NaCl aqueous environment for 96 h are compared with non-salt-sprayed component test samples in Fig. 7.3. As shown in the initial microstructure in Fig. 7.4, Sn–Pb has a dual phase microstructure, and the SAC305 has a finely distributed Ag_3Sn IMC network. The characteristic lifetime cycle number for Sn–Pb was relatively unchanged before and after salt spray. But the thermally cycled SAC305 packages that had a 96 h 5 % NaCl salt spray were degraded by over 43 %, which is a significant reduction in the lifetime.

The reason for the degraded lifetime is clearly shown in cross-sectioned joints of Sn–Pb and SAC305 with and without the salt pretreatment in Fig. 7.5. The Sn–Pb joint without a salt spray treatment reveals a crack that has initiated at the corner of the solder joint near the package-side interface region and has propagated through the package-side bulk solder. Compared to Fig. 7.5a and b shows a cross section of a solder joint which had been thermally cycled to failure after salt spray treatment. The cross section shows a few corroded areas, one of which is at the lower left corner of the joint on the surface (indicated with an outlined box). Despite the fact that the corroded area extends approximately 20 μm into the depth of the solder joint, this region did not affect either fatigue crack initiation or propagation. The cross section of the SAC305 joint with and without salt spray treatment and thermal cycling, shown in Fig. 7.5c, d, also shows crack propagation through the bulk solder

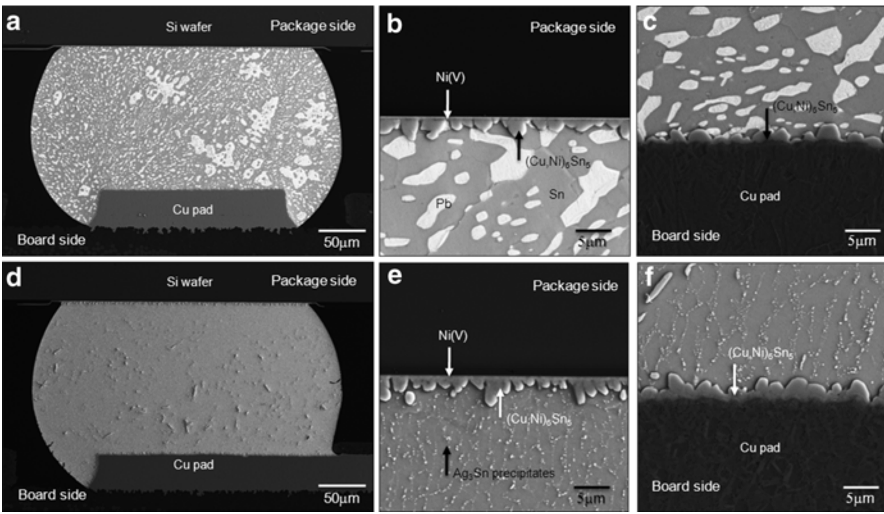


Fig. 7.4 Cross-section SEM image of as assembled WLCSP package. (**a**) SnPb Solder joint, (**b**) package side interface, (**c**) board side interface, (**d**) SAC305 Solder joint, (**e**) package side interface, (**f**) board side interface

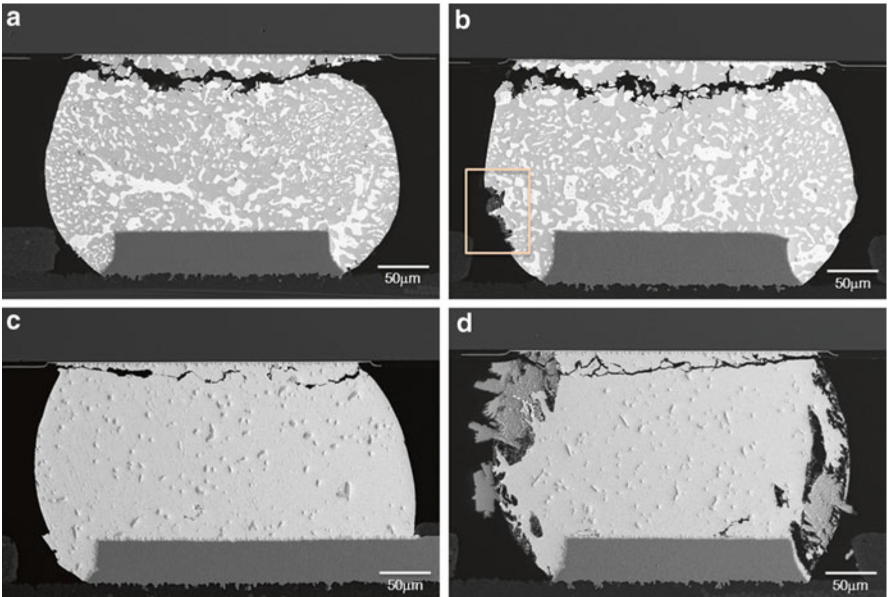


Fig. 7.5 Cross-section SEM microstructure after thermal cycling. (**a**) SnPb solder joint as assembled and thermal cycled. (**b**) SnPb solder joint after salt spray treatment and then thermal cycling. Corrosion area indicated as a box. (**c**) SAC305 solder joint as assembled and thermal cycled (**d**) SAC305 solder joint after salt spray treatment and then thermal cycling

region near the interface, similar to the Sn–Pb solder joint fatigue crack. However, the involvement of the brittle corroded area in the SAC305 joint led to crack initiation at an earlier time. The Weibull plot shows this accelerated crack initiation phenomenon, which drives the Weibull plot to a lower characteristic lifetime cycle number. Furthermore, the multiple corrosion sites on each solder joint pose an additional risk factor related to the structural stability of the joint. These corrosion sites can all be potential crack initiation sites. Unlike Sn–Pb joints, which have a dual phase structure with continuous phase boundaries, the SAC305 joint is nearly pure Sn with isolated Ag_3Sn and Cu_6Sn_5 intermetallic precipitate islands.

The Effect of Grain Orientation on Corrosion Damage Nucleation

In addition to the role of IMCs as galvanic couples in solder joints, the Sn grain orientation also influences the stability of the solder joint in a corrosive environment. As discussed in prior chapters, Sn-based solder alloys have strong anisotropic thermal expansion and plastic deformation characteristics, resulting in mechanical properties that differ significantly from Sn–Pb alloy joints [12–15], where each individual lead-free solder joint has its own unique characteristics arising from the anisotropic Sn properties. This uniqueness also affects chemical properties, as illustrated in Fig. 7.6, which shows cross sections of an edge row of a WLCSP package (joints A1 to joint A10) with SAC305 solder that failed near the characteristic life cycle number. Figure 7.6a shows the sample thermally cycled to failure without any pretreatment. The fatigue cracks mostly initiated and propagated along the package-side interface inside the bulk solder. Full cracks are observed in many joints, particularly those on the left side. Partially cracked solder joints are also observed in

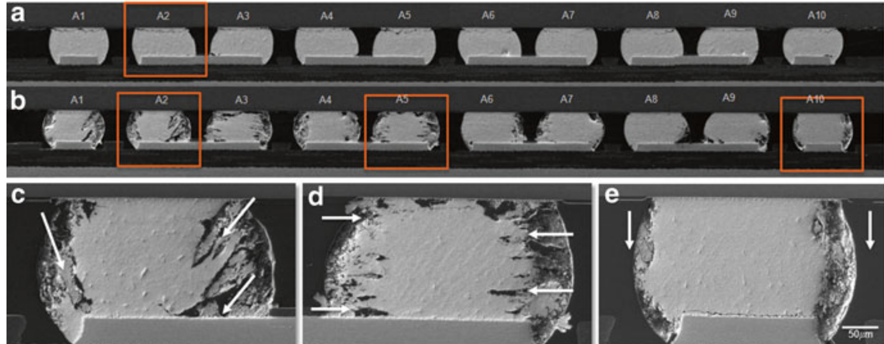


Fig. 7.6 Cross-section SEM image of WLCSP package. (**a**) SAC305 Solder joint as-assembled and thermal cycled and (**b**) as-assembled and 5%NaCl preconditioned and then thermal cycled, with enlargements of boxed joints A2, A5, and A10. The *white arrows* indicate a sense of directionality in the corrosive attack

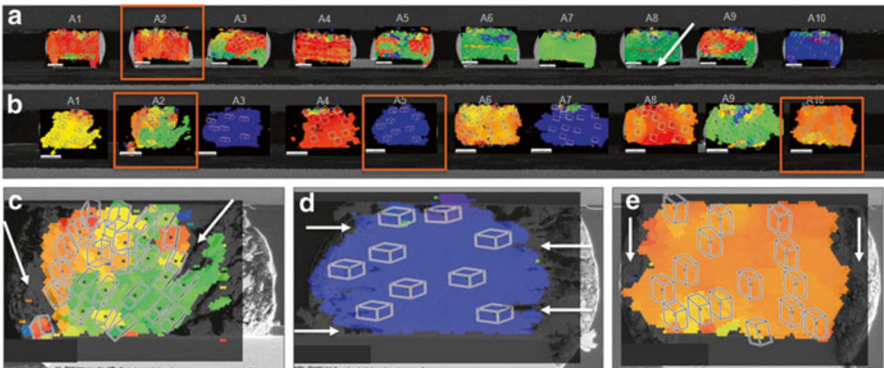


Fig. 7.7 OIM images overlapped to the cross-section SEM images in Fig. 7.5 (**a**) SAC305 Solder joint as-assembled and thermal cycled (**b**) 150 °C/500 h aged and thermal cycled (**c**) as-assembled and 5%NaCl preconditioned and then thermal cycled (**d**) 150 °C/500 h aged and 5%NaCl preconditioned and then thermal cycled

the middle of the package and the rightmost joint. In contrast, Fig. 7.6b shows the cross section from a sample initially treated in 5 % NaCl salt spray for 96 h and then thermally cycled to failure, showing numerous corrosion regions. For example, joints A1 and A2 in Fig. 7.6b show a ~45° angle corrosion trace penetrating from the upper region of the solder joint inward to the bulk solder, whereas joints A3 and A5 show horizontal penetration. These localized corrosion areas at the corners of the solder joints facilitated crack nucleation and reduced the characteristic lifetime shown in the Weibull plot in Fig. 7.3b.

As shown in Fig. 7.6c–e, the corrosion path direction in each joint differs, and this can be correlated with the Sn grain orientation in Fig. 7.7, which shows the Sn c-axis maps corresponding to the SEM images in Fig. 7.6. Each color represents a different c-axis orientation with respect to the substrate and package as discussed in the earlier chapters. "Red-oriented" joints have the c-axis nearly parallel to the substrate plane. In "blue-oriented" joints the c-axis is highly inclined to the package plane. The correlation between the Sn grain orientation and corrosion path can be readily seen by comparing corresponding images in Figs. 7.6c, d, e and 7.7c, d, e. Joint A2 shows corroded regions at the package-side interface corners, and, as indicated by white arrows, the corrosion paths have a distinguishable direction, which points downwards with an angle that differs on the two sides. In the orientation map, the corrosion path aligns with the Sn lattice basal plane and penetrates along the Sn basal planes into the bulk solder joint; the angle of the basal plane differs on the two sides of the joint, due to different crystal orientations. While this joint is severely corroded, it did not crack. In contrast, joint A5 has a Sn grain c-axis perpendicular to the package side and shows a single blue-oriented grain orientation, in which the basal plane is aligned parallel to the package interface. The corrosion path shown in Fig. 7.6d also matches the basal plane direction, and a continuous crack is visible near the top of the joint. In joint A10, in contrast to the blue-oriented solder joint,

the c-axis direction is parallel to the package interface, and thus the basal plane is perpendicular to the interface. This crystal orientation allowed corrosion to occur from the edges of the joint inward, particularly at the corners of the solder joint, either from the package-side corners or from the board-side interface corners. Due to this orientation, the corrosion attack occurred fairly uniformly along the edges of the solder ball but without deep penetration into the joint. The penetration probably still facilitated crack nucleation at the lower Cu solder interface, because the corner of the Cu pad was exposed.

The observations shown here illustrate the opportunity to identify a mechanism that could not be identified without knowing the Sn grain orientation. First, there is a correlation between the Sn lattice basal plane and the preferential corrosion path. Second, this reveals the potential risk of blue-oriented solder joints to corrosion attack. Blue-oriented joints, in which the basal planes are aligned nearly parallel to the package-side interface, have corrosion attack points that correlate with typical crack initiation directions, so it is likely that lower thermal cycling performance arose due to the especial vulnerability of "blue" joints to corrosive attack, when they are least vulnerable to thermal cycling degradation due to recrystallization described in Chap. 5.

Corrosion in Wearable Electronics

While the discussion above focused on the marine environment, NaCl is present also in human sweat. With more electronic devices in our daily life with function and capability closer to human skin, the importance of chemical performance on consumer electronics is also crucial. Unlike a salt spray test, the concentration of NaCl is lower in human sweat compared to salt water or fog, so the salt spray test is not the best method, so artificial sweat is used. The study on metal corrosion caused by human sweat has a long history [39] with interesting subjects such as the study on sweat-induced corrosion on metal guitar strings [56, 57]. To test the corrosion behavior with sweat, artificial sweat solutions are available. In addition to NaCl, artificial sweat also contains $NaH_2(PO_4)$, NaOH, lactic acid, and acetic acid. Normally higher NaCl content in human sweat causes more corrosion. Sweat is an aqueous solution containing 0.5–1.0 % solids consisting of 30–300 mg/100 mL of chloride ions and 45–452 mg/100 mL lactic acid [58]. The lactate concentration in sweat is between 27 and 3,600 mg/100 mL at rest and 90 and 135 mg/100 mL during high sweat rates, while the typical pH of sweat varies between 4 and 6 [7, 58]. Many studies agree that the major corrosion agent in sweat is chloride ions [4–7] although controversy exists around the effect of acids on corrosion behavior. One study showed that lactic acid produced a small increase in corrosion and that a small reduction of pH produced a small increase in corrosivity [5]. Another study showed that acidic sweat corrodes more than alkaline sweat,

although the effect of acidity is much less important than the chloride content [6]. Overall based on recent publications, chloride ions greatly increase the corrosivity; along with more lactic acid and a slight reduction in pH, a general increase of the corrosivity is expected [3].

Prevention and Mitigation: Conformal Coating

One of the methods to prevent the degradation caused by chemical and environmental effects is conformal coating. Conformal coatings are protective coating materials that adhere to printed circuits or other electronic substrates that cover the component assembled on the board. These coatings are applied in thin layers (typically 25–200 μm thick) by literally "conforming" to its irregular profile as shown in Fig. 7.8. The coating provides electrical insulation and environmental protection to significantly extend the life of components and interconnects. The direct role of these conformal coatings is to protect boards from moisture and contaminants, preventing short circuits and corrosion of conductors and solder joints; minimize dendrite growth (ion migration) and electromigration of metal between conductors; relieve stress; prevent tin whiskers [59, 60]; and protect insulation resistance of the circuit board, and in some cases, mechanically support for better mechanical performance.

Because conformal coatings have a variety of roles, each industry sector has different reasons for using these materials and method. For example, the main focus in the aerospace industry is to mitigate Sn whiskers and prevent humidity penetration due to the dewing effect. The military is examining various end-use conditions (cryogenic, marine environment, etc.) that involve solvents, chemical- and oil-based corrosion mitigation, prevention of dust and fine sand deposition, and also mechanical vibration and shock-induced failure mitigation. On the other hand, the telecommunication sector is expecting the conformal coating to provide a long-term reliability from corrosion-induced failures such as in marine environments.

However, it is important to know that all conformal coatings breathe. Coatings permit air, which may contain moisture, and if there is a soluble contamination on

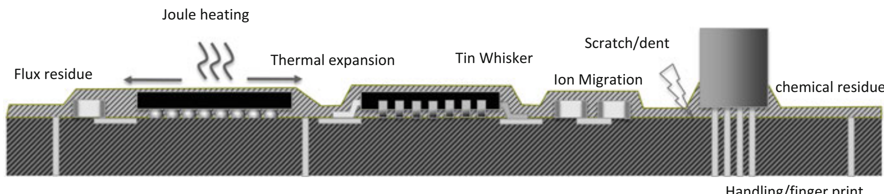


Fig. 7.8 Schematic drawing of conformal coated PCB

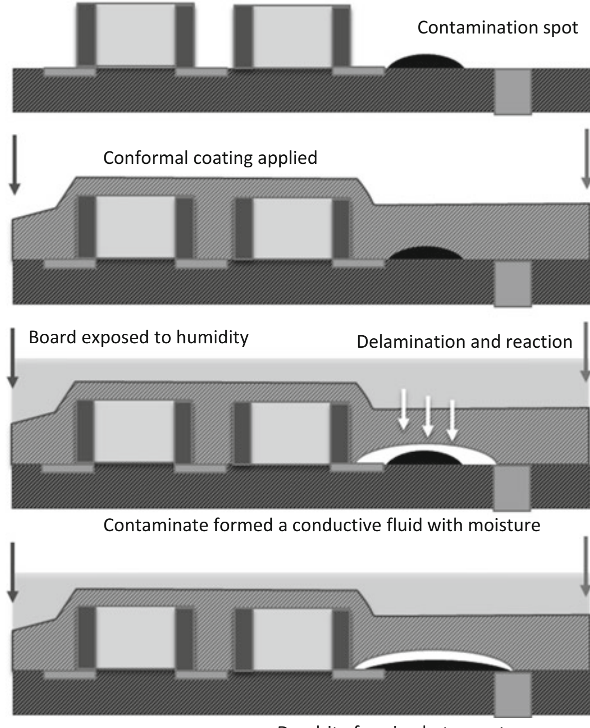


Fig. 7.9 Osmosis mechanism induced defect development including ion migration

the surface beneath the coating, then this may cause osmosis, schematically shown in Fig. 7.9. A contaminant solubilizing and recrystallizing can occur between the coating film and substrate, as moist air moves in and out. The contaminant is usually a salt (e.g., NaCl) and can induce different osmotic pressures, which may be extreme. If it is extreme, it may well cause ion migration/electromigration and circuit failure. This failure occurs only if the conditions are all ideal: Moisture penetration is needed, a contamination reaction is needed, delamination needs to be occurring in place, and ion migration pathways need to be developed. Thus, it needs a closer look to assure that the coating is preventing the degradation, not accelerating it. Covering all the exposed components and exposed traces or metal pads poses new potential risk factors. Manufacturing process, thermal control, thermomechanical stress, ion migration due to trapped humidity, and osmosis are additional factors which need a closer look to assure that the conformal coating provides improved reliability for the device or equipment. Various types of material sets exist in the industry. A brief summary is shown in Table 7.3. Each material set is developed for a specific purpose, and detailed information can be found in various sources.

Table 7.3 Conformal coating materials types and properties

Factors	Acrylic (AR)	Epoxy (ER)	Polyurethane (UR)	Silicones (SR)	Poly-Para-Xylene (XY)
General advantage and disadvantages	Typically solvent based and are easily repaired	Coatings are *hard*, usually opaque and are good at *resisting the effects of moisture*	Coatings are *tough, hard* and exhibit *excellent resistance to solvents*	Coatings range from elastoplastic (tough, abrasion-resistant) to soft	Coatings are very uniform and yield excellent pin coverage
	High Fluorescence level	*Can cause stress* on components during thermal extremes	Good dielectric properties	*Stable over wide temperature range*	*Sensitivity to contaminants and the need for vacuum application technique*
	Ease of viscosity adjustment	CTE closer to epoxy PCB substrate	Less reversion potential	Flexible, provides dampening and impact protection	Chemical inertness/barrier properties, insoluble in organic solvents, acids, or bases, with very low permeability rates
	Represents 80 % of market	Higher T g	Abrasion resistance	Good UV/sunlight resistance	Low environmental impact process
	Single component materials	Good dielectric resistance	*Easy to apply*	High dielectric strength	Excellent dielectric resistance
	Easy to apply	*Excellent chemical* resistance	*Longer cure times (unless using UV cure)*	Low surface energy to enable *effective penetration* under components	Excellent chemical resistance
	Cure quickly	*Excellent temperature* resistance	Difficult to repair	Excellent *high temperature performance*	Excellent temperature resistance
		Poor flexibility	*Combination of Acrylic and Urethane is popular*	Limited solvent resistance	*High cost of process*
		Poor repair		Harder to apply	*Critical processing*
		Fluctuating temperatures can cause considerable drift in viscosities and difficulties in controlling cure times and coating thicknesses		Can be difficult to cure	
				Nearly impossible to repair	
				Expensive	

(continued)

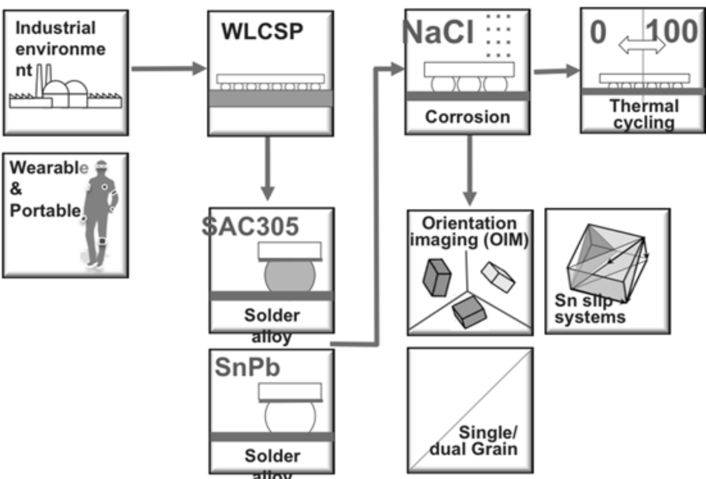
Table 7.3 (continued)

Factors	Acrylic (AR)	Epoxy (ER)	Polyurethane (UR)	Silicones (SR)	Poly-Para-Xylene (XY)
Moisture resistance	very good	Good	Very good	Good	Best
Thickness	25–75 μm	25–75 μm	25–75 μm	50–200 μm	12.7–17.8 μm
Methods of application	Dipping	Dipping	Robotic coating	Brushing	Chemical vacuum deposition (CVD)
	Robotic coating	Robotic coating	Spraying	Dipping	
	Spraying	Spraying	Brushing	Spraying (limited)	
	Brushing	Brushing	Dipping		

Summary and Further Challenges

The effect of chemical environment on SAC solder long-term reliability was explored in this chapter. Unlike Sn–Pb eutectic solder, the Sn-based SAC alloy shows an accelerated degradation mechanism in thermal cycling performance after exposure to NaCl, which can potentially be seen in marine environments. The reaction between NaCl and Sn is due to the galvanic coupling between Sn and IMC precipitates. The corrosion path is favored along the basal plane of the Sn orientation, which can cause pre-crack nucleation sites near the highly stressed interface region. These pre-cracks are observed as crack initiation sites from which thermal cycling cracks can propagate, resulting in a degraded reliability. These corrosion penetration conditions can be mitigated by total conformal coverage of the board. Conformal coatings are one of the technologies that are designed for this purpose. However, covering all the exposed components poses new potential risk factors, which need to be considered together and assessed to protect the whole system. Manufacturing process issues, thermal issues, thermomechanical stress build, ion migration due to trapped humidity, and osmosis are some of the topics which need additional assessment to predict the expected reliability (Fig. 7.9).

In Chapter Seven, we briefly look into the chemical stability of Sn based solder interconnects, which differs from Sn-Pb eutectic microstructures. Instead of the Sn-Pb two ductile phase eutectic microstructure, the Sn microstructure with a small fraction of equiaxed IMC precipitates alters the nature of the galvanic couple, which allows the Sn based solder to corrode.



The solder joint stability in a salt spray environment is examined, and damage is analyzed to identify the corrosion path and effect of grain orientation. The corrosion from NaCl attacks the basal plane in the Sn phase, thus developing a pre-crack at critical localized regions, which result in an accelerated degradation in thermal cycling performance. A mitigation method is also introduced at the end of the chapter, using a conformal coating.

Fig. 7.10 Chapter seven overall summary

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Chapter 8
Challenges in Future-Generation Interconnects: Microstructure Again

The aim of this chapter is not to introduce the packaging technology of the future nor the challenges in specific packaging structure. Rather, it is to review the characteristics of technology on the horizon along with the introduction of materials under consideration, briefly consider possible problems associated with such technology, and stress the need for understanding more on the solder itself. For this, this chapter firstly discusses the need for considering new boundary condition of the interconnects that arise from the use of electronics in harsher environment in a small form factor. It is followed by the discussion on the packaging challenges in higher power devices such as the power handling devices and LEDs. Then, material challenges associated with device miniaturization as well as the increased current density in solder interconnects are presented. Finally, the need for and difficulty in developing multiscale model for solder joint property and its behaviors in packaging structure is briefly discussed in order to reemphasize the urgency of achieving more advanced understanding of the Pb-free solder materials in general.

Future Packaging and Next-Generation Interconnects: Keywords

The keywords for future packaging and next-generation interconnects are smaller form factor, higher performance, flexible in form factor and applications, and lower power consumption than the devices used in today's technology. Demand for such devices emerges as electronic devices are increasingly used in unconventional places, and this trend will only increase in the foreseeable future. Such devices will be designed with miniaturization, wider applications, extreme environments, wearable electronics, low power, flexible, more functionality, vertical stacking and 3D architectures, active thermal management, and high current density as design goals and constraints. Critical issues in relation to the development of such devices include the power device package design, MEMS, 3D wafer-level packages, complex

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T.-K. Lee et al., *Fundamentals of Lead-Free Solder Interconnect Technology*,
DOI 10.1007/978-1-4614-9266-5_8

3D-TSV-based system in package (SIP), and photonics to the package. All of these packages are subjected to a much more punishing loading environment and thus become more prone to failures than the examples discussed in this book. In short, the systems in electronic devices are getting smaller with more complexity, to enable more end-use conditions with a higher reliability expectation. This trend poses many new challenges. Individual mechanistic phenomena are combined to become a complex coupled mechanism. Higher current in a smaller system brings electro-current plus Joule heating plus diffusion plus isothermal aging into one mechanism, which needs material models that consider all of these phenomena concurrently. There will be a need for better understanding of microstructure evolution and its relation to failure mechanisms.

Challenges in Future-Generation Interconnects: Introduction

As is evidenced in previous chapters, the primary objective of this book is to highlight the importance of understanding the linkage between the microstructure and the reliability of solder joint. However, it is important to realize that our understanding is still limited to cope with tough challenges ahead of the packaging technology. Presently, it is not easy to foresee what type of packaging structures, materials, and processes will be used in the future technology. Undoubtedly, some of the packages used in today's technology or under intense development will continue to be used in a number of devices perhaps with needed modifications. However, it is certain that many of the future devices will employ radically different device packaging technology where solder-based interconnects are likely to be subjected to different process conditions, service environments, and load conditions. With demand for device miniaturization, they can no longer enjoy material redundancy. With increasing demand for multifunction and high-performance devices, they may be situated in places where thermal, electrical, and mechanical constraints are excessively punishing. In some cases, some devices may be packaged into a flexible substrate to enable the wearable electronics, which demands solder interconnects with exceptional resilience against vibration and fatigue. Electronic industry is currently experimenting with several devices of such kinds, and some of them are already introduced to packaging community with reception varying from excitements to skepticism. Those devices include the ones with employing 3D wafer-level packaging, multi-die stacking, and 3D-TSV (through-Si via)-based system in package. While many more will be added to this list in the near future, one thing clear is the fact that the solder interconnects will be subjected to unprecedentedly pushing environment as they are required to endure higher temperature, mechanical stress and its variations, and current density. What this means is that it is necessary to extract more strength from the solder joint than we have achieved and that much deeper knowledge on the mechanisms governing various properties and behaviors of solder joint is necessary.

The ultimate goal for an engineer or a scientist is to develop physically based models that can describe the performance of interconnects in the context of the device operation. To achieve that, one needs to understand how physical mechanisms are related to the microstructure of interconnects and adjacent systems. With a comprehensive model, various design parameters can be changed computationally to accurately estimate the performance of interconnections within the system and hopefully avoid or at least minimize surprises arising from unintended consequences.

The New User Condition for Future Electronics: Wider Temperature Range and Smaller Device

As history has demonstrated numerous times, demand shapes the future of electronic devices. The main driving force for electronic device development is the desire to enable electronics consuming low power, multitasking, be robust, and be cheap to own. The equally strong desire to use electronics in places is conventionally considered to be impossible. An example of such kind is wearable electronics, which is emerging as a new technology frontier. Another example may be the autonomous systems like the remote telecommunication stations, the satellite, and the cloud (more recently fog) computing that are required to be with the unprecedented level of reliability. All these demands make the electronic devices to face a new end-user condition, which is unfortunately harsher than the presently accepted end-use condition.

Facing a new end-use condition is not new in the history of electronic industry. The most well-known example is the situation created by the transition to Pb-free electronics as is extensively discussed throughout this book. This type of transition creates all types of problems and often brings old problems to surface again as a new threat. An example can be found from the case of Sn whisker and tin pest. The ban of using Pb from electronics forced electronic industry to adapt high-Sn solder alloys that are known to be easy to form whisker and suffer from tin pest. Short-circuit failure by Sn whisker growth in low quality environment is well known in electronics industry, the first serious incident dating back to the Second World War period. The communication equipment used by all nations suffered from high failure rates due to short circuit failure of capacitors. Analysis of the failed capacitors revealed that it was created by the growth of Sn whisker. A more recent episode is the Galaxy IV satellite failure, the source of which was traced to the short circuit in CPU caused by Sn whisker that grew out of the Sn-plated PCB. Since the Pb-free solder alloys contain Sn in excess of 90 %, the whisker growth is very likely, which poses a serious reliability threat. This threat created by whisker growth will become more critical in devices with high-density interconnects because the smaller spacing between the interconnects increases the short circuit probability even with minor growth of Sn whisker. The precise mechanism behind the whisker growth is still under intense debate, but it is commonly understood to be the growth of single-crystal Sn under the influence of hydrostatic pressure. For this reason, it is important

to prevent the formation of Sn oxide, or any type of passivation layer, on solder surface that creates such a stress state. The prevention of such oxide formation is problematic when the solder is exposed to high temperature and high humidity. Thus improvements in packaging structure and employment of molding compounds deserve careful consideration as they can reduce the level of hydrostatic pressure and prevent formation of Sn oxide.

Another possible problematic property of Sn is the Tin pest. Tin pest is not related to degradation of the Sn phase by corrosion or cracking but rather from the formation of α (gray) tin. There exists two stable phases of Sn, α-Sn and β-Sn, and their stability are determined by the ambient temperature. In case of pure Sn, the critical temperature that separates the stability of these phases is 13.2 °C. At temperature above the critical, β-Sn is the preferred phase, α-Sn becomes stable at temperature below the critical. The β-Sn is a metallic phase with tetragonal structure and shows reasonable ductility. On the other hand, α-Sn is a semimetallic phase with a much lower density diamond cubic structure and is mechanically brittle. The first report of tin pest causing engineering disaster is known as the case of "Napoleon's button," as buttons were made from tin. The French troops led by Napoleon took more casualties from frostbite than fighting during the Russian campaign of 1812, in part blamed on failure to secure uniforms due to fracture of the buttons, and hence this phenomenon was named tin pest. Later analysis showed that the transformation from white to gray tin can be suppressed by a small amount of impurities in Sn. Whether the tin pest suffered by Napoleon's troop can be attributed to the gray Sn formation or not, this story illustrated the risk of using high-Sn solder in extremely cold weather. Figure 8.1 shows a series of Sn-0.5%Cu samples exposed to −20 °C. The transformation from the white to gray Sn is visible, evidencing a risk of solder joint failure when electronics are used at low-temperature environment [1].

As exemplified in the case of tin pest, unforeseen properties of materials in extreme or harsh environment are the source of future challenges ahead of the future electronics.

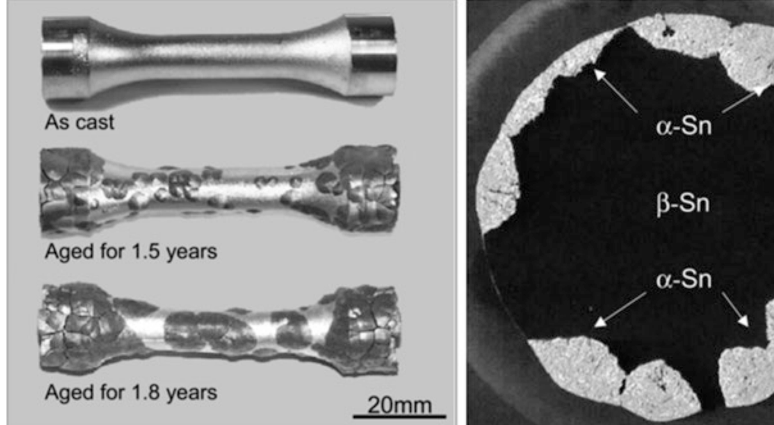

Fig. 8.1 Extreme low temperature effect on Sn-based solder alloy composition. Sample tested at −20 °C resulted in beta to alpha Sn transformation [1]

New degradation mechanisms will become critical, and new methods to mitigate such mechanisms will shape the development planning. With continuously expanding application areas, electronic devices will satisfy increasingly challenging requirements in terms of not only reliability but also performance and production cost. Some of these challenges are explained in the early part of Chap. 1. Increasing demands for devices with higher reliability intended for automobile and other transportation vehicles, high-temperature and high-pressure environment in energy-harvesting sector, and more wearable mobile devices with high-density packaging are some of the areas where consideration on harsh environment is critical. With the development of molecular and nanoscale electronics, new technological approaches for electronic packaging will become necessary in the near future. Also important is development of new materials like self-healing materials. Devices equipped with such materials or package designs will be useful in equipment that cannot be easily accessed after its installation.

While it may appear that the Pb-free initiative is at its final stage and all commercial electronics have Pb-free solder interconnects, there is still a segment of the electronic components, which have to use Pb-containing solder materials. High melting temperature applications require the high-Pb alloys, for example, Pb-10Sn, Pb-2Sn-2.5Ag, or Pb-5Sn alloys. These alloys are mostly used for the die attachment, for silicon die to substrate attachment, and in power-related components. The power modules or power ASIC components can reach a junction temperature over 175 °C. The Pb-containing alloys have shown excellent reliability and stability in this condition while permitting effective heat drainage from Si die to substrate. Thus a solder alloy with melting temperature higher than 260 °C is needed to replace the Pb-containing solder alloys, given the need for the multiple reflow events. There are several candidate materials and technologies but their feasibility hasn't been fully demonstrated yet.

Among several technologies for high-temperature interconnects under development are but not limited to Ag powder sintering, alternative alloys, high thermal conductivity adhesives, and transient liquid phase sintering (TLPS) that could replace high-Pb alloys. Ag powder sintering is a pressureless die attachment process using micro- or, in some cases, nanometer scale Ag particles. The nanoscale particle size enables the sintering to be possible at around 200 °C due to its high surface energy/volume [2,3]. Some of the benefits of this method include the completion of the process at low temperature without damaging Si die or interconnects and formation of interface that has better thermal conductivity than conventional Ag epoxy die attach materials. For alternative alloys, Zn- or Bi-based alloys are under investigation, but their mechanical stability and thermal fatigue resistance need more improvement to be practical. High thermal conductive adhesive is a kind of composite material with Ag particles and filler material. This material is designed to provide electrical and thermal conductivity using the Ag particles and structural stability through filler material. The TLPS is a mixture of solder and Cu particles, where the liquid Sn phase assists sintering of Cu. All these materials have their own merits, but they also have limitations in terms of successfully replacing the high-Pb solder. The key to success will be formation of interfaces with high thermal conductivity, while the interconnecting material has to tolerate extreme mechanical and chemical stability. High-temperature Pb-free solder alloys need development and further research attention is expected.

High-Power LED Packaging

After the discovery of blue LEDs and their conversion to white light by phosphor technologies [4], the LED for general lighting finally becomes viable. This led to significant changes in LED packaging development from the earlier low-power packaging for indicators to high-power packaging for general lighting. Years of research have greatly improved the efficiency of the LED chip, but in current technology, LED conversion is only about 20 %, so more than 80 % of the energy is converted into heat causing a temperature rise at the LED PN junction. A LED junction temperature rise of 10 °C reduces the LED life by 50 % [5]. Furthermore, at high temperatures, the LED light color temperature can shift due to the forward voltage change [6]. When the chip temperature rises, the temperature of the package along the device increases, and the device packaging materials, such as phosphor, silicone lens, and substrate, degrade faster, thereby reducing the efficiency and life of the light source. Due to the high power in the LED package, the selection of thermal interface material (TIM) is critical for heat dissipation to obtain a stable light output and color and to maintain normal device lifetime [7]. For example, a nanoscale Ag thermal interface material can be sintered at low temperature, can provide higher thermal conductivity similar to Ag itself [8], and can have potentials to improve the heat dissipation, performance, and life of LED packages. There are other novel ideas in studies of high-performance die attach thermal interface materials, like carbon nanotubes as thermal interface materials in semiconductor packages which also show significant improvement in thermal conductivity for both single- and double-wall nanotubes [9,10].

Further Miniaturization

Higher functionality and miniaturization not only drive the Si die stack-up and high-density package but also increase the number of IOs needed to connect the components to the board. For a given area under the component, the trend is moving to a finer pitch component. A finer pitch component with a larger die is a challenge, as discussed in Chap. 5. It is expected to be down to 0.15 mm pitch for fine-pitch FBGA in the coming years. With this reduced pitch size and reduced solder volume, all the issues and mechanisms addressed in Chaps. 5 and 6 will be accelerated. The larger CTE mismatch not only influences the thermal cycling performance but also causes the current density to be higher, which leads to various electromigration mechanisms. With fine-pitch geometries, power "crowding" and performance limitations will need to be understood. A current density of the order of 10^4 A/cm^2 is a limiting parameter for power handling. Innovative solutions are needed to overcome detrimental current crowding effects, Joule heating, and current stress-induced diffusion in high-current electronic devices.

Heat generation by electronic devices and Joule heating from high current density must be dissipated to avoid isothermal aging, to improve reliability, and to prevent premature failure. The component package now has to provide significant thermal management capability, and future demands are unlikely to be met unless some novel processes or structures can be developed. The packaging community has been providing thermally enhanced devices for many years, but as device geometries shrink, the internal junctions dissipate more heat, while increased functionality requires more power, which in turn generates a higher thermal load. The ITRS roadmap is also projecting an increase in operating ambient temperature from 45 to 55 °C and harsh environments going up to 200 °C in the next 10 years.

In terms of enhanced functionality, device structures such as multi-chip modules, SiP (system in package), and PoP (package on package) hold the most promise at this time. All of these technologies have a common objective in that they allow performance-enhancing opportunity while limiting cost. By thinning, stacking, and connecting chips, 3-D provides a way to greatly increase functionality, a goal common to many packaging technologies such as system in package (SiP) (Fig. 8.2). SiP products have already penetrated deeply into current electronics such as the components used in tablet PCs and smartphones. The future direction of SiP is not determined yet but is likely to go to either a larger body size or a more compact and smaller body size with employment of wafer-level packaging (WLP) and direct chip attach (DCA) to the system board. Due to the possibility of cost reduction and performance enhancement, the use of WLCSP will increase especially in devices for the consumer market. However, since WLCSPs are subjected to a higher CTE mismatch, they would suffer from reliability failure by thermal cycling. Several mitigation methods for thermal cycling failure of WLCSP, such as the use of the underfill, are under active development, but the question as to the long-term reliability remains unanswered. Also, the desire to increase the body size clearly exists in ASICs where a denser and a large die size offer gain in performance, but it should

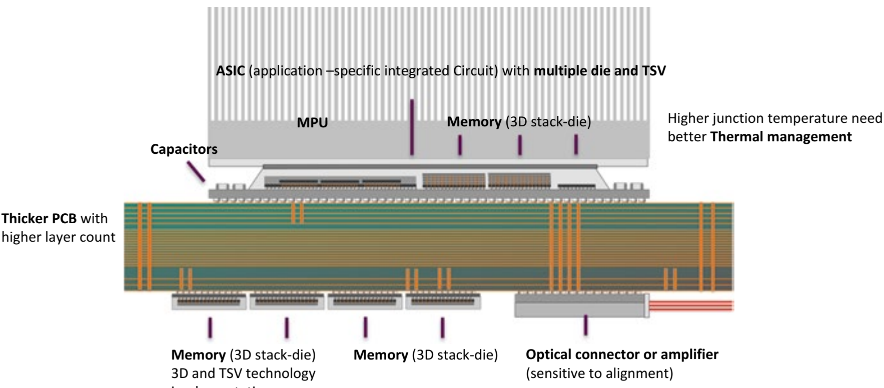

Fig. 8.2 Miniaturization and increase functionality in a given volume will drive the importance of the current and thermal and mechanical reliability interaction

be done with careful consideration on the long-term reliability as it would suffer more from CTE-induced reliability problems. TSV or through-silicon via technology has been a hot topic in the last few years in the packaging development industry, as it is considered the core technology of future 3D packaging due to the possibility of crossing the barrier of integrating chips into one package [11,12]. This is a further miniaturization of system in package (SiP) technologies. The purpose of TSV is to integrate chips by vertical "vias" in silicon chips in order to establish an electrical and mechanical connection from the active side to the backside of the die and connection to the active side of the next die. However, the challenges of TSV remain, in terms of thermal management and electrical and mechanical integrity. The thermal management is the key challenge; although TSV technology provides a high density of interconnection to enable more powerful output of the devices, the thermal sink is limited to the vias between the dies, which limits the redistribution of heat. Optimization of vias, redistribution strategies, and further die thinning are all keys for better thermal management. Future TSV technology will be focused on improving the overall reliability by developing more coherent packages in terms of material selection, die processing, and via material and via processing. Further thinning of the die to 15 μm will greatly help TSV development in terms of minimizing the key risks. Also other TSV technologies, such as via in glass, have been studied for low-cost interposer solutions in 3D IC using TSV technologies [12].

Further Challenges Related to the Effect of High-Density Current

The effect of high-density current on solder joint reliability has become one of the most important and challenging issues in recent years with the growing demand for high-performance but compact devices. The size reduction imposes high current densities exceeding 10^4 A/cm^2. Multiple reliability issues emerge from such a high level of current density. The most obvious is the increase in the joint temperature due to the Joule heating. Although it is increasingly difficult to manage, heat can be dissipated by the use of cooling devices attached to the package. A more serious reliability threat is failure induced by electromigration (EM).

EM refers to atomic diffusion under high-density electric current and has a long history of investigation because it is one of the leading sources of thin film interconnect failure in Si-integrated circuits. Thin film Al or Cu interconnects used in integrated circuits often carry currents exceeding 10^6/cm^2, making them prone to EM failure in the form of either voids or hillocks at places where flux divergence exists. Therefore, assessment of EM reliability is a part of the requirement for qualification of new device structures or processes. The current density in the solder joint is much lower than along thin film interconnects. However, since the ambient temperature of solder at device operating conditions is at a high homologous temperature, EM can occur with an appreciable rate even under lower current density and make solder interconnects fail by EM. Figure 8.3 shows voids formed by EM in a

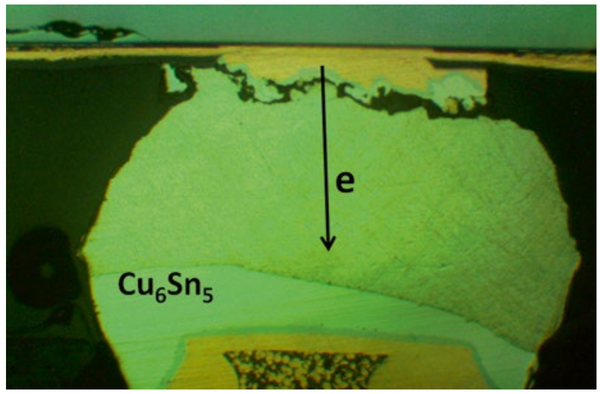

Fig. 8.3 A cross-sectional optical micrograph of SAC solder ball taken after electromigration (EM) testing. Both chip side and PCB side of metallization layers were Cu. EM voiding is visible at upstream end of mass flow, while thick Cu_6Sn_5 IMC is visible and downstream end of mass flow

SAC305 solder ball, illustrating one of the typical EM failures that can form at solder interconnects. As illustrated in this micrograph, EM induces void formation at the upstream end of the electron/Sn flow, while concurrent EM of Cu results in the excessive growth of IMC at the downstream side of electron flow.

There are many possible ways that high-density current can impart either a positive or negative influence on joint reliability, but they are not yet known. EM is the mechanism that is likely to be most influential on solder reliability, so it is valuable to introduce the method of EM reliability assessment and the failure mechanism here. The underlying assumption is that it would negatively influence the mechanical stability of the solder joint.

Because EM failure takes an excessively long time in normal-use conditions, evaluation of EM reliability is conducted by extrapolation of the failure rate gained from accelerated testing. Using established practice in thin film interconnects, the extrapolation is generally conducted using so-called Black's equation, an empirical relationship that equates the time to failure to the current density (*n*) and temperature *T*:

$$ttf = Aj^{-n} \exp\left(\frac{E}{kT}\right) \tag{8.1}$$

The constant *A* represents the geometry and chemistry of the joint, while the other terms have their usual meaning. In the case of thin film interconnects, *E* is usually linked to the diffusion activation energy of the migrating species, and *n* is taken to be 2 following the mass of accumulated experimental data as well as a few theoretical models that specify *n*. For solder interconnects, experimental values reported so far do not show such consistency. The variation is too great to make any meaningful conclusions on *E* and *n* yet. The measured activation energy for EM failure in SAC solder varies from 0.5 to 1.5 eV, while n is reported to range from 1 to 7. It is highly unlikely that *E* and *n* would vary to such a degree due to variations in the EM mechanisms that lead to failure. Rather, it is more likely a reflection of the difficulty in conducting EM testing and EM failure analysis with desired

consistency, perhaps resulting from variations related to current flow geometry and its interactions with anisotropic crystalline properties of Sn and Cu_6Sn_5.

The understanding achieved so far suggests that the EM failure mechanisms in solder interconnects are fundamentally different from that in thin films in many aspects. The most striking may be related to the voiding kinetics. In the case of thin film interconnects, the size of an embryonic void is comparable to that of interconnect. This implies that EM failure is limited primarily by void nucleation. On the other hand, the dimension of solder interconnects is far greater than the embryonic void, so the EM failure rate is limited by void growth. Since the void growth rate should be inversely proportional to the atomic flux, which is proportional to the current density and diffusivity of atoms in solder, the current exponent is expected to be 1 and the activation energy to be that of solder diffusivity in an ideal situation. However, complexity arises from the fact that the interconnect temperature is not constant in the region of void growth. In the case of thin film interconnects, an increase in temperature by Joule heating (by EM-induced voiding) can be ignored because the Si substrate provides an effective heat sink. This is not the case in case of solder interconnects, so it not only makes EM testing more difficult but also implies that EM failure is a more dynamic process because the temperature changes with voiding.

Another EM characteristic unique to solder interconnects is related to the extreme anisotropy in EM kinetics with Sn grain orientation. Recent reports suggest that the diffusivity of Cu in Sn as well as Sn itself varies dramatically with direction in the Sn unit cell (grain orientation). Specifically, the c/a ratio of Sn self-diffusion is reported to be 0.38, meaning that the Sn diffusion rate, and thus the EM rate, is much slower when electron flows along the c-axis of Sn grain. A much greater anisotropy is reported in the opposite sense for Cu and Ni diffusion. The Cu diffusivity along the c-axis is reported to be 100–500 times faster than along the *a*-axis. Ni diffusivity is even faster, 70,000 times higher than a-axis diffusivity. This extreme level of anisotropy in diffusivity poses considerable challenges in correctly assessing EM reliability because the solder joint has an intrinsic EM resistance variation due to varying anisotropies for different elements of the diffusing species.

It is also critical to consider the possibility of coupling between the void growth and mechanical stress in joint developed by EM or Joule heating. It is inevitable that variation in temperature, mechanical load, and current will exist even in a solder joint, and they may not produce a mutually independent influence on void formation and growth. For example, current raises the temperature via Joule heating; both temperature and current induce microstructural changes, particularly in the nature and distribution of precipitates and interfacial intermetallics, which influences the electrical resistivity and the creep rate under load; the current induces the electromigration of vacancies that may significantly affect the diffusional processes that govern creep. None of these coupling relationships is well understood.

EM is conventionally understood as a mechanism that induces failure in a solder joint by forming a void at the upstream end of the joint. It is also probable, though not well explored, that EM can result in a short circuit by promoting a growth of Sn whisker at the downstream end of the EM flow. An accumulation of Sn atoms at a local site,

as a result of EM, produces compressive stress that can only be released either by hillock formation (creep) or by a growth of Sn whisker. Since future solder interconnects are not only small in size but also closely spaced, interconnect failure by a short circuit would be a more serious reliability problem than an open-circuit failure by voiding. These open and short circuits by EM failure processes will be in competition, and therefore the failure type and its kinetics will be highly dependent on the size of the solder interconnect and the space between them. Regardless of the failure type, the reliability threat stemming from EM will only intensify with further progress in packaging technology due to miniaturization driving forces. There is no doubt that EM failure will be a major reliability concern in future device packaging technology.

Additionally, EM in solder interconnects presents two difficult challenges to the reliability community. The first is related to the difficulty in conducting EM test itself. Without an effective heat sink, the solder interconnects are very prone to Joule heat-induced temperature increase. Since EM testing needs to be done at an accelerated conditions, the testing demands the use of excessively high current. This makes the temperature for EM testing difficult to control and monitor. Furthermore, slight local temperature difference can trigger thermomigration because the temperature gradient is large due to the small dimension, making EM testing prone to errors originating from thermomigration. These make the EM condition of samples vary significantly, resulting in great difficulty in correctly analyzing a failure distribution. Secondly, our knowledge of the EM failure mechanism in solder joint is so limited that contributing factors to EM failure are not fully identified. This reduces confidence on the reliability assessment, but more importantly it makes EM failure to be difficult to control or prevent.

Another source of difficulties in conducting and analyzing EM reliability is related to the fact that EM occurs concurrently with IMC phase growth at interface. In one respect, the growth of the IMC phase becomes a source of error in evaluating the EM failure rate. EM failure is monitored through measurement of electrical resistance of solder interconnects. Because IMC growth results in a resistance increase, it can obscure the true EM failure rate. If a failure criterion is chosen to be a small increase in resistance, the measured failure rate would be contaminated by the growth rate of IMC phase which is initially fast and slows down over time. In an opposite consideration of choosing a large increase in resistance as the failure criterion, the failure time is less affected by the IMC growth but is subjected to error stemming from temperature change. Another aspect of IMC growth, which may be more important in terms of understanding EM mechanism, is the fact that EM failure is greatly affected by the atomic species entering into the solder from the substrate. The two interfaces of solder interconnects react with solder. They can add migration species to the solder. For example, in case when the current polarity is chosen to induce electron flow from Cu substrate to the other side of interface, EM induces dissolution of Cu into SAC solder. Then, two migration species, Cu and Sn, compete under EM driving force. Recent observations suggest that Cu migrates faster than Sn such that EM voiding is retarded until sizable amount of Cu substrate is removed by EM. The EM void shown in Fig. 8.3 is believed to have formed by this process. In this case, there is a possibility that the activation energy for EM

failure is not a reflection of the activation energy for Sn self-diffusion but Cu diffusion in Sn matrix. Diffusion of Cu as well as Ni in Sn matrix is believed to occur by an interstitial mechanism. Thus, the activation energy for EM failure can be significantly smaller in the case when voiding kinetics are controlled by the Cu or Ni rather than self EM of Sn.

While EM itself plays a critical role as a major reliability failure mechanism, it can also seriously limit the joint reliability when combined with other failure mechanisms. For example, an EM-induced void at the solder interconnect, even if it is small, can serve as a nucleus for crack growth. Also, the growth of thick IMC layers at the downstream end of the EM flux would make the joint to be more susceptible to failure by mechanical impact loading. This means that EM weakens the mechanical stability of the solder interconnects, and this effect cannot be predicted in the normal reliability evaluations. It is therefore highly probable that actual resistance of the solder interconnects against failure by shock, fatigue, and vibration is considerably worse than what is predicted from reliability evaluation of each mechanism if EM-induced mechanical weakening effect from EM is not included.

Finally, because EM can assist other failure mechanisms, this makes reliability assessment error prone and reliability mechanisms become highly convoluted. There is a possibility that the EM and mechanical failure mechanisms interact in a unique way that suppresses one or both failure mechanisms. For example, if compressive stress is present in the solder joint while EM is progressing, the EM failure rate is likely to be reduced because it closes the void. Conversely, an opposite effect can result if fatigue-induced crack accelerates EM failure. Although the need for considering the coupled effect is apparent, it is not so clear how to include such effects into consideration. It is realistic to expect that the already complex and not well-understood EM mechanism in solder interconnect affects other failure mechanisms such as fatigue and fracture, making any of the failure mechanisms so complex that it is difficult to sort out without extensive resources. Complexity of the failure mechanism in parallel with the ever increasing EM risk will be one of the most challenging issues that reliability engineers will face and have to overcome in future technology.

Estimating Microstructure Evolution with Modeling

From the above discussion about interrelated effects, it is obvious that development of models capable of concurrent operation of multiple mechanisms will be required for identification of worst case scenarios that can be used to guide design decisions. Modeling of the properties of Sn is still in its infancy, due to its dramatic anisotropy. Because of the nature of complex interrelated effects from the atomic to the joint length scales and long time scales, integration of many models covering different length and time scales will be required. Efforts to link together more focused modes of specific phenomena will enable the complex interrelated effects discussed above to be explored computationally.

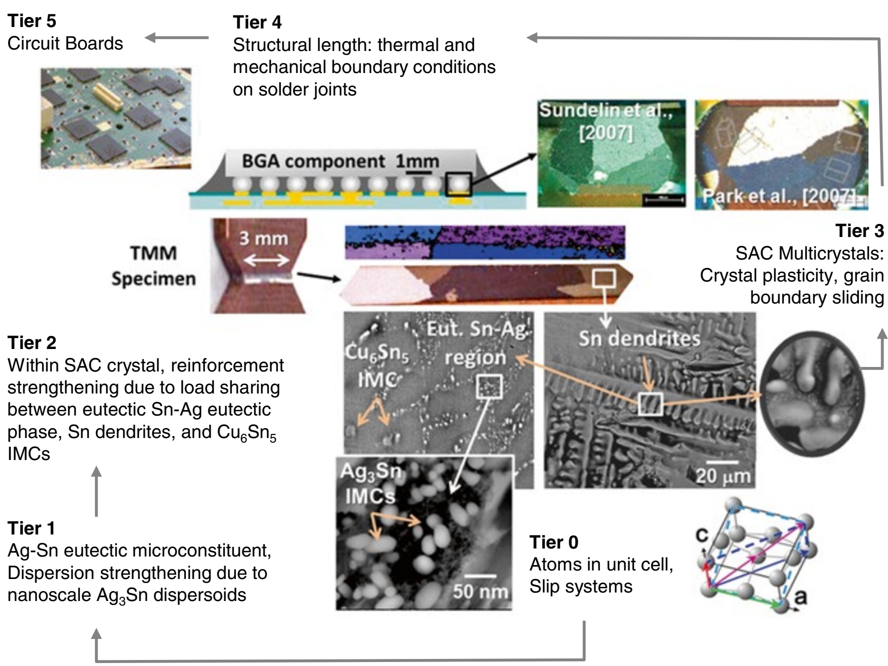

Fig. 8.4 Multiple length scales (Tiers 0–5) in Sn–Ag–Cu solder alloys

Figure 8.4 identifies six length scales across which salient information must be passed between linked models, so that macroscale properties needed for practical design exercises can be found. The length scales involved with complex microstructure evolution start with the highest length scale relevant to interconnects, the electronic subsystem of the circuit board (Tier 5), where heat generation, internal and external stresses, and vibration cause bending on a large scale. System designers need an efficient continuum material model that captures the history-dependent variation in solder properties to use when designing systems at the board scale. The solder joint is the means through which mechanical equilibrium between the package component and the board is maintained. Hence, at the Tier 4 level, complex evolving boundary conditions are imposed on the actual physical geometry of the solder joint (including the interfacial metallization that creates the intermetallic bond between the solder and the component [13–17]). The next lower length scale (Tier 3) is the grain scale microstructure, typically consisting of an anisotropic single crystal or a few Sn grains and grain boundaries and sometimes a truly polycrystalline microstructure arising from microstructural evolution processes including continuous recrystallization (cRx, based upon dislocation recovery) and primary recrystallization (Rx, involving nucleation and growth of new orientations). At this scale, crystal plasticity finite element models for a particular microstructure are effective.

The next lower length scale (Tier 2) focuses on the structure within individual grains, comprised of multiple tin dendrites arising from solidification that are surrounded by a eutectic Sn–Ag microconstituent that was the last to solidify. Additional micron scale intermetallic precipitates such as Cu_6Sn_5 and Ag_3Sn are embedded throughout the grain. At this scale, composite models are effective. Tier 1 describes the structure of the eutectic Sn–Ag microconstituent consisting of a locally homogeneous distribution of nanoscale Ag_3Sn intermetallic particles embedded in a monocrystalline tin matrix. Here, 3-D anisotropic models of dislocation interactions with particles that depend on spacing/size are appropriate. In Tier 0, dislocation slip systems needed for modeling in Tier 3, and other atomistic scale effects arising from atomic diffusion of Sn and alloy elements, and dislocation structure/core relaxation interactions need to be modeled. Clearly, passing information from each of these levels of scale efficiently to models at the next higher or lower level is an enabling component of integrated computational materials engineering, and this provides the fundamental motivation for linking models together.

Many models for specific phenomena exist that consider some of these interrelated effects, such as growth of particles and their influence on evolving creep properties [18], and nascent progress in crystal plasticity slip system property identification (described briefly in Chap. 5), but they have not yet been linked together into comprehensive model systems. One particular approach to link models is illustrated in Fig. 8.5, which illustrates three primary modules needed to model the evolving solder joint properties. The primary units are an analytical dislocation flow model that captures phenomena in Tiers 1 and 2, which can be passed as evolving phenomenological flow models into crystal plasticity finite element (CPFE) models of a single solder joint in Tiers 3 and 4. From the CPFE simulation, an evolving yield surface can be extracted for use at the continuum scale for package and board design (Tier 5). The linked model needs to begin with the influence of microlevel inhomogeneity in the initial as-solidified microstructure and stress state, to develop a nonuniform distribution of IMC particles that affect partial and full relaxation of stored plastic energy by recovery and possibly recrystallization, leading to localized constraints due to the presence of voids or large IMC particles and EM-induced stresses and the influence of evolving elemental concentration gradients.

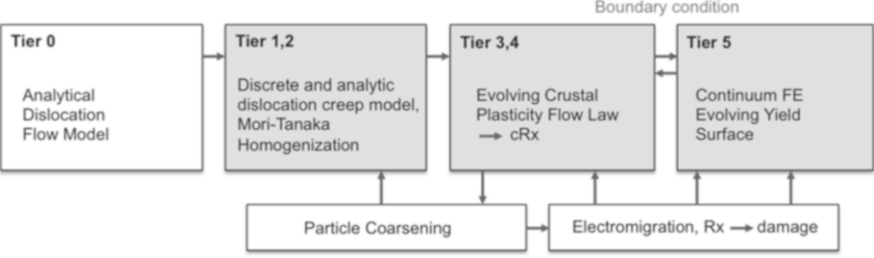

Fig. 8.5 Information transfer strategy for multi-scale modeling of solder joints

One component of a rudimentary multiscale modeling framework [19] uses simple dislocation mechanics and homogenization principles to capture the physics of creep deformation at Tier 1 and 2 length scales. This dislocation-based approach provides a good starting point for modeling the initial nonequilibrium conditions arising from solidification; however, it needs introduction of the anisotropic properties of Sn. This model starts with Tier 0 steady state creep properties of pure Sn as an input parameter. In Tier 1, the model accounts for dislocation interaction with nanoscale Ag_3Sn intermetallic particles in the eutectic regions between Sn dendrites within a SAC grain, where the rate-limiting process for dislocation motion is a dislocation detachment mechanism [20]. Assuming an initial saturated dislocation density, equilibrium between three competing processes must evolve: (1) dislocation generation; (2) dislocation impediment caused by the back stress from pinning of dislocations at IMCs and forest dislocations; and (3) dislocation recovery due to detachment from IMCs. This balance identifies the net increment in hardening or softening of the material. The Tier 2 load sharing between the eutectic Ag_3Sn dispersion regions and hexagonal Cu_6Sn_5 IMC rods and ellipsoidal Sn dendritic lobes can be approximately captured with isotropic self-consistent homogenization schemes based on rudimentary viscoplastic Eshelby eigenstrain methods [18–23]. However, such an approach does not predict transient primary creep transients arising from the nonequilibrium solidification state that also depends on anisotropic properties of Sn. Introduction of anisotropic Eshelby tensors into a Mori-Tanaka homogenization scheme could make such models effective. The output of the Tier 1 model is the effective creep properties and creep strain rates for individual slip systems as well as the overall dispersion strengthened eutectic region on SAC solders. However, such models will also need to incorporate coarsening of the nanoscale Ag_3Sn IMC particles that also affect recrystallization of the coarse-grained Sn microstructure and also grain boundary-sliding kinetics. As EM modeling efforts are less well developed, it is likely that these components and the field-based boundary conditions that drive diffusion mechanisms will need to be introduced into models at this scale.

The outputs of such a model will provide the *handshake* between the dislocation-based Tier 0–2 model and the CPFE-based Tier 3–4 model, which includes the following parameters for each dominant slip system: (1) dislocation density history expressed as hardening parameters; (2) critical resolved shear stress; and (3) effective activation energy of shear strain rate. Crystal plasticity finite element modeling algorithms account for the effect of microstructure and slip mechanisms that influence the plastic deformation in crystalline materials [23–30]. Models such as the one briefly described in Chap. 5 can capture the kinematics of slip in a multigrain joint, as illustrated in Fig. 8.6. However, evolving resistance to dislocation slip must be informed by models in Tiers 2 and 3. The outcomes of EM effects, such as voiding and rapid intermetallic growth, will need to be introduced spatially into the appropriate regions of the CPFE model, and current flow and related heat generation effects will need to be incorporated into evolving CPFE boundary conditions or run in a parallel manner to inform the CPFE boundary conditions.

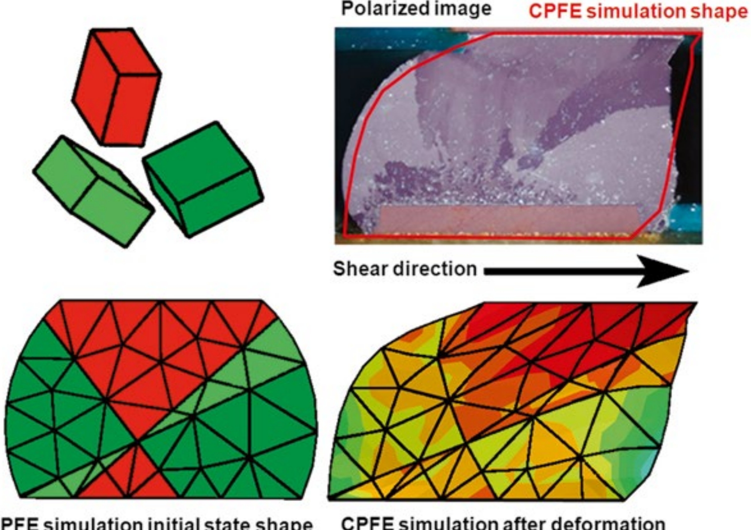

Fig. 8.6 CPFE simulation of a solder joint with beach ball microstructure deformed in shear matched the kinetic shape change fairly closely

$$\phi\left(\sigma,\tau_y^\alpha,T\right)=\frac{1}{2n}\left(\sum_{\alpha-1}^{N}\left|\frac{\sigma:\mathbf{P}^\alpha}{\tau_y^\alpha}\right|^{2n}-\mathrm{int}\left[\frac{1}{kM}\sum_{\alpha=1}^{M}\sum_{\beta=1}^{M}\mathbf{P}^\alpha:\mathbf{P}^\alpha\right].\exp\left(-\frac{Q^\alpha}{KT}\right)\right) \tag{8.2}$$

Unlike CPFE models, phenomenological yield functions used in continuum scale models commonly used by system designers are computationally efficient and can capture the initial anisotropy of the material. However, to capture the evolving deformation induced anisotropy of the material, yield functions must also evolve, using approaches as such as those described in [28].

The modeling strategies are different at each length scale, and hence integration for a fully multiscale implementation requires appropriate strategies for information handoff. At Tiers 1 and 2, modeling strategies involve semi-closed-form models with specific model parameters. At Tier 3, models for crystal plasticity and crystal visco-plasticity and grain boundary sliding require semi-computational techniques [31]. At Tier 4, fully computational methods such as finite element methods are required, to capture actual geometry and boundary conditions of realistic solder joints [32].

All of these modeling efforts will require concurrent and strategic experiments tailored to provide crucial information for the models in order to provide feedback to each other for improvement. Highly characterized experimental data are needed for effective model development to provide feedback and insights for refining model components. The modeling can assist interpretation of experimental observations and must also account for the observations made in experiments, which helps validate the models. This mutual check and balance between two interrelated efforts is critical for the success of the ultimate goal of integrated multiscale modeling.

Summary and Further Challenges

Future designs will increasingly impose conditions on solder joints that are more similar to the aggressive accelerated testing currently used to evaluate long-term performance of joints, packages, and systems. The aggressive accelerated tests bring failures at shorter times than in service conditions. This implies that designs under consideration for envisioned future products will not last very long. Thus, there are strong driving forces to improve the performance of solder joints, which will require extensive research and development to improve alloy performance, as well as to develop complex models capable of identifying and predicting interactions of many different mechanisms operating at different length scales. This will require two major approaches: first, sub-modeling to insure that mechanisms are correctly modeled and, secondly, assembly of sub-models into a larger integrated framework. To be useful to design engineers, evolving continuum yield functions that vary according to evolving macroscale boundary conditions will need to inform lower length scale models to determine how properties evolve in critical and strategically identified locations, so that reasonable interpolation of property evolution can be introduced at the highest length and time scales. Such integrated efforts will enable effective identification of worst case scenarios that can inform designers so that major unanticipated or unexpected consequences of new approaches can be minimized as the demands on improved performance of interconnects continue to increase (Fig. 8.7).

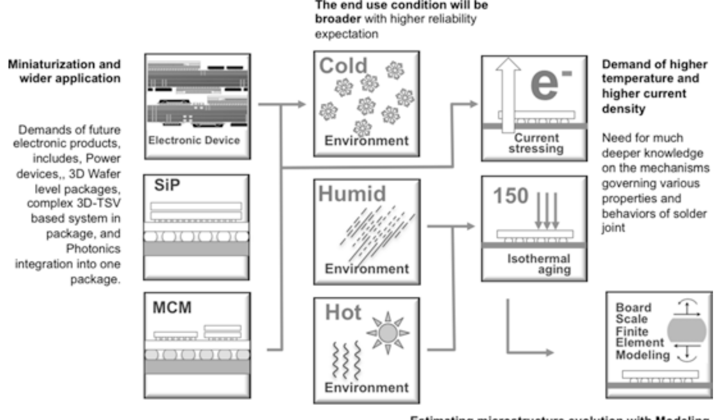

Fig. 8.7 Chapter 8 overall summary

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