

Chapter 2

If It's Pinched It's a Memristor

Leon Chua

This chapter consists of two parts. Part I gives a circuit-theoretic foundation for the first four elementary nonlinear 2-terminal circuit elements, namely, the resistor, the capacitor, the inductor, and the memristor. Part II consists of a collection of colorful “Vignettes” with carefully articulated text and colorful illustrations of the rudiments of the memristor and its characteristic fingerprints and signatures. It is intended as a self-contained pedagogical primer for beginners who have not heard of memristors before.

L. Chua (✉)

Department of Electrical Engineering and Computer Sciences, University of California,
Berkeley, CA 94720, USA

e-mail: chua@eecs.berkeley.edu

Part I

2.1 Abstract

This tutorial clarifies the axiomatic definition of $(v^{(\alpha)}, i^{(\beta)})$ circuit elements via a look-up-table dubbed an *A-pad*, of admissible (v, i) signals measured via Gedanken Probing Circuits. The $(v^{(\alpha)}, i^{(\beta)})$ elements are ordered via a complexity metric. Under this metric, the *memristor* emerges naturally as the *fourth element* [1], characterized by a state-dependent Ohm's law. A logical generalization to memristive devices reveals a common *fingerprint* consisting of a dense continuum of *pinched hysteresis loops* whose area decreases with the frequency ω and tends to a straight line as $\omega \rightarrow \infty$, for all bipolar periodic signals and for all initial conditions. This common fingerprint suggests that the term *memristor* be used henceforth as a moniker for memristive devices.

2.1.1 Axiomatic Definition of Circuits Elements

How do you *characterize* a 2-terminal “black box” B such that its response to any electrical signal can be predicted? Since you are not allowed to peek inside B your only recourse is to carry out measurements by probing B with *all possible* electrical circuits, containing arbitrary interconnections of circuit elements, such as resistors, capacitors, inductors, diodes, transistors, op amps, batteries, voltage and current sources with arbitrary time functions, etc. We will henceforth call such circuits “*Gedanken Probing Circuits*,” as depicted in the *Gedanken* experimental setup shown in Fig. 2.1. Let us insert an instrument called an ammeter in series with the top wire to record a time function $i(t)$ called the *current* in Amperes entering the top terminal (labeled by a plus (+) sign). Next let us connect an instrument called a *voltmeter* across B to record a time function $v(t)$ called the *voltage* in Volts across the *plus-minus* terminals of B.¹ Let us call $(v(t), i(t))$ an *admissible* (v, i) signal of B. The recorded list

$$B(v, i) \triangleq \{(v_1(t), i_1(t)), (v_2(t), i_2(t)), \dots, (v_n(t), i_n(t)), \dots\} \quad (2.1)$$

of *admissible* (v, i) signals (*AVIS*) from *all possible Gedanken Probing Circuits* constitutes the *complete* characterization of the 2-terminal black box B in the sense that given any voltage signal or current signal, one can search the *AVIS* “memory bank,” henceforth called the *AVIS-pad* of B or just *A-pad*, and identify the unique admissible signals $(\tilde{v}(t), \tilde{i}(t))$ being sought. The *A-pad must* contain this entry in its memory bank because the signal is associated with *some* circuit connected to B, and

¹Observe that the voltage v and the current i are defined axiomatically via two instruments called voltmeter and ammeter, without invoking any physical concepts such as electric field, magnetic field, charge, flux linkages, etc. One does not even have to know how a voltmeter, or an ammeter, works. They are just names assigned to the instruments.

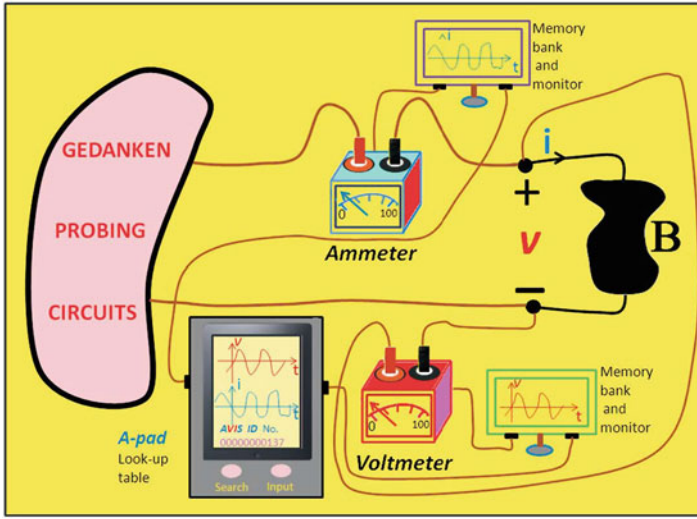


Fig. 2.1 Axiomatic definition of a 2-terminal circuit element

this circuit is a Gedanken probing circuit, by definition. The *A-pad* is just a *look-up-table* containing all admissible (v, i) signals of B . Observe that the *A-pad* is in general an infinitely long pad containing infinitely many pairs of admissible signal waveforms $(v(t), i(t))$ of B , as depicted in Fig. 2.1.

The above Gedanken experiment is only a thought experiment. However, for a large number of real-world 2-terminal devices, the *A-pad* for B can be generated via equations.

Example 2.1 (Ohm's Law). A very small subset of all 2-terminal black boxes are characterized by an *A-pad* that satisfies Ohm's Law; namely,

$$v = Ri \quad \text{or} \quad i = Gv \tag{2.2}$$

where R is called the *resistance* in Ohms (Ω) of B and G is called the *conductance* in Siemens (S) of B . In this case

$$AVIS = \{(Ri_1(t), i_1(t)), (Ri_2(t), i_2(t)) \dots (Ri_n(t), i_n(t)), \dots\} \tag{2.3}$$

can be reconstructed by (2.2). When Ohm's law is written with i as the independent variable, namely; $v = Ri$, it is called *current controlled*. If it is written in the form $i = Gv$, it is called *voltage controlled*. Often it is more convenient to recast (2.2) in the *implicit form*

$$f_R(v, i) = v - Ri = 0 \tag{2.4}$$

Since (2.4) is neither a function of v , nor of i , it is called a *relation* in mathematics. In *nonlinear circuit theory*, it is called a *constitutive relation* [2–4]. Observe that the constitutive relation is just a compact formula, or algorithm, for generating the *A-pad* of B .

Example 2.2. Suppose the *A-pad* of the 2-terminal black box B in Fig. 2.1 can be written in the form

$$\mathbf{AVIS} = \left\{ \left(v_1, v_1 + \frac{1}{3}v_1^3 \right), \left(v_2, v_2 + \frac{1}{3}v_2^3 \right), \dots, \left(v_n, v_n + \frac{1}{3}v_n^3 \right) \dots \right\} \quad (2.5)$$

for all possible voltage signals

$$v(t) = v_1(t), v(t) = v_2(t), \dots, v(t) = v_n(t) \dots$$

then the *A-pad* of B can be generated by the much more compact constitutive relation

$$f_R(v, i) = v + \frac{1}{3}v^3 - i = 0 \quad (2.6)$$

Since both (2.4) of Example 2.1 and (2.6) of Example 2.2 involve the same pair of circuit variables (voltage, current), and since all 2-terminal devices that can be characterized by a constitutive relation

$$f_R(v, i) = 0 \quad (2.7)$$

between the variable pair (v, i) can be proved to be dissipative (or passive) if $v \times i > 0$ for all (v, i) listed in the *A-pad*, this class of 2-terminal elements are called *resistors* [2–4].

Example 2.3. Most 2-terminal black boxes can *not* be described by a constitutive relation between the variable pair (v, i) . However, another important subclass can be expressed by a relationship between the variable pair (v, q) , where

$$q(t) = \int_{-\infty}^t i(\tau) d\tau = q_0 + \int_{t_0}^t i(\tau) d\tau \quad (2.8)$$

and

$$q_0 \triangleq \int_{-\infty}^{t_0} i(\tau) d\tau \quad (2.9)$$

is called the initial state² of $q(t)$ at the initial time $t = t_0$. This subclass of 2-terminal black boxes can be characterized by a collection of admissible signals between the variable pair (v, q) , namely,

$$B(v, q) = \{(v_1(t), q_1(t)), (v_2(t), q_2(t)), \dots, (v_n(t), q_n(t)), \dots\} \quad (2.10)$$

where

$$q = Cv \quad (2.11)$$

and C is a constant called the *Capacitance* of B . Equation (2.11) is the constitutive relation of B because we can generate the corresponding *AVIS* $(v(t), i(t))$ via (2.8); namely

$$i(t) = \frac{dq(t)}{dt} \quad (2.12)$$

Indeed, any relationship

$$q = f_C(v) \quad (2.13)$$

is a valid constitutive relation and this class of 2-terminal devices are called *capacitors*.

By the same reasoning, the constitutive relation

$$\varphi = f_L(i) \quad (2.14)$$

involving the variable pair (i, φ) defines a third subclass of 2-terminal devices called *inductors*, where

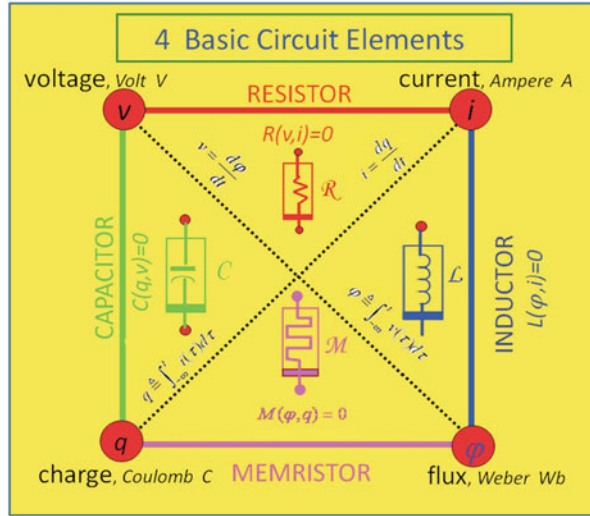
$$\varphi(t) = \int_{-\infty}^t v(\tau) d\tau = \varphi_0 + \int_{t_0}^t v(\tau) d\tau \quad (2.15)$$

Observe that the above three classes of basic circuit elements, called resistors, capacitors, and inductors, are defined *axiomatically*, via a constitutive relation between a pair of variables chosen from $\{v, i, q, \varphi\}$. There are six different pairs that can be formed from these four variables; namely

$$\{(v, \varphi), (i, q), (v, i), (v, q), (i, \varphi), (\varphi, q)\} \quad (2.16)$$

²In practice one can never know the precise signal $i(t)$ over the infinite past. Rather we can only set up our measurements to begin at some initial time $t = t_0$. Consequently, the initial condition q_0 in Eq. (2.8) represents a summary of the past memory of $q(t)$ measured at $t = t_0$.

Fig. 2.2 Four axiomatically defined circuit elements



The first two pairs (v, φ) and (i, q) are already related via (2.15) and (2.8), respectively, and are *not* constitutive relations because they cannot predict the corresponding current $i(t)$ and voltage $v(t)$. However, the last pair (φ, q) defines yet another constitutive relation since given any *admissible* signals $(\varphi(t), q(t))$, one can recover the corresponding $(v(t), i(t))$ via (2.15) and (2.8). For logical consistency, and symmetry considerations, it is necessary to define a *4th circuit element* [1] via the constitutive relation

$$f_M(\varphi, q) = 0 \tag{2.17}$$

between the variables φ and q . This element was postulated and named the *memristor* (acronym for *memory resistor* in [5]). A physical approximation of such an element has been fabricated in 2008 as a TiO_2 nano device by Dr. Stanley Williams group at hp [6]. The above axiomatic definition of the four basic circuit elements is summarized in Fig. 2.2, along with their respective symbols [7]. Note that the standard symbols for resistor, capacitor, and inductor are enclosed by a thin rectangle with a dark band at the bottom because it is essential to distinguish the reference polarity of each nonlinear element if its constitutive relation is *not* odd-symmetric.

We wish to stress that although the symbols of q and φ in Fig. 2.2 are given the names *charge* and *flux*, respectively, *they need not* be associated with a real physical *charge* as in the case of a classical *capacitor* built by sandwiching a pair of parallel metal plates between an insulator, or a real physical *flux* as in the case of a classical *inductor* built by winding a copper wire around an iron core.

2.1.2 $(v^{(\alpha)} - i^{(\beta)})$ Circuit Elements

Let us introduce the notations [4]

$$v^{(\alpha)}(t) \triangleq \begin{cases} \frac{d^\alpha v(t)}{dt^\alpha}, & \text{if } \alpha = 1, 2, \dots, \infty \\ v(t), & \text{if } \alpha = 0 \\ \int_{-\infty}^t v(\tau) d\tau, & \text{if } \alpha = -1 \\ \int_{-\infty}^t \int_{-\infty}^{\tau_1} \dots \int_{-\infty}^{\tau_{|\alpha|}} v(\tau_1) d\tau_1 d\tau_2 \dots d\tau_{|\alpha|}, & \text{if } \alpha = -2, -3, \dots, \infty \end{cases} \quad (2.18)$$

and

$$i^{(\beta)}(t) \triangleq \begin{cases} \frac{d^\beta i(t)}{dt^\beta}, & \text{if } \beta = 1, 2, \dots, \infty \\ i(t), & \text{if } \beta = 0 \\ \int_{-\infty}^t i(\tau) d\tau, & \text{if } \beta = -1 \\ \int_{-\infty}^t \int_{-\infty}^{\tau_1} \dots \int_{-\infty}^{\tau_{|\beta|}} i(\tau_1) d\tau_1 d\tau_2 \dots d\tau_{|\beta|}, & \text{if } \beta = -2, -3, \dots, \infty \end{cases} \quad (2.19)$$

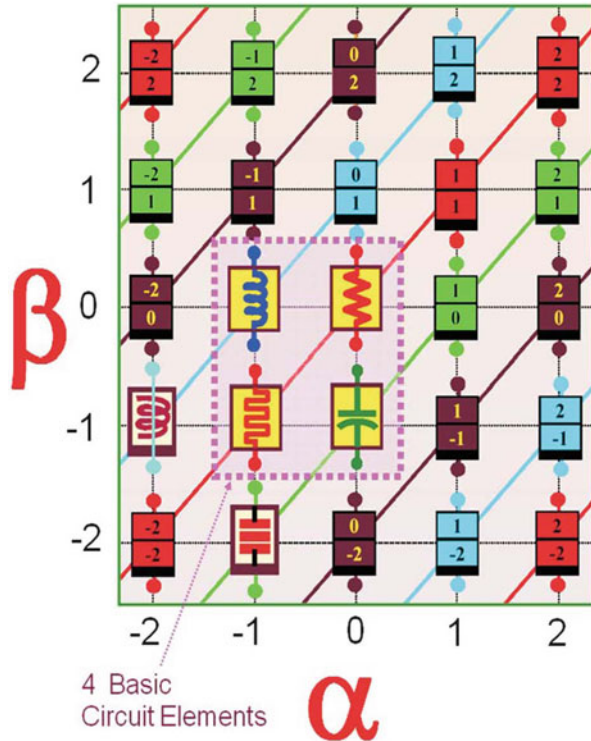
where $|\alpha|$ and $|\beta|$ are integers. Let us identify a $(v^{(0)}, i^{(0)})$ element as a *resistor*, a $(v^{(0)}, i^{(-1)})$ element as a *capacitor*, a $(v^{(-1)}, i^{(0)})$ element as an *inductor*, and a $(v^{(-1)}, i^{(-1)})$ element as a *memristor*. Using this notation, we can define an infinite family of circuit elements, each one identified by its element code $(v^{(\alpha)} - i^{(\beta)})$ and referred to simply as an (α, β) element.

The first 25 (α, β) elements are listed in Fig. 2.3, each coded by an integer pair (α, β) , and identified by a rectangular box where “ α ” and “ β ” are printed on the “top,” and at the “bottom,” respectively. Each (α, β) element is located at the intersection between a vertical line through α , and a horizontal line through β . The four circuit element symbols shown in Fig. 2.2 are printed in their corresponding locations in Fig. 2.3. The two elements $(\alpha, \beta) = (-1, -2)$ and $(\alpha, \beta) = (-2, -1)$ are called *memcapacitor* and *meminductor*, respectively [8], and are identified by their corresponding symbols.

The above infinite family of circuit elements are defined *not* for the sake of generality. Rather, they are *essential* for developing a rigorous mathematical theory of nonlinear circuits in the sense that if one excludes all elements with $|\alpha| > k$ and $|\beta| > k$, for any finite integer k , then one can construct hypothetical circuits whose solutions do *not* exist after certain finite times $t \geq T_k$ due to the presence of a “singularity” called an *impasse point* [2, 3, 9]. It is unlikely, however, that (α, β) elements with $|\alpha| > 2$ and $|\beta| > 2$ will be needed in modeling most real-world devices.

It can be proved that any (α, β) element with $|\alpha| + |\beta| > 2$ is *active* in the sense that it can be built only with active components, such as transistors and op amps, which requires a power supply. Finally, we remark that every (α, β) element can be built by the same procedure illustrated in [2, 5, 10] using a family of linear active

Fig. 2.3 The first 25 (α, β) circuit elements, $-2 \leq \alpha \leq 2$, $-2 \leq \beta \leq 2$



2-ports called *mutators*. They can also be *emulated* via various off-the-shelf digital components [11], or by programmable softwares interfaced with analog-to-digital (A/D) and digital-to-analog (D/A) converters.

2.1.3 Complexity Metric of Circuit Elements

For each (α, β) element, let

$$\chi \triangleq |\alpha| + |\beta| \tag{2.20}$$

be its associated *complexity metric* [12]. For example, $\chi(0,0) = 0$ for a *resistor*, $\chi(0,-1) = 1$ for a *capacitor*, $\chi(-1,0) = 1$ for an *inductor*, $\chi(-1,-1) = 2$ for a *memristor*, $\chi(-1,-2) = 3$ for a *memcapacitor*, and $\chi(-2,-1) = 3$ for a *meminductor*. If one associates the vertical and horizontal lines passing through the elements in Fig. 2.3 as streets of Manhattan, New York city, then the complexity metric χ of an (α, β) element gives a measure of its distance from the resistor $(\alpha, \beta) = (0,0)$. The larger the metric $\chi(\alpha, \beta)$, the farther it is from the resistor.

The complexity metric measures not just only the distance of (α, β) element from the resistor but also the *minimum number* of capacitors (or inductors) needed to build an (α, β) element using off-the-shelf components. For example, a minimum of one capacitor along with active elements such as transistors and op amps is needed to build a *memristor* while a minimum of two capacitors are needed to build a meminductor. From a mathematical perspective, the larger the complexity metric, the higher the dimension of the *state space* and the larger the number of nonlinear differential equations and exotic dynamical phenomena that can emerge.

Based on any of the above measures of complexity, the four elements depicted in Fig. 2.3 are indeed the simplest circuit elements, with the memristor ranked as the 4th element in increasing complexity.

2.1.4 Fingerprint of Memristors

The formal mathematical definition of the memristor is given in [5], along with its circuit-theoretic properties. Here we recall that the memristor is defined by a collection of all admissible signals, namely, an *A-pad* listing all signals measured from all admissible “Gedanken Probing Circuits” (Fig. 2.1) and which can be completely reproduced by the constitutive relation (2.17).

For example, a charge-controlled memristor can be defined by

$$\varphi = f_M(q) \quad (2.21)$$

where f_M is a *piecewise-differentiable* function [12]. In this case, we can generate all $(v(t), i(t))$ from the *A-pad* via the following q -dependent Ohm’s law:

$$v = R(q)i \quad (2.22a)$$

$$R(q) \triangleq \frac{df_M(q)}{dq} \quad (2.22b)$$

The function $R(q)$ is called the memristance (acronym for Memory Resistance) where

$$R(q) \geq 0 \quad (2.23)$$

for all passive *memristors* [2].

Now observe from (2.8) that since

$$\frac{dq}{dt} = 0 \quad \text{when} \quad i = 0 \quad (2.24)$$

the memristor can assume a *continuous* range of distinct equilibrium states

$$q = q(t_0), \quad t \geq t_0 \quad (2.25)$$

when the power is switched off at any time $t = t_0$. It follows that the *memristor* can be used as a *nonvolatile analog memory*. In particular, it can be used as a nonvolatile *binary* memory where two sufficiently different values of resistance are chosen to code the binary states “0” and “1,” respectively. Because the hp *memristor* reported in [6] as well as in many other nano devices [13] can be scaled down to atomic dimensions, the *memristor* offers immense potentials for an ultra low-power and ultra dense nonvolatile memory technology that could replace flash memories and DRAMS.

An incisive analysis of (2.22) reveals that the *nonvolatile* memory property possessed by the memristor is a direct consequence of its *state-dependent* Ohm's law. Moreover, all circuit-theoretic properties possessed by the *memristor* are preserved if we generalize (2.22) to the form [14].

$$v = R(x, i)i \quad (2.26a)$$

$$dx/dt = \mathbf{f}(x, i) \quad (2.26b)$$

The generalized *memristor* defined in (2.26) is dubbed a memristive *device* in [14] where $x = (x_1, x_2, \dots, x_n)$ denotes n *states variables*, which do not depend on any external voltages or currents. However, since both (2.22) and (2.26) are endowed with the same circuit-theoretic properties, it is more convenient and logical to refer to both equations as defining a *memristor*. In the rare events where a distinction may be desirable, one can refer to (2.22) as defining an “ideal memristor.”

The most important common property of (2.22) and (2.26) is that the loci (i.e., Lissajous figure) of $(v(t), i(t))$ due to *any* periodic current source, or periodic voltage source, which assumes both positive and negative values, must always be *pinched* at the origin in the sense that $(v, i) = (0, 0)$ must always lie on the (v, i) -loci, called a *pinched hysteresis loop* in the literature [13]. We wish to stress that (2.22) and (2.26) imply that the pinched hysteresis loop phenomenon of the memristor must hold for *any periodic signal*, $v(t)$ or $i(t)$, that assumes both positive and negative values, as well as for any initial condition used to integrate the differential equations to obtain the corresponding steady state $i(t)$ and $v(t)$, respectively.

Another unique property shared by all memristor hysteresis loops is that for every given periodic function $i = f(t)$ (where $f(\bullet)$ assumes both positive and negative values), and for any initial state $\mathbf{x}(0)$ the area enclosed within the part of the pinched hysteresis loop in the first quadrant, and the third quadrant, of the $v - i$ plane shrinks continuously as the frequency ω increases, and the hysteresis loop tends to a *single-valued function* through the origin as ω tends to ∞ .

The above dense continuum of pinched hysteresis loops, as well as their *single-valued function* limiting phenomenon as $\omega \rightarrow \infty$ must hold for *all memristors*. Any purported system which may exhibit a pinched hysteresis loop but which violates the above continuum and frequency-dependent limiting *memristor fingerprint* is *not* a memristor, the reader is referred to [15] for several contrived examples which fails the above “*memristor fingerprint test*.”

We end this tutorial by pointing out that not all memristors are nonvolatile memories. In fact there is an even *larger class* of *locally active* memristors [2, 4, 9] which exhibit many exotic nonlinear dynamical phenomena. A very interesting and scientifically significant example is the classic Hodgkin–Huxley Axon circuit model of the squid giant axon.³ Notwithstanding the immense importance of their circuit model, Hodgkin and Huxley had erroneously named two circuit elements in their model associated with the potassium ion, and the sodium ion, respectively, as *time-varying conductances*. This mistaken identity has led to numerous confusions and paradoxes ever since the publications of their classic axon circuit model [16]. Well-known physiologists were puzzled by experimentally observed *rectification phenomenon* as well as *gigantic inductances* that could not exist within the soft tissues of the brain. The following quotation from Cole (see page 78 of [17]), an eminent physiologist and the recipient of the 1967 USA *National Medal of Science*, is a case in point:

“The suggestion of an inductive reactance anywhere in the system was shocking to the point of being unbelievable”

We have solved the above conundrum, and many other hitherto unresolved paradoxes associated with the Hodgkin–Huxley Axon, by showing the Hodgkin–Huxley *time-varying* potassium conductance is in fact a 1st-order memristor, and the Hodgkin–Huxley *time-varying* sodium conductance is in fact a 2nd-order memristor, as defined in Fig. 2.4b, c, respectively [18]. Also depicted in Fig. 2.4 are the pinched hysteresis loops associated with each memristor. Observe that they are all pinched at the origin, and that the lobe area in the first and third quadrants shrinks continuously to a straight line as ω increases, both being the fingerprint of memristors.

We conclude this tutorial by stressing that memristors are not inventions. They are *discoveries* and are ubiquitous. Indeed, many devices, including the “*electric arc*” dating back to 1801, have now been identified as memristors [19, 20]. Aside from serving as nonvolatile memories [21], *locally passive* memristors, have been used for switching electromagnetic devices [22], for field programmable logic arrays [23–27], for synaptic memories [28–30], for learning [31–33], etc.

In addition, *locally active* memristors have been found to exhibit many exotic dynamical phenomena, such as *oscillations* [34], *chaos* [35, 36], *Hamiltonian vortices* [37] and *autowaves* [38], etc.

³Hodgkin and Huxley were awarded the 1965 Nobel Prize in physiology for their derivation of the circuit shown in Fig. 2.4a, where the two memristors were drawn as time-varying resistors in Fig. 1 (page 501) of [16].

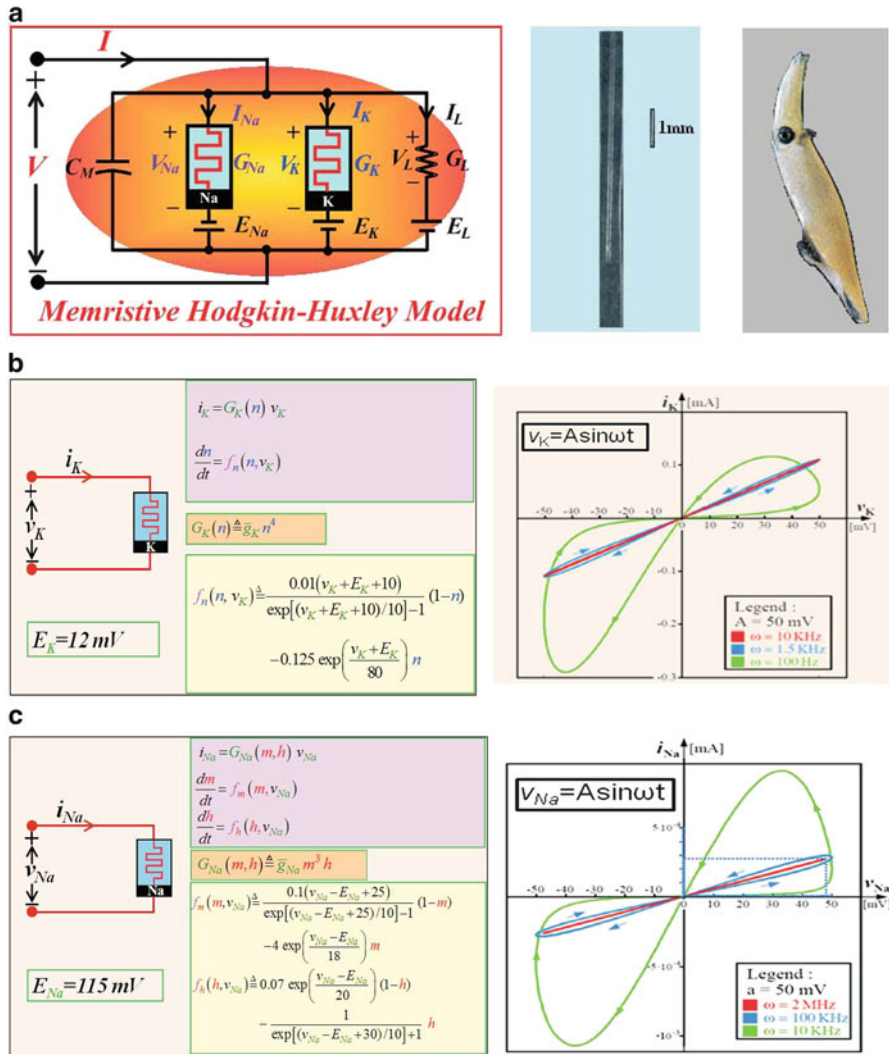


Fig. 2.4 Hodgkin–Huxley Axon. (a) Memristive Hodgkin–Huxley Circuit model of giant axon (center) of North Atlantic squid *Loligo* (right). (b) Potassium ion-channel memristor and its pinched hysteresis loops. (c) Sodium ion-channel memristor and its pinched hysteresis loops [18]

2.2 Concluding Remarks

Any 2-terminal device which exhibits a pinched hysteresis loop in the v - i plane when driven by *any* bipolar periodic voltage or current waveform, for *any* initial conditions, is a *memristor*. In the case where the *memristance* $R(x_1, x_2, \dots, x_n)$ does not depend on the current i , the loop shrinks to a straight line whose slope depends on the excitation waveform, as the excitation frequency tends to infinity.

Except in ideal cases, memristors, memcapacitors, and meminductors do *not* behave like resistors, capacitors, and inductors, respectively. For example, the potassium and sodium ion channel memristors in the Hodgkin–Huxley axon circuit model behave like R-L circuits ([18, 39]). It is conceptually wrong and misleading to identify memristors, memcapacitors, and meminductors with resistors, capacitors, and inductors. Each (α, β) element is a distinct circuit element because it cannot be built from the other elements.

Readers who may have been misled by some erroneous commentary in the popular press which associates an earlier *gadget* called a *memistor* with the *memristor* are referred to a technical clarification in [40].

We end this tutorial with the following succinct signature of a *memristor* [13]:

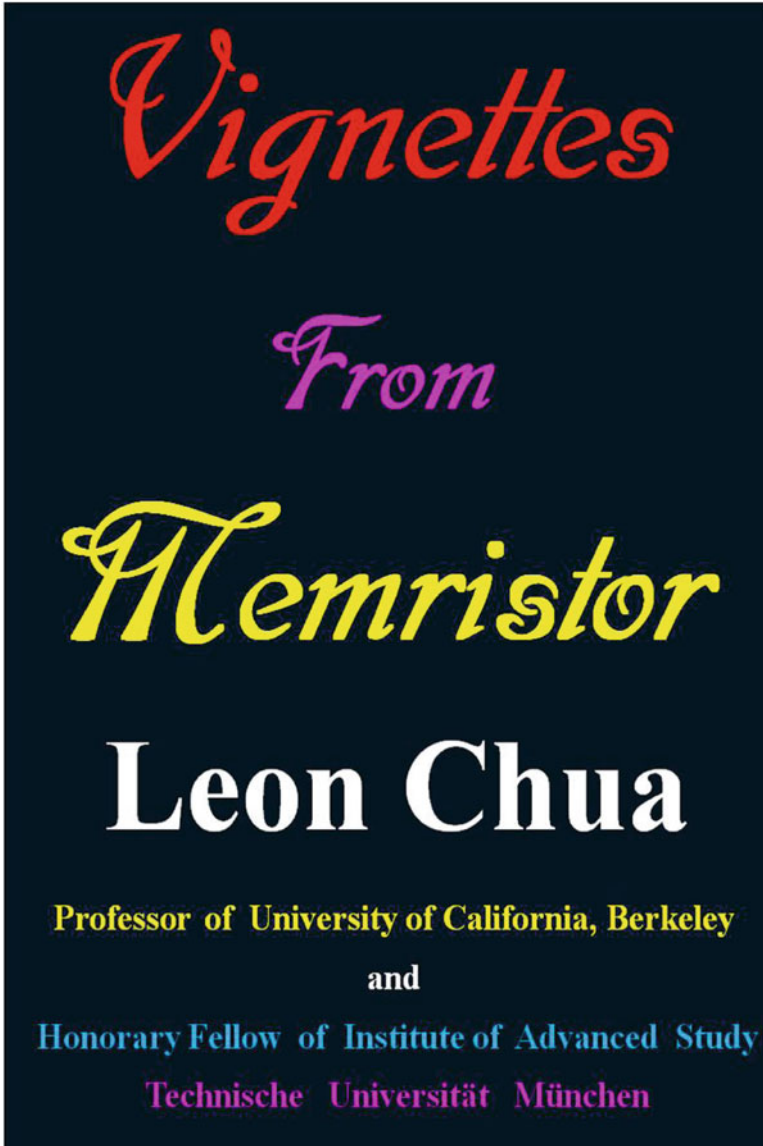
If it's pinched it's a memristor.

References

1. J.M. Tour, T. He, The fourth element. *Nature* **453**, 42–43 (1 May 2008)
2. L.O. Chua, *Introduction to Nonlinear Network Theory* (McGraw Hill Book Co., New York, 1969)
3. L.O. Chua, Device modeling via basic nonlinear circuit elements. *IEEE Trans. Circuit Syst.* **27**, 1014–1044 (1980)
4. L.O. Chua, Nonlinear circuit foundations for nano devices, Part I: The four-element torus. *Proc. IEEE* **91**, 1830–1859 (2003)
5. L.O. Chua, Memristor: The missing circuit element. *IEEE Trans. Circuit Theory* **18**, 507–519 (1971)
6. D.B. Strukov, G.S. Snider, D.R. Stewart, R.S. Williams, The missing memristor found. *Nature* **453**, 80–83 (2008)
7. L.O. Chua, Introduction to memristors. *IEEE Expert Now*, Educational Course, 2009
8. M. Di Ventra, Y.V. Pershin, L.O. Chua, Circuit elements with memory: memristors, memcapacitors, and meminductors. *Proc. IEEE* **97**, 1717–1723 (2009)
9. L.O. Chua, L.O.: Dynamic nonlinear networks: State of the art. *IEEE Trans. Circuits Syst.* **27**, 1059–1087 (1980)
10. D. Birolek, V. Biroleova, Mutator for transforming memristor into memcapacitor. *Electron. Lett.* **46**, 1428–1429 (2010)
11. Y.V. Pershin, M. Di Ventra, Teaching memory circuit elements via experiment-based learning. *arXiv: 1112.5427v1 [physics.ins-det]*
12. R.G. Bartle, *The Elements of Real Analysis*, 2nd edn. (Wiley, New York, 1976)
13. L.O. Chua, Resistance switching memories are memristors. *Appl. Phys. A* **102**, 765–783 (2011)
14. L.O. Chua, S.M. Kang, Memristive devices and systems. *Proc. IEEE* **64**, 209–223 (1976)
15. H. Kim, M.P. Sah, S.P. Adhikari, Pinched hysteresis loop is the fingerprint of memristive devices. *arXiv:1202.2437v1 [cond-mat.mes-hall]*
16. A.L. Hodgkin, A.F. Huxley, A quantitative description of membrane current and its application to the conduction and excitation in nerve. *J. Physiol.* **117**, 500–544 (1952)
17. K.S. Cole, *Membranes, Ions and Impulse* (University of California Press, Berkeley, 1972)
18. L. Chua, V. Sbitnev, H. Kim, Hodgkin Huxley axon is made of memristors. *Int. J. Bifurcat. Chaos* **22**(3), 1230011 (2012)
19. H. Ayrton, *The Electric Arc* (D. Van Nostrand Co., London, 1902)

20. T. Prodromakis, C. Toumazou, L. Chua, Two centuries of memristors. *Nat. Mater.* **11**, 478–481 (June 2012)
21. I. Valov, R. Waser, J.R. Jameson, M.N. Kozicki, Electrochemical metallization memories: Fundamentals, applications, prospects. *Nanotechnol.* **2**, 254003 (2011)
22. M.G. Bray, D.H. Werner, Passive switching of electromagnetic devices with memristors. *Appl. Phys. Lett.* **96**, 0735041-3 (2010)
23. J. Borghetti, G.S. Snider, P.J. Kukes, J.J. Yang, D.R. Stewart, R.S. Williams, Williams memristive switches enable 'stateful' logic operations via material implication. *Nature* **464**, 873–876 (2010)
24. D.B. Strukov, R.S. Williams, Four-dimensional address topology for circuits with stacked multilayer crossbar arrays. *Proc. Natl. Acad. Sci.* **106**, 20155–20158 (2009)
25. W. Lehtonen, M. Laiho, Stateful implication logic with memristors. *Proc. IEEE/ACM International Symposium on Architectures*, pp. 33–36, San Francisco, CA 2009
26. J. Borghetti, Z. Li, X. Straznicky, X. Li, A. Ohlberg, W. Wu, D.R. Stewart, R.S. Williams, A hybrid nanomemristor/transistor logic circuit capable of self-programming. *Proc. Natl. Acad. Sci.* **106**, 1699–1703 (2009)
27. K. Kim, S. Shin, S.-M. Kang, Field programmable stateful logic array. *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **30**, 1800–1813 (2011)
28. B. Linares-Barranco, T. Serrano-Gotarredona, Memristance can explain spike-time-dependent-plasticity in neural synapses. *Nature Precedings*, hdl:10101/npre. 2009.3010.1 : 31 March 2009
29. S.H. Jo, T. Chang, I. Ebong, B.B. Bhadviya, P.Lu.W. Mazumder, Nanoscale memristor device as synapse in neuromorphic systems. *Nano Lett.* **10**, 1297–1301
30. Pershin, Y.V., Di Ventra, M.: Neuromorphic, digital and quantum computation with memory circuit elements. arXiv:1009.6025v3 [cond-mat.mes-hall]
31. G.S. Snider, Spike-timing dependent learning in memristive nanodevices, *IEEE/ACM International Symposium on Nanoscale Architecture*, Anaheim, CA, 85–92, 2008
32. T. Liu, Y. Kang, M. Verma, M. Orlowski, Novel Highly Nonlinear Memristive Circuit Elements for Neural Networks. *Proceedings, 2012 IJCNN International Joint Conference on Neural Networks*, in Brisbane, Australia, June 2012, doi 10.1109/IJCNN.2012.6252460
33. T. Chang, S.-H. Jo, W. Lu, Short-term memory to long-term memory transition in a nanoscale memristor. *Am. Chem. Soc. (ACS) Nano* **5**, 7669–7676 (2011)
34. M. Itoh, L.O. Chua, Memristor oscillators. *Int. J. Bifurcat. Chaos* **18**, 3183–3206 (2008)
35. B. Muthuswamy, L.O. Chua, Simplest chaotic circuit. *Int. J. Bifurcat. Chaos* **20**, 1567–1580 (2010)
36. J.-M. Ginoux, C. Letellier, L.O. Chua, Topological analysis of chaotic solution of a three-element memristive circuit. *Int. J. Bifurcat. Chaos* **20**, 3819–3827 (2010)
37. M. Itoh, L.O. Chua, Memristor Hamiltonian circuits. *Int. J. Bifurcat. Chaos* **21**, 2395–2425 (2011)
38. V.-T. Pham, A. Buscarino, M. Frasca, L. Fortuna, Autowaves in memristive cellular neural networks. *Int. J. Bifurcat. Chaos* **22**, 12300271-9 (2012)
39. L. Chua, V. Sbitnev, H. Kim, Neurons are poised near the edge of chaos. *Int. J. Bifurcat. Chaos* **22**(4), 1250098 (2012)
40. H. Kim, S.P. Adhikari, Memristor is not memristor. *IEEE Circuits and Systems Magazine*, First Quarter 2012, pp. 75–78

Part II



Vignettes

From

Memristor

Leon Chua

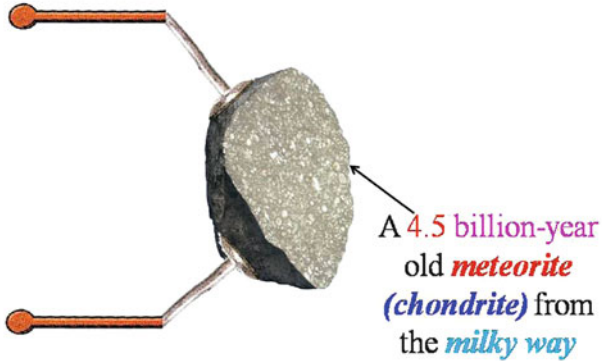
Professor of University of California, Berkeley

and

Honorary Fellow of Institute of Advanced Study

Technische Universität München

What is this Device ?



What is a *resistor*, *inductor*, and *capacitor* ?

Shocking Fact !

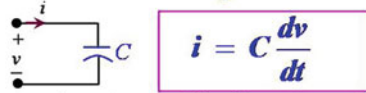
Before the publication of my book *Introduction to Nonlinear Network Theory* in 1969, there was no scientific definition of *basic circuit elements*.

Standard definitions from classical Circuit Theory textbooks:

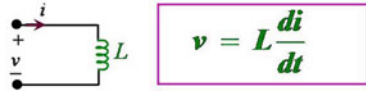
What is a **Resistor** ?



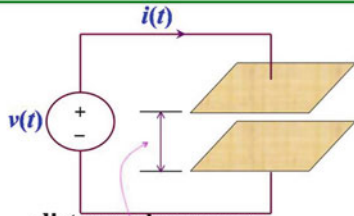
What is a **Capacitor** ?



What is an **Inductor** ?



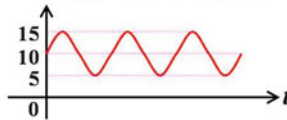
Time-varying Capacitance $C(t)$



distance changes as a function of time, giving a *time-varying capacitance* $C(t)$

Example:

$$C(t) = 10 + 5 \sin t$$



Example : Time-varying Capacitance

$$i(t) = \underbrace{(10 + 5 \sin t)}_{C(t)} \frac{dv(t)}{dt}$$

Does this obvious generalization of the formula

$$i = C \frac{dv}{dt}$$

give the correct current $i(t)$ for any applied voltage $v(t)$?

Does this calculated
capacitor current agree
with the *laboratory*
measurement?

No !

Reason :

Our classical definition
of the *capacitor* is wrong.

The *classical* definition

$$i(t) = C \frac{dv(t)}{dt}$$

uses an *incorrect pair* of
variables

$$i(t) \text{ and } v'(t) \triangleq \frac{dv(t)}{dt}$$

Let us *integrate* both
sides to obtain

$$q(t) = C v(t)$$

This equation defines a
relationship between a
different pair of
variables $q(t)$ and $v(t)$,
and gives the *correct*
answer.

Correct formula:

$$q(t) = C(t) v(t)$$

$$q(t) = (10 + 5 \sin t) v(t)$$


$$i = \frac{dq(t)}{dt} = \underbrace{(10 + 5 \sin t)}_{C(t)} \frac{dv(t)}{dt} + (5 \cos t) v(t)$$

$$i = \frac{dq(t)}{dt} = C(t) \frac{dv(t)}{dt} + v(t) \frac{dC(t)}{dt}$$

extra term is needed !

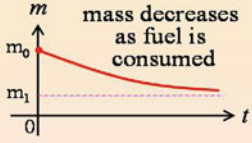
An analogy of a
similar mistake
from **Mechanics**

Rocket Launching



Rocket

force $f(t)$



mass decreases
as fuel is
consumed

Newton's
Law of Motion

$$f(t) = m(t) \frac{dv}{dt}$$

Is this formula
correct ?

Newton's Law of Motion

High school physics:

$$f = m a$$

College Physics:

$$f = m \frac{dv}{dt}$$

➔ $p = m v$

NO !

Correct Newton's Formula is:

$$f = \frac{dp}{dt}$$

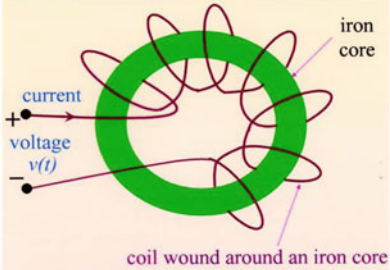
$$p = mv \quad \leftarrow \text{momentum}$$

For *time-varying mass*, we have:

$$p = m(t) v$$

∴

$$f(t) = m(t) \frac{dv}{dt} + v(t) \underbrace{\frac{dm(t)}{dt}}_{\text{extra term !}}$$

Inductor L 

$$v = L \frac{di}{dt}$$

L is called
the *Inductance* of the Inductor L .

Inductor

The *classical definition*

$$v = L \frac{di}{dt}$$

which relates the 2 variables *voltage* v and the *derivative* $i' \triangleq \frac{di}{dt}$ gives the **wrong** answer !

The correct definition

$$\varphi = L i$$

relates the 2 variables *flux* φ and *current* i

Correct formula:

$$\varphi(t) = L(t) i(t)$$

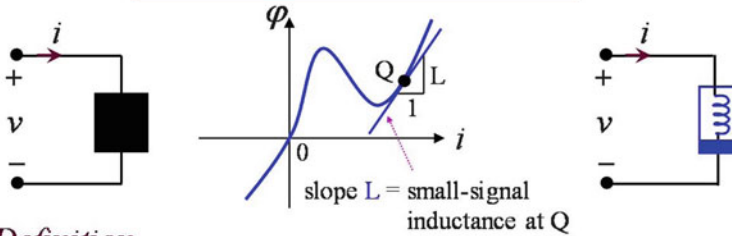
$$\varphi(t) = \underbrace{(10 + 5 \sin t)}_{L(t)} i(t)$$

$$v = \frac{d\varphi(t)}{dt} = \underbrace{(10 + 5 \sin t)}_{L(t)} \frac{di(t)}{dt} + (5 \cos t) i(t)$$

$$v = \frac{d\varphi(t)}{dt} = L(t) \frac{di(t)}{dt} + \underbrace{i(t) \frac{dL(t)}{dt}}_{\text{extra term is needed !}}$$

Conclusion:
 A *time-varying inductance* $L(t)$ must be defined by a relationship between the *flux* $\varphi(t)$ and the *current* $i(t)$, and *not* between $v(t)$ and $\frac{di(t)}{dt}$, as in the *incorrect* formula $v = L(t) \frac{di}{dt}$

What is an Inductor ?



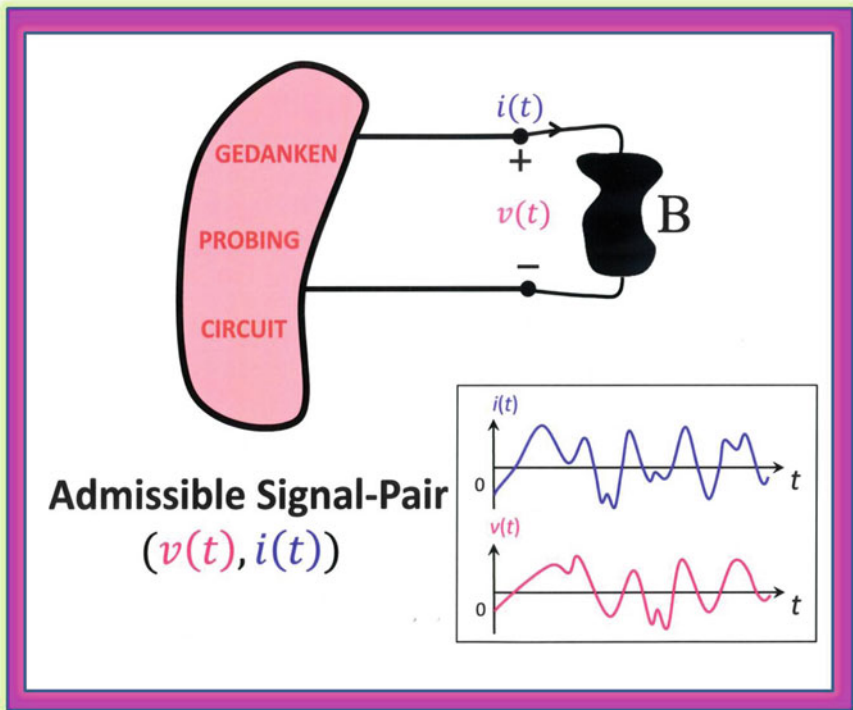
Definition

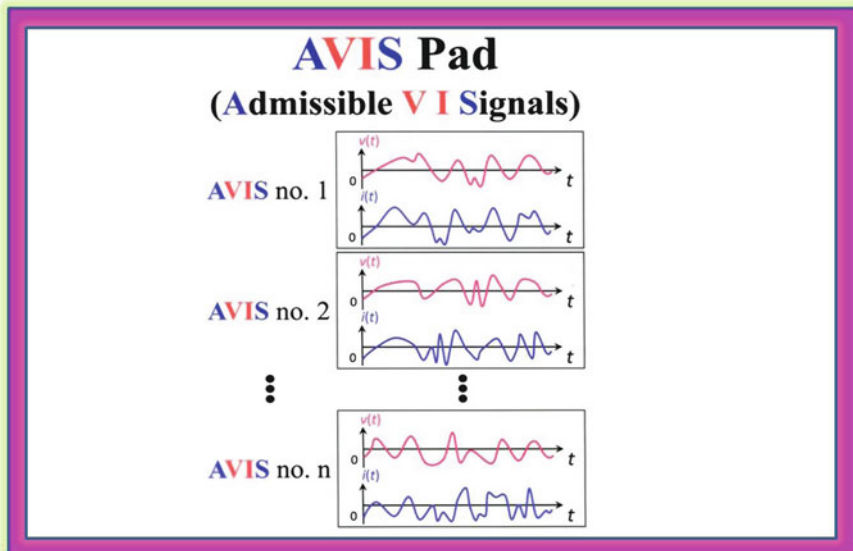
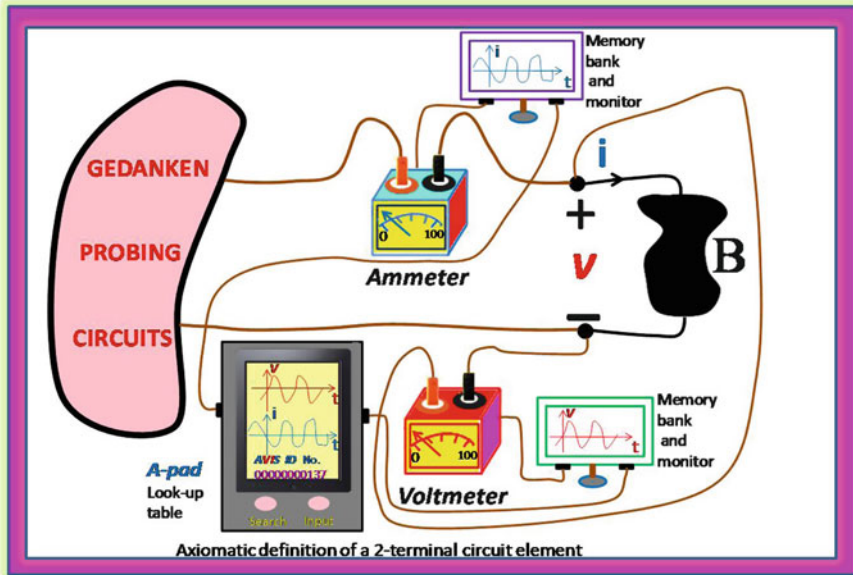
Any device which imposes a *relationship* between the **flux** $\varphi \triangleq \int_{-\infty}^t v(t) dt$ and the **current** i is an **inductor**. The *slope* at any point Q is called the *small-signal inductance* L at Q

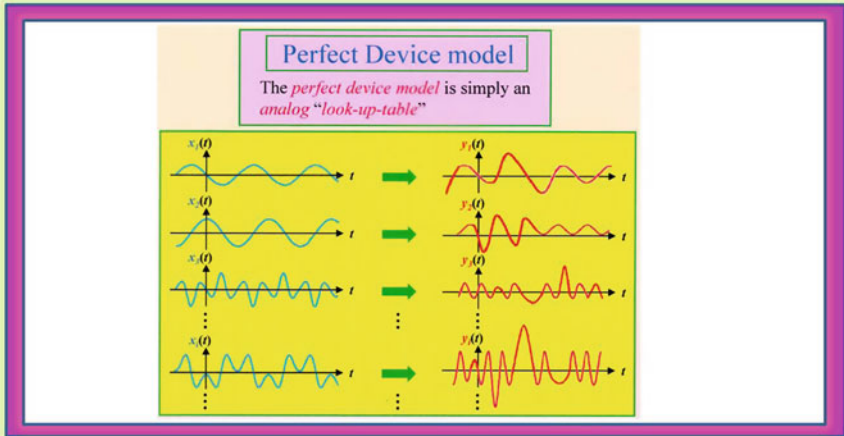
Axiomatic Definitions

To obtain the correct definitions of *elementary circuit elements*, it is necessary to introduce an *axiomatic approach* involving the 4 basic circuit variables *voltage* $v(t)$, *current* $i(t)$, *flux* $\varphi(t)$, and *charge* $q(t)$.

Axiomatic Definition of Circuit Elements



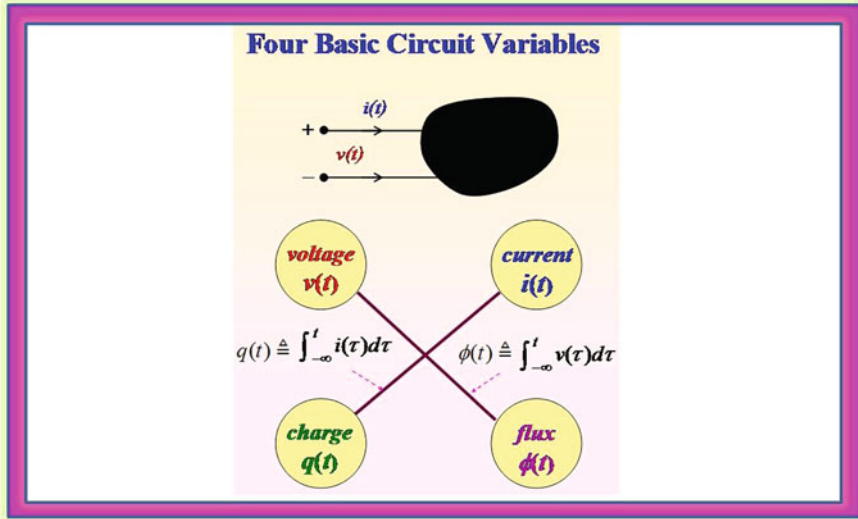




No device model is Perfect

A useful device model must reproduce the input-output behaviors of a physical device to acceptable engineering accuracy.

Model must Predict !

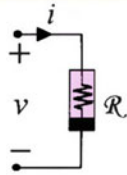
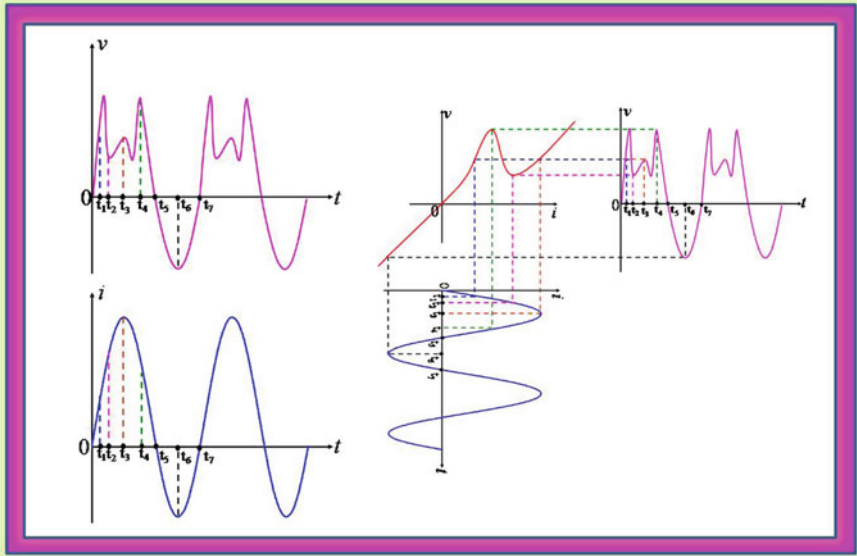


FOUR ELEMENTARY CIRCUIT ELEMENTS

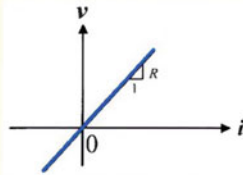
What is a Resistor ?

Definition

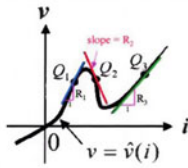
Any device which imposes a *relationship* between the **voltage** v and the **current** i is a **resistor**. The *slope* at any point Q is called the *small-signal resistance* R at Q



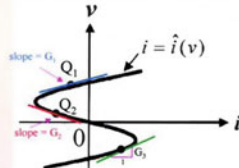
Nonlinear Resistor \mathcal{R}



Linear resistor: $V = Ri$ or $i = GV$
 $R = \text{Resistance}$, $G \triangleq \frac{1}{R} = \text{Conductance}$

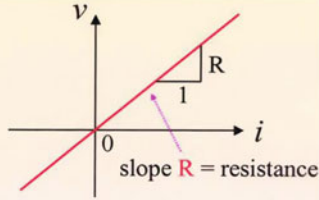
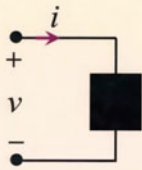


Current-controlled Resistor: $v = \hat{v}(i)$
 $R_i = \text{small-signal resistance at } Q_i$



Voltage-controlled Resistor: $i = \hat{i}(v)$
 $G_i = \text{small-signal conductance at } Q_i$

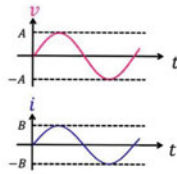
Simplest Example of a Resistor



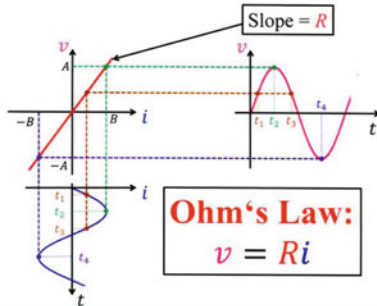
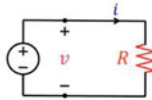
Special Case : Linear resistor

Ohm's Law

$$v = R i$$

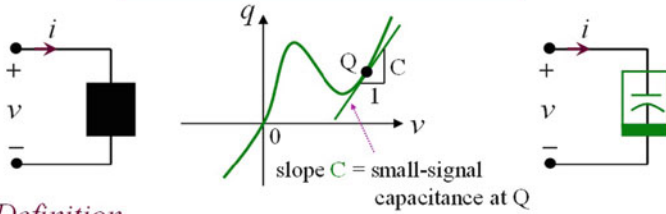


Resistor



Ohm's Law:
 $v = Ri$

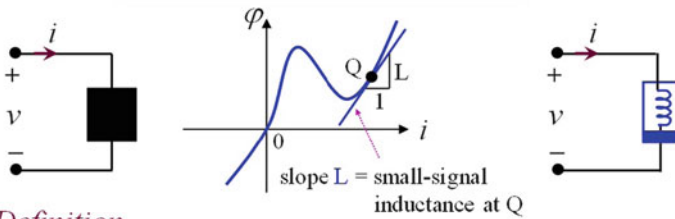
What is a Capacitor ?



Definition

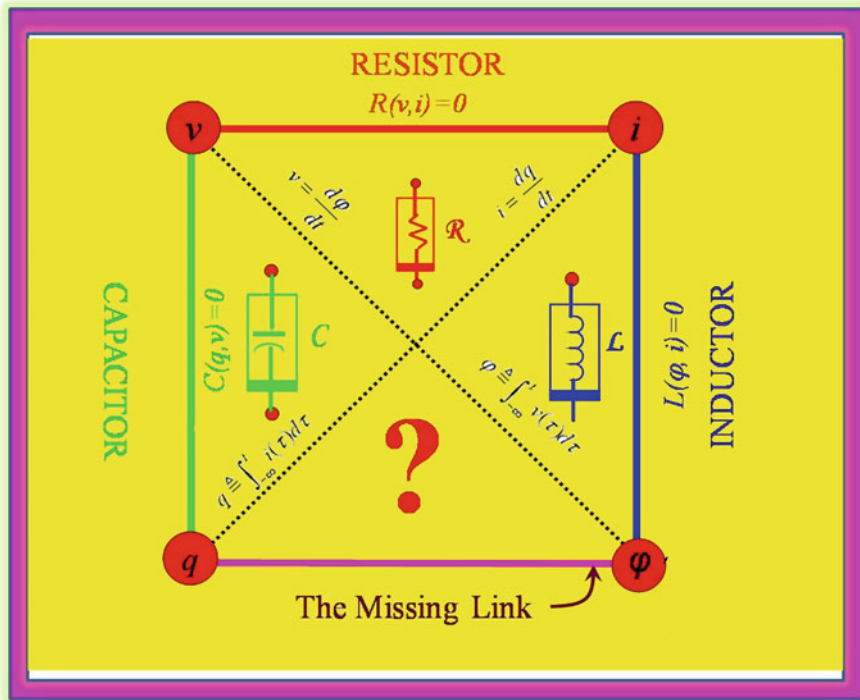
Any device which imposes a *relationship* between the **voltage** v and the **charge** $q \triangleq \int_{-\infty}^t i(t) dt$ is a **capacitor**. The *slope* at any point Q is called the *small-signal capacitance* C at Q

What is an Inductor ?



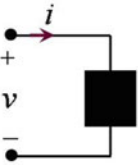
Definition

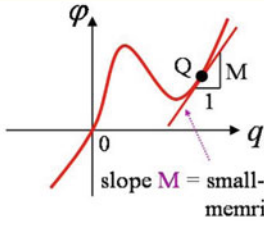
Any device which imposes a *relationship* between the **flux** $\varphi \triangleq \int_{-\infty}^t v(t) dt$ and the **current** i is an **inductor**. The *slope* at any point Q is called the *small-signal inductance* L at Q



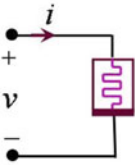
The missing
circuit element
is the
memristor!

What is a Memristor ?



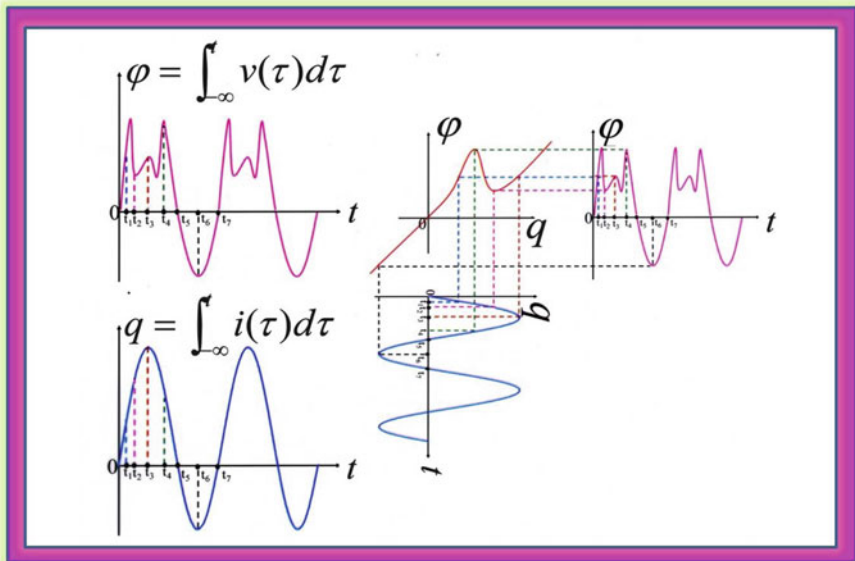


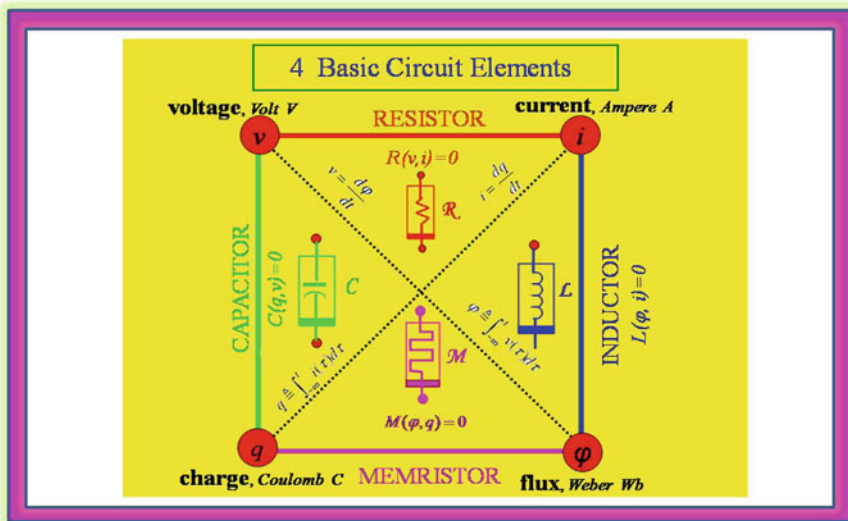
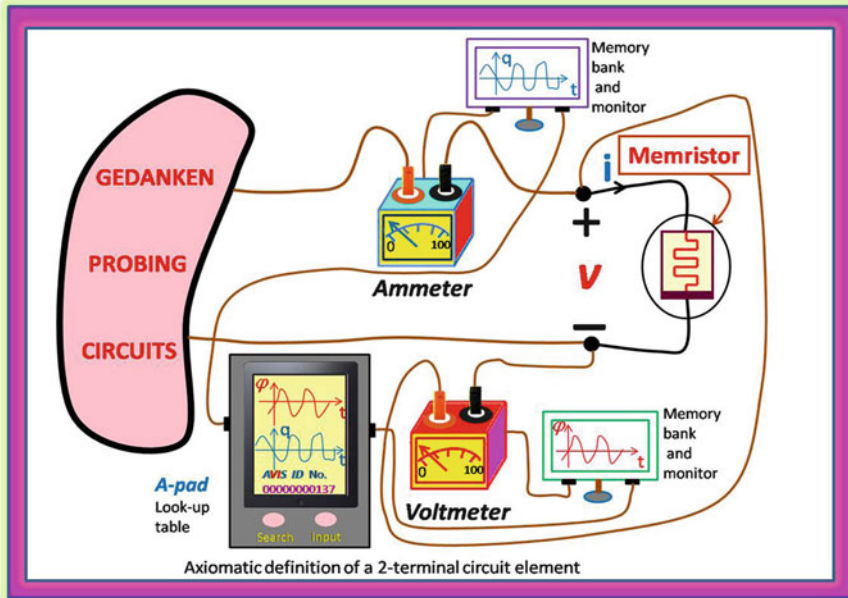
slope M = small-signal memristance at Q

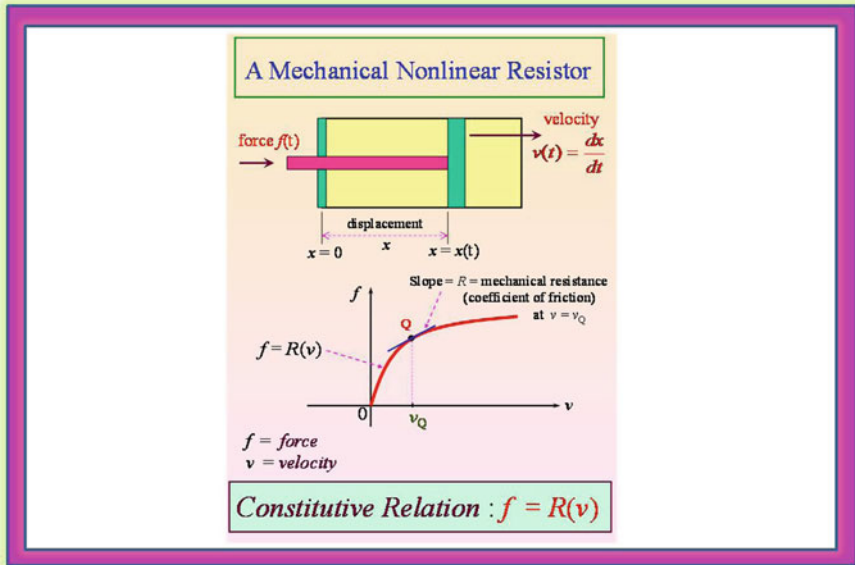
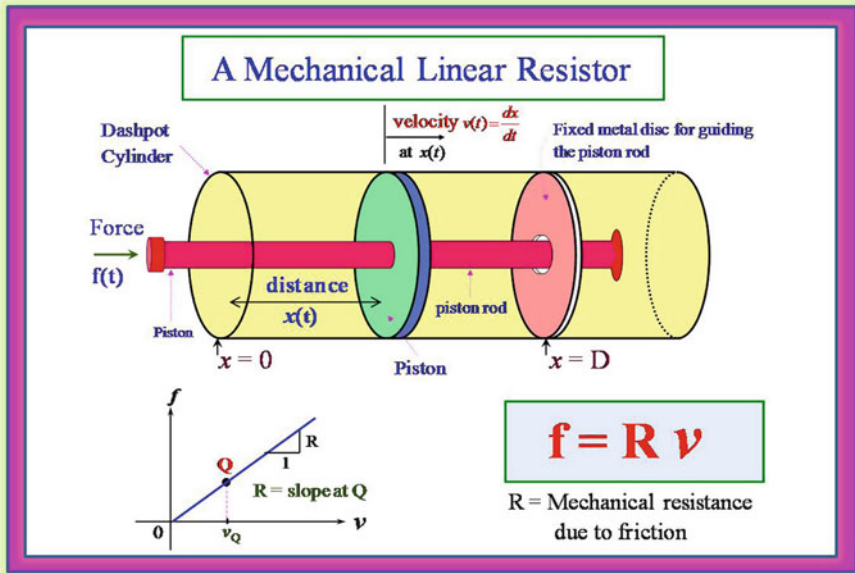


Definition

Any device which imposes a *relationship* between the **charge** $q \triangleq \int_{-\infty}^t i(t) dt$ and the **flux** $\phi \triangleq \int_{-\infty}^t v(t) dt$ is a **Memristor**. The *slope* at any point Q is called the *small-signal memristance* M at Q







Newton's Equation

High School version:

force = mass \times acceleration

$$f = m \frac{dv}{dt}$$

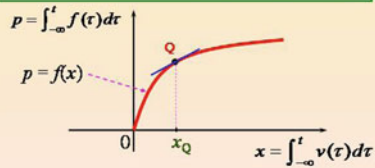
Integrating both sides:

$$\underbrace{\int_{-\infty}^t f(t) dt}_{\text{Momentum}} = m \underbrace{\int_{-\infty}^t \frac{dv}{dt} dt}_{\text{velocity}}$$

Correct Newton's Equation:

$$p = mv$$

A Mechanical Memristor



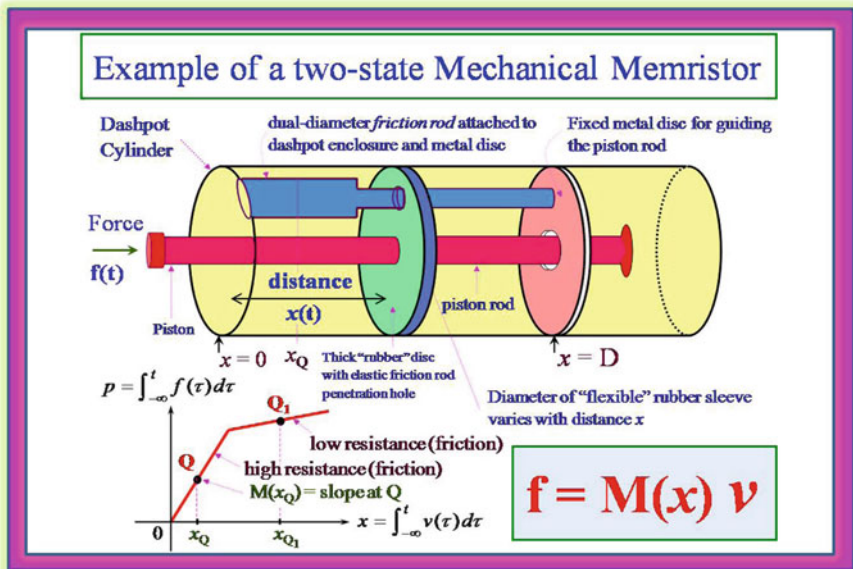
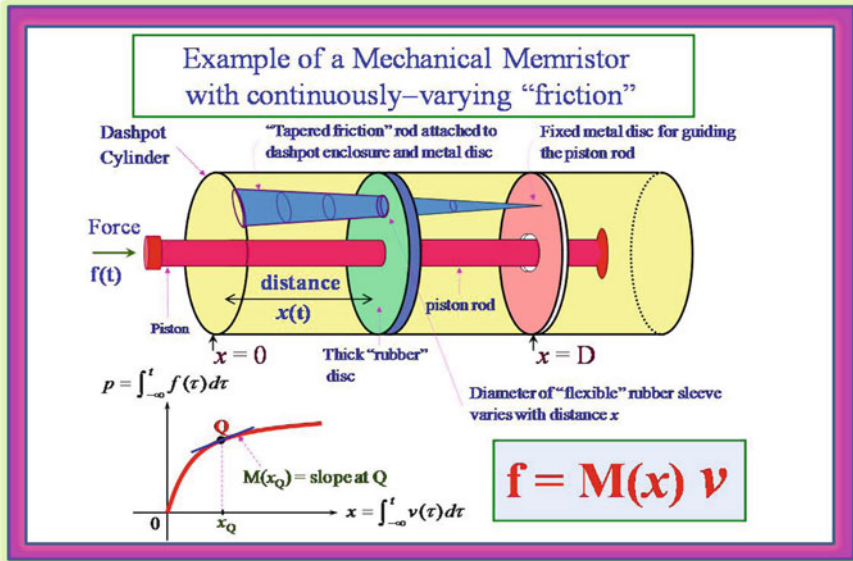
p = momentum, f = force

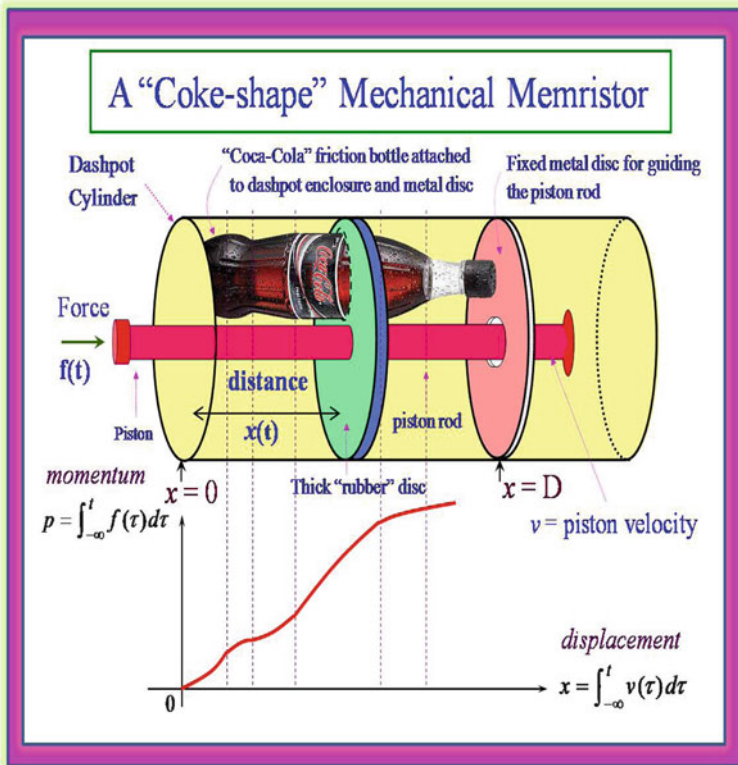
x = displacement (distance)

from some reference point, v = velocity

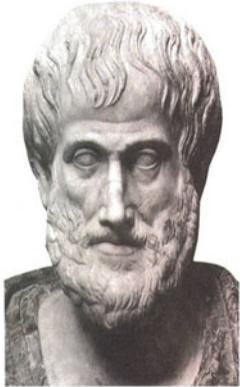
Constitutive Relation : $p = f(x)$

$$\underbrace{\frac{dp}{dt}}_{\text{Force}} = \underbrace{\frac{df(x)}{dx}}_{\text{Memristance}} \underbrace{\frac{dx}{dt}}_{\text{Velocity}}$$





Our
4 Circuit-Element
Axiomatic
Approach
dates back to
Aristotle !



Aristotle, 350 BC

Our *axiomatic definitions*
of the *4 elementary circuit*
elements is analogous to
Aristotle's definitions of the
4 building blocks of matter.

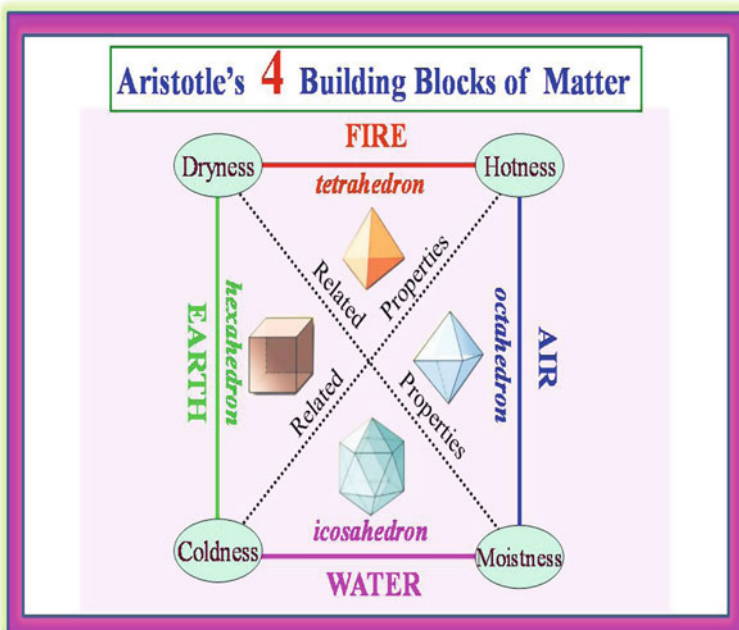
Aristotle's Theory of Matter

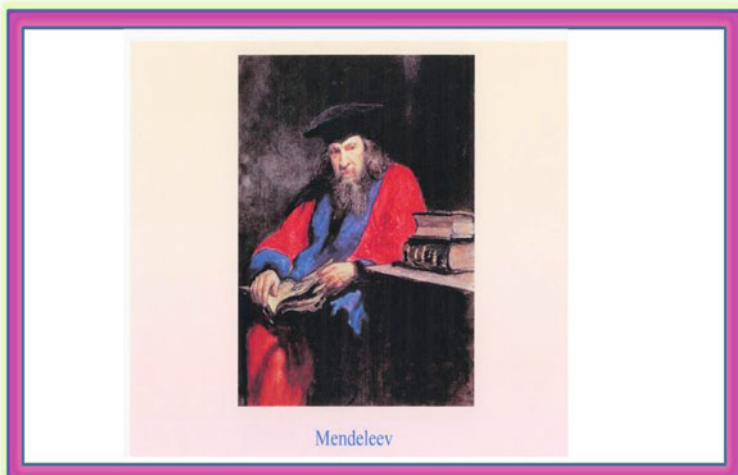
All *matter* consisted of *four elements*:

1. EARTH
2. WATER
3. AIR
4. FIRE

Each of these elements exhibited two of *four*
fundamental properties :

- Moistness
- Dryness
- Coldness
- Hotness





Mendeleev's First Published Periodic Table, 1869

но въ ней, мнѣ кажется, уже ясно выражается приближность въ ставляемаго мною начала ко всей совокупности элементовъ, пай которыхъ известны съ достоверностію. На этотъ разъ я и желаю преимущественно найти общую систему элементовъ. Вотъ этотъ опытъ:

			Ti=50	Zr=90	?=180.
			V=51	Nb=94	Ta=182.
			Cr=52	Mo=96	W=186.
			Mn=55	Rh=104,4	Pt=197,4
			Fe=56	Ru=104,4	Ir=198.
			Ni=Co=59	Pt=106,6	Os=199.
			Cu=63,4	Ag=108	Hg=200.
			Zn=65,2	Cd=112	
			?=68	Ur=116	Au=197?
			?=70	Su=118	
			As=75	Sb=122	Bi=210
			Se=79,4	Te=128?	
			Br=80	I=127	
			Rb=85,4	Cs=133	Tl=204
			Sr=87,6	Ba=137	Pb=207.
			Ce=92		
			La=94		
			Di=95		
			Th=118?		
			?=45		
			?Er=56		
			?Yt=60		
			?In=75,6		

и потому приходится изъ разныхъ рядовъ нѣять различное количество элементовъ, чего нѣтъ въ главныхъ члесахъ предлагаемой таблицы. Не же придется предполагать при составленіи системы очень много недостающихъ членовъ. То и другое было бы выгодно. Мнѣ кажется притоку, наиболее естественныхъ составовъ

Dmitri Mendeleev's
idea of the *periodic table*
of elements originated
from a *dream*.

Nature

pages 42–43

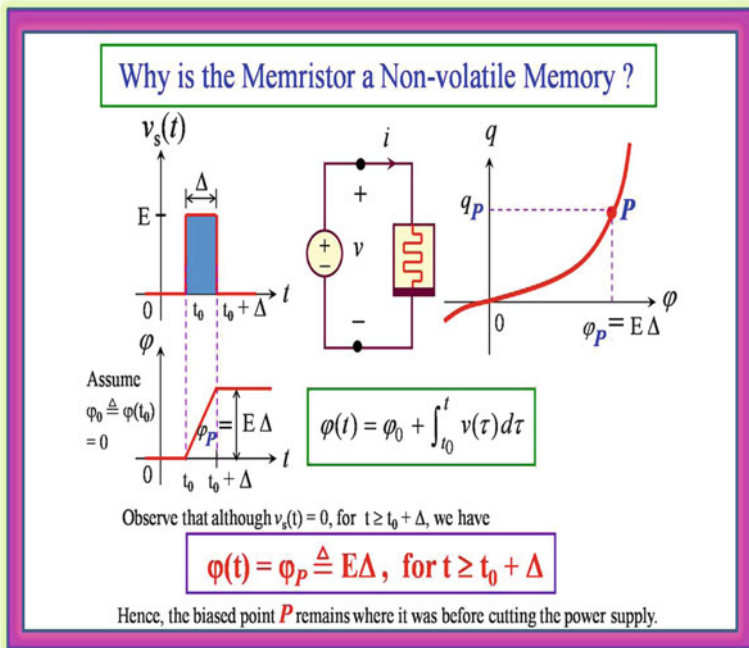
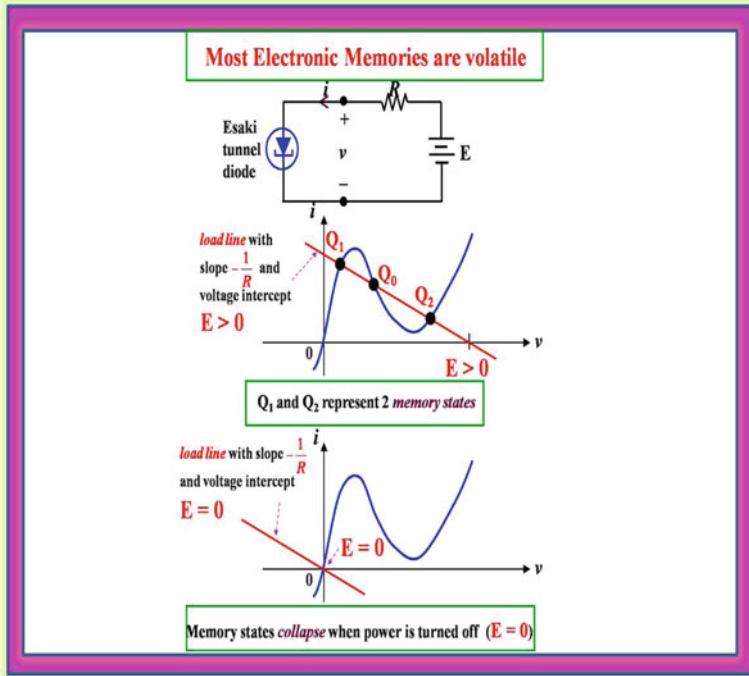
May 1, 2008

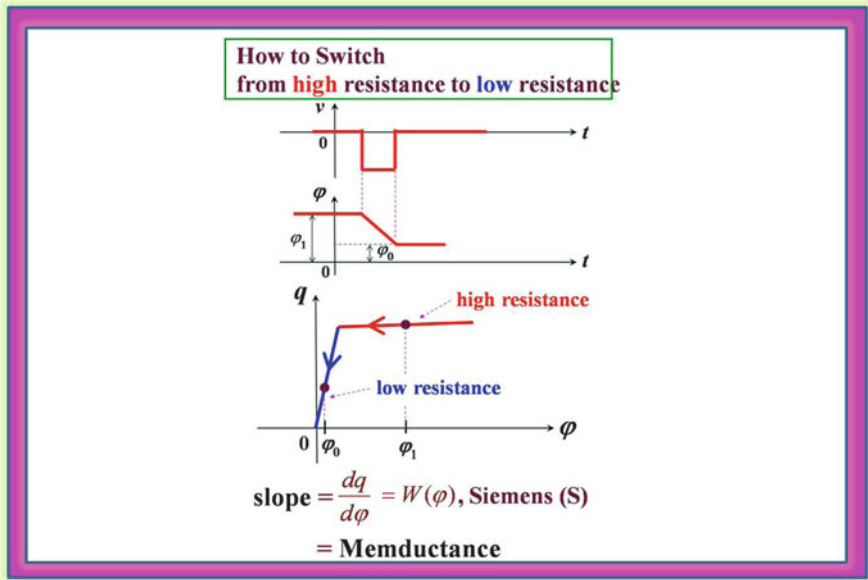
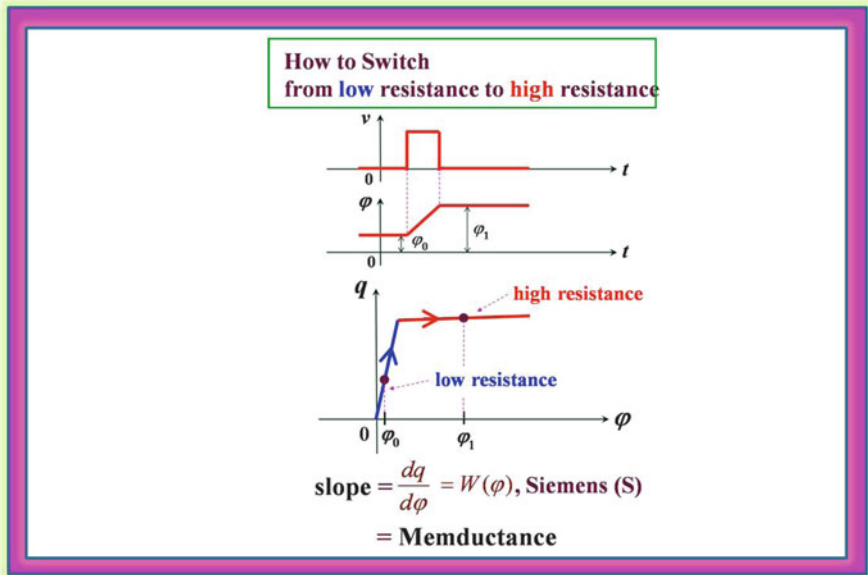
ELECTRONICS

The fourth element

James M. Tour and Tao He

Almost four decades since its existence was first proposed, a fourth basic circuit element joins the canonical three. The 'memristor' might herald a step-change in the march towards ever more powerful circuitry.





How to Write Memory State ?

An Illustrative Example

Assume initial condition $\varphi_0 \hat{=} \varphi(0) = 0$

Initial condition Assume $\varphi(0) = 0$ at $t = 0$

$$\varphi(t) = \int_0^t v(\tau) d\tau$$

To WRITE binary state **0**, bias memristor at $Q_0(1, 0.5)$
 $\varphi(Q_0) = (\Delta E) (\Delta t) = 1$
 \therefore Choose $\Delta E = \frac{1}{\Delta t}$ Volt

To WRITE binary state **1**, bias memristor at $Q_1(3, 3)$
 $\varphi(Q_1) = (\Delta E) (\Delta t) = 3$
 \therefore Choose $\Delta E = \frac{3}{\Delta t}$ Volt

How to Read Memory State ?

An Illustrative Example

$i(t) = \dot{q}(t)$


flux-controlled q-φ curve

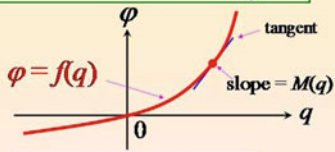
Apply a small and narrow voltage doubles sensing signal.

High-resistance state **1**
 $R_1 = \frac{1}{\epsilon_1}$ gives large output i_0 current doubles

Low-resistance state **0**
 $R_2 = \frac{1}{\epsilon_2}$ gives small output current i_0 doubles

Memristor





$\phi = f(q)$

slope = $M(q)$

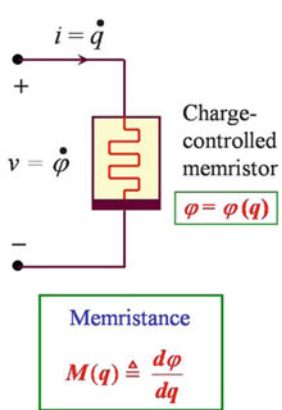
$\phi = f(q)$

$$v = \frac{d\phi}{dt} \equiv \underbrace{\frac{df(q)}{dq}}_{M(q)} \cdot \underbrace{\frac{dq}{dt}}_i$$

$v = M(q) i$

$M(q)$ is called the *Memristance*.

Example: A two-state Charge-Controlled Memristor

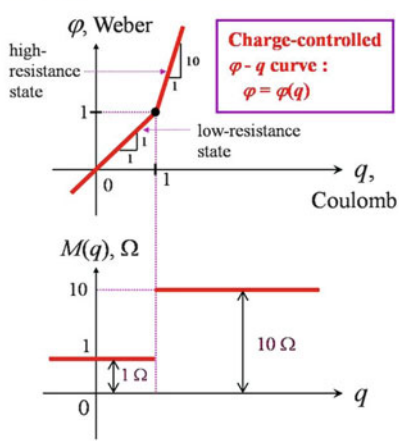


Charge-controlled memristor

$\phi = \phi(q)$

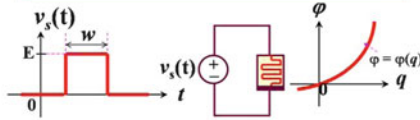
Memristance

$$M(q) \triangleq \frac{d\phi}{dq}$$



Charge-controlled $\phi - q$ curve : $\phi = \phi(q)$

Memristor is an Analog Non-volatile memory



For a *memristor* with a *smooth* function $\phi = \phi(q)$, we can obtain a *continuous range* of *resistances*, *not* just binary states, by simply choosing the *pulse height* E , or the *pulse width* w of a biasing voltage pulse.

Application : Ideal for neural network learning via *synaptic* tunings. With the tiny HP memristor, which can be scaled down to 2 nanometers, it is possible to mimic biological neurons with more than 20,000 synapses per neuron.

How do you know your device may be a Memristor ?

Examine:

$$v = M(q) i$$

or

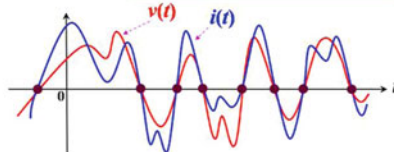
$$i = G(\phi) v$$

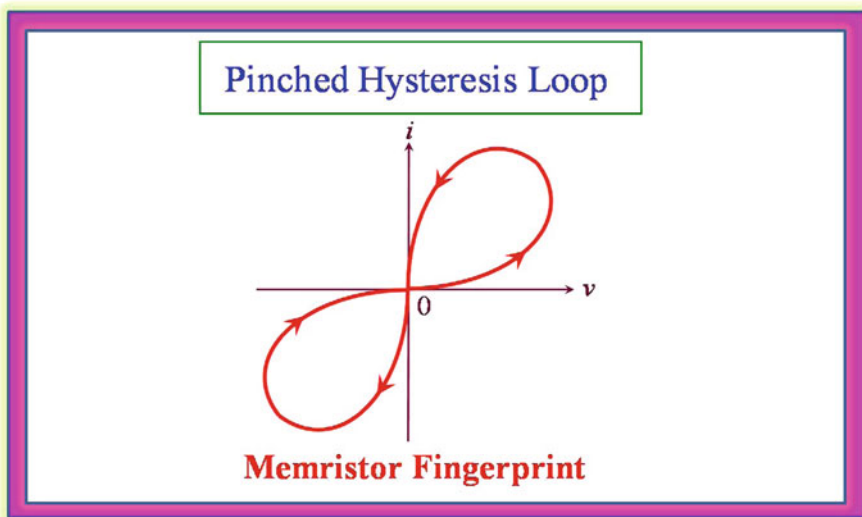
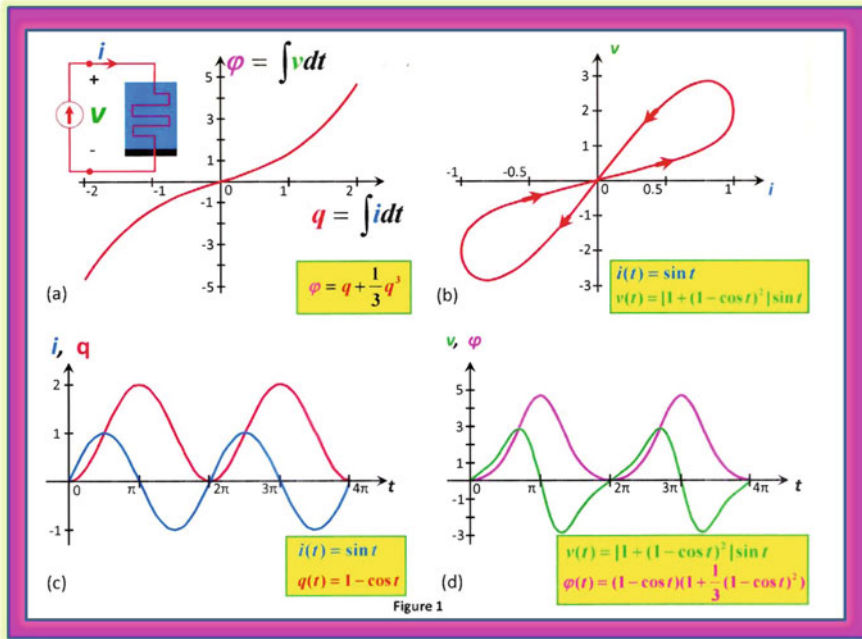


$$v(t) = 0 \iff i(t) = 0$$

Memristor Fingerprint

Both $v(t)$ and $i(t)$ of a *memristor* must have *identical zero crossings*, i.e., they must be *in phase*.

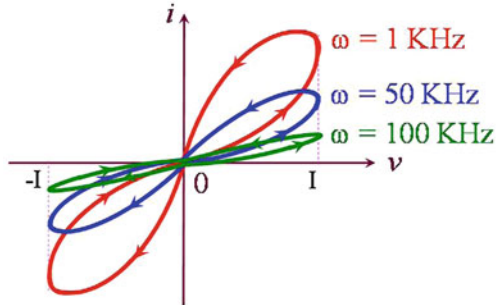




Theorem

Memristor pinched hysteresis loop shrinks continuously as frequency increases.

Example



The *pinched hysteresis loop* of a memristor becomes *thinner* as frequency ω increases, and tends to a *straight line* as $\omega \rightarrow \infty$

High-Frequency Memristor Behavior

$$\begin{aligned} \varphi(t) &= \varphi_0 + \int_0^t A \sin(\omega\tau) d\tau \\ &= \varphi_0 + \frac{A}{\omega} (\cos \omega t - \cos \omega t_0) \rightarrow \varphi_0, \text{ as } \omega \rightarrow \infty \end{aligned}$$

Memductance at $\omega \rightarrow \infty$

$$W(\varphi(t)) \rightarrow W(\varphi_0)$$

Memristance at $\omega \rightarrow \infty$

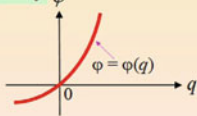
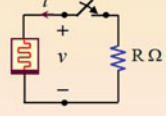
$$M(q(t)) \rightarrow M(q_0)$$

where

$$M(q_0) = \frac{1}{W(\varphi_0)}$$

Theorem : No Energy-Storage Property
Memristors can not Store Energy

Proof

Assumptions:
 $R > 0, M(q) \triangleq \frac{d\phi(q)}{dq} \geq 0, q(0) \neq 0$ (Initial condition)

$$\frac{d\phi}{dt} = \frac{d\phi(q)}{dq} \frac{dq}{dt}$$

$$\overset{v_M = -Ri}{=} -R \frac{dq}{dt} = \frac{d\phi(q)}{M(q)} \frac{dq}{dt}$$

$$\Rightarrow [R + M(q)] \frac{dq}{dt} = 0 \Rightarrow \frac{dq}{dt} = 0$$

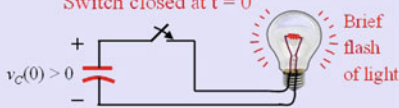
$$\Rightarrow q(t) = q(0), t > 0$$

$$\Rightarrow i(t) = v(t) = 0, t > 0$$

$$\Rightarrow \text{Power } p(t) = v(t)i(t) = 0, t > 0 \quad \blacksquare$$

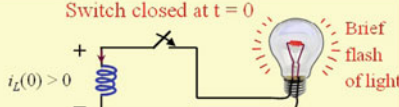
Demonstration Showing
Memristors can not Store Energy

Switch closed at $t = 0$



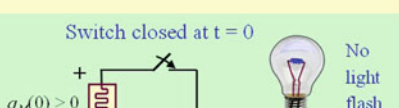
Brief flash of light

Switch closed at $t = 0$



Brief flash of light

Switch closed at $t = 0$



No light flash

Memristor

Memristor Passivity Condition

The $\phi - q$ curve of all physical *memristors* must be a *monotone-increasing* function.

Examples

Proof of the Memristor Passivity Condition

Consider a *non-monotone-increasing* memristor, and apply the following voltage signal $v_s(t)$, and its associated flux $\phi(t)$.

$\delta\phi(t) = -k\delta q(t)$

$\delta\phi(t) \cdot \delta q(t) < 0$

$\delta v(t)$ and $\delta i(t) = \frac{d}{dt}(\delta\phi(t))$ have *opposite phase*, i.e.,

$\delta v(t) \cdot \delta i(t) < 0$

$\delta w(t) \triangleq \int_{-\infty}^t (\delta v(\tau))(\delta i(\tau)) d\tau \rightarrow -\infty$

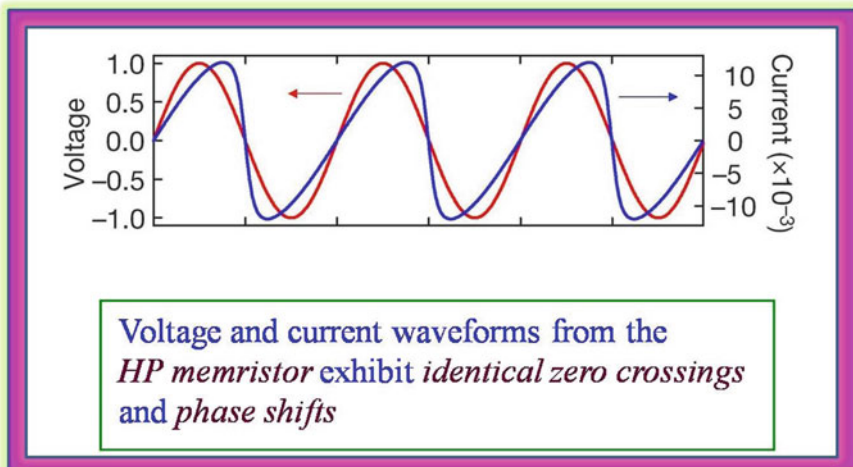
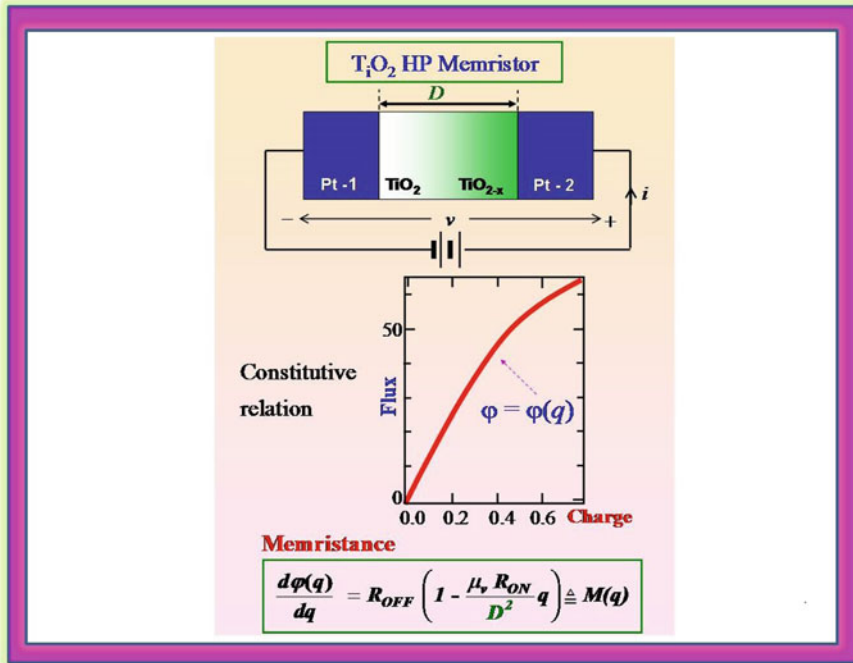
$w(t) \triangleq \int_{-\infty}^t v_s(\tau) i(\tau) d\tau = \text{Energy}$

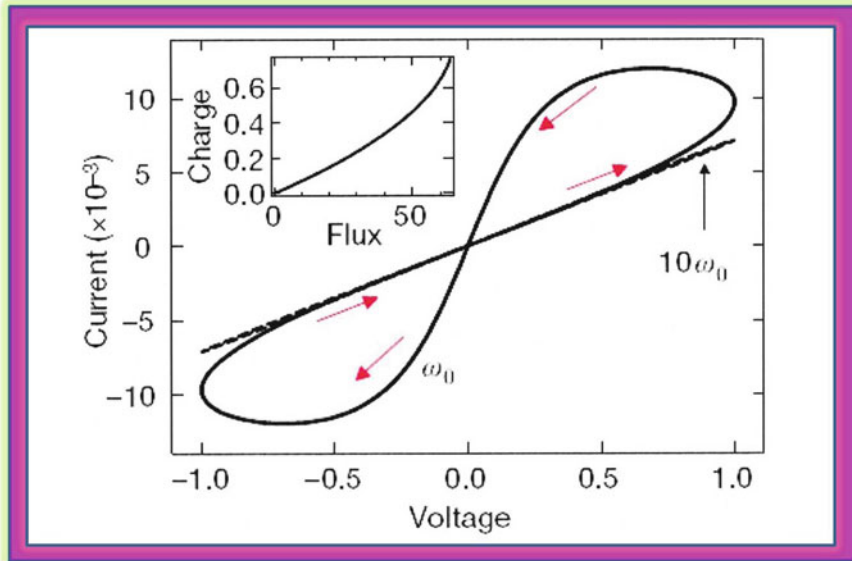
$w(t) \rightarrow -\infty$ implies that this *memristor* is capable of supplying an infinite amount of energy, which is impossible!

Is it possible to
build a
*passive solid state
memristor* ?

Answer :

Yes, provided the *memristor* satisfies the *memristor passivity condition*.



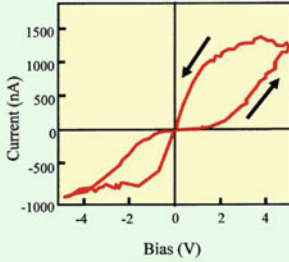


Memristor Model of an Experimental Nano Device

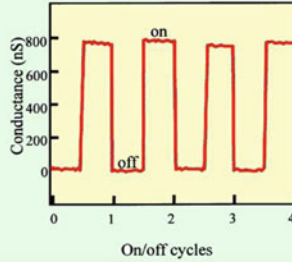
The following slide shows a nano device, reported from Professor Lieber's Harvard Nano-device Laboratory, whose experimentally measured v - i *characteristic* is a *pinched hysteresis loop*. The conductance of the device can be switched from "0" nS (*off state*), to 800 nS (*on state*), by applying a *square wave*.

Professor Lieber had confirmed (private communication) that the loop "shrinks" with increasing frequency. This device can therefore be modeled as a *memristor*.

Pinched Hysteresis Loop from Lieber's Harvard Laboratory



(a) Pinched hysteresis loop of Lieber's nano device

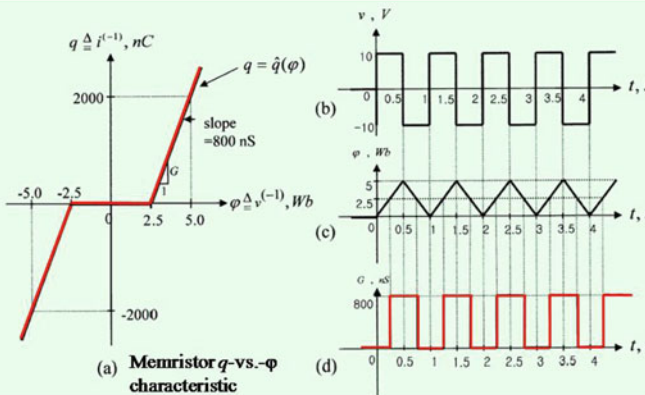


(b) Conductance switches from 0 to 800 nano Siemens

From:

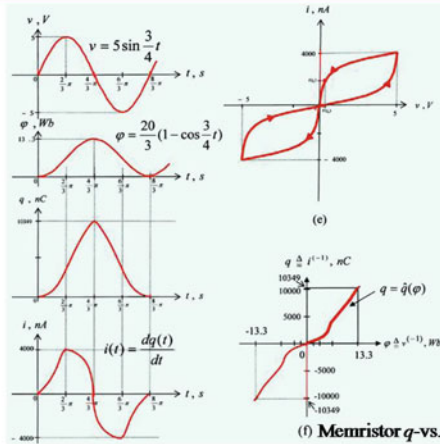
Xiangfeng Duan, Yu Huang, and Charles M. Lieber, "Nonvolatile Memory and Programmable Logic from Molecule-Gated Nanowires," *Nano Letters*, Vol. 2, No. 5, p. 487, 2002

Piecewise-linear Memristor Model of Lieber's Nano Device



The above memristor reproduces almost exactly Lieber's measured conductances.

Smooth Memristor Model of Lieber's Nano Device



The above memristor reproduces approximately Lieber's pinched hysteresis loop in the first quadrant.

Ideal and Generalized Memristors

$$v = M(q)i$$

$$\frac{dq}{dt} = i$$

Ideal Memristor
($x = q = \text{charge}$)

1. Change "charge" q to " n " state variables $\mathbf{x} = (x_1, x_2, \dots, x_n)$ and current i :

$$M(q) \rightarrow M(\mathbf{x}, i)$$

2. Generalize to a nonlinear differential equation:

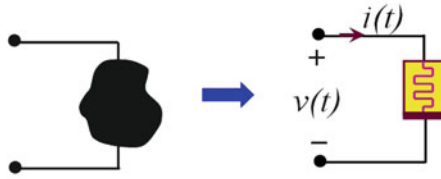
$$i \rightarrow f(\mathbf{x}, i)$$

$$v = M(\mathbf{x}, i)i$$

$$\frac{d\mathbf{x}}{dt} = f(\mathbf{x}, i)$$

Memristor

What is a Memristor ?



1. It has 2 electrical terminals
2. It obeys *Ohm's law*
3. R is **not** a constant:

$$v = R i$$

$$R = g(x_1, x_2, \dots, x_n; i)$$

$$\dot{x}_1 = f_1(x_1, x_2, \dots, x_n; i)$$

$$\dot{x}_2 = f_2(x_1, x_2, \dots, x_n; i)$$

$$\vdots$$

$$\dot{x}_n = f_n(x_1, x_2, \dots, x_n; i)$$

Physical Definition of Memristor

Any 2-terminal device defined by a *state-dependent* Ohm's Law is a *memristor*.

Memristor v - i Pinched Hysteresis Loop Fingerprint

Theorem
The v -vs.- i loci of a memristor can cross the *voltage* and *current* axes only at the origin.

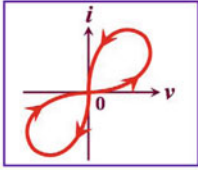
Proof
Assumption:
 $M(q) \triangleq \frac{d\phi(q)}{dq} > 0$

$$\frac{d\phi}{dt} = \frac{d\phi(q)}{dq} \frac{dq}{dt}$$

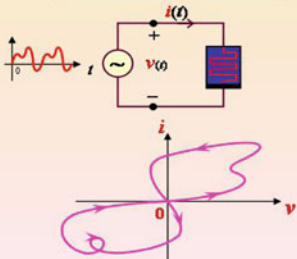
$$\Rightarrow v(t) = \underbrace{M(q)}_{M(q)} i(t)$$

Since $M(q) > 0$,

$$v(t) = 0 \iff i(t) = 0$$



Experimental Definition of Memristor



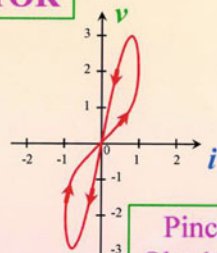
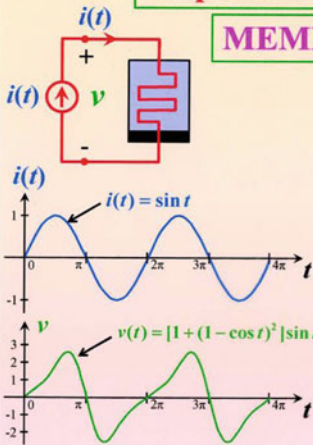
Any *2-terminal* device which exhibits a *pinched hysteresis loop* in the *voltage-vs.-current* plane under *any periodic* excitation is called a *memristor*.

Concise Definition of Memristor

A memristor is any *state-dependent linear 2-terminal resistor*.

Experimental Definition

MEMRISTOR



Pinched Ohm's Law

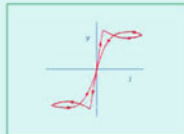
$$v = R(q)i$$

$$\frac{dq}{dt} = i$$

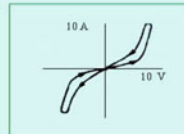
Experimental Test for Memristors

Any 2-terminal device exhibiting the following fingerprint characteristics is a *memristor*:

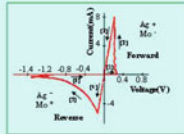
1. The **Lissajoux figure** in the **voltage-current plane** is a **pinched hysteresis loop** when driven by *any* bipolar periodic **voltage $v(t)$** , or **current $i(t)$** , and under *any* initial conditions.
2. The area of each lobe of the **pinched hysteresis loop** shrinks as the frequency ω of the forcing signal increases.
3. As the frequency ω tends to infinity, the **pinched hysteresis loop** degenerates to a straight line through the origin, whose slope depends on the **amplitude** and **shape** of the forcing signal.



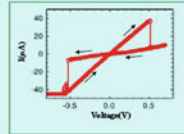
(a) 1947



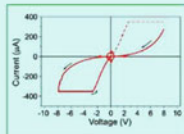
(b) 1968



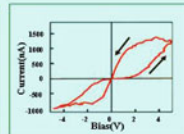
(c) 1976



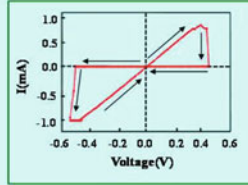
(d) 2000



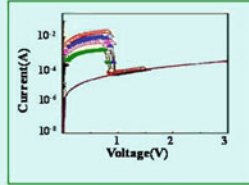
(k) 2001



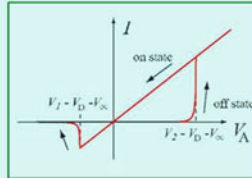
(l) 2002



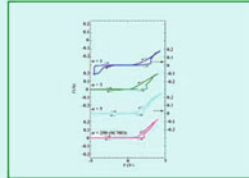
(g) 2003



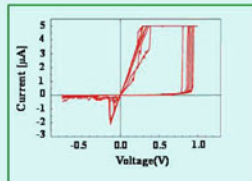
(h) 2004



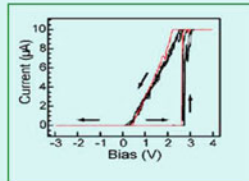
(i) 2005



(j) 2006



(k) 2007



(l) 2008

*If it's pinched,
It's a memristor*

Resistance Switching
implies
Memristor

RRAM
and
Phase Change
Memory
are
Memristors

commentary


Two centuries of memristors

Themistoklis Prodromakis, Christofor Toumazou and Leon Chua


Memristors are dynamic electronic devices whose nanoscale realization has led to considerable research interest. However, their experimental history goes back two centuries.

NATURE MATERIALS | VOL 11 | JUNE 2012 | www.nature.com/naturematerials

The Oldest Known Memristor Device (1801)



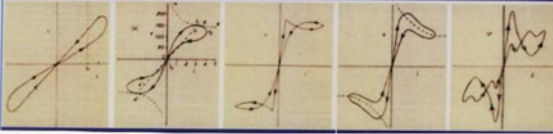
Sir Humphry Davy



ELEMENTS.
OF
CHEMICAL PHILOSOPHY.
BY
SIR HUMPHRY DAVY, LL. D.
PHILADELPHIA.
PUBLISHED BY AN ANDRÉ DUFF BRIDGE,
AND MERCHANT OF IMPORTATION,
107 N. 3rd ST. PHILA.
1801.

The Oldest Known Memristor

Figure 1. Dynamic characteristics of memristors. From left to right: tungsten filament, high-pressure mercury-vapour lamp, low-pressure mercury tube, discharge tube and sodium tube. Image reproduced from ref. 10.

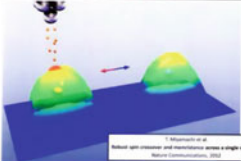


Breaking News!

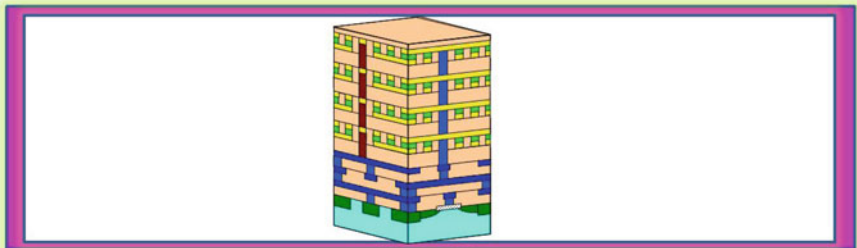
A memristor
has been built
with only
one molecule.

July 3, 2012


Nature: Molecule Changes Magnetism and Conductance



© Nature 2012.
Nature Communications, 3, 1022 (2012)



The entire *library of congress* can be stored in a multi-layer 1p memristor chip



Library of Congress

21,218,408 books
10 terabytes (10¹²)



Brian Josephson
 1973 Nobel Prize for Physics for discovering
 the Josephson junction device and circuit model.

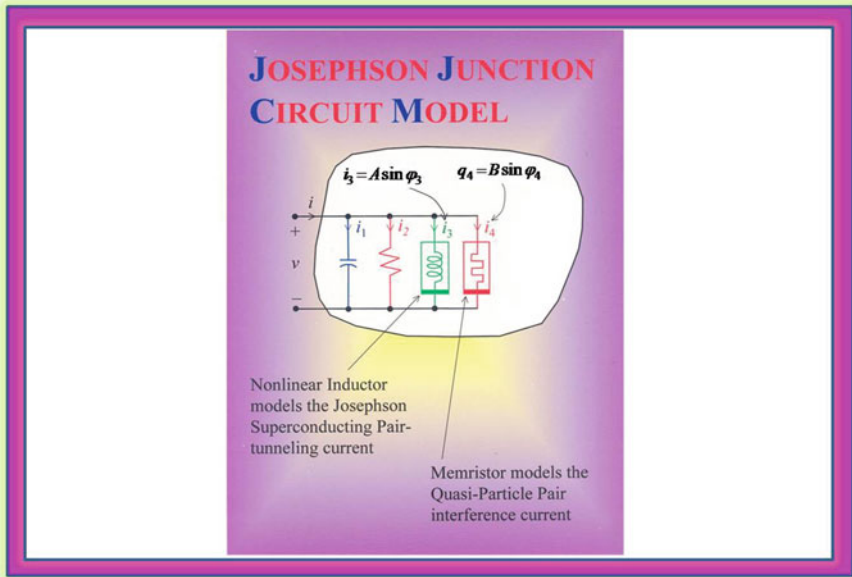
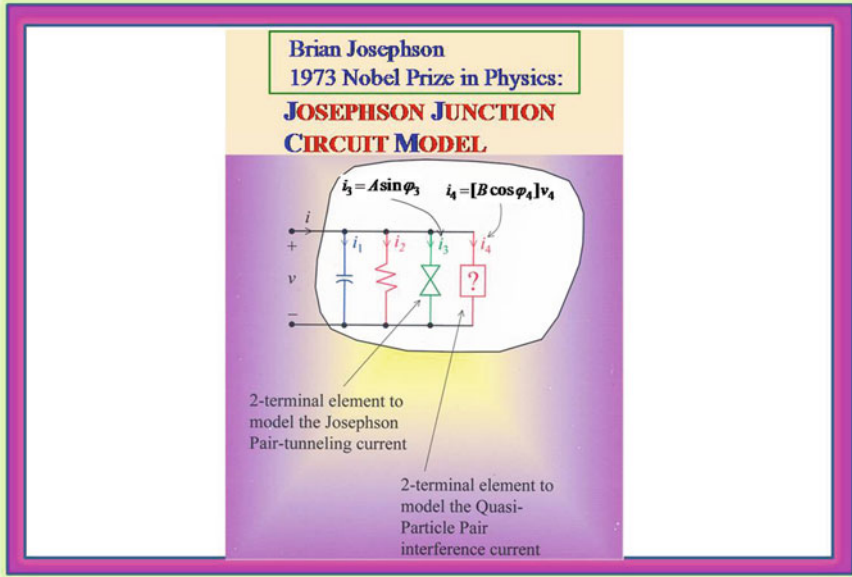
Modeling Quasi-Particle Pair Interference Current in Josephson Junctions

In the quantum-mechanical analysis of the Josephson junction, a small contribution to the device current is derived by Josephson to be given by

$$i = M (\cos \varphi) v$$

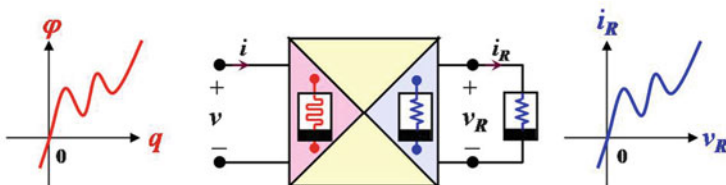
where M is a constant which depends on the device parameters. This equation, which is usually negligible, represents a **memristor** defined by

$$q = M \sin \varphi$$



How to Make a Memristor ?

A memristor with *any* ϕ -vs.- q characteristic can be synthesized via a **mutator** and a nonlinear **resistor**.



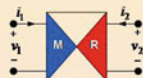
Resistor-to-Memristor Mutator

Resistor-to-Memristor Mutator

Constitutive Relation

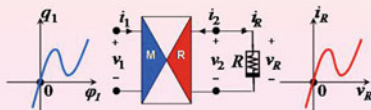
$$\begin{aligned} v_1 &= \frac{dv_2}{dt} \\ i_1 &= -\frac{di_2}{dt} \end{aligned}$$

Symbol



Theorem

A Resistor-to-Memristor *Mutator* transforms any nonlinear *resistor R* connected across port 2 into a *memristor* when viewed across port 1, with the same constitutive relation obtained by changing the variables (v_2, i_2) of the resistor into (ϕ, q) .



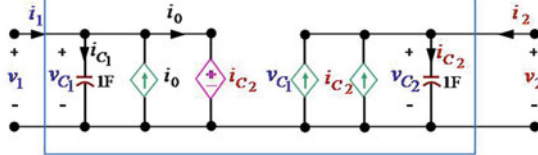
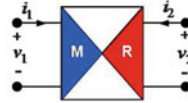
Building a Resistor-to-Memristor Mutator

Constitutive Relation

$$v_1 = \frac{dv_2}{dt}$$

$$i_1 = -\frac{di_2}{dt}$$

Symbol



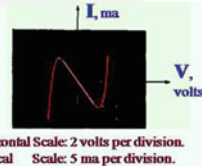
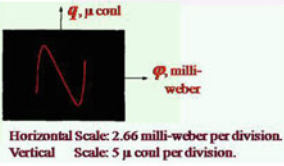
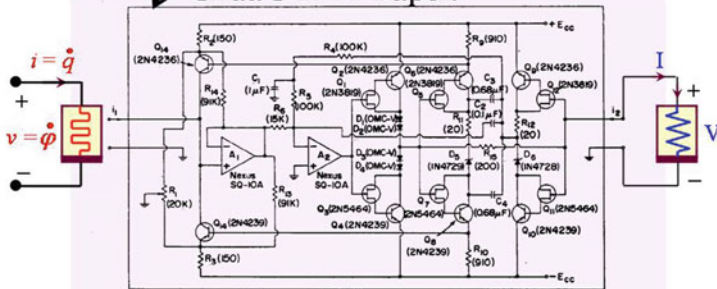
Proof:

$$i_{C2} = \frac{dv_{C2}}{dt} = \frac{dv_2}{dt} \quad i_{C1} = i_1 \Rightarrow v_1 = v_{C1} = \int i_1(t) dt$$

$$\Rightarrow v_1 = i_{C2} = \frac{dv_2}{dt} \quad i_2 = -v_{C1} = -\int i_1(t) dt$$

$$\Rightarrow i_1 = -\frac{di_2}{dt}$$

This circuit is copied from page 509 of
√ Chua's 1971 Paper.



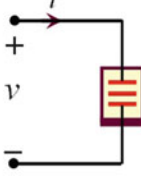
What's Next ?

Memristors are not Lossless

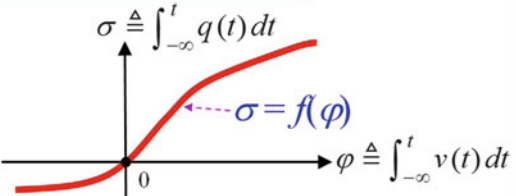
As *non-volatile* memories,
memristors do not consume power
when idle.

It does *dissipate a little heat*
whenever it is being
“*written*” or “*read*”

Memory Capacitor



$\sigma \triangleq \int_{-\infty}^t q(t) dt$



$\phi \triangleq \int_{-\infty}^t v(t) dt$

$\frac{d\sigma}{dt} = \frac{df(\phi)}{d\phi} = \frac{df(\phi)}{d\phi} \frac{d\phi}{dt}$

$\underbrace{\frac{d\sigma}{dt}}_q = \underbrace{\frac{df(\phi)}{d\phi}}_{C(\phi)} \underbrace{\frac{d\phi}{dt}}_v$

Constitutive Relation

$\sigma = f(\phi) \implies q = C(\phi) v$

where

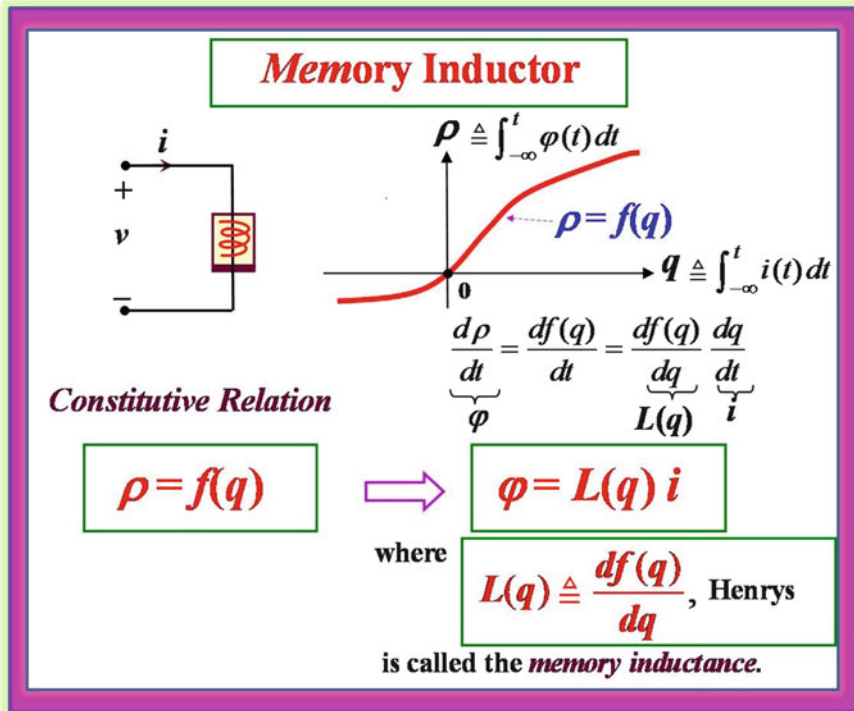
$C(\phi) \triangleq \frac{df(\phi)}{d\phi}$, Farads

is called the *memory capacitance*.

Theorem

The *memory capacitor*

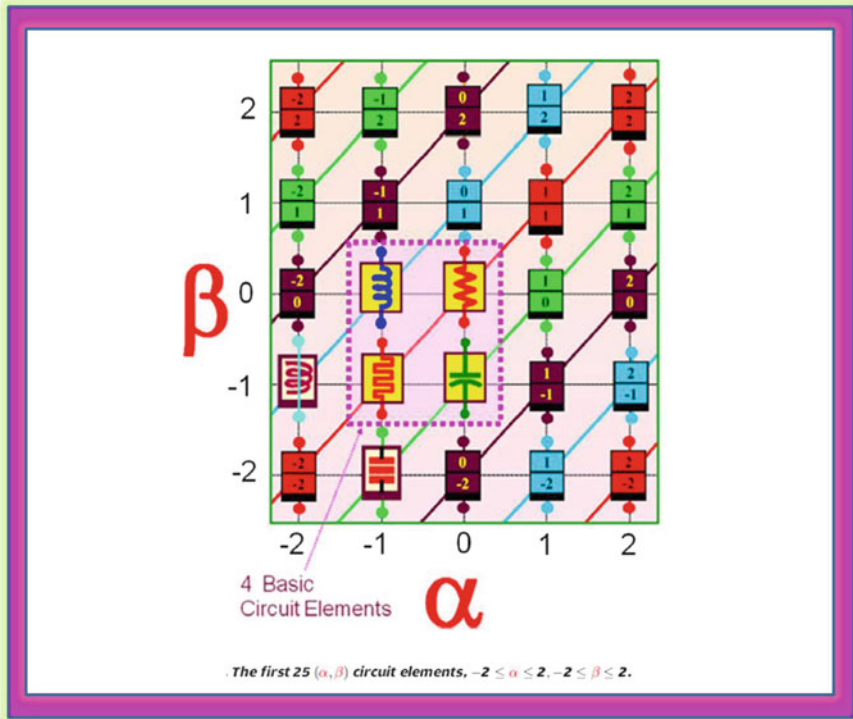
is a *lossless* element



Theorem

The *memory inductor*

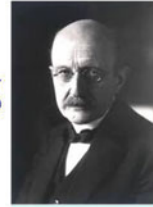
is a *lossless* element



Frequently Asked Question

Why did it take so long for your *memristor* theory to be validated ?

New Scientific ideas do not succeed by converting contemporary scientists, but rather by their opponents' dying off



Max Planck

Max Planck

New theories have four stages of acceptances:

- I. this is worthless nonsense;
- II. this is interesting, but perverse;
- III. this is true, but quite unimportant;
- IV. I always said so.



J. B. S. Haldane

J. B. S. Haldane