Chapter 13
Memristor for Neuromorphic Applications: Models and Circuit Implementations

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13.1 Introduction

The current-controlled *ideal memristor* is a passive bipole linking charge $q(t)$ and flux $\varphi(t)$ through a nonlinear relation, i.e. $\varphi(t) = \varphi(q(t))$. From application of Faraday's Law and of the chain rule it follows that voltage $v(t)$ depends upon current $i(t)$ through

$$v(t) = \frac{d\varphi(t)}{dt} = M(q(t))\, i(t), \tag{13.1}$$

where $M(q) = \frac{d\varphi(q)}{dq}$ is the memristance (i.e. memory-resistance) of the bipole. Since $q(t) = \int_{-\infty}^{t} i(t')dt'$, then $M(q) = M(\int_{-\infty}^{t} i(t')dt')$. In other words the resistance of the memristor depends upon the time history of the current flowed through it. This explains the memory capability of the memristor, theoretically envisioned by Chua in 1971 [1] and later classified by Chua and Kang in 1976 as the simplest element from a large class of nonlinear dynamical systems endowed with memristance, the so-called memristive systems [2].

In [2] a memristive system (or memristor system[1]) is a nonlinear dynamical circuit element defined by the following differential-algebraic system of equations:

[1] In the following memristive systems are referred to as memristor systems, whereas the term ideal memristor is used for systems described by (13.1).

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R. Tetzlaff (ed.), *Memristors and Memristive Systems*,
DOI 10.1007/978-1-4614-9068-5_13,

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{f}(\mathbf{x}(t), u(t)), \tag{13.2}$$

$$y(t) = \mathbf{g}(\mathbf{x}(t), u(t))u(t), \tag{13.3}$$

where[2] $\mathbf{x} \in \mathbb{R}^n$ is the state, $u \in \mathbb{R}$ refers to the input, $y \in \mathbb{R}$ describes the output, $\mathbf{f}(\mathbf{x}, u) : \mathbb{R}^n \times \mathbb{R} \to \mathbb{R}^n$ stands for the *state evolution function*, while $\mathbf{g}(\mathbf{x}, u) : \mathbb{R}^n \times \mathbb{R} \to \mathbb{R}$ denotes the *memductance* (*memristance*) if input u is in voltage (current) form.

Since 2008, when its existence at the nano-scale was certified at Hewlett-Packard (HP) Labs [3], the memristor has attracted a strong interest from both industry and academia for its central role in the setup of novel integrated circuit (IC) architectures, especially in the design of high-density nonvolatile memories [4], programmable analog circuitry [5], neuromorphic systems [6], and logic gates [7,8].

The development of innovative strategies for the design of memristor-based electronic systems requires the availability of mathematical models [3, 9–14, to name but a few] for the memristor nano-structures under study. A good model should be as general as possible, i.e. it should be able to capture the memristor dynamics of a large number of nano-films. In this respect the Boundary Condition Memristor (BCM) model, recently introduced in [12], was developed so as to meet this generality requirement. In fact the distinctive feature of the BCM model is the adaptability of the nano-device behavior at boundaries. In particular, the model makes use of adaptable[3] threshold voltages v_{th0} and v_{th1}, respectively, defining[4] the magnitude of the limit value the input voltage (i.e., the voltage drop across the memristance) needs to cross after its negative-to-positive and positive-to-negative sign reversal before the memristor state may be released from its lower and upper bound. It is straightforward to establish an optimization procedure, which, on the basis of observed data, sets the most suitable values for the threshold voltages, i.e. those values, let us identify them as v^*_{th0} and v^*_{th1}, minimizing the mean squared error between observed and modeled data. This enables the BCM model to stand out over other models available in the literature for the larger number of detectable dynamics, despite the extreme simplicity of the window function embedded into the state equation (when the state variable lies within its two bounds its time evolution is governed by the basic linear dopant drift model [3]). It is noteworthy that the class of detectable dynamics include not only all the behaviors observed in the HP memristor [3], but also phenomena exhibited by various other nano-structures

[2]For the sake of brevity the explicit time dependency is dropped where it is not strictly necessary.

[3]Note that by defining a time evolution rule for the threshold voltages, it was recently demonstrated [15] that an adaptable threshold voltage-based version of the memristor model from [6] may explain the Suppression Principle [16] of the Spike-Timing-Dependent-Plasticity (STDP) Rule [6], which may occur in the case of triplet spikes.

[4]Throughout the paper, unless stated otherwise and without loss of generality, we assume that the doped layer is spatially located to the left of the un-doped layer along the horizontal extension of the nano-film [12], and in this case we assign a value of $+1$ to the memristor polarity coefficient η (see (13.6)).

where memristor behavior arises from distinct physical mechanisms [17–20]. In order to enable the BCM model to support various neural learning rules, we recently developed a generalized version [21], in which the activation threshold property characterizing the boundary behavior in the original BCM model [12] is extended to the whole admissible range of the state variable, thus allowing the modeling of the degree of non-volatility of the nano-device.

Another necessary requirement for the investigation of potential applications of memristor devices is the implementation of the mathematical models into a software package for computer-aided integrated circuit design. In this chapter we shall first present the PSpice [22] implementation of the generalized BCM model. In the PSpice realization the voltage drop across a linear capacitor models the memristor state. Further the memristance is determined by the series combination of a linear resistance and a nonlinear resistance depending upon the capacitor voltage. The current through the memristance is first nonlinearly filtered so as to model the degree of non-volatility of the nano-structure. In other words, this current is multiplied by a nonlinear function which is responsible for the activation of the state dynamics as the control voltage crosses a tunable positive (negative) threshold v_{t0} $(-v_{t1})$ in its ascent (descent). The filtered current drives a current source, which, under positive (negative) input voltage polarity, charges (discharges) the capacitor. For each of the two lower and upper bounds of the memristor state, flexible boundary conditions are implemented in PSpice by means of a reference voltage source with value equal to that bound and by a pair of voltage-controlled voltage switches, one controlled by the voltage across the capacitor and responsible for clipping the memristor state at the lower (upper) limit under negative (positive) input voltage, the other calling for the release of the state from its lower (upper) bound as the input voltage cuts through yet another tunable positive (negative) threshold v_{th0} $(-v_{th1})$ in its ascent (descent).

The PSpice circuit of the generalized BCM model may be used to model dynamics typical of biological synapses. It is in fact capable to support various rules governing the way neurons learn from each other. As an example, this chapter demonstrates how the PSpice circuit favors associative learning based on the Hebbian rule, one of the most important adaptation rules in neural learning [23].

The last part of this chapter proposes a novel class of memristor emulators. Each element from the class is an electronic circuit comprising standard passive electrical components from circuit theory, namely static nonlinear devices such as diodes and linear dynamical elements such as resistors, inductors, and capacitors.

The structure of the manuscript is organized as follows. Section 13.2 reviews the most noteworthy memristor circuit models available in the literature. Section 13.3 briefly reviews the generalized BCM model and describes its PSpice implementation. Section 13.4 illustrates the ability of the PSpice circuit model to support the Hebbian neural learning rule. Section 13.5 introduces a novel class of memristor emulators. Finally Sect. 13.6 outlines the conclusions.

13.2 Brief Review of Memristor Models

Various memristor circuit models have been proposed in the literature. A large number of models assume that the control waveform is in current form (the voltage v-current i relationship is expressed by (13.1)), views the memristance as the series between two variable resistances, associated with the insulating and conductive layers of the nano-film, and sets the width w of the conductive layer, normalized with respect to the entire length D of the device, as the state $x = \frac{w}{D} \in [0, 1]$ of the system. The linear drift model from Williams [3], where the time derivative of the state is proportional to the input waveform in current form, is valid under the assumption that the state is confined within its two bounds, since it does not take into account the boundary behavior.

In the nonlinear drift models from [9, 10] and [24] the rate of change of the state is proportional to the product between the input waveform in current form and a window function accounting for nonlinear dynamical behavior and imposing suitable boundary conditions.

In Joglekar's model [9] the window function is defined as $f_J(x) = 1 - (2x - 1)^{2p}$ ($p \in \mathbb{Z}_+$). Such window describes the suppression of dopant drift close to the extremities, but is not vertically scalable (i.e. its maximum value may not be up- or down-shifted) and introduces the so-called terminal-state problem [24], since if the state is at either of its two bounds it may not leave it for any subsequent time instant. Note that for $p = 1$ Joglekar's window is a scaled (by a factor of 4) version of yet another window previously derived by Strukov in [3], i.e. $f_S(x) = x(1 - x)$. Benderli [25] presented a circuit realization of Strukov's model [3], where the use of comparators and logic gates allowed the emulation of the state clipping at or release from either bound.

In Biolek's model the window function depends on both state x and input current i, being defined as $f_B(x, i) = 1 - (x - stp(-i))^{2p}$, where $stp(x) = 1$ for $x \geq 0$ and 0 otherwise ($p \in \mathbb{Z}_+$). Such window resolves the "terminal-state problem," but has limited scalability (in particular, its maximum value may not exceed $+1$ [24]). PSpice implementations of Joglekar's and Biolek's models are reported in [10].

In the versatile model proposed by Prodomakis [24] the window function $f_P(x) = j(1 - ((x - 0.5)^2 - 0.75)^p)$ has two control parameters j and p lying in $\mathbb{R}_+$ and is vertically scalable, i.e. $0 \leq max\{f_P(x)\} \gtrless 1$. A PSpice version of such model may be easily derived by modifying the PSpice .circ [22] file available in [10].

Another model endowed with a PSpice circuit implementation was developed by Cserey [26]. In this model the state evolution function in Strukov's model [3] was augmented with an additive state-dependent linear term to resolve the "terminal-state problem."

One of the finest circuit emulators of memristor behavior is credited to Shin and Kang [11], which proposed a general model where the control waveform may be in either current or voltage form and the state is defined as the memristance. Their model, from which the charge-flux relationship of the memristor under modeling may be easily extracted, may be suitably tuned through the introduction of a window function depending on the memristor charge.

Kavehei [27] proposed a memristor model based upon the specification of a piecewise-linear charge q-flux φ relationship. In such model the state and output equations are not specified. Its PSpice implementation is based on Chua's [1] first circuit realization of a memristor through a type-1 memristor-resistor mutator.

An interesting model was presented in [28] to explain the memristor behavior of nanoparticle assemblies.

The nonlinear dependence of the time derivative of the state on the input signal is taken into account in Lehtonen's model [29], inspired by the experimental work from [30], where the current is related to the voltage by means of a rectifying exponential function in the off state (as in a diode) and of a sinh function in the on state (typical of electron tunneling). This model, where the control waveform is in voltage form, was implemented in PSpice to describe the neighborhood connections among cellular neural networks (CNNs) [31, 32].

An even more nonlinear function of the input governs the state equation in the voltage-controlled model from Poikonen [33], which studied the transition between non-programming and programming phases in memristor devices.

In the memristor emulator circuit from [34], used as basic building block of a 4-memristor bridge synapse for neuromorphic applications, the memristance, modeled by the input impedance of an active circuit, is made proportional to the time integral of the memristor current by constraining the voltage at one of the input terminals of an operational amplifier to be the analogue multiplication between the voltage across a resistor, proportional to the memristor current, and the voltage across a capacitor, proportional to the time integral of the memristor current.

In [35] Strukov and Williams demonstrated the exponential relationship between drift velocity and local electric field. Since this discovery a number of models have been introduced to support threshold-activated state dynamics.

Among them, one which merits mention, is the physics-based Pickett's model from [13], in which the dependency of the rate of change of the state on the current-form input is strongly nonlinear. In such model the memristor is seen as the series between a low resistance associated with the conductive layer of the nano-film and Simmons' electron tunneling barrier [36], whose width is chosen as the system state. A PSpice version of Pickett's model was presented in [37].

More recently Kvatinski developed a simplified version of the Pickett's model [13] and named it as ThrEshold Adaptive Memristor (TEAM) model [14]. In such model for input current magnitude below a certain adaptable threshold no state change occurs, otherwise the state evolution rule may be tuned to the memristor element under modeling through specification of an appropriate set of control parameters and of suitable window and memristance functions. The PSpice architecture of the TEAM model is similar to the one originally presented in [11].

Another activation-type state model, where the state variable expresses the memristance and the control signal is in voltage form, embedded in the PSpice software program [38], enabled to capture the adaptive behavior of a unicellular organism named amoeba through a simple memristor-based oscillator [39].

Another interesting model with threshold-activated state dynamics was proposed in [40] to explain Spike-Timing-Dependent-Plasticity (STDP) in neural synapses.

Most of these PSpice models have been classified in [41]. Another insightful discussion on the models available in the literature was recently published in [42], where a novel model inspired from Simmons' electron tunneling theory [36], endowed with programming threshold capability and PSpice circuit implementation, was also proposed.

The Boundary Condition Memristor (BCM) model is a simple yet accurate boundary condition-based mathematical model for memristor nano-structures made up of two layers with different conductivity levels, whose longitudinal extensions depend on the time history of the input. In comparison with the classical BCM model [12], the generalized version [21] is augmented with programming threshold capability [42], i.e. with tunable nonvolatile behavior.

Recently, in [43], assuming Pickett's model [13] as reference for comparison, various memristor models, including Biolek's, the TEAM and the BCM models, were first compared on the basis of the ability to reproduce (after an optimization process) the dynamics of the reference model in a particular simulation scenario, and secondly employed in a couple of memristor-based circuits to investigate the variance in the nonlinear dynamical behaviors they give rise to. The latter study revealed the model-dependency of the dynamics of memristor-based circuits, and thus raised a warning against a blind faith in the memristor models and pointed out the necessity to develop a universal mathematical model for exploring the full potential of the memristor and unfolding its unique properties.

Section 13.3 describes the recently proposed generalized BCM model and its PSpice-based circuit [21] (the PSpice emulator of the classical BCM model is reported in [44]).

13.3 Generalized BCM model and Its Circuit Implementation

Let R_{on} and R_{off} stand for the on and off resistances of a memristor nano-film. The memristor state variable x is chosen as the length $w(t)$ of the conductive layer of the nano-film normalized with respect to the entire longitudinal extension D of the nano-film (i.e. $x = \frac{w(t)}{D} \in [0,1]$). Denoting memristor current and voltage as i and v, respectively, the state-dependent input–output algebraic relationship of the generalized BCM model is expressed by

$$i(t) = W(x(t))\, v(t), \tag{13.4}$$

where $W(x(t))$ describes the state-dependent memductance, expressed by

$$W(x(t)) = \frac{G_{on} G_{off}}{G_{on} - \Delta G x(t)}, \tag{13.5}$$

with $G_{on} = R_{on}^{-1}$, $G_{off} = R_{off}^{-1}$, while $\Delta G = G_{on} - G_{off}$.

The state equation of the generalized BCM model is defined as

$$\frac{dx(t)}{dt} = \eta\, k\, W(x(t))\, v(t)\, f\,(x(t), \eta\, v(t), v_{th0}, v_{th1}, v_{t1}, v_{t2}, a, b)\,, \tag{13.6}$$

where $k \in \mathbb{R}$ is a constant depending on physical properties of the memristor (its dimensions are C^{-1}), $\eta \in \{-1, +1\}$ is a coefficient denoting the polarity of the nano-device, while $f\,(x(t), \eta\, v(t), v_{th0}, v_{th1}, a, b) \in \{0, a, b\}$, a switching window function defining not only the boundary behavior but also the degree of non-volatility [42], is expressed as

$$f\,(x, \eta\, v, v_{th0}, v_{th1}, v_{t0}, v_{t1}, a, b) = \begin{cases} b \texttt{ if } C_1 \texttt{ or } C_2 \texttt{ holds}, \\ 0 \texttt{ if } C_3 \texttt{ or } C_4 \texttt{ holds}, \\ a \texttt{ if } C_5 \texttt{ holds}, \end{cases} \tag{13.7}$$

where tunable conditions C_n ($n = 1, 2, 3, 4, 5$) are mathematically described by

$$C_1 = \{\ (x(t) \in (0,1) \texttt{ and } ((\eta\, v(t) > v_{t0}) \texttt{ or } (\eta\, v(t) < -v_{t1})))\}, \tag{13.8}$$

$$C_2 = \{\ (x(t) = 0 \texttt{ and } \eta\, v(t) > v_{th0}) \texttt{ or } (x(t) = 1 \texttt{ and } \eta\, v(t) < -v_{th1})\}, \tag{13.9}$$

$$C_3 = \{\ x(t) = 0 \texttt{ and } \eta\, v(t) \leq v_{th0}\}, \tag{13.10}$$

$$C_4 = \{\ x(t) = 1 \texttt{ and } \eta\, v(t) \geq -v_{th1}\}, \tag{13.11}$$

$$C_5 = \{\ (x(t) = \bar{x} \in (0,1) \texttt{ and } ((\eta\, v(t) \leq v_{t0}) \texttt{ and } (\eta\, v(t) \geq -v_{t1})))\}, \tag{13.12}$$

where $v_{th0} \in \mathbb{R}_+$, $v_{th1} \in \mathbb{R}_+$ represent the input thresholds at boundaries, $v_{t0} \in \mathbb{R}_+$, $v_{t1} \in \mathbb{R}_+$ define the programmability thresholds, ($v_{t0} \leq v_{th0}$ and $v_{t1} \leq v_{th1}$), while a and b are constants modulating the degree of non-volatility of the memristor ($b \in \mathbb{R}_+$, $a \in \mathbb{R}_{0,+}$, $a < b$).

The PSpice implementation of the generalized BCM model is depicted in Fig. 13.1. The source code is reported in Table 13.1.

In the circuit of Fig. 13.1 voltages at nodes y and z, the two terminals of the bipole, are, respectively, denoted as v_y and v_z, while $v = v_y - v_z$ and i, respectively, stand for voltage across and current through the memristor. The architecture of this circuit realization takes inspiration from the design of Batas and Fiedler [45], which, however, was lacking the adaptability of the boundary behavior and the tunability of the degree of non-volatility.

The memristor state x is modeled by the voltage v_θ across capacitance C_x. The series between linear resistor R_{off} and nonlinear voltage-controlled resistor $R(v_\theta) = -\Delta R v_\theta$, where $\Delta R = R_{off} - R_{on}$, implements the input–output equation (13.4).

If the value of window function (13.7) were unitary at all times, as in the original model from Williams [3], state equation (13.6) would be simply implemented by letting memristor current i flow through linear capacitor C_x (in any case a tiny conductance g is placed in parallel to the capacitor so as to prevent node z from floating). However, $f\,(v_\theta(t), \eta\, v(t), v_{th0}, v_{th1}, a, b) \in \{0, a, b\}$ and its behavior is regulated by conditions C_1 and C_5, governing the degree of non-volatility, and by conditions C_2-C_4, determining the boundary behavior.

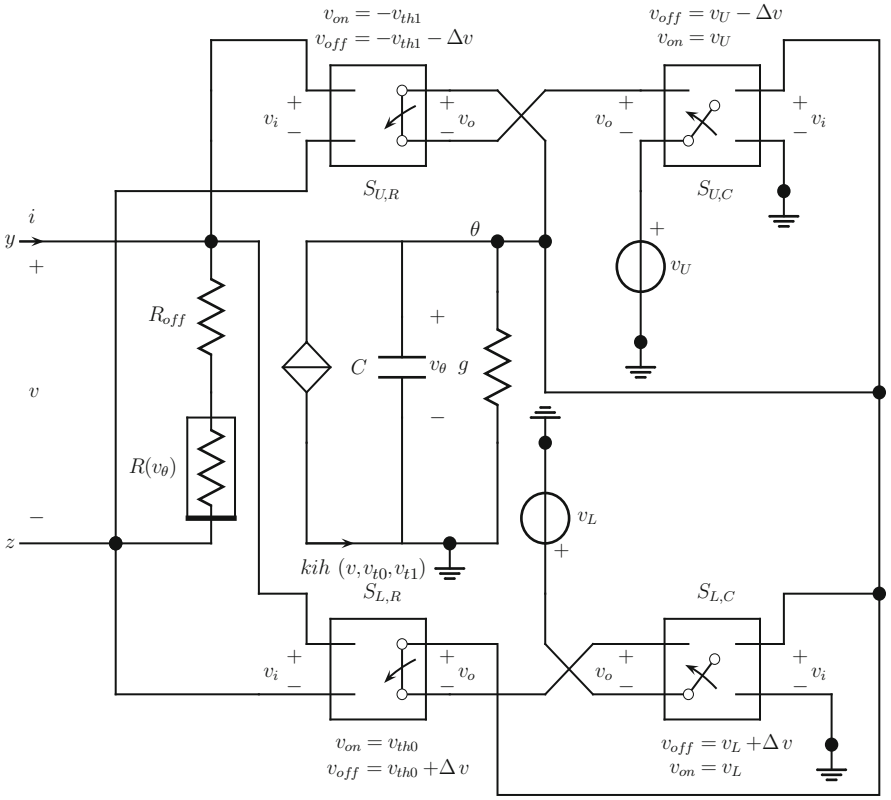

Fig. 13.1 PSpice implementation of the generalized BCM model. Note that Δv denotes for each switch the width of the transition region between on and off states

Conditions (13.8) and (13.12) are implemented by nonlinearly filtering memristor current i before letting it flow through capacitor C_x. This filtering consists of performing the multiplication between a k-scaled version of memristor current i and a nonlinear function $h(v, v_{t0}, v_{t1}, a, b)$, which, under $x \in (0, 1)$, is responsible for the modulation of the evolution rate of the state. In particular, under positive (negative) input larger (smaller) than a suitable threshold v_{t0} $(-v_{t1})$ the right-hand-side of state equation (13.6) is multiplied by a factor (b) larger than the factor (a) by which it is multiplied in the sub-threshold input case. Nonlinear function $h(v, v_{t0}, v_{t1}, a, b)$ is mathematically expressed by

$$h(v, v_{t0}, v_{t1}) = b + \frac{a-b}{2}(sign(v + v_{t1}) - sign(v - v_{t0})), \tag{13.13}$$

Note that the multiplication between current $k\,i$ and function (13.13) may be easily implemented by letting flow through capacitor C_x one of the currents of two complementary-activated parallel branches. One of these branches is activated

Table 13.1 Netlist of the PSpice implementation of the generalized BCM model in Fig. 13.1

```
* Local parameters:
* Ron, Roff: on and off resistances
* delta_R: difference between Roff and Ron
* x0: initial state
* vth0: activation threshold for x=0
* vth1: activation threshold for x=1
* vt0,vt1: activation thresholds for 0<x<1
* Cx: capacitance value
* k: memristor charge scaling factor
* a, b: constants modulating the degree of non-volatility
* delta_v: width of the transition region of the switches
.SUBCKT BCM_MEMRISTOR 1 2 3
* node 1: node y in Fig. 13.1
* node 2: node z in Fig. 13.1
* node 3: node theta in Fig. 13.1
R1 1 8 {Roff}
Vsense1 8 7 0
E1 7 2 VALUE={{-delta_R}*I(Vsense1)*V(3)}
C1 3 0 {Cx} IC={x0}
R3 3 0 1G
Vsense2 10 0 1
G1 0 3 VALUE={k*Cx*I(Vsense1)*V(10)*h(V(1)-V(2),vt0,vt1,a,b)}
S1 3 9 1 2 SMODRH
S2 9 4 3 0 SMODCH
S3 3 6 1 2 SMODRL
S4 6 5 3 0 SMODCL
V1 5 0 0
Vu 4 0 1
.MODEL SMODRH VSWITCH Roff=1G Von={-vth1} Voff={-vth1-delta_v}
.MODEL SMODCH VSWITCH Roff=1G Voff={1-delta_v} Von={1}
.MODEL SMODRL VSWITCH Roff=1G Von={vth0} Voff={vth0+delta_v}
.MODEL SMODCL VSWITCH Roff=1G Voff=delta_v Von=0
.func h(v,v0,v1,a,b)={b+(a-b)/2*SGN(v+v1)-(a-b)/2*SGN(v-v0)}
.ENDS
```

through a voltage-controlled voltage-switch for $v > v_{t0}$ or $v < -v_{t1}$ and carries a current equal to kbi. The other branch is activated through another voltage-controlled voltage-switch for $v \leq v_{t0}$ and $v \geq -v_{t1}$ and carries a current equal to kai.

Boundary conditions (13.9)–(13.11) are modeled by two reference voltage sources, i.e. $v_L = 0$ and $v_U = 1$, respectively, denoting the lower and upper limits of capacitor voltage v_θ (hence the use of letter L or U as subscript of symbol v for the reference voltage source), and by two pairs of voltage-controlled voltage switches, one pair for each of the two memristor state bounds $v_\theta = 0V$ and $v_\theta = 1V$ (the first subscript of symbol S for a switch indicates whether it refers to the lower or upper state bound, hence letter L or U is chosen). Within each pair of switches, the clipping switch is controlled by capacitor voltage v_θ, while the release switch is controlled by input voltage v (the second subscript of symbol S for a switch hints at whether it models the exit from or the entrance into condition C_2 expressed by

(13.9), i.e. the clipping or release event, hence letter C or R is chosen). Basically, for each state bound, node θ is connected to a reference voltage source through the series between the output resistances of the corresponding pair of clipping and release switches. With regard to the upper (lower) state bound, the relative clipping switch remains open, i.e. in the off state, as long as the memristor state keeps below the unitary (above the zero) value. In this case, due to the large output resistance of the clipping switch, reference voltage source v_U (v_L) is unable to constrain the voltage at node θ, irrespective of the behavior of the release switch. However, the clipping switch turns into on state in case v_θ approaches its upper (lower) bound in its ascent (descent). When this occurs, the associated release switch is always closed, i.e. in the on state, thus allowing the memristor state to be clipped at the upper (lower) bound. Only with memristor state v_θ clipped to $+1V$ ($0V$), do the dynamics of the release switch become relevant: this switch turns into off state in case the input voltage v goes below (above) a certain adaptable negative (positive) threshold voltage $-v_{th1}$ (v_{th0}), thus enabling the memristor state to be released from the upper (lower) bound.

Note that it is possible to develop a more realistic implementation of the PSpice circuit of Fig. 13.1 by replacing the voltage-controlled voltage switches with suitable combinations of Complementary-Metal-Oxide-Semiconductor (CMOS) transistors.

13.4 Case Study: Neuromorphic Applications

This section uses the PSpice circuit of the generalized BCM model to model dynamics typical of biological neural networks. One of the most natural ways in which neurons strengthen their synaptic connections is by sending signals to each other at the same time. This primitive form of neural learning is named Hebbian rule [23]. In order to demonstrate that the circuit of Fig. 13.1 does indeed favor Hebbian-based associative learning, we set up a transient simulation (with time step equal to $0.1\,ms$, initial and final time, respectively, fixed to $0\,s$ and $1.4\,s$) in which we excite nodes y and z with pulses of magnitude, let us call it v_p, equal to $-1V$ and $+1V$, respectively, width, let us name it Δt_p, of value $10\,ms$, rise and fall time $1\,ms$ and period $10\,s$ (i.e. larger than the simulation final time). The time delay of the pulse exciting node y (i.e. the post-synaptic signal), let us name it $t_{d,pos}$, was swept in steps of $0.1\,ms$ from $0.975\,s$ to $1.025\,s$, while that of the pulse exciting node z (i.e. the pre-synaptic signal), let us name it $t_{d,pre}$, was chosen as $1\,s$.

The memristor under modeling is a nano-structure of the kind discussed in Sect. 13.3, therefore $k = \frac{\mu R_{on}}{D^2}$. The BCM parameters were specified as follows: $R_{on} = 526.3158\,\Omega$, $R_{off} = 18182\,\Omega$, $v_\theta(0) = 1V$, $D = 10\,nm$, $\mu = 1e-10^{-14}\,m^2\,V^{-1}\,s^{-1}$ (therefore $k = 52631.58\,C^{-1}$), and $C_x = 50\,\mu F$. The activation threshold voltages at the boundaries (used in conditions (13.9–13.11)) and those within the boundaries (used in conditions (13.8) and (13.12)) are set to $v_{th0} = v_{th1} =$

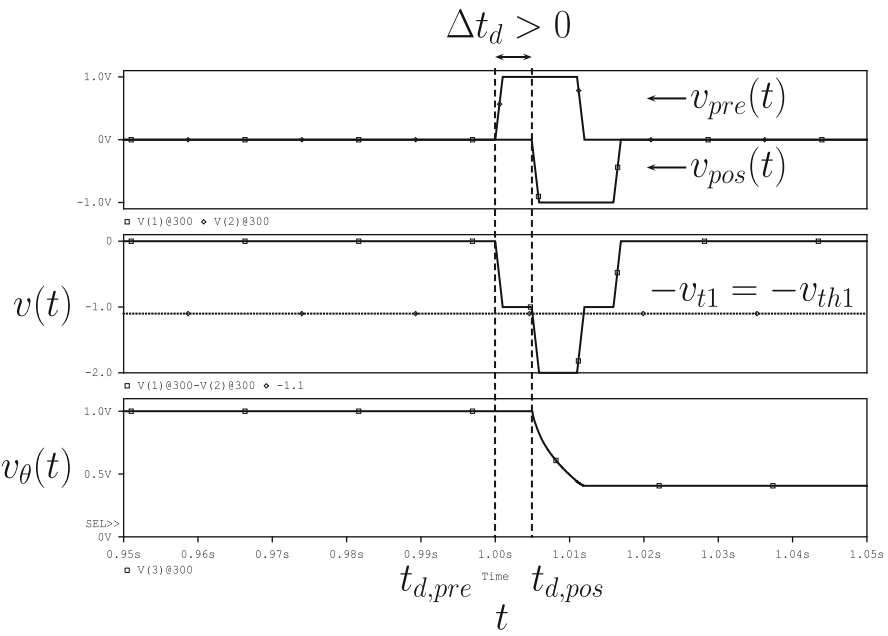

Fig. 13.2 Demonstration of Hebbian-based associative learning under partial temporal overlap between pre- and post-synaptic signals ($\Delta t_d = 0.0049\,s$). *Top plot*: Pre- and post-synaptic pulses. *Middle plot*: Memristor voltage (negative activation thresholds are shown with *dotted lines*). *Bottom plot*: Memristor state

$1.1\,V$ and to $v_{t0} = v_{t1} = 1.1\,V$, respectively. The parameters modulating the degree of non-volatility are set to $a = 0$ and $b = 5$. The width of the transition region of the switches is set to $\Delta v = 0.1\,V$.

Figure 13.2 shows for $t_{d,pos} = 1.0049\,s$ the pulse waveforms at nodes y and z, i.e. $v_y = v_{pos}$ and $v_z = v_{pre}$, the voltage across the memristor, i.e. $v = v_y - v_z$, and the memristor state, modeled by capacitor voltage v_θ in the PSpice circuit of Fig. 13.1. In this case the post- and pre-synaptic pulses overlap in time. The difference between the time delays of such pulses, defined as $\Delta t_d = t_{d,pos} - t_{d,pre}$, is $0.0049\,s$. Only within the overlapping time window is the memristor voltage below the negative activation threshold referring to upper boundary $v_\theta = 1V$, i.e. $-v_{th1}$ (and, since $v_{th1} \geq v_{t1}$, also below the negative activation threshold within the boundaries, i.e. $-v_{t1}$) and, as a result, does the memristor state decrease from its initial unitary value. As Fig. 13.3 demonstrates, the change in memristor state $\Delta v_{theta} = v_{theta} - v_{theta}(0)$ is more significant as the overlapping time window gets larger, i.e. as the magnitude of Δt_d gets smaller. The maximum of the absolute value of Δv_{theta} occurs in fact when the two pulses completely overlap in time, i.e. when $t_{pos} = 1\,s$, implying $\Delta t_d = 0\,s$.

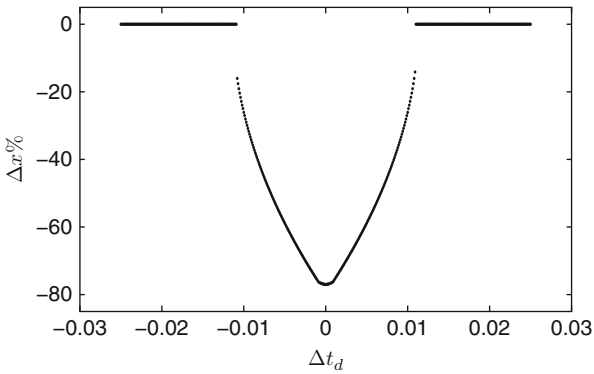

Fig. 13.3 Change in memristor state (recall that $x = v_\theta$, therefore $\Delta x = x - x(0) = v_\theta - v_\theta(0) = \Delta v_\theta$) versus difference of time delays of post- and pre-synaptic signals. The more simultaneous are the pulses, the more pronounced is the change in synaptic strength

13.5 A Novel Class of Passive Memristor Circuits

This section shall introduce a novel class of memristor systems. Each element from the class is an electrical circuit employing only purely passive components from circuit theory (diodes and linear capacitors, inductors and resistors).

Each of the circuits from the class to be presented shall be characterized by a system of differential-algebraic equations of the kind given in (13.2)–(13.3). Section 13.5.1 is devoted to the presentation of the core block of each element from the novel class of memristor systems, i.e. *a switching two-port based upon the Graëtz diode bridge*.

13.5.1 The Graëtz Diode Bridge

Let us consider the full-wave rectifier shown in Fig. 13.4. It is a two-port where v_i and i_i, respectively, denote input voltage and current, while v_o and i_o, respectively, refer to output voltage and current.

The voltage across and the current through diode D_j are, respectively, expressed as v_j and i_j, where $j = \{1,2,3,4\}$. Let us identify the constraints upon voltages and currents of the two-port. These constraints shall play a key role in the emergence of memristor behavior in the circuits from the class to be presented. Application of Kirchhoff's Current Law (KCL) to the input and output port, respectively, yields

$$i_i = i_1 - i_4, \tag{13.14}$$

$$i_i = i_3 - i_2, \tag{13.15}$$

$$i_o = i_1 + i_2. \tag{13.16}$$

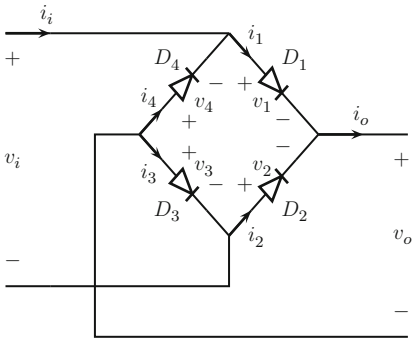

Fig. 13.4 The Graëtz diode bridge

Combining (13.14) and (13.15) yields

$$i_1 + i_2 = i_3 + i_4. \tag{13.17}$$

Applying Kirchhoff's Voltage Law (KVL) to the input and output port gives

$$v_i = v_1 - v_2, \tag{13.18}$$

$$v_i = v_3 - v_4, \tag{13.19}$$

$$v_o = -v_1 - v_4. \tag{13.20}$$

Combination of (13.18)–(13.19) results into

$$v_1 + v_4 = v_2 + v_3. \tag{13.21}$$

Assuming perfectly matched diodes, we express $i_j = i_j(v_j)$, where $j = \{1,2,3,4\}$, as $i_j = I_S\left(\exp\left(v_j n^{-1} V_T^{-1}\right) - 1\right)$, where I_S symbolizes the saturation current, $V_T = KTq^{-1}$ stands for the thermal voltage and n is the emission coefficient, where $K = 1.38 \cdot 10^{-23} JK^{-1}$ is the Boltzmann's constant, T represents the absolute temperature, and $q = 1.6 \cdot 10^{-19} C$ refers to the elementary electronic charge.

Defining $y_j = \exp\left(v_j n^{-1} V_T^{-1}\right)$, (13.17) and (13.21) may be recast as

$$y_1 + y_2 = y_3 + y_4, \tag{13.22}$$

$$y_1 y_4 = y_2 y_3. \tag{13.23}$$

Solving (13.22) for y_1 and inserting the resulting expression into (13.23) gives:

$$y_4^2 + (y_3 - y_2)y_4 - y_2 y_3 = 0,$$

from which, given the sign of y_4, the only acceptable solution is $y_4 = y_2$. Using (13.22), we also have $y_1 = y_3$. Recalling the definition of y_j, we then have $v_4 = v_2$ and $v_1 = v_3$. Note that these two voltage constraints, each involving one pair of

parallel diodes, represent *the key mechanism at the origin of the memristor behavior of the circuits to be proposed*. Recalling the current-voltage relationship for a diode it follows that $i_4 = i_2$ and $i_1 = i_3$.

Equations (13.14) and (13.18) for input port current and voltage and (13.16) and (13.20) for output port current and voltage may thus be recasted as

$$i_i = i_1 - i_2, \tag{13.24}$$

$$v_i = v_1 - v_2, \tag{13.25}$$

$$i_o = i_1 + i_2, \tag{13.26}$$

$$v_o = -v_1 - v_2. \tag{13.27}$$

Equations (13.24)–(13.27) represent the four bridge constraints. Let us present the novel class of memristor electronic systems.

13.5.2 Classification and Properties

Each element from the proposed class is characterized by the following properties:

1. The switching two-port of Sect. 13.5.1 is cascaded with a suitable n^{th}-order dynamical one-port employing n linear dynamical elements (capacitors or inductors) and, not necessarily though, some linear resistor.
2. The input voltage v_i and current i_i of the bridge, taken in any prescribed order, denotes input and output of the memristor element.
3. Either the output voltage v_o or the output current i_o of the bridge denotes one of the n state variables of the memristor element. In the first (latter) case the linear dynamical one-port contains a capacitor (an inductor) with voltage v_o across it (current i_o through it).

The first and third properties constrain the set of one-port topologies which may be chosen as load to the Graëtz diode bridge.

Remark 1. The elements from the novel class, one of which was recently presented in [46], represent the first-ever circuit implementations of memristor systems employing only diodes and linear inductors, capacitors and resistors. This discovery contradicts common expectations according to which memristor behavior may not arise out of elementary circuits comprising solely purely passive components known in circuit theory before the advent of the memristor.

The novel class of memristor electronic systems may be split into two sub-classes, respectively, comprising *voltage-controlled* and *current-controlled* systems, i.e. systems where the input, respectively, is voltage v_i and current i_i (and thus the output, respectively, is i_i and v_i). The first sub-class is dealt with in Sect. 13.5.3, while the reader may derive the second class by duality. Within each of such sub-

classes, two further sub-classes shall be identified, respectively comprising *voltage-state* and *current-state* systems, i.e. systems where one of the states respectively is voltage v_o and current i_o. Such systems shall be presented in Sects. 13.5.3.1 and 13.5.3.2, respectively.

13.5.3 Voltage-Controlled Systems

The input and output to each of these systems, respectively, are v_i and i_i. Let us present the two sub-classes a circuit of this kind may belong to.

13.5.3.1 Voltage-Controlled Voltage-State Systems

For these systems one of the states is v_o. The most appropriate representation of the two-port of Fig. 13.4 for the synthesis of such systems is the current-voltage form. Let us derive it. Solving (13.25)–(13.27) for v_1 and v_2 yields

$$v_1 = \frac{v_i - v_o}{2}, \tag{13.28}$$

$$v_2 = -\frac{v_i + v_o}{2}. \tag{13.29}$$

Recalling the current-voltage relationship for a diode and using (13.28)–(13.29) into (13.24) and (13.26), the current-voltage representation of the two-port of Fig. 13.4 is found to be:

$$i_i = 2I_S \exp\left(-\frac{v_o}{2nV_T}\right) \sinh\left(\frac{v_i}{2nV_T}\right), \tag{13.30}$$

$$i_o = 2I_S \exp\left(-\frac{v_o}{2nV_T}\right) \cosh\left(\frac{v_i}{2nV_T}\right) - 2I_S. \tag{13.31}$$

Equation (13.30) may be recast as

$$i_i = g(v_o, v_i) v_i, \tag{13.32}$$

with $g(\cdot,\cdot)$ expressed by

$$g(v_o, v_i) = \frac{I_S}{nV_T} \exp\left(-\frac{v_o}{2nV_T}\right) \sum_{k=0}^{\infty} \frac{\left(\frac{v_i}{2nV_T}\right)^{2k}}{(2k+1)!}, \tag{13.33}$$

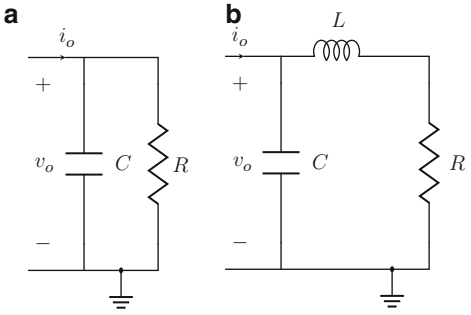

Fig. 13.5 First-order (**a**) and second-order (**b**) linear dynamic one-ports for voltage-controlled voltage-state circuits

where we used the Taylor series expansion of the hyperbolic sine [47]. From (13.32) it follows that any time $v_i = 0$, then $i_i = 0$ and vice versa. This is the so-called *zero crossing property*, typical of a memristor system [2]. Equation (13.32) models the input–output relation of the voltage-controlled voltage-state circuits, whose memductance function is expressed by (13.33).

The state equation of the elements from this class depends on the particular linear dynamic one-port chosen as load to the full-wave rectifier. After choosing a particular one-port topology (making sure it contains a capacitor with voltage v_o across it), the constitutive equations of the dynamical elements within the one-port are then written down. Then, inserting (13.31) into these constitutive equations yields the state equations of a voltage-controlled voltage-state system. Let us present examples of first- and second-order circuits of this kind, deriving their state equations.

- **First-order circuit**

With regard to a first-order case, let us close the output port of the diode bridge onto the parallel combination of a capacitor of value C and of a resistor of value R (see Fig. 13.5a). Inserting (13.31) into the constitutive equation of the capacitor, i.e. $i_o - \frac{v_o}{R} = C\frac{dv_o}{dt}$, the state equation of the resulting system is found to be

$$\frac{dv_o}{dt} = \frac{2I_S}{C}\exp\left(-\frac{v_o}{2nV_T}\right)\cosh\left(\frac{v_i}{2nV_T}\right) - \frac{2I_S}{C} - \frac{v_o}{RC}, \tag{13.34}$$

where v_o denotes the state of the system. This first-order voltage-controlled voltage-state memristor circuit is modeled by (13.32) and (13.34).

- **Second-order circuit**

Let us introduce a second-order example. Let the two-port be cascaded with the second-order one-port of Fig. 13.5b, which is an inductor L-capacitor C parallel circuit augmented with the series resistance R of the inductor and characterized by a resonance frequency expressed by $\omega_o = \sqrt{\frac{1}{LC} - \left(\frac{R}{L}\right)^2}$. Choosing v_o and i_L, the current through the inductor, as the states of the system, writing down the

constitutive equations of the dynamical elements of the one-port, and using (13.31) into them, the following state equations are finally obtained:

$$\frac{d}{dt}\begin{bmatrix} v_o \\ i_L \end{bmatrix} = \begin{bmatrix} -\frac{1}{C} i_L + \frac{2I_S}{C} \exp\left(-\frac{v_o}{2nV_T}\right) \cosh\left(\frac{v_i}{2nV_T}\right) - \frac{2I_S}{C} \\ \frac{1}{L}\left(v_o - R i_L\right) \end{bmatrix}. \tag{13.35}$$

In conclusion, (13.32) and (13.35) define this second-order voltage-controlled voltage-state memristor circuit.

13.5.3.2 Voltage-Controlled Current-State Systems

For these systems one of the states is i_o. The use of the inverse hybrid representation of the two-port of Fig. 13.4 is the most appropriate for the synthesis of these elements. Let us derive such representation. Rearranging (13.31), we have:

$$2I_S \exp\left(-\frac{v_o}{2nV_T}\right) = \frac{(i_o + 2I_S)}{\cosh\left(\frac{v_i}{2nV_T}\right)}. \tag{13.36}$$

Using (13.36) into (13.30) and extracting from (13.36) an expression for v_o as function of v_i and i_i, the inverse hybrid representation of the two-port turns out to be

$$i_i = (i_o + 2I_S) \frac{\sinh\left(\frac{v_i}{2nV_T}\right)}{\cosh\left(\frac{v_i}{2nV_T}\right)}, \tag{13.37}$$

$$v_o = -2nV_T \ln\left(\frac{i_o + 2I_S}{2I_S \cosh\left(\frac{v_i}{2nV_T}\right)}\right). \tag{13.38}$$

Equation (13.37) may be recast as

$$i_i = g(i_o, v_i) v_i, \tag{13.39}$$

with $g(\cdot,\cdot)$ given by

$$g(i_o, v_i) = \frac{(i_o + 2I_S)}{2nV_T} \frac{\sum_{k=0}^{\infty} \frac{\left(\frac{v_i}{2nV_T}\right)^{2k}}{(2k+1)!}}{\sum_{k=0}^{\infty} \frac{\left(\frac{v_i}{2nV_T}\right)^{2k}}{(2k)!}}, \tag{13.40}$$

where we used the Taylor series expansions of the hyperbolic sine and cosine [47].

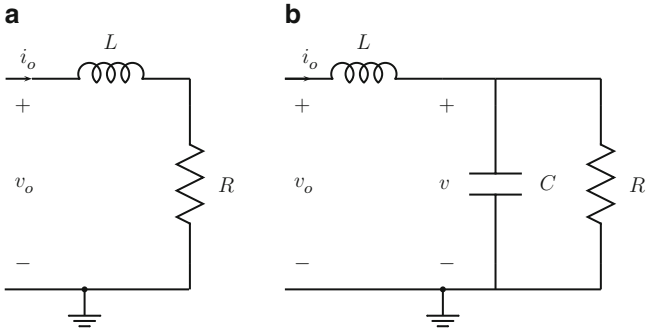

Fig. 13.6 First-order (**a**) and second-order (**b**) linear dynamic one-ports for voltage-controlled current-state circuits

From (13.39) we deduce that $v_i = 0$ implies $i_i = 0$ and viceversa. Equation (13.39) defines the input–output relation of the voltage-controlled current-state circuits, whose memductance function is modeled by (13.40).

The state equation of the elements from this class depends on the particular linear dynamic one-port chosen as load to the full-wave rectifier. After choosing a particular one-port topology (making sure it contains an inductor with current i_o through it), the state equations of a voltage-controlled current-state circuit are obtained by inserting (13.38) into the constitutive equations of capacitors and inductors of the one-port. Let us describe examples of first- and second-order circuits of this kind and determine their state equations.

- **First-order circuit**

With regard to a first-order case study, the series combination between an inductor L and a resistor R, as given in Fig. 13.6a, is taken as the load of the switching network of Fig. 13.4. Inserting (13.38) into the constitutive equation of the inductor, i.e. $v_o - Ri_o = L\frac{di_o}{dt}$, yields the following state equation:

$$\frac{di_o}{dt} = -\frac{2nV_T}{L}\ln\left(\frac{i_o + 2I_S}{2I_S\cosh\left(\frac{v_i}{2nV_T}\right)}\right) - \frac{R}{L}i_o, \tag{13.41}$$

where i_o denotes the state of the system. In conclusion, (13.39) and (13.41) define this first-order voltage-controlled current-state memristor circuit.

- **Second-order circuit**

With regard to a second-order example, let us close the output port of the full-wave rectifier of Fig. 13.4 onto the inductor L-capacitor C series circuit augmented with the parallel resistance R of the capacitor. The resonance frequency of such second-order one-port, shown in Fig. 13.6b, is expressed by $\omega_o = \sqrt{\frac{1}{LC} - \left(\frac{1}{RC}\right)^2}$. Writing

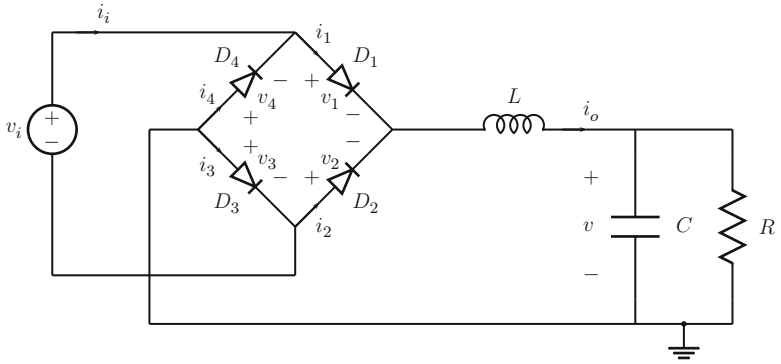

Fig. 13.7 A second-order voltage-controlled current-state memristor element from the proposed class. The element is driven by input voltage source v_i

down the constitutive equations of the dynamic elements of the one-port and the inserting (13.38) into them, the state equations are found to be:

$$\frac{d}{dt}\begin{bmatrix} v \\ i_o \end{bmatrix} = \begin{bmatrix} \frac{1}{C}\left(i_o - \frac{v}{R}\right) \\ -\frac{1}{L}v - \frac{2nV_T}{L}\ln\left(\frac{i_o+2I_S}{2I_S\cosh\left(\frac{v_i}{2nV_T}\right)}\right) \end{bmatrix}, \tag{13.42}$$

where v, the voltage across the capacitor, and i_o denote the states of the system.

In conclusion, the defining equations of this second-order voltage-controlled current-state memristor circuit are (13.39) and (13.42).

13.5.4 Simulation Results

With reference to the voltage-controlled current-state second-order memristor circuit of Fig. 13.7 [46], making use of the diode bridge of Fig. 13.4 loaded by the second-order one-port shown in Fig. 13.6b and discussed in Sect. 13.5.3.2, the system state is expressed as $\mathbf{x} = [x_1\, x_2]'$, where state variables are defined as $x_1 = v\,(V_T)^{-1}$ and $x_2 = i_o\,(I_S)^{-1}$. Further system input and output are chosen as $u = v_i\,(V_T)^{-1}$ and $y = i_i\,(I_S)^{-1}$ respectively, and dimensionless time variable is taken as $\tau = t\,(t_0)^{-1}$, where $t_0 = 2\pi\,(\omega_0)^{-1}$ stands for the time normalization factor and ω_0 is the resonant frequency of the one-port of Fig. 13.6b, which we previously defined. After some algebraic manipulation we get:

$$\frac{d\mathbf{x}}{d\tau} = \begin{bmatrix} \beta(x_2 - \alpha x_1) \\ \gamma\left(-x_1 - 2n\ln\left(\frac{x_2+2}{2\cosh\left(\frac{u}{2n}\right)}\right)\right) \end{bmatrix} \tag{13.43}$$

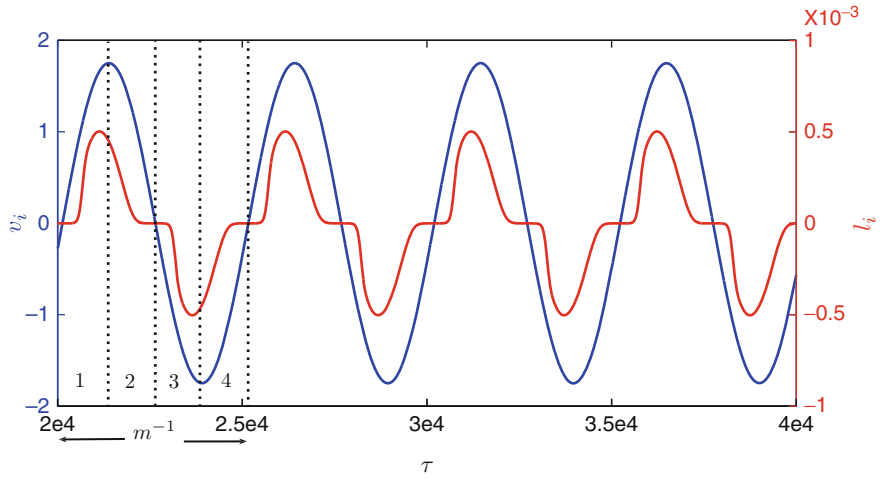

Fig. 13.8 Time waveforms of current i_i (*red signal*) and voltage v_i (*blue signal*) under sinusoidal excitation with $v_{io} = 1.75V$ and $f_i = 10Hz$. The dimensionless input period m^{-1} is divided into 4 intervals, numbered from 1 to 4, separating zeros, minimum and maximum of the voltage waveform

$$y = (x_2 + 2)\frac{\sinh\left(\frac{u}{2n}\right)}{\cosh\left(\frac{u}{2n}\right)} \tag{13.44}$$

where $\alpha = \frac{V_T}{RI_S}$, $\beta = \frac{t_0 I_S}{CV_T}$ and $\gamma = \frac{t_0 V_T}{LI_S}$ are dimensionless parameters. The Matlab software environment [48] was used for the numerical integration of the *mathematical model* of the memristor circuit of Fig. 13.7, i.e. (13.43)–(13.44), for a sine-wave input source with amplitude $v_{io} = 1.75V$ and varying frequency f_i, expressed as $v_i = v_{i0}\sin(2\pi f_i t)$, which yields $u = u_{i0}\sin(2\pi m\tau)$, where $u_{io} = v_{io}\,(V_T)^{-1}$ and $m = f_i t_0$ denotes the dimensionless input frequency. The values of the circuit components were set to $R = 1.5k\Omega$, $C = 4\mu F$, and $L = 2.5\mu H$. The values for saturation current I_S and emission coefficient n of the four matched diodes were respectively taken as $2.682 \cdot 10^{-9}$ and 1.836, i.e. as in the case of standard diode $D1N4148$. The initial conditions of the voltage across the capacitor and of the current through the inductor are respectively chosen as $v(0) = 0.01V$ and $i_L(0) = 0.01A$. Ordinary differential equation solver ode15*s* [48] was employed to integrate (13.43)–(13.44) from $\tau = 0$ up to τ equal to 10 times the dimensionless input period $m^{-1} = f_i^{-1} t_0^{-1}$. Under such parameter setting, letting the input frequency $f_i = 10Hz$, the time evolutions of voltage v_i and current i_i are depicted in Fig. 13.8, from which it is evident that voltage and current exhibit zeros at the same instants but have misaligned maxima and minima. As a result, the circuit of Fig. 13.7 manifests the typical pinched hysteretic current-voltage loop characterizing memristor systems, as it is shown in Fig. 13.9 (black bow-tie). With reference to Fig. 13.8, note that over each normalized period m^{-1} the maximum and minimum of the current always occur before the maximum and minimum of the voltage. As a result, following the path

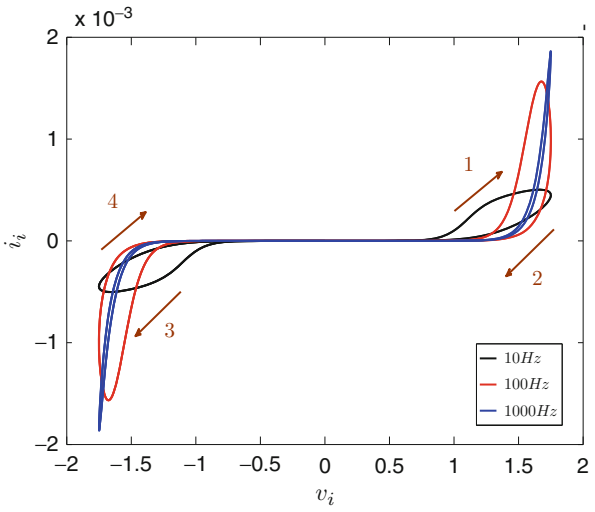

Fig. 13.9 Current i_i-voltage v_i bow-ties under sinusoidal excitation with $v_{io} = 1.75\,V$ and f_i, respectively, equal to $10\,Hz$ (*black loop*), $100\,Hz$ (*red loop*), and $1000\,Hz$ (*blue loop*). *Brown arrows*, mapping one-to-one with time intervals 1-4 in Fig. 13.8, show the non-self-crossing property of the i_i-v_i loop for $f_i = 10\,Hz$ (note that this property is exhibited by the other loops as well)

drawn by the trajectory point on the i_i-v_i plane in one period, as indicated by the four consecutively numbered brown arrows in Fig. 13.9 (corresponding to the four intervals in which the period is divided in Fig. 13.8), it may be realized that the loop is non-self-crossing, i.e. it is of type *II*, according to the definition given by Biolek in [49]. With reference to Fig. 13.7, the voltages across the bridge diodes may be expressed as

$$\begin{aligned} v_1 &= v_3 = nV_T \ln\left(\frac{x_2+2}{2\cosh\left(-\frac{u}{2n}\right)\exp\left(-\frac{u}{2n}\right)}\right), \\ v_2 &= v_4 = v_1 - v_i. \end{aligned} \tag{13.45}$$

Figure 13.10 shows the time dependence of v_1 and v_2 in the simulation of Fig. 13.8.

Sweeping frequency above $10\,Hz$, the lobes of the loop get increasingly squeezed (while stretching along the i_i axis), as it is demonstrated in Fig. 13.9, where the red and blue bow-ties respectively refer to an input frequency f_i set to $100\,Hz$ and $1000\,Hz$. Note that these other two loops also are of type *II*.

It is worth pointing out that at infinite frequency, when the inductor and the capacitor respectively are an open and a short circuit, the electronic system of Fig. 13.7 behaves as a nonlinear resistor. Furthermore, sweeping frequency below $10\,Hz$ also yields a gradual flattening of the loop lobes. Finally, bear in mind that nonlinearly resistive behavior also arises at direct current (dc), when the inductor and the capacitor respectively are a short and an open circuit.

An experimental proof for the occurrence of memristor behavior in the circuit of Fig. 13.7 is reported in [50].

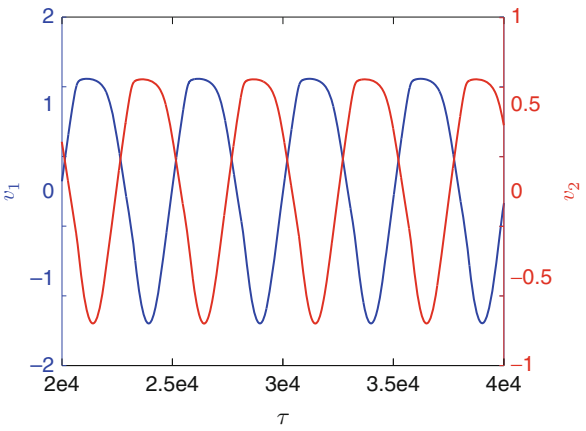

Fig. 13.10 Voltage drops across the bridge diodes for the sinusoidal excitation at frequency $f_i = 10Hz$

13.6 Conclusions

After a brief review of the memristor models available in the literature, this paper describes the PSpice-based implementation of the generalized Boundary Condition Memristor (BCM) model, which stands out over the other models thanks to the adaptability of the boundary behavior and to the tunability of the non-volatility degree. The first part of the paper ends with a case study where the use of the PSpice emulator sheds light into the synapse-like behavior of the memristor. Such circuit implementation of the generalized BCM model may be of great help to researchers willing to investigate in the user-friendly PSpice environment the extraordinary opportunities memristors offer in integrated circuit design.

The second part of the paper introduces a class of purely passive circuits, each made up of a nonlinear static two-port (a full-wave rectifier employing a four diode bridge) cascaded with a linear dynamic one-port (employing standard linear components from circuit theory, namely resistors, inductors and capacitors). The state equations of these circuits fall into the class of memristor systems, as originally formulated by Chua and Kang in 1976 [2]. This manuscript presents voltage-controlled elements from the proposed class. Dual memristor emulators with current-control may be derived in a similar manner [50]. These novel circuits may be used to introduce the undergraduate students to the concept of memory systems [51, 52]. In conclusion, it is important to note that all the novel memristor circuits proposed in this manuscript are *volatile*. However, we conjecture that non-volatility could be attained by inserting active elements into the one-port loading the diode bridge. This shall be the topic of future studies, where we aim at increasing the complexity of the circuits presented in this manuscript so as to model memristor systems within the Hodgkin-Huxley neuron [53].

Acknowledgments This work was partially supported by the CRT Foundation, under the project no. 2012.1121 and by the Ministry of Foreign Affairs "*Con il contributo del Ministero degli Affari Esteri, Direzione Generale per la Promozione del Sistema Paese*."

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