

Low-Power 60-GHz CMOS Radios for Miniature Wireless Sensor Network Applications

Kuo-Ken Huang and David D. Wentzloff

Abstract This chapter discusses several design considerations for low-power 60-GHz complementary metal-oxide semiconductor (CMOS) radios for wireless sensor network applications at the cubic-mm scale. A background study is provided first, followed by a discussion of challenges to provide a practical scope of the hardware design for the readers. Finally, a compact 60-GHz CMOS transmitter with on-chip frequency-locked loop is presented as an example. This transmitter utilizes the on-chip patch antenna as both a radiator and a frequency reference. This eliminates the bulky off-chip crystal, is FCC compliant, and ensures the node transmits at the antenna's peak efficiency point, making this a cost-effective 60-GHz radio for mm-scale sensor nodes.

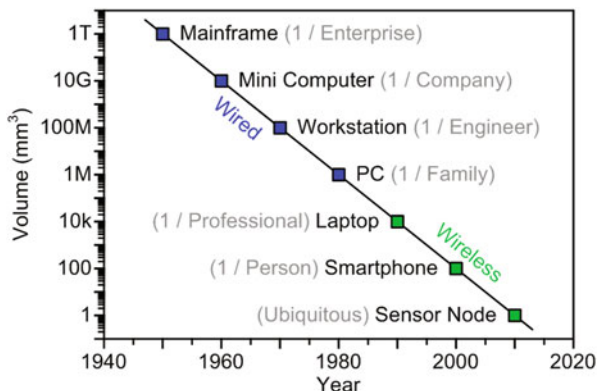
Keywords Wireless sensor networks · CMOS · Transmitter · 60 GHz · Low-power · Crystal replacement · Frequency reference · Integrated antenna

Introduction

The continual evolution of computing devices has significantly changed daily life over the past several decades. In the 1950s, mainframe computers occupied large rooms because of their substantial size and provided the basic data computation for hundreds of employees in a company. Nowadays, smartphones have become the platform of personal computing, as predicted by Bell's Law [1]. Emerging applications such as wireless sensing, smart health care, unobtrusive surveillance, etc. will demand ubiquitous computing, which will continue to drive the computing platform down to the mm scale, while also driving production volume of these devices up to 100s to 1,000s per person. According to Bell's Law, a new class of computers will dominate the market approximately every decade [1]. Gordon Bell defines a computer class as a set of computers with similar cost, programming environment, network, and user interface. He postulates that each class undergoes a standard product life

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Fig. 1 Scaling and production trend of computing devices over several decades [1]



cycle of growth and decline. Based on prior market trends, a new computer class has come into existence approximately every decade, and each successive class has resulted in a 100-fold reduction in volume. Figure 1 shows the scaling and production trend of computing devices over several decades. Computers progressed from the mainframe in the early 1950s, through minicomputers, workstations, personal computers (PCs), and laptops, to the class of smartphones in the 2000s. Based on the trends, a new computer class has in fact emerged approximately every decade, each class resulting in both a reduction in unit cost and a 100-fold increase in production volume [2].

The next computer class is expected to be even smaller and more pervasive—the class of cubic-mm-scale devices. Ubiquitous sensing is projected to reach volumes of 1,000 sensors per person by 2017 [3]. Considering that today we are surrounded by about 100 sensors while at work, in the car, and at home, this target does not seem that far off. At the mm scale, there is a growing demand for “smaller and smarter” devices in applications such as biomedical implants and unobtrusive monitoring. Wireless sensor networks (WSNs) are perceived as the next big step in the decades-long trend toward smaller, more ubiquitous computing. A WSN consists of distributed autonomous sensor nodes to monitor the environmental conditions around them, such as temperature, vibration, imaging, and sound, etc. Each node is made up of components to process, sense, and communicate with other nodes in the network, and to cooperatively pass their data through the network to a main location [4–8]. WSNs eliminate the need for costly and obtrusive wiring between sensors, allowing sensors to be deployed in almost any location, which is promising for many emerging applications (Fig. 2).

Cubic-mm Wireless Sensor Nodes

The requirements on a WSN can vary widely depending on the application. The hardware design plays an important role for many of these applications. Compact hardware, wireless connectivity, and local processing, along with long node lifetime

Wireless Sensor Networks Applications

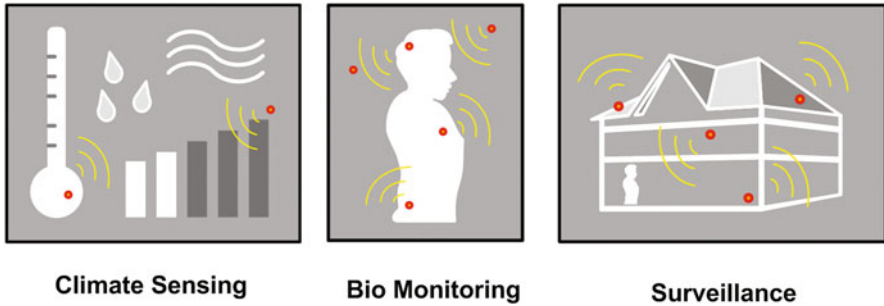
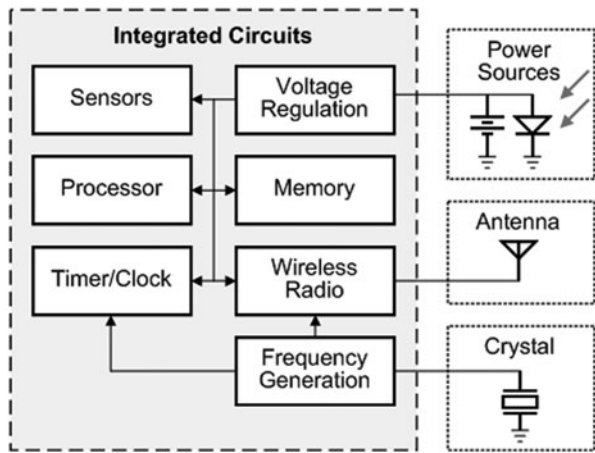


Fig. 2 Wireless sensor network applications

Fig. 3 Block diagram for a typical wireless sensor network (WSN) node

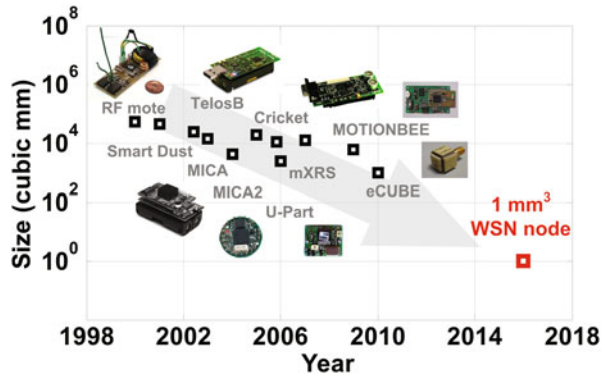


are generally desirable, nonetheless, quite challenging. In this section, we will start with the conventional WSN node and then explain the difficulties of realizing a low-power mm-scale WSN radio.

Conventional Wireless Sensor Node

Figure 3 shows the block diagram of a typical integrated WSN node. Each node generally has one to five sensors (e.g., temperature, pressure, accelerometer), a digital signal processor (DSP), voltage regulation and power management controller, a radio frequency (RF) front end and antennas for wireless communication, a battery as the energy source, and a crystal for a frequency reference. Among the building blocks, the power source, antenna, and the crystal are the hardest components to integrate in silicon [4], which is desirable for lowering cost and miniaturization of

Fig. 4 Size reduction trend of integrated wireless sensor network (WSN) nodes over years



the node. Figure 4 summarizes commercially available integrated WSN nodes over the past decade. We can see there is a clear trend of size reduction for the WSN nodes [9]. In the late 1990s, WSN nodes were composed of multiple components on a printed circuit board (PCB) as shown in Fig. 4. These nodes consistently use commercial-off-the-shelf (COTS) components, and as a result, their sizes are in the tens of cubic centimeters. Higher levels of integration and better system-level node design are pushing this to the mm scale. Nonetheless, there are few bottlenecks in cubic-mm WSN system integration that need to be solved to achieve long lifetimes and small volumes.

mm-Scale Energy Storage: Microbatteries

Rechargeable batteries are being manufactured today at the mm scale, termed microbatteries, by using solid-state lithium technology. These batteries are manufactured on wafers with a planar process and with connections on the top side, similar to integrated circuits (ICs), and they can be diced with sub-mm dimensions. Also like ICs, no special packaging is required once the batteries are fabricated; therefore, they are amenable to die stacking and integrating with other silicon ICs in a stack. However, these microbatteries have limited capacity and small peak current due to the direct relationship between capacity and volume [10–17]. For a $1.38 \times 0.85 \times 0.15$ mm custom lithium-ion (Li-ion) battery from Cymbet Corporation, the capacity is only 1 μAh (Fig. 5) and the maximum discharge current is only 10 μA [11]. This presents direct challenges on the radio circuits, which typically consume $> 100 \mu\text{W}$ when active. As a result, for a node to survive longer, it must be duty-cycled heavily and energy must be harvested from other sources to supplement battery power. From a circuit design point of view, energy usage must be reduced by clever circuit techniques. The radio and oscillators easily dominate system energy usage if they are operated continuously to maintain synchronization for WSN nodes to communicate at the same frequency band [18]. A phase-locked loop (PLL) with a crystal reference

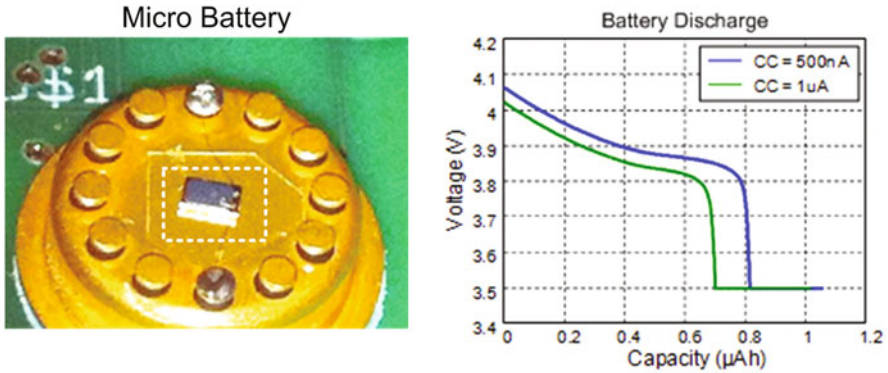


Fig. 5 Micrograph of the Cymbet microbattery and its discharge curves

is typically used to accurately set the center frequency of the radio [19]. Reducing the RF synchronization power consumption can greatly improve the WSN node lifetime and alleviate the burden of cubic-mm-scale microbatteries.

mm-Scale Frequency References

A frequency reference provides a stable frequency over process, voltage, and temperature (PVT) variations for synchronization of a communication system. The accuracy requirement depends on the system specifications (e.g., frequency allocations, modulation type, etc.) [18], and can be achieved through different ways. A quartz crystal is the most common source for a frequency reference. It provides excellent stability with PVT variations. However, its size has not scaled down significantly with processes or frequency. Furthermore, crystals require a piezoelectric process and special packaging, which are incompatible with monolithic integration for ICs. In order to achieve stable oscillation out of crystals, a certain amount of driving power is still necessary [20]. Figure 6 shows a COTS WSN node, the TelosB [24]. The 32 kHz crystal is highlighted with a red square, illustrating the volume and packaging of these references. Therefore, bulky size and power become the bottlenecks for using crystals at the mm scale. Recently, microelectromechanical systems (MEMS) and complementary metal-oxide semiconductor (CMOS) references have been demonstrated with near-crystal accuracies [20–23]. Table 1 shows a comparison of compact frequency references made of crystal, MEMS and CMOS. These frequency accuracies are acceptable for typical WSN node specifications; however, powers are high and none of their sizes are below 1 mm³. A compromise must therefore be made on the frequency accuracy, in order to allow a stable frequency reference to be integrated in CMOS at the mm scale, along with other WSN circuits, with a power consumption that better matches what can be supported by a microbattery.

Fig. 6 A 32-kHz crystal on wireless sensor network (WSN) node, TelosB [24]

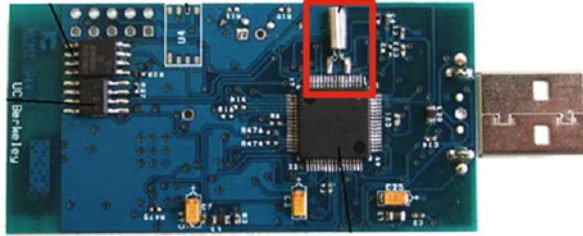


Table 1 Comparison of compact frequency references

	Crystal [21]	MEMS [22]	CMOS [23]
Manufacturer	Vectron International	SiTime	Silicon Labs
Volume	9.6 mm ³	4.5 mm ³	11.5 mm ³
Accuracy	25 ppm	50 ppm	150 ppm
Power	82.5 mW	72.6 mW	26.4 mW

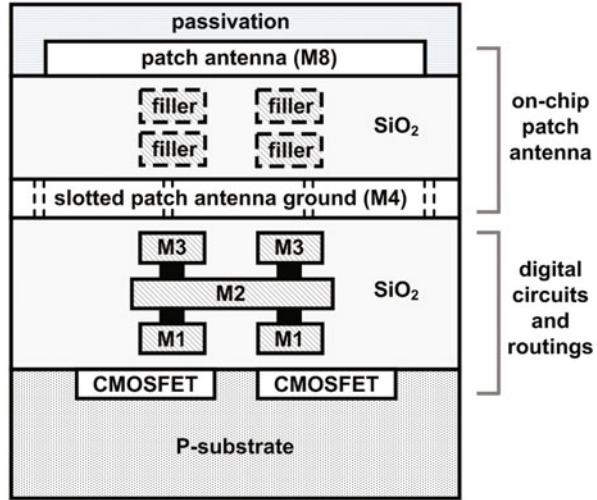
MEMS microelectromechanical systems, *CMOS* complementary metal-oxide semiconductor

mm-Scale Antennas

Among the building blocks in a WSN node, the antenna plays a critical role because it is traditionally off-chip for better performance, and its size dominates at least one dimension of the node. Antennas integrated in a CMOS process have a size advantage over external packaged antennas; however, reducing antenna size at a fixed frequency, in general, results in reduced performance [25]. Antennas can be integrated directly on-chip, but at the mm scale, the operating frequencies need to be at least 10 GHz for good radiation efficiency [9]. However, operating at higher frequency has other disadvantages. First, the path loss in the wireless channel increases [25]. As a result, more signal power is lost for a fixed communication distance. Second, RF front end circuits that operate at these higher frequencies will consume more power. On-chip antennas seem to be a good candidate to meet the mm³ volume requirement of future sensor nodes, but there are several design trade-offs to consider.

CMOS technology is preferable nowadays of ICs because of its low cost, decent performance, and ease of integration [32]. Nevertheless, there are several challenges for on-chip antenna integration. First, the area occupied by the antenna and the space for isolating the crosstalk between antenna and active circuits should be considered. Additionally, the lossy silicon P-substrate ($\sim 10 \Omega \text{ cm}$) in a CMOS process degrades the antenna performance significantly because energy dissipates in the substrate instead of radiating into the air. Moreover, the design rules in CMOS technology such as metal slotting and density requirements also impact the antenna design. Figure 7 shows the cross section of an on-chip CMOS patch antenna [32]. In this example, the patch radiator is in top metal, with the patch ground plane in an intermediate metal layer, and metal layers below the ground plane are used for routing circuits under the patch (e.g., DSP and memory). This approach suffers from reduced antenna

Fig. 7 Layout cross section of an on-chip patch antenna integrated in complementary metal-oxide semiconductor (CMOS) technology



efficiency due to the higher ground plane, but allows for reusing the area below the patch for circuits and routing in a system-on-a-chip (SoC) application. For example, conventional digital circuits typically use four to six metal layers for wire routing; fewer metal layers is feasible, but at the cost of lower circuit density. Consequently, the patch antenna is a good candidate for system integration in CMOS technology because of the better performance (ground shielding) and reusable area beneath the patch ground plane.

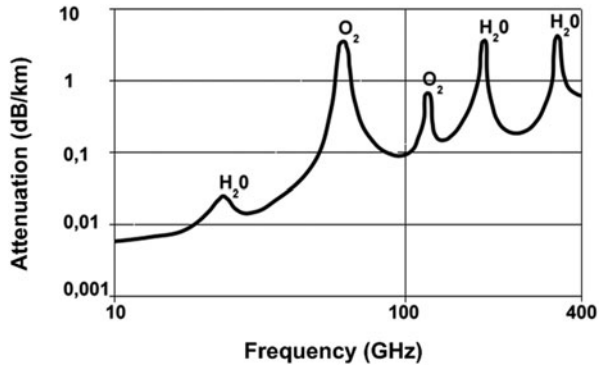
A 60-GHz Transmitter for WSNs

The 60-GHz band is an emerging field for miniature radio design because the sizes of the antenna and passive components are at or below mm scale. Recently, several highly integrated CMOS radio systems with on-chip antennas operating at the mm-wave range have been reported [26–29], showing promising opportunities for complete SoC integration. In this section, we will discuss the 60-GHz band allocation and show a design example of a low-power 60-GHz frequency-locked loop (FLL) that can serve as a fully integrated transmitter for WSNs. The transmitter described in this section was designed in a 130-nm CMOS process with eight metal layers, including a thick top metal for RF routing.

60-GHz Wireless Communication

The industrial, science, and medical (ISM) band approved by Federal Communications Commission (FCC) has 7 GHz of bandwidth from 57 to 64 GHz [30]. At 60

Fig. 8 Atmosphere attenuation of electromagnetic wave versus frequency

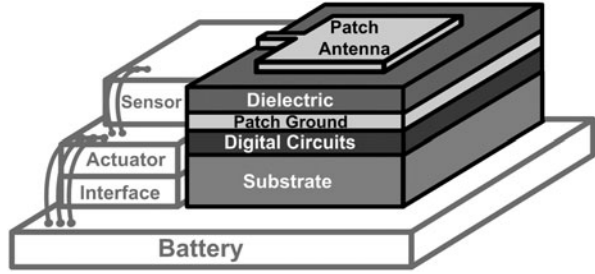


GHz, the guided wave length λ in silicon is about 2.5 mm; which is on the same scale as the active circuit blocks implemented in CMOS (e.g., processor, memory, and radio circuits). Furthermore, the elimination of expensive off-chip antennas, path loss, crystal references, and the total size reduction makes 60-GHz operation more appealing for wireless system integration. Sixty gigahertz is also referred to as the oxygen absorption band [31]. As shown in Fig. 8, the oxygen molecule (O_2) absorbs electromagnetic energy due to resonance at different frequencies. The excessive attenuation causes high path loss at 60 GHz. Despite this increased attenuation, the 60-GHz band can still be beneficial for short-range applications like WSNs and wireless personal area networks (WPAN).

60-GHz Antenna-Referenced Frequency-Locked Loop

In order to eliminate the bulky off-chip components and further reduce the size of a fully integrated WSN node, we will discuss a solution of using a 60-GHz on-chip patch antenna as both the radiator and frequency reference in this section. The natural resonant frequency of the patch antenna serves as the frequency reference. The resonant frequency is mainly determined by the physical dimensions of the patch antenna, and the standard deviation due to process variation is around 1,100 ppm. This accuracy level is suitable for, e.g., low-rate communication with a noncoherent energy-detection receiver, commonly used in ultralow power WSN radios. With the antenna as the reference, an FLL circuit to track the reference frequency for RF synchronization is described and implemented. Furthermore, the area beneath the patch antenna ground plane is investigated for containing additional circuits for higher integration. Figure 9 depicts the concept of a complete mm-scale WSN node. By integrating the antenna, frequency reference, RF front end, and digital circuitry onto the same die, a form factor of 1 mm^3 is feasible.

Fig. 9 A miniature fully integrated wireless sensor network (WSN) node system



Patch Antenna Design

As an on-chip radiator, the patch antenna topology is chosen because its ground plane shields the radiating element from the lossy substrate in standard CMOS processes, and thus provides higher radiation efficiency than nonshielded integrated antennas. Moreover, the patch antenna is also a good candidate for system integration because of the reusable area beneath the ground plane for high noise margin digital circuits. The distance between the patch metal layer (top-metal M8) and the ground metal layer determines the height of the patch antenna. The tradeoff between radiation efficiency and height are discussed by Huang and Wentzloff [32]. The analysis suggests that lower antenna height (or implementing the patch ground in a higher metal layer in a CMOS process) results in lower radiation efficiency. In this 130-nm CMOS process, Metal 4 is used as the ground plane, resulting in an antenna height of 14.1 μm . On the basis of simulations, using Metal 4 for the ground plane instead of Metal 1 reduces the radiation efficiency by 15 %, but frees up three metal layers for routing of circuits beneath the antenna. With the center frequency (f_0), dielectric constant of the silicon dioxide (SiO_2) (ϵ_r), and the height (h), we can calculate the required width (W) of the patch antenna by antenna theory.

$$W = \frac{c}{2f_0\sqrt{\frac{\epsilon_r+1}{2}}}, \tag{1}$$

where c is the speed of light [25]. With the calculated W , we can find the effective dielectric constant ϵ_{eff} .

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \left(1 + 12 \frac{h}{W} \right)^{-\frac{1}{2}}. \tag{2}$$

It follows that the length of the patch antenna (L) is

$$L = \frac{c}{2f_0\sqrt{\epsilon_{reff}}} - 0.824h \frac{(\epsilon_{eff} + 0.3) \left(\frac{W}{h} + 0.264 \right)}{(\epsilon_{eff} - 0.258) \left(\frac{W}{h} + 0.8 \right)}. \tag{3}$$

Note that the size of the ground plane layer is greater than the patch dimensions by approximately six times the height all around the periphery to achieve results similar

Fig. 10 The dimensions of the 60-GHz patch antenna

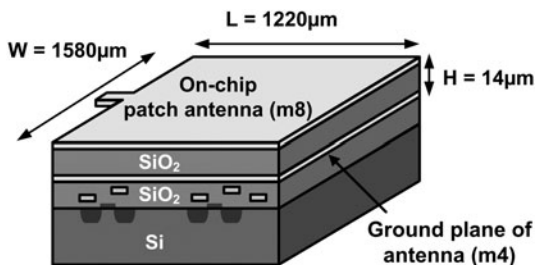
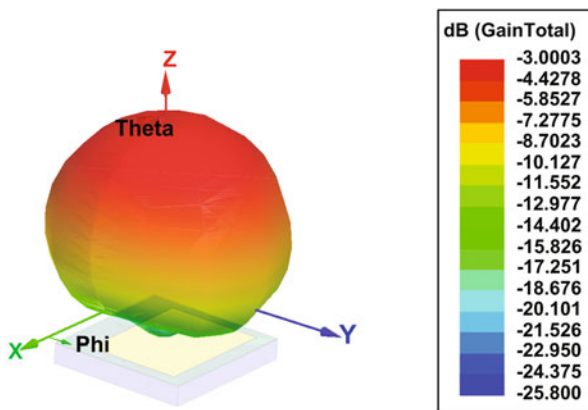


Fig. 11 Radiation pattern of the 60-GHz on-chip patch antenna

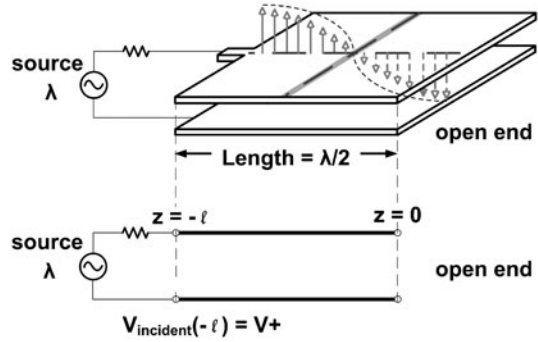


to that of an infinite ground plane [25]. Figure 10 illustrates the final dimensions of the patch antenna. The resonant frequency is mainly determined by the width and length that can be verified by back calculating for f_0 from Eqs. 1–3 when W and L are known. The 3σ process variation parameters on length and width of the top metal layer are on the order of 400 ppm, resulting in the same order of accuracy of the resonant frequency of the patch antenna, determined by the first-order antenna theory. The simulated antenna radiation pattern is shown in Fig. 11. The simulation results include the effects of required dummy filling for meeting local metal density requirements, and show that the center frequency is 60.54 GHz with a bandwidth of 920 MHz. The peak antenna gain is -3 dB while the efficiency at resonance is 15.6 %.

Resonant Frequency Detection

Another advantage of the integrated patch antenna at 60 GHz is the ability to design circuits that monitor the standing wave pattern along the edge of the radiator. This allows for detecting the resonant frequency of the antenna, and ultimately using it as a replacement for a crystal reference. To detect the resonant frequency, we will need to understand the physical phenomena on the patch antenna when it is resonating.

Fig. 12 Simplified lossless transmission line model of the patch antenna



A simplified lossless transmission line model for the antenna is adopted for this analysis. Figure 12 shows the transmission line model corresponding to the patch antenna along the length axis. We can consider the patch antenna as a very wide transmission line, with the feed point being the source terminal, while the other edge behaves as the open end. When the source frequency is exactly at the resonant frequency, the length of the transmission line is equal to $\lambda/2$, and a standing wave pattern is generated by the superposition of the incident wave from the source and the reflected wave from the load. At this frequency and under these conditions, the patch antenna radiates at its peak efficiency value. The source end and open end have the strongest electric fields, and those are the radiation edges. Note that there is an electrical null located in the center of the length axis (e.g., $z = -l/2$, where l is the length of the patch), shown as the solid shaded area in Fig. 12. The amplitude of the standing wave on the transmission line as a function of the length can be written in the general form [33]:

$$V(z) = V^+(e^{-j\beta z} + \Gamma e^{j\beta z}), \tag{4}$$

where V^+ is the incident wave magnitude at $z = -l$, β is the propagation constant $2\pi/\lambda$, and Γ is the voltage reflection coefficient. When the load is open, $\Gamma = 1$, thus the magnitude of the standing wave reduces to

$$|V(z)| = |V^+| \sqrt{[2 + \cos(2\beta z)]} \tag{5}$$

Figure 13a shows the magnitude plot of three standing wave patterns corresponding to three different source frequencies. The standing wave pattern according to Eq. 5 changes with frequency, and the corresponding location of the electrical null will move along the transmission line length as frequency changes. When the source frequency is lower than the resonant frequency, the electrical null moves toward the source end. On the other hand, the electrical null will move toward the open end if the source frequency is higher than the resonant frequency. Consider two taps, Z_A and Z_B (Fig. 13a), placed along the edge but at equal distances from the center of the patch, that monitor the magnitude of the standing wave. By monitoring the

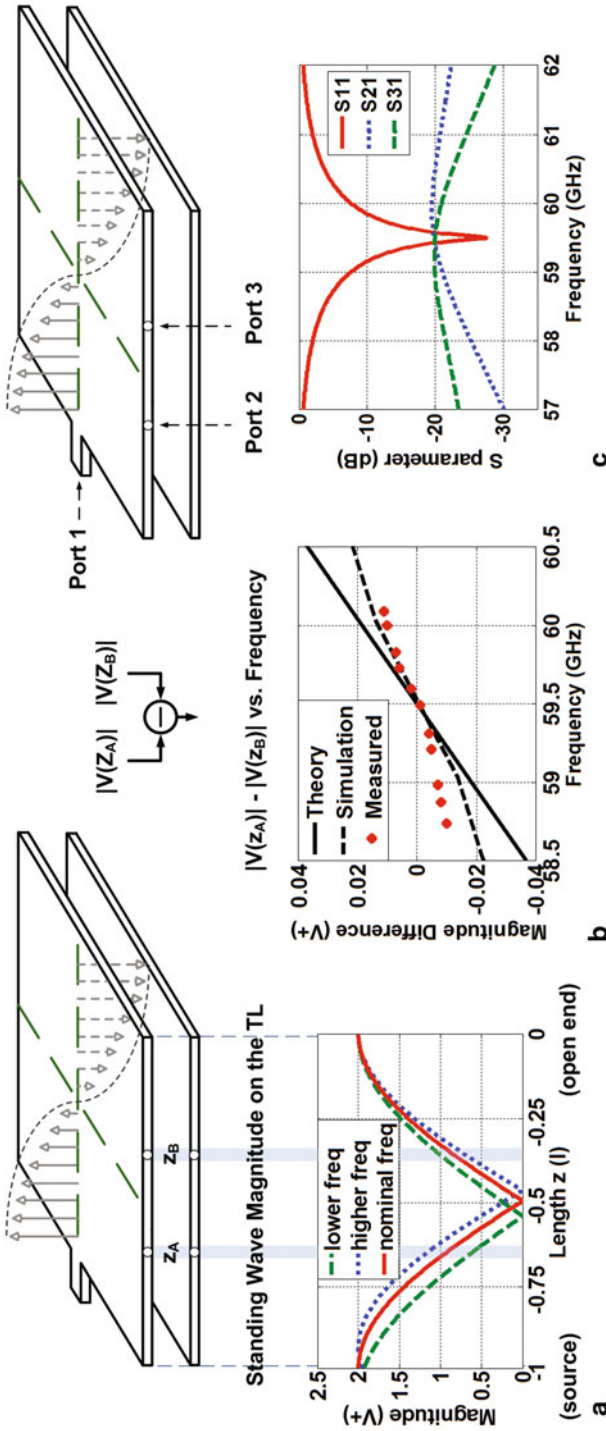


Fig. 13 Center frequency detection of the antenna reference. **a** Standing wave magnitude along the length for three frequencies at source. **b** The difference in magnitude of two taps Z_A and Z_B versus frequency. **c** S-parameter analysis of the three-port antenna reference. TL = Transmission Line

difference in voltage magnitudes at these two taps as frequency changes, a monotonic curve passing through zero will be traced out, with the zero-crossing occurring at the resonant frequency. Figure 13b shows three monotonic curves plotting the difference in magnitude measured at these two taps. The solid line is derived from the lossless transmission line model, assuming perfect matching over the frequency band. The dashed line is obtained from Ansoft HFSS full-Electro-Magnetic (EM) simulations of the three-port antenna reference setup in Fig. 13c, showing the discrepancy due to the limited bandwidth of the patch antenna. Measured results from a 60-GHz patch antenna fabricated in 130-nm CMOS are shown as dots in Fig. 13b, which follow the same trend as the simulation. Figure 13c also shows the S-parameter analysis. S₂₁ and S₃₁ represent the ratio of power delivered onto Z_A and Z_B , respectively, from the antenna feed point at Port 1. The two tap nodes are designed to be high-impedance nodes, so that they do not load the patch antenna significantly, but provide enough voltage swing for envelope detector circuits below the patch to measure the standing wave magnitude. Simulation results show that only 2% of the power delivered onto the patch antenna is lost on the two tap nodes.

The locations of the two taps along the edge of the antenna depend on several factors. A wider separation between the two taps provides a larger slope of the monotonic curve, thus a larger controller gain in the FLL and more accurate resonant frequency detection. However, the frequency locking range over which the sensed voltage magnitude difference remains monotonic is inversely proportional to the separation between taps. Therefore, if the separation is too wide for a target frequency range, the monotonic characteristic no longer applies, which could result in instability in the FLL. Furthermore, the two envelope detectors would be placed far away from each other on the chip, causing mismatch from separation within the single IC [34], and thus affecting the accuracy of tracking the resonant frequency. In the final layout of the antenna reference, the two taps are equally spaced, 110 μm away from the length center, resulting in a calculated locking range of 8.5 GHz. Another factor that will affect the locking range of the antenna reference is the antenna bandwidth. A larger bandwidth implies a wider locking range. In this case, the antenna bandwidth is around 1 GHz, which provides sufficient range for covering process variation of the patch antennas.

In order to test the antenna resonant frequency and bandwidth, the patch antenna design with the same dimensions as the one in the FLL was fabricated in 130-nm CMOS. Twenty of the patch antennas were tested, all from the same wafer. Figure 14 shows the distribution on measured resonant frequency and bandwidth over 20 replica patch antennas. The mean and standard deviation of the center frequency is 59.7 GHz and 65.1 MHz, respectively. The mean and standard deviation of the bandwidth is 1.03 GHz and 67.9 MHz, respectively. This results in a 3σ variation in center frequency of 3,270 ppm, which is enough to ensure the transmitter is FCC compliant (i.e., it remains in the 60-GHz ISM band). In order for the transmitter to reliably communicate with, e.g., an energy-detection receiver with an identical patch antenna (not included in this work), process variation should not cause the transmitter frequency to fall outside the bandwidth of the receiving antenna. Assuming a worst-case 3σ variation on all parameters from process variation, the 3,270 ppm variation is

Fig. 14 Measured antenna resonant frequency and bandwidth distribution over 20 replicas

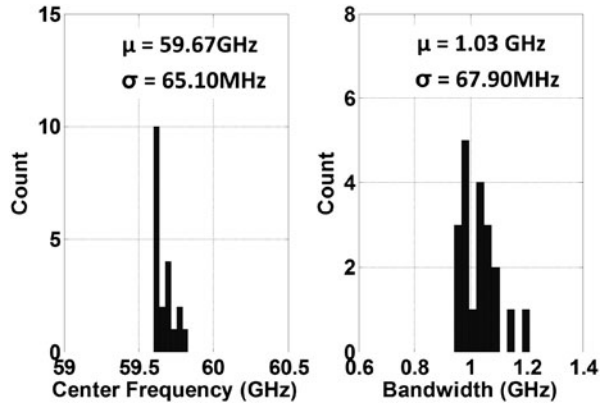
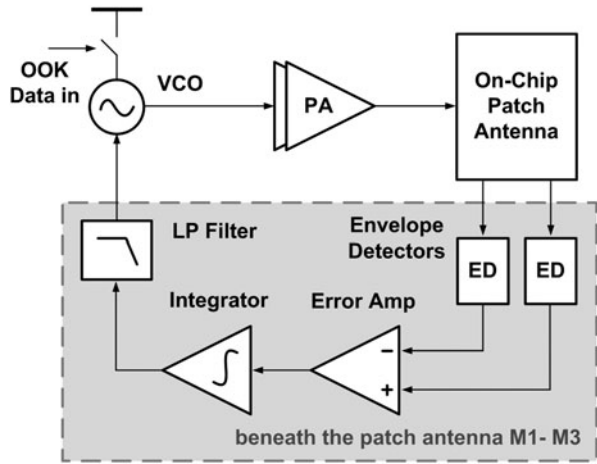


Fig. 15 Block diagram of the 60-GHz FLL. *OOK* on-off keying, *VCO* voltage-controlled oscillator, *PA* power amplifier, *LP* low pass



not enough to prevent two patch antennas from overlapping in frequency responses. On the basis of the measured S11 of 20 dies from a single wafer, no missed alignment between two antennas was observed.

Frequency-Locked Loop

Figure 15 shows the block diagram of the 60-GHz FLL. The FLL mainly consists of two parts: a feed-forward RF part and a feedback baseband part. The RF part comprises a differential voltage-controlled oscillator (VCO), a buffered output of the VCO, a power amplifier (PA), and the on-chip patch antenna reference. The baseband part functions as a Proportional Integral (PI) controller, and has two envelope detectors, an error amplifier, an integrator, and a loop filter. The VCO signal is amplified by the PA and radiated through the antenna. The frequency of the VCO is

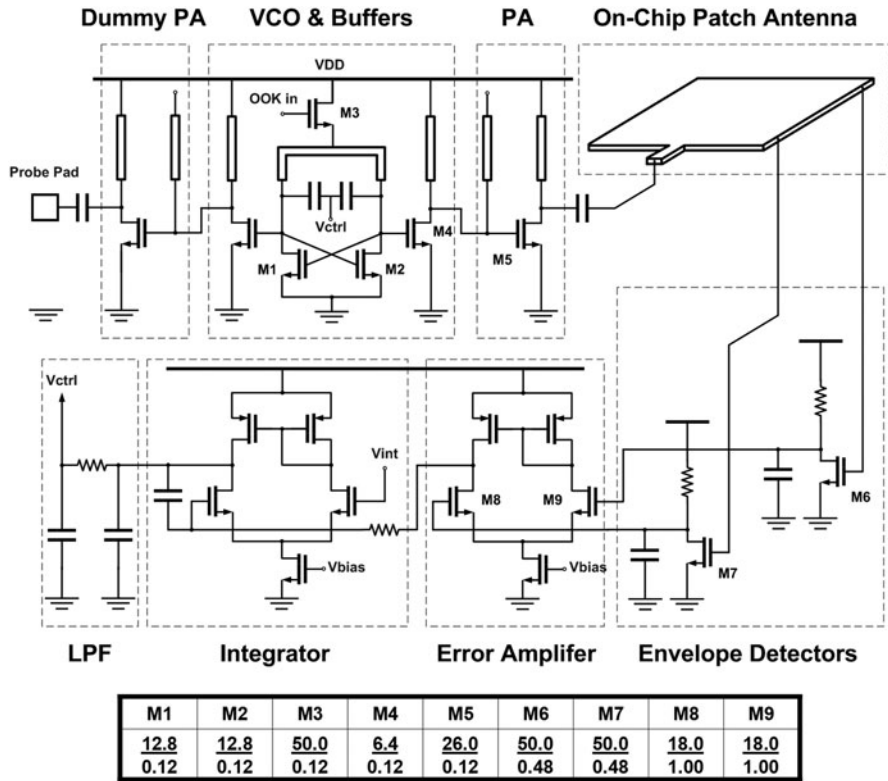


Fig. 16 Schematic of the 60-GHz frequency-locked loop (FLL). *VCO* voltage-controlled oscillator, *PA* power amplifier, *LPF* low-pass filter

regulated by the feedback baseband part. The VCO is designed to be on-off keying (OOK) modulated by power gating with a PMOS header device, so that the FLL can serve as a simple low-rate OOK transmitter. Note that the baseband circuits highlighted in Fig. 15 are placed beneath the patch antenna ground plane using Metal 1 to Metal 3 routing layers.

Figure 16 shows the schematic of the 60-GHz FLL. The VCO uses a cross-coupled pair topology with an LC resonator. The resonator is realized by a half-wavelength transmission line at the top metal layer, and the simulated Q-factor of the resonator is 15 at 60 GHz. The frequency tuning is achieved by a pair of thin oxide negative-channel metal-oxide semiconductor (NMOS) varactors. One of the differential VCO outputs feeds the signal onto the patch antenna through a common source stage buffer and a PA. The PA is designed for maximum power delivery, using the top metal layer for high-Q transmission lines for matching. Ideally, we want to probe the signal at the antenna input, where the FLL output is. However, the pad and probing might destroy the matching condition between the PA and the antenna, so the secondary output of the differential VCO is used for testing and is connected to an RF probe

Fig. 17 Tuning range of the voltage-controlled oscillator (VCO) in the frequency-locked loop (FLL)

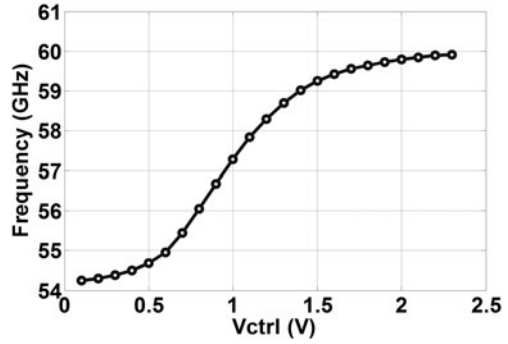
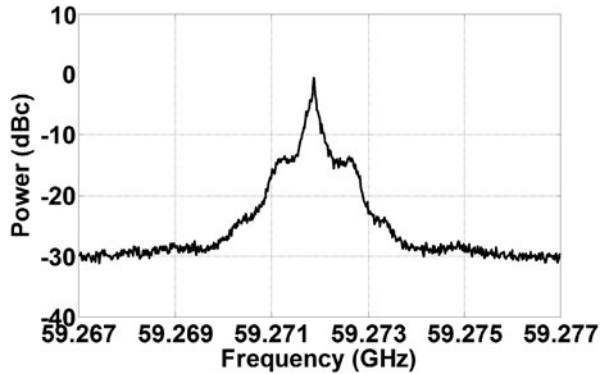


Fig. 18 Output spectrum of the frequency-locked loop (FLL) in 10-MHz span



pad through a dummy PA. In this way, we can monitor the FLL output frequency. However, the absolute output power is not available through direct measurement because of an extra 500 μm routing that is necessary for the on-chip probing pads setup. The simulated FLL output frequency and power are 60.12 GHz and -3.6 dBm, respectively. The measured power consumption of the VCO core, buffers, and PA are 8.8, 2.6, and 16.0 mW, respectively.

The envelope detectors sense the magnitude of the standing wave on the antenna, and down-convert the signal from 60 GHz to direct current (DC). An active envelope detector topology is used for larger output voltage levels, which is a class-AB biased amplifier with parallel resistor–capacitor (RC) load at the output [35]. The bias of the two envelope detectors is critical, and the connection through the patch antenna ensures the DC voltage at both gates of the envelope detectors are the same. The setup also makes sure that the patch antenna is not DC floating when it is operating. Moreover, large devices are used and they are laid out in close proximity to lower the mismatch between the two envelope detectors [34]. The simulated offset voltage of the envelope detector inputs due to process variation is 190 μV , corresponding to a frequency offset of roughly 6 MHz (100 ppm). By changing the bias gate voltage and the drain current, the input node of the envelope detectors can be designed as high-impedance nodes, so that the two taps on the edge of the patch antenna do not significantly affect the standing wave pattern. The measured power consumption of one envelope detector is 670 μW .

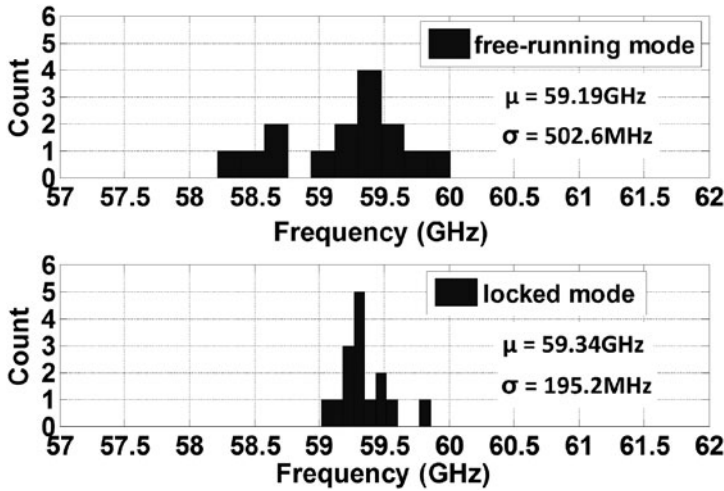


Fig. 19 Frequency distribution of the frequency-locked loop (FLL) in different modes

The error amplifier provides the difference and controller gain for the FLL. It is an amplifier with a differential input and an active load for single-ended output. Gain of 20 dB and bandwidth of 300-MHz bandwidth is obtained from this stage. The simulated offset voltage at the input of the error amplifier is 52 μ V, corresponding to a frequency offset of roughly 11 MHz. The integrator introduces a pole at DC, minimizing the steady state error between the FLL output and the natural resonant frequency of the patch antenna. Bias conditions of the error amplifier, envelope detectors, and the integrator must be considered together for the proper input voltage range and gain margin. The loop filter stabilizes the FLL and is realized by a distributed resistive transmission line with metal comb capacitor units with a self-resonant frequency above 60 GHz. The cutoff frequency of the loop filter is designed to be 100 MHz.

Measurement Results and Summary

The FLL is fabricated in a 130-nm CMOS process and the power consumption (excluding the dummy PA to test pads) is 29.6 mW. Figure 17 shows the tuning range of the VCO in the FLL, which covers $\pm 3\sigma$ of the patch antenna resonant frequency.

The output spectrum measured with a 10-MHz span while the FLL is locked is shown in Fig. 18. The locked frequency is at 59.27 GHz, which is within the variation of the replica antenna. There are no reference spurs in the output spectrum, which would typically appear in a frequency synthesizer with a crystal reference multiplied by a PLL [36]. Fifteen FLLs from a single wafer were tested, and Fig. 19 compares

Fig. 20 On-off keying (OOK) modulating the voltage-controlled oscillator (VCO) at 1 kbps

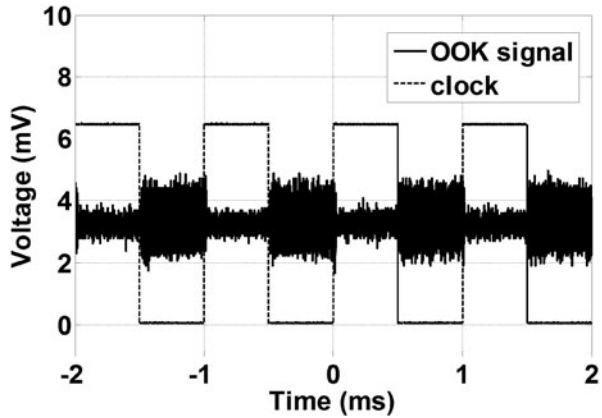
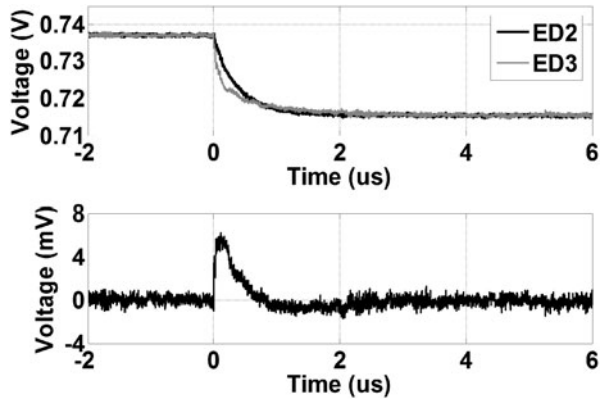


Fig. 21 Transient response of the two envelope detector outputs when turning the frequency-locked loop (FLL) on and the envelope outputs difference for settling time characterization



the frequency distribution of the free-running VCO when the feedback loop is off and when operating in locked mode. The mean center frequency is 59.34 GHz, with a standard deviation of 195 MHz. Compared with the 503-MHz standard deviation of the free-running VCO, the FLL provides an improvement in frequency variation, while eliminating the need for an external reference and tracking the peak-efficiency frequency of the integrated antenna.

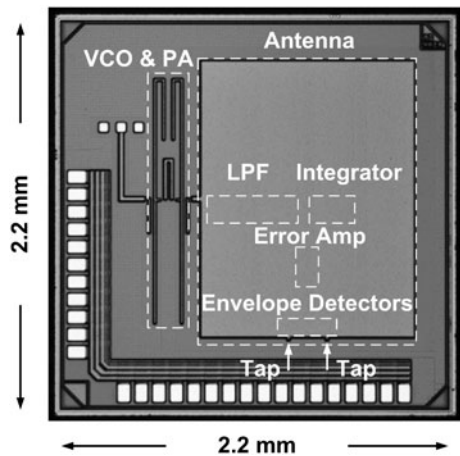
Figure 20 shows the FLL Tx signal when the VCO is being OOK modulated at 1 kbps. The signal amplitude is small because it is down-converted through a passive harmonic mixer which has an uncalibrated attenuation; therefore, this plot simply verifies the OOK functionality. Figure 21 shows the two envelope detector output signals when the FLL is OOK modulated and the difference of the two envelope detector outputs as the error signal. The settling time is around $3 \mu\text{s}$ once the loop is turned on; therefore, the VCO can be powered on and FLL locked during every bit transmission for data rates less than around 200 kbps. The measured results of the FLL are summarized in Table 2 and compared with a state-of-the-art PLL, frequency synthesizer, and OOK transmitter. While a frequency synthesizer requires a crystal

Table 2 FLL performance summary

Study	[37]	[38]	[39]	This work
Type	PLL	Frequency synthesizer	OOK Tx	FLL
Technology	90-nm CMOS	90-nm CMOS	90-nm CMOS	0.13- μ m CMOS
Power	80.0 mW	80.0 mW	183.0 mW	29.6 mW
Frequency	75 GHz	60 GHz	60 GHz	60 GHz
Antenna	N/A	N/A	Off-chip	On-chip
Area	0.80 mm ²	0.95 mm ²	0.43 mm ²	2.85 mm ²
Active circuit area	0.80 mm ²	0.95 mm ²	0.43 mm ²	0.64 mm ²

N/A not applicable, *PLL* phase-locked loop, *OOK* on-off keying, *FLL* frequency-locked loop, *CMOS* complementary metal-oxide semiconductor

Fig. 22 Die micrograph of the 60-GHz frequency-locked loop (FLL). *VCO* voltage-controlled oscillator, *PA* power amplifier, *LPF* low-pass filter



reference, this antenna-referenced FLL performs closed-loop frequency regulation without any off-chip components. A die micrograph of the FLL is shown in Fig. 22. The FLL including antenna occupies $1.60 \times 1.78 \text{ mm}^2$ without pads.

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