Chapter 7
Front End of the Line Process

Jeong Hwan Han, Moonju Cho, Annelies Delabie, Tae Joo Park and Cheol Seong Hwang

7.1 Introduction

The gate dielectric oxide plays a key role in the performance and reliability of Metal–Oxide–Semiconductor Field Effect Transistors (MOSFETs), a typical logic device in modern ultra large-scale integrated chips. The interface state density (N_{it}) and the charge trapping behavior at the interface between the gate dielectric film and a Si substrate determine the channel mobility degradation, threshold voltage (V_{TH}) instability, and life time of the device. SiO_2/Si gate stack fabricated by thermal oxidation of the Si substrate has provided the outstanding interface properties for several decades. However, the continuous scaling of the devices has driven the development of the alternative gate dielectric materials and processes. In recent years, atomic layer deposition (ALD) HfO_2-based gate dielectrics with a metal gate have been implemented in a mass production [1].

ALD of metal oxides is based on sequential self-limiting chemisorption reactions of a metal-containing precursor and an oxygen source [1, 2]. Both precursors affect the quality of high-k films as well as the interfacial layer (IL) at the interface with a substrate. Therefore, appropriate choice of metal precursor and oxygen source, and understanding of their reaction mechanisms on the various surfaces are important to obtain the promising performance and reliability of MOSFETs.

J. H. Han (✉) · M. Cho · A. Delabie
Imec, Kapeldreef 75, 3001 Leuven, Belgium
e-mail: hanj@imec.be

A. Delabie
Department of Chemistry, University of Leuven, Celestijnenlaan 200F, 3001 Leuven, Belgium

T. J. Park
Department of Materials Engineering, Hanyang University, Ansan 426-791, Korea

C. S. Hwang
Department of Materials Science and Engineering and Inter-university Semiconductor Research Center, Seoul National University, Seoul 151-744, Korea

C. S. Hwang (ed.), *Atomic Layer Deposition for Semiconductors*,
DOI: 10.1007/978-1-4614-8054-9_7,

Furthermore, evolutions of new channel materials (SiGe, Ge, and III–V compound semiconductors such as GaAs, InGaAs, GaSb, InP, etc.) [3, 4] and multi-dimensional devices including FinFETs or nanowire devices [5–7] further increased the importance of appropriate metal precursor and the oxygen source for the ALD process.

In this chapter, the ALD characteristics and properties of Hf-based high-k films from different types of metal precursors, such as $HfCl_4$, $Hf(N(C_2H_5)(CH_3))_4$, $(HfN(CH_3)_2)_4$, and $HfO^tBu(NEtMe)_3$ are compared, and the influences of oxygen sources type, H_2O and O_3, are discussed. The discussion covers the ALD high-k films on not only Si substrate but also the assorted alternative substrates such as Ge and III–Vs. Finally, the performance and reliability of the sub 1 nm equivalent-oxide-thickness (EOT) planar Si channel devices, SiGe- or III–Vs channel devices, and FinFET devices with HfO_2-based gate oxides grown by ALD are discussed in detail. In fact, there have been many studies of other high-k dielectrics, such as lanthanide-based oxides and ternary oxides, but dealing with all the other high-k layers than HfO_2 is not feasible for the given space of this chapter. However, this does not undermine the importance of other high-k and higher-k dielectrics for futuristic MOSFET devices.

7.2 Metal Precursor

7.2.1 Hafnium Chlorides ($HfCl_4$)

$HfCl_4$ has been the most commonly employed inorganic Hf precursor to fabricate HfO_2-based dielectrics because it has the advantages of smaller molecule size and high thermal stability (>600 °C) providing less steric hindrance and a wider temperature window for self-limited growth compared with the metal-organic (MO) Hf precursors. In addition, HfO_2 film from $HfCl_4$ is free from carbon contamination which might deteriorate the physical/chemical and electrical properties of HfO_2. HfO_2 ALD using $HfCl_4$ is typically performed in combination with either H_2O or O_3. In combination with H_2O as the oxygen source, the process demonstrates fluent ALD saturation behavior at the reactor temperatures between 200 and 600 °C.

For $HfCl_4/H_2O$ process, reaction pathway of ALD HfO_2 is explained by the ligand exchange reaction between $HfCl_4$ and surface hydroxyl (OH) groups, releasing HCl [8, 9]. Thus, the amount of OH groups existing on the surface can strongly influence the initial growth behavior as well as the steady-state growth. The steady-state growth per cycle of ALD HfO_2 films at the deposition temperatures of 200 and 400 °C are ~0.13 and ~0.044 nm/cycle, respectively, as shown in Fig. 7.1a [10]. Here, decrease in growth rate as increasing growth temperature is attributed to lower OH density on the film surface at higher reactor temperature [9–11]. Initial HfO_2 growth behavior is also very sensitive to the status of starting

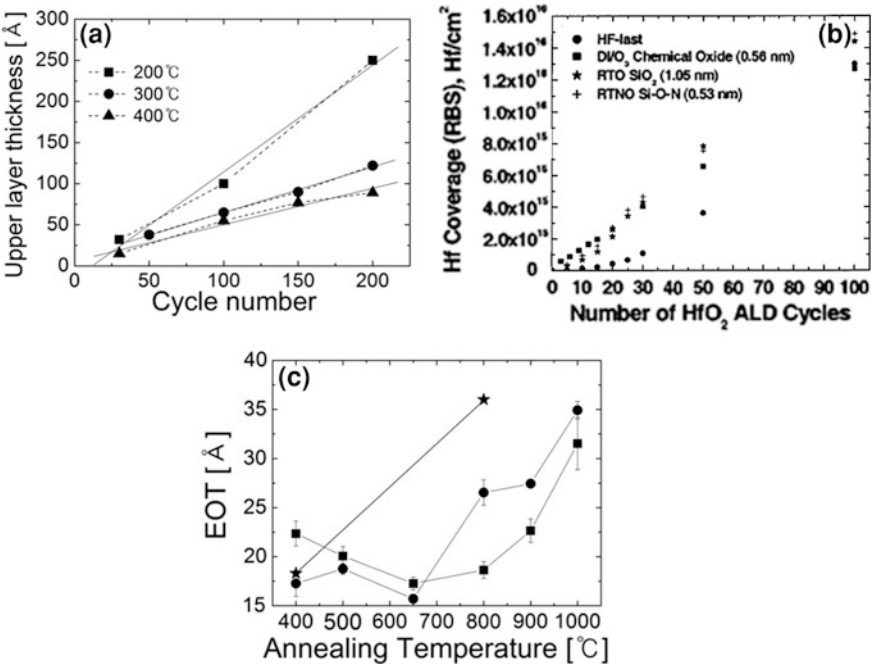

Fig. 7.1 (**a**) Change in the HfO_2 (*upper layer*) thicknesses as a function of the number of ALD cycles at the reactor temperatures from 200 to 400 °C [10]. (**b**) The Hf coverage as a function of the number of ALD $HfCl_4/H_2O$ cycles on the various substrates [12]. (**c**) The EOT of MIS stacks after PDA at the various temperatures. The HfO_2 films were deposited at the temperatures of 300 (*square symbol*) and 400 °C (*circle symbol*), respectively. *Star symbol* corresponds to HfO_2/Si stack without a RBL [15]

surfaces. Figure 7.1b showed the variation of Hf-coverage at the early growth stage with the number of ALD cycles on the variously prepared Si surfaces, such as chemical SiO_2, thermal SiO_2, and diluted HF-cleaned Si [12]. To achieve excellent EOT scalability of gate stack, thick interfacial low-k SiO_2 layer is unfavorable in spite of the improved initiation behavior of ALD on it. However, on HF-cleaned Si surface (H-terminated surface) an incubation period of ~20 cycles was observed, because of the lack of OH functional group, while linear growth behavior without the incubation step was exhibited on the chemical SiO_2 surface. H-terminated Si hinders nucleation of ALD HfO_2 resulting in rough, three-dimensional (3D), and nonlinear growth during first few ALD cycles due to the retarded chemisorptions of $HfCl_4$. Beyond the influence on the nucleation and growth rates of HfO_2 films, wafer temperature of ALD process affected the crystalline structure of resulting HfO_2 and thickness of the interfacial SiO_x layer which is formed between Si and HfO_2 layer during HfO_2 ALD process. The microstructure of HfO_2 films deposited on Si was investigated with varying the growth temperatures from 200 to 370 °C [13]. As-deposited HfO_2 film grown at

200 °C showed amorphous phase, whereas HfO_2 films grown at 300 and 370 °C appeared polycrystalline with monoclinic and tetragonal phases. With increasing post deposition annealing (PDA) temperature, the portion of tetragonal phase was decreased, resulting in the monoclinic-rich phase [13]. The formation of the interfacial layer (IL) is influenced by the process temperature of HfO_2 ALD, but PDA and pre-metal degas conditions play a critical role. Cho et al. [10] reported that an IL is spontaneously growing at all investigated growth temperatures ranging from 200 to 400 °C when ALD HfO_2 films using $HfCl_4/H_2O$ were deposited on the H-terminated Si. At 200 °C, thickness of the interfacial SiO_x layer increased with the increasing number of ALD HfO_2 cycles from 1.4 nm at 30 cycles to 5.5 nm at 200 cycles. However, IL thickness decreased as increasing growth temperature over 300 °C due to the dissolution of the IL into the growing HfO_2 layer. It was reported that the use of a pre-metallization degas improves EOT scaling [14]. The origin of the improvement is in the removal of H_2O from the high-*k* dielectric. Since HfO_2 is a poor diffusion barrier for H_2O, and H_2O is a strong oxidizer of silicon, H_2O adsorbed to the dielectric during air exposure can diffuse down to the silicon surface and contribute to interfacial layer regrowth during subsequent high temperature steps in the process. As a result, the interfacial oxide thickness and hence the EOT increases. For aggressive EOT scaling, it is therefore important to reduce the amount of H_2O released at temperatures where oxidation of the silicon is favorable.

In spite of thin IL layer of ~1–2 nm at the high growth temperatures of 300 or 400 °C, the low-k $HfSiO_x$ layer formed after PDA over 800 °C by intermixing of HfO_2 and SiO_x which increased the EOT.

To prevent the increase in EOT resulting from IL formation, a thin ALD Al_2O_3 layer was introduced as a reaction barrier layer (RBL) [15]. By interposing RBL, EOT increase of $HfO_2/Al_2O_3/SiO_2$ stack after PDA can be remarkably reduced indicating Si diffusion into HfO_2 layer is suppressed as shown in Fig. 7.1c. Although ALD Al_2O_3 films grown with either O_2 plasma or H_2O as oxygen source were adopted, Al_2O_3 layer from O_3 showed the best electrical properties regarding the charge injection, stability against flat band voltage (V_{FB}) shift, and increase in leakage current density due to stoichiometric O/Al composition originating from strong oxidation power of O_3. Al_2O_3 RBL, however, brings about high density of negative interfacial fixed charge between Al_2O_3 and SiO_2 which induces positive V_{FB} shift. Nitridation of RBL layer greatly improved the thermal stability of the capacitance–voltage (C–V) characteristics, providing ideal V_{FB} and very small hysteresis for HfO_2/Al_2O_3 stack [16]. As the N incorporation into the Al_2O_3 layer produced positive fixed charges, the negative fixed charges at Al_2O_3/SiO_2 could be compensated. Another way to optimize V_{FB} is the combination of the thicknesses of the Al_2O_3 and HfO_2 with an appropriate ratio which results in the ideal V_{FB} value because positive fixed charge at the HfO_2/Al_2O_3 interface can be compensated by the negatively fixed charge at Al_2O_3/SiO_2.

Unlike HfO_2 film deposited from MO precursors, effect of Cl residue in the HfO_2 on the electrical properties of HfO_2-based MOSFETs should be considered in case of $HfCl_4/H_2O$ process. Therefore, time-dependent dielectric breakdown

(TDDB) characteristics of HfO_2 films grown with different H_2O pulse time were examined [17]. Cl concentration in the deposited HfO_2 films is decreasing as increasing H_2O pulse time from 0.3 to 90 s. It was found that one order higher magnitude of Cl concentration does not exacerbate the TDDB characteristic of the film. Furthermore, first-principles calculation proved that additional trap energy level is not formed inside the HfO_2 band gap when Cl content of HfO_2 film increases.

As MOSFET on high-mobility channels such as Ge and III–V compound semiconductors would offer significant improvements in the electrical performances over Si-based MOSFET, ALD HfO_2 on Ge, GaAs, and InGaAs substrates has obtained intensive interests [18–20]. ALD HfO_2 on HF-cleaned Ge surface was investigated using $HfCl_4$ and H_2O. The available reaction sites existing on HF-cleaned Ge for $HfCl_4$ chemisorptions are OH groups and possibly also oxygen bridges (Ge–O–Ge). These remain present on the Ge surface after HF-cleaning, in contrast to Si surfaces, which provide Si–H termination which is a poor reaction site for chemisorptions of $HfCl_4$. HF-cleaned Ge is, therefore, a more favorable surface for initiation of HfO_2 film than HF-cleaned Si. For this reason, substrate-enhanced ALD HfO_2 growth was obtained at 300 °C for first a few ALD cycles on Ge surface. The steady-state growth rate is $\sim$0.04 nm/cycle which is comparable with that on Si. The optimized growth condition allowed promising scalability of HfO_2/Ge stack with thin interfacial GeO_2 layer ($< \sim$0.4 nm) and uniform/smooth HfO_2 film which was as thin as 1.6 nm [18]. In contrast, additional oxidation of Ge occurred when O_3 was employed as the oxygen source in $HfCl_4$-based ALD process [21]. HfO_2 ALD process with $HfCl_4/O_3$ induces thicker interfacial GeO_2 compared to HfO_2 ALD from $HfCl_4/H_2O$. Interestingly, an even thinner IL was formed during Al_2O_3 ALD process from trimethylaluminum (TMA)/O_3 on HF-cleaned Ge than $HfCl_4/O_3$ process. This is related to the difference in required O_3 pulse time for ALD saturation according to the types of metal precursor. ALD process using $HfCl_4$ precursor requires higher O_3 dose than other processes using MO precursor due to strong Hf–Cl bond. Change in the thickness of interfacial GeO_2 layer before and after ALD of HfO_2 and Al_2O_3 films on 1 nm-thick GeO_2 and HF-cleaned Ge is summarized in Fig. 7.2a.

Ge channel layer, however, has still suffered from inadequate interface properties with high-k oxide due to the high electrically active N_{it} originating from the lack of stable passivating native oxide in contrast to Si channel. In the case of Ge substrate, the volatilization and desorption of GeO from the interfacial GeO_2 layer [as described by $GeO_2 + Ge \rightarrow 2GeO(g)$] occurs at rather low temperatures ($\sim$400 °C) and leaves a large amount of interface states and charge trapping sites [22, 23]. This can be suppressed using the high-k materials to form a stable germanate such as La_2O_3, ZrO_2, Y_2O_3, etc., [22, 24–29] or the interfacial reaction barriers by various surface treatments [30–39]. Prior to high-k deposition, therefore, surface nitridation, oxidation, or sulfur (S) treatments have been performed on Ge to reduce N_{it} by passivating the defective sites on surface [37–39] Among them, effect of S-passivation of the Ge channel using $(NH_4)_2S$ on the interface quality of HfO_2/S/Ge stack deserves detailed explanation due to its high

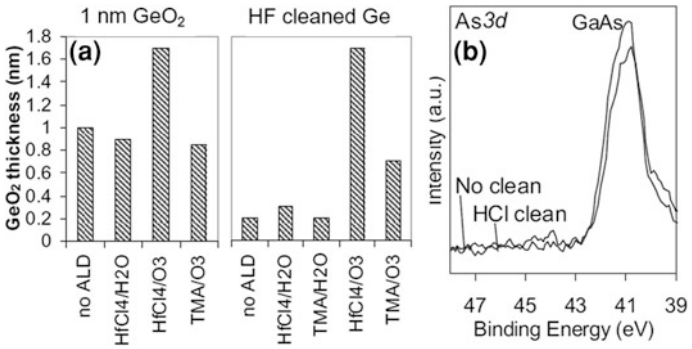

Fig. 7.2 (**a**) Thickness of GeO_2 layer before and after ALD of 2 nm thick HfO_2 or Al_2O_3 on 1 nm thick GeO_2 and HF-cleaned Ge [21]. (**b**) XP spectra of As 3d after 40 cycles $HfCl_4/H_2O$ process on GaAs with native oxide and HCl-cleaned GaAs [19]

effectiveness [39]. When the Ge surface is treated with $(NH_4)_2S$ prior to ALD HfO_2 or ALD Al_2O_3, interfaces between high-k oxides and Ge channel show improved IL properties that is free from defective GeO_x, suggesting S-treatment is very promising for EOT scaling as well as interfacial quality. Nevertheless, the midgap N_{it} of $10^{13}/cm^2$-eV for HfO_2/S-treated Ge is not sufficiently low compared to N_{it} for Al_2O_3/S-treated Ge. Therefore, bi-layer of HfO_2/Al_2O_3 was fabricated to reduce N_{it} and EOT. Consequently, high mobility of >200 cm^2/Vs at an EOT of 1.5 nm was obtained using 2 nm-HfO_2/2 nm Al_2O_3/S-treated Ge stack.

Another important channel material for future CMOS is III–V compound semiconductors, such as GaAs, InGaAs, etc., because of its higher carrier mobility even though their density of states is lower compared with Si. Initial reaction of $HfCl_4$ on GaAs substrate is quite different from that of Ge. ALD HfO_2 growth using $HfCl_4$ and H_2O was performed on native GaAs oxide and HCl-cleaned GaAs [19]. Here, "self-cleaning" of native oxide of GaAs was observed during the early growth stage. In X-ray photoelectron spectroscopy (XPS) of Fig. 7.2b, as 3d spectra corresponding to AsO_x native oxide disappeared after ALD $HfCl_4/H_2O$ process indicating that interfacial "self-cleaning" occurred. When an ALD HfO_2 process using tetrakis[diethylamino]hafnium (TDEAH, $Hf(N(C_2H_5)_2)_4$) precursor was employed to fabricate HfO_2 film on GaAs surface, the self-cleaning of IL was not found. On the other hand, Chang et al. [40] reported the removal of native AsO_x on InGaAs during HfO_2 deposition using tetrakis[ethylmethylamino]hafnium (TEMAH, $(HfN(C_2H_5)(CH_3))_4$). The "self-cleaning" of GaAs native oxide was also achieved from ALD Al_2O_3 growth where TMA and H_2O precursors are used [41–43]. These results suggest that the reduction of IL on III–V channel is strongly related to not only process parameters but also the types of metal precursors, emphasizing the importance of appropriate selection of metal precursor for native oxide free interface.

7.2.2 Metal–Organic Precursors

In spite of many advantages of $HfCl_4$ precursor mentioned in the previous section, the low reactivity and low vapor pressure of $HfCl_4$ lead to undesired growth behavior and film properties such as high substrate-dependent growth, low growth rate, and presence of Cl residue. Furthermore, formation of the HCl by-product might result in film etching as well as corrosion of reactor wall and increases the risk of failure of abatement system. Therefore, ALD growth of HfO_2 film from MO precursors has been investigated for achieving better growth characteristics and more ALD-hardware-friendly growth conditions. Hf–amide and Hf–alkoxide compounds are the most widely used among a wide variety of MO Hf precursors. In this section, growth behaviors and properties of ALD HfO_2 film from MO precursors are described.

7.2.2.1 Tetrakis[ethylmethylamino]hafnium ($Hf(N(C_2H_5)(CH_3))_4$, TEMAH) and Tetrakis[dimethylamino]hafnium ($Hf(N(CH_3)_2)_4$, TDMAH)

The nucleation behavior of ALD HfO_2 using TEMAH precursor is less dependent on the types of starting surfaces due to its higher reactivity as compared to the $HfCl_4$ precursor. The metal-nitrogen bond of the amide precursors such as Hf–N has relatively weak bond strength compared to metal-halide bond. Figure 7.3a showed the number of Hf atom on chemical SiO_2 and HF-cleaned Si as a function of the number of ALD TEMAH/H_2O cycles [44]. Although there are small incubation cycles on HF-cleaned Si, relatively less substrate dependency of initial behavior were obtained compared to $HfCl_4/H_2O$ ALD process shown in Fig. 7.1b. This allowed smoother surface morphology even on low-OH containing surface.

Influences of the growth temperature on the resulting HfO_2 properties were investigated on Si and Ge substrates using TEMAH and O_3 at the growth temperatures ranging from 160 to 360 °C [45]. Because of limited thermal stability of TEMAH precursor, high impurity concentration, too high growth rate, and non-uniformity of HfO_2 film were resulted in when the deposition temperature is over 300 °C due to thermal decomposition of Hf precursor (Fig. 7.3b). Growth rate of ALD HfO_2 at 160 °C is $\sim$0.12 nm/cycle and decreases with increasing growth temperature to 280 °C indicating that the density of reaction sites decreases with increasing growth temperature, whereas film density increases with temperature, and saturated at 280 °C. Generally, lower growth temperature induces higher C impurity in the film which adversely affects the physical/electrical properties of the film. Jung et al. [46] reported the effects of the C concentration on the dielectric property and leakage current density of HfO_2. Crystalline structure of HfO_2 film grown at 200 °C showed a tetragonal phase after PDA at 600 °C which has higher dielectric constant than amorphous and monoclinic phase. The residual C can stabilize the tetragonal phase because defects induced by C impurity lower the

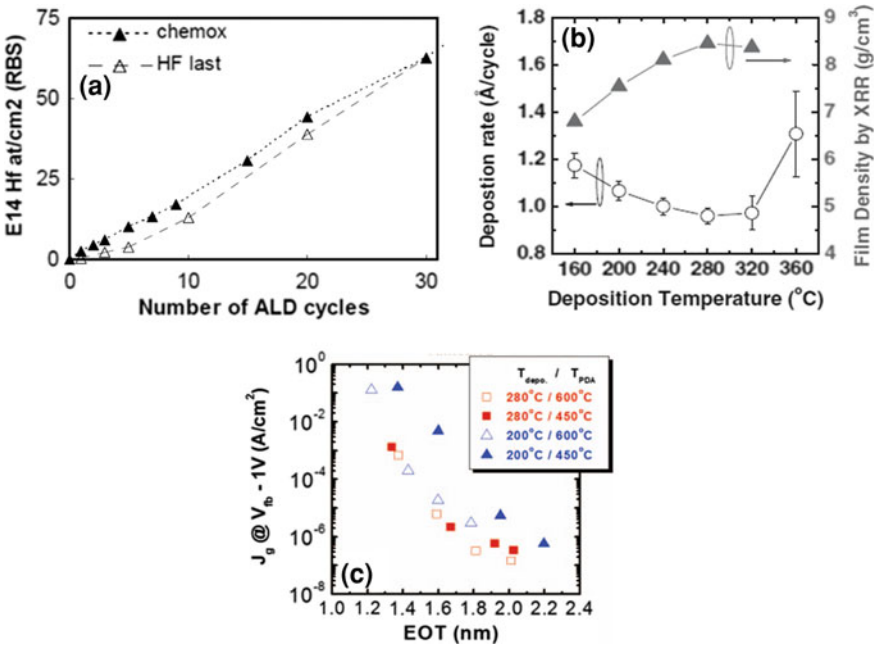

Fig. 7.3 (**a**) Hf coverage as a function of the number of ALD TEMAH/H_2O cycles on the chemical SiO_2 and HF-cleaned Si [44]. (**b**) Variations in the growth and film density of ALD HfO_2 films on Si as a function of deposition temperature [45]. (**c**) Variations in the leakage current density (at a voltage of V_{FB}—1 V) as a function of EOT of the HfO_2 films grown at 200 and 280 °C after PDA at 450 and 600 °C [46]

phase transition energy from monoclinic to tetragonal. However, gain on the dielectric performance with low process temperature is nullified by deteriorated leakage current property of HfO_2. Figure 7.3c showed the changes in the leakage current density as a function of EOT of HfO_2 film grown at 200 and 280 °C. Although HfO_2 film deposited at low temperature (200 °C) showed higher dielectric constant (and thus lower EOT), no improvement in gate current density-EOT (J_g-EOT) curve was found.

To obtain EOT of sub 1 nm on Ge channel, TiO_2/HfO_2 gate stacks was implemented on ultra-thin GeO_2 which is formed by O_2 plasma treatment prior to ALD high-k process [47]. HfO_2 film is deposited with TEMAH and O_2 plasma. Presence of stable and uniform GeO_2 IL prevents intermixing of HfO_2 and Ge during ALD HfO_2 process and resulted in significantly reduced hysteresis of <30 mV, whereas C–V hysteresis of 900 mV was achieved without GeO_2 passivation layer. Furthermore, very low interfacial trap density of $N_{it} \sim 5 \times 10^{11}$ eV^{-1} cm^{-2} indicates HfO_2/GeO_2 provides high interface quality for high-k TiO_2 on Ge channel. Finally, an EOT of 0.9 nm with low leakage current of 2×10^{-7} A/cm^2 at $V_{FB} \pm 1$ V was achieved for TiO_2(3 nm)/HfO_2(1.2 nm)/GeO_2(0.7 nm)/Ge capacitor.

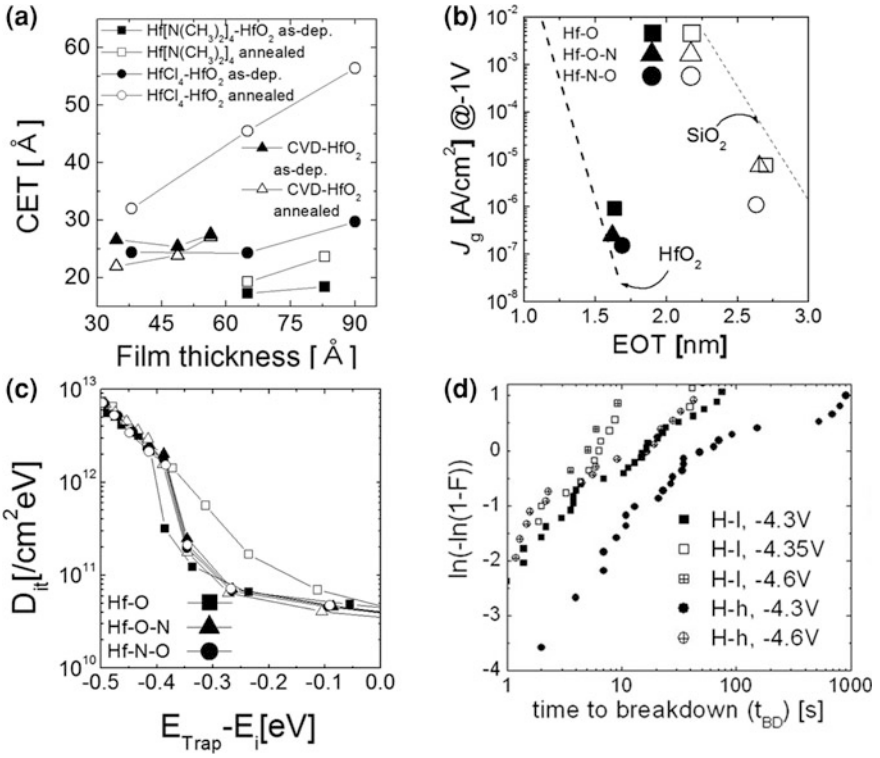

Fig. 7.4 (**a**) Variations in the capacitance equivalent thickness (CET) of the HfO_2 films grown from the $Hf[N(CH_3)_2]_4$ and $HfCl_4$ precursors, respectively, after PDA as a function of the physical thickness. The CVD HfO_2 film data were also included for comparison [48]. (**b**) The leakage current density as a function of EOT for Hf–O, Hf–O–N, and Hf–N–O films. The *filled* and *open symbols* correspond to before and after PDA, respectively [49]. (**c**) The variations in N_{it} as a function of E_{trap}-E_i before (*closed*) and after (*open*) CVS (5 MV/cm, 300 s) [49]. (**d**) Weibull distribution from TDDB analysis deposited as H–h and H–l samples [50]

HfO_2 films were also grown by ALD using Tetrakis[dimethylamino]hafnium ($(HfN(CH_3)_2)_4$, TDMAH) and H_2O at 300 °C. TDMAH precursor belongs to amide precursor group like as TEMAH. The growth rate of HfO_2 film from TDMAH was 0.078 nm/cycle and less substrate-dependent initial growth was observed compared to $HfCl_4/H_2O$ process [48]. As TDMAH contains nitrogen atoms in the precursor, SiN_x layer was simultaneously formed on Si during HfO_2 deposition. It was found that this spontaneously formed SiN_x layer that plays a role as a RBL which prevents diffusion of Si into the HfO_2. Figure 7.4a showed the variations in the EOTs of the TDMAH-HfO_2 film and $HfCl_4$-HfO_2 film after PDA as a function of the physical HfO_2 thickness. Interestingly, the increase in the EOT of HfO_2 film after PDA is much smaller for the TDMAH-HfO_2 than $HfCl_4$-HfO_2 film due to suppression of Si diffusion into HfO_2 by the SiN_x RBL.

To effectively incorporate N into the HfO_2 and IL layers for obtaining better electrical properties of metal–oxide–semiconductor capacitor (MOSCAP), modified ALD HfO_2 processes with in situ NH_3 injection, where the sequence of TDMAH/purge-NH_3/purge-H_2O/purge (Hf–N–O) or TDMAH/purge-H_2O/purge-NH_3/purge (Hf–O–N) was adopted, were demonstrated [49]. Interfacial SiN_x layer is formed at the HfO_2/Si interface for both HfO_2 ALD processes. The in situ NH_3 pulse leads to reduced C and increased N contents in the HfO_2 and IL layers compared to conventional ALD HfO_2 (Hf–O). Decreased C concentration might be ascribed to enhanced desorption of C by NH_3 injection. Figure 7.4b showed the J_g-EOT curve of Hf–O, Hf–O–N, and Hf–N–O samples before and after PDA. The leakage current density of HfO_2 film was improved by NH_3 injection. This might be attributed to the formation of SiN_x IL and the lower density of electrical defects induced by C residue. The variation in the N_{it} was measured by the conductance method before and after constant-voltage stress (CVS) at 5 MV/cm. Figure 7.4c showed that larger degradation in the N_{it} was observed after CVS in case of the HfO_2 film without NH_3 injection compared to in case of the HfO_2 film with NH_3 injection. It is believed that SiN_x IL suppresses the degradations of N_{it}. The effect of C impurity concentration on the reliability of HfO_2 was also examined by varying concentration of O_3 to make HfO_2 films with different C concentration [50]. Figure 7.4d shows Weibull distribution from TDDB analysis for HfO_2 films from high O_3 concentration (H–h) and low O_3 concentration (H–l). The films grown with higher O_3 concentration has a lower amount of C residue. It was confirmed that C impurity in the HfO_2 film produces deep acceptor-like trap states in the band gap, and results in inferior leakage current and poor TDDB properties.

7.2.2.2 Tert-butoxytris[ethylmethylamido]hafnium ($HfO^tBu(NEtMe)_3$, BTEMAH)

In this section, the growth behavior and electrical properties of ALD HfO_2 film deposited using heteroleptic tert-butoxytris(ethylmethylamido)hafnium (BTEMAH) precursor and O_3 at a deposition temperature of 300 °C are described [51]. The structure of BTEMAH is slightly modified from that of TEMAH precursor by replacing one of four amido ligands in TEMAH with a tert-buthoxy ligand. This buthoxy ligand largely increases the volatility and reactivity of Hf precursor which results in not only improved growth rate (0.16 nm/cycle) but also 20 % higher Hf density of the HfO_2 film compared with the HfO_2 film grown with TDMAH precursor. Higher Hf density induces more amorphous-like nature of HfO_2 film and the amorphous phase at the as-deposited state is maintained up to $\sim$15 nm while it changes to crystalline (monoclinic) phase at $< \sim$10 nm for TDMAH (or TEMAH) case. Changes in the microstructure of HfO_2 and thickness of IL between Si and HfO_2 are observed by high-resolution transmission electron microscopy (HRTEM) in comparison with the TDMAH HfO_2 film (Fig. 7.5). After PDA at 700 °C, HfO_2 from BTEMAH remains amorphous phase while HfO_2 film from TDMAH is fully crystallized. Both HfO_2 films are crystallized after

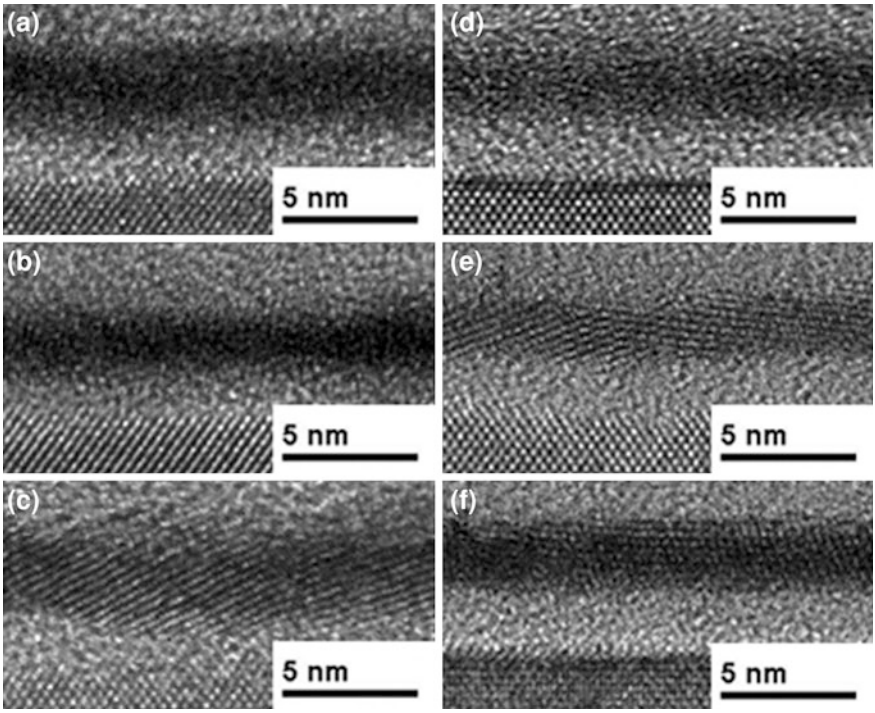

Fig. 7.5 HRTEM images of HfO_2 films grown on Si from the BTEMAH precursor (**a**) in the as-deposited state, and after annealing at (**b**) 700 °C and (**c**) 1,000 °C. (**d–f**) show the corresponding films from TDMAH [51]

PDA at 1,000 °C. It should be noted that thicknesses of interfacial SiO_2 layers are different according to the types of Hf precursor. The thickness of IL layer for BTEMAH-HfO_2 is thinner than that for TDMAH-HfO_2, and there is significantly smaller increase in the thickness of IL after annealing up to 1,000 °C in the case of BTEMAH which might be attributed to higher density of HfO_2 film grown from BTEMAH.

7.3 Oxygen Sources

7.3.1 Effect of Oxygen Source on Properties of ALD High-k Films on Si

The type of oxygen source crucially affects the various properties of ALD high-k metal-oxide films for the give n metal precursor. From the early stages of the ALD process development, H_2O has been extensively used as an oxygen source which

provides near-perfect ALD reaction (ligand exchange). This can be most typically observed from the ALD of Al_2O_3 films using TMA as the Al-precursor. As various metal precursors have been developed for more stable and efficient ALD process, another oxygen source than H_2O, such as O_3, NO_2 and H_2O_2 has been required for the better reactivity because they also functions as a reaction agent which removes or exchanges the ligand molecules in the metal precursor during ALD reaction [52, 53]. However, the understanding of the detailed chemical reaction routes for ALD processes is limited. The well-known chemical reactions between TMA and H_2O, and diethylzinc and H_2O are two examples for the well-understood ALD mechanisms. Nevertheless, it seems that the detailed chemical reaction mechanism of oxygen source during ALD is directly related with the physical density and the impurities level of the film, which determine the electrical properties of the ALD high-k film such as the permittivity and gate leakage current density. In addition, interface properties of the ALD high-k films with a substrate are also greatly influenced by the oxygen source, because the surface reaction of the oxygen source with a substrate in the initial stage of the film growth determines the IL growth, nucleation behavior, incubation time (cycle), etc. H_2O and the representative alternative, O_3 as an oxygen source for ALD high-k film process on Si are mainly discussed in this section.

The growth rate is one of the most important physical factors for the ALD process, which is influenced by the oxygen source as well as the metal precursor. In general, O_3 provides the higher growth rate of the ALD high-k film due to the stronger oxidation power and higher reactivity compared to H_2O, which diminishes the steric hindrance effect originating from the incompletely reacted ligand molecules during the surface reaction. Liu et al. reported the higher growth rate of ALD HfO_2 film using TEMAH with O_3 than H_2O as shown in Fig. 7.6a. Similar results have been reported for the cases with other precursors [54–59]. However, it also depends on the process conditions such as the chemical structure of the metal precursor, deposition temperature, etc. [60, 61].

The residual impurities in ALD high-k films are unavoidable, because it is either difficult to remove perfectly the ligand molecules in the metal precursor or

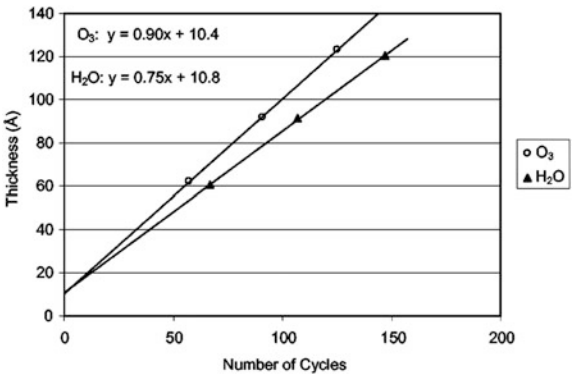

Fig. 7.6 Thickness of ALD Al_2O_3 film grown using TMA with H_2O and O_3 as an oxygen source as a function of the number of cycles. The slope in the fitting equation is the deposition rate, and the intercept is the thickness of the native oxide of the Si wafer [56]

to avoid the incorporation of by-product gas molecules into the film during ALD process. The device performance and reliability could be significantly deteriorated by the residual impurities in the gate dielectric high-k film, even in minute quantities, because the impurities can act as active electrical defects during device operation. In addition, too high impurity concentrations result in a lower physical density of the film, which can enhance the interfacial reactions with a Si substrate such as inter-mixing and Si out-diffusion [62]. In general, the concentration of residual impurities from the precursor molecules, such as Cl, C, H, N, etc., can be decreased by adopting O_3 due to the higher reactivity and stronger oxidation power compared with H_2O [62–64]. Park et al. recently reported the O_3 in ALD process largely decreased the C- and N-related residual impurities in La_2O_3 high-k film compared to H_2O, which was observed by high-resolution in situ XPS at the each half-ALD cycle as shown in C 1s core level spectra of Fig. 7.7a, b. While the residual impurities such as C–N, C–O, C–H, and C–O–H were accumulated with

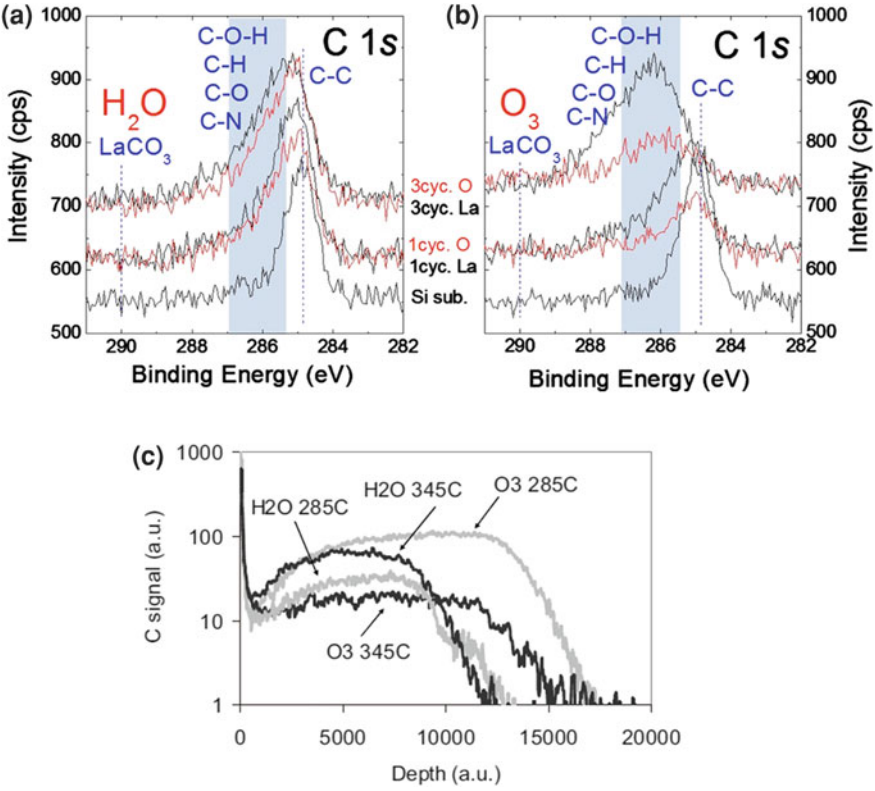

Fig. 7.7 C 1s core level XPS spectra of the ALD La_2O_3 films grown on Si using Tris(N,N′-diisopropylformamidinato)lanthanum with (**a**) H_2O and (**b**) O_3 for first and third ALD half-cycles [62]. (**c**) TOF–SIMS depth profiles of the C impurities in 10 nm thick ALD HfO_2 films grown using TEMAH with H_2O and O_3 at low and higher temperatures [55]

increasing ALD cycle number from 1 to 3 cycle in H_2O process (Fig. 7.7a), the accumulated impurities were removed considerably at each O_3 pulse in O_3 process as indicated in red (Fig. 7.7b). Therefore, O_3 with a higher concentration was even more effective to decrease the impurity level, which improved the reliability of the high-k films, such as breakdown voltage (time-zero dielectric breakdown, TZDB) and TDDB [63, 65–68]. However, it also depends on the process conditions such as the feeding time and purging time of oxygen source, process temperature, etc. The different temperature dependence of C impurity between O_3 and H_2O was reported for HfO_2 ALD using TEMAH, whereas the O_3 process effectively decreased the C concentration in the ALD high-k film grown at 345 °C compared to H_2O process, but it result in a higher C concentration in the film grown at 285 °C as shown in Fig. 7.7c [55, 56]. The lower impurity concentration and higher physical density of the ALD high-k film grown using O_3 results in the higher permittivity and higher breakdown voltage (field) compared to H_2O process [63, 64, 69–73]. Nevertheless, there are several other reports revealing the reversed trend making this issue still somewhat controversial [54, 55, 65, 66].

Interfacial reactions such as initial oxidation of a Si substrate and the intermixing of the related elements by diffusion-out of Si from a substrate are inevitable during the ALD film growth and various post-deposition processes. Especially, the initial oxidation of a Si substrate affects even the crystallinity of the film bulk as well as IL formation. Figure 7.8a showed the comparisons in the initial growth behavior of ALD HfO_2 on various substrates using either H_2O or O_3 as the oxygen source. While H_2O process on the HF-last Si substrate induces the long incubation time (or cycle) and the island-type film growth due to a lack of the reactive sites, O_3 process forms a thin surface SiO_2 layer during the initial stages of ALD film growth to induce a more 2D growth without incubation time. As a result, the larger grain size and flat surface with thicker IL were observed in the ALD high-k film grown with O_3 compared to H_2O as shown in the HRTEM image of Fig. 7.8c [54, 64]. However, the thicker IL of the film grown using O_3 is the critical drawback with respect to the scaling of EOT of the film.

The initial oxidation status of a Si surface during ALD process, which is mainly determined by the oxygen source, influences significantly the N_{it} of the high-k film affecting the carrier mobility in the MOSFETs. This results in a very delicate balance, because the improvement in N_{it} can be achieved not only by the thicker IL in O_3 process (more SiO_2/Si-like interface), but also by H-passivation at the interface with Si in H_2O process [74, 75]. However, it seems obvious that the severe interfacial oxidation by O_3 with a high concentration deteriorates the N_{it}, because the excess concentration of oxygen in the film grown in a higher O_3 concentration induced excess bonding with interfacial Si so as to decrease the thickness of interfacial sub-oxide (SiO_{2-x}) releasing the interfacial stress [65, 66, 74]. Moreover, the influence of oxygen source on the fixed charge and charge trap density of the ALD high-k film causing the V_{FB} shift and hysteresis, respectively, heavily depends on the process conditions.

The diffusion-out of Si from a substrate degrades the permittivity, device reliability, and interface properties of the ALD high-k film. While the thicker IL

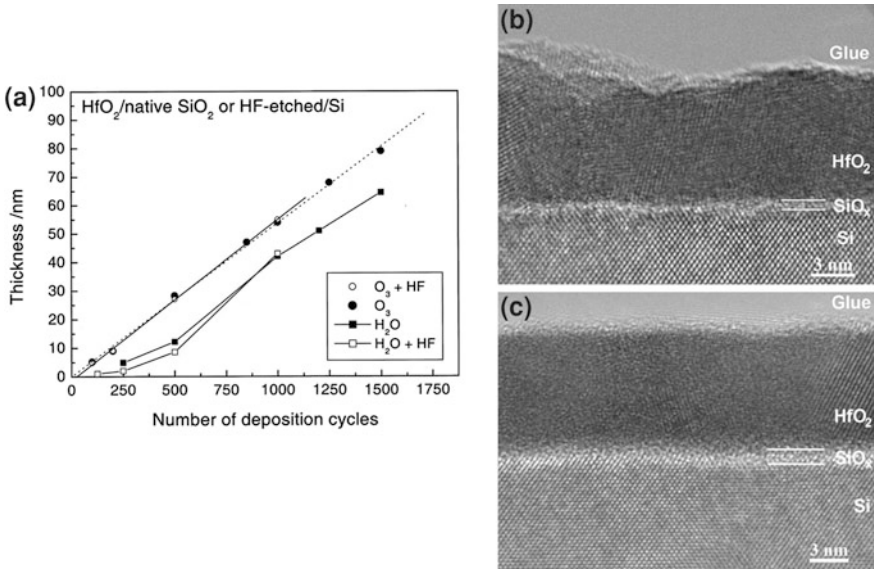

Fig. 7.8 (**a**) The thickness of ALD HfO_2 film using $Cp_2Hf(CH_3)_2$ with H_2O and O_3 as a function of the number of cycles. HF indicates a surface pretreatment with HF etching. Otherwise, the films were deposited on Si covered by native oxide. Linear fitting curves are provided when ozone was used. The deposition temperature was 350 °C. Cross-sectional HRTEM images of HfO_2 films grown on HF-etched Si(100) using (**b**) H_2O and (**c**) O_3 as oxygen source [54]

grown during ALD using O_3 decreases the permittivity of the film compared to H_2O, it plays as a good diffusion barrier for Si diffusion-out from a substrate during PDA [76]. Hence, the very thin SiO_2 can be intentionally grown with various methods prior to the ALD high-k film growth for achieving the thermal stability of the film.

Consequently, O_3-process provides the better physical properties as well as the related electrical properties of the ALD high-k film on Si compared to H_2O. However, identifying the various aspects of the O_3-process for high-k deposition including the structural and chemical changes occurring during the whole CMOSFET fabrication processes requires further study.

7.3.2 Effect of Oxygen Source on Interface Properties of ALD High-k Films on Ge and III–Vs

While the alternative substrates such as Ge and III–V compound semiconductors provide the enhanced device performances due to their high intrinsic carrier mobilities, the reliabilities such as V_{TH} instability, TDDB, etc., were deteriorated compared to the Si-based devices. This is because the interface properties of ALD

high-k film/substrate are degraded, partly by complicated interfacial reactions during ALD process of high-k films resulting in the high N_{it} and high density of the charge trapping sites near the interface. Therefore, the interfacial reactions between the ALD high-k film and Ge or III–V compound semiconductors occurred during ALD and the post-deposition processes should be carefully controlled. On the other hand, the bulk properties of the high-k films were reported similar with those of the film grown on a Si substrate [77].

In the case of Ge substrates, the oxygen-deficient GeO_x IL deteriorates the interface properties as mentioned in the preceding sections [22, 23]. Therefore, regarding the oxygen source, the understanding of the properties of IL grown simultaneously on a Ge substrate during ALD process of high-k film is most important [77]. Figure 7.9 shows the cross-sectional HRTEM image of ALD HfO_2 film grown with (Fig. 7.9a, b) H_2O and (Fig. 7.9c, d) O_3 on Ge substrate [78]. While HfO_2 film grown with O_3 has flat HfO_2 film and uniform IL, that is grown with H_2O is locally in direct contact with the Ge substrate and has very thin non-uniform IL resulting in the rough surface. This is similar with the ALD film grown with H_2O on a Si substrate but more serious, because the suppressed (negligible) GeO_2 IL growth compared to SiO_2 [21, 79]. Therefore, the high-k film grown with O_3 shows the higher EOT than that grown with H_2O due to the thicker IL, but the N_{it} is obviously lower for O_3 process than H_2O process [78, 80], which is quite different from the case of Si substrate. It was also reported that the band gap energy of the interfacial GeO_2 layer grown during H_2O-based ALD process ($\sim$4.3 eV) is lower than that during O_3-based ALD process ($\sim$5.7 eV) due to the incorporated hydroxyl group, which would affect the gate leakage current density through the film and charge trapping characteristics of the device [78, 81–83].

The interfacial reactions at the interface between ALD high-k film and III–V substrates, such as GaAs, InGaAs, InAs, etc., are even more complicated as compared to Ge substrate because the selective oxidation and reduction of the substrate elements and the volatile group V oxides induces the high N_{it} in the band gap energy of semiconductor. Although the "self-cleaning" of IL on III–Vs by ALD process was reported [84–87], the interfacial reaction is still a key restriction for the adoption of III–Vs because even the tiny quantity of elemental As, specific Ga oxidation state, etc., at the interface deteriorates significantly the interface

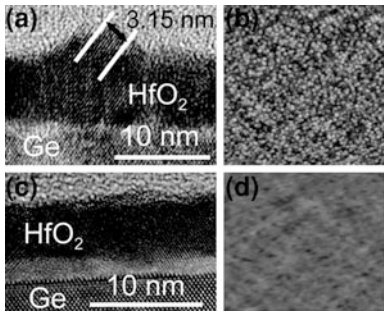

Fig. 7.9 Cross-sectional HRTEM images and corresponding AFM surface morphology of HfO_2 films grown using $HfCl_4$ with (**a**) and (**b**) H_2O and (**c**) and (**d**) O_3 as oxygen sources [78]

properties [88–91]. Many surface passivation (or cleaning) methods using various chemicals, such as H_2SO_4, HCl, HF, NH_4OH, H_2O_2, H, $(NH_4)_2Sx$, Na_2S, H_2S, etc., along with ALD process [92–105], hardly provide the sufficient improvement in the interface properties. The interfacial RBL such as Si and Ge grown by various methods suppressed interfacial reaction efficiently, but this buried channel structure has an EOT scaling limit of the gate dielectrics [106–111].

Although "self-cleaning" [84–87] during ALD of high-k film suggests the reactivity of the metal precursor affects the interfacial reaction at high-k/III–V substrate, the oxygen source mainly determines the interfacial reaction. H_2O has been popular oxygen source for ALD of high-k on III–Vs because it minimizes the interfacial reaction (thinner IL) during ALD compared to O_3 [112]. In situ XPS study by Brenan et al. revealed that ALD Al_2O_3 grown using O_3 induced the thick IL with a high oxidation state (As^{5+}) on $In_{0.53}Ga_{0.47}As$ substrate, which was hardly eliminated by self-cleaning effect of TMA pulse [113]. The thick IL formed by O_3 generated the larger amount of elemental As and Ga-oxide at the interface than the case of H_2O, which degraded the electrical properties including interface property [113]. Madan et al. also reported that ALD Al_2O_3 process using O_3 resulted the 1.5 time higher N_{it} and an order of magnitude higher capture cross section of the midgap trap at the interface with $In_{0.53}Ga_{0.47}As$ substrate than that using H_2O. The typical C–V curves of Al_2O_3 grown using H_2O and O_3 on $In_{0.53}Ga_{0.47}As$ substrate in Fig. 7.10 show that the H_2O process improved the interface property with the less frequency dispersion compared to O_3 process [114]. For the same reason, the lower O_3 concentration for the ALD HfO_2 process on GaAs substrate allowed the better electrical properties than the case with a higher O_3 concentration [115].

7.4 Transistor Characteristics with ALD Gate Oxides

7.4.1 Sub 1 nm EOT Devices

Since continuous MOSFET downscaling is inevitable, investigating the performance and reliability of sub 1-nm EOT regime devices became an important topic. The sub 1 nm EOT has been mainly obtained by ALD high-k oxides, thanks to the precise thickness control across the wafer. However, reduction of the interfacial SiO_2 layer (or IL with slightly different chemical composition) while at the same time maintaining a good quality of the Si/oxide interface is not straightforward.

Several approaches have been followed to obtain the sub 1 nm EOT devices, such as depositing $HfSiO_x$ IL before ALD-HfO_2 deposition [116], controlling oxygen source during ALD-HfO_2 deposition [117], or mixing exotic materials to HfO_2 to increase the dielectric constant [118]. One popular method introduced recently is remote scavenging of oxygen by a very thin TiN metal layer on top of the ALD gate oxide [119, 120]. The oxygen transfer from the SiO_2 IL to the TiN

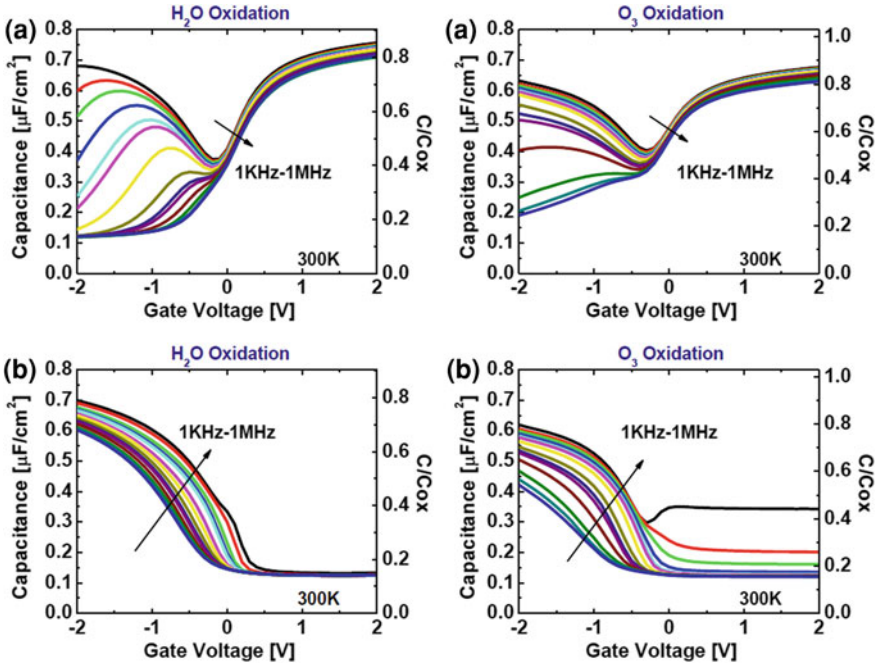

Fig. 7.10 C–V characteristics as a function of frequency of MOSCAP with ALD Al_2O_3 grown using H_2O and O_3 (**a**) on n-type and (**b**) p-type $In_{0.53}Ga_{0.47}As$ [114]

metal through the high-k layer decreases the physical SiO_2 IL thickness and as such the EOT. The IL thickness can be controlled by the TiN layer thickness.

HRTEM images showed the thickness of the IL decreases in SiO_2/HfO_2 gate stacks when a TiN metal gate is present instead of TaN [5], while the HfO_2 layer thickness does not change. Since the initial SiO_2/HfO_2 stacks are deposited by exactly the same process, this scavenging effect is coming from the metal gate difference only. Finally thinner SiO_2 layer generates smaller EOT as shown in Fig. 7.11a [5]. Note that a Lanthanum (La) oxide capping layer is used for the V_{TH} tuning in this case, but this does not disturb the scavenging effect. Figure 7.11b shows variation in J_g as a function of EOT. Thinner EOT devices, which experienced severe scavenging process, still show a reasonable J_g trend in both 1.2- and 1.8 nm-thick ALD HfO_2 devices. However, the mobility significantly decreases because the thinner SiO_2 layer enhances remote phonon and charge scattering from the HfO_2 layer to the channel region (Fig. 7.11c) [5]. Ando et al. [119] also showed that scavenged devices, with HfO_2 dielectric layers with or without La-capping layer show decreased mobility in the sub 1-nm EOT range.

Next, the device reliability in sub 1nm EOT devices is focused. The negative bias temperature instability (NBTI) degradation mechanism was investigated for metal-gated ALD high-k devices as shown in Fig. 7.12a [121]. The NBTI degradation was studied from 2 down to 0.5 nm EOT with a severe criterion of 30 mV

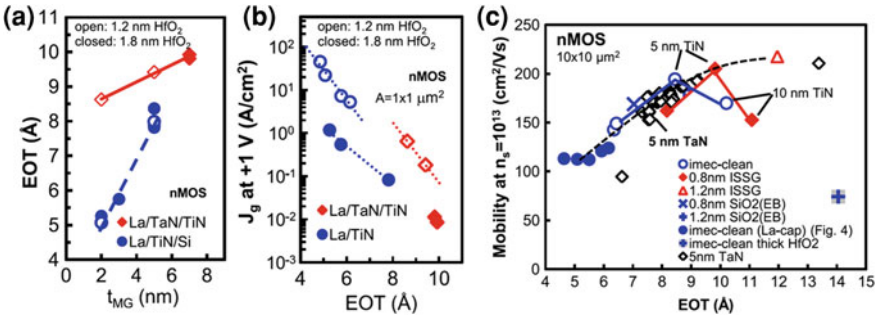

Fig. 7.11 (**a**) EOT extracted from C-V measurements on n-type MOSCAPs with ALD-HfO_2 and La capping layer as a function of the metal gate thickness for TiN and TaN. (**b**) The variation in J_g as a function of EOT for TaN and TiN gates and for two different ALD-HfO_2 thicknesses. Thinner EOTs are found with TiN. (**c**) The long channel electron mobility as a function of EOT for stacks with different interface layers, metal electrodes (TiN, TaN) and TiN thicknesses. IL has no impact on the mobility. TiN thickness is 2 nm when not indicated [5]

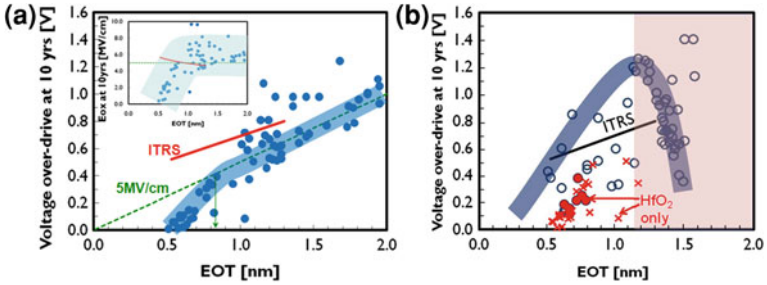

Fig. 7.12 (**a**) Over-drive voltage at 10 years extracted from NBTI on 70 different p-type MOSFET devices. Below 1 nm EOT, the over-drive voltage decreases more than the iso-electric field at 5 MV/cm. ITRS data is also added. The *inset* shows electric field at 10 years. In sub 1 nm EOT, ITRS suggests increased electric field, but real devices shows even more decreased NBTI reliability. (**b**) Over-drive voltage at 10 years extracted from PBTI on 63 different n-type MOSFET devices is shown (*circles*). The straight line is from ITRS. Over-drive voltage at 10 years from N/PBTI is shown together, with only HfO_2 devices. N/PBTI does not show clear difference (*closed circles* for PBTI, "x" symbols for NBTI) [121]

in V_{TH} difference (ΔV_{TH}). The international technology roadmap for semiconductors (ITRS) [122] suggests that satisfying the demand for a rapidly increasing electric field in the sub 1 nm EOT regime will become difficult to meet even with a higher quality oxide because the hole trapping into the bulk defects has been increased. Therefore, an *iso*-electric field target at 5 MV/cm has also been considered in Fig. 7.12a together with the ITRS standard. In the EOT regime higher than 1 nm, the NBTI degradation followed an *iso*-electric field model because the Si/SiO_2 interface degradation mechanism is dominant [123–126]. However, in the sub 1 nm EOT regime, NBTI was in addition affected by hole trapping into bulk

defects in the high-k dielectric. The kinetics for V_{TH} shift according to the stress time showed much lower time exponent ($\sim$0.13) in the 0.5 nm EOT device than in the 2 nm EOT device ($\sim$0.24) [121], indicating a reduced interface degradation contribution to the total NBTI degradation. Charge pumping analysis combined with NBTI showed that bulk trap degradation increases to $\sim$two orders of magnitude higher than the interface trap generation during NBTI stress in a 0.58 nm EOT device [121]. The activation energy was lower in the 0.58 nm EOT device (0.49 eV) than in the 2 nm EOT (0.68 eV) due to the increased bulk trapping component including direct tunneling, which is independent of temperature. The bulk defects affecting NBTI are mostly preexisting defects in the ALD high-k layer. Therefore, decreasing high-k bulk defects can improve NBTI in sub 1 nm EOT regime, at least up to the *iso*-electric field limitation from interface degradation.

In case of positive BTI (PBTI) reliability, the degradation in the EOT regime higher than 1 nm is known to be driven by electron trapping into defects in the high-k layer [127–129]. Figure 7.12b shows lower voltage over-drive because thicker high-k dielectric layers contain more defects to be filled (the IL thickness is fixed at 1 nm). However, the PBTI lifetime decreases when the EOT decreases below 1 nm, because the thinner SiO_2 thickness increases the electron tunneling probability from the Si substrate into the high-k defects. Indeed, slight transconductance (G_m) degradation was also observed after stress in a 0.61 nm device with ALD HfO_2 gate oxide [130], which indicates trap generation near the Si/oxide interface. However, Fig. 7.12b clearly shows that PBTI degradation largely depends on the process and the high-k material quality at a given EOT. Depositing a La-oxide capping layer on top of the ALD HfO_2 dielectric or applying Ar/As implantation can improve PBTI by shifting up the trap levels away from the Si conduction band. As such, these levels cannot be reached by injected electrons during PBTI stress [128–131]. In addition, adding Gadolinium in the HfO_2 dielectric by ALD can also improve PBTI because a trap level aligned to the Si conduction band is absent in contrast to $HfLaO_x$ [132].

TDDB is also a large concern in sub 1 nm EOT devices, because the very thin oxide layer can be broken down by a percolation path containing just a few generated defects. Figure 7.13 shows an All-in-one TDDB map on a 0.63 nm EOT pMOSFET device with ALD-HfO_2 layer [133]. The All-in-one TDDB map is obtained by extracting soft breakdown (SBD) and post-SBD wear-out parameters from measuring the time to hard breakdown (HBD) [134]. Although the EOT is extremely small, the device shows a 10 years lifetime at $V_G = 0.5$ V from the SBD, and $V_G = 1.0$ V from the HBD. Since the operation voltage is lower than 1.0 V in this EOT regime, the device is not limited by the HBD until 10 years. This shows TDDB is a lower concern than NBTI in sub 1 nm EOT devices with ALD-HfO_2 dielectric layers.

On the other hand, the impact of impurities resulting from the ALD process needs to be studied carefully, because they can generate interface or bulk defects and affect device performance and reliability. Fortunately, Cl residue from $HfCl_4$ precursor does not degrade mobility and TDDB reliability when combined with

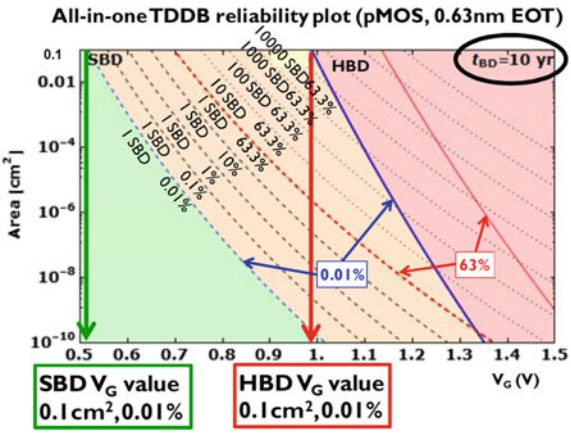

Fig. 7.13 'All-in-one' TDDB reliability for a 0.63 nm EOT p-type MOSFET device. For a fixed lifetime of 10 years three different regions of area/V_G combinations can be distinguished: SBD free, SBD & wear-out, and H_{BD}. For this very thin ALD-HfO_2 devices, a $V_{G,SBD} = 0.5$ V and $V_{G,HBD} = 1$ V is extracted [133]

H_2O oxidant in the 0.9 nm EOT devices as mentioned earlier in this chapter [17]. This observation was further confirmed by first-principles calculations, which proved that residual chlorine does not form additional trap energy levels inside the HfO_2 band gap [17]. In case of O_3 with $HfCl_4$, optimizing the O_3 concentration during ALD process is important to improve the interface trap density and mobility [135].

Study on carbon residue related to the ALD-HfO_2 dielectric was also reported regarding the TDMAH and O_3 precursors. The 10 years TDDB lifetime of high density O_3 condition was guaranteed at −1.0 V, whereas that of low density O_3 was only obtained at voltages lower than −0.8 V [50], which may imply higher O_3 successfully removed carbon residue-related defects. The first-principles calculations showed that the interstitial carbon atoms in the HfO_2 films produced deep acceptor-like trap states in the band gap, which may enhance the electrical conduction by a trap-mediated conduction mechanism. TEMAH precursor has been studied also, which showed using D_2O oxidant instead of H_2O oxidant decreases interface and bulk trap generation after CVS, and improves TDDB reliability [136].

7.4.2 SiGe and III–V Channel Devices

pMOSFETs with Ge or SiGe channels have been demonstrated to be a viable option for future logic device applications thanks to the high hole mobility and the possible integration onto silicon substrates [137–139]. However, a high N_{it} between Ge substrate and high-k materials is a big concern [140]. Adopting a thin Si layer on top of the Ge substrate can reduce the N_{it} significantly as mentioned in previous section [141]. When the Si capping layer thickness increases, the carrier scattering by the Si/oxide interface reduces, however, the carrier density in the Ge channel also decreases. Therefore, a careful optimization of the Si capping layer thickness is important for the mobility enhancement [142, 143].

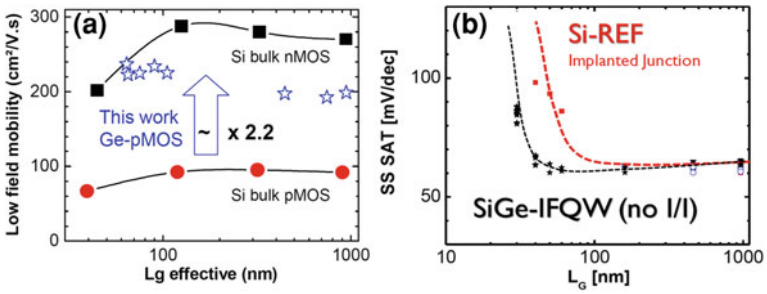

Fig. 7.14 (**a**) Low field hole mobility as a function of effective gate length for Ge p-type MOSFETs. About twice higher and stable mobility are found than in Si p-type MOSFETs [137]. (**b**) Enhanced short channel effect control with SiGe channel p-type FETs is shown. SiGe channel p-type FETs are compared to control Si planar devices (with implants) [145]

Figure 7.14a shows a good example of enhanced hole mobility in ALD-HfO_2 devices on Ge substrate, regardless of channel length (L_G) [137]. The low field hole mobility in pMOSFET devices increases about twice higher for the Ge substrate as compared to the Si substrate. ALD-HfO_2/Al_2O_3 structures also showed high hole mobility of 546 cm^2/Vs at 0.76 nm of EOT [144]. The mobility enhancement continues as Si_xGe_y substitutes Ge channel [3]. Furthermore, there is a report that the short channel effect has been improved with Si_xGe_y channel as shown in Fig. 7.14b [145].

NBTI reliability on the Ge channel device with a 0.5 nm of Si layer and an ALD-HfO_2 high-k dielectric showed similar 10 years lifetime as the Si substrate device [146], even though the initial N_{it} was about two orders of magnitude higher in the Ge device. Further NBTI study on the Si_xGe_y channel devices suggested a possible solution to obtain reliable pMOS devices in sub 1 nm EOT regime [147]. Figure 7.15a shows improved NBTI with the $Si_{0.45}Ge_{0.55}$ channel, and the ALD-HfO_2 device is more robust when the Si capping layer thickness on the $Si_{0.45}Ge_{0.55}$ channel decreases. This improved NBTI is due to the charge-injection level adjustment [147]. By adopting a Si_xGe_y channel and a thin Si capping layer, the Fermi level of the Si_xGe_y channel moves further from the oxide valence band edge, and less high-k bulk defects can be charged during the NBTI stress. Therefore, the reduction of bulk defects in the ALD high-k layer can improve further the NBTI reliability in the Si_xGe_y channel devices.

Hot carrier reliability studies have been also performed on the Si_xGe_y channel devices with ALD high-k layers. Loh et al. [148] showed that a higher Ge content and thinner Si capping layer can help to improve the channel hot carrier reliability. However, the Si_xGe_y channel devices showed more degradation than Si substrate devices after stressing at maximum impact ionization or ($V_G - V_{TH} = V_D$) conditions as shown in Fig. 7.15b, c. Franco et al. [149] showed less degradation after hot carrier stress than NBT stress in ALD-HfO_2 devices, due to the reduced charge trapping into the pre-existing HfO_2 bulk defects. However, again the Si_xGe_y

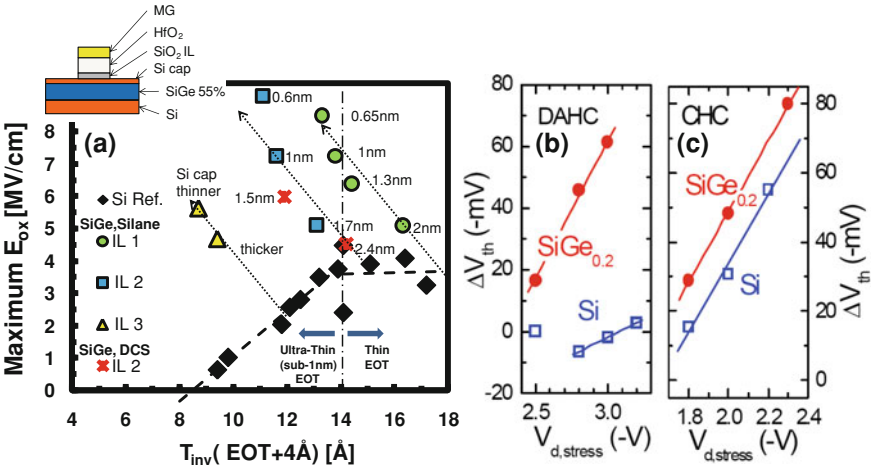

Fig. 7.15 (**a**) The operating electric field (E_{ox}) for 10 year NBTI reliability improves when reducing the Si cap thickness, which is observed consistently for several SiO_2 IL and for different Si precursors and epi-growths ('Prec. 1' and 'Prec. 2'). The *inset* shows a schematic diagram of a SiGe pFET [147]. In (**b**) and (**c**), voltage dependency of HC degradation at maximum impact ionization (DAHC) and $V_G = V_D$ (CHC) for Si and SiGe (Ge 20 %) devices are shown. HC stress performed for 100 s [148]

channel devices were more degraded than Si substrate devices after the hot carrier stress at $V_G = V_D$ (V_D is the drain voltage).

Although the III–V substrate for nMOSFETs is receiving intense research interests, the N_{it} between III–V substrate and gate oxide is a serious problem as in the Ge substrate case. The oxidation of the surface introduces stress at the surface, and reduction of the oxides does not decrease N_{it} generated by the oxidation [150]. Further, N_{it} in mid-gap is independent of the oxide, or different surface cleans and post-anneals, it is likely that the defects are originally due to the $In_{0.53}Ga_{0.47}As$ itself [151]. This mid-gap N_{it} generates the Fermi level pinning [152]. Figure 7.16a shows mobility from InGaAs or Ge substrate devices with different surface treatments, and sulfur treatment shows about 3 times higher peak mobility than HCl treatment for the InGaAs devices [153].

Another important factor in III–V devices is the border traps located in the high-k layer [153]. The spatial and energetic distribution of the traps inside the ALD-Al_2O_3 layer on InGaAs has been extracted by the TSCIS technique [154, 155] as shown in Fig. 7.16b [4]. 9 nm-thick ALD-Al_2O_3 were grown with TMA and H_2O on the $In_{0.53}Ga_{0.47}As$ channel after surface preparation for those devices. The border trap density inside the ALD Al_2O_3 layer was significantly reduced by $(NH_4)_2S$ treatment, and time-of-flight secondary ion mass spectroscopy showed lower In concentration inside the Al_2O_3 layer. Sulfur acted as an In-diffusion barrier during the ALD of Al_2O_3, lowered the border trap density in the oxide.

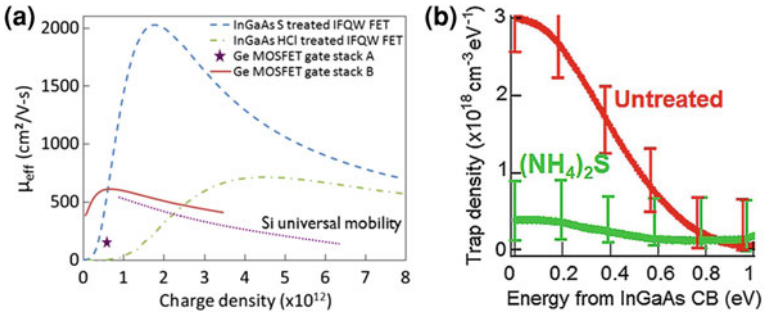

Fig. 7.16 (**a**) Mobility of InGaAs or Ge substrate devices with ALD-Al_2O_3 layer [153], (**b**) Al_2O_3 trap density as a function of energy at a depth of 1.5 nm inside the oxide measured from the interface of InGaAs/ALD-Al_2O_3 [4]

It is also reported that direct ALD of $TaSiO_x$ on (100) InP and (100) $In_{0.53}Ga_{0.47}As$ substrates results in low electron barriers that cannot prevent electron injection into the oxide [156]. This increases electron trapping in the $TaSiO_x$ and can degrade the device reliability.

7.4.3 Three-Dimensional Devices

The 3D device or FinFET is recently highlighted due to its superior electrostatic control to the devices with planar-geometry, which improves the short channel effect [157]. The conformality of ALD can be used to deposit a gate dielectric oxide and metal gate on the side- and top-walls of the fin structure.

The recent production of the 3D device in the 22 nm node [158] has accelerated related research. Indeed the 22 nm p-type FinFET device shows 27 % improved saturated drain current (I_{dsat}) characteristics from I_{on}–I_{off} analysis, and 13 % of I_{dsat} improvement was reported in n-type FinFET as compared to the 32 nm planar transistors. Another performance boost has been demonstrated with the conformal doping process using plasma (self-regulatory plasma doping, SRPD) [159]. The SRPD device with ALD HfO_2 gate stack shows 15 % improved I_{on}–I_{off} characteristic in n-type FinFETs by increasing the side-wall doping concentration relative to the ion implanted devices.

Replacement metal gate (RMG) process has been strongly considered recently, in order to lower thermal budget for the high-k/metal gate stacks [160, 161]. Figure 7.17a shows the 25 % higher I_{on} at 10^{-7} A/μm of I_{off} in the RMG p-type FinFET with ALD HfO_2 layer compared to the traditional gate first (GF) devices [162]. The high-k first (HKF) device where the deposited high-k layer is protected during gate removal or the high-k last (HKL) device where the high-k layer is deposited at the end of the process does not show a large difference in the I_{on}–I_{off} characteristics. Lower V_{TH} is also observed in the RMG devices compared to the

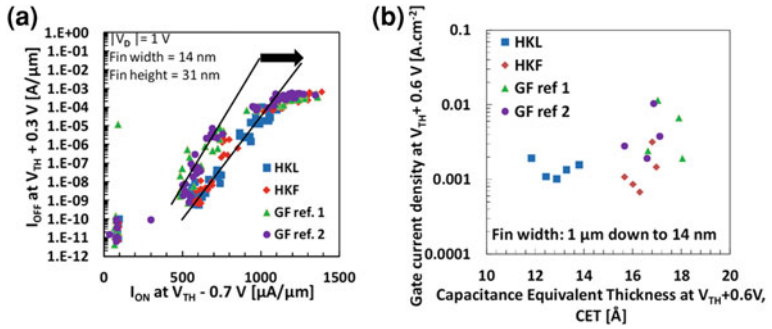

Fig. 7.17 (**a**) I_{on}–I_{off} for gate first and high-k first/high-k last bulk p-type FinFET devices at |VD| = 1 V, $(V_G - V_{TH}) = -0.7$ V (ON-state) and $(V_G - V_{TH}) = 0.3$ V (OFF-state). (**b**) Gate leakage current density versus CET at $V_{TH} + 0.6$ V for TiN/HfO_2 gate stack in gate first and high-k first/high-k bulk p-type FinFETs [162]

GF. Additionally, the HKL p-type FinFET devices revealed a lower EOT as compared to the HKF and GF devices at similar gate leakage (Fig. 7.17b). The lower thermal budget in HKL process can suppress the regrowth of low-k interfacial SiO_2.

A conventional FinFET device includes a top-wall with (100) direction, and side-walls with (110) direction. Especially, in this structure, the N_{it} from side-walls is an important factor to understand device performance and reliability, because the main channel is formed on the fin side-walls rather than the top-wall. In order to separate the top- and side-wall interface defect density N_{it}, charge pumping can be applied. By measuring charge pumping current in various fin width devices with a 2 nm ALD-HfO_2 gate oxide (Fig. 7.18a), N_{it} from top-wall and side-walls is calculated from the slope and y-intercept respectively [163].

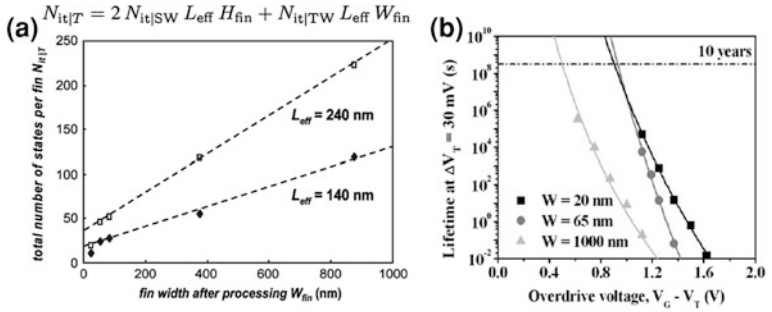

Fig. 7.18 (**a**) Total interface trap density per fin is plotted against the fin width for devices fabricated on a rotated-notch wafer. The slope of the *line* is a measure of N_{it} on top surface, while the intercept is a measure of the N_{it} on the sidewall [163]. (**b**) PBTI lifetime versus gate voltage over-drive for different W_{fin} (TiN gate thickness of 3 nm) is shown. PBTI improves in narrower FinFET devices with ALD-HfO_2 gate stack [167]

The main degradation mechanism for N/PBTI reliability on FinFETs remains the same as in planar devices, as described in the previous section. NBTI degradation is a combination of interface defect generation and hole trapping into the high-k bulk defects. Therefore, substrate rotation to change the side-wall orientation from (110) to (100) improves NBTI by reducing the number of interface states which can be broken during the NBTI stress [164–166]. PBTI degradation originates mainly from the electron trapping into the high-k bulk defects, and the parallel and close side-walls in a FinFET structure reduce the degradation effectively. Indeed PBTI improves in narrower FinFET devices with ALD-HfO_2 gate stack (Fig. 7.18b) [167], possibly due to the reduced injection charge density from the Si substrate by decreased electric field near the channel region [168]. This implies that NBTI in sub 1 nm EOT regime can be improved by reducing hole trapping, and ALD technique giving a high quality high-k layer can help to improve further both N and PBTI reliability. Additionally, it is reported that applying ALD-TiN metal gate instead of sputtered-TiN shows better NBTI [169], due to lower defect generation in the ALD HfO_2 high-k layer during the gate metal deposition.

TDDB reliability is strongly affected by the fin corners. When the fin corner is sharp, the Weibull distribution is much wider in the FinFET than planar devices [170], probably due to the non-uniform electric field at the fin corner in different devices. The corner rounding improves Weibull characteristic in FinFETs to a similar level as the planar devices [171]. As a result, TDDB is not a serious problem in FinFET devices compared to planar, when the corner rounding process is successfully introduced and conformal ALD oxide is deposited around the fin.

7.5 Summary

The influences of metal precursors and oxygen sources on the ALD high-k film growth, resulting film properties, and device performance were discussed focusing on HfO_2-based materials. They crucially affect the interface properties as well as the bulk properties of the film.

$HfCl_4$ was introduced as a Hf precursor for HfO_2 ALD due to its advantages of simple molecular structure, high thermal stability, and good HfO_2 dielectric quality. However, some drawbacks of $HfCl_4$ are low reactivity with H-terminated Si surface, low vapor pressure, strong Hf–Cl bond strength, low growth -per-cycle, Cl residue, and corrosive HCl by-product. Several metal–organic Hf precursors such as TEMAH and TDMAH have been employed to obtain comparable film properties as $HfCl_4$ precursor. They were characterized by their relatively weak Hf–N bond providing less substrate-dependent growth and higher growth rate compared to HfO_2 film grown using $HfCl_4$. In addition, these N-containing MO precursors simultaneously formed $SiON_x$ layer during ALD of HfO_2 on Si, which prevents out-diffusion of Si during ALD and PDA to result in low interfacial trap density. However, HfO_2 film grown from MO precursors is hardly free from C

impurity which deteriorates interface and bulk properties. Therefore, process parameters such as precursor pulse time and reactor temperature should be carefully optimized according to the types of the metal precursors. Recently, BTEMAH was synthesized by replacing one of four amido ligands in TEMAH with a tert-butoxy ligand to obtain higher reactivity and volatility over amide precursors. Consequently, it showed improved growth-per-cycle and higher density of HfO_2 compared with HfO_2 grown from TDMAH.

O_3 provides the higher growth rate and lower impurity level of the ALD high-k film due to the stronger oxidation power and higher reactivity than those of H_2O. The thicker IL grown during ALD with O_3 improved the thermal stability against the Si out-diffusion from the substrate, but degrades the EOT of the film. The stable GeO_2 IL grown on Ge substrate during ALD with O_3 improves the interface property compared to ALD with H_2O. However, in case of III–V substrates, O_3 induced the severe interfacial reactions of the ALD high-k film with the substrates such as the selective oxidation and reduction of the substrate elements resulting in the degraded interface property.

The performance and reliability of various recently highlighted devices including ALD high-k film are also discussed. Adopting thin TiN metal layer decreased SiO_2 interface layer thickness and EOT of the total gate stack by scavenging effect, which enables to achieve sub 1 nm EOT but the mobility decreased due to the higher remote phonon and charge scattering from the ALD-HfO_2 layer to the channel region. NBTI degradation in sub 1 nm EOT devices was enhanced by increased hole trapping into the ALD high-k bulk defects. TDDB on a pMOSFET device having 0.63 nm EOT with ALD-HfO_2 layer showed the device was not limited by the HBD until 10 years of lifetime. NBTI reliability of the Si_xGe_y channel devices with ALD-HfO_2 showed improved lifetime as compared to Si channel devices due to the adjustment of the charge-injection level. For InGaAs substrates, both interface and bulk traps are crucial problems in device performance and reliability. The border trap density inside the ALD-Al_2O_3 layer was significantly reduced by $(NH_4)_2S$ treatment. ALD technique is essential for 3D FinFET devices due to the structural characteristic. RMG process with lower thermal budget for the ALD high-k gate stacks improved I_{on}–I_{off} characteristics and showed lower EOT at equal J_g.

It is evident that the usefulness of ALD for futuristic MOSFET devices will be ever-increasing as the device structure becomes more 3D and smaller thanks to its perfect conformality and atomic-level controllability.

References

1. http://www.intel.com/technology/index.htm
2. Suntola T (1984) Proceeding of the 16th international conference on solid state devices and materials, p 647
3. Mitard J, Witters L, Garcia Bardon M, Christie P, Franco J, Mercha A, Magnone P, Alioto M, Crupi F, Ragnarsson L-Å, Hikavyy A, Vincent B, Chiarella T, Loo R, Tseng J,

Yamaguchi S, Takeoka S, Wang W-E, Absil P, Hoffmann T (2010) Technical digest—International electron devices meeting, p 249
4. Alian A, Brammertz G, Degraeve R, Cho M, Merckling C, Lin D, Wang W-E, Caymax M, Meuris M, De Meyer K, Heyns M (2012) Elecron Device Lett 33:1544
5. Ragnarsson L-Å, Chiarella T, Togo M, Schram T, Absil P, Hoffmann T (2011) Microelectron Eng 88:1317
6. Kang CY, Choi R, Song SC, Choi K, Ju BS, Hussain MM, Lee BH, Bersuker G, Young C, Heh D, Kirsch P, Barnet J, Yang J-W, Xiong W, Tseng H–H, Jammy R (2006) Technical digest—International electron devices meeting, p 1
7. Thelander C, Fröberg LE, Rehnstedt C, Samuelson L, Wernersson L-E (2008) Elecron Device Lett 29:206
8. Delabie A, Caymax M, Brijs B, Brunco D, Conard T, Sleeckx E, Van Elshocht S, Ragnarsson L-Å, De Gendt S, Heyns M (2006) ECS Trans 1(5):433–446
9. Nyns L, Delabie A, Caymax M, Heyns MM, Van Elshocht S, Vinckier C, De Gendt S (2008) J Electrochem Soc 155:G269
10. Cho M, Park J, Park HB, Hwang CS, Jeong J, Hyun KS (2002) Appl Phys Lett 81:334
11. Ritala M, Leskelä M, Nykänen E, Soininen P, Niinistö L (1993) Thin Solid Films 225:288
12. Green ML, Ho M-Y, Busch B, Wilk GD, Sorsch T, Conard T, Brijs B, Vandervorst W, Räisänen PI, Muller D, Bude M, Grazul J (2002) J Appl Phys 92:7168
13. Triyoso D, Liu R, Roan D, Ramon M, Edwards NV, Gregory R, Werho D, Kulik J, Tam G, Irwin E, Wang X-D, La LB, Hobbs C, Garcia R, Baker J, White BE Jr, Tobin P (2004) J Electrochem Soc 151:F220
14. Ragnarsson L-Å, Brunco DP, Yamamoto K, Tökei Z, Pourtois G, Delabie A, Parmentier B, Conard T, Roussel P, Gendt SD, Heyns MM (2009) J Electrochem Soc 156:H416
15. Cho M, Park HB, Park J, Hwang CS, Lee J-C, Oh S-J, Jeong J, Hyun KS, Kang H-S, Kim Y-W, Lee J-H (2003) J Appl Phys 94:2563
16. Park HB, Cho M, Park J, Hwang CS, Lee J-C, Oh S-J (2003) J Appl Phys 94:1898
17. Cho M, Degraeve R, Pourtois G, Delabie A, Ragnarsson L-Å, Kauerauf T, Groeseneken G, De Gendt S, Heyns M, Hwang CS (2007) IEEE Trans Electron Dev 54:752
18. Delabie A, Puurunen RL, Brijs B, Caymax M, Conard T, Onsia B, Richard O, Vandervorst W, Zhao C, Heyns MM, Meuris M, Viitanen MM, Brongersma HH, de Ridder M, Goncharova LV, Garfunkel E, Gustafsson T, Tsai W (2005) J Appl Phys 97:0641004
19. Delabie A, Brunco DP, Conard T, Favia P, Bender H, Franquet A, Sioncke S, Vandervorst W, Elshocht SV, Heyns M, Meuris M, Kim E, McIntyre PC, Saraswat KC, LeBeau JM, Cagnon J, Stemmer S, Tsaie W (2008) J Electrochem Soc 155:H937
20. Goel N, Majhi P, Chui CO, Tsai W, Choi D, Harris JS (2006) Appl Phys Lett 89:163517
21. Delabie A, Alian A, Bellenger F, Caymax M, Conard T, Franquet A, Sioncke S, Van Elshocht S, Heyns MM, Meurisa M (2009) J Electrochem Soc 156:G163
22. Kita K, Takahashi T, Nomura H, Suzuki S, Nishimura T, Toriumi A (2008) Appl Surf Sci 254:6100
23. Suzuki S, Kita K, Nomura H, Takahashi T, Nishimura T, Toriumi A (2007) Ext. Abstract International conf on solid state device and materials, p 20
24. Chui CO, Ramanathan S, Triplett BB, McIntyre PC, Saraswat KC (2002) IEEE Electron Device Lett 23:473
25. Kamata Y, Kamimuta Y, Ino T, Nishiyama A (2005) Jpn J Appl Phys 44:2323
26. Chi D, Chui CO, Saraswat KC, Triplett BB, McIntyre PC (2004) J Appl Phys 96:813
27. Kamata Y et al (2005) Jpn J Appl Phys 44:2323
28. Nomura H et al (2006) Solid State Device Mater:406
29. Mavrou G, Galata S, Tsipas P, Sotiropoulos A, Panayiotatos Y, Dimoulas A, Evangelou EK, Seo JW, Dieker Ch (2008) J Appl Phys 103:014506
30. Chui CO, Kim H, McIntyre PC, Saraswat KC (2004) IEEE Electron Device Lett 25:274
31. Kim H, McIntyre PC, Chui CO, Saraswat KC, Cho MH (2004) Appl Phys Lett 85:2902
32. Oh J, Majhi P, Tseng H–H, Jammy R, Kelly DQ, Banerjee SK, Campbell JC (2008) Thin Solid Films 516:4107

33. Fukuda Y, Ueno T, Hirono S, Hashimoto S (2005) Jpn J Appl Phys 44:6981
34. Robertson J (2005) Solid State Electron 49:283
35. Maeda T, Nishizawa M, Morita Y, Takagi S (2007) Appl Phys Lett 90:072911
36. Delabie A, Bellenger F, Houssa M, Conard T, Van Elshocht S, Caymax M, Heyns M, Meuris M (2007) Appl Phys Lett 91:082904
37. Fukuda Y, Yazaki Y, Otani Y, Sato T, Toyota H, Ono T (2010) IEEE Trans Electron Devices 57:282
38. Xie Q, Musschoot J, Schaekers M, Caymax M, Delabie A, Qu XP, Jiang YL, Berghe SVD, Liu J, Detavernier C (2010) Appl Phys Lett 97:222902
39. Sioncke S, Lin HC, Brammertz G, Delabie A, Conard T, Franquet A, Meuris M, Struyf H, De Gendt S, Heyns M, Fleischmann C, Temst K, Vantomme A, Muller M, Kolbe M, Beckhoff B, Caymax M (2011) J Electrochem Soc 158:H687
40. Chang CH, Chiou YK, Chang YC, Lee KY, Lin TD, Wu TB, Hong M, Kwo J (2006) Appl Phys Lett 89:242911
41. Tallarida M, Adelmann C, Delabie A, Van Elshocht S, Caymax M, Schmeisser D (2011) Appl Phys Lett 99:042906
42. Ye PD, Wilk GD, Yang B, Kwo J, Chu SNG, Nakahara S, Gossmann H-JL, Mannaerts JP, Hong M, Ng KK, Bude J (2003) Appl Phys Lett 83:180
43. Frank MM, Wilk GD, Starodub D, Gustafsson T, Garfunkel E, Chabal YJ, Grazul J, Muller DA (2005) Appl Phys Lett 86:152904
44. Maes JW, Fedorenko Y, Delabie A, Ragnarsson L-Å, Swerts J, Nyns L, Van Elshocht S, Wang C-G, Wilk G (2007) ECS Trans 11(4):59–72
45. Jung H-S, Kim HK, Yu I-H, Lee SY, Lee J, Park J, Jang JH, Jeon S-H, Chung YJ, Cho D-Y, Lee N-I, Park TJ, Choi J-H, Hwang CS (2012) J Electrochem Soc 159:G33
46. Jung H-S, Jeon SH, Kim HK, Yu I-H, Lee SY, Lee J, Chung YJ, Cho D-Y, Lee N-I, Park TJ, Choi J-H, Han S, Hwang CS (2012) ECS J Solid State Sci Technol 1:N33
47. Xie Q, Deduytsche D, Schaekers M, Caymax M, Delabie A, Qu X-P, Detavernier C (2010) Appl Phys Lett 97:112905
48. Cho M, Park HB, Park J, Lee SW, Hwang CS, Jang GH, Jeong J (2003) Appl Phys Lett 83:5503
49. Kim JH, Park TJ, Cho M, Jang JH, Seo M, Na KD, Hwang CS, Won JY (2009) J Electrochem Soc 156:G48
50. Cho M, Kim JH, Hwang CS, Ahn H-S, Han S, Won JY (2007) Appl Phys Lett 90:182907
51. Seo M, Min Y-S, Kim SK, Park TJ, Kim JH, Na KD, Hwang CS (2008) J Mater Chem 18:4324
52. Shevjakov AM, Kuznetsova GN, Aleskovskii VB (1965) Proceedings of the second USSR conference on high-temperature chemistry of oxides, Leningrad, USSR, p 26
53. Suntola T, Antson J (1977) U.S. Patent No. 4,058,430
54. Niinistö J, Putkonen M, Niinistö L, Arstila K, Sajavaara T, Lu J, Kukli K, Ritala M, Leskelä M (2006) J Electrochem Soc 153:F39
55. Swerts J, Peys N, Nyns L, Delabie A, Franquet A, Maes JW, Elshocht SV, De Gendt S (2010) J Electrochem Soc 157:G26
56. Liu X, Ramanathan S, Longdergan A, Srivastava A, Lee E, Seidel TE, Barton JT, Pang D, Gordon RG (2005) J Electrochem Soc 152:G213
57. Won S-J, Suh S, Lee SW, Choi G-J, Hwang CS, Kim HJ (2010) Electrochem Solid-State Lett 13:G13
58. Choi G-J, Kim SK, Won S-J, Kim HJ, Hwang CS (2009) J Electrochem Soc 156:G138
59. Won S-J, Kim J-Y, Choi G-J, Heo J, Hwang CS, Kim HJ (2009) Chem Mater 21:4374
60. Cheng Y-L, Chang Y-L, Hsieh C-Y, Lin J-R (2013) JVST A 31(1)
61. Campabadal F, Beldarrain O, Zabala M, Acero MC, Rafi JM (2011) Proceeding og the 8th Spanish conference on electron devices, CDE
62. Park TJ, Sivasubramani P, Coss BE, Kim H-C, Lee B, Wallace RM, Kim J, Rousseau M, Liu X, Li H, Lehn J-S, Hong D, Shenai D (2010) Appl Phys Lett 97:092904

63. Cho M, Jeong DS, Park HB, Lee SW, Park TJ, Hwang CS, Jang GH, Jeong J (2004) Appl Phys Lett 85:5953
64. Park HB, Cho M, Park J, Lee SW, Hwang CS, Kim J-P, Lee J-H, Lee N-I, Lee J-C, Oh S-J (2003) J Appl Phys 94:3641
65. Kamiyama S, Miura T, Nara Y (2006) Electrochem Solid-State Lett 9:G285
66. Chung KJ, Park TJ, Sivasubramani P, Kim J, Ahn J (2010) ECS Trans 28:221
67. Degraeve R, Kerber A, Roussel Ph, Cartier E, Kauerauf T, Pantisano L, Groeseneken G (2003) IEEE technical digest of international electron devices meeting, p 935
68. Kyuno K, Kita K, Toriumi A (2005) Appl Phys Lett 86:063510
69. Lee C-K, Cho E, Lee H-S, Hwang CS, Han S (2008) Phys Rev B 78:012102
70. Fujimori H, Yashima M, Sasaki S, Kakihana M, Mori T, Tanaka M, Yoshimura M (2001) Chem Phys Lett 346:217
71. Bernay C, Ringuedé A, Colomban P, Lincot D, Cassir MJ (2003) J Phys Chem Solids 64:1761
72. Park TJ, Kim JH, Jang JH, Lee C-K, Na KD, Lee SY, Jung HS, Kim M, Han S, Hwang CS (2010) Chem Mater 22:4175
73. Kukli K, Ritala M, Sajavaara T, Keinonen J, Leskelä M (2002) Chem Vapor Depos 8:199
74. Park J, Cho M, Kim SK, Park TJ, Lee SW, Hong SH, Hwang CS (2005) Appl Phys Lett 86:112907
75. Baldovino S, Spiga S, Scarel G, Fanciulli M (2007) Appl Phys Lett 91:172905
76. Park TJ, Kim JH, Seo MH, Jang JH, Hwang CS (2007) Appl Phys Lett 90:152906
77. Delabie A, Puurenen RL, Brijs B, Caymax M, Conrad T, Onsia B, Richard O, Vandervorst W, Zhao C, Heyns MM, Meuris M, Viitanen MM, Brongersma HH, de Ridder M, Goncharova LV, Garfunkel E, Gustafsson T, Tsai W (2005) J Appl Phys 97:064104
78. Spiga S, Wiemer C, Tallarida G, Scarel G, Ferrari S, Seguini G, Fanciulli M (2005) Appl Phys Lett 87:112904
79. Kim H, Chui CO, Saraswat KC, McIntyre PC (2003) Appl Phys Lett 83:2647
80. Houssa M, De Jaeger B, Delabie A, Van Elshocht S, Afanasiev V, Autran J, Stesmans A, Meuris M, Heyns M, Non-Cryst J (2005) Solids 351:1902
81. Perego M, Scarel G, Fanciulli M, Fedushkin IL, Skatova AA (2007) Appl Phys Lett 90:162115
82. Broqvist J, Binder JF, Pasquarello A (2009) Appl Phys Lett 94:141911
83. Afanas'ev VV, Stesmans A, Delabie A, Bellenger F, Houssa M, Meuris M (2008) Appl Phys Lett 92:022109
84. Dalapati GK, Tong Y, Loh WY, Mun HK, Cho BJ (2007) IEEE Trans Electron Devices 54:1831
85. Shahrjerdi D, Tutuc E, Banerjee SK (2007) Appl Phys Lett 91:063501
86. Kim CY, Cho SW, Cho M-H, Chung KB, An C-H, Kim H, Lee HJ, Ko D-H (2008) Appl Phys Lett 93:192902
87. Hackley JC, Demaree JD, Gougousi T (2008) Appl Phys Lett 92:162902
88. Hinkle CL, Sonnet AM, Vogel EM, McDonnell S, Hughes GJ, Milojevic M, Lee B, Aguirre-Tostado FS, Choi KJ, Kim J, Wallace RM (2007) Appl Phys Lett 91:163512
89. Hinkle CL, Sonnet AM, Vogel EM, McDonnell S, Hughes GJ, Milojevic M, Lee B, Aguirre-Tostado FS, Choi KJ, Kim HC, Kim J, Wallace RM (2008) Appl Phys Lett 92:071901
90. Aguirre-Tostado FS, Milojevic M, Hinkle CL, Vogel EM, Wallace RM, McDonnell S, Hughes GJ (2008) Appl Phys Lett 92:171906
91. Shin B, Choi D, Harris JS, McIntyre PC (2008) Appl Phys Lett 93:052911
92. Chang CC, Citrin PH, Schwartz B (1977) J Vac Sci Technol 14 (4):943–952
93. Ishikawa Y, Ishii H, Hasegawa H, Fukui T (1994) New Paltz, New York (unpublished)
94. Abrahams MS, Buiocchi CJ (1965) J Appl Phys 36(9):2855–2863
95. Adachi S, Kikuchi D (2000) J Electrochem Soc 147(12):4618–4624
96. Liu Z, Sun Y, Machuca F, Pianetta P, Spicer WE, Pease RFW (2003) J Vac Sci Technol, A 21(1):212–218

97. DeSalvo GC, Bozada CA, Ebel JL, Look DC, Barrette JP, Cerny CLA, Dettmer RW, Gillespie JK, Havasy CK, Jenkins TJ, Nakano K, Pettiford CI, Quach TK, Sewell JS, Via GD (1996) J Electrochem Soc 143(11):3652–3656
98. Yablonovitch E, Cox HM, Gmitter TJ (1988) Appl Phys Lett 52(12):1002–1004
99. Lebedev MV, Ensling D, Hunger R, Mayer T, Jaegermann W (2004) Appl Sur Sci 229(1–4):226–232
100. Arthur JR (1974) Surf Sci 43(2):449–461
101. Kawai NJ, Nakagawa T, Kojima T, Ohta K, Kawashima M (1984) Electron Lett 20(1):47–48
102. Chang RPH, Darack S (1981) Appl Phys Lett 38(11):898–899
103. Callegari A, Hoh PD, Buchanan DA, Lacey D (1989) Appl Phys Lett 54(4):332–334
104. Sugata S, Takamori A, Takado N, Asakawa K, Miyauchi E, Hashimoto H (1988) J Vac Sci Technol, B 6(4):1087–1091
105. Sugaya T, Kawabe M (1991) Jpn J Appl Phys 30(3A):L402–L404
106. Grant RW, Waldrop JR (1987) J Vac Sci Tech B 5(4):1015–1019
107. Fountain GG, Hattangady SV, Vitkavage DJ, Rudder RA, Markunas RJ (1988) Electron Lett 24(18):1134–1135
108. Tiwari S (1988) IEEE Electr Device L 9 (3):142–144
109. Callegari A, Sadana DK, Buchanan DA, Paccagnella A, Marshall ED, Tischler MA, Norcott M (1991) Appl Phys Lett 58(22):2540–2542
110. Freeouf JL, Silberman JA, Wright SL, Tiwari S, Batey J (1989) Bozeman, Montana (unpublished)
111. Ivanco J, Kubota T, Kobayashi H (2005) J Appl Phys 97(7):073712–073717
112. Brennan B, Milojevic M, Kim HC, Hurley PK, Kim J, Hughes G, Wallace RM (2009) Electrochem Solid State Lett 12:H205
113. Byun Y-C, Mahata C, An C-H, Oh J, Choi R, Kim H (2012) J Phys D Appl Phys 45:435305
114. Madan H, Veksler D, Chen YT, Huang J, Goel N, Bersuker G, Datta S (2011) IEEE 117
115. Chung KJ, Park TJ, Sivasubramani P, Kim J, Ahn J (2012) Microelectron Eng 89:80
116. Ogawa A, Iwamoto K, Ota H, Morita Y, Ikeda M, Nabatame T, Toriumi A (2007) Microelectron Eng 84(9–10):1861
117. Delabie A, Caymax M, Brijs B, Brunco DP, Conard T, Sleeckx E, Van Elshocht S, Ragnarsson L-A, De Gendt S, Heyns MM (2006) J Electrochem Soc 153:F180
118. Lee T, Rhee SJ, Kang CY, Zhu F, Kim H-S, Choi C, Ok I, Zhang M, Krishnan S, Thareja G, Lee JC (2012) Electron Device Lett 27:640
119. Ando T, Frank MM, Choi K, Choi C, Bruley J, Hopstaken M, Copel M, Cartier E, Kerber A, Callegari A, Lacey D, Brown S, Yang Q, Narayanan V (2009) Technical digest—International electron devices meeting, p 423
120. Ragnarsson L-Å, Li Z, Tseng J, Schram T, Rohr E, Cho MJ, Kauerauf T, Conard T, Okuno Y, Parvais B, Absil P, Biesemans S, Hoffmann TY (2009) Technical digest—International electron devices meeting, p 663
121. Cho M, Lee J-D, Aoulaiche M, Kaczer B, Roussel P, Kauerauf T, Degraeve R, Franco J, Ragnarsson L-A, Groeseneken G (2012) IEEE Trans Electron Devices 59(8):2042
122. International Technology Roadmap for Semiconductors 2003 (or 2009) Edition, downloaded on 18 July 2011. http://www.itrs.net/Links/2009ITRS/2009Chapters_2009Tables/2009_PIDS.pdf
123. Jeppson KO, Svensson CM (1977) J Appl Phys 48(5):2004
124. Ogawa S, Shiono N (1995) Phys Rev B 51(7):4218
125. Alam MA, Mahapatra S (2005) Microelectron Reliab 45(1):71
126. Houssa M, Aoulaiche M, De Gendt S, Groeseneken G, Heyns MM, Stesmans A (2005) Appl Phys Lett 86(9):093506-1
127. Cartier E, Pantisano L, Kerber A, Groeseneken G (2003) Presented at the IEEE Insulating Films on Semiconductors Conference (INFOS), Leuven, Belgium

128. Aoulaiche M, Kaczer B, Cho M, Houssa M, Degraeve R, Kauerauf T, Akheyar A, Schram T, Roussel Ph, Maes HE, Hoffmann T, Biesemans S, Groeseneken G (2009) In: Proceedings of the international reliability physics symposium, p 1014
129. Zafar S, Callegari A, Gusev E, Fischetti MV (2003) J Appl Phys 93(11):9298
130. Cho M, Aoulaiche M, Degraeve R, Kaczer B, Franco J, Kauerauf T, Roussel P, Ragnarsson LÅ, Tseng J, Hoffmann TY, Groeseneken G (2010) In: Proceedings of the international reliability physics symposium, p 1095
131. Sahhaf S, Degraeve R, Srividya V, Cho M, Kauerauf T, Groeseneken G (2010) In: Proceedings of the international reliability physics symposium, p 1078
132. Cho M, Aoulaiche M, Degraeve R, Kaczer B, Kauerauf T, Ragnarsson L-Å, Adelmann C, Van Elshocht S, Hoffmann TY, Groeseneken G (2011) Solid State Electron 63(1):5
133. Kauerauf T, Degraeve R, Ragnarsson L-Å, Roussel P, Sahhaf S, Groeseneken G (2011) In: Proceedings of the international reliability physics symposium, p 7
134. Sahhaf S, Degraeve R, Roussel PJ, Kaczer B, Kauerauf T, Groeseneken G (2009) IEEE Trans Electron Devices 56(7):1424
135. Park J, Park TJ, Cho M, Kim SK, Hong SH, Kim JH, Seo M, Hwang CS (2006) J Appl Phys 99:094501
136. Lee T, Park I-S, Ko H-K, Lee S, Kim K-R, Ahn J (2005) International microprocesses and nanotechnology conference, p 94
137. Mitard J, De Jaeger B, Leys FE, Hellings G, Martens K, Eneman G, Brunco DP, Loo R, Lin JC, Shamiryan D, Vandeweyer T, Winderickx G, Vrancken E, Yu CH, De Meyer K, Caymax M, Pantisano L, Meuris M, Heyns M (2008) Technical digest—International electron devices meeting, p 873
138. Witters L, Takeoka S, Yamaguchi S, Hikavyy A, Shamiryan D, Cho MJ, Chiarella T, Ragnarsson L-Å, Loo R, Kerner C, Crabbe Y, Franco J, Tseng J, Wang W-E, Rohr E, Schram T, Richard O, Bender H, Biesemans S, Absil P, Hoffmann T (2010) Symposium on VLSI Technology, p 181
139. Sze SM (1981) Physics of semiconductor devices, 2nd edn. Wiley, New York
140. De Jaeger B, Bonzom R, Leys F, Richard O, Van Steenbergen J, Winderickx G, Van Moorhem E, Raskin G, Letertre F, Billon T, Meuris M, Heyns M (2005) Microelectron Eng 80(17):26
141. Leys FE, Bonzom R, Kaczer B, Janssens T, Vandervorst W, De Jaeger B, Van Steenbergen J, Martens K, Hellin D, Rip J, Dilliway G, Delabie A, Zimmerman P, Houssa M, Theuwis A, Loo R, Meuris M, Caymax M, Heyns MM (2006) Mater Sci Semicond Process 9:679
142. Yeo CC, Cho BJ, Gao F, Lee SJ, Lee MH, Yu C-Y, Liu CW, Tang LJ, Lee TW (2005) Electron Device Lett 26(10):761
143. Mitard J, Martens K, De Jaeger B, Franco J, Shea C, Plourde C, Leys FE, Loo R, Hellings G, Eneman G, Wang W-E, Lin JC, Kaczer B, De Meyer K, Hoffmann T, De Gendt S, Caymax M, Meuris M, Heyns MM (2009) European Solid-State Device Research Conference, p 411
144. Zhang R, Huang PC, Taoka N, Takenaka M, Takagi S (2012) Symposium on VLSI Technoogy, p 161
145. Mitard J, Eneman G, Hellings G, Witters L, Hikavyy A, Vincent B, Loo R, Bender H, Horiguchi N, Collaert N, Thean A (2012) SiGe, Ge, and related compunds 5: materials, processing, and devices, p 131
146. Aoulaiche M, Kaczer B, De Jaeger B, Houssa M, Martens K, Degraeve R, Roussel P, Mitard J, De Gendt S, Maes HE, Groeseneken G, Meuris M, Heyns MM (2008) In: Proceedings of the international reliability physics symposium, p 358
147. Franco J, Kaczer B, Eneman G, Roussel PhJ, Grasser T, Mitard J, Ragnarsson L-Å, Cho M, Witters L, Chiarella T, Togo M, Wang W-E, Hikavyy A, Loo R, Horiguchi N, Groeseneken G (2011) Technical digest—International electron devices meeting, p 445
148. Loh W-Y, Majhi P, Lee S-H, Oh J-W, Sassman B, Young C, Bersuker G, Cho B-J, Park C-S, Kang C-Y, Kirsch P, Lee B-H, Harris HR, Tseng H–H, Jammy R (2008) Symposium on VLSI Technology, p 56

149. Franco J, Kaczer B, Eneman G, Roussel PhJ, Cho M, Mitard J, Witters L, Hoffmann TY, Groeseneken G, Crupi F, Grasser T (2011) In: Proceedings of the international reliability physics symposium, p 624
150. Sioncke S, Lin D, Nyns L, Delabie A, Thean A, Horiguchi N, Struyf H, De-Gendt S, Caymax M (2012) ECS Trans 45(4):97
151. Brammertz G, Lin HC, Martens K, Alian A, Merckling C, Penaud J, Kohen D, Wang W-E, Sioncke S, Delabie A, Meuris M, Caymax M, Heyns M (2009) ECS Trans 19(5):375
152. Heyns M, Bellenger F, Brammertz G, Caymax M, Cantoro M, De Gendt S, De Jaeger B, Delabie A, Eneman G, Groeseneken G, Hellings G, Houssa M, Iacopi F, Leonelli D, Lin D, Magnus W, Martens K, Merckling C, Meuris M, Mitard J, Penaude J, Pourtois G, Scarrozza M, Simoen E, Soree B, Van Elshocht S, Vandenbergheb W, Vandooren A, Vereecke P, Verhulst A, Wang W-E (2010) Optical Microlithogr XXIII:764003
153. Lin D, Alian A, Gupta S, Yang B, Bury E, Sioncke S, Degraeve R, Toledano ML, Krom R, Favia P, Bender H, Caymax M, Saraswat KC, Collaert N, Thean A (2012) Technical digest—International electron devices meeting, p 645
154. Degraeve R, Cho M, Govoreanu B, Kaczer B, Zahid MB, Van Houdt J, Jurczak M, Groeseneken G (2008) Technical digest—International electron devices meeting, p 1
155. Cho M, Degraeve R, Roussel P, Govoreanu B, Kaczer B, Zahid M, Simoen E, Arreghini A, Jurczak M, Houdt JV, Groeseneken G (2010) Solid State Electron 54(11):1384
156. Afanas'ev VV, Chou H-Y, Thoan NH, Adelmann C, Lin HC, Houssa M, Stesmans A (2012) Appl Phys Lett 100:202104
157. Colinge J-P (2004) Solid-State Electron 48:897
158. Auth C, Allen C, Blattner A, Bergstrom D, Brazier M, Bost M, Buehler M, Chikarmane V, Ghani T, Glassman T, Grover R, Han W, Hanken D, Hattendorf M, Hentges P, Heussner R, Hicks J, Ingerly D, Jain P, Jaloviar S, James R, Jones D, Jopling J, Joshi S, Kenyon C, Liu H, McFadden R, McIntyre B, Neirynck J, Parker C, Pipes L, Post I, Pradhan S, Prince M, Ramey S, Reynolds T, Roesler J, Sandford J, Seiple J, Smith P, Thomas C, Towner D, Troeger T, Weber C, Yashar P, Zawadzki K, Mistry K (2012) Symposium on VLSI Techology, p 131
159. Zschätzsch G, Sasaki Y, Hayashi S, Togo M, Chiarella T, Kambham AK, Mody J, Douhard B, Horiguchi N, Mizuno B, Ogura M, Vandervorst W (2011) Technical digest—International electron devices meeting, p 841
160. Frank MM (2011) IEEE European solid-state device research conference, p 25
161. Witters L, Mitard J, Veloso A, Hikavyy A, Franco J, Kauerauf T, Cho M, Schram T, Sebai F, Yamaguchi S, Takeoka S, Fukuda M, Wang W-E, Duriez B, Eneman G, Loo R, Kellens K, Tielens H, Favia P, Rohr E, Hellings G, Bender H, Roussel P, Crabbe Y, Brus S, Mannaert G, Kubicek S, Devriendt K, De Meyer K, Ragnarsson L-Å, Steegen A, Horiguchi N (2011) Technical digest—International electron devices meeting, p 654
162. Boccardi G, Ritzenthaler R, Togo M, Chiarella T, Kim MS, Yuichiro S, Veloso A, Chew SA, Vecchio E, Locorotondo S, Devriendt K, Ong P, Brus S, Horiguchi N, Thean A (2012) International conference on solid state devices and materials, p 723
163. Kapila G, Kaczer B, Nackaerts A, Collaert N, Groeseneken GV (2007) Elecron Device Lett 28(3):232
164. Hu VP-H, Fan M-L, Hsieh C-Y, Su P, Chuang C-T (2011) IEEE Trans Electron Devices 58(3):805
165. Park H, Song SC, Woo SH, Abu-Rahma MH, Ge L, Kang MG, Han BM, Wang J, Choi R, Yang JW, Jung SO, Yeap G (2010) In: Proceedings of the international reliability physics symposium, p 1008
166. Maeda S, Choi J-A, Yang J-H, Jin Y-S, Bae S-K, Kim Y-W, Suh K-P (2004) In: Proceedings of the international reliability physics symposium, p 8
167. Feijoo PC, Cho M, Togo M, San Andrés E, Groeseneken G (2011) Microelectron Reliab 51:1521
168. Cho ES, Lee CH, Fayrushin A, Park HB, Park D (2006) In: Proceedings of the international reliability physics symposium, p 663

169. Kim JJ, Cho M, Pantisano L, Jung U, Lee YG, Chiarella T, Togo M, Horiguchi N, Groeseneken G, Lee BH (2012) Electron Device Lett 33(7):937
170. Shickova A, Collaert N, Rooyackers R, De Keersgieter A, Kauerauf T, Jurczak M, Kaczer B, Groeseneken G (2006) In: Proceedings of the ULIS conference, p 141
171. Crupi F, Kaczer B, Degraeve R, Subramanian V, Srinivasan P, Simoen E, Dixit A, Jurczak M, Groeseneken G (2006) IEEE Trans Electron Devices 53(9):2351