

Chapter 1

The Design for High Dynamic GPS Receiver in a Combined Method of FLL and PLL

Na Shen and Xiangjin Zhang

Abstract To solve the problems that the large Doppler shift makes satellite signals difficult to be captured and the high dynamic stress damages the health of the tracking loop, a novel design is proposed for high dynamic GPS receiver, which can rapidly capture signals against the large Doppler shift and has high tolerance of the high dynamic stress in its tracking loop. The satellite signals are captured by means of linear search method. The carrier wave is tracked by carrier tracking loop using Frequency-locked loop (FLL) assisted by phase-locked loop (PLL). The form of Carrier wave aided is adopted in the pseudo-code tracking loop. The experiment shows the receiver prototype can track 100 g/s high dynamic signal, which indicates that the receiver prototype could satisfy the error limits of the tracking loop, and it also can capture the visible satellite signals with a good effect of real-time tracking lock.

Keywords GPS receiver • Frequency-locked loop (FLL) • Phase-locked loop (PLL)

1.1 Introduction

Global Positioning System (GPS) has been developed for almost 30 years. However the study of high dynamic GPS receiver starts relatively late, it still needs further research. The difficulties in the design of high dynamic GPS receiver are listed as following [1]: (1) the satellite signals are difficult to be captured because

N. Shen (✉)

The National key lab of instant physics, Nanjing University of Science and Technology,
Nanjing, China
e-mail: snbox@163.com

X. Zhang

ZNDY of Ministerial Key Laboratory, Nanjing University of Science and Technology,
Nanjing, China

the carrier waves received with high dynamic have a large Doppler shift; (2) The tracking loop must be designed rationally to the satellite signals with high tolerance of the high dynamic stress. In order to track the carrier wave stably, Literature [2] proposes a method using INS auxiliary carrier loop, Literature [3] develop a carrier tracking algorithm used in high dynamic and static environments based on the nature of adaptive bandwidth adjusting of IMM. However, both of the two methods have complicated structure and cost highly.

In this paper, a novel design program is proposed for high dynamic GPS receiver. It uses the method of frequency-locked loop (FLL) assisted by phase-locked loop (PLL), which has a good effect and lower cost compared with the above two methods. The system uses the frequency (RF) chip GP2015 as the RF front-end. And the baseband part consists of digital signal processor DSP6713 and the 12-channels correlator GP2021 which form the desired digital tracking loop.

1.2 Hardware Components

Figure 1.1 shows the hardware system of the whole GPS receiver. The GPS RF signals are received by the antenna, and then amplified by the low noise preamp with 2.4 MHz bandwidth. After filtering the signals are amplified by a passive band pass amplifier between the antenna and preamp to minimize out-of-band RF interference. The RF front-end is composed of the GP2015 and peripheral circuits, it is used to convert those RF signals to an intermediate frequency (IF). Due to the Doppler shift, the frequency of the received signal would not be 1575.42 MHz accurately, there will be some deviation. The GP2015 degrades the signal frequency from 1575.42 to 4.309 MHz by three-stage down-conversion [4]. The first level and second level of the filter must be designed separately, and the third level of the filter has been integrated within the chip. After down-conversion, the IF analog signal is discrete into two bits digital signal after sampling, one is amplitude bit, and another one is sign bit. The sampling frequency is 5.714 MHz and the digital IF signal after sampling is 1.405 MHz. The baseband signal processing part is complemented

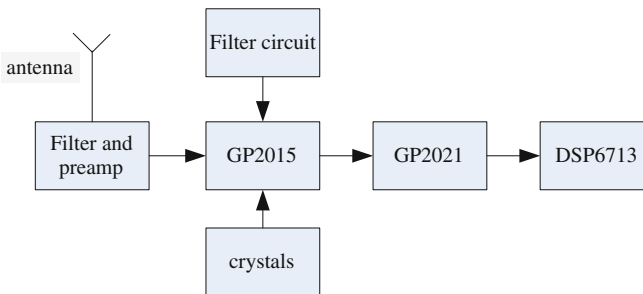


Fig. 1.1 GPS receiver hardware system block diagram

through the combination of hardware and software, which includes the correlator and the DSP, playing a role of capturing and tracking the satellite signals. The correlator controlled by the DSP has integrated 12 correlation channels, as well as Carrier generator, the pseudo-code generator and the points clear.

1.3 Satellite Signals Acquisition

The algorithm of satellite signal acquisition is mainly linear search, parallel frequency search and parallel code phase search method. In this paper, a linear search method to search for satellite signals with the multi-channels correlator because this method is relatively simple.

Figure 1.2 shows the block diagram of the linear search for satellite signal. Firstly, the receiver searches the satellite signal with step of 500 Hz. When the satellite signals are searched, a 100 Hz frequency is adopted to refine the Doppler shift and the estimated value of the code phase. After refining, the capture should be verified, and then the satellite signals are captured for certain (Fig. 1.3).

At the beginning of search, the eudipleural search is executed with the search step-length of 500 Hz and centered on 1.405 Hz. When the signal amplitude calculated in a search unit is greater than the predefined threshold, there are may be some signals in the unit. Then make the unit as a search centre, with the search step 100 Hz, search seven times symmetrically to find out the unit which has the largest non-coherent integral amplitude as the capture result. By doing this, we can control the frequency error within the range of 50 Hz. After captured the satellite

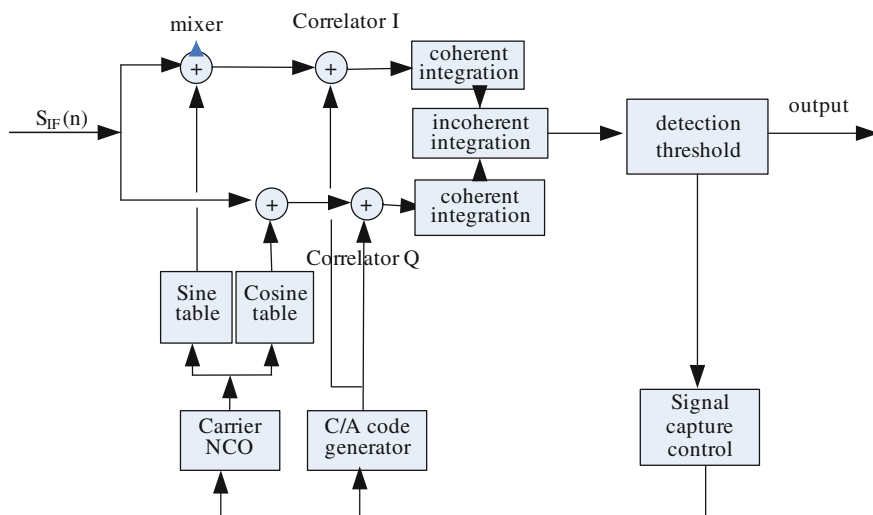


Fig. 1.2 The block of linear search method

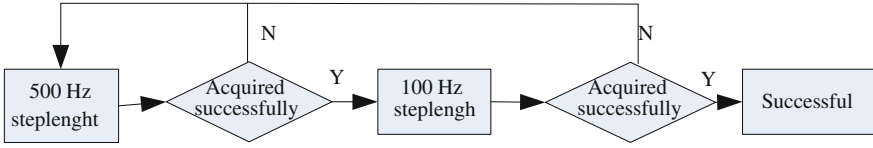


Fig. 1.3 The search flowchart

signals, we use Tong Search Recognition Act to make sure the unit does exist in the visible satellite signal. In the search process, the pseudo-code search step is 0.5 code chip, and with the error of 0.25 code chip.

1.4 Satellite Signals Tracking

After the satellite signals have been captured, the satellite signals should be tracked in real time. A combination method of FLL, the PLL and the code loop is used in here. When designing the tracking loop, the order of the tracking loop should be set firstly, and then the bandwidth of the tracking loop is selected, which is the most important parameter in the design of the tracking loop.

1.4.1 Carrier Tracking Loop

A combination of PLL and FLL is used for Carrier tracking loop. The PLL uses a narrower noise bandwidth, which can track the signals more closely. The output of the carrier phase measurement are more accurately, and the demodulated data bit error rate is low, but it has a poor performance under the dynamic stress; While FLL can adopt a wide noise bandwidth, it has a good dynamic tracking performance while tracking the signals with the low signal to noise ratio. However, the FLL signal tracking is not close enough and the demodulation of the bit error rate is high [5].

Consider the relative motion between the satellite and user, the GPS receiver will be interfered by the excitation signal of frequency ramp. Under this interference, only the third-order or more than third-order phase-locked loop can track the signal accurately. However the second-order FLL can achieve the performance of third-order PLL, therefore, a 3rd-order PLL assisted by 2nd-order FLL will adopted to track the signals.

The following table lists the characteristics of the phase detector and the frequency detector in this paper (Table 1.1).

When the phase difference or frequency difference are detected, a loop filter is used to filter high frequency signal and noise. The block diagram of the loop filter is shown in Fig. 1.4.

Table 1.1 The Discriminator characteristics

	Calculation method	Advantage	Disadvantage
Phase detection algorithms	$\Phi_e = \arctan(Q/I)$	Phase accurate, insensitive to the data transition	Calculation large
Frequency detection algorithms	$w_e = \frac{P_{cross} \times \text{sign}(P_{dot})}{t(n) - t(n-1)}$	Calculation small, insensitive to the data transition	Frequency pull-in range of small

It can be seen from the figure that the loop filter of the FLL is one integrator ahead than the PLL filter. Since the output of the frequency discriminator is frequency difference, it changes to be a phase difference after passing away the integrator, and then the local carrier frequency is adjusted by adjusting the digital controlled oscillator (DCO).

The process of loop filter which is implemented by software is shown as follows.

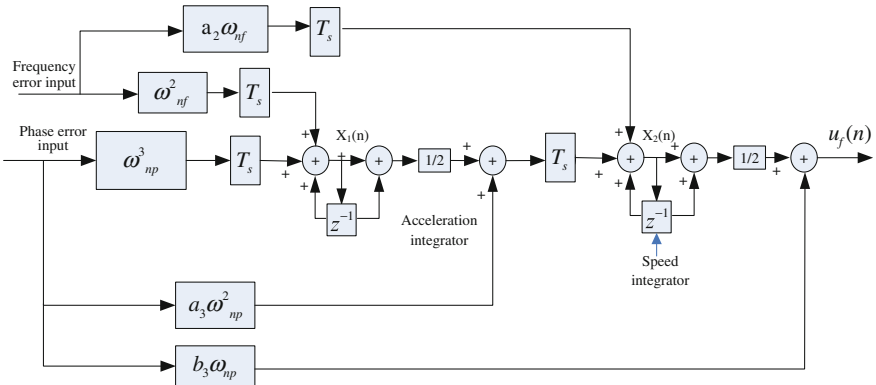
$$X_1(n) = \Delta f(n)\omega_{nf}^2 T + \Delta p(n)\omega_{np}^3 T + X_1(n-1) \quad (1.1)$$

$$X_2(n) = +\Delta p(n)a_3\omega_{np}^2 T + X_2(n-1) + [\Delta f(n)\omega_{nf}^2 T + \Delta p(n)\omega_{np}^3 T + 2X_1(n-1)]T/2 + \Delta f(n)a_2\omega_{nf} T \quad (1.2)$$

$$u_f(n) = [\Delta f(n)a_2\omega_{nf} + \Delta p(n)a_3\omega_{np}^2]T/2 + [\Delta f(n)\omega_{nf}^2 T + \Delta p(n)\omega_{np}^3 T + 2X_1(n-1)]T/4 + X_2(n-1) + \Delta p(n)b_3\omega_{np} \quad (1.3)$$

where $X_1(n)$ and $X_2(n)$ are the intermediate variables, $\Delta f(n)$ and $\Delta p(n)$ are the output of the frequency discriminator and the phase detector, respectively. $u_f(n)$ is the output of the loop filter which controls the frequency of the carrier digital controlled oscillator to adjust the output signal frequency.

The parameters of loop filter are shown in Table 1.2 [6].

**Fig. 1.4** The carrier tracking loop

1.4.2 Pseudo-code Tracking Loop

The code loop assisted by carrier is adopted in this system. The Doppler shift measured values of the carrier loop can be used to assist the code loop for adjusting the bit rate. Because the Doppler frequency shift of the pseudo-code is much smaller than the carrier Doppler frequency shift, the carrier aiding is 1/1540 of carrier wave. Figure 1.5 shows the block diagram of code tracking loop.

With the aid of the carrier loop, second-order code loop do not need high order filter any more. So a two-order code loop is adopted here. The non-coherent early minus late method is used while detecting the phase difference in the code loop. Calculation method is shown as follows [7].

$$\frac{1}{2} \frac{\sqrt{I_E^2 + Q_E^2} - \sqrt{I_P^2 + Q_P^2}}{\sqrt{I_E^2 + Q_E^2} + \sqrt{I_P^2 + Q_P^2}}$$

This phase detection algorithm has a large computing and needs two pairs of correlators, but it has a small errors.

1.5 Experiment Results

Based on the design method of the loop, we developed a high-dynamic GPS receiver principle prototype as Fig. 1.6 shows.

The experiments include static and kinematic. Figure 1.7 shows the non-coherent integration amplitude of the promote branch and the promote branch while searching the seventh satellite while the receiver is in static state. While the non-coherent integration amplitude of the two branches exceeds the preset threshold, the system considers that the coarse acquisition is successful, and signals may exist in the current unit.

Because the vehicle-mounted experiment is unable to get an enough high speed, so here we used the high dynamic satellite signal simulator to test the tracking performance of the tracking loop. When the FLL bandwidth is set to 18 Hz, the PLL bandwidth is set to 10 Hz, the receiver principle prototype can track 100 g/s high dynamic signal. The test results show that the receiver principle prototype have achieved the desired indicators, it can search the satellites signal and Complete Satellite Positioning under the high dynamic environment.

Table 1.2 The Loop filter characteristics

Loop order	BW of noise	Filter parameters	Steady state error	Characteristics
Second order	$\frac{\omega_0(1+a_2^2)}{4a_2}$	$a_2\omega_{hf} = 1.414\omega_{hf}$ $B_n = 0.53\omega_{hf}$	$\frac{d^2R/dt^2}{\omega_{hf}^2}$	Sensitive to stress of acceleration. Unconditionally stable for all the noise bandwidth
Third order	$\frac{\omega_0(a_3b_3^2+a_3^2-b_3)}{4(a_3b_3-1)}$	$a_3\omega_{hp}^2 = 1.1\omega_{hp}^2$ $b_3\omega_{hp} = 2.4\omega_{hp}$ $B_n = 0.7845\omega_{hp}$	$\frac{d^2R/dt^3}{\omega_{hp}^3}$	Sensitive stress jerk. When the bandwidth is less than or equal to 18 Hz it can remain stable

Fig. 1.5 Code loop structure

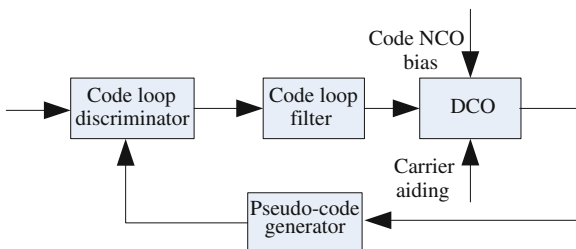


Fig. 1.6 High dynamic satellite positioning receivers principle prototype

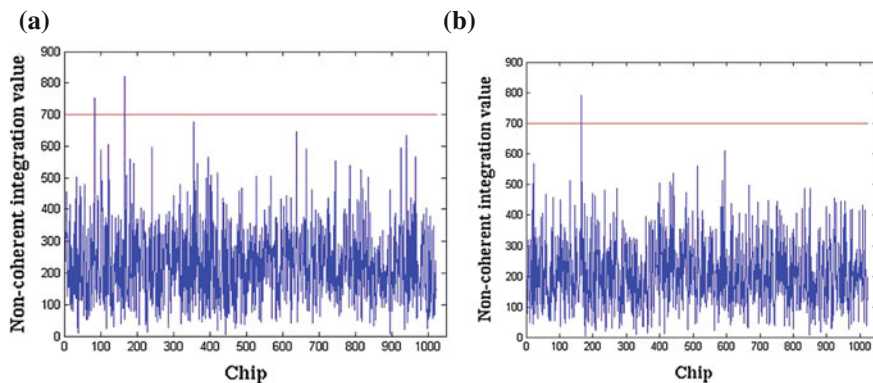
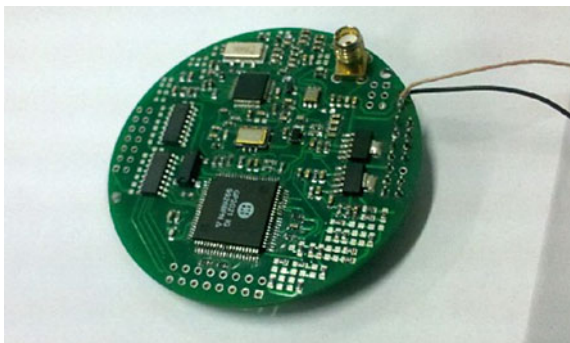


Fig. 1.7 Non-coherent integration values of the No. 7 satellite (Band 0) **a** the early branch **b** the promote branch

1.6 Conclusion

This paper proposed a novel design program of high dynamic GPS receiver, whose phase-locked loop bandwidth is 10 Hz, frequency-locked loop bandwidth 18 Hz, and code loop bandwidth 2 Hz. The experiment shows that the receiver prototype could satisfy the error limits of the tracking loop, and it also can capture the visible satellite signals with a good effect of real-time tracking lock.

References

1. Tian, M., Shao, D., Cheng, N., Xue, W.: A scheme for high dynamic GPS receiver. *Telemetry & Telecontrol* **23**(2), 15–20 (2002)
2. Ma, X., Liu, B.: Design of an INS aided high dynamic GPS receiver. *Electronics, Communication and Control (ICECC)*, pp. 1404–1407. Ningbo, China (2011)
3. Li, J., Ba, X., Chen, J.: New high dynamic GPS receiver carrier tracking algorithm based on IMM. *J. Syst. Simul.* **20**(9), 2483–2486 (2008)
4. Xin, Z., Li, J., Liang, H., Wang, F., Yan, Y.: Design of a GPS receiver based on ARM and FPGA. *Transducer Microsyst. Technol.* **30**(7):108–110 (2011)
5. Xie, G.: *Principle of GPS Receiver Design*. pp. 78–85, Electronic Industry Press, Beijing (2009)
6. Kaplan, E.: *Understanding GPS: Principles and Applications*. pp. 180–181, Artech House, Inc., Norwood (2006)
7. Parkinson, B.: *Global Positioning System: Theory and Applications*. pp. 245–325, American Institute of Aeronautics and Astronautics, Reston (1996)