Chapter 4
Design of Data Acquisition Systems

Abstract In this chapter the main aspects of the design and a possible system will be described. The idea is to develop a design approach that can be a guide for future electronic designer. By this, an approach with general description of requirements will be presented.

4.1 Introduction to the Design

Today, computer-based system used in many applications are composed of simple stand-alone personal computer with board connected or microprocessor-based systems to realize a complete network of minicomputers. Such systems are used in many real time applications including process control and monitoring. Design process of data acquisition systems (DASs) is an obscure process. It is possible to consider system design in two principal phases: functional design and final design. The functional design is visualized in Fig. 4.1. The first step is to value the requirements according to the user. The second step is to translate the specific requirements in electric criteria, for example: accuracy and bandwidth. At the end, the third step is to establish a specific configuration of the system [1, 4].

4.2 Functional Design of High Speed Computer-Based DAS

The goal of this study is to describe a technical note used to design a high speed computer-based DAS [1–4].

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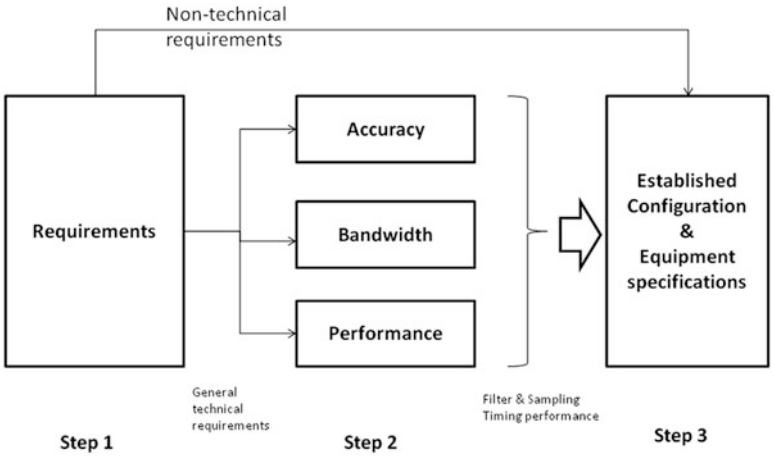

Fig. 4.1 Functional design: outline

4.2.1 Requirements

The requirements, in according to the first step, can be described in the following points (we will make an example):

Analog Input Channels: the system is designed to store 64 channels of analog data. The analog signals have a maximum differential voltage range of 10 V. Some transducers will be used to convert the signal in electrical form.
Analog Output Channels: the system is designed for a parallel transmission of eight analog signals reconstructed from digital form stored in memory board. All output analog signals (maximum voltage range 10 V–10 kΩ) are in singled-ended mode. According to the parallel transmission, the system is planned for simultaneous outputting of eight channels with bandwidth of DC-5 kHz.
Accuracy: the mean squared error between an analog signal and its reconstruction in output can be defined by the following equation:

$$\frac{\int_{T_1}^{T_2}[y(t)-x(t)]^2\mathrm{d}t}{\int_{T_1}^{T_2}[y(t)]^2\mathrm{d}t} \tag{4.1}$$

With $x(t)$ is the analog input signal, $y(t)$ is the analog output signal, and $T_2 - T_1$ is the analysis interval. This value must not exceed 0.2 %. This equation and corresponding variables are subject to the following conditions:

- Output signal are reconstructed from digital data stored in memory board.
- All input signals are considered of low pass type.
- The accuracy will be applied to each input and output signals at a data rate up to maximum frequency.
- System gain is unitary.

Analog Data Sampling Frequency: It is important to have an high accurate reproduction of the signals for each input corresponded to the bandwidth. The sampling frequency can be selected manually or via computer. The system will permit the simultaneous collection of 64 channels with bandwidth DC-5 kHz. The frequency sampling is designed according to the highest frequency of the bandwidth, the maximum level of attenuation for aliasing frequencies, and roll-off of the anti-aliasing filter.
Anti-Aliasing Filters: Each analog input will be provided with an anti-aliasing filter; it will be managed manually or via computer.
Minimum and Maximum Analysis Times: the system will be capable to store 64 analog channels with time interval from 10 ms to 1 s according to the sampling frequency. Accuracy of time interval should be of about $\pm 25\,\mu s$.
Analysis Bandwidth: The data bandwidth of any input or output channel will be operated from a minimum of DC-2.5 kHz to the maximum of DC-25 kHz in conformity with the sampling frequency.
System Calibration Program: A program is designed to verify that the DAS is operated following the requirements. The program will locate which element is not in work.
Data Collection Program: A program that starts and stops the recording of 64 analog channels. In particular the program is designed to have the following operations: set the number of data input, select the bandwidth, the data interval, the sampling rate, and the gain of input channel signal conditioner.
Transducer Calibration Program: A program is designed to make the test and calibration of the transducers. All calibration data are stored in memory board or exported in other mass storage devices.
Temperature: The system is designed to operate in a temperature range of, for example, $-10°–+70°$ without damage. Normally, the system will be operated at a temperature of 20°.
Shock and Vibration: The system is designed to resist from the repeated shock and/or vibration. Vibrations of, for example, 15.24 mm double amplitude at frequency from 5 to 60 Hz.

4.2.2 Analysis of Accuracy (Static)

Equation (4.1) can be indicated in the following form:

$$\frac{\int_{T_1}^{T_2}[y(t)-x(t)]^2\mathrm{d}t}{\int_{T_1}^{T_2}[y(t)]^2\mathrm{d}t} \leq \frac{0.2}{100} \tag{4.2}$$

$$E = y(t) - x(t) \tag{4.3}$$

$$y(t) = C \tag{4.4}$$

Then

$$\frac{\int_{T_1}^{T_2}[E]^2 \mathrm{d}t}{\int_{T_1}^{T_2}[C]^2 \mathrm{d}t} \leq 0.002 \tag{4.5}$$

$$\frac{E^2(T_2 - T_1)}{C^2(T_2 - T_1)} \leq 0.002 \tag{4.6}$$

$$E \leq (0.044)C \tag{4.7}$$

The static accuracy requirement is interpreted to be 0.044 times of input. If we design a data system with:

$$(0.044)C = 0.2 \tag{4.8}$$

and $I = 10\,\mathrm{V}$ for example, C will be 0.45 V.

4.2.3 Analysis of Accuracy (Dynamic)

About the accuracy of dynamic signal analysis, some possible discussion can be described as below:

Filter Pass-Band Ripple: We consider specifications of 0.1 dB for pass-band ripple. For full scale (10 V), this value is corresponded to an error of:

$$0.1\ \mathrm{dB} = 20\log(e_0/e_1), e_1 = 10\,\mathrm{V} \tag{4.9}$$

$$\mathrm{e}_0 = 9.885 \tag{4.10}$$

The error is 1.2 %. At the level of 1 V, for example, the component of ripple error represents a value of 11.4 % on the reading.

Aperture and Input Filter Consideration: Aperture time is the width of the sampling window. The value of aperture time can be estimated assuming a sinusoidal input and calculating by the time required for input to change less than the resolution. For 14 bit converter with 5 kHz input, the time to maintain error less than resolution is 3.9 ns.

In the first chapter we have described the problems about the communication cabling; a cable for connecting the test transducer of the conditioner device is used. It is composed of resistance and capacitance, the capacitance in conjunction with the resistance of the transducer forms a low-pass RC filter that can attenuate high frequencies. Using a cable with about 160 pF/m (C) and output sensor impedance of 300 ohm (R), the effective filter for 100 m for example is:

$$RC = 300 * 160 * 10^{-12} * 100 = 3 * 10^{-6} s \tag{4.11}$$

The filter's transfer function can be described by the following equation:

$$G(\mathrm{i}\omega) = \frac{1}{1 + \mathrm{i}\omega RC} \tag{4.12}$$

with

$$\text{Amplitude} : |G(\mathrm{i}\omega)| = \frac{1}{(1 + (\omega RC)^2)^{1/2}} \tag{4.13}$$

$$\text{Phase} : \theta = -\tan^{-1}(\omega RC) \tag{4.14}$$

The effective filter for the cable and sensor has a cutoff of 53 kHz. According to the specifications, we want to process the information for all sensors at frequencies up to 5 and 25 kHz. The errors introduced can be valued in the following way: Amplitude 0.44 % and phase -5.4° at 5 kHz, Amplitude 9.5 % and phase -25° at 25 kHz. The sampled data are used to reconstruct the analog signal by using a D/A converter, then this value is compared with input to value the error. The error is described by a zero-order hold:

$$\text{AmplitudeError}, \% = (1 - \sin x/x) \times 100 \tag{4.15}$$

with

$$x = \pi(f/f_s) \tag{4.16}$$

f_s is the sampled frequency; and for the phase:

$$\text{PhaseDegrees} = \pi(f/f_s) \tag{4.17}$$

ADC Resolution According to magnitude of the error, we can estimate the resolution of ADC considering that all aliases must be attenuated by at least 80 dB, thus implying that the system's dynamic range is at least 80 dB:

$$\text{db} = 20\log(\text{ADC} - \text{resolution}) = 0.0001 \tag{4.18}$$

Thus, it is required a 14-bit A/D converter.
Bandwidth The bandwidth is calculated to be 5 kHz expandable to 25 kHz for some channels conveniently selected, with all aliases attenuated by at least 80 dB.

We assume that the frequency content of the analog signal is visualized in Fig. 4.2, with f_c the highest frequency of interest. If we use a filter with cut-off f_a with roll-off rate *Rdb*/octave, we can conservatively establish the highest frequency as f_a. We can choose the holding frequency f_n to be:

$$\log f_n = \log f_c + \frac{\log f_a - \log fc}{2} = \frac{1}{2}\left(\log f_c + \log f_a\right) \tag{4.19}$$

$$f_n = \log^{-1}\left(\frac{1}{2}\log f_a\right) \tag{4.20}$$

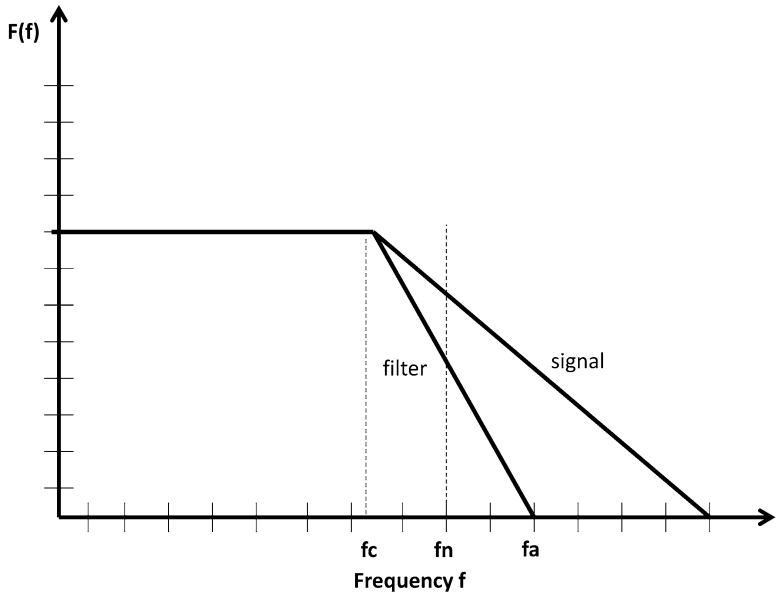

Fig. 4.2 Frequency content

Rolloff Rate	N	F_c (kHz)	F_n (kHz)	F_s (kHz)
12 dB/octave	6.6	500	50	100
24	3.3	50	15.8	31.6
36	2.2	23.2	10.8	21.5
48	1.6	15.8	8.9	17.8
80	1	10	7.1	14.1

Fig. 4.3 Filtering and sampling rate

To establish an acceptable distortion we can value it by using the following equation:
Establish number of octaves above f_c where input is attenuated by dB level:

$$N = \frac{\text{Attenuation} - \text{dB}}{RdB/\text{octave}} \tag{4.21}$$

Folding and sampled frequency:

$$f_n = \log^{-1}\left(\frac{1}{2}\log f_a\right) \tag{4.22}$$

$$f_s \geq 2f_n \tag{4.23}$$

Considering a distortion of 80 dB we can value the filtering with consideration according to Fig. 4.3: Based on these data, the sampling rate for individual channel for a 5-kHz of bandwidth can change from 14 to 100 kHz depending of roll-off rate of the filter.

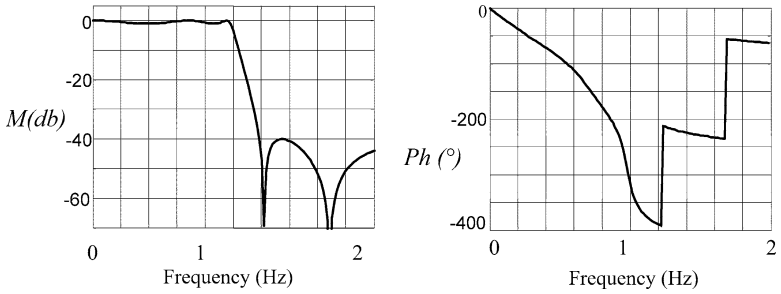

Fig. 4.4 Elliptic filter

Filter selection: Conforming with above considerations, we can use a elliptic filter (Fig. 4.4) defined by the following parameters:

- Roll off rate: 80 dB/octave
- Ripple: 0.1 dB pass band and stop band
- Phase linearity: linear over the range: $0.1 \leq \frac{f}{f_c} \leq 0.33$

An elliptic filter (also known as a Cauer filter) is a filter with equalized ripple behavior in both of the passband and the stopband. The ripple can be adjustable for each band independently. The gain of a lowpass elliptic filter is given by:

$$G_n(\omega) = \frac{1}{\sqrt{1 + \varepsilon^2 R_n^2(\zeta, \omega/\omega_0)}} \tag{4.24}$$

where: ω_0 is cut-off frequency, ε is the ripple factor, ζ is the selectivity factor, and R_n is the nth-order of Chebyshev rational function.
Sampling Frequency: For a bandwidth of 5 kHz, we design the cut-off of the filter to 15 kHz to obtain linear phase requested. With $f_c = 15$ kHz, we compute the following parameters: N = 1, $f_a = 30$ kHz (effective cut-off frequency), $f_n = 21.2$ kHz, and $f_s = 42.4$ kHz. With these, amplitude error is 2.3 % and phase is 3.7°.
Signal Conditioner, Amplifier, Multiplexer, and ADC: Each channel required to include a differential amplifier which CMRR of 80 dB, a differential input impedance of 20 MΩ, offset current of 30 nA, and adjustable sensitivity from ±1 to ±100 mV. Instrumentation amplifiers (differential amplifier) amplify small differential voltages in the presence of large common-mode voltages, while offering a high input impedance. This characteristic has made them attractive to a variety of applications, such as strain-gauge bridge interfaces for pressure and temperature sensing, thermocouple temperature sensing, and a variety of low-side and high-side current-sensing applications [5]. The classic three-op-amp instrumentation amplifier (see Fig. 4.5) offers excellent common-mode rejection and accurate differential gain programmable by a single resistor. The architecture is based on a two-stage configuration: the first stage provides unity common-mode gain and all (or most) of the differential gain, while the second stage provides unity (or small) differential-

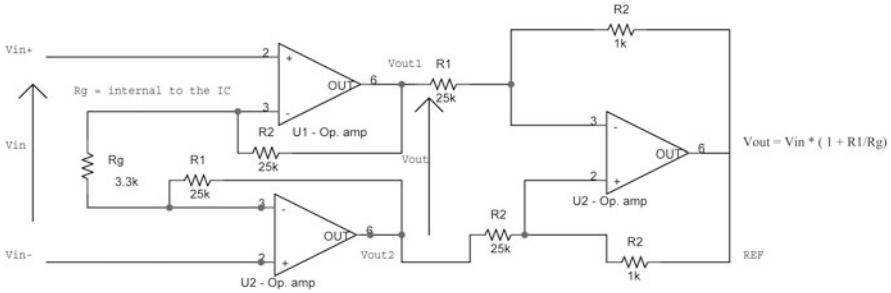

Fig. 4.5 Differential amplifier

mode gain and all of the common-mode rejection. Example of differential amplifier is MAX4198/99. The MAX4198/MAX4199 low-power, rail-to-rail differential amplifiers are ideal for single-supply applications that benefit from a low 0.01 % gain error. The MAX4198 is factory trimmed to a fixed gain of +1 V/V, and the MAX4199 is trimmed to a fixed gain of +10 V/V. Capable of operating from a single +2.7 to +7.5 V supply or from dual ±1.35 to ±3.75 V supplies, they consume only 42 µA while achieving −3 dB bandwidths of 175 kHz (MAX4198) and 45 kHz (MAX4199). These amplifiers feature a shutdown mode that reduces the supply current to 6.5 µAA. The MAX4198/MAX4199 can drive 5 kΩ loads to within 100 mV from each rail. The standard differential amplifier configurations provide common-mode rejection of 90 dB for the MAX4198 and 110 dB for the MAX4199. The input common-mode voltage range for the MAX4198 extends 100 mV Beyond-the-Rails [6].

The system is required to support 32 channels concurrently. It is preferable if a multiplexer/ADC is chosen with the sampling capability to accommodate all 32 channels, in other case we should use multiple ADC. We can define aggregate throughput F_s based on sampling frequency f_s for 5 kHz of bandwidth:

$$F_s = n - \text{channels} * f_s = 1357\,\text{kHz} \tag{4.25}$$

We can use eight separate 1 MHz ADCs-14 bit MAX1324 of Maxim, each of 32 input channels: the processor must be capable to accept 2 Mbyte/s of data at the same time.

The MAX1324 (Fig. 4.6) is 14-bit ADC eight channels independently selectable. Simultaneous sampling of all active channels preserves relative phase information. These devices are available ±10 V input ranges. The 0 to +5 V devices feature ±6 V fault-tolerant inputs. All eight channels convert in 3.8 µs, with a maximum eight-channel throughput of 263 ksps per channel. Internal or external reference and internal- or external-clock capability offer great flexibility and ease of use. A write-only configuration register can mask out unused channels, and a shutdown feature reduces power. A 16.6-MHz, 14-bit, parallel data bus outputs the conversion result [7].

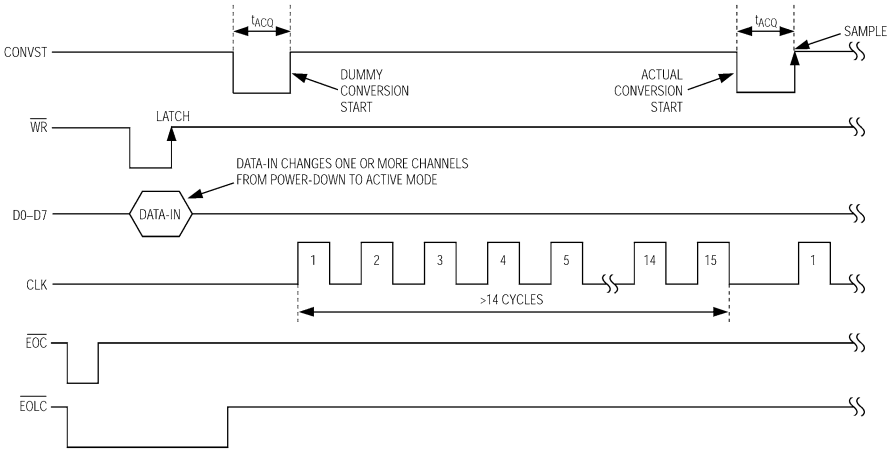

Fig. 4.6 Timing diagram of MAX1324 of Maxim [7]

Figure 4.7 shows the functional diagram of these devices. To preserve phase information across these multichannel devices, each input channel has a dedicated T/H amplifier. Use a low-input source impedance to minimize gain error harmonic distortion. The time required for the T/H to acquire an input signal depends on the input source impedance. If the input signals source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. The acquisition time (t_1) is the maximum time that the device takes to acquire the signal. Use the following formula to calculate acquisition time:

$$t_1 = 10 * (R_S + R_{IN}) * 6pF \tag{4.26}$$

where $R_{IN} = 2.2\,\text{k}\Omega$, R_S is the input signals source impedance, and t_1 is never less than 180 ns. A source impedance of less than 100Ω does not significantly affect the ADCs performance. To improve the input-signal bandwidth under AC conditions, drive the input with a wide band buffer (>50 MHz) that can drive the ADCs input capacitance and settle quickly. The T/H aperture delay is typically 13 ns. The aperture delay mismatch between T/Hs of 50 ps allows the relative phase information of up to eight different inputs to be preserved. During shutdown, the analog and digital circuits in the device power down and the device draws less than 100 µA from AVDD, and less than 100 µA from DV_{DD}. Select shutdown mode using the SHDN input. Set SHDN high to enter shutdown mode. After coming out of shutdown, allow a 1-ms wake-up time before making the first conversion. When using an external clock, apply at least 20 clock cycles with CONVST high before making the first conversion. When using internal-clock mode, wait at least 2 µs before making the first conversion [7]. The outline of the DAS can be visualized in Fig. 4.8.

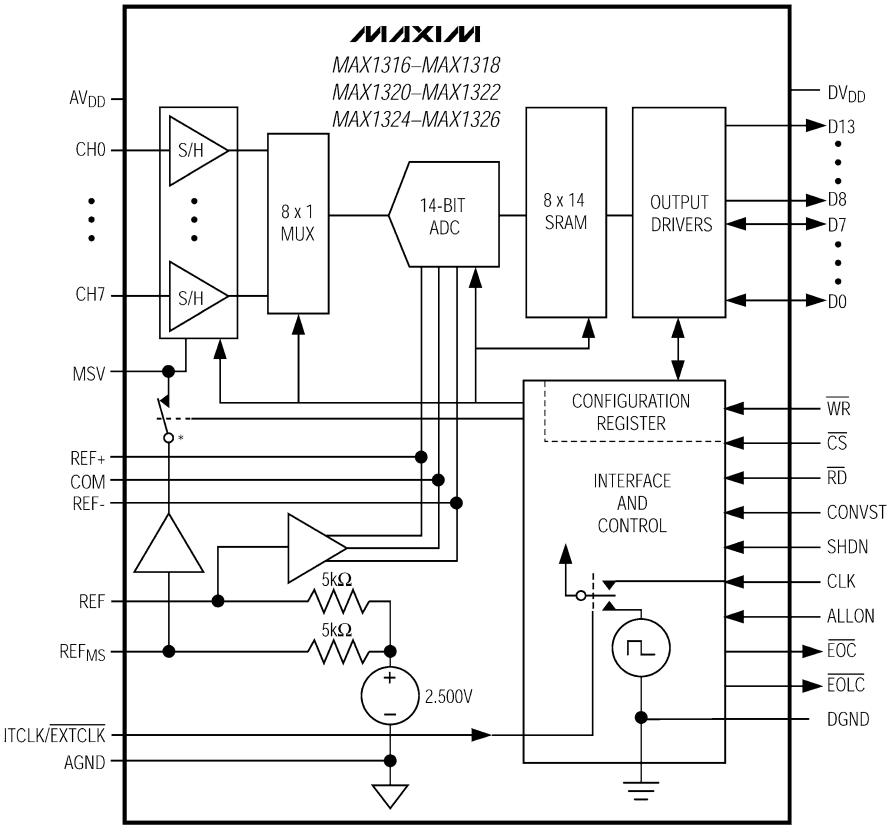

Fig. 4.7 Functional diagram of MAX1324 of Maxim [7]

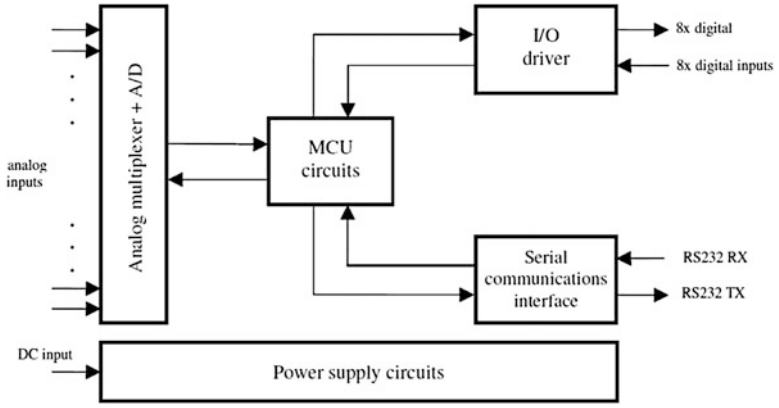

Fig. 4.8 Outline of DAQ hardware

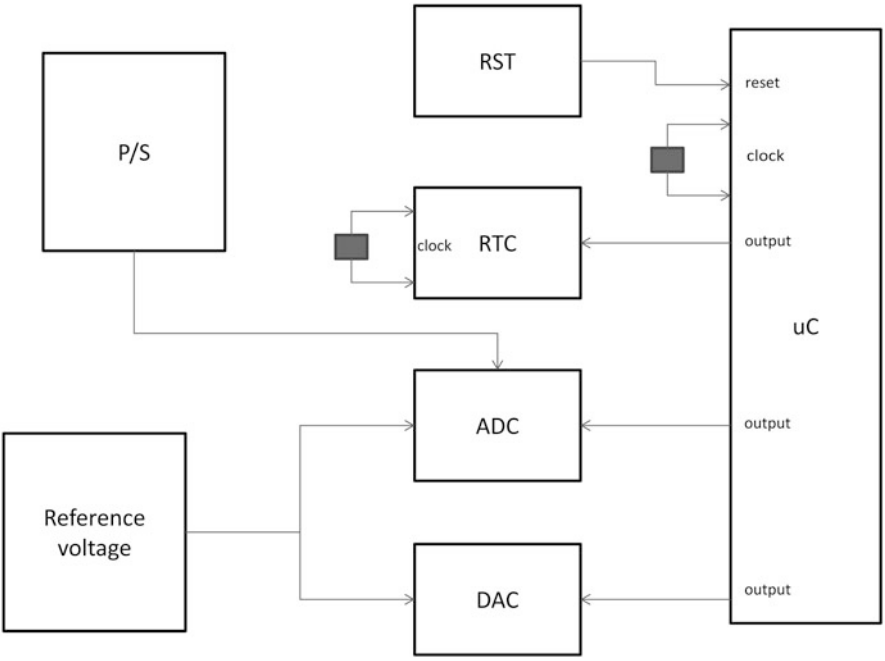

Fig. 4.9 Block diagram of portable data acquisition system [8]

4.3 Portable DAS

The hardware and software design of a portable measurement system is more complicated than just choosing the right IC to meet the required electrical performance. There are many tradeoffs to be considered. For example: size respect to the board, total cost, life cycle, and so on. At one extreme is a discrete design using readily available standard components and at the other extreme is a custom design using a single mixed-signal chip. The following will compare a discrete design to a design using the MAX1407 of Maxim Integrated.

Figure 4.9 shows the functional block diagram for a portable DAS using discrete components. The system includes power, analog, and digital circuitry. The power is derived from the batteries, with a power supply for a regulated output voltage. The battery voltage can be measured on demand with the A/D converter and there are reset circuits for the battery and the regulated output voltage. The analog includes the analog front end (AFE) circuitry (which may include D/A converters, op-amps, and analog switches) to interface with an electrochemical sensor, a thermistor circuit to measure temperature, an A/D converter with an input multiplexer, and a voltage reference for use with the AFE, thermistor, and A/D converter. The digital circuitry includes a 32-kHz oscillator, real-time clock (RTC), and a microcontroller including a high-frequency crystal, external interrupts for the user interface, internal memory,

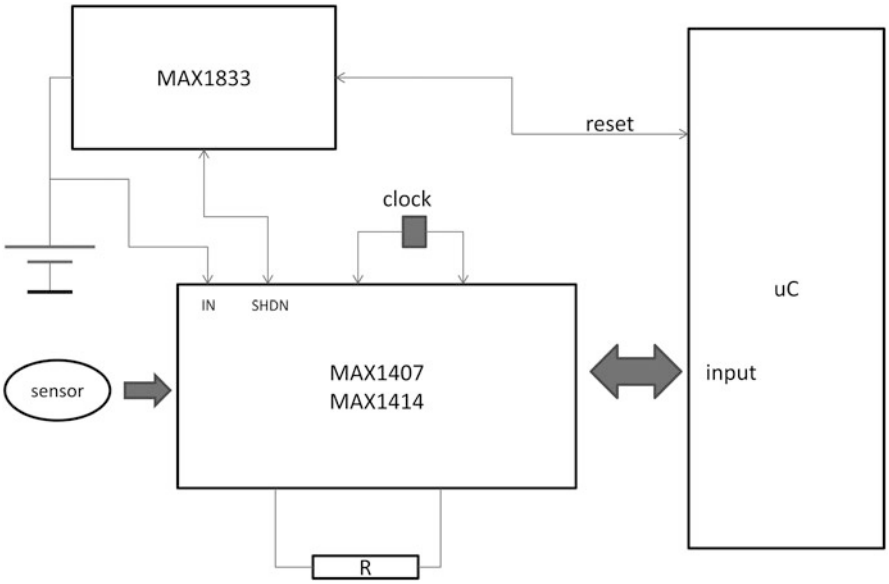

Fig. 4.10 Block diagram of portable data acquisition system using MAX1407 [8]

and possibly other peripherals, such as a liquid crystal display (LCD) bias and driver circuit to interface to an LCD. The sensor shown in Fig. 4.9 is an electrochemical type sensor configured in a counter configuration where the working electrode (WE) is biased via the FB1 pin. The external resistor between FB1 and OUT1 configures the force/sense D/A converter as a transimpedance amplifier to measure the current through the sensor. The reference electrode (RE) is biased via the FB2 pin, and the feedback loop is closed through the sensor impedance to the OUT2 pin to regulate a constant potential between WE and RE over varying sensor currents. In Fig. 4.10 is shown, instead, the functional block diagram for the same portable DAS using the MAX1407, simplifying the system design in Fig. 4.9. The MAX1407 contains all the circuitry required [8].

4.4 Design Guidelines for High-Performance, Multichannel

Many advanced industrial applications require the use of high-performance, simultaneous-sampling, multichannel ADCs. Consider as examples an advanced power-line monitoring (Fig. 4.11) or contemporary three-phase motor-control system (Fig. 4.12). These applications require accurate simultaneous, multichannel measurement over a wide dynamic range of 70–90 dB (depending on the application). A sample rate of 16 ksps or higher is common. Each power phase

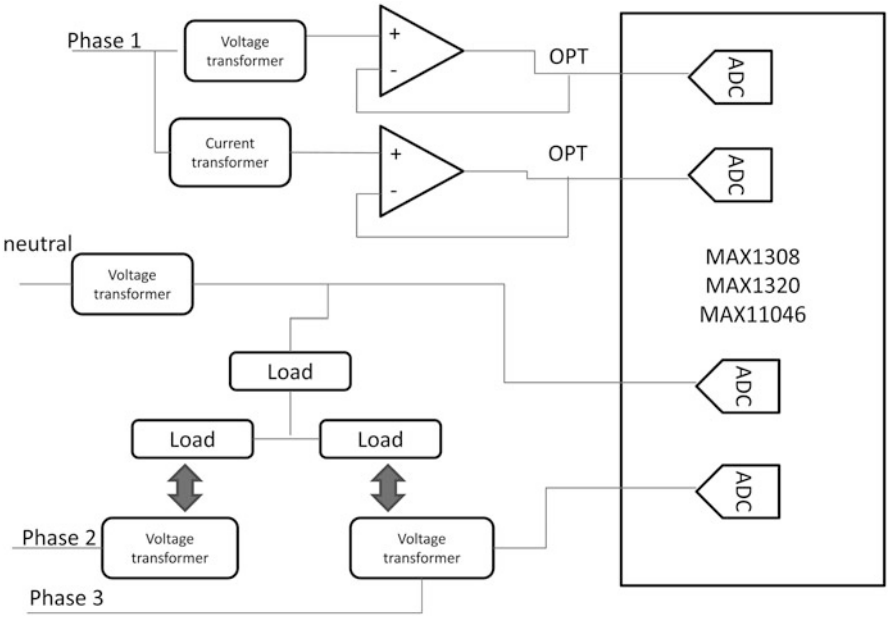

Fig. 4.11 Advanced power-line monitoring

in Fig. 4.11 is represented by a current transformer (CT) and a voltage transformer (PT). The complete system is comprised of four such pairs (one pair for each of the three phases plus neutral).

Two classes of noise/interference can be defined in the DAQ. The first class of noise comes from the internal electronic component noise. Sources include ADC conversion process noise and harmonic distortion, buffer amplifier noise and distortions, and reference noise and stability. A second source of interference is the system's external environment. Examples include external electromagnetic noise, power-supply noise/ripple, I/O pin crosstalk, and digital system noise and interference. These various noise sources are shown in Fig. 4.13.

General PCB Layout Guidelines: Several important PCB guidelines will help achieve the best performance in multichannel, simultaneous-sampling DAQ (DAQ or DAS) applications.

- Use PC boards with ground planes.
- Ensure that the analog and digital lines are separated from each other.
- Do not run digital and analog lines parallel to one another.
- Avoid running digital lines underneath the ADC package.
- Use a single, solid GND plane with digital signals routed from one direction and analog signals from the other.

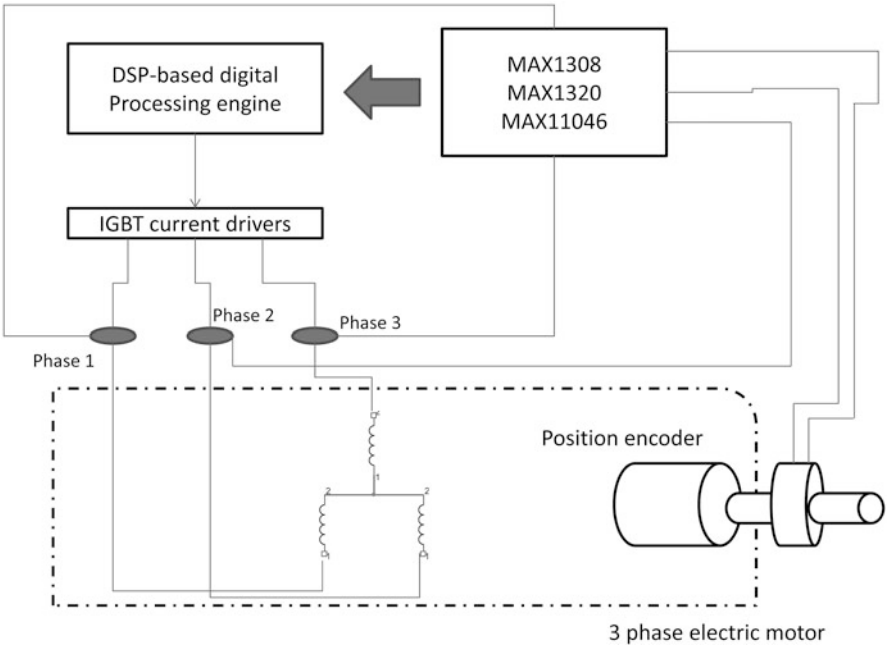

Fig. 4.12 Typical power-grid monitoring application [9]

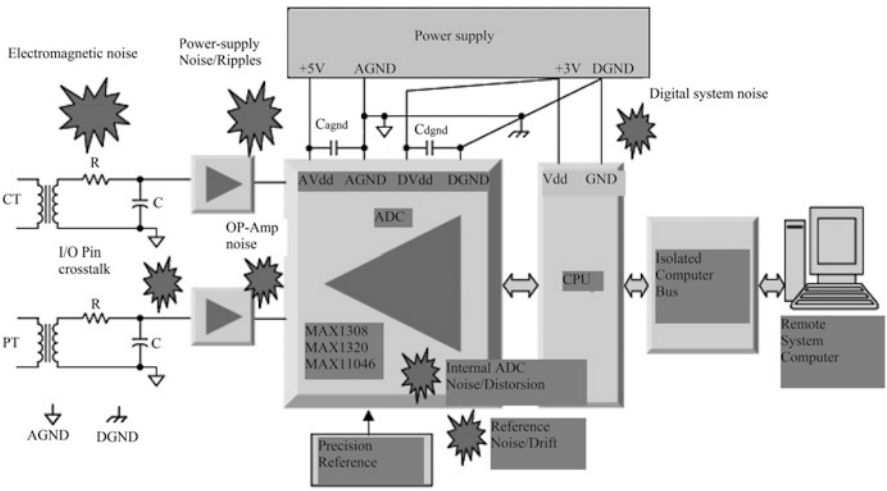

Fig. 4.13 Noise in a data acquisition system [9]

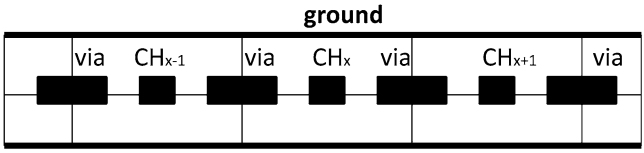

Fig. 4.14 Example of analog input routing [9]

- Keep the ground return to the power supply for this ground low impedance and as short as possible for noise-free operation.

Input PCB traces which carry sensitive analog signals from the connector to the ADC inputs can be subject to noise, interference, and channel-to-channel crosstalk. Special ground and signal shielding of these analog traces is critical to the integrity of the input signal. Figure 4.14 shows an example of a PCB layout intended to protect the analog signal [9].

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