Chapter 8
Analog-to-Digital Conversion

Abstract Several classifications exist of Nyquist-rate analog-to-digital converters. In this chapter the converters are subdivided in parallel search, sequential search, and linear search. Each of these architectures requires a comparator. Therefore this building block is extensively analyzed in all its aspects. The section is concluded with a comparator catalog.

The full-flash converter is the conversion solution for the highest speed range. Moreover it is a building block for more complex converters. Variants, such as gain stage, interpolation, and folding are analyzed and described.

The sub-ranging methods and pipeline converters are the solutions for the medium speed range demands. Next to a treatise on the various aspects of the architecture an analysis is made of the error sources, calibration techniques, and design issues.

In the next sections the successive approximation and linear topologies are discussed. These topologies are slower but receive today more attention as a massive parallelism allows them to compete with the performance of the pipeline converter. The issues associated with multiplexing are analyzed.

Finally some less prominent ideas for conversion are briefly highlighted.

The analog-to-digital converter compares the input signal to a value derived from a reference by means of a digital-to-analog converter (Fig. 8.1). The basic functions of an analog-to-digital converter are the time and amplitude quantization. The circuit ingredients that implement these functions are the sample- or track-and-hold circuit where the sampling takes place, the digital-to-analog converter, and a level-comparison mechanism. The comparator circuit is the location where the signal changes from its preprocessed analog form into a digital decision. After the comparator a digital circuit processes the decisions into a usable digital signal representation.

Various subdivisions of analog-to-digital converters can be made. Based on the timing of the conversion four categories can be identified; see Fig. 8.2:

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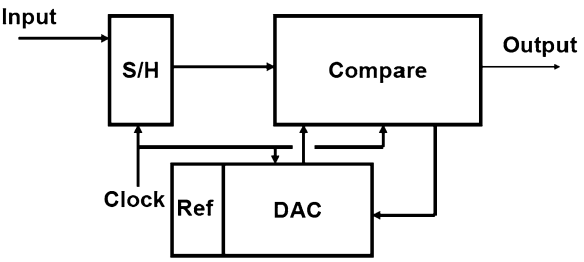


Fig. 8.1 Components in analog-to-digital conversion

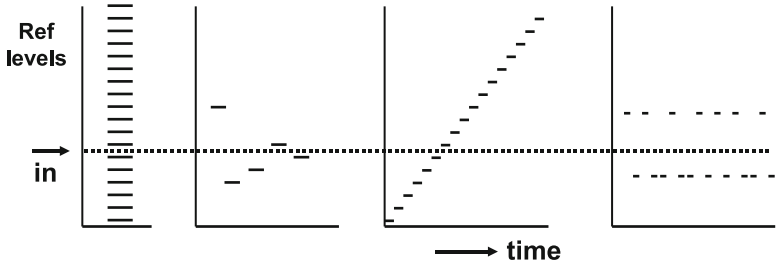


Fig. 8.2 Classification of analog to digital conversion principles. In the vertical dimension the available levels are depicted. *Left*: in direct conversion all levels are provided. The sequential search algorithm chooses the next level based on the information of the previous comparisons. In linear search each level is available at consecutive clock periods. Finally the oversampled conversion switches between a few levels

- The "flash" converters or "parallel search" converters use one moment in time for the conversion. The input signal and all the required reference levels must be present at that time moment. From a topological point of view no sample-and-hold on the analog side is required. The latches in the comparators form a sort of digital hold structure. Fast converters are possible; however, the requirement to provide decisions on 2^N reference levels leads to an exponential growth of the area and power of the converter. An elegant variant is the "folding" converter. Applications that require the highest speed and modest accuracy are served by these converters.
- The second category is the "sequential search" converter. This class builds up the conversion by choosing at every new clock strobe a new set of reference levels based on the information processed up to that moment. For each step a suitable resolution can be chosen, mostly based on a power of 2: 2^1, 2^2, 2^3, etc. A fundamental choice is to use the same hardware for all processing steps of one sample or to use dedicated hardware for each next resolution step. In the last approach the total processing time for a sample is still the same, but more samples can be processed at the same time. Principles in this category are successive approximation conversion, pipeline conversion, and multistep conversion. The combination of high accuracy and rather high speed makes these converters suitable for many industrial and communication applications.

- On the opposite side of the spectrum is the "linear search" converter. All potential conversion levels are in increasing or decreasing order generated and compared to the input signal. The result is an extremely slow conversion, built with a minimum amount of hardware, and tolerant to component variations. An example is the dual-slope converter. The robustness of these converters makes them popular for slow-speed harsh environments, such as sensor interfaces.
- The last category of conversion principles is mentioned here for completeness. The oversampled converters use mostly a few reference levels and the output switches frequently between those reference levels to create a time average approximation of the input. The accuracy comes from the time domain. These feedback-based delta-converters do not provide the conversion result at a determined point in time but are accurate over a larger number of samples. The special techniques and analysis tools for these delta modulators are discussed in Chap. 9.

The first three categories are called "Nyquist converters." These circuits convert a bandwidth[1] close to $f_s/2$ and often operate at the speed limit of the architecture and process. This chapter discusses the flash, subranging, successive approximation and linear converters after a discussion of the comparator.

8.1 Comparator

Every analog-to-digital converter contains at least one comparator. There are as many comparator circuits as there are analog-to-digital converter designers. Many aspects need consideration when designing a comparator. These aspects may vary for every different application, for specific class of signals, a technology, etc. No universal "one design fits all converters" comparator exists. Yet some general remarks on the design of the comparator can be made. Accuracy and speed are the global design parameters that have to be balanced versus the power consumption.

The fundamental task of a comparator is to amplify a big or small difference between its input terminals into a digital decision. In other words to extract the sign of the differential input signal, a number of requirements can be specified for a comparator:

- A large amplification is imperative.
- A wide bandwidth for operating on high-frequency signals.
- Accuracy of various forms is required. In practical terms this means a low input offset, a low noise figure, for 1/f noise as well as for thermal noise. Clocked comparators should not add uncertainty to the decision moment: a low timing jitter is required.
- A low-power consumption, especially in analog-to-digital converters employing a lot of comparators.

[1]This bandwidth can start at DC, but also far above f_s using sub-sampling in Sect. 12.1.4.

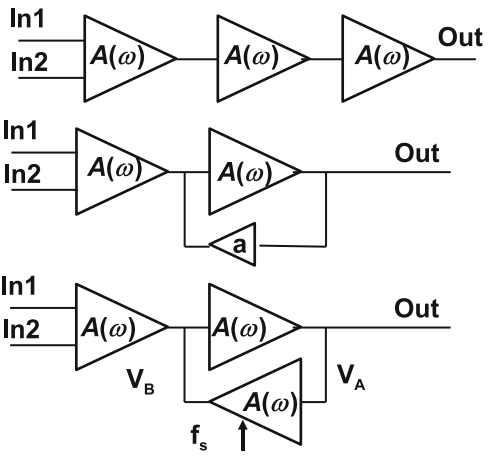


Fig. 8.3 Three basic comparator designs: straightforward amplification, amplifier with hysteresis, and a latched or regenerative amplifier

- A wide input common-mode voltage range, with a high common-mode rejection.
- The previous comparator decision should not affect the following, no memory effect.

Figure 8.3 shows three topologies for comparators. The straight-forward limiting amplifier (top) consists of a cascade of amplification stages to obtain as much gain as possible. For a given current consumption the unity gain bandwidth per stage determines the overall speed of this chain of amplifiers (compare Sect. 2.7.2).

If a single amplifier stage has a unity gain bandwidth ω_{UGBW} and an amplification A, then the dominant pole is at $\tau = A/\omega_{\mathrm{UGBW}}$. The response of a cascade of M comparators is

$$H(\omega) = \left(\frac{A}{1+s\tau}\right)^M = \left(\frac{\omega_{\mathrm{UGBW}}}{s+\omega_{\mathrm{UGBW}}}\right)^M .$$

An excitation with a step function results in

$$V_{\mathrm{out}}(t) = A^M V_{\mathrm{in}}(t=0)\left[1 - \mathrm{e}^{-t/\tau}\sum_{i=1}^{M}\frac{(t/\tau)^{i-1}}{(i-1)!}\right]. \tag{8.1}$$

For $t < \tau$ the cascade of comparators behaves as a cascade of integrators; therefore the response is proportional to $(t/\tau)^M$.

A second problem concerning the speed of this comparator is the recovery from the previous decision. Unless limiter circuits like diodes are used, the last stages of the amplifier will go into saturation. This will cause the inversion charge of MOS devices to be lost. The time required to resupply this charge leads to a delay during the next comparison.

Yet, the straightforward limiting amplifier is popular as it requires no activation by a clock pulse. Often a string of inverters is used or some simple differential stages.

The second topology of Fig. 8.3 uses a small amplifier as a positive feedback element. As long as this amplifier is much weaker than the feed-forward path it will only marginally contribute to the amplification. What it can do is add a threshold in the decision process. This so-called hysteresis is discussed in Sect. 8.1.2.

In the last topology the feedback path of the amplifier is of comparable strength to the forward path. The idea of this regenerative stage or latch is that the already build up difference in the forward stages feeds the positive feedback in order to reach a fast decision. This mode of amplification must be reset by a clock phase that clears the data after the decision.

The analysis of two positively fed back amplifiers or a latch is done in the Laplace domain. The nodes are labeled $v_A(t)$ and $v_B(t)$ or in the Laplace domain: $V_A(s)$ and $V_B(s)$. It will be assumed that there is an initial condition $v_B(t=0) \neq 0$:

$$V_A(s) = \frac{A}{1+s\tau}\left(V_B(s) - \frac{v_B(t=0)}{s}\right) = \left(\frac{A}{1+s\tau}\right)^2 V_A(s) - \frac{A}{1+s\tau}\frac{v_B(t=0)}{s},$$

where τ and A have the same meaning as above, but A is negative:

$$\begin{aligned} V_A(s) &= v_B(t=0)\frac{-A(1+s\tau)}{s((1+s\tau)^2 - A^2)} \\ &= v_B(t=0)\left(\frac{-A/(1-A^2)}{s} + \frac{A\tau/(2(1+A))}{1+s\tau+A} + \frac{A\tau/(2(1-A))}{1+s\tau-A}\right). \end{aligned}$$

The inverse Laplace transform gives

$$v_A(t) = v_B(t=0)\left(\frac{-A}{(1-A^2)} + \frac{A}{2(1+A)}\mathrm{e}^{-(A+1)t/\tau} + \frac{A}{2(1-A)}\mathrm{e}^{(A-1)t/\tau}\right). \quad (8.2)$$

After a few time constants have elapsed only the middle term in brackets is relevant:

$$v_A(t) \approx \frac{-v_B(t=0)}{2}\mathrm{e}^{-(A+1)t/\tau} \approx \frac{-v_B(t=0)}{2}\mathrm{e}^{\omega_{\mathrm{UGBW}}t}. \quad (8.3)$$

The nodes of the latch show an exponential increase determined by the start value and the unity-gain bandwidth. In order to reach a gain comparable to a cascade of M amplifiers with a gain A a time of $M\ln(A)/\omega_{\mathrm{UGBW}}$ is needed. Ultimately the node voltage will be limited by the circuit and its power supplies. The exponential signal growth makes a latch a fast decision element in a regenerative comparator.

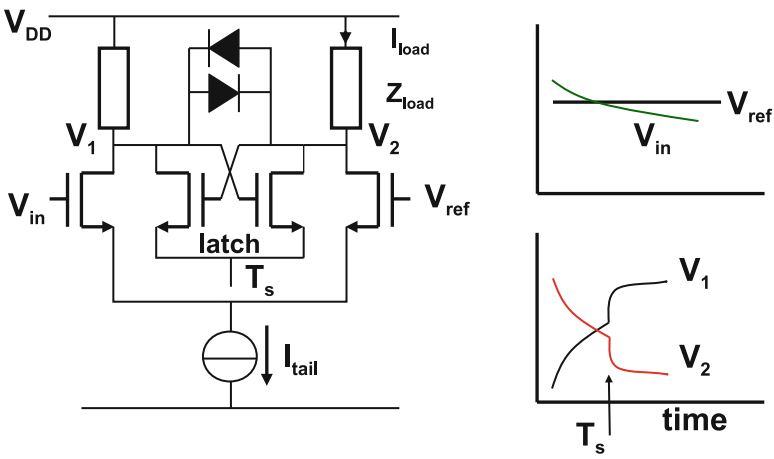


Fig. 8.4 A simple regenerative comparator circuit

8.1.1 Dynamic Behavior of the Comparator

Most comparators use an input differential pair. Here the difference is formed between the input value and the reference value. The differential pair allows to create some tolerance for the common-mode level of the input signal. The differential current is applied to a positive feedback latch. A clock pulse will activate the latch and amplify the small input voltage difference to a large signal. A simple example is shown in Fig. 8.4.

The gain of the comparator is determined by the transconductance of the input differential pair and the load: $g_{m,\text{in}} \times Z_{\text{load}}$. This gain must be sufficient to suppress any secondary effects in the circuit. On the other hand there is no reason to boost the DC gain to very high values. Too much gain will cause saturation, slewing, and unnecessary kickback. The achievable speed performance is limited by the unity-gain bandwidth; see the previous section.

The bandwidth of the comparator must be analyzed both in small-signal mode as well as in large-signal mode. In small-signal mode the input transconductance and the capacitive load of the nodes V_1 and V_2 determine the bandwidth:

$$\omega = \frac{g_{m,\text{input}}}{C_{\text{load}}}. \tag{8.4}$$

A large input transconductance is beneficial for a large small-signal bandwidth. Choosing a wide input transistor also helps in reducing the input-referred mismatch but creates a larger capacitive load. Also the parasitic coupling between the drain voltages and the input terminals will become stronger enhancing kickback.

In order to achieve the overall performance also the large-signal bandwidth of the circuit must be considered. Two main issues are crucial for the large-signal bandwidth:

- The fastest change of the signal that is amplified without distortion is limited by the slew-rate:

$$\begin{aligned} \text{slew-rate} = \frac{\mathrm{d}V}{\mathrm{d}t} &= \frac{I_{\text{tail}}}{C_{\text{load}}} \\ C_{\text{load}} \frac{\mathrm{d}V_1(t)}{\mathrm{d}t} &\leq I_{\text{tail}} \\ 2\pi f_{\text{in}} V_{1,\text{max}} C_{\text{load}} &\leq I_{\text{tail}}, \end{aligned} \tag{8.5}$$

  where $V_{1,\text{max}}$ is the amplitude of an equivalent sine wave. If the charging current during the transient of the signal exceeds the tail current, the charging of the capacitors in the circuit will be limited and distortion can follow.
- A large-signal effect in this comparator is saturation.[2] The large signals that drive a comparator will force the input transistors and the internal components in a saturated "on" or "off" regime. Saturation of the input transistors creates significant currents in the gate connection; see Sect. 8.1.5. In order to revitalize the comparator all saturated components will have to be brought back into their linear operation regimes. This process requires current and the signal processing will experience a delay time. This will result in signal distortion. To prevent saturation effects, the comparator of Fig. 8.4 uses two diodes to limit the signal swing on the internal nodes from saturation. Various other circuit techniques can be used to reduce the internal voltage swings (nonlinear loads, cascode stages, etc).

8.1.2 Hysteresis

A comparator is designed to discriminate between positive and negative levels at its input terminal, irrespective how small these levels are and what the previous decision was. In many comparator designs this ideal situation is not achieved. Either intentionally or as an unwanted consequence of the topology, the comparator remembers its previous state. Figure 8.5 shows an elementary comparator consisting of two inverters. The output of the second inverter is partly fed back in positive phase to the input. The comparator input has now a preference to keep its present state and a small input value around the trip level of the inverter will not cause the output to change. Depending on the resistor ratio, the input will see a trip level that

[2]The term saturation is used to indicate that the circuit is far out of its operating point. Saturation of circuits has no relation with the operating regime of a transistor.

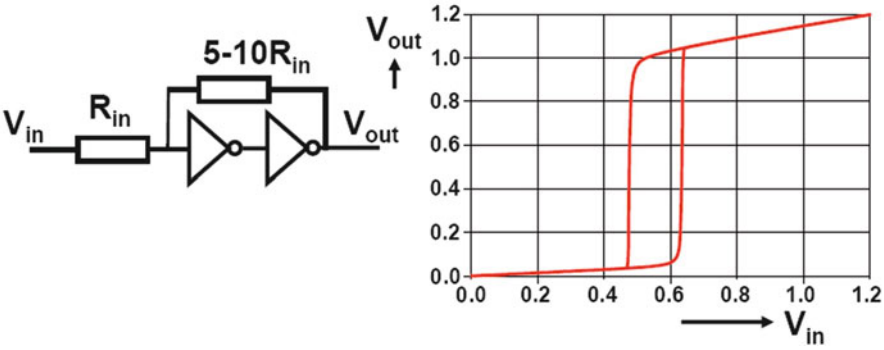


Fig. 8.5 Hysteresis created by positive feedback in a two-stage buffer

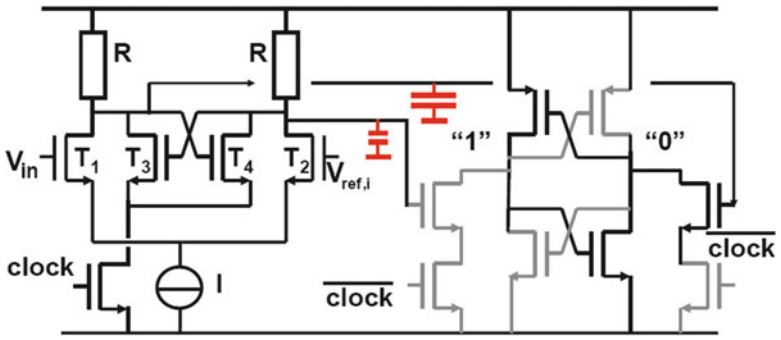


Fig. 8.6 Hysteresis created by the signal-dependent loading of the input latch by the second latch. The *gray*-colored transistors are not conductive and form only a small load capacitor

depends on the present state of the output. Going from negative input to positive or vice versa results in different switching characteristics; see Fig. 8.5(right). This effect is in analogy with magnetic materials called "hysteresis." In this example the hysteresis creates an additional threshold for change. The example circuit in Fig. 8.5 belongs to the class of "Schmitt-trigger" circuits. These comparators are designed to allow a single decision in case of noise signals. In other words a Schmitt-trigger circuit decides only if a clear input signal is present and the hysteresis avoids that noise generates false outputs.

A practical example of unwanted hysteresis is a pre-latch stage that is connected to a second stage consisting of a latch activated by the inverse clock. In Fig. 8.6 the signal is fed from the amplifier to the latch via two transistors that are activated via two clocked transistors. The left-hand transistors will be out of inversion when that side of the latch stores a "1" signal. The right-hand transistor sees a "0" signal and is in inversion. Thereby the two coupling transistors create an unequal capacitive loading of the first stage. This loading favors a similar signal in the first latch when the latch sees only a small input signal. The consequence is a comparator with hysteresis.

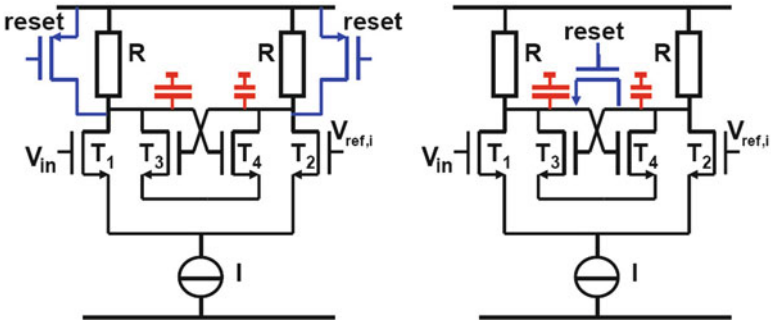


Fig. 8.7 Two methods to clear the state in comparator circuit

In other configurations the opposite effect may be the case: the hysteresis favors change and the comparator toggles at every clock cycle for an input signal close to the trip level.

The previous state can be removed by resetting the latch in the comparator. Some designs simply disconnect the latch from the supply. This method assumes that there is sufficient time to discharge the latch nodes. A more active approach consists of adding a specific clear or reset mechanism to the latch. Figure 8.7 shows two configurations. The left-hand circuit connects the latch nodes to the power supply and actively removes all state information. The low-ohmic switches change the DC levels in the amplification branch. The DC level must be restored, and during that process any inequality in capacitive loading will show up as inaccuracy.

The construction on the right-hand side circumvents the restoration problem by pinching the two latch nodes together. This will keep the DC level of the nodes intact and sets the latch to its trip point. A proper choice of the impedance of the switch allows to use it as a differential load for the current of the input pair. The reset transistor must be bootstrapped in case of low power supply.

8.1.3 Accuracy

The required accuracy of a comparator depends on the required specification and the architecture of the analog-to-digital converter. In dual-slope, successive approximation and pipeline designs, the static random offset is a second-order effect and generates a (random) DC shift of the entire signal. In a full-flash converter the input-referred random offset is crucial because it will shift the individual reference levels and it impacts both integral and differential nonlinearities. Also in multiplexed analog converters the random offset returns as a spurious tone. The input-referred random offset σ_{Vin} must be designed to a value a factor 5–10 lower than the size of the LSB at the comparator as an initial target. Fine-tuning of this requirement depends on, e.g., the tolerance for conversion errors on system level.

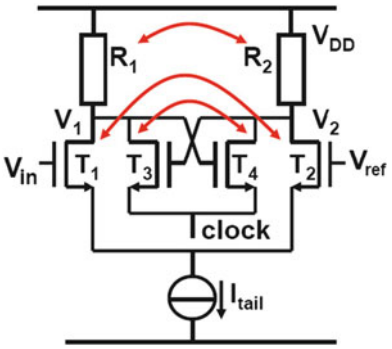


Fig. 8.8 Mismatch sources in a comparator

Accuracy has static and dynamic components. Just as in every analog circuit the static accuracy is (in a carefully laid-out circuit) determined by the random mismatch of a transistor pair; see Sect. 11.4. Of course the input differential pair is not the only contributor, also the mismatch of the load and the latch must be taken into account.

In the schematic diagram of Fig. 8.8 current differences caused by the input pair, the load and the latch all come together on the drains of the transistors. All contributions can be referred back to an equivalent input-referred random mismatch σ_{Vin}. With the help of Eq. 2.18, the input-referred random offset is described as

$$\sigma^2_{\mathrm{Vin}} = \left(\frac{\partial V_{\mathrm{in}}}{\partial V_{\mathrm{T},12}}\right)^2 \sigma^2_{V_{\mathrm{T},12}} + \left(\frac{\partial V_{\mathrm{in}}}{\partial V_{\mathrm{T},34}}\right)^2 \sigma^2_{V_{\mathrm{T},34}} + \left(\frac{\partial V_{\mathrm{in}}}{\partial R_{1,2}}\right)^2 \sigma^2_R$$

$$\sigma^2_{\mathrm{Vin}} = \sigma^2_{V_{\mathrm{T},12}} + \frac{g^2_{m,34}}{g^2_{m,12}} \sigma^2_{V_{\mathrm{T},34}} + \frac{I^2_{\mathrm{load}}}{g^2_{m,12}} \frac{\sigma^2_R}{R^2_{1,2}}. \tag{8.6}$$

The equation assumes that the random mismatch can be calculated in a linearized model of the circuit. Unfortunately in this equation the transconductance of the latch does not behave in a linear fashion. In one extreme there is no current running in the latch and its contribution to the input-referred random offset is zero. Directly after the clock is activated and a current flows in the latch transistors, a step function on the nodes V_1 and V_2 will occur. If the gates are not equal or in the presence of mismatches due to differences in capacitive loading, different charges are drawn from the local nodes and will create random differences in these voltage steps.

If, on the other hand, the latch is constantly fed with a small tail current that is not sufficient to activate the latch, the dynamic errors can largely settle before the clock is activated. However, the nonzero transconductance will contribute an additional component to the input-referred random offset.

Thermal noise and $1/f$ noise create additional accuracy limitations. Because these contributions are time varying, also offset compensated analog-to-digital converter architectures suffer from this limitation. The contributions to the noise of the individual components are referred back to an equivalent input noise source

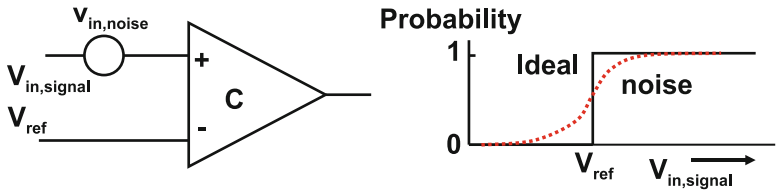


Fig. 8.9 Thermal noise will create a probabilistic behavior of the comparator decision (*dotted line*)

in a similar manner as for mismatch. If the input transconductance dominates the noise, the effective value of the input-referred noise is

$$v_{\text{in,noise}} = \sqrt{4kT\frac{\text{BW}}{g_m}} \tag{8.7}$$

and with a bandwidth of 10 GHz and an input transconductance of 1 mA/V the value for the input-referred rms noise is $v_{\text{in,noise}} = 400\,\mu\text{V}$. The thermal noise amplitude distribution creates a cumulative Gaussian probability distribution around the trip level (Fig. 8.9). In order not to exceed the accuracy specifications the bandwidth has to be reduced or more power has to be spent on improving the impedance levels.

8.1.4 Metastability and Bit Error Rate

In the comparator a fundamental problem arises in the form of metastability. Metastability is associated with any form of comparison and is also well known in, e.g., synchronization circuits. The crucial observation is that the time a comparator or latch needs to form a digital signal depends on the initial overdrive voltage. In other words, the input differential voltage determines the delay of the comparator.[3]

For very small overdrive voltages, there is a fraction α of the LSB size where the comparator has insufficient voltage difference on its nodes to reach a decision in the limited time T_s of a clock pulse. Now the comparator will not generate a clear "zero" or "one" output level. Without unambiguous signals the succeeding logical circuitry can generate large errors, e.g., if this digital signal is crucial for determining the MSB.

For small signals the latch can be viewed as two single-pole amplifiers in a positive (regenerative) feedback mode. The voltages on the nodes of the latch develop exponentially in time with a time constant τ; see Eq. 8.3. This time constant

[3]This voltage-delay relation can be exploited: measuring the delay is used to quantify the input voltage and create more resolution.

is determined by the internal node capacitance and the transconductance of the latch transistors. Now α can be approximated by

$$\alpha \approx \frac{V_{\text{latch}}}{V_{\text{LSB}}} \mathrm{e}^{-T_s/\tau} \quad \Rightarrow \quad \text{BER} \approx 2^N \mathrm{e}^{-T_s/\tau}, \tag{8.8}$$

where the ratio between the maximum latch swing V_{latch} and V_{LSB} is estimated as 2^N. The bit error rate is an important parameter in the design of fast converters with a high accuracy. In CMOS the time constant τ is formed by the parasitic and gate capacitances and the achievable transconductance.

A typical example with 8 bits assumes 5 fF total capacitance for 1 µm gate width, with 5 µA/V transconductance for the same gate width. A time period of $T_s = 20$ ns results in a BER of 10^{-7}. This BER can be improved to better than 10^{-8} by means of more current in the latch transistors. For converters with sample rates in excess of 100 Ms/s a BER of the order 10^{-8} means one error per second. Especially in industrial and medical equipment such an error rate can be unacceptable. A method to get an impression of the bit error rate is to apply a slow sine wave to the device with an amplitude that guarantees that no more than one LSB change occurs at the digital output. Now the bit error rate can be estimated by recording output codes that differ more than 1 bit from the preceding code.

From a fundamental point of view the BER cannot be avoided completely; however, decreasing the time constant (by lower capacitance and higher transconductance), a BER of 10^{-13} is possible. Measures to improve the BER include improving the latch speed with more current and smaller capacitances, additional gain stages or even a second latch, and a special decoding scheme avoiding large code errors due to a metastable state.

Example 8.1. Calculate the bit error rate of a latch in 0.18 µm CMOS with 0.5/0.18 µm NMOS transistors and 100 µA total current. The latch is used in a 0.5 Gs/s application.

Solution. The transconductance of the transistors is $g_m = \sqrt{2I(W/L)\beta_\square} = 0.3$ mA/V. The gate capacitance is $0.5 \times 0.18 \times 8.3$ fF = 0.75 fF. The succeeding stage will load latch with double or triple this amount. Some wiring and diffusion capacitance will result in a total load of around 10 fF, leading to a time constant of 35 ps. The decision period is a 40% fraction of the 2 ns sample rate. So the bit error rate is estimated at $\approx 2^N \mathrm{e}^{-T_s/\tau} = 2^N \times 1.2 \times 10^{-10}$. For a 7-bit resolution converter this would lead to BER = 1.5×10^{-8}.

8.1.5 Kickback

The comparator is a nonlinear element: the only relation between the input signal and the output is the sign. The decision process in the comparator is often implemented with transistors that pass through all operation modes of the devices.

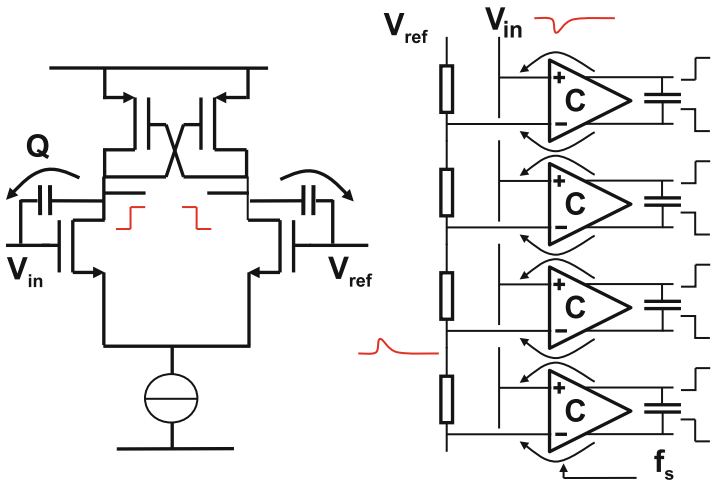


Fig. 8.10 Kick-back in a comparator circuit

The charges controlling the devices will show considerable variation. These charges have to be provided and will be dumped preferably in the power supply lines; however, also an exchange to the input and reference signals will occur.

Figure 8.10(left) shows a differential input pair. The input voltage difference will lead in the succeeding circuits to a decision marked by sharp voltage transitions. Despite that the input differential pair remains in normal operating mode, the drain-gate capacitors of these MOS devices will pass these fast edges to the input and reference nodes thereby generating "kickback." In some comparator designs these transitions can be as large as the power supply voltage. Figure 8.10(right) shows a full-flash circuit. In this architecture the kickback effect is strong as the contributions of many comparators add up. During the simulation of the comparator ideal voltage sources instantly drain the charges from saturation effects and therefore will result in an optimistic performance prediction. Realistic impedances at the input terminals of the comparator allow a better simulation prediction of the performance in the presence of kickback.

Reducing the kickback signal requires to decrease the coupling capacitances by reducing the dimensions of the input-related circuit elements. Inside the comparator the swing of the signals must be sufficient to drive the next stages but can be kept as low as a few tenths of a volt by swing limiting measures. The additional advantage is that the transistors in the comparator remain in inversion, thereby avoiding time loss due to recharging. A rigorous method applies an additional preamplifier. Unfortunately these measures compromise the performance. Small input transistors cause high random offset. Lowering the swing of the transitions requires some form of separation between the full-swing digital output and the input. Separation stages, however, will create additional delay.

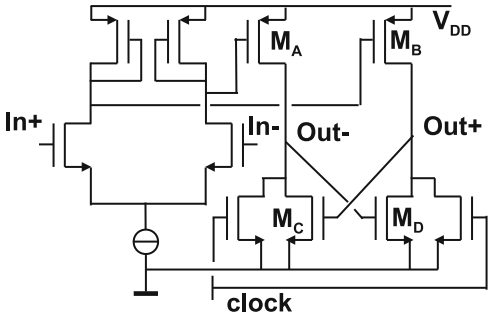


Fig. 8.11 A comparator in CMOS based on an NMOS enhancement/depletion design [166]

8.1.6 Comparator Schematics

Many comparator designs have been published in literature and there is obviously not a standard circuit topology. This is on one hand caused by the evolution of the technology. The drive capabilities of the transistors have improved, but the power supply voltage and the input signals have reduced. On the analog-to-digital converter architecture side also a lot of developments have taken place over the last 25 years. The rise in popularity of the pipeline converter has allowed to spend more area and power on a comparator than a flash converter can tolerate. The following examples of comparator circuits are a subset of the published work and are meant to educate and perhaps inspire a new design.

The comparator published in [166] was designed in a 7 µm NMOS metal-gate technology. Figure 8.11 shows a CMOS variant of that design. A similar topology is found in [149, Fig. 13]. The input stage serves to amplify the differential signal and allows some common-mode rejection. The second stage is fed with the amplified signal to generate a digital decision. The intermediate amplification nodes separate the preamplifier from the latch. The problem with an intermediate node is that it creates an additional pole and slows down the design. In the design of Fig. 8.11 the poles are formed by the PMOS mirrors. These mirrors cannot easily be operated at a large gate-source voltage as the input range is reduced. This mirror also contributes to the input random offset. The strict separation of latch and input allows a small kickback effect.

The original design (1981) resulted in a random offset at the input of 6.1 mV, 5-bit resolution, 4 MHz signal bandwidth at 20 Ms/s.

The comparator in Fig. 8.12 also consists of a preamplifier (left) and a latch [167]. The preamplifier does not use a differential pair with tail current, but the inputs are capacitively coupled into the comparator. In the cross-coupled loop formed by the source followers and the capacitors, capacitive voltage shifting is used. The residual offset is 2 mV and in a 2 µm process 40 Ms/s was reported.

The comparator in Fig. 8.13 is designed for a folding analog-to-digital converter [168]. It consists of an input stage that feeds its differential current in a cascode stage. This construction avoids an intermediate pole that would slow down the

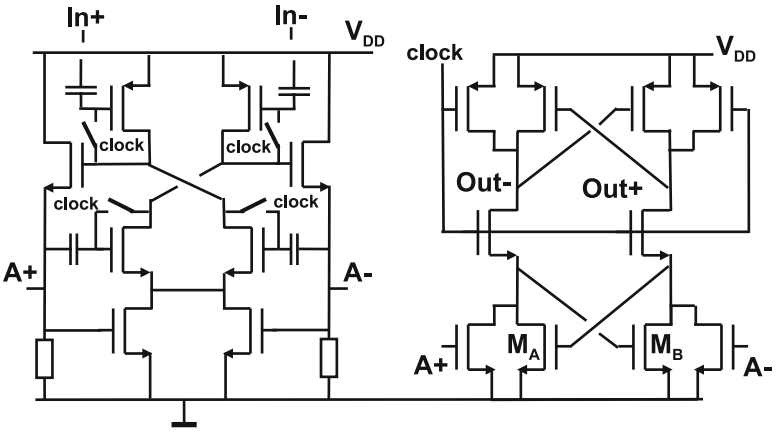


Fig. 8.12 A comparator based on the work in [167]

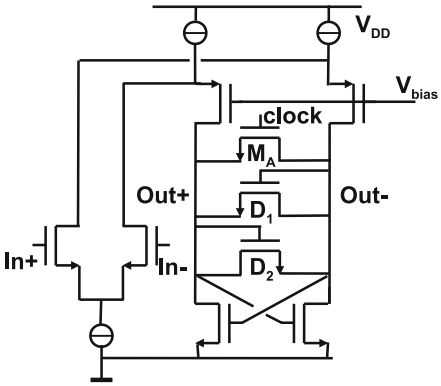


Fig. 8.13 A comparator designed for a folding analog-to-digital converter [168]

circuit. On the other hand a reasonable shielding for kickback is obtained. The latch is equipped with two diode-connected transistors to have a current path available even if the latch is activated. Saturation of the input stage is thereby prevented. In a 0.8 µm CMOS process the 1-sigma input-referred random offset is 2.5 mV. The circuit runs up to 70 Ms/s sample rate in this process. Its speed will certainly benefit from advanced processes.

Figure 8.14 uses three phases to reach a decision [169]. When $\overline{clock}$ is high the comparator is in reset mode. The signal is amplified over the resistance of the reset transistor. After $\overline{clock}$ goes low, during a short period, the lower latch can amplify the signal. This amplification allows to suppress the mismatch of the upper latch section. After *clock* goes high, this amplified signal is boosted to digital levels. Some sensitivity to the nonoverlapping clock phases is present, as well as a considerable kickback.

The comparator in Fig. 8.15 is based on former bipolar designs [170]. The comparator routes a constant current through either the amplification side (clock is

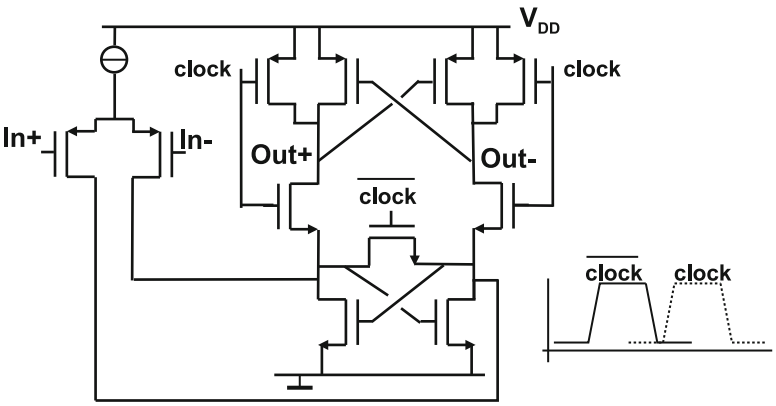


Fig. 8.14 A comparator for high speed operation [169]

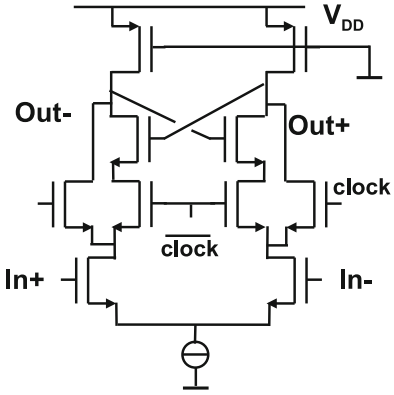


Fig. 8.15 A comparator designed for a folding analog-to-digital converter [170]

high) or through the latch. The speed is limited by the latch pair and its load. A lot of imperfections add up in the current path; therefore some more input-referred mismatch is expected. Also the kickback noise can be significant. This effect will depend on how well the drains of the input pair are kept stable. The accuracy of the crossing of the clock and the inverse clock is crucial. The design was used in a 0.5 µm CMOS process with a clock speed of 80 Ms/s.

A comparator for a 4-bit 12 Gs/s analog-to-digital converter uses a two-stage comparator (Fig. 8.16). The middle PMOS in the preamplifier serves as a load for the input pair. The sources of the input pair are switched to the positive power supply at the end of the amplification, which produces kickback noise via the coupling of the gate. The latch (right) is also used in the "StrongArm" design [172] and is not intended to resolve small voltage differences as it serves as an edge-triggered latch. If the clock is low the cross-coupled pair is reset and no current flows. A high-ohmic resistor (dotted) prevents leakage currents to charge nodes asymmetrically. At rising clock the input signal is amplified and regenerated in the latch to a full digital signal.

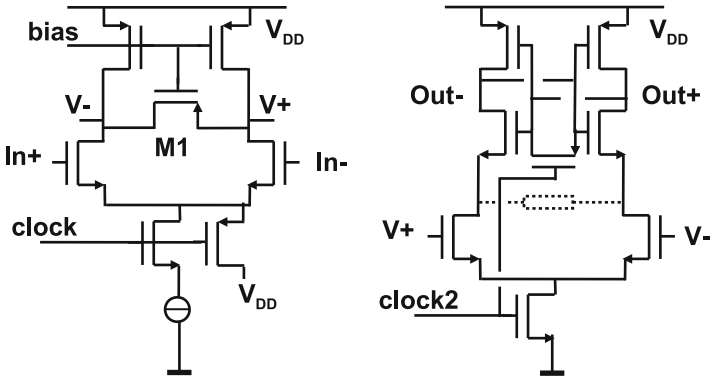


Fig. 8.16 A comparator for high-speed operation [171]. The latch (*right*) is based on a design for the "StrongArm" processor [172]

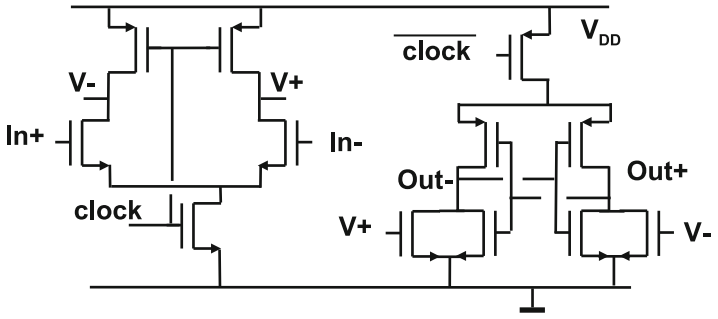


Fig. 8.17 A double-tail comparator combines accuracy with speed [174]

After full settling the latch is consuming no current. The 1-sigma input-referred random offset in [171] was in 0.25 µm CMOS 60 mV and the bandwidth exceeded 2.5 GHz at 12 Gs/s. Another example of an implementation of this comparator is in a flash converter [173] where a good energy efficiency is achieved.

The comparator in Fig. 8.17 [174] is a further development of Fig. 8.16. The amplification is now carried out in a pre-stage, thereby reducing the amount of stacked transistors and the kickback noise. The design does not require any DC current, which makes it very suited for achieving low-power operation.

A more advanced comparator is shown in Fig. 8.18. The design is differential, thereby eliminating the PSRR problems. The random input offset of the comparator is estimated at 36 mV 1-sigma [99]. Still some time is needed for the bias setting in this 0.18 µm CMOS design. Interleaving of two input stages reduces in this converter this speed penalty.

Example 8.2. A differential NMOST input pair $(W/L = 50/2)$ is loaded with a PMOST current mirror $(W/L = 36/1\,\mu\text{m})$ in a process with $A_{V_{T},N} =$

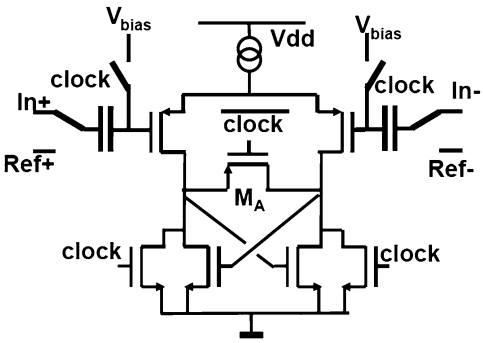


Fig. 8.18 A comparator design for an interleaved pipeline converter [99]

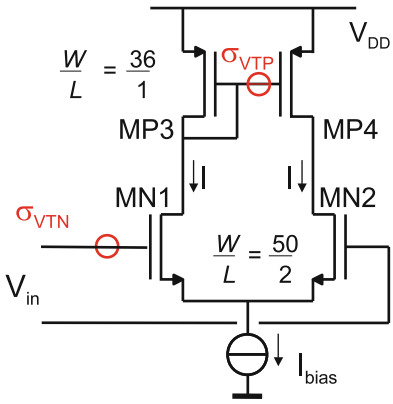


Fig. 8.19 The circuit schematic

$A_{V_{T,P}}$=6 mV µm, and the ratio between the beta square (for $W/L = 1$) is $N/P = 3$. Calculate the input-referred mismatch.

Solution. In Fig. 8.19 the schematic of this circuit is drawn. With the help of Eq. 2.110 the standard deviations for the NMOS and PMOS threshold voltages are found: $\sigma_{V_{TN}} = 6/\sqrt{50 \times 2} = 0.6\,\text{mV}$, and $\sigma_{V_{TP}} = 1\,\text{mV}$. The PMOS transistor mismatch must be referred back to the input. This threshold mismatch translates into a PMOS current mismatch via $g_{m,P}\sigma_{V_{TP}}$. The effect at the input terminals is the input-referred mismatch voltage. This voltage must generate in the NMOS transistors a current that compensates the mismatch current generated by the PMOS devices: $g_{m,N}\sigma_{V_{\text{in}}P} = g_{m,P}\sigma_{V_{TP}}$. So the total input-referred mismatch is composed of the NMOS and PMOS contributions:

$$\sigma_{\text{Vintot}} = \sqrt{\frac{g_{m,P}^2}{g_{m,N}^2}\sigma_{V_{TP}}^2 + \sigma_{V_{TN}}^2} = 0.92\,\text{mV}.$$

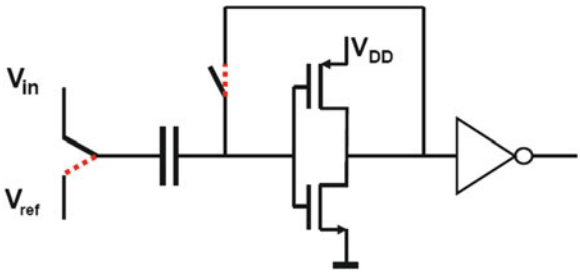


Fig. 8.20 An auto-zero comparator as used in [175]

8.1.7 Auto-Zero Comparators

Input-referred random offset is one of the key problems to battle in comparator design. Early on attempts have been made to "auto-zero" [175] or cancel [176] this offset. The basic schematic of Fig. 8.20 is similar to the track-and-hold circuit in Fig. 4.20. During the auto-zero mode the switches are in the dashed positions and the inverter is essentially in unity gain mode. The capacitor is charged on its left-hand side to V_{ref} and on the right-hand side to the input offset. When the switches toggle the change on the input of the comparator equals $V_{\text{in}} - V_{\text{ref}}$. This voltage is amplified with the small-signal gain of the inverter and its successors. Some residual offset is due to limited gain and charge variation in the switches. This scheme was used in a 1.4 µm CMOS process [175] and allowed an analog-to-digital converter running at 40 Ms/s with 10 MHz bandwidth. It is clear that the charging and discharging of the input capacitor puts extreme demands on the input and the reference impedances. The implementation as depicted in Fig. 8.20 has the additional disadvantage that the power supply rejection ratio (PSRR) is low. A large part of the power supply variation is translated in a signal contribution on the input. In the case of an inverter the PSRR is around 0.5. So the power supply has to be kept clean to the level of a few V_{LSB}. Also the timing of the offset cancellation is a point of consideration. Offset compensation per clock cycle costs 30–50% of the available sample period and reduces the maximum speed. Offset compensation at a fraction of the sample rate is possible but can introduce spurious components at those lower frequencies.

The auto-zero cancellation, as shown in Fig. 8.20, acts as a transfer function for all (unwanted) signals $e(z)$ that originate at the input of the inverter. The error component in the output signal is found in a similar manner to the analysis in Sect. 4.4. The error component in the output signal is

$$V_{\text{out, error}} = e(z)(1 - z^{-0.5}). \tag{8.9}$$

The exponent -0.5 assumes a 50% duty cycle of the switching signal. This transfer is characterized by a term $2\sin(\pi f/2f_s)$. Low-frequency components are suppressed, but higher frequencies can even experience some amplification. Moreover the switching sequence acts as a sampling mechanism for unwanted high-frequency signals, thereby shifting these high frequencies into the signal band.

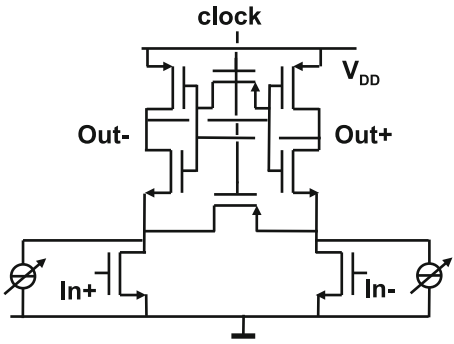


Fig. 8.21 The current sources are controlled to auto-zero this comparator [177]

The auto-zero capacitor acts as a sampling capacitor for which the kT/C noise analysis applies. Running this offset compensation scheme at low frequencies results in stacking of noise and down-sampling of spurious signals (e.g., from the substrate). See also the current-calibration technique in Sect. 7.7. Another class of auto-zero mechanisms uses adjustable voltages or currents to reduce the input-referred offset. Figure 8.21 shows the basic idea implemented with two controlled current sources [177]. The necessary corrections are carried out by means of an algorithm, either at start-up or during operation. If the chip contains non-volatile memory also programming after production is possible.

8.1.8 Track-and-Hold Plus Comparator

Random-offset reduction is necessary to achieve 8-bit DNL performance. In most offset reduction schemes the offset + signal and the offset are determined at different points in time, so at least one must be stored in a capacitor. Fukushima et al. [175] and Kusumoto et al. [178] describe a well-accepted method to perform offset reduction with the aid of a capacitor at the input of the comparators which switches between input and reference; see Fig. 8.20. The disadvantage of this method is that the high capacitive input load requires a low-ohmic ladder (300 Ω) and poses high demands on the circuitry for driving the analog-to-digital converter. The single-sided input capacitor has a large parasitic capacitance to a bouncing substrate in a mixed signal chip. The inherent capacitive input voltage division attenuates the signal. The basic inverter-type comparator has a poor power supply rejection [179], which affects the performance if power supply bouncing occurs between coarse and fine cycles. These comparator design points have to be solved for embedded operation.

Figure 8.22 shows the comparator that was used in several analog-to-digital converter designs (see Sects. 8.9.1–8.9.3).

With the exception of input and ladder terminals, the design is fully balanced and the PMOS current sources allow a good PSRR. The design consists of an input stage

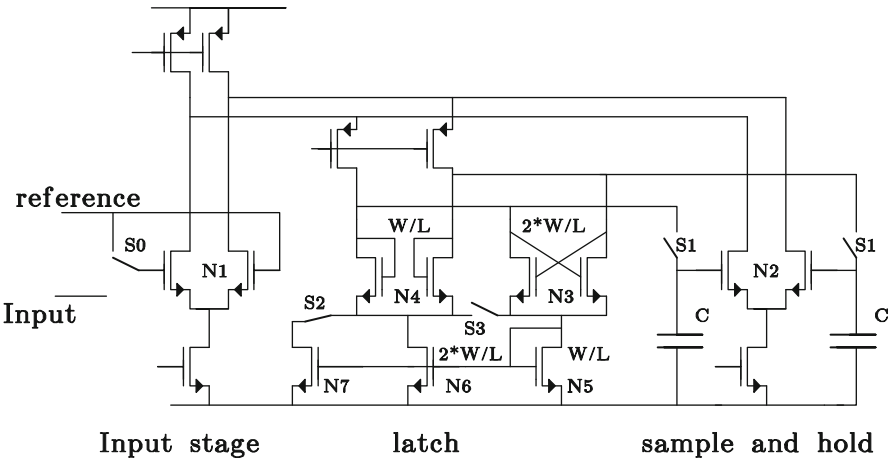


Fig. 8.22 The basic comparator schematic. Switches are shown in the position for the amplification phase (Design: J.v.Rens)

N1, from which the signal is fed into a sample-and-hold stage N2,S1,C. Comparison involves three cycles: sampling, amplification, and latching. During the sampling phase switch S1 is conducting and $V_{\text{in}} - V_{\text{ref}} + V_{\text{off}}$ is stored on both capacitors. These capacitors are grounded on one side and do not suffer from parasitic coupling to substrate. V_{off} represents the sum of all the offsets in the comparator. During the sampling phase the negative conductance of latch stage N3 is balanced by the positive conductance of the load stage N4. Their combination acts as an almost infinite impedance, which is necessary for good signal + offset storage. The latch stage has twice the W/L of the load stage, but its current is only half due to the current mirror ratio N5, N6. For large differential signals the effect of the factor 2 in W/L of N3 and N4 becomes important: the conductance of N3 reduces at a much higher rate that of N4, so the effective impedance of N3–N4 collapses. The large-signal response is consequently improved by the reduced time constant. The feedback of N2 via the switches S1 allows a 150 MHz bandwidth, resulting in a high-quality S/H action.

After the sampling phase, the switch S0 at the input connects to the reference voltage, effectively disconnecting the common input terminal from the comparator. As switches S1 are disconnected, the sample-and-hold stage will generate a current proportional to $V_{\text{in}} - V_{\text{ref}} + V_{\text{off}}$, while the input stage and the rest of the comparator generate only the part proportional to V_{off}. The (differential) excess current is almost free of offsets and will be forced into the load-latch stage N3–N4. Switch S2 is made conductive, which increases the conductance of N4 and decreases the conductance of N3; the gain of N2 on N3–N4 is now about eight for small differential signals.

Finally, S3 is made conductive; the current now flows in a 2:1 ratio into N3–N4, thereby activating the latch operation. The latch decision is passed on to the decoding stage and a new sample can be acquired. Remaining random offsets

(approx. 0.4 mV) are caused by limited gain during the sampling phase, charge dump of S1, and the difference in matching contributions of N3 and N4 in the sampling and amplification phases.

8.2 Full-Flash Converters

Full-flash[4] converters are used for two main purposes. As a stand-alone device, this converter can achieve the highest conversion speeds for low (6-bit) resolutions [180]. Another important field is the application in lots of other analog-to-digital conversion architectures, such as subrange converters. A full-flash converter is comprised of a resistor ladder structure whose nodes are connected to a set of $2^N - 1$ comparators; see Fig. 8.23. A decoder combines the comparator decisions to a digital output word.

The input signal is compared to all reference levels simultaneously. After the sampling clock becomes active, a part of the comparator circuits with an input signal lower than the local ladder voltages will generate a logical "zero," while the other comparators will show a logical "one." The digital code on the outputs of the comparators is called a "thermometer code." A digital decoder circuit converts the thermometer code in an N-bits output format (mostly in straight binary format).

The input signal for a full-flash converter is only needed at the moment the latches are activated. The sample-and-hold function is inherently present in the digital latches of the comparators. For most applications an external sample-and-hold circuit is not needed. Full-flash converters are the fastest analog-to-digital converters; however, their complexity and their power consumption grow with the number of comparator levels 2^N. Also the area and the input capacitance grow exponentially with N.

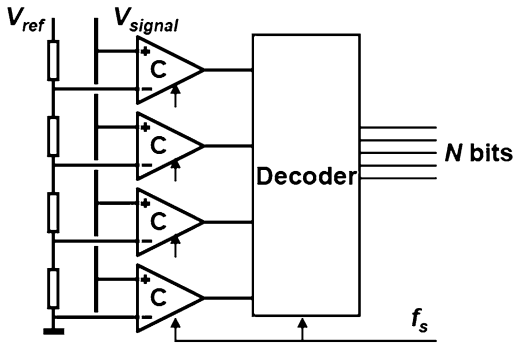


Fig. 8.23 A "full-flash" analog-digital converter

[4]The origin of the addition "full" in full flash can refer to the conversion of the full range. "Partial-flash" converters can refer to a subranging architecture.

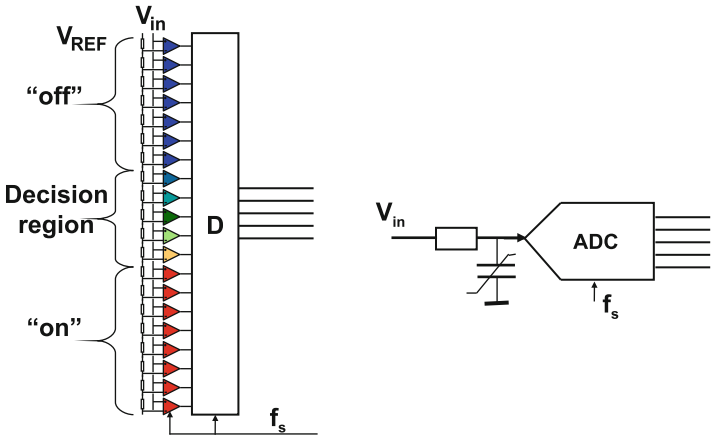


Fig. 8.24 A "full-flash" converter presents a non-linear input impedance

The capacitance at the input of a full-flash converter is largely determined by the input capacitance of the comparator. If that input capacitance is formed by, e.g., a differential pair, the effective input capacitance of the comparator will depend on the input signal. Low-level single-ended input signals with respect to the local reference voltages of the comparators will result in a current starved input branch of the differential pair and a high signal will keep the input transistor in inversion. An input signal lower than the local reference voltage will see a low input capacitance as the MOS input transistor is out of inversion. A high input signal creates an inversion charge, a considerable input gate-source capacitance, and a high input capacitance. The group of comparators below the decision level with a high input capacitance and the group above the decision level with a low capacitance, Fig. 8.24, make the input impedance of a full-flash converter signal dependent. Second-order distortion will arise if the converter is fed from a source with source impedance. If the input capacitance for single-sided operation is defined as

$$C(V_C(t)) = C_0 + \Delta C \frac{V_C(t)}{V_{\text{ref}}} \tag{8.10}$$

with V_C as the voltage over the nonlinear capacitor, the capacitive current is found using Eq. 2.56:

$$I_C = C(V_C(t)) \frac{\mathrm{d}V_C(t)}{\mathrm{d}t} + V_C(t) \frac{\mathrm{d}C(V_C(t))}{\mathrm{d}t} = C_0 \frac{\mathrm{d}V_C(t)}{\mathrm{d}t} + \frac{2V_C(t)\Delta C}{V_{\text{ref}}} \frac{\mathrm{d}V_C(t)}{\mathrm{d}t}. \tag{8.11}$$

A correct analysis requires to equate this current to the current through the resistor, resulting in a nonlinear differential equation. The substitution $V_C(t) = 0.5V_{\text{ref}} + 0.5V_{\text{ref}} \sin(\omega t)$ assumes that the nonlinear term is relatively small and will not substantially change $V_C(t)$. Evaluation of the last part of the equation leads to a

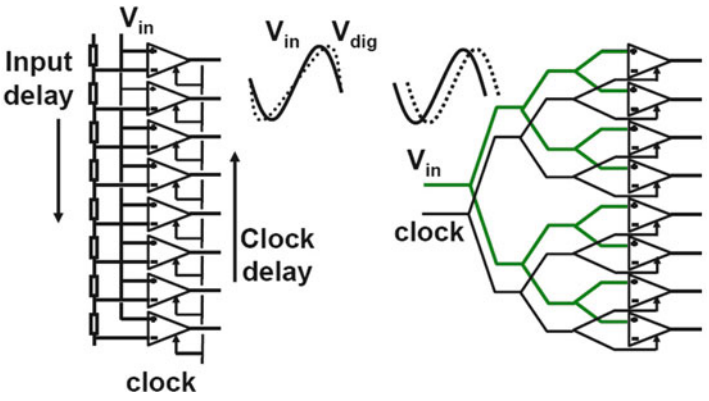


Fig. 8.25 A simple distribution strategy for input signal and clock can easily lead to performance loss at high frequencies (*left*). A tree-like lay-out is necessary to avoid delay differences

second harmonic current, which is multiplied with the input resistor R and compared to the first harmonic term in $V_C(t)$:

$$\mathrm{HD2} = \frac{\omega R \Delta C}{2}. \tag{8.12}$$

This estimate for HD2 is proportional to the signal frequency, the input impedance, and the amount of capacitive variation. For $f = 1\,\mathrm{GHz}$, $R = 50\,\Omega$, and a capacitive variation of 100 fF a distortion level of $-37\,\mathrm{dB}$ results. Changing the comparator into a full-differential design with two input terminals and two reference voltage terminals will solve this problem at the expense of more current and area.

Full-flash converters are predominantly used in high-speed applications. These applications require tight control on the timing of the converter. Jitter control is crucial to high performance; see Sect. 3.1.7. However, also in the actual design of the converter, attention has to be paid for balancing the timing accurately. The impedance of the wiring in combination with a string of load elements (e.g., inputs to the comparators) can easily lead to delay differences between individual comparators. In the example of Fig. 8.25(left) the clock and the signal come from opposing sides in the structure. For signal levels close to the bottom of the structure the signal will be delayed with respect to the sample clock, while at levels close to the top, the signal will be advanced with respect to the sample clock. In a structure where the signal conversion is linearly related to the position of the comparators, the relative delay (ΔT) of the signal versus the clock is proportional to the signal:

$$\begin{aligned} V_{\mathrm{in}}(t + \Delta T(t)) &= V_a \sin(\omega(t + \Delta T \sin(\omega t))) \approx V_a \sin(\omega t) + V_a \omega \Delta T \sin(\omega t)\cos(\omega t) \\ &= V_a \sin(\omega t) + 0.5 V_a \omega \Delta T (1 - \cos(2\omega t)). \end{aligned} \tag{8.13}$$

This timing error translates in a second-order distortion component with a relative magnitude of $0.5\omega\Delta T$. Even with modest signal frequencies of, e.g., 10 MHz and a delay of 100 ps this results in a -50 dB distortion component. This example shows that the relative timing of the signal and sample must be accurate. Therefore a treelike structure as in Fig. 8.25(right) is applied in high-performance converters.

Example 8.3. A group of comparators is on regular intervals connected to the input signal line of total length 640 µm and width 1 µm. Every comparator has an input capacitance of 0.1 pF. The clock arrives synchronously at all comparators. Estimate the expected distortion for a 100 MHz signal.

Solution. The total resistance of the wire is $(640/1) \times 0.1\,\Omega = 64\,\Omega$. The total capacitance is 6.4 pF. In Sect. 7.2.1 an analysis was made for a double terminated structure with distributed resistance and capacitance. The structure in the present example can be considered a half of that problem. So the time constant is easily found by considering that a double structure behaves with $\tau R_{\text{tot}} C_{\text{tot}}/8$ leading to $\tau = 0.2$ ns. The relative magnitude of the second harmonic component is estimated with Eq. 8.13 as 6%.

8.2.1 Ladder Implementation

In Sect. 7.2.2 the dynamic behavior of a resistor string was analyzed. This theory is applicable to the design of the ladder structure in the full-flash converter. The time constant for settling was found to be

$$\tau = rcL^2/\pi^2 \tag{8.14}$$

with r and c the resistivity and capacitance per unit length. In a full-flash converter with N-bit resolution, this equation is rewritten as

$$\tau = R_{\text{tap}} C_{\text{tap}} 2^{2N}/\pi^2 \tag{8.15}$$

R_{tap} is the resistance between two tap positions on the resistor ladder and C_{tap} represents the total capacitance on a tap and is composed of the input capacitance of the comparator, the bottom-plate stray capacitance of the resistor, and all wiring parasitics. With $C_{\text{tap}} = 0.1$ pF, $R_{\text{tap}} = 1\,\Omega$, and $N = 7$ a time constant $\tau = 0.16$ ns will result, which would allow a sampling speed of around 1 Gs/s. The ladder impedance is 128 Ω. A 1 V reference voltage over the ladder already requires 8 mA.

In a similar manner as the time constant, the DC current that, e.g., bipolar transistors or some auto-zeroing schemes can draw from the ladder can be estimated. See also example 7.1.

$$\Delta V_{\text{middle}} = R_{\text{tap}} I_{\text{tap}} 2^{2N}/8. \tag{8.16}$$

With the same parameters and $I_{\text{tap}} = 10^{-6}$ A, the voltage deviation in the middle of the ladder equals 1.6 mV. This loading effect of the ladder by the comparators is more pronounced in bipolar design. Darlington stages in the comparators are used to reduce the loading of the ladder by base currents and at the same time reduce the kickback effects [181].

This example shows that even modest specifications in a standard full-flash converter require a low-ohmic ladder. Often the ladder is constructed from the metal layers or special materials on top of the device. These materials can easily exhibit gradients and although no more than 6–7 bits of resolution is required, some precautions have to be taken to mitigate the gradients. An antiparallel connection of two ladders reduces the gradient (Fig. 7.9).

8.2.2 Comparator Yield

The key requirements for the choice of a comparator are a low capacitive load, no DC input current, low random offset, low kickback, high switching speed and bandwidth, and low power. With the exception of low random offset, most of these requirements can be met by using small-size transistors.

One of the major differences in the design of CMOS and bipolar analog-to-digital converters is the lack of accuracy in CMOS comparators. A bipolar differential pair has a random offset on the base-emitter voltage V_{be} in the order of $\sigma_{\Delta V_{\text{be}}} = 0.3$ mV. A pair of NMOS transistors with small gate lengths show random offsets in the order of $\sigma_{\Delta V_{\text{T}}} = 2$–$6$ mV; see Sect. 11.4. Because of the low CMOS gain, the offsets of the entire comparator accumulate, which may lead to $\sigma = 5$–20 mV as a total input-referred random offset.

The random comparator offset in an N-bit full-flash analog-to-digital converter (with $2^N - 1$ comparators) affects the DNL or non-monotonicity (DNL $= -1$LSB). The DNL for a converter with 2^N conversion levels is specified as

$$\text{DNL} = \frac{V_{j+1} - V_j}{V_{\text{LSB}}} - 1, \quad \forall j = 0, \ldots, 2^N - 2 \tag{8.17}$$

V_j is the value of the input signal which causes comparator j to flip and consequently contains the comparator random input-referred offset. V_{LSB} is the physical value corresponding to an LSB.

The DNL is often used as an elimination criterium and determines the yield. The actual value of the DNL, being the maximum of $2^N - 1$ differences of stochastic variables, is a random function itself. Figure 8.26 shows the distribution of the actual DNL of 1,000 8-bit full-flash converters, generated by means of Monte–Carlo simulation. The shape of the distribution is characteristic for production measurements of various types of converters. The distribution is not Gaussian as the DNL is a nonlinear function. The comparator random offset was in this example chosen to be $\sigma = 0.15 V_{\text{LSB}}$, corresponding to $\sigma = 0.586 \times 10^{-3} V_{\text{ref}}$.

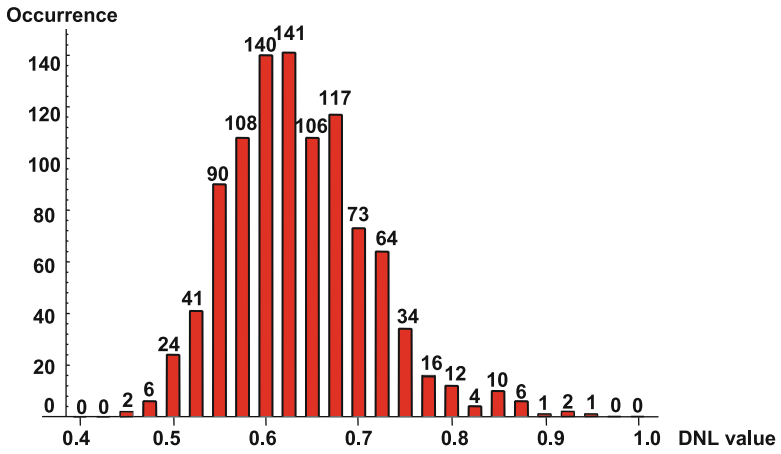


Fig. 8.26 Typical histogram of DNL values for an 8-bit full-flash architecture, with $\sigma = 0.15V_{\text{LSB}}$. The mean DNL in this simulation is 0.64 LSB

There are almost no trials with an actual DNL<0.5 LSB, although all trials result in monotonicity. For half of the trials the actual value of the DNL is lower than 0.64 LSB, which is also found in the following first-order calculation:

$$\begin{aligned} \text{Yield} = (1-p)^{2^N-2} < 0.5 \qquad & \rightarrow p > 0.9973 \\ \text{from Table 2.11} \quad p = 0.9973 \leftrightarrow \alpha = 3.0 \qquad & \rightarrow \frac{\text{DNL} \times \text{V}_{\text{LSB}}}{\sigma\sqrt{2}} = 3.0 \\ \text{with } \sigma = 0.15V_{\text{LSB}} \qquad & \rightarrow \text{DNL} = 0.64. \end{aligned} \tag{8.18}$$

The $\sqrt{2}$ factor in the second line stems from the fact that the DNL is due to the difference between two comparator trip levels.

A more formal analysis results in a yield prediction. If the input random offset of every comparator is given by a Gaussian distribution with zero mean and a standard deviation σ, then the probability of all the comparators being within the monotonicity limit can be calculated. This probability is an estimation of the yield of the analog-to-digital converter. Ideally, $(V_{j+1} - V_j) - V_{\text{LSB}} = 0$. Non-monotonicity occurs when comparator $j+1$ (fed with a rising input signal) switches before the adjacent comparator j with a lower reference voltage does. In mathematical formulation the probability that non-monotonicity occurs is $p = P(V_{j+1} < V_j)$. Then $(1-p)$ is the probability of comparators j and $j+1$ switching in the correct order; this condition must hold for all $2^N - 2$ pairs of comparators, so

$$\begin{aligned} &\text{Yield} = (1-p)^{(2^N-2)} \quad \text{with} \\ &p = P\left(\frac{V_{j+1} - V_j - V_{\text{LSB}}}{\sigma\sqrt{2}} < \frac{-V_{\text{LSB}}}{\sigma\sqrt{2}}\right). \end{aligned} \tag{8.19}$$

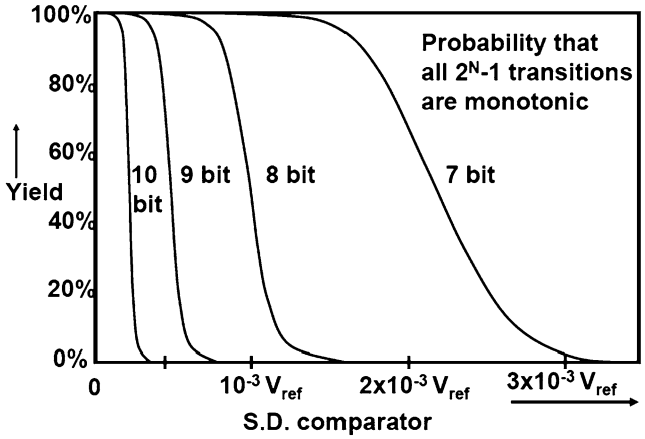


Fig. 8.27 Yield on monotonicity versus the standard deviation of the comparator random offset

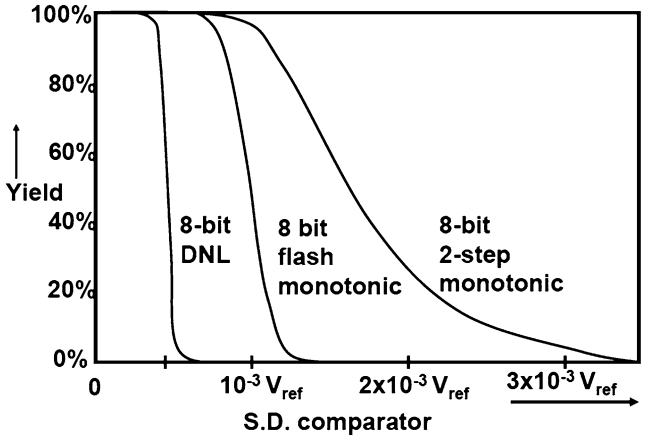


Fig. 8.28 Yield on DNL<0.5 LSB, on monotonicity for 8-bit full-flash, and on monotonicity for an 8-bit 2-step subrange architecture

The mean value of the argument in the probability function for p is 0, while the standard deviation of the argument corresponds to $\sqrt{2}\times$ the standard deviation of a single comparator σ in mV. The probability function is normalized to a standard normal curve $N(0,1)$.

Figure 8.27 shows the curves that relate the yield to the standard deviation σ of the comparator random offset for an input voltage range of V_{ref}. A 10-bit converter requires a $\sigma < 0.25 \times 10^{-3} V_{\text{ref}}$. This is still achievable in bipolar technology [182]. For higher accuracies trimming, higher input voltages or other forms of offset correction are needed. The 8-bit converter from Fig. 8.26 with $\sigma = 0.586 \times 10^{-3} V_{\text{ref}}$ is indeed monotonic with close to 100% yield.

At first sight 1-bit more resolution requires that the comparator random offset should reduce by a factor of two. A 7-bit full-flash converter has to reach an input standard deviation of $1.8 \times 10^{-3} V_{\text{ref}}$ to achieve an acceptable yield. At the 8-bit level comparators with random offset better than $0.8 \times 10^{-3} V_{\text{ref}}$ are needed for the same yield. One-bit more resolution translates in a factor two reduction of the random offset standard deviation. Moreover, the same yield must be reached with twice the number of comparators resulting in a random offset reduction factor of 1.8/0.8, slightly higher than 2.

In Fig. 8.28 the requirements are more severe: now the probability of the converter achieving a DNL of less than 0.5 LSB has been calculated. The probability p of two adjacent comparators exceeding the DNL limits is

$$\text{Yield} = (1-p)^{(2^N-2)} \quad \text{with}$$
$$p = P\left(\left|\frac{V_j - V_{j-1} - V_{\text{LSB}}}{\sigma\sqrt{2}}\right| > \frac{\text{DNL} \times V_{\text{LSB}}}{\sigma\sqrt{2}}\right). \tag{8.20}$$

As expected, the σ required for a DNL value of 0.5 LSB has been more than halved with respect to the non-monotonicity requirement.

The demands for a two-stage subranging architecture are also shown for (a theoretical minimum of) 15 coarse and 15 fine comparators. Owing to the steep nature of the Gaussian distribution the advantage of having only 15 critical comparators results in marginally more tolerance on the input random offset voltage at a 95–99% yield level. This example indicates that these yield considerations for full-flash architectures give a good first-order approximation for more complex architectures.

Table 8.1 shows the effect of increasing the resolution with 1 bit in a full-flash analog-to-digital converter. In this table it is assumed that the comparator's design comprises three transistor pairs that contribute to the random offset: the input pair, a current source pair, and a latch pair.

The first three lines specify the range and number of comparators in a full-flash converter. In line 4 the required overall yield of, e.g., 95% is recalculated to the required probability that a pair of adjacent comparators remains monotonic. This number is close to 1. For 1 bit more and double the number of comparators, this probability is even closer to 1. Now in line 5 a table for a normal distribution is used to find the number of sigma's needed to reach this probability outcome. In line 6 the input-referred mismatch is found by dividing the value of 1 bit by this number of sigma's. Another division by $\sqrt{2}$ accounts for the step from a difference between two comparators to a single comparator. In lines 7 and 8 this mismatch budget is divided over three relevant pairs of transistors in a comparator. In line 9 the required gate area is shown, and finally line 10 gives the total capacitance per analog-to-digital converter. The input capacitance is dominated by the resolution 2^{3N}, yet it remains important to come to a high ratio between reference voltage (equals the signal swing) and mismatch coefficient. The difference between the input capacitance of an N-bit and an $N+1$-bit converter is

Table 8.1 Comparison of N- and $N+1$-bit full-flash analog-to-digital converters

		N bit	$N+1$ bit
1	Input range	V_{ref}	V_{ref}
2	LSB size	$2^{-N}V_{\text{ref}}$	$2^{-(N+1)}V_{\text{ref}}$
3	Number of comparators	2^N-1	$2^{(N+1)}-1$
4	Probability per comparator pair for 95% ADC yield	$p_N = \sqrt[2^N-1]{0.95}$	$p_{N+1} = \sqrt[2^{(N+1)}-1]{0.95} \approx \sqrt{p_N}$
5	Required σ's in $N(0,\sigma)$	$S_N \approx 3\cdots4$	$S_{N+1} \approx S_N + 0.3$
6	Input-referred random error	$2^{-N}V_{\text{ref}}/S_N\sqrt{2}$	$2^{-(N+1)}V_{\text{ref}}/S_{N+1}\sqrt{2}$
7	MOS pairs in comparator	3	3
8	Random error per pair	$\sigma_N = 2^{-N}V_{\text{ref}}/S_N\sqrt{6}$	$\sigma_{N+1} = 2^{-(N+1)}V_{\text{ref}}/S_{N+1}\sqrt{6}$
9	Area per MOS	$WL = A_{V_T}^2/\sigma_N^2$	$WL = A_{V_T}^2/\sigma_{N+1}^2$
10	Capacitance of all gates	$3\times2^N A_{V_T}^2 C_{\text{ox}}/\sigma_N^2 = 18S_N^2 2^{3N} A_{V_T}^2 C_{\text{ox}}/V_{\text{ref}}^2$	$3\times2^{N+1} A_{V_T}^2 C_{\text{ox}}/\sigma_{N+1}^2 = 18S_{N+1}^2 2^{3(N+1)} A_{V_T}^2 C_{\text{ox}}/V_{\text{ref}}^2$

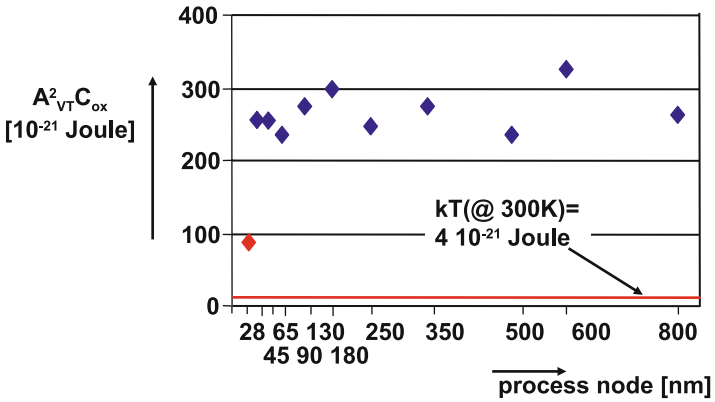


Fig. 8.29 The technology factor $A_{V_T}^2 C_{\text{ox}}$ versus process generation

$$\frac{C_{\text{in},N+1}}{C_{\text{in},N}} = \frac{8S_{N+1}^2}{S_N^2} \approx 10 \quad \text{for } N = 5,\ldots,8. \tag{8.21}$$

The last lines in Table 8.1 show that the technology factor $A_{V_T}^2 C_{\text{ox}}$ with dimension of energy, joule, is determining the outcome. This factor can be plotted versus the process generation, in Fig. 8.29. It is clear that the energy associated with threshold mismatch hardly changes over time. Given the reducing power supply (from 3.3 V down to 1.1 V) this implies that the power efficiency of straight-forward full-flash architectures will not scale and perhaps even deteriorate. The first indications on the performance in 28-nm high-k factor metal-gate processes are promising.

Table 8.2 Comparison of 7- and 8-bit full-flash analog-to-digital converters

		7-bit	8-bit
1	Input range	1 V	1 V
2	LSB size	7.8 mV	3.9 mV
3	Number of comparators	127	255
4	Probability on monotonicity per comparator pair for 95% ADC yield	0.99960	0.99980
5	Required σ's in $N(0,\sigma)$	3.35	3.55
6	Allowed input-referred random error	2.33 mV	1.10 mV
7	Number of MOS pairs in comparator	3	3
8	Random error per input pair	1.34 mV	0.63 mV
9	Area per MOS $A_{V_T} = 3.5\,\text{mV}\,\mu\text{m}$	6.8 μm^2	30.7 μm^2
9	Capacitance per MOS $C_{ox} = 12.6\,\text{fF}/\mu\text{m}^2$	86 fF	387 fF
11	Capacitance of all input gates	11 pF	99 pF

Table 8.3 The calculated yield for 6, 7, and 8 bit

N	V_{LSB} (mV)	x	$P(x)$	$P^{2^N}(x)$
6	15.6	7.1	$1-10^{-11}$	0.999999
7	7.8	3.55	0.0002	0.975
8	3.9	1.77	0.0384	4×10^{-5}

Example 8.4. Compare the input capacitance of a 7-bit and an 8-bit full-flash converter with 1-V input range in a 65-nm process.

Solution. Table 8.2 shows the effect of increasing the resolution with 1 bit in a full-flash analog-to-digital converter.

Example 8.5. In a simple flash converter the size of the transistor input pair of the comparators is 20/5 µm in a process with $A_{V_T} = 15\,\text{mV}\,\mu\text{m}$. The expected input signal is $1\,\text{V}_{\text{peak}-\text{peak}}$. What resolution limit (if monotonicity is required with 99% yield) do you expect?

Solution. Monotonicity means that in case of an increasing input voltage, the comparator connected to a lower reference voltage switches before the comparator connected to a V_{LSB} higher reference voltage. The standard deviation of the input pair and trip level is calculated as: $\sigma_{\text{trip},i} = A_{V_T}/\sqrt{WL} = 1.5\,\text{mV}$, ignoring other contributions. The nominal difference between two trip levels is $V_{LSB} = 2\text{V}/2^N$. As both trip levels suffer from uncertainty, the standard deviation of the difference equals $\sigma_{i+1,i} = \sqrt{\sigma^2_{\text{trip},i+1} + \sigma^2_{\text{trip},i}} = 1.5\sqrt{2}\,\text{mV}$. The probability $P(x)$ that the difference between two trip levels stays within V_{LSB} corresponds to the value of a normal $N(0,1)$ distribution for the quantity $x > \sigma_{i+1,i}/V_{LSB}$.

Monotonicity in a converter requires that all 2^N differences are within one LSB. So this probability requires to multiply all 2^N individual probabilities. Table 8.3 shows that a 7-bit converter is at the edge of acceptable yield.

The faster way to this result uses Fig. 8.27.

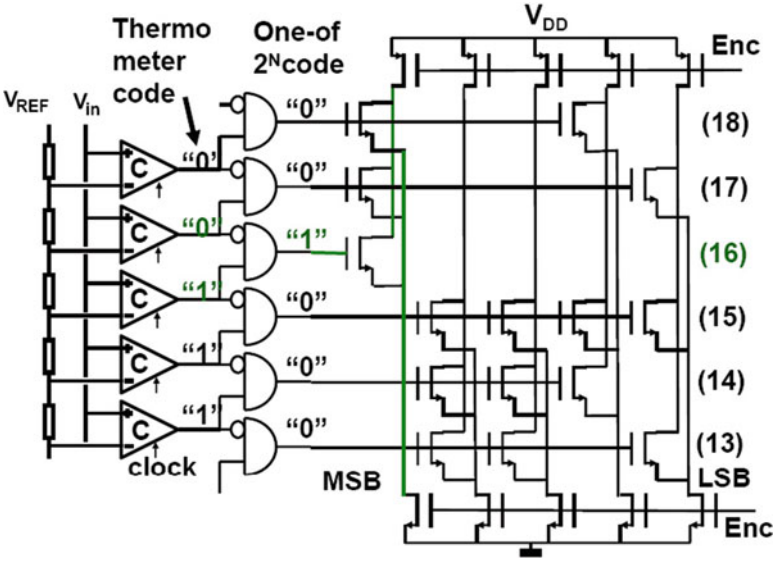


Fig. 8.30 A wired NOR based decoder scheme

8.2.3 Decoder

In many analog-to-digital converters the decoding of the comparator decisions into a digital output word is not a problem, only the algorithm behind the decoding is interesting. Figure 8.30 shows a basic wired NOR decoding scheme for a full-flash converter. The decoding starts by a simple gate that converts the thermometer code at the output of the comparators in a 1-of-*N* code. This is the digital form of the mathematical derivative function. The function will indicate the pair of comparators where the input signal is between the reference values. The corresponding decode line is connected to a matrix of transistors laid-out in a straight binary code. The above-sketched operation can be disturbed by various mechanisms. If mismatch creates a situation where a lower or higher comparator switches too, more than one wired NOR input lines will be active. These errors are called "sparkles" or "bubbles." This situation can also occur in the presence of high-slew-rate signals or metastability errors. Most of these sparkles will create a deviating code; however, if the sparkle affects a decode region around a major bit, full-scale errors can be the result. There are numerous ways to avoid that these sparkles upset the decoder. Figure 8.31 simply extends the thermometer decoding with an additional input. Many other solutions exist where different trade-offs with speed are made.

In many medium performance applications this scheme will work fine. However, if the operating frequency is increased to the limits of the technology, performance problems arise. At high operating frequencies the inherent capacitive load of a wired NOR structure becomes a burden. Buffering is required at the cost of

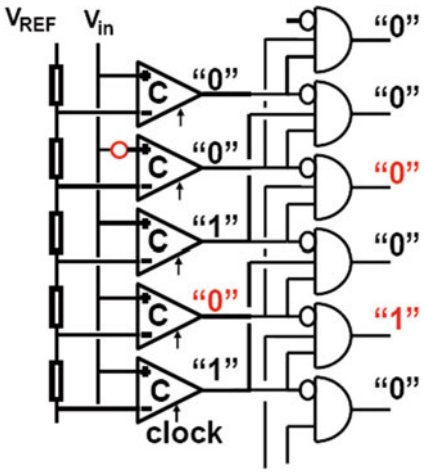


Fig. 8.31 A wired NOR-based decoder scheme with bubble correction

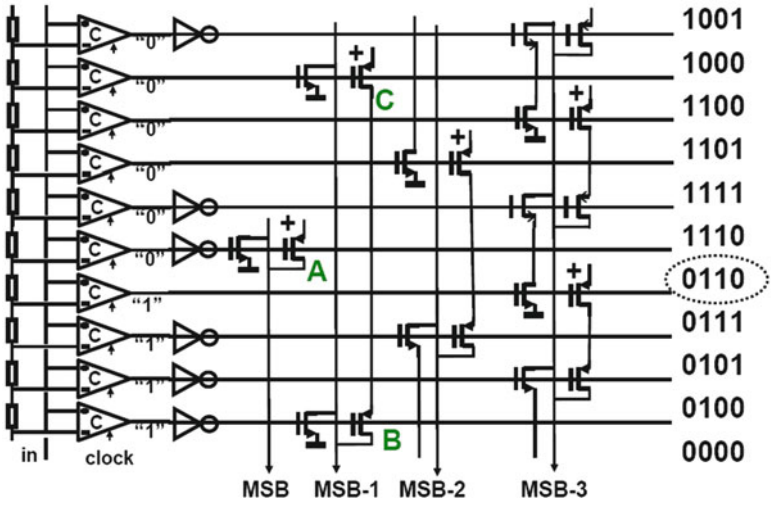


Fig. 8.32 A wired gray-decoder scheme

power. In advanced processes the parasitic wiring capacitance fortunately reduces significantly thereby allowing fast processing of the decoding signals.

The above decoding schemes show a disadvantage in case of metastability. A meta-stable comparator output in Fig. 8.30 will affect two decode gates and their associated decode lines. If the metastable condition continues, opposing signals may appear in the two decode gates and a major decoding error will happen.

The MSB line in the Gray-decoding scheme of Fig. 8.32 is controlled via a comparator and two inverters. The last inverter, labeled "A," drives the output line. The MSB-1 uses two gates "B" and "C." For a signal on the input terminal lower than the reference voltage of this scheme, all comparators will signal a logical zero.

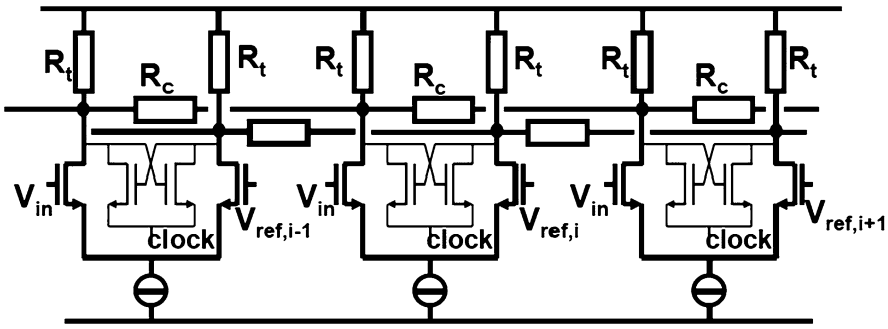


Fig. 8.33 The averaging scheme after [183]

Gate "B" receives a logical one and the NMOS will pull the line to a logical zero state. After the input signal increases to the level corresponding to the encircled code in Fig. 8.32 the input of gate "B" will go to logical zero just as gate "C." Via both PMOS devices the MSB-1 line is set at a logical one state. If the input signal exceeds the reference levels in this drawing, the input to gate "C" will be a logical one, pulling the MSB-1 line to zero.

Each comparator in a Gray-decoder sets one single output line. A potential metastable condition does not spread out over more than one cell and can still be resolved if more time is allowed. The Gray code is an often used strategy in the first part of the decoder. For large decoders the remaining decoding can be done in conventional style.

8.2.4 Averaging and Interpolation

The main problem for improving the accuracy of a full-flash converter is the mismatch of the comparator stages. This mismatch directly translates in INL and DNL performance loss. In order to alleviate this problem the ratio between signal amplitude and input-referred random offset of the comparators must be improved. Since the early 1990s two techniques are applied for this purpose: averaging and gain stages with interpolation. The random mismatch problem in traditional full-flash converters is based on the ratio of the input signal and random offset in one comparator stage. The fundamental observation by Kattmann and Barrow [183] is to combine multiple input stages. The signals of these stages are added up linearly, while their mismatch adds up in a root-mean-square manner. Consequently their ratio will improve if more input stages are combined. Figure 8.33 shows the topology. The input stages of the comparators generate a differential current that forms a differential voltage over the resistors R_t. These currents are combined through coupling resistors R_c.

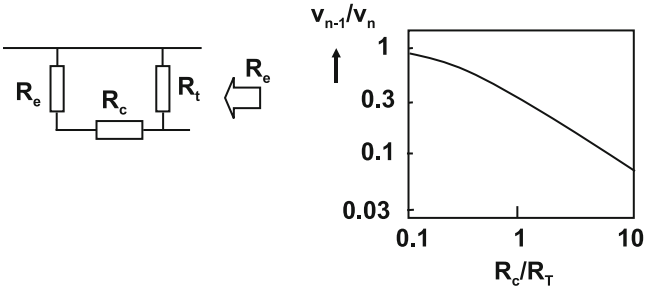


Fig. 8.34 Starting point for the analysis is the equivalent resistor network on the *left*. Equation 8.23 is shown to the *right* [184]

Figure 8.34(left) shows a part of the resistor network. R_e is the equivalent impedance seen to the left and R_t and R_c add another stage to this network. Now the equivalent resistance after the addition of these two elements should again be equivalent to R_e. Some arithmetic gives [183, 184]

$$\frac{R_e}{R_t} = -\frac{1}{2}\alpha + \frac{1}{2}\sqrt{\alpha^2 + 4\alpha}, \tag{8.22}$$

where $\alpha = R_c/R_t$. Based on this equivalent impedance the effect of the coupling resistor R_c on various performance aspects can be derived. If one input pair creates an offset current resulting in a voltage v_n over resistor R_t, then the impact of v_n on the neighboring voltage v_{n-1} is

$$\frac{v_{n-1}}{v_n} = \frac{-\alpha + \sqrt{\alpha^2 + 4\alpha}}{\alpha + \sqrt{\alpha^2 + 4\alpha}}. \tag{8.23}$$

With $\alpha = 1$ this factor is 0.38. Equation 8.23 is depicted in Fig. 8.34(right). A small α (low R_c) increases the coupling between the node voltages and improves the ratio between the linear signal component and the stochastic variation. Also the range of comparators that contribute is increased. This range cannot be made infinitely long because only comparators with input stages operating in the linear regime can effectively contribute. As an example Bult [185] used an averaging over five stages.

An issue with the averaging technique is the termination of the range. A low α factor means that a larger number of neighboring comparator stages are combined and a better random offset reduction is achieved. Near the limits of the range this means that a relatively large number of additional comparators are needed for achieving also an offset reduction at the extremes of the converter range. Scholtens [184] has proposed to use a dedicated termination cell at the end of each side of the comparator structure, which reduces this problem. Other techniques involve folding or are based on the Möbius band.

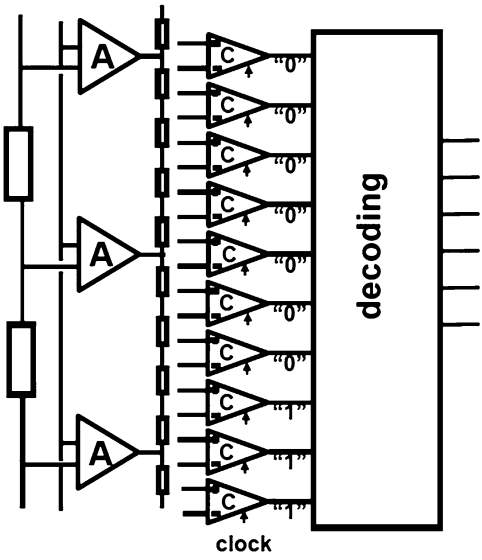


Fig. 8.35 A gain stage is applied to increase the voltage swing on the comparators

A second form of improving the ratio between the signal and random mismatch is shown in Fig. 8.35. In this scheme a group of additional amplifiers is placed before the comparators. The amplifiers locally boost the difference voltage between the signal and the adjacent reference voltages. The result is applied to an interpolation ladder. A typical gain stage will serve 4–8 comparators. The trade-off in this scheme is between the additional power needed for the high-performance gain stages and the reduction on the side of the comparators.

Figure 8.36 shows a full-flash converter placed in a system-on-chip design. Frequently averaging and interpolation are combined into the same design [184, 186].

8.2.5 Frequency-Dependent Mismatch

So far, no frequency dependencies of the input gain stages have been considered. Figure 8.37 shows an example of comparators during offset reduction. The offset reduction is accomplished by means of a gain stage before the latch stage. These elements can be identified in most offset reduction schemes. The latch stage is considered ideal except for a load capacitor C and a random offset source V_o. Both are related to the latch transistor dimensions by $C = WLC_{\text{ox}}$ and $\sigma_{Vo} = A_{V_\text{T}}\sqrt{N_T/WL}$. A_{V_T} is the process constant for threshold matching (Sect. 11.4) and N_T is the number of latch transistor pairs that contribute to the random offset. For low-frequency operation the input-referred mismatch due to the latch mismatch is calculated by dividing the latch mismatch by the effective DC gain. For high-frequency operation the input-referred random offset due to the latch is given by σ:

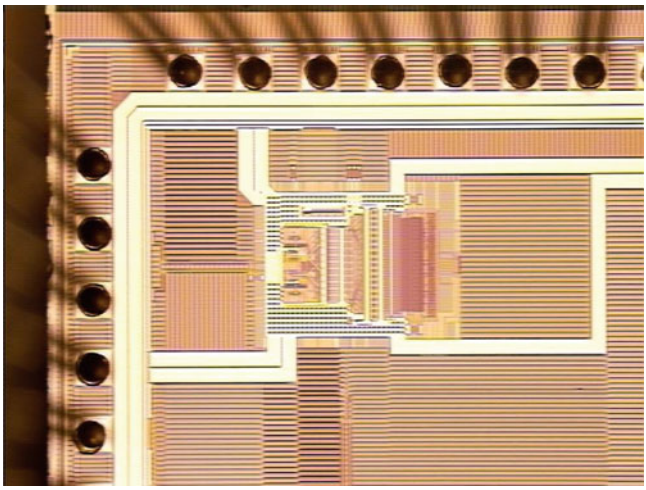


Fig. 8.36 A picture of a 6-bit full-flash ADC converter [184]

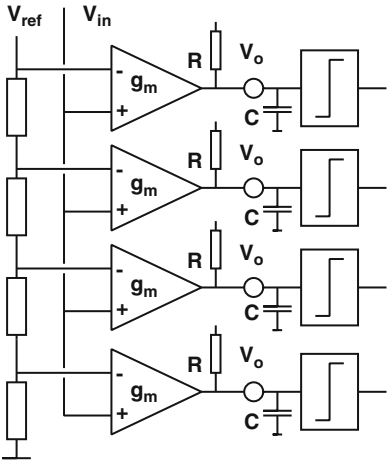


Fig. 8.37 Random offset reduction by means of a gain stage

$$\sigma = \frac{\sigma_{Vo}(1+j\omega RC)}{g_m R} \approx \frac{A_{V_T}\omega C_{ox}\sqrt{N_T WL}}{g_m} \qquad \omega RC > 1. \tag{8.24}$$

This is only a rough approximation, which must be adapted for the sample-and-hold operation, timing, and different architectures. It indicates that random-offset reduction is frequency limited and depends on design (N_T, g_m), technology (A_{V_T}, W, L), and power (g_m, number of comparators). For example, in a 1 µm CMOS technology $\sigma_{Vo} \approx 20$ mV, $gm/2\pi C \approx 250$ MHz, so the desired input random offset of 0.8 mV can be achieved up to 10 MHz bandwidth.

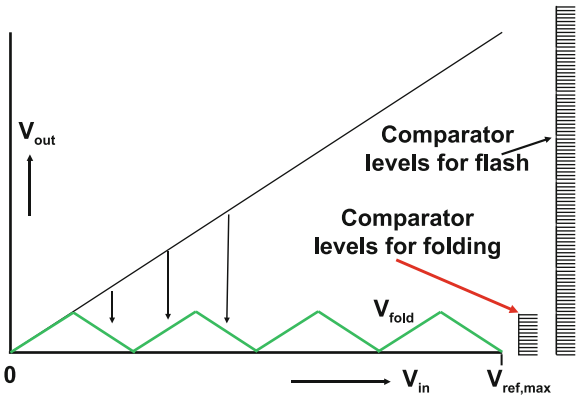


Fig. 8.38 A folding analog-to-digital converter folds the input signal into a smaller signal range

8.2.6 *Technology Scaling for Full-Flash Converters*

In 90-nm, 65-nm, and 45-nm various analog design constraints appear that affect the performance of converters. A few of these effects are:

- The power supply drops to 1 V. As a consequence all signal levels will be lower. Differential design is imperative, yet it will be difficult to handle more than 0.3 V of single-sided signal swing.
- Thresholds go down in order to keep the current drive at an acceptable level. Low-threshold voltages are not convenient for cascode structures because the input and output DC levels start to differ too much.
- The mismatch for a fixed area device is less predictable due to additional implants. At 45 nm the same transistor size may show comparable random variation as in 90 nm.
- The beta factor is low for minimum size devices; it can be improved by backing off on the designed gate length; see Fig. 2.44.
- The construction of the transistor with high additional pocket dopes near channel to control the electric fields (halo implant) leads to a low intrinsic amplification factor of the device.
- Deep *n*-well constructions reduce substrate noise and allow floating NMOS devices next to the floating PMOS devices.
- Gate leakage of transistors with less than 1.5-nm effective gate oxide becomes a issue as the gate current (1–10 nA/µm gate width for 1.2 nm gate oxide) will load the ladder.

8.2.7 *Folding Converter*

A variant of a full-flash converter is the folding analog-to-digital converter [2, 168, 187, 188] in which a preprocessing stage "folds" the input signal. Figure 8.38 shows

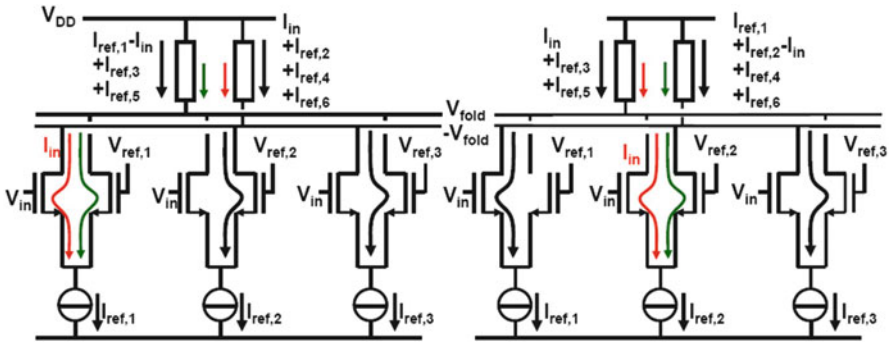


Fig. 8.39 The basic folding circuit: the input pairs are designed to reverse the signal current in the top resistors for each folding section

the general idea: the input signal is folded into (in this example) eight sections. The resulting folded range is applied to the succeeding analog-to-digital converter and is reduced to 1/8 of the original range. Next to this analog-to-digital converter, this method requires a circuit that performs the folding operation and a coarse analog-to-digital converter to keep track of the section number. This partitioning reduces the total number of comparators. If an 8-bit flash converter is split in eight folding sections (3-bit) and a remaining 5-bit fine flash converter, a total of $2^3 + 2^5 = 40$ comparators are needed. The folding principle was originally developed in bipolar technology [187, 189]. Later on the folding principle was applied in CMOS analog-to-digital conversion [168, 170]. In both technologies the basic topology is a parallel arrangement of differential pairs. These pairs are driven by the input signal and have each a local reference voltage of $1/16, 3/16, 5/16, \ldots$ of the full-scale reference voltage. In Fig. 8.39 the first three sections of a folding stage are depicted. In this example the reference voltages are chosen for $F = 8$ folding sections spaced at $1/F$ fractions of the overall reference voltage. The transconductance of each stage is designed to cover an input voltage range of $\pm 1/2F$ of the reference voltage. In this setting the F stages cover the entire input range. The signal itself will select the input stage. The output of the folding stage on an input ramp is a triangle-shaped signal with a periodicity of half of the number of fold sections. A full-range sinusoidal input signals will be multiplied with this triangular function and generate frequency folding signals at $(F + 1)$ and $(F - 1)$ times its own frequency. A full-range input signal results in a folding signal with $(F + 1)$th and $(F - 1)$th harmonics. Smaller signals use less folding stages and result in lower-frequency harmonics. This multiplication effect is a potential cause for distortion products in a folding analog-to-digital converter when this higher-order signals proceed to the output. Moreover the bandwidth of the output stage needs to accommodate these frequencies. After the folding stage some gain can help to reduce the accuracy requirements for the comparators in the succeeding full-flash stage.

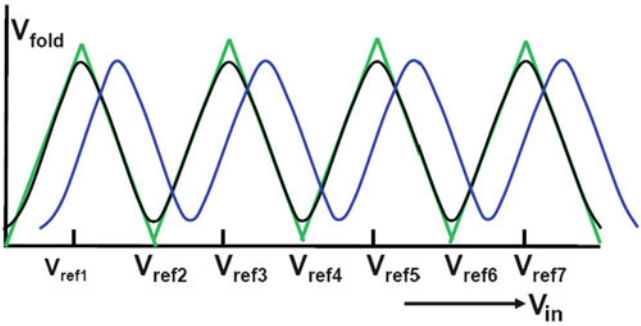


Fig. 8.40 The basic folding circuit suffers from distortions near the switch points. In a practical design two folding circuits with a mutual offset allow an interpolation scheme to determine the switching levels

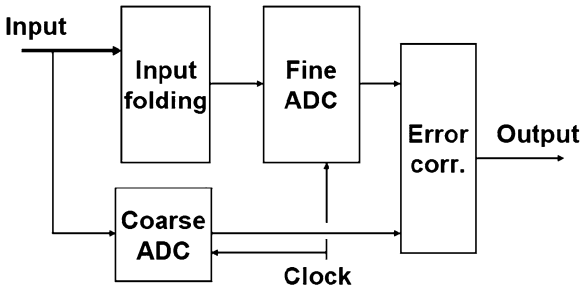


Fig. 8.41 A folding analog-to-digital converter architecture incorporating a sample-and-hold [168]

The crossover point between the stages in the basic concept is a weak point in the architecture of Fig. 8.39. In order to mitigate the problems with the crossover points, mostly a dual folding architecture as in Fig. 8.40 is used. The second folding stage is shifted by half of the range of a single folding section $1/2F$, thereby creating a linear transfer at the crossover points of the first folding stage. The coarse sub analog-to-digital converter selects the linear part of the transfer curves. More recent designs use a resistive interpolation technique between the outputs of these voltage-shifted folding stages. This results in bundles of transfer curves where the comparators trigger at the crossover of the appropriate combination of (interpolated) folding signals [168, 185]. Proper design of the preprocessing stage where high speed and high yield are combined is the critical issue.

The architecture of Fig. 8.41 requires a sample-and-hold circuit. The first observation is that the input signal uses two paths through this converter: the path via the coarse converter and the path through the folding stage. The outcome of these paths must remain synchronous within one clock period. The advantage of using a S/H circuit is that signal propagation errors in the analog preprocessing are reduced and that architectures can be used that make multiple use of the input signal. The second reason for using a sample-and-hold lies in the observation that folding stages generate frequency multiples of the input. A sample-and-hold will reduce

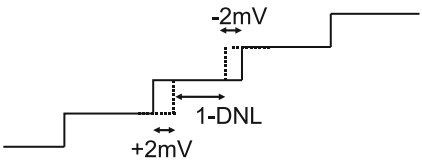


Fig. 8.42 The shift of two trip levels in a worst case situation

this problem to a settling issue. Design experience has shown that a high-speed S&H running at full signal and bandwidth requires 30% of the total analog-to-digital converter power budget.

The remaining problem with folding analog-to-digital converters is random offset in the folding input pairs. Any deviation in one of the folding stages will translate in performance loss. An attempt has been made to address this issue [185] by using an interpolation method at the cost of a lot of power. In bipolar technology a performance level of 10 bits has been reported [190], while in CMOS an 8–9-bit level is state of the art [168, 170, 185]. A form of calibration can further improve the resolution [191].

Example 8.6. In an AD converter with an input range of 1.024 V the comparator can have an input-referred error of maximum/minimum $+2/-2$ mV. What is the best resolution a full-flash converter can reach if a DNL of maximum 0.5 LSB is required? Which converter type could reach a better resolution?

Solution. A DNL error is caused because the trip levels shift due to comparator mismatch (Fig. 8.42). In this case potentially the ith trip level can shift $+2$ mV, while the $i+1$th trip level shifts -2 mV. These two errors together cause a maximum DNL error of 0.5 LSB. Consequently $0.5V_{\mathrm{LSB}} = 2+2$ mV. An LSB size of 8 mV results in a 7-bit converter.

Any converter based on a single comparator can perform better, e.g., a successive approximation converter.

8.2.8 Digital Output Power

The result of an analog-to-digital conversion is a digital word changing its value at the speed of the sample clock. Obviously this interface to the digital processing consumes power as is given by the standard digital power equation. Charging a capacitance C_{load} requires $C_{\mathrm{load}}V_{\mathrm{DD}}^2$ energy from the power supply. Assuming that at every sample pulse half of the N output pins will change state and only half of those will require energy from the power supply yields

$$P_{\mathrm{dig-out}} = N f_s C_{\mathrm{load}} V_{\mathrm{DD}}^2/4.$$

With $f_s = 1$ GHz, $V_{\mathrm{DD}} = 1$ V, $N = 10$ bit, and on-chip capacitive load of $C_{\mathrm{load}} = 1$ pF, the power consumption is 10 mW. Much of this power contains signal-related

components that can cause serious performance degradation if these components influence the analog signals. The digital output power is preferably delivered by a separate power supply.

If an external load must be driven by the digital output, the capacitive load is at least an order of magnitude higher: 10–20 pF. The power needed in the digital output driver climbs to 0.2 W or more. Special precautions must be taken to avoid coupling between these drivers and the rest of the analog-to-digital converter and other analog circuits. Separate power wiring, power bond pads interleaved between the output bits. Also the heat production of the drivers can be of importance. There are various ways to reduce the effect of the digital output section. Examples are: reducing the output load[5] by connecting an extern digital register closely to the analog-to-digital package, low-swing outputs, and small damping resistors in series. More expensive measures implement differential output ports or digitally coded outputs. Low-sample-rate converters can use a parallel-to-series output. All N data bits are shifted out via a single bond pad at a clock rate of $N \times f_s$. In fact, this will not reduce the needed output power, but the much higher frequencies will contain less signal-related energy.

8.3 Subranging Methods

For accuracies of 8 bits or more, full-flash converters are no economical solution due to the exponential growth of input capacitance, area, and power. Multistep methods allow to achieve higher resolutions. In Fig. 8.43 the signal flow in a two-step converter is shown. The signal is sampled and held at the input. A limited

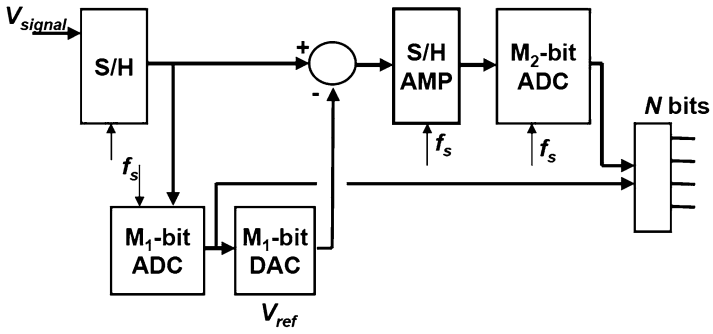


Fig. 8.43 Block diagram of a two-step converter

[5] An often encountered error is a direct connection between the ADC chip and the input port of a laptop. Certainly some spurs related to the internal processing will be visible in the analog-to-digital conversion spectrum.

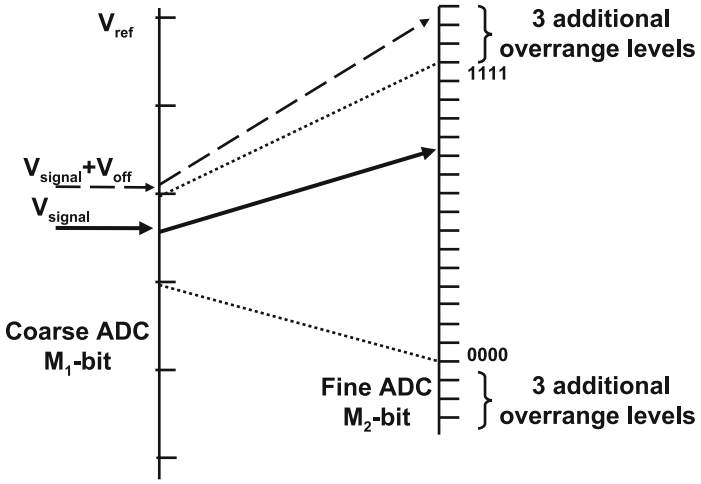


Fig. 8.44 Coarse-fine conversion: on the *left-hand* scale the trip points of the first (*coarse*) converter are indicated. The remaining signal (*bold line*) is amplified and converted by the second (*fine*) converter. The *dashed arrow* indicates a situation where the coarse converter has decided for the wrong range. Over range in the fine converter corrects this decision

resolution analog-to-digital converter (a small full-flash) with a resolution M_1 estimates the signal. This information is fed to a digital-to-analog converter and subtracted from the held input signal. The subtraction results in a residue signal, with a maximum amplitude fraction of 2^{-M_1} of the input range. This signal is amplified in a second S&H gain stage. A second converter with a resolution M_2 converts this residue signal. This simple approach results in a converter with a resolution of $M_1 + M_2 = N$. In this elementary approach of this converter only $2^{M1} + 2^{M2} \ll 2^N$ comparator circuits are needed. Converters based on this principle are known under names as "subranging analog-to-digital converters," or "coarse-fine analog-to-digital converters."

For this type of conversion additional components are present such as sampling circuits and an additional digital-to-analog converter. After the subtraction the amplitude of the remaining signal is small: an additional amplification step boosts the signal and consequently reduces the effects of errors in the succeeding processing.

8.3.1 Overrange

A disadvantage of the set-up in Fig. 8.43 with $M_1 + M_2 = N$ is the need for a perfect match between the ranges of the first and second converters. If the first (coarse) converter decides for the wrong range, there is no correction possible. However, by adding additional levels on both sides of the second converter range (see Fig. 8.44),

errors from the first converter can be corrected [192]. This "over range" limits the accuracy requirements on the coarse analog-to-digital converter. In some designs the over range doubles the total range of the fine converter.

Full accuracy (N-bit) is still needed in the digital-to-analog converter and in the subtraction circuit. Implicit in this method is that the subtracted portion of the signal is known with the accuracy of the full converter. The speed of this converter is in first instance limited to the time needed for the input track-and-hold, the first coarse conversion, the digital-to-analog settling, the subtraction, and the second fine conversion. This processing can however be pipelined over two sample periods by inserting a track-and-hold circuit behind the subtraction and amplification point. Now two successive samples are processed in a pipelined fashion, and the sampling speed is limited to the processing speed of just a single section.

The over range feature allows to reduce the time for the signal to settle in the chain from coarse converter, via digital-to-analog converter and subtraction node. The resulting error and the potential offsets should remain within the over range section. This observation allows a considerable increase of the speed. The principle of coarse-fine conversion can be extended to three or more stages and resolutions of 14–15 bits [193].

8.3.2 Monkey Switching

The principle of subranging is limited by the quality of the correspondence between the digital-to-analog conversion and the fine conversion range. There are various ways to link the output of the coarse conversion to the fine range. In Fig. 8.45 an elementary connection topology is depicted. The fine ladder is connected to the selected range of the coarse ladder via two buffers A and B. These buffers can have a gain of 1 or more. If these buffers suffer from offsets the range defined by the coarse ladder will be stretched or shrunk. In Fig. 8.45 the buffers A and B move over the coarse ladder in a fixed mutual position: A is connected to the low side of the coarse-ladder tap and B to the high side and this order remains if the signal increases the sample that is in the adjacent coarse-ladder segment. This sequence causes an INL and a DNL error at the transition points and shows up in the integral and in the differential linearity plots. Especially the sharp transition at the coarse conversion transitions leads to large DNL errors.

In Fig. 8.46 the control of the connections is different: if the converter decides to connect to a higher segment the lower buffer (A in this example) is disconnected and reconnected to the top side of the next higher segment, while buffer B remains connected to the same tap of the coarse ladder. When increasing the input voltage slowly the buffers will alternately connect. This method is often referred to as "monkey switching."[6] The DNL transitions are strongly reduced. However, the INL

[6]Some similarity exists with the way a monkey climbs a tree.

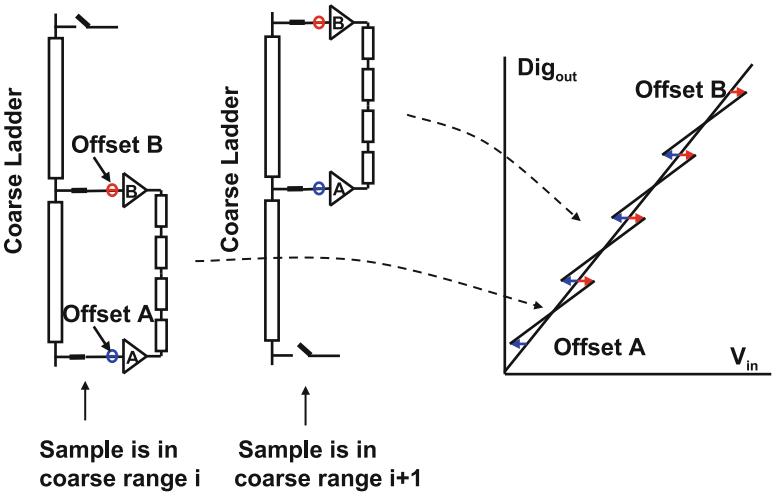


Fig. 8.45 The effect of offset in a subranging scheme. INL and DNL are degraded at the coarse code transitions

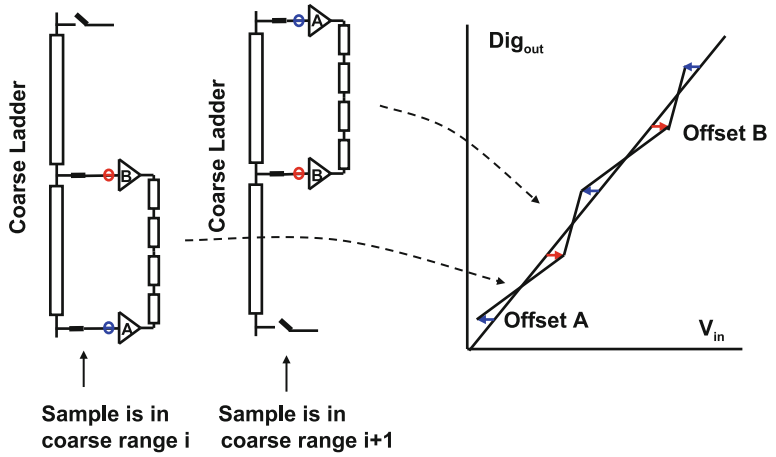


Fig. 8.46 The effect of offset can be reduced by appropriate switching schemes. Only the INL is seriously degraded at the coarse code transitions while the DNL is reduced

errors remain and are visible together with the errors in the fine converter as a repetitive pattern; see Fig. 8.47. For a recent alternative see [194].

The setup of the timing is essential especially if additional time periods are allocated to offset cancellation. Typically the coarse converter is activated after some 10–20% of the hold period. This allows maximum time for the digital-to-analog converter, the subtraction mechanism, and the succeeding amplifier to settle.

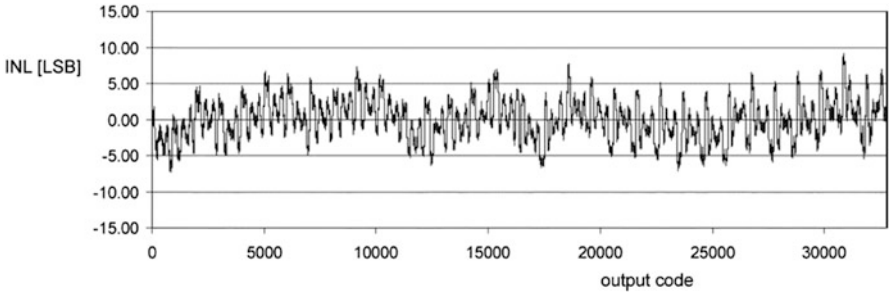


Fig. 8.47 Sub-ranging converters show a repetitive pattern in their transfer curve. This curve is from a 15-bit resolution converter [193]

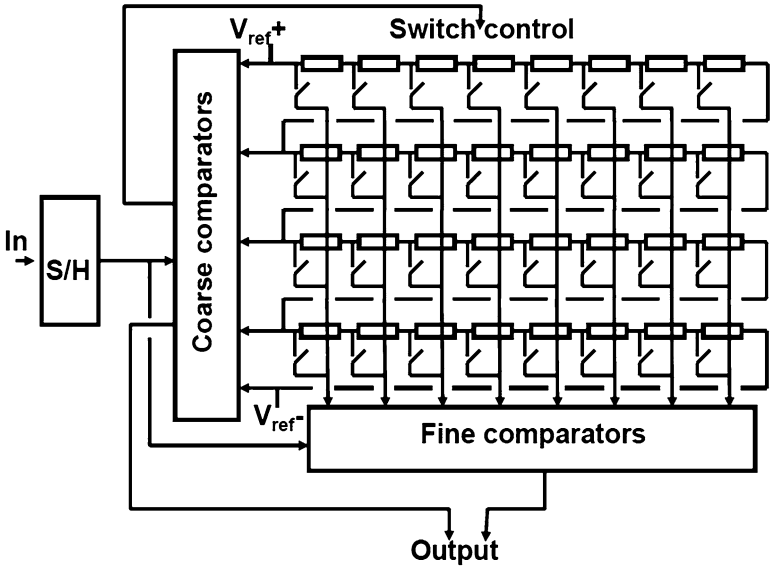


Fig. 8.48 A subranging analog-to-digital converter based on a switched resistor array [160, 175, 178]

An alternative to the standard subrange scheme avoids the subtraction and the issues due to offsets between fine and coarse sections. A resistive ladder structure feeds both the coarse and the fine converter sections [160, 175, 178, 179] as shown in Fig. 8.48. The coarse comparators are connected to ladder taps spaced at eight LSB positions apart. The decision of the coarse converter will select a row of switches which is then fed to the fine comparators. Another extension [175] is to use two banks of fine comparators that will alternately digitize the signal, thereby allowing more time for the settling process. In [178] a capacitive interpolator is used to form the intermediate values for the fine conversion.

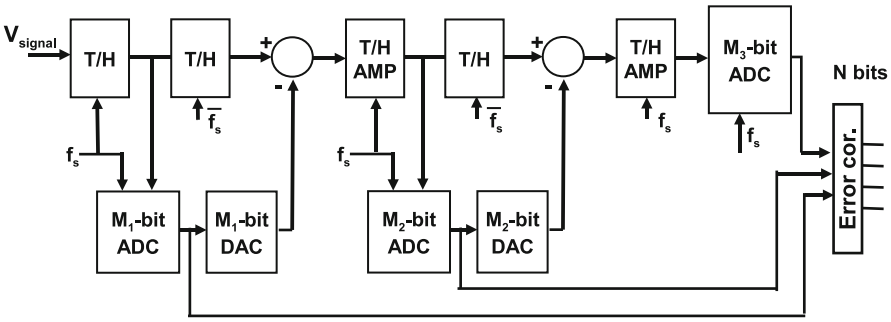


Fig. 8.49 A subranging analog-to-digital converter with three sections. A typical partitioning uses $M_1 = M_2 = 5$ bits and $M_3 = 4$ bits for a 14-bit converter

These methods use the main resistive ladder structure for both the coarse and fine conversion. This requires special measures to keep the spurious voltage excursions on the ladder under control. In [160] this is realized via a second low-ohmic ladder in parallel to the main ladder similar to Fig. 7.44.

The dominant implementation of stand-alone subrange analog-to-digital converters for industrial applications[7] uses a three-stage approach [195]; see Fig. 8.49. The first stage typically converts 4–5 bits and is equipped with a high-performance track-and-hold. The reduction of the distortion in the track-and-hold is the dominant challenge in these converters. A low distortion results in an excellent spurious free dynamic range (SFDR), which is required for communication systems such as mobile phone base stations. The succeeding stages use 5 bits and 4–6 bits in the last stage. The different track-and-hold stages run on different clocks to allow the optimum usage of the sample period.

For a nominal resolution of 14 bits the ENOB ranges from 11.3 to 11.8 bits. Sample rates between 150 and 400 Ms/s are available with power consumptions ranging from 400 mW at 80 Ms/s to 2 W for 400 Ms/s. The SFDR ranges from 80 to 95 dB. Special low-swing digital output stages (LVDS) are applied to suppress digital noise. For a more elaborate comparison see Sect. 12.2.

Example 8.7. In a 10-bit 1-V subrange ADC the buffers between the 7-bit coarse and the 3-bit fine converter have 3 and -2 mV offsets. Sketch the resulting INL in case the buffers are switched directly or in a "monkey" way. What is in both cases the largest DNL?

Solution. Figure 8.50 shows a part of the transfer curve in case the low-side buffer has a positive offset and the high-side buffer a negative offset. A plateau appears in

[7] See data sheets from ADI, TI, and NXP. Some 2010 products: AD9640, AD6645, ADS5474, and ADC1410. In some data sheets these converters are called pipeline converters. In the terminology of this book they are classified as subrange converters.

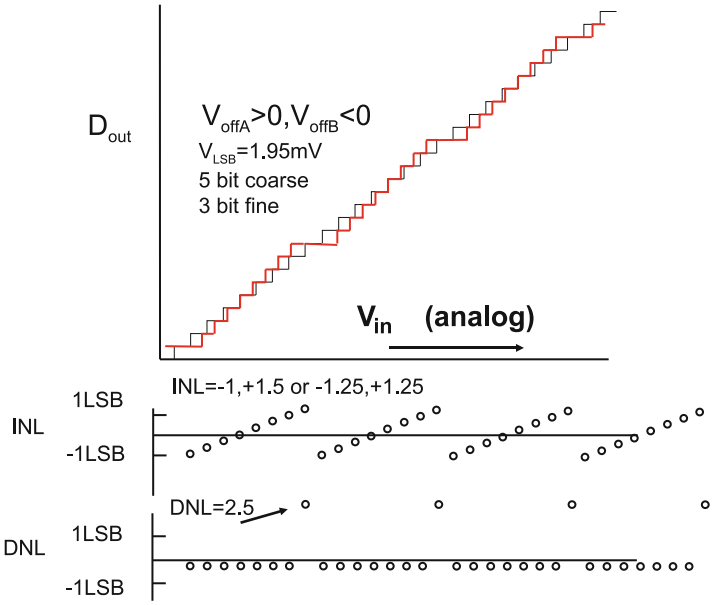


Fig. 8.50 Transfer curve, INL, and DNL for a 3-bit fine section in a two-step analog-to-digital converter, with offsets in the buffers

the overall transfer curve with a DNL error corresponding to the offsets divided by V_{LSB}. If the offset appear the other way around, the transfer will look like Fig. 8.51. In this example two codes will be missing.

Figure 8.52 shows the effect of the monkey-switching scheme. The maximum deviation of the INL has not changed, as it is determined by the offsets, but the local deviations at the ends of the fine range have largely disappeared. The remaining transfer curve consists of 8 codes that are together $|V_{\mathrm{off},A}| + |V_{\mathrm{off},B}|$ too large, followed by 8 codes that are the same amount too small. The DNL error per code is 5 mV/8; related to a 10-bit LSB this would result in DNL = 0.6 LSB.

8.4 1-Bit Pipeline Analog-to-Digital Converters

Subranging avoids the exponential hardware and power increase of flash conversion. Using more bits per subrange stage reduces the number of stages needed and the associated track-and-holds. If the first stage is implemented with M_1 =3–5 bits, the intermediate gain can be 2^{M_1}, thereby reducing the influence of errors in the succeeding stages. When a design is pushed to the limits of the technology, the maximum unity-gain bandwidth is determined by the available power. More intermediate gain will then correspond to slower settling. Reducing the subrange to the extreme results in subranges of one single bit. Therefore a popular variant

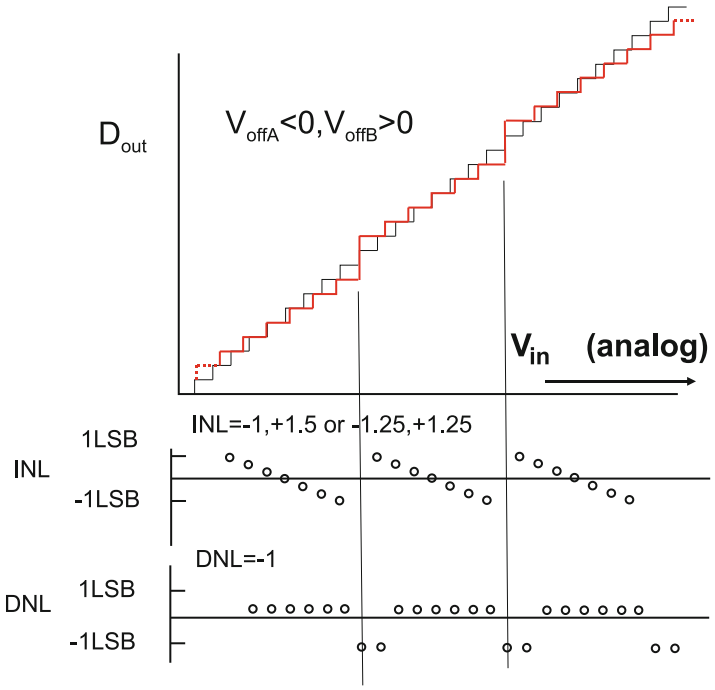


Fig. 8.51 Transfer curve, INL, and DNL for a 3-bit fine section in a two-step analog-to-digital converter, with opposite offsets in the buffers

of the subrange analog-to-digital converter in CMOS technology is the "pipeline" converter (Fig. 8.53) [192, 196]. This converter consists of a pipeline of N more-or-less identical 1-bit stages. For each bit of resolution there is one stage. Each stage comprises a track-and-hold, a comparator connected to a 1-bit digital-to-analog converter, a subtraction mechanism, and a multiplication circuit.

The important advantages are fast settling due to a low interstage gain (2 or less) and a 1-bit digital-to-analog converter. With only two output values, this digital-to-analog converter is by definition perfectly linear.

The operation of the pipeline converter can be viewed from different angles. A pipeline converter can be seen as the extreme form of subranging with 1 bit per subrange.

From another point of view, the track-and-hold circuit stores the intermediate value of the signal. A comparator determines whether the input is higher or lower than the reference. The comparator decision leads to a subtraction or addition of the reference value. The result is multiplied with a factor 2 and passed to the next stage. For the ith stage,

$$V_{\text{out},i} = 2 \times V_{\text{in},i} - D_i V_{\text{ref}}, \tag{8.25}$$

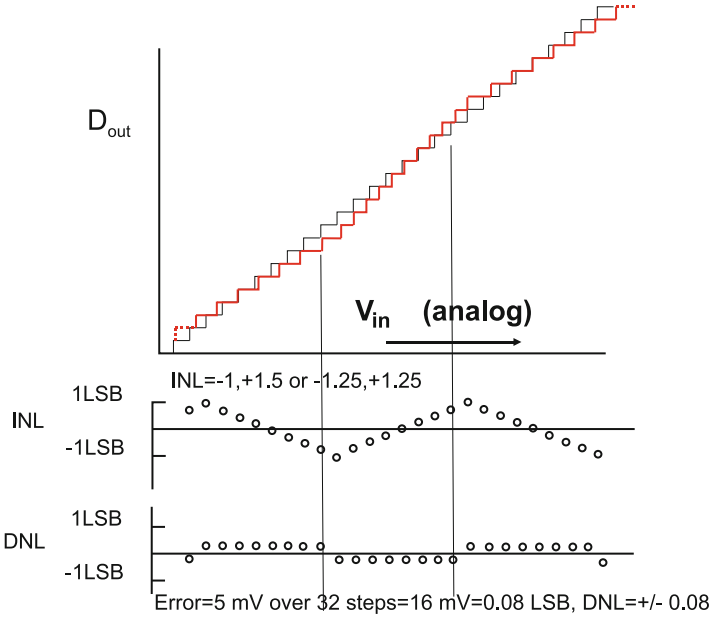


Fig. 8.52 Transfer curve, INL, and DNL for a 3-bit fine section in a two-step analog-to-digital converter. Monkey switching reduces the DNL errors

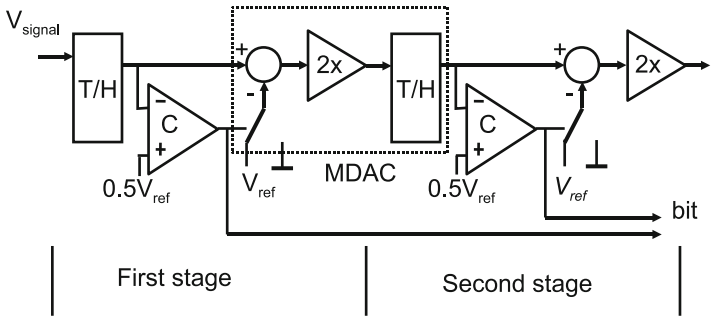


Fig. 8.53 Basic pipe-line analog-to-digital converter

where $D_i = 0, 1$ is the decision bit. This is essentially the kernel of the successive approximation algorithm from Fig. 8.70. The pipeline converter can therefore also be understood as a successive approximation converter, where every separate approximation step is implemented in dedicated hardware.

The transfer function of the input to the output of a single stage is shown in Fig. 8.54. For a stage at the input the transfer can be seen as a continuous function represented by a pair of straight lines. On the right-hand side the discrete steps in low-resolution stage are visible.

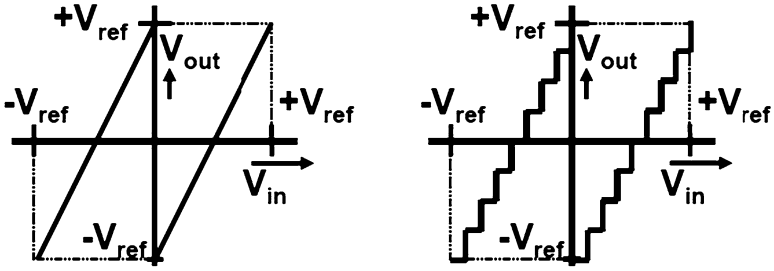


Fig. 8.54 Transfer characteristics for an MDAC in a pipe-line analog-to-digital converter. *Left*: the first stage, *right*: indicating the levels where a succeeding 3-bit flash converter would quantize. The MDAC and the flash form a four-bit converter

The choice to operate the sections at 1-bit resolution has a number of consequences. The analog-to-digital coarse converter becomes a comparator and similar to the subrange converter its inaccuracy can be overcome with redundancy as will be shown later. The digital-to-analog converter reduces in this scheme to a single-bit converter deciding between a positive and a negative level. Two levels are by definition perfectly linear, solving an important distortion problem in the digital-to-analog converter.

The pipeline stages are separated by multiply-by-two track-and-hold stages. The factor two in the stage gain implies that the output range of a section $(2V_{\text{in}} - V_{\text{ref}})$ equals the input range. Errors in the second stage will affect the input by half of their magnitude. For the third stage the errors are reduced by 4. Random errors, such as mismatch and noise (see Sect. 4.4), reduce in a root-mean-square sense. The random errors of the second stage and next stages add up as

$$v_{\text{in, random}} = \sqrt{v_{1,\text{random}}^2 + 2^{-2} v_{2,\text{random}}^2 + 2^{-4} v_{3,\text{random}}^2 + \cdots}. \tag{8.26}$$

The limited resolution reduction per stage and the low amplification per stage make that the effect of errors of many stages remains traceable at the input. Preferably a designer would like to reduce the size of the capacitor for the second-stage track-and-hold and to minimize the associated currents. However, the impact of the second stage noise does not allow drastic reductions. In many designs a similar size capacitor is used for the first three stages. For the successive stages the requirements on the gain and accuracy drop by a factor two per stage. "Stage scaling" implies reduction of the currents in these stages resulting in power-efficient designs [197].

With a conversion of 1 bit per stage, N stages are needed and N samples are simultaneously present in the converter. Additional time is needed for the digital reconstruction and error correction. Therefore the time between the first sampling of the signal and the moment the full digital value is on the output is rather long ($N + 3$ clock periods). The resulting delay, called latency, will impair the system performance if this converter is part of a feedback loop.

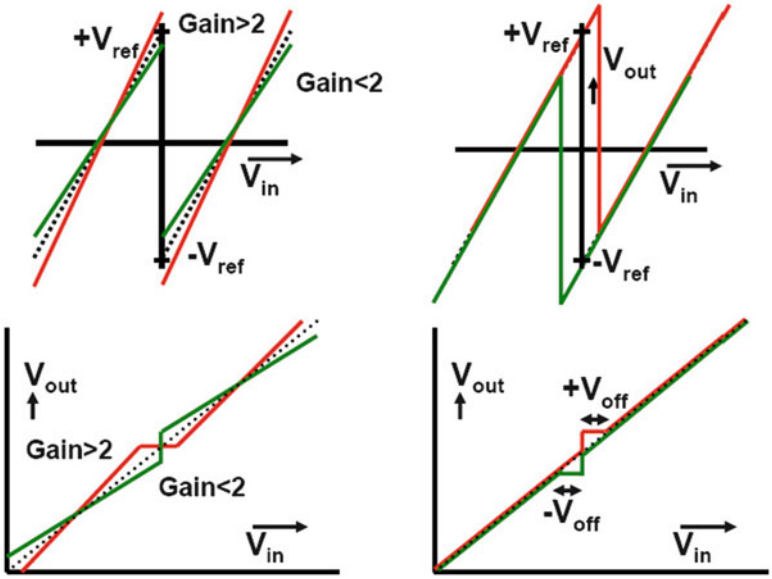


Fig. 8.55 Two errors in a pipeline stage. *Left*: the gain is not equal to 2 and *right*: the comparator suffers from a positive or negative offset. A converter with these errors in the first stage has an overall transfer characteristics as shown in the lower plots

8.4.1 Error Sources in Pipeline Converters

Two important errors in this architecture are gain errors and comparator offset (Fig. 8.55). At the moment the transfer curve exceeds V_{ref} either on the positive side or on the negative side, the signal goes out of the input range of the succeeding stage. If, on the other hand, the transfer curve does not reach the reference values, not all of the digital codes will be used. Both types of errors result in loss of decision levels or missing codes in the transfer characteristic. The comparator offset must remain under 0.5 LSB to guarantee a correct transfer curve. With some offset compensation, this value can be reached for 10–12-bit accuracies. The comparator offset problem is effectively solved in 1.5-bit pipeline converters.

The multiply-by-two operation in a pipeline converter is implemented by sampling the signal on two equal capacitors; see Fig. 8.56. In the multiply phase all charge is transferred to C_2:

$$V_{\text{out}} = \frac{C_1 + C_2}{C_2} V_{\text{in}}. \tag{8.27}$$

If $C_1 = C_2$ this operation results in an exact multiplication by two. A gain error is the result of insufficient opamp gain, capacitor mismatch, or switch charge injection; see Sect. 4.3.2. The error affects the transfer of the residue signal and must remain

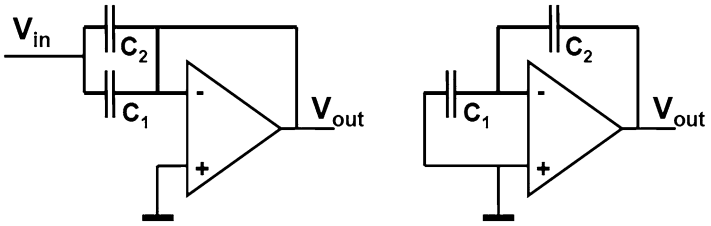


Fig. 8.56 The multiply-by-two operation in a pipeline converter is implemented by sampling the signal on two equal capacitors (*left*). In the multiply phase (*right*), all charge is transferred to C_2 [149]

within a fraction (0.1–0.2) of an LSB. The opamp DC error after settling is given by feedback theory and must be smaller than the overall required accuracy:

$$\varepsilon_{\text{DCgain}} = \frac{1}{A_0 C_2/(C_1+C_2)} \ll 2^{-N+i} \quad \rightarrow \quad A_0 > 2^{N-(i-1)} \tag{8.28}$$

with resolution N and the feedback ratio is assumed to be equal to 2. For stages further on in the pipeline the demands are less critical. The stage number $i = 1,2,\ldots,N$ illustrates the option for stage scaling. The amplification of the first stage is the highest. The amplification requirement holds for the entire output range, so any saturation effects in the output range will cause loss of accuracy. Alternative ways to reduce the gain are based on reduction of the output swing in Fig. 4.24 [102] and multiple gain steps [198].

Errors in the capacitor ratio can be the result of technological problems or deviations caused by the layout environment. A deviation in gain creates either missing range on the analog side or missing codes on the digital side. The overall DC accuracy requirement is translated in a minimum mismatch error for the capacitor ratio of

$$\varepsilon_{\text{cap}} = \frac{C_1 - C_2}{C_1 + C_2} \ll 2^{-N+i}. \tag{8.29}$$

The limited settling speed of the operational amplifiers determines the speed of the pipeline converter. Limited settling will cause errors comparable to static gain errors. The time constant corresponding to the unity-gain bandwidth of the operational amplifier $\tau_{\text{UGBW}} = 1/2\pi f_{\text{UGBW}}$ and the available time $T_{\text{settle}} = \alpha T_s$ define the settling error:

$$\varepsilon_{\text{settle}} = \mathrm{e}^{-2\pi f_{\text{UGBW}} T_{\text{settle}}} \ll 2^{-N+1} \quad \rightarrow \quad f_{\text{UGBW}} > \frac{f_s(N-i)}{2\pi\alpha} \tag{8.30}$$

$\alpha < 0.5$ is the fraction of the clock period T_s that is allocated to the settling process. If the converter is operated in a simple mode where the comparator is active in one clock phase and the settling takes place in the other clock phase, α must be set according to the minimum duty cycle of the clock. The UGBW of the operational

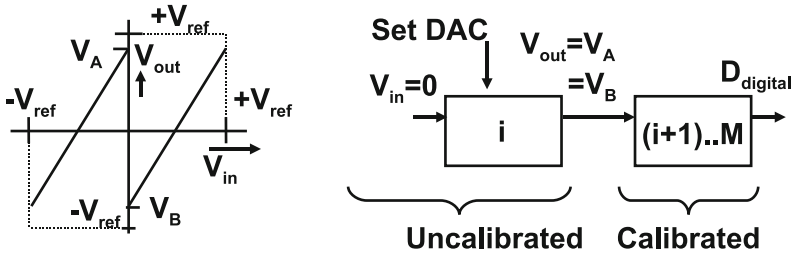


Fig. 8.57 The gain in the stage is deliberately made smaller than 2. The converter is calibrated starting at its back end and working toward the front-end [200]

amplifier will have to be high requiring a lot of power. If a more complex timing circuit is used, the settling time for the operational amplifier and the time needed for the comparator can be better controlled allowing more time for the settling and saving of some power.

The above-mentioned error sources must not exceed a total of $0.5V_{\mathrm{LSB}}$. The balance between the error sources depends on the required specifications and available technology: high accuracy requires high gain and low mismatch. High speed requires simple transconductance stages. A first estimate of the error allocation over the stages of the converter is according to the relative weight: 1/2, 1/4, 1/8, etc.

Next to minimizing the capacitor mismatch in a technological manner, several schemes try to mitigate this error in an algorithmic way. Li [199] proposed the ratio-independent technique. A signal is sampled in a capacitor and in a second cycle stored in an intermediate capacitor. In a third cycle, the first capacitor takes another sample, and in a fourth cycle the first sample is retrieved and added to the second sample.

Song [100] presented a scheme where the multiply-by-two is executed in two phases: in the first phase the capacitors are arranged as shown in Fig. 8.56 and, in the second phase C_1 and C_2 are interchanged. The results of both are averaged yielding a reduced effect of the capacitor mismatch. Unfortunately these schemes cost hardware and several clock cycles.

8.4.2 Reduced Radix Converters with Digital Calibration

In order to circumvent the accuracy problems Karanicolas [200] proposed to use a gain factor which is deliberately smaller than 2. The gain factor is chosen to avoid range excess either by offset or gain errors; see Fig. 8.57. With less than 1-bit resolution per stage, more stages M are needed than the resolution N. This is in fact a conversion with a radix or base less than 2.

In order to reconstruct the input from a given output value the following equations are used:

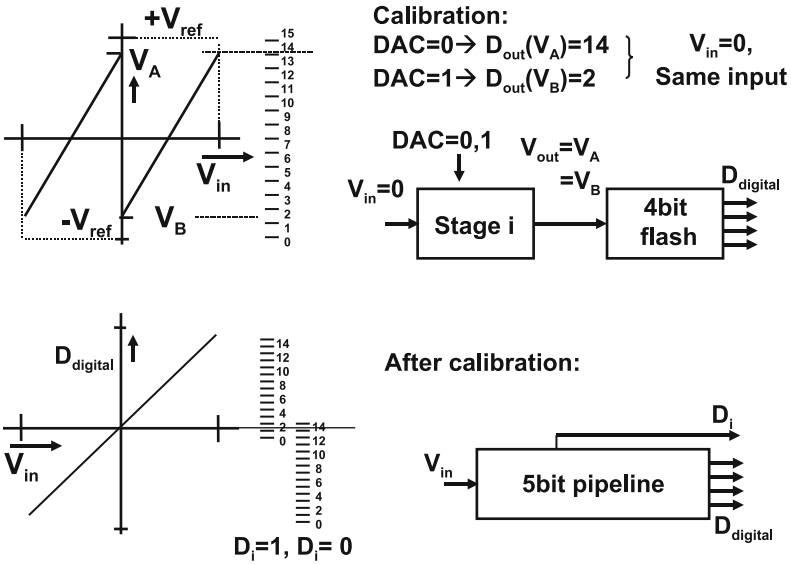


Fig. 8.58 Example of pipeline calibration

$$V_{\text{in}} < 0, \rightarrow V_{\text{in}} = V_{\text{out}} - V_A$$
$$V_{\text{in}} > 0, \rightarrow V_{\text{in}} = V_{\text{out}} - V_B. \tag{8.31}$$

The reconstruction requires that the intersection points with the vertical axis V_A and V_B are known. During the digital calibration cycle the values of V_A and V_B are measured as digital codes with the help of the calibrated part of the converter itself. In calibration mode the input of section i is grounded and the digital-to-analog converter is set to $+V_{\text{ref}}$. The output will be equal to the value V_A. Similarly V_B is obtained with the digital-to-analog converter set to $-V_{\text{ref}}$. The digital values of the intersection points correspond to a fraction of the reference voltage. Calibrating stage i requires that stages $i+1,\ldots,M$ have been measured before.

Figure 8.58 gives an example of the calibration. Before the pipeline converter is used, the calibration cycle has to determine the digital values for V_A and V_B. In this example the last converter stage is a 4-bit full-flash converter and V_A and V_B are measured as digital values of 14 and 2. In fact these two codes correspond to one and the same input voltage (in this example $V_{\text{in}} = 0$). Therefore the conversion curves corresponding to DAC $= 0$ and DAC $= 1$ can be aligned on these points. The resulting converter is close to a 5-bit range with 29 codes.

The local reference and the quality of the first subtraction or addition must still achieve the accuracy level of the converter. The reconstruction of signal samples is now a simple addition of the digital codes weighted with the decision of the comparator in each section. This calibration relaxes the accuracy requirements on the overall gain. Also comparator offset is not critical, as long as V_A and V_B stay within the reference range.

8.5 1.5 Bit Pipeline Analog-to-Digital Converter

The straight-forward pipeline converter of Fig. 8.53 requires full and accurate settling in all stages. Digital correction is possible when the gain factor is reduced.

The 1.5-bit pipeline converter allows a more extensive error correction as in each stage two comparators are used; see Fig. 8.59. The trip levels of these comparators are typically located at 3/8 and 5/8 of a single-sided reference or at $\pm 1/4$ of a differential reference; see Fig. 8.60 [98, 201–205]. These decision levels split the range in three more or less equivalent pieces, thereby optimally using the dynamic range of the circuit. In case of a double positive decision of both comparators the digital-to-analog converter will set the switches to subtract a reference value. In case of two negative decisions the digital-to-analog converter will add a reference value and in case of a positive and a negative decision, the signal will be passed on to the amplifier. Every stage therefore is said to generate 1.5 bits:

$$V_{\text{out}} = 2V_{\text{in}} + \begin{pmatrix} +V_{\text{ref}} \\ 0 \\ -V_{\text{ref}} \end{pmatrix}. \tag{8.32}$$

The digital-to-analog converter uses three levels. In a fully differential design these levels can be made without loss of accuracy: zero, plus, and minus the reference voltage. The last two levels are generated by straight-forward passing the reference voltage or twisting the connections.

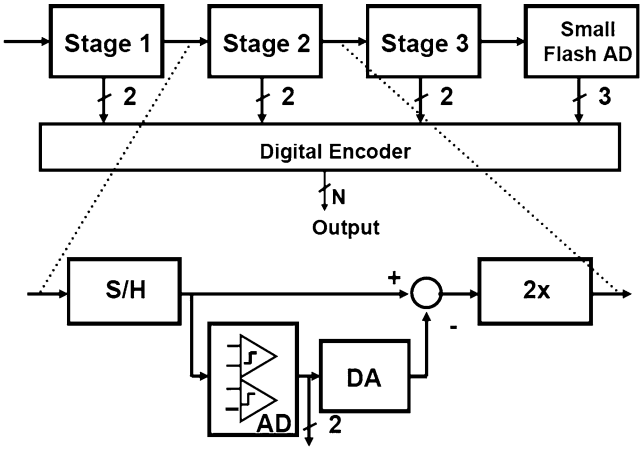


Fig. 8.59 The architecture of a 1.5-bit pipeline analog-to-digital converter is derived from the coarse-fine architecture

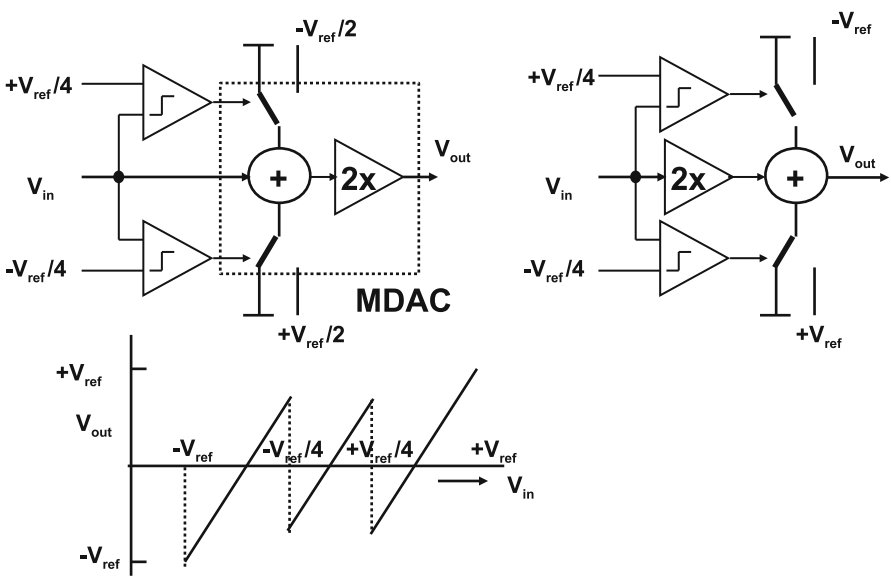


Fig. 8.60 Basic operation of a 1.5-bit pipe-line analog-to-digital converter. The section in the *dotted box* is called a multiplying digital-to-analog converter (MDAC)

The typical transfer curve from Fig. 8.60 shows that negative signals are shifted upwards and positive signals are shifted downwards in the plot with respect to the values around zero.

The section consisting of the subtraction of the reference and the multiplication is called a multiplying digital-to-analog converter (MDAC).

8.5.1 Design of an MDAC Stage

Like in most CMOS analog-to-digital principles also 1.5-bit pipeline converters need good capacitors, high-performance operational amplifiers, and low-leakage CMOS switches to implement high-quality track-and-hold stages and to create a pipeline of N stages. The first choice that has to be made is the signal swing. Operating the converter in differential mode is preferred as it doubles the amplitude with respect to a single-sided approach. Moreover it minimizes even order distortion, power supply, and substrate noise influence. However, analog-to-digital converters that take their input directly from external sources will normally see a single-sided signal. Also many RF and filter circuits before a converter are designed single-sided to allow optimum and/or minimum use of components. In both cases it is desirable to have an as large as possible input signal swing.

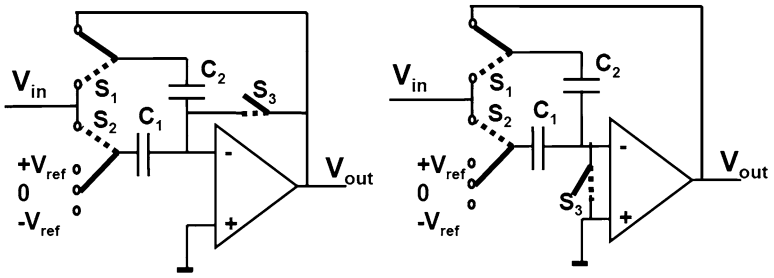


Fig. 8.61 A track-and-hold with multiply-and-subtract stage (MDAC) used in 1.5-bit pipeline converters. Two alternative schemes are shown for creating a ground node in pipeline converters. In the hold phase the switches in the drawn positions; for the track phase the switches are in the dotted positions

A popular implementation is shown in Fig. 8.61(left). This MDAC configuration allows a large-signal swing without any repercussion for the input of the operational amplifier. Its inputs remain at virtual ground level thereby avoiding common-mode problems (such as in telescopic amplifiers; see Sect. 2.7.10). During the track phase in Fig. 8.61(left), the switch S_3 puts the operational amplifier in unity-gain feedback. The capacitors C_1 and C_2 are connected in parallel to the input signal. When the transition to the hold-phase occurs, switch S_1 creates via C_2 the feedback path for the amplifier. S_2 switches capacitor C_1 to one of three reference voltages, depending on the result of the two comparators. The original charge corresponding to the input signal on C_1 is transferred to C_2. In addition a charge packet corresponding to the chosen reference voltage is moved into C_1 and out of C_2. The overall transfer of this circuit is

$$V_{\text{out}} = \frac{(C_1 + C_2)}{C_2} V_{\text{in}} \begin{pmatrix} + \\ 0 \\ - \end{pmatrix} \frac{C_1}{C_2} V_{\text{ref}}. \tag{8.33}$$

Both signal and reference are multiplied by two. This principle has a lot of similarity with algorithmic analog-to-digital converters; see Sect. 8.6.2.

The required capacitor accuracy is given by Eq. 8.29. Plate or fringe capacitors normally allow to reach 12–14-bit capacitor matching. Moreover, the size of the capacitors is in this range more determined by the noise requirements. High-resolution converters require the track-and-hold capacitor to fulfill the kT/C noise limit. The input-referred noise of the opamp must be added and during the switching another kT/C addition occurs. Depending on the required specifications and the design of the opamp a design guideline is to use an excess factor of $E_{\text{noise}} \approx 3$:

$$\frac{E_{\text{noise}} kT}{C_1} < \frac{V_{\text{LSB}}^2}{12} = \frac{V_{\text{pp}}^2 2^{-2N}}{12}, \tag{8.34}$$

where V_{pp} represents the peak–peak value of the input signal.

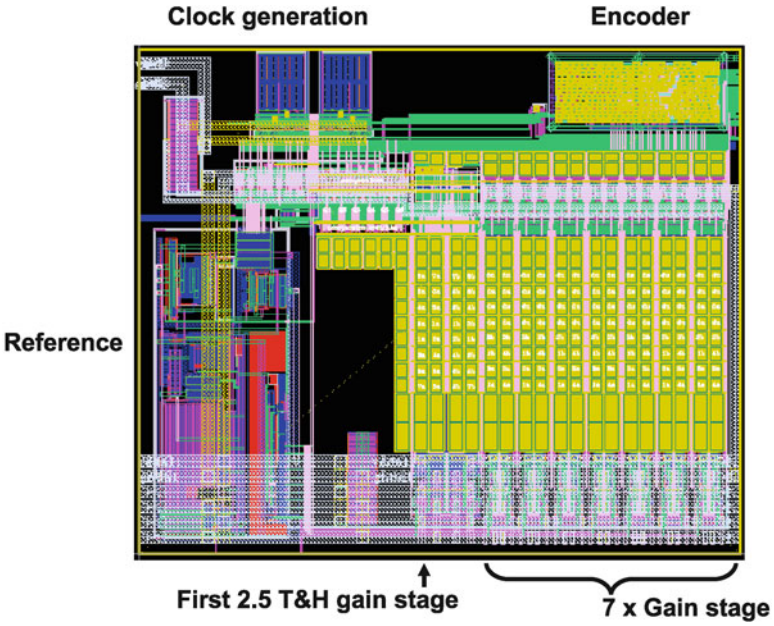


Fig. 8.62 A 10-bit pipeline layout. The first stage contains 2.5 bits and the seven remaining stages 1.5 bits. The depicted area in 90 nm CMOS is $500 \times 600\,\mu m^2$ (courtesy: Govert Geelen NXP [206])

The capacitor choice is a determining factor in the design. The total noise accumulates as in Eq. 8.26 and Fig. 4.21. However, the capacitor value also determines the current setting of the buffer and thereby most of the analog-to-digital converters power.

When all stages resolve 1.5 bits, the contribution of the second and third stages is still significant. Often the same capacitor value for these stages is used and scaling is applied after the third stage. Lower capacitive load means lower currents, and power saving is obvious [197]. The alternative is to use more levels in the first stage, e.g., 6 [206] or 7 [99].

Figure 8.62 shows the layout of a 10-bit pipeline converter. Most of the area is used by the capacitors.

With a large swing of the input signal ($2\ V_{pp}$) the capacitors can remain relatively small, causing less problems with area, power, etc. The input switches can either be complementary or bootstrapped (see Sect. 4.3.4) and are of minimum length. A potential issue is formed by the bond pad that is connected to the input terminals. Its protection measures must be examined as too much parasitic capacitance will affect the performance. Special RF bond pads are an alternative.

The amplification stage has to fulfill similar demands as in the 1-bit pipeline converter. The topology of the opamp depends on the specifications. Low accuracy and high speed will push toward simple transconductance stages, while high accuracy may involve (folded) cascode amplifiers. The DC gain is set by the overall resolution

Table 8.4 Comparison of 8- and 12-bit 1.5-bit pipeline stages

Parameter	Equation	$N = 8$ bits	$N = 12$ bits
Sample rate	f_s	100 Ms/s	20 Ms/s
LSB size	$V_{\text{LSB}} = 2^{-N} V_{\text{pp}}$	3.9 mV	0.24 mV
Sampling cap	8.34: $E_{\text{noise}} kT/C_1 < V_{\text{LSB}}^2/12$	9.5 fF	2.4 pF
Capacitor matching	8.29: $(C_1 - C_2)/(C_1 + C_2) \ll 2^{-N}$	10^{-3}	10^{-4}
Opamp gain	8.28: $A_0 > 2^N$	256	4096
UGBW ($\alpha = 0.5$)	8.30: $f_{\text{UGBW}} > f_s N/2\pi\alpha$	270 MHz	80 MHz
Slew current	8.35: $I_{\text{slew}} > C_{\text{load}}(\text{d}V/\text{d}t)$	4 µA	400 µA

Inspired by ISSCC workshops

in Eq. 8.28 and the settling in Eq. 8.30. The implementation of the opamp starts with the current. The current must be able to generate sufficient transconductance to reach the UGBW of Eq. 8.30. Moreover the slew-rate requirements must be met:

$$I_{\text{bias}} > I_{\text{slew}} = C_{\text{load}} \frac{\text{d}V}{\text{d}t}, \tag{8.35}$$

where the load capacitance C_{load} includes the feedback and parasitic capacitances as well as the input capacitance of the next stage. A safe measure for the voltage slope is $V_{\text{max,swing}}/\tau_{\text{UGBW}}$. The first stage is most demanding, and the next stages can be designed with relaxed specifications, following the stage-scaling principle.

In this example of Fig. 8.61(left) switch S_3 sets the opamp in unity-gain mode in order to create a virtual ground during track mode. The consequence of this choice is that the opamp and the switches operate as described for auto-zeroing comparators in Sect. 8.1.7 with an increased noise level due to the sampling of the input-referred noise of the opamp. The switch S_3 can be moved to a position where it shorts the input terminals of the amplifier Fig. 8.61(right); see, e.g., [206]. The real ground node for the sampling process removes the input-referred opamp noise. This configuration trades off the offset cancellation of the scheme in Fig. 8.61(left) for reduced noise performance in Fig. 8.61(right).

Example 8.8. Determine the parameters for the first section of a pipeline stage for 8-bit resolution at 100 Ms/s and 12-bit resolution at 20 Ms/s, with a 1 V input range.

Solution. Table 8.4 lists the main parameters. Of course fine-tuning with a simulation is needed to incorporate the parasitic effects.

8.5.2 Redundancy

Figure 8.63 shows the redundancy mechanism of a 1.5-bit scheme. The upper curve shows seven stages and the voltage levels in between. An input voltage equal to

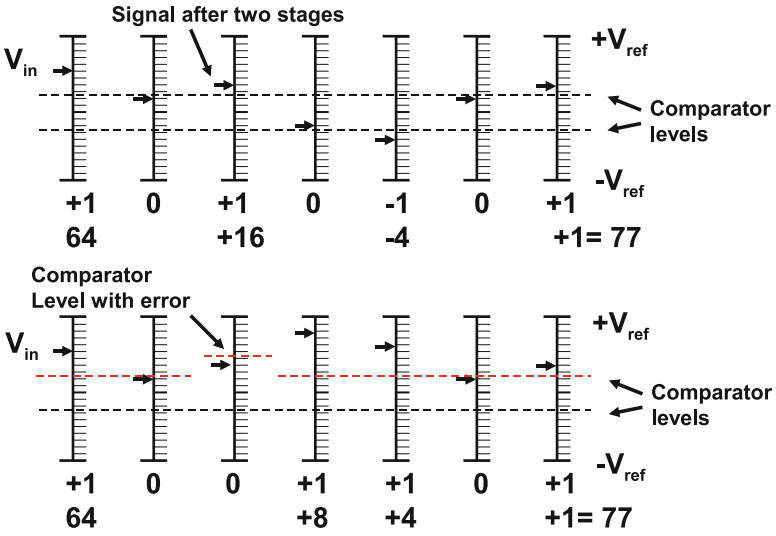


Fig. 8.63 1.5-bit pipeline analog-to-digital converter uses the redundancy of two decisions per stage. The *upper sequence* shows the ideal behavior. In the *lower sequence* one comparator level is shifted, e.g., due to offset. The redundancy corrects the mistaken decisions

$V_{\text{in}} = 0.6V_{\text{ref}}$ clearly exceeds the upper comparator threshold at $0.25V_{\text{ref}}$. Therefore the first coefficient is determined to be $a_{N-1} = 1$. The residue is formed as $2 \times V_{\text{in}} - V_{\text{ref}} = 0.2V_{\text{ref}}$. This value generates in the second stage a $a_{N-1} = 0$ decision. In the following stages the rest of the conversion takes place. The result "77" equals $77/128 = 0.602V_{\text{ref}}$.

In the lower trace of Fig. 8.63 the comparator level of the third section is moved to $0.45V_{\text{ref}}$. It is easy to see how the redundancy scheme corrects for this error. See also the remarks for the RSD converter in Fig. 8.79. The redundancy eliminates the need for accurate comparators but leaves full accuracy requirements on the switched-capacitor processing stages.

Figure 8.64 shows the layout of a 16-bit pipeline converter.

8.5.3 Pipeline Variants

Judging from the number of published papers, the pipeline converter is the most popular analog-to-digital converter. Most effort is spent on converters in the range of 10–14 bits of resolution and 50–500 Ms/s sampling rates. These high-performance converters aim at the same markets as high-end subranging converters. Similar to the high-performance subranging converters the main problems are found in the design of the first track-and-hold circuit, constant switch resistance, the settling behavior of the opamp, and parasitics. In order to avoid too many stages contributing to the

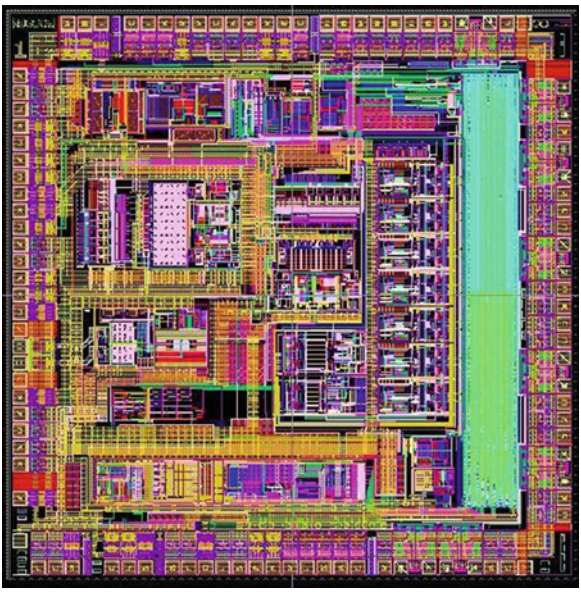


Fig. 8.64 Lay-out of a 16-bit 125 Ms/s pipeline analog-to-digital converter ENOB = 11.6 (courtesy Ph. Gandy, NXP Caen)

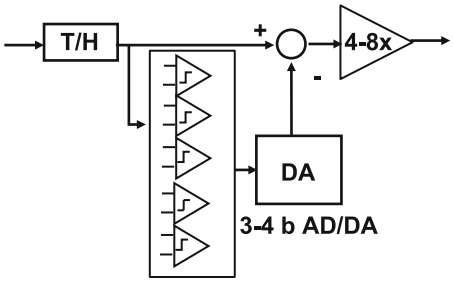


Fig. 8.65 Advanced pipeline concepts use a multi-bit input stage

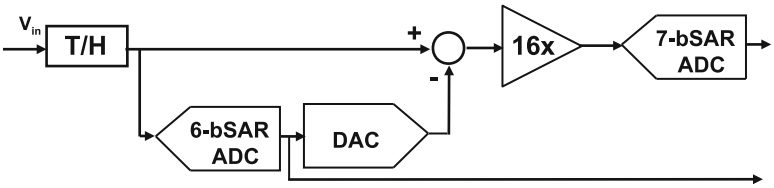


Fig. 8.66 A 6-bit successive approximation analog-to-digital converter strongly reduces the input range [210]

noise and distortion budget, most of these converters use input stages with 2.5–4-bit resolution (Fig. 8.65) [207–209]. The analysis in [202] indicates that this is an optimum range.

A radical variant is proposed in Fig. 8.66 [210]. The input quantizer is a 6-bit successive approximation analog-to-digital converter that reduces the input

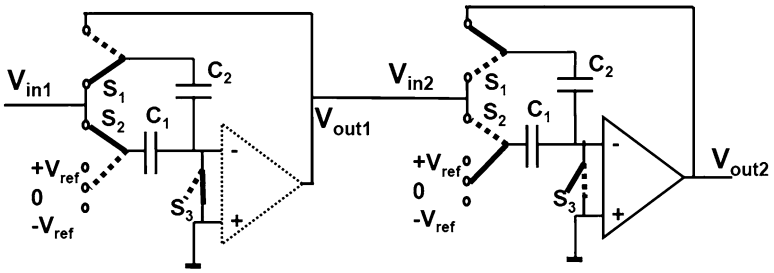


Fig. 8.67 The opamp is shared between two stages in a 1.5-bit pipeline converter. The *left stage* is sampling, and the *right stage* is amplifying. During the next half phase the opamp is moved to the first stage which amplifies, while the second stage samples without an opamp. The switches for reconnecting the opamp have been left out for clarity

range significantly. The linearity requirements of the summation and multiply operation are easier met at the cost of the loss of timing for the successive approximation operation. Compare [211].

Power efficiency is a driving force in 1.5-bit pipeline converters. One possibility to improve power efficiency is found in a better use of the hardware. A feature of the configuration in Fig. 8.61(right) is the fact that during sampling the opamp is redundant. Opamp sharing is a technique that effectively uses the opamp redundancy in the scheme of Fig. 8.67. The opamp now serves two sections of the pipeline converter and reduces the required number of opamps by a factor two [201, 212]. During the sampling the input capacitor C_1 and the feedback capacitor C_2 do not need the opamp as long as a separate ground switch S_3 is present. The opamp can be used for the second stage, where the subtraction and multiplication by a factor two takes place. The odd and even sections now run half a sample phase delayed and one opamp can serve two sections. The opamp can show a "memory effect" due to signal charges stored in the internal capacitors. This interference between one sample and the next is undesired. A fraction of the clock period or special switching schemes are used to avoid coupling between the samples.

The pipeline converter uses digital calibration techniques to overcome analog imperfections. Many authors propose to extend these calibration techniques to eliminate the energy consuming opamps. Mehr and Singer [213] propose to remove the dedicated front-end track-and-hold function. The pipeline stage as in Fig. 8.61 samples directly the time continuous input and performs the first processing. The timing mismatch between this stage and the first set of comparators must be solved.

Replacing the opamps with less performing building blocks or allowing incomplete settling [204, 205] requires more extensive calibration. Sensitivity to changing environmental conditions (power supply, bias, temperature) is unclear.

A radical idea to avoid the opamp in the processing of a pipeline converter is proposed in [214, 215]. A comparator switches on and off two current sources in

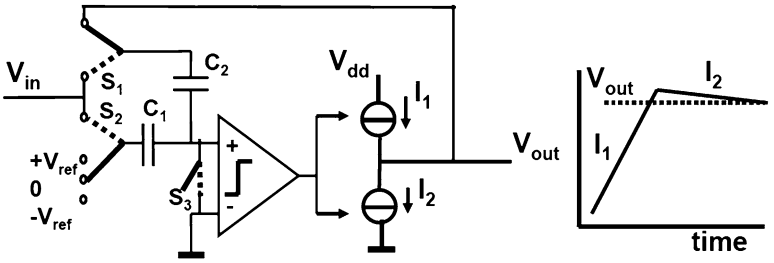


Fig. 8.68 The opamp is removed and replaced by a comparator and two current sources

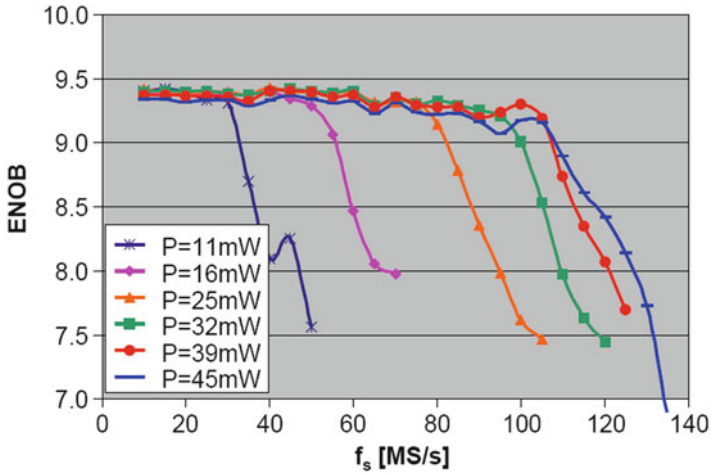


Fig. 8.69 Measured effective number of bits versus sample rate at different power levels. The signal frequency is each time just below $f_s/2$ (courtesy: Govert Geelen NXP [206])

Fig. 8.68. I_1 is used for fast charging; however, some overshoot must be expected due to the delay between the crossing of the levels at the input of the comparator and the current switching. A second current source I_2 discharges at a slower rate and reaches the required output level.

Power efficiency is crucial for the application of converters in large system chips. Next to optimizing the power consumption of the individual blocks and techniques such as opamp sharing, also converters are published with adjustable power and performance specifications; see Fig. 8.69 [206]. Another approach to calibrate the errors in a fast pipeline converter is in combination with a slow high-precision analog-to-digital converter. Synchronization of both converters is achieved by a track-and-hold circuit or post-processing [216].

8.6 Successive Approximation Converters

Where a full-flash converter needs a single clock edge and a linear converter 2^N clock cycles for a linear approximation of the signal, the successive approximation converter (SAR stands for successive approximation register) will convert the signal in N cycles. Figure 8.70 shows an abstract flow diagram of a successive approximation algorithm. The output bits a_{N-1} to a_0 are set to 0. In the first cycle the coefficient corresponding to the highest power a_{N-1} is set to 1 and the digital word is converted to a value V_{DAC}. The input level is compared to this value and depending on the result the bit a_{N-1} is kept or set back to 0. This cycle is repeated for all required bits.

Figure 8.71 shows a circuit implementation. After the signal is stored in the sample-and-hold circuit the conversion cycle starts. In the register the MSB is set to 1 and the remaining bits to 0. The digital-to-analog converter will generate a value representing half of the reference voltage. Now the comparator determines whether the held signal value is over or under the output value of the digital-to-analog converter and keeps or resets the MSB. In the same fashion the next bits in the output register are determined. The internal clock runs much faster than the sample clock, for every sample a sample-and-hold cycle and N clock cycles are needed. In this scheme the digital-to-analog output value approximates the input value. Another implementation reduces the input value by subsequent subtraction.

The approximation algorithm in Figs. 8.71 and 8.72(left) requires that the comparator operates over the entire input range to full specification. The reverse and complementary forms Fig. 8.72(middle and left) either decrease the signal value to a zero level or complement to reach the full reference. The comparator has a much

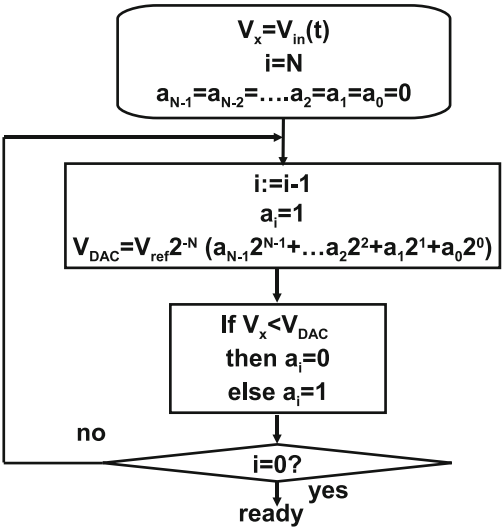


Fig. 8.70 A flow diagram for successive approximation

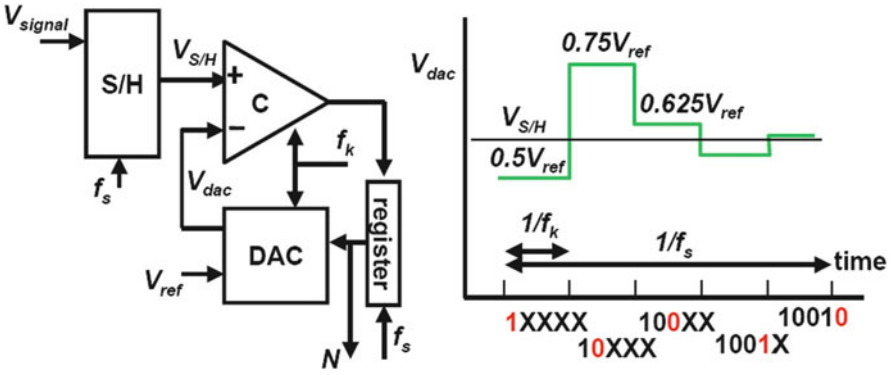


Fig. 8.71 A successive approximation analog-to-digital converter with approximation sequence

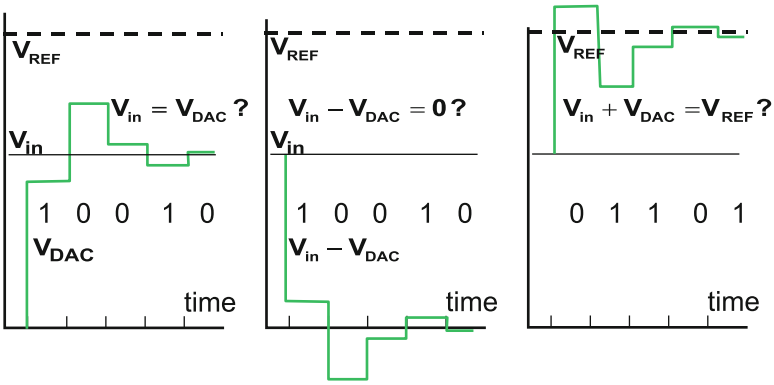


Fig. 8.72 Three forms of successive approximation analog-to-digital converter algorithms: normal, reverse, and complementary

easier task. As can be seen from the example, the processed signal can reach beyond the reference range. In low-power supply circuits this may lead to leakage through forward-biased pn-junctions.

Offsets in the sample-and-hold circuit or the comparator will generate a shift of the conversion range, but this shift is identical for every code. This principle allows sample rates of tens of megahertz. The demands on the various constituent parts of this converter are limited. Main problem is a good sample-and-hold circuit that needs a good distortion specification for relatively low sample periods. Next to the sample-and-hold, the digital-to-analog converter determines the overall linearity and will take up most of the area. The conversion speed is determined by the settling of the digital-to-analog converter. Especially in larger structures with a lot of elements this settling time constant τ_{DAC} can be rather long. For reaching half-an-LSB accuracy in an N-bit converter the settling time requirement is

$$t_{\mathrm{settle}} > \tau_{\mathrm{DAC}} \ln(2^{N+1}). \tag{8.36}$$

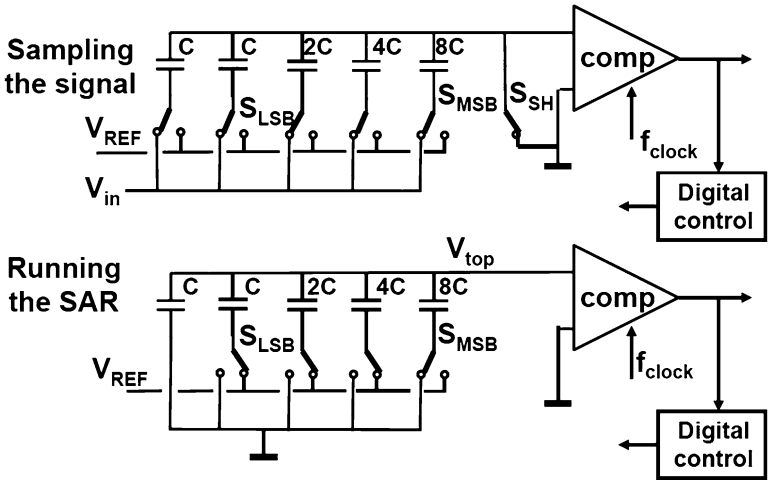


Fig. 8.73 An early implementation of a successive approximation analog-to-digital converter is based on capacitor switching, after [217]

For many applications that do not need the maximum conversion speed that is possible in a technology, successive approximation is a safe and robust conversion principle. In applications with a built-in sample-and-hold function (e.g., a sensor output) the combination with a successive approximation converter is appropriate. In combination with a microcontroller, the register function and the timing can be controlled with software. However, special attention must be paid to processor interrupts that can easily disturb the conversion process.

8.6.1 Charge-Redistribution Conversion

One of the early fully integrated CMOS successive approximation analog-to-digital converters is known as "charge-redistribution" converters [217, 218]. The principle is shown in Fig. 8.73 and utilizes optimally the properties of CMOS technology: good switches and capacitors. In the sampling phase the input signal is stored on a capacitor bank with a total capacitance value of $16C$. "C" is the unit capacitor and is laid-out in a standardized manner. In the second phase the ground plates of the capacitors are switched one after the other from ground to the reference voltage. If the MSB switch is toggled the top-plate voltage changes from ground to

$$V_{\text{top}} = -V_{\text{in}} + \frac{8C}{C+C+2C+4C+8C} V_{\text{ref}}. \tag{8.37}$$

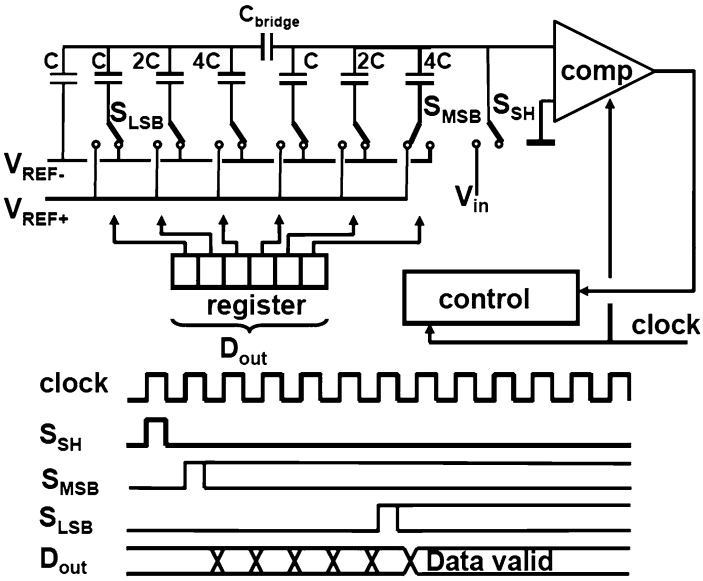


Fig. 8.74 A successive approximation analog-to-digital converter based on capacitor switching [219, 220]

Depending on the original value of the input voltage, the comparator will decide to keep the MSB switch in this position or return to ground. Every bit is subsequently tested. In this implementation the result is a digital code and an output voltage of the digital-to-analog converter that approximates the original input signal.

In another implementation the sampling is performed on the upper plates of the capacitors and the algorithm will converge to the digital code that complements the input voltage to full scale.

Figure 8.74 shows a second example of a successive approximation analog-to-digital converter in standard CMOS technology. The digital-to-analog converter is implemented as a bridged capacitor array; see Fig. 7.25. An important difference is that the summation node is not a virtual ground node as it is in the digital-to-analog converter. The voltage swing on the input node of the comparator depends on a correct charge sharing between the capacitors connected. The bridging capacitor and the left hand in series capacitors must sum up to a unit capacitor, so

$$\frac{C_{\text{bridge}} 2^k C}{C_{\text{bridge}} + 2^k C} = C, \tag{8.38}$$

where k is the resolution of the left-hand side array. From this equation the bridge capacitor is found as

$$C_{\text{bridge}} = \frac{2^k}{2^k - 1} C. \tag{8.39}$$

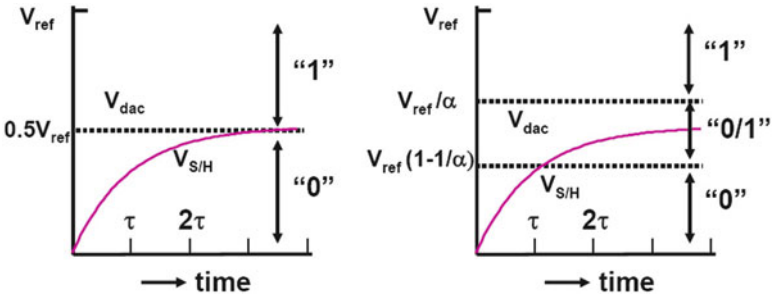


Fig. 8.75 In a base-2 successive approximation the settling of the input signal must reach the final accuracy level before the next step is taken. In non-binary search the base is smaller than 2 and an intermediate region of signal levels exists, where initial decision can be corrected

The bridging capacitor can be rounded to unity if k is large [219], thereby avoiding the need for a fraction of a capacitor with various mismatching issues.

The conversion cycle starts after the sample is loaded on the capacitors through switch S_{SH}. In this example this action also resets the structure; however, also a separate reset clock cycle and switches can be used. The reference voltages are chosen with equal but opposite voltages with respect to the signal ground level. The purpose of this successive approximation is to make the signal on the input of the comparator equal to the ground level. To achieve that goal in this implementation the MSB-switch in the sampling phase is connected to the plus reference, while the other switches are connected to the negative reference. After the sampling the MSB can be tested and then sequentially all other bits.

These successive approximation converters use a limited amount of hardware and good energy efficiencies have been reported [219–221].

Successive approximation converters can be easily equipped with forms of redundancy. In a successive approximation with a base of 2, the first decision is the final decision on the MSB. It is necessary to let the signal from the track-and-hold stage settle till sufficient accuracy is reached before the decision is taken; see Fig. 8.75. In [222] the base for the digital calculation is not 2 but, e.g., $\alpha = 1.85$. After the MSB decision, the range for the remaining search is not the half of the original range but a fraction $1/\alpha$. This decision range for a "0" (see the right side of Fig. 8.75) extends over the "1" decision level and therefore allows an intermediate range where the initial decision can be corrected. Of course some more clock cycles are needed for this redundancy; however, as the signal needs far less settling time the frequency can be a factor 2–3 higher. This type of search is also called: "non-binary" search (compare Sect. 8.4.2). An extension to this nonbinary work is, e.g., found in [223].

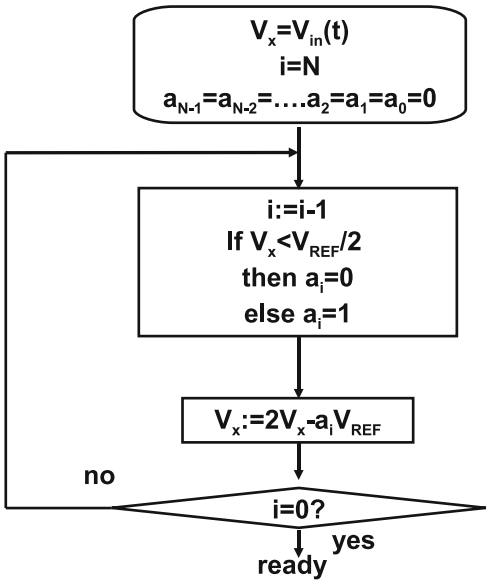


Fig. 8.76 A flow diagram for a cyclic converter

8.6.2 Algorithmic Converters

In the previous examples of successive approximation converters the searching process is implemented by comparing the input value to a set of values from the digital-to-analog converter. Next to the design of the sample-and-hold, the accuracy and the area are determined by the digital-to-analog converter. Algorithmic or "cyclic" analog-to-digital converters keep the reference value constant and avoid a large digital-to-analog structure. By capacitive manipulation the signal is modified [196, 224].

A flow diagram of a basic algorithm is shown in Fig. 8.76. The value V_x is set to the input value and compared to half of the reference. If V_x exceeds half of the reference, this value is subtracted. The remainder is multiplied by 2 and treated as the new input value of the process. This multiplication is an advantage over the elementary successive approximation algorithm. Now errors in the smaller bits count less. Obviously the result of N executions of this flow diagram is

$$V_x = 2^N V_{\text{in}}(t) - V_{\text{ref}}\left(a_{N-1}2^{N-1} + \cdots + a_1 2^1 + a_0 2^0\right). \tag{8.40}$$

If the remainder V_x is set to zero (ideally it should be less than an LSB), V_{in} will equal a binary-weighted fraction of the reference voltage. The critical factors in this algorithmic converter are the offsets and the accuracy of the multiplication by 2. The total multiplication error must remain within one LSB. If the amplification equals $(2+\varepsilon)$ the difference between the value at the MSB transition and the (MSB-1LSB) transition (the DNL at that code) equals

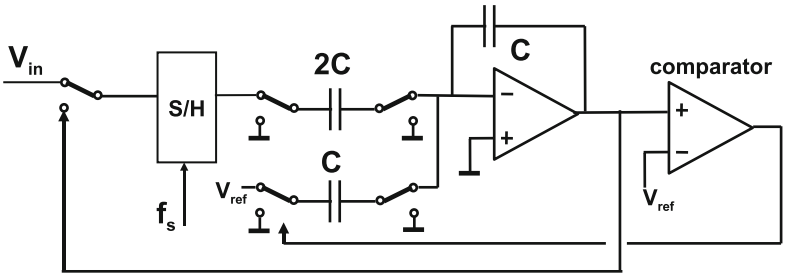


Fig. 8.77 An example of a cyclic analog-to-digital converter, after [199]

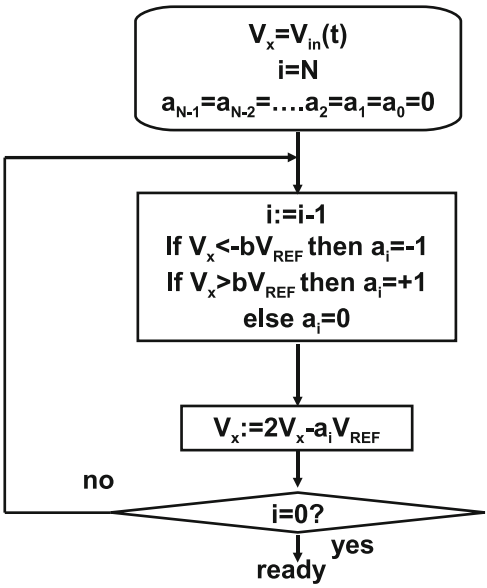
$$D = (2+\varepsilon)^{N-1} - [(2+\varepsilon)^{N-2} + (2+\varepsilon)^{N-3} + \cdots + (2+\varepsilon)^{1} + (2+\varepsilon)^{0}]$$
$$= (2+\varepsilon)^{N-1} - \frac{1-(2+\varepsilon)^{N-1}}{1-(2+\varepsilon)} = \frac{1-\varepsilon(2+\varepsilon)^{N-1}}{1-\varepsilon} \approx 1-\varepsilon 2^{N-1}[\text{ in LSB}]. \tag{8.41}$$

The error in the multiplication factor is itself multiplied by the term 2^{N-1}. In order to keep the DNL sufficiently low, $\varepsilon < 2^{-N}$.

Figure 8.77 shows a basic circuit topology of the converter. After the sample-and-hold circuit has acquired a sample and all capacitors have been discharged, the signal is multiplied by two and compared with the reference voltage to generate the MSB bit. Based on this bit zero or the reference voltage is subtracted from the signal. This remainder signal is fed back to the sample and hold for the next run.

Offsets are critical. The comparator offset must remain under an LSB. In switched-capacitor technique the offsets at the inputs of opamps and comparators can be removed. The remaining problem is the required accuracy of the multiplication by 2. The minimum capacitor value is mostly determined by the accumulated noise. And the minimum gain of the operational amplifiers is given as in Eq. 8.28. The implicit mismatch of the capacitor structure may jeopardize accuracy. However, a careful layout, where the capacitor "2C" is built from two parallel capacitors "C" and properly surrounded by dummy structures, will reduce this error source to the 10–12-bit level. The injection of charge by the switches is especially an issue in older technologies. The channel charge in the relatively large switch transistors varies with the signal and will affect the overall gain; see Eq. 4.5. Differential operation or special switching sequences help to reduce this effect [199].

Several accuracy issues can be removed if some redundancy is built in. The flow diagram in Fig. 8.78 shows that instead of a single decision now the signal is compared to values bV_{ref} and $-bV_{\text{ref}}$, with $b \approx 0.25$. The redundancy is due to the three values that each coefficient can take: $a_i = (-1, 0, +1)$. In simple terms, the algorithm assigns only $a+1$ or -1 value to a coefficient if the signal is unambiguously positive, respectively, negative. In case of doubt, the signal is left unaltered. In Fig. 8.79 the algorithm converts a signal $V_{\text{in}} = 0.6V_{\text{ref}}$. The first decision



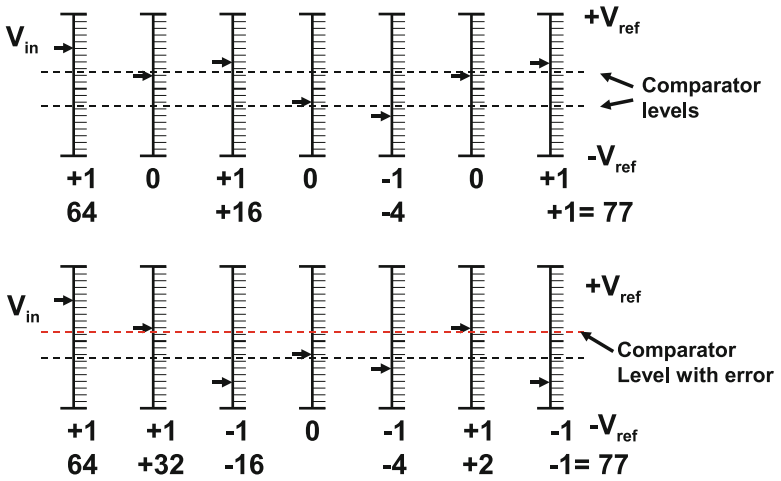


Fig. 8.78 The redundant signed digit algorithm [225]

Fig. 8.79 *Upper sequence*: an input voltage of $0.6V_{\text{ref}}$ is converted in seven cycles with comparator levels at $\pm 0.25V_{\text{ref}}$. *Lower sequence*: the positive comparator level is now at $0.15V_{\text{ref}}$, e.g., due to offset; however, with the help of redundancy is the same code is reached: $77/128 = 0.602$. Note that the exactly matching end result is partly a coincidence. The difference at the one-but-last stage is 2 LSB

is therefore $a_{n-1} = +1$, and the remainder is formed as $(2 \times 0.6 - 1)V_{\text{ref}} = 0.2V_{\text{ref}}$. This new residue value leads to a $a_{n-2} = 0$ decision and the next remainder is simply $2 \times 0.2V_{\text{ref}}$. The process repeats until after seven cycles a value of 77 is found: $77/128 = 0.602$.

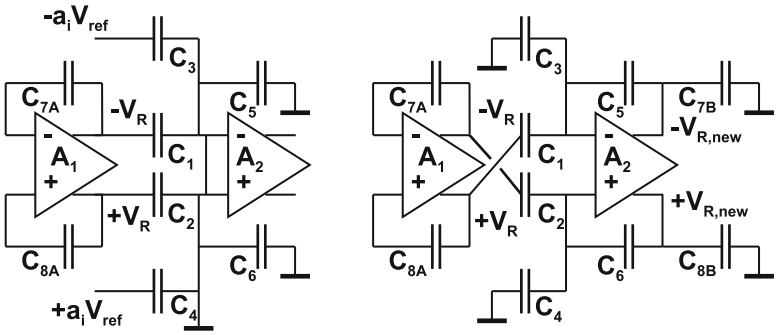


Fig. 8.80 The redundant signed digit (RSD) converter [225]

In the lower part of the figure, the upper comparator level is reduced to $0.15V_{\text{ref}}$, e.g., due to offset. Still the algorithm converges to the same overall result. The RSD algorithm[8] creates in this way robustness for comparator inaccuracies. Figure 8.80 shows an implementation of the RSD principle [225]. During the first phase of the cycle the residue is stored in capacitors C_{7A}, C_{8A}. The result of the comparison results in a value for a_i. In the second phase of the cycle, the signal is multiplied by two by means of the cross-coupling of the differential signals on C_1, C_2. This trick allows that C_1, C_2, C_5, C_6 are all equal. Gain errors due to capacitive mismatches are reduced by interchanging the pair C_1, C_2 with C_5, C_6 for every odd-even cycle. The new values for V_R are stored on C_{7B}, C_{8B} which take the place of C_{7A}, C_{8A} in the next cycle. The typical performance of algorithmic converters is in the 12-bit range at relatively low-power consumption. Applications are found in sensors, e.g., [226].

Example 8.9. Compare the 1-bit pipeline converter and the successive approximation converter.

Solution. Both converters use a logarithmic approximation of the signal: first the MSB is decided, and based on the outcome a residue is evaluated. Both principles use a track-and-hold circuit to store the signal. Most bandwidth related specifications will therefore be comparable.

Where the standard successive approximation converter is executing the algorithm in time, the pipeline converter uses additional hardware stages. The pipeline converter can reach a high throughput, because the intermediate results are shifted from one hardware section to the next. The successive approximation converter can achieve a similar throughput rate, when N parallel converters are used.

Mismatch affecting comparators is reduced in the pipeline converter by going to reduced base or 1.5-bit schemes with calibration. In a multiplexed successive

[8]The general form of this principle is in [225] identified as the Sweeney-Robertson-Tocher division principle.

approximation converter also a calibration is required, which is mostly done at a architecture level.

A major difference between both converters is that in all forms of pipeline conversion, an amplification stage is used to suppress the errors and noise from the lower bit stages. This feature is missing in successive approximation implementations. The amplification stage is the most power hungry part in a pipeline converter, but it allows to achieve a higher signal-to-noise ratio.

8.7 Linear Approximation Converters

Full-flash converters and successive approximation converters will yield at every clock cycle a result. In the case of a full-flash conversion that will be after a latency of 1 or 2 clock periods, and for multistage conversion that delay may last some $N+3$ clock periods. Linear approximation methods and converters need for their operation a operating clock frequency that is at least 2^N times higher in frequency than the sample pulse.

Figure 8.81 shows a simple implementation of a counting analog-to-digital converter or a "digital-ramp" converter. After a start pulse an input sample is taken and the counter is reset. The counter will start incrementing the code that is applied to the digital-to-analog converter. If the level of the input sample is reached, the register will copy the counter value and deliver this value as the conversion result to the succeeding logic. An example of a linear converter with clock subdivision is [228].

These converters are often applied in image sensors. The pixel array of an image sensor is read out via its columns. A row of column analog-to-digital converters is used to process all pixels on one line. The simple structure of a counting converter fits well to the narrow pitch of less than 10 µm, the relatively slow-speed requirement, but high accuracy of 10–11 bits. In [227] the counting idea is

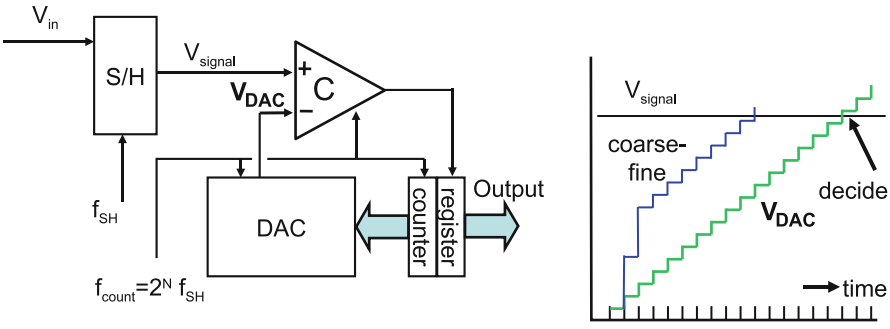


Fig. 8.81 A counting analog-to-digital converter. The *thin line* indicates a coarse step-fine step architecture [227]

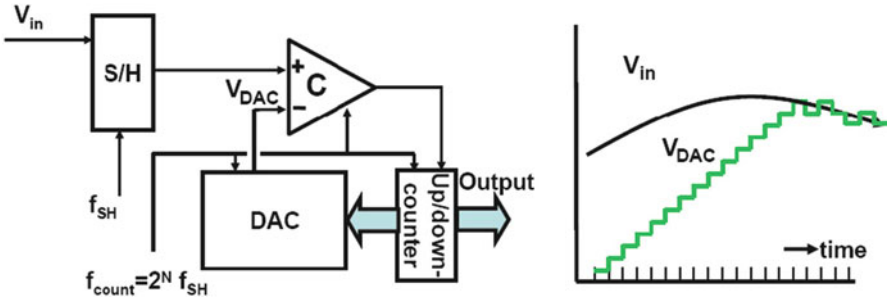


Fig. 8.82 A tracking analog-to-digital converter

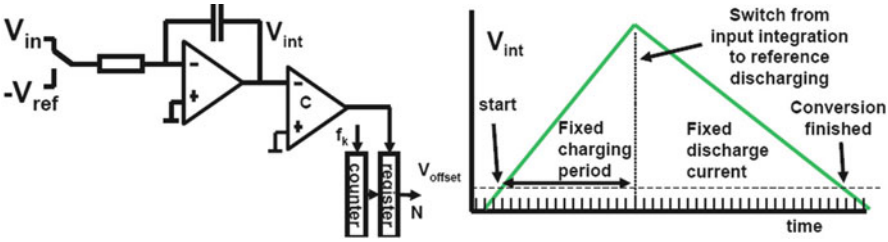


Fig. 8.83 A "dual-slope" analog-to-digital converter

implemented in a phase with increments of $2^n V_{\mathrm{LSB}}$, followed by a phase with V_{LSB} steps, thereby reducing the long conversion time; see the thin line in Fig. 8.81(right). similarities to algorithm converters certainly exist (compare Sect. 8.6.2).

The counting converter can be turned into a tracking analog-to-digital converter [229] by changing the counter in an up-down counter and connecting the comparator output to the up-down switch (Fig. 8.82). The system will operate in a way that the counter and digital-to-analog converter output will follow the input signal. The speed is limited to the speed of the counter clock. The accuracy is determined by the digital-to-analog converter. Yet with simple means a reasonable analog-to-digital converter can be built, e.g., for microprocessor interfacing of slow signals. The same type of feedback loop can also be used in other domains, e.g., mechanical tracking systems. Some offset correction systems, e.g., [230], also show similarity with a tracking analog-to-digital converter.

A "dual-slope" converter is suited for slowly varying input signals. In Fig. 8.83 an integrator circuit integrates the input signal during the fixed sample period. During a second time frame a reference current discharges the integrator, while a counter measures the number of clock periods. The maximum number of clock cycles is around 2×2^N. The input integration has a transfer characteristic comparable to a sample and hold circuit:

$$H(\omega) = \frac{\sin(\pi \omega T_{\mathrm{int}})}{\pi \omega T_{\mathrm{int}}}. \tag{8.42}$$

The low-pass characteristic of this operation makes that this principle is tolerant to RF noise and interference.

A dual-slope converter is an example of a zero-point detecting method or zero-crossing method. The converter determines the value of the unknown signal by subtracting an equivalent signal from the digital-to-analog converter until the zero starting level is reached. The advantage of zero-crossing methods is that the system needs to be linear only around the zero level. Voltage dependency of the integration elements (nonlinear capacitor) in Fig. 8.83 will not impair the conversion accuracy. Moreover an offset in the comparator or integrator is implicitly canceled by the operation as long as the offset in the crossing of the rising edge is still present when the signal returns to zero at the end of the cycle. Hysteresis around the zero crossing cannot be tolerated.

Dual-slope converters find their application especially in the harsh industrial environments and multimeters.

Example 8.10. Compare at flash converters, successive approximation converters, and dual-slope converters with respect to DNL, INL, and absolute accuracy in case of comparator threshold mismatch.

Solution.

	DNL	INL	Absolute accuracy
Flash	Poor, limited by comparator mismatch	Poor, due to ladder and comparator mismatch	Poor, due to ladder and comparator mismatch
Successive approximation	Good, limited by digital-to-analog converter	Good, limited by digital-to-analog converter	Poor, due to comparator offset
Dualslope	Good, digital-to-analog converter	Good, digital-to-analog converter	Excellent, only drift

8.8 Time-Interleaving Time-Discrete Circuits

All converter types except for the full-flash converter need several intermediate timing cycles to convert a signal. This reduces the overall throughput speed. Demultiplexing or time-interleaving the signal over several identical structures allows to match the limited speed of the basic structure to the high-speed requirements. Time-interleaving can also help reduce the power consumption. Equivalent to the situation in digital circuits, demultiplexing will not reduce the number of steps to be taken; on the contrary the number of steps may increase. Power saving is possible because the steps can run at lower speed with lower (stand-by) currents and supply voltages.

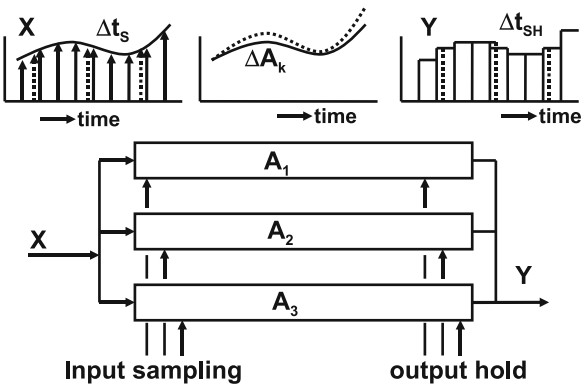


Fig. 8.84 Three different errors in a time-interleaved or multiplexed time-discrete structure

Figure 8.84 analyzes multiplexing of analog time-discrete circuits. A chain of analog-to-digital and digital-to-analog converters is included. The disadvantage of multiplexing is of course the unwanted output signal which consists of a fixed pattern noise, due to DC inequalities, and uncanceled folding products around multiples of the sample frequency of the individual structures. The problem in designing a chip with analog multiplexing is that a two-dimensional wiring pattern has its limitations in achieving a fully identical structure. For example, a one-layer metalization gives asymmetrical crossings. And the speed of signal propagation is roughly half of vacuum, so 1 ps corresponds to 150 µm. Unwanted components to the output signal are caused by random and systematic errors.

The systematic errors can be subdivided according to their origin:

- Technological fixed errors are reduced if all multiplexed structures have the same orientation on chip: no mirrored or rotated placements; see Table 11.7. Although it is important to keep identical circuits close together (e.g., in order to avoid gradients), a trade-off is necessary with respect to the proximity effects of other structures. Many technological fixed errors cause either patterns at the multiplex frequencies or gain errors.
- Electrical errors such as voltage-drop errors are reduced by star-connected signal, pulse, and power wiring; see Fig. 8.25. RC time constants should be matched in value, but preferably consist of identical components. Digital and analog power supplies are separated; however, the common substrate is difficult to avoid and precautions in the digital part have to be taken as well.
- Timing errors affect in first order only the input sampling and the output restoration. The relative position of the pulses has to be accurate. Moreover, fast edges are important to avoid that the moment of sampling or holding becomes signal dependent.

In Sect. 7.7 several techniques are discussed to avoid additive errors. Here especially the multiplicative errors and timing errors are analyzed.

The error signal due to multiplexing of time-discrete structures can be analyzed by means of the spectrum of the output signal [231, 232]; see Fig. 8.85 for $N = 2$.

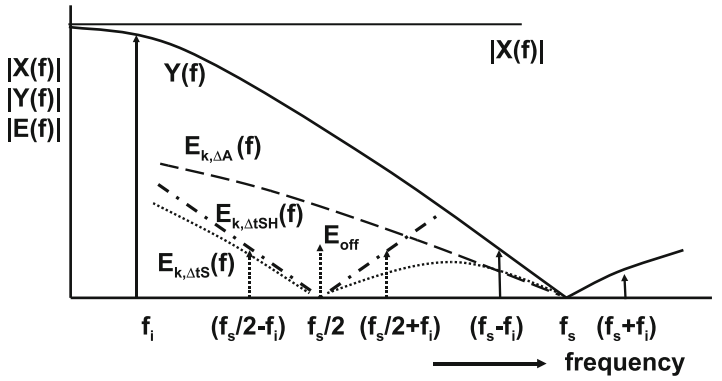


Fig. 8.85 The signal and the trajectory for different error components due to two-times multiplexing

The time-continuous analog input signal $X(f)$ is in this analysis sampled with a frequency f_s and reconstructed to a signal $Y(f)$ with a zero-order hold function with a hold time T_s. The signal is multiplexed over N branches with N samplers in N multiplex phases, each running at $f_{sN} = f_s/N$ and spaced in time at kT_s with $k = 0 \cdots (N-1)$. At the end of the chain the N signals are combined after the sample-and-hold operation over a period T_s.

The spectral contribution of a signal in multiplex line k to the spectrum of the output signal is identical to a sampling system running at frequency $f_{sN} = f_s/N = 1/NT_s$ and is written as (compare Eqs. 3.12 and 4.2)

$$Y_k(f) = \sum_{r=-\infty}^{r=\infty} A_k X(j2\pi(f - rf_{sN}))\mathrm{e}^{j2r\pi fkT_s} \frac{\sin(\pi fT_s)}{\pi fT_s} \mathrm{e}^{-j\pi fT_s} \tag{8.43}$$

with:

$Y_k(f)$ = the contribution of line k to the output signal $Y(f)$
r = index of spectrum repetition around f_{sN}
A_k = amplification of line k
$X(f)$ = the spectrum of the input signal
T_s = the period of the overall clock frequency

The formula is composed of the amplification A_k, the sampled spectrum $X(f)$, the multiplexing phase shift, and the sample-and-hold $\sin(\pi fT_s)/\pi fT_s$ function including the delay term. The analog input spectrum is repeated around multiples of the subsample frequency f_{sN}, but each structure k has a phase shift with respect to structure $(k-1)$ corresponding to the time delay between the sampling moments T_s.

Adding up the outputs of the N lines ideally only gives nonzero contributions for those values of r that are multiples of N. All other spectra around multiples r or f_{sN} (except those which are multiples of f_s itself) extinguish. The ideal total output of this sampled data system is therefore

$$Y(f) = \sum_{m=-\infty}^{m=\infty} AX(j2\pi(f - mf_s)) \frac{\sin(\pi f T_s)}{\pi f T_s} \mathrm{e}^{-j\pi f T_s} \tag{8.44}$$

m is the index of spectrum repetition around f_s. The errors that cause uncanceled components in the output spectrum can be subdivided into four categories:

- The first error is a DC offset between the N branches. This error leads to fixed frequency components at multiples of the branches:

$$E_{\text{off}}(t) = \sum_{r=0}^{r=\infty} V_{\text{off},r} \sin(j2\pi r f_{sN} t). \tag{8.45}$$

- A static time error Δt_s in the input sampling of line k will result in

$$\left| \frac{E_{k,\Delta t}(j2\pi f_r)}{AX(j2\pi f_i)} \right| = \frac{2}{N} \sin(\pi f_i \Delta t_s) \frac{\sin(\pi f_r T_s)}{\pi f_r T_s}. \tag{8.46}$$

- An amplification error ΔA_k in line k leads to

$$\left| \frac{E_{k,\Delta A}(j2\pi f_r)}{AX(j2\pi f_i)} \right| = \frac{1}{N} \frac{\Delta A_k}{A} \frac{\sin(\pi f_r T_s)}{\pi f_r T_s}. \tag{8.47}$$

- A time error Δt_{SH} in the sample-and-hold pulse in line k gives

$$\left| \frac{E_{k,\Delta SH}(j2\pi f_r)}{AX(j2\pi f_i)} \right| = \frac{2}{N} \sin(\pi f_r \Delta t_{SH}) \frac{\sin(\pi f_i T_s)}{\pi f_r T_s}. \tag{8.48}$$

The errors are expressed as the amplitude ratio of a spurious output signal $E_k(j2\pi w f_r)$ at signal frequency, $f_r = f_i + r f_{sN}$, with respect to the amplified input signal at frequency f_i . The three errors due to uncanceled folding components can easily be recognized: the timing errors have input-frequency dependent amplitudes, and the amplification and input timing errors are filtered by the sample/hold transfer function.

Figure 8.85 shows the error components in the case of $N = 2$. E_{off} is the fixed error at f_{sN}. At $f_s/2 \pm f_i$ two errors are indicated caused by time-interleave errors. The dotted and dashed lines $E_k(f)$ indicate the trajectory of each component. The timing-related errors extinguish if the input frequency is low, because a timing error will not lead to a change in input/output signal. Consequently a test with a proper choice of f_i will allow to analyze the type of error in a practical multiplexed device.

An additional class of problems are frequency dependent deviations. Differences in bandwidths between signal processing sections that form a multiplexed structure, will also give rise to timing-dependent errors. Sections with differing bandwidths, will consequently show different group delays; see Eq. 2.157:

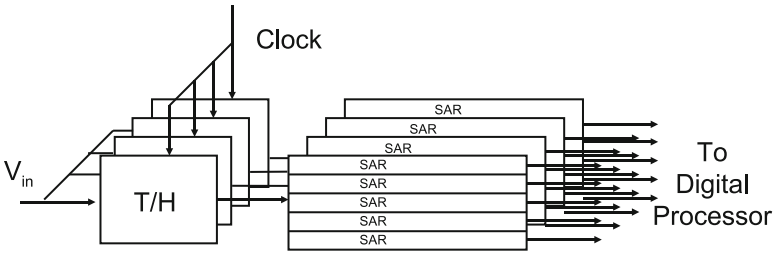


Fig. 8.86 Example of a multiplexed successive approximation analog-to-digital converter, for digitizing a full-spectrum video signal DOCSIS3.0 (BW = 1 GHz, $f_s = 480$ mW, 65-nm CMOS) [233] (courtesy photo: NXP design team)

$$\text{Group delay}(H_{\text{section }i}(\omega)) = \tau_{g,i} = \frac{\tau_i}{1+\omega^2\tau_i^2}, \tag{8.49}$$

where the bandwidth of section i is specified as $1/2\pi\tau_i$. If the input consists of a sine wave $A\sin(\omega t)$, the error signal between two sections i and j can be approximated by an additional term in one of the channels of the form:

$$A\omega(\tau_{g,i} - \tau_{g,j})\cos(\omega t)$$

The resulting error is proportional to the input frequency and bears similarity with the analysis of jitter; see Sect. 3.1.7. At a section bandwidth of approximately two times the sample rate and an input signal frequency of 1/3 of the sample rate, the difference in bandwidths in percent will translate in a similar difference in amplitude error.

Figure 8.86 shows a block diagram of a 64-channel multiplexed 2.6 Gs/s successive approximation converter [233]. The signal is first distributed over four track-and-holds. These circuits each drive the track-and-hold in the four section each containing 16 successive approximation converters. Figure 8.87 gives an impression: the main track-and-hold circuits are placed in the center in order to keep the wires to the four sections as balanced as possible. An overall performance of 48.5 dB in a 65-nm technology is achieved.

Next to interleaving successive approximation converters (see also [211]), also pipeline converters can be multiplexed interleaved and calibrated [234].

8.9 Implementation Examples

Based on a single comparator architecture of Sect. 8.1.8 a full-flash, a successive approximation, and a multistep pipeline converter are described.

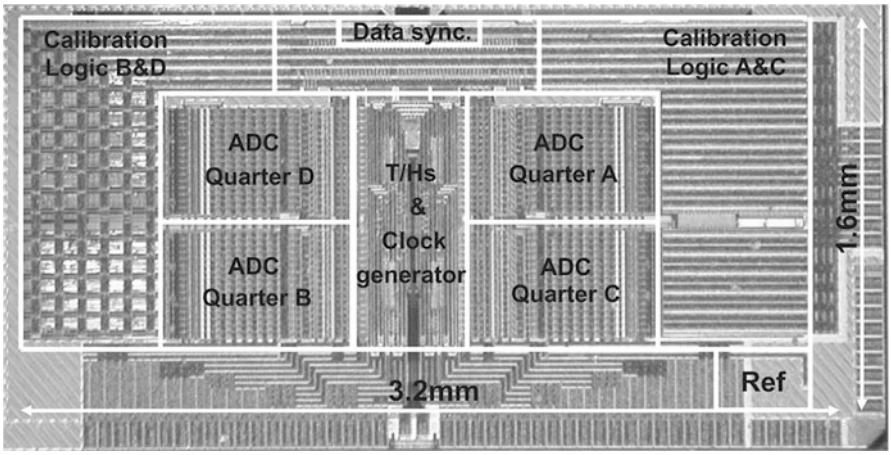


Fig. 8.87 Chip photograph of a multiplexed successive approximation analog-to-digital converter [233]

8.9.1 Full-Flash Analog-to-Digital Converter

The comparator described in the previous section forms the basis for three types of converters: an 8-bit full-flash analog-to-digital converter, a 10-bit successive-approximation analog-to-digital converter, and a multistep analog-to-digital converter, which combines a 3-bit full flash with a 5-bit successive approximation in a multiplexed approach.

The full-flash analog-to-digital converter has been subdivided into eight sections of 32 comparators; each section uses local 5-bit Gray-coding for the LSBs. This scheme allows fast and efficient (2 MOS/comparator) decoding. The 32nd, 64th, etc., comparator in a 3-bit MSB analog-to-digital converter decides which section output will be passed to the data rails.

The ladder structure is identical to that described in Sect. 7.8.1: a two-ladder structure provides a good quality reference voltage. Due to the fact that the comparator uses a differential input pair, the input load and reference ladder load are limited to parasitic charges of the input switch. The reference supply current and the decoupling required in this design are both small. Care has been taken to avoid delay skew between the on-chip-generated clock scheme and the input signal; the generation of bias voltages for 255 comparators and the power distribution also require a careful design and layout.

The main characteristics of the analog-to-digital converter are summarized in Table 8.5.

Figure 8.88 shows the measured SINAD in dB; the ENOB has been plotted on the right axis. The converter achieves an ENOB of 7.5 bits at low-signal frequencies and 7.4 bits at 4.43 MHz and 20 Ms/s.

Table 8.5 Specifications of the three analog-to-digital converters

A/D converter	Full-flash	Successive app.	Multistep
Resolution	8 bit	10 bit	8 bit
Sample rate	25 Ms/s	2 Ms/s	30 Ms/s
Differential linearity	0.6 LSB	0.5 LSB	0.5 LSB
Integral linearity	0.6 LSB	1 LSB	0.6 LSB
ENOB at input 4.43 MHz	7.4	8.5 (1 MHz)	7.4
SINAD (4.43 MHz)	46 dB		46 dB
SD (2–5 harm, 4.43 MHz)	>52 dB		>52 dB
Input bandwidth (1 dB)	>70 MHz	20 MHz	70 MHz
Input signal swing	2 V	1.5 V	1.6 V
Ladder resistance	1,200 Ω	4,800 Ω	1,200 Ω
Active area	2.8 mm^2	1.2 mm^2	1.1 mm^2
		0.4 mm^2 (8 bit)	
Technology		0.8–1 µ (1 PS, 2 Al)	
Current	55 mA	3 mA	13 mA
Current/comparator	200 µA	500 µA	200 µA
Number of comparators	256	1	56

All the converters are based on the comparator shown in Fig. 8.22

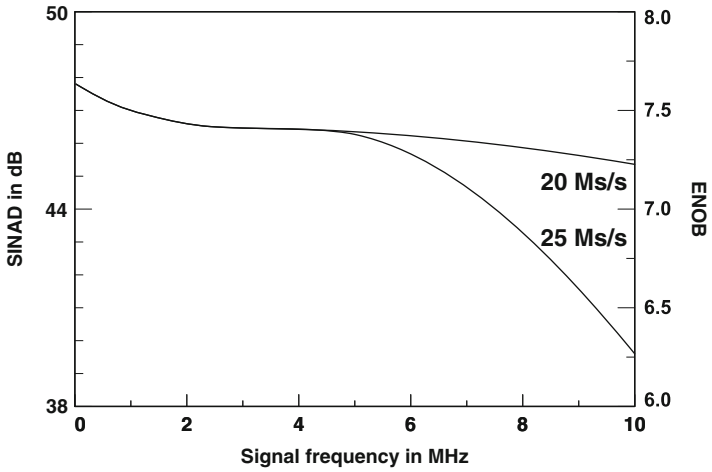


Fig. 8.88 Signal to noise and distortion at 20 and 25 Ms/s as a function of the input frequency

In order to the test substrate immunity, a 17.7 MHz 200 mV_{pp} pulse wave was applied to the substrate of a 13.5 Ms/s running analog-to-digital converter digital-to-analog converter combination. The resulting 4.2 MHz (17.7–13.5) disturbance was 45 dB below the 4.4 MHz converted signal at the digital-to-analog converter output. The analog-to-digital converter in 1 µ CMOS technology was used on several prototype and production chips [235–237].

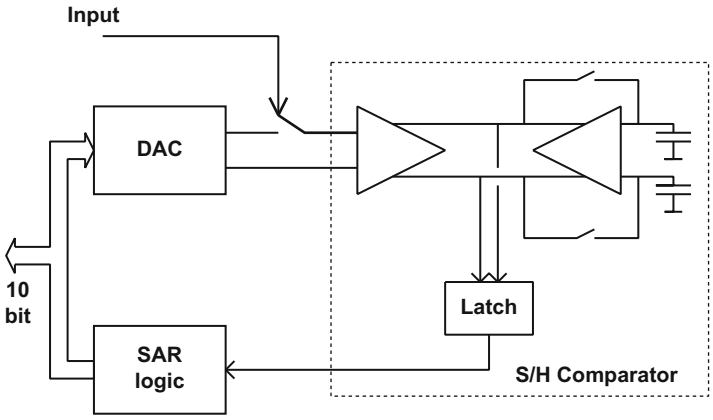


Fig. 8.89 Successive-approximation analog-to-digital converter

8.9.2 Successive-Approximation Analog-to-Digital Converter

Basically, the successive-approximation technique consists of comparing the unknown input voltage with a number of precise voltages generated by a digital-to-analog converter, by means of a single comparator (see Fig. 8.89). As the input voltage may not change during the comparisons, there has to be a sample and hold circuit in front of the actual analog-to-digital. The offset-compensated comparator described in the previous section has a built-in sample-and-hold stage and can therefore be used for comparison as well as for storage of the input signal. The SA analog-to-digital converter realized consists of one offset-compensated comparator, a 10-bit digital-to-analog converter, and some control logic for controlling the digital-to-analog converter and storing the intermediate results. The converter requires 11 clock cycles for complete conversion. Therefore, the actual sampling frequency is limited to about 1–2 Ms/s. Inherent to the architecture, the DNL of the analog-to-digital converter is good. A disadvantage of the converter is the relatively small-signal input range (or the risk of INL errors in the case of large signal swings) which is a consequence of using long-channel tail pairs at the input of the comparator to improve the common-mode rejection.

The successive-approximation analog-to-digital converter design is used in servo applications and microcontroller inputs. Specifications are given in Table 8.5.

8.9.3 Multistep Analog-to-Digital Converter

The multistep analog-to-digital converter[9] (Fig. 8.90) is an 8-bit converter based on a technique involving a combination of successive approximation, flash, and

[9]This section is based on a design by Jeannet v. Rens.

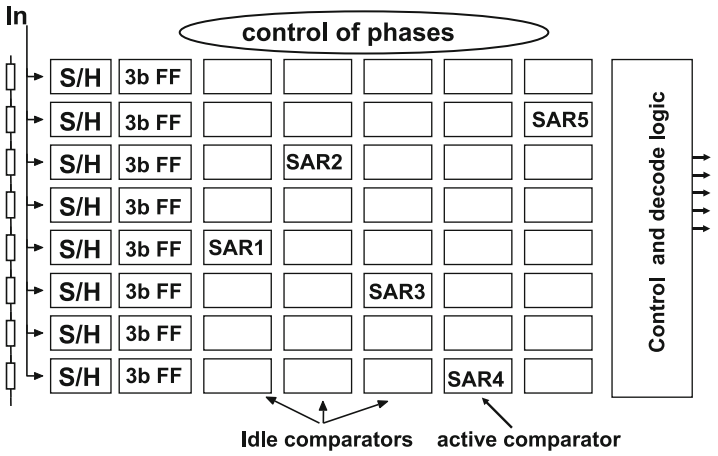


Fig. 8.90 Multi-step analog-to-digital converter (design: J. v. Rens)

time-interleaving. The three most significant bits of the conversion are determined by means of a flash conversion; the remaining 5 bits are realized through successive approximation. Multiple time-interleaved signal paths have been used to increase the maximum sampling frequency.

The hardware of the analog-to-digital converter consists of an array of 56 comparators with a built-in sample and hold stage. The array is grouped in seven channels of eight comparators in a flash structure. The channels operate in a time-interleaved manner. The actual conversion takes place in seven clock cycles. First, the input signal is sampled by, and stored in, one channel of eight comparators (sample phase). A flash decision generates the three coarse bits and selects the comparator that stores the replica of the unknown input signal closest to a reference voltage. This comparator is used in a successive approximation loop to determine the remaining bits, while the other comparators are idle.

The input ranges of the eight comparators in that form the flash structure determine the signal input range of the analog-to-digital converter. Note that use of parallel signal paths can be successful only if the different channels match well. Offset, gain, and timing mismatches between multiple channels give rise to fixed patterns which manifest themselves as spurious harmonic distortion in the frequency domain. The effect of offset is minimized by the use of the previously described offset-compensated comparators. Gain mismatch is minimized by the use of a common resistor ladder digital-to-analog converter and timing mismatch by the use of a master clock which determines the sampling moments of all the channels. The production device is shown in Fig. 8.91.

This converter was produced as a stand-alone product TDA8792 and was the building block for many video integrated circuits.

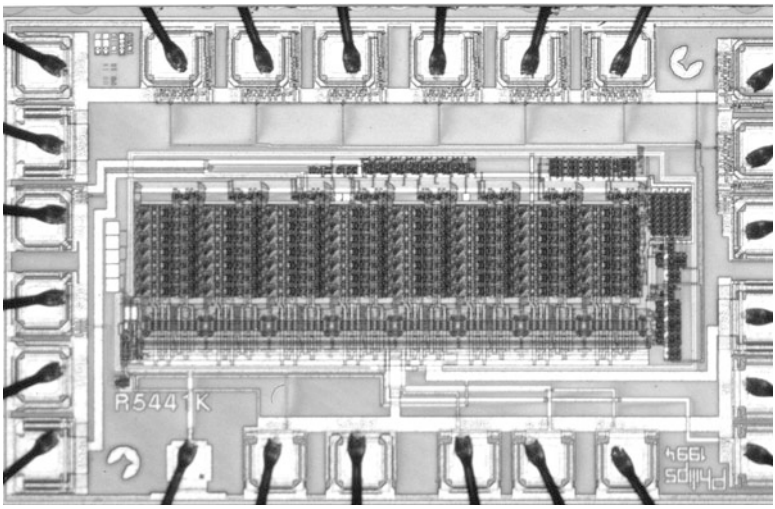


Fig. 8.91 Photograph of multistep analog-to-digital converter TDA8792

8.9.4 Comparison

Table 8.5 shows the main specifications of the three analog-to-digital converters. Basic to all converters is the comparator of Fig. 8.22, in which signal speed and accuracy have been traded-off versus power. The decisive factor for the power comparison is the comparator current. In the successive approximation design this current is higher because this comparator has to handle a larger signal span. The lower kickback of the single comparator in the successive approximation analog-to-digital converter also makes it possible to increase the ladder impedance. All the converters have been extensively used in consumer ICs: digital video, picture-in-picture, instrumentation, etc. In 0.5 µm CMOS the 8-bit multistep runs at 50 Ms/s, while the 9-bit version achieves 8.2 ENOB.

Example 8.11. In an IC process input pairs (as used in comparators, gain stages, etc.) suffer from σ_{Vin}= 50 mV maximum uncorrelated errors, while resistors can be made with 0.1% accuracy. Which ADC architectures can be made advantageously in this process (give indication of the resolution).

Solution. If a signal range of approximately 1 V is assumed, a 5% error results. The main trade-offs are summarized in (Table 8.6):

Table 8.6 Comparison of converters in case of extreme mismatch

ADC architecture	Remarks	Resolution
Flash converter	2^N parallel comparators, limited by comparator mismatch	N = 4 bit
Pipeline and dual-slope converter	Comparator error will be cancelled, INL,DNL determined by digital-to-analog conversion	$N \approx 10$ bit
Logarithmic approximation, successive approximation	Comparator error results in offset, INL, DNL determined by digital-to-analog conversion	$N \approx 10$ bit

8.10 Other Conversion Proposals

Many other principles exist to convert signals from the physical domain to bits. Not all of them are relevant for a larger community, yet some of them may be considered in specific circumstances.

8.10.1 Level-Crossing Analog-to-Digital Conversion

In the previous sections analog-to-digital converters were designed by sampling the signal and subsequently quantizing the signal to reference levels. In this process rounding errors occurred, which were labeled quantization errors. The sequence of sampling and quantizing can also be reversed. The level-crossing analog-to-digital converter in Fig. 8.92 [238–240] generates a new digital output code at each time moment an amplitude quantization level is passed. In its simplest form, this is a flash converter with unclocked comparators. With infinite time resolution this level-crossing algorithm will lead to a digital representation of the input signal with some harmonic distortion, depending on the density of the levels. There is no folding back of spectra and a rather high-quality signal representation be obtained. In a conventional digital system, it is impractical to process this pulse-width modulation signal and therefore a rounding to a time grid is needed. That step introduces rounding errors and quantization problems. Suppose that the rounding will be towards a time grid specified by a sample frequency f_s with a time period T_s. If the level crossing occurs ΔT_s before a sample moment nT_s, the amplitude error is

$$\Delta A(nT_s) = \frac{\mathrm{d}V_{\mathrm{in}}(t)}{\mathrm{d}t}\Delta T_s. \tag{8.50}$$

Assuming that the signal $V_{\mathrm{in}}(t) = A\sin(\omega t)$ is so slow that only one level is passed during a time period T_s, that the probability of the occurrence of a level crossing moment is uniformly distributed, and that the level crossing is independent of the signal derivative, the expectation value of the error is

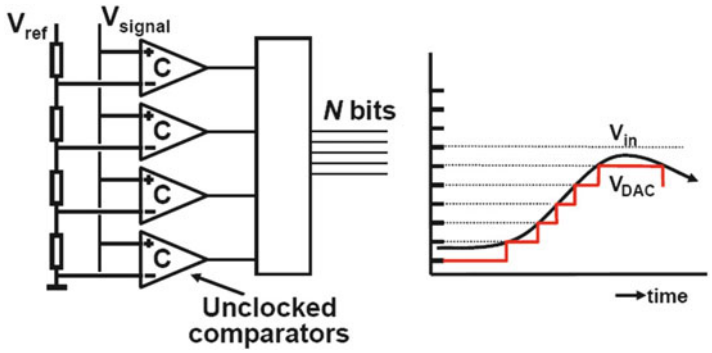


Fig. 8.92 The principle of a level-crossing analog-to-digital converter

$$E((\Delta A)^2) = \left(\frac{\mathrm{d}V_{\mathrm{in}}(t)}{\mathrm{d}t}\right)^2 \times E(\Delta T_s^2) = \frac{A^2\omega^2 T_s^2}{6}. \tag{8.51}$$

The resulting signal-to-noise ratio between signal power and error power is

$$\mathrm{SNR} = 10\log(3) - 20\log(\omega T_s). \tag{8.52}$$

An increase in sample rate or a decrease in sample time of a factor two results in 6 dB of signal-to-noise ratio or the equivalent of 1 bit. When discussing oversampling in Sect. 9.1, the increase in sample frequency in a converter must be a factor of four higher to gain the same amount of signal-to-noise ratio. In a level-crossing device the time axis serves as the quantization axis and a frequency doubling doubles the accuracy. In the oversampled situation, the time axis only serves to spread out the quantization energy.

The requirement that the signal passes no more than one quantization level in one sample period makes this principle not suited for many application domains. A major implementation problem is that the delay between the actual level crossing and the resulting digital transition must be constant, which is not trivial as the delay of latches depends on the overdrive voltage (Sect. 8.1.4).

For low resolutions this principle converges towards asynchronous delta modulation (Sect. 9.8.2 [240]).

8.10.2 Feedback Asynchronous Conversion

Asynchronous converters constantly monitor the signal and create in a feedback path a best-fitting replica. Several low-resolution high-speed examples are reported [241, 242]. An example is shown in Fig. 8.93. The unclocked MSB comparator continuously monitors the signal. The MSB bit is fed into a simple digital-to-analog

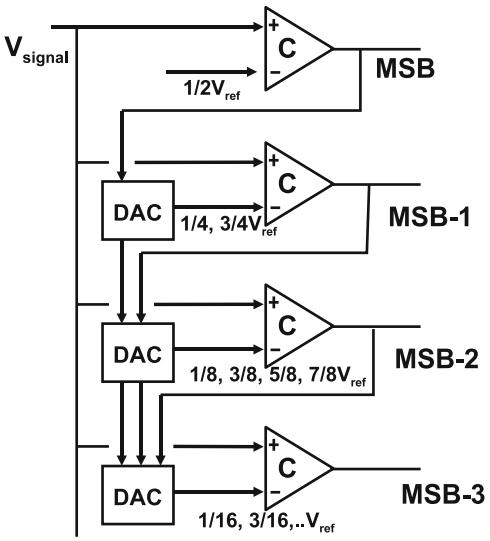


Fig. 8.93 The asynchronous successive approximation analog-to-digital converter [241]

converter that supplies either a $1/4V_{\text{ref}}$ or $3/4V_{\text{ref}}$. The second comparator uses this input reference to determine the MSB-1. If a signal passes through its range the converter will follow the digital code. A settling time of a few nanoseconds for 6 bits suffices.

Comparable to the level-crossing analog-to-digital converter the interfacing to the (clocked) digital world introduces quantization errors.

8.10.3 Mismatch Dominated Conversion

In this entire chapter mismatch is regarded as a severe problem for performing analog-to-digital conversion. Nevertheless it is certainly possible to use mismatch to the advantage [243]. The comparators in Fig. 8.94 are designed to have a large input-referred mismatch. The group comparators connected to $V_{\text{ref},1}$ will span a voltage range of several tens of mV and follow a Gaussian distribution. In order to increase the range a second group of comparators is connected to $V_{\text{ref},2}$ overlapping the first range. The total network will show a probability density function. A summation network (e.g., a Wallace tree structure) is used to count the number of flipped comparators. This number allows to estimate the input voltage via the probability density function. The Wallace tree is a very power hungry network and the input range is determined by the $A_{V_{\text{T}}}$ coefficient.

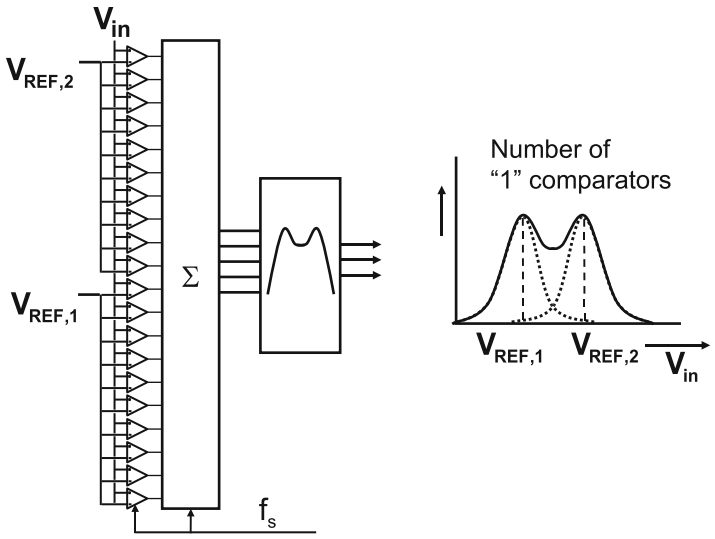


Fig. 8.94 Using mismatch of the comparators to cover an input range

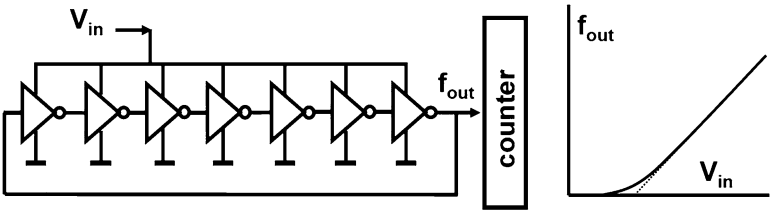


Fig. 8.95 VCO as voltage-to-frequency converter

8.10.4 Time-Related Conversion

In some systems, where a full analog-to-digital converter is not the optimum solution for area or power reasons, the conversion of a voltage to an intermediate quantity (such as a frequency) can be a solution. A voltage-controlled oscillator (VCO) is by principle a voltage-to-frequency converter. The frequency deviation is in first order proportional to the voltage deviation. Both domains, input and output, are time-continuous and amplitude continuous; see Fig. 8.95. However, a frequency is easily mapped on the digital domain by using a time window to count the number of frequency periods. The resolution is proportional to the time window and the sample rate is inversely proportional.

In some systems a time interval contains the required information or a time interval must be monitored. The class of time-to-digital converters is based on principles resembling the counting analog-to-digital converter. A high-frequency

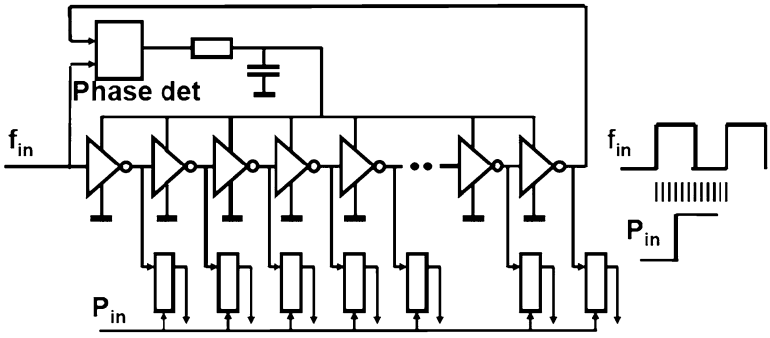


Fig. 8.96 Time-to-digital converter [244]

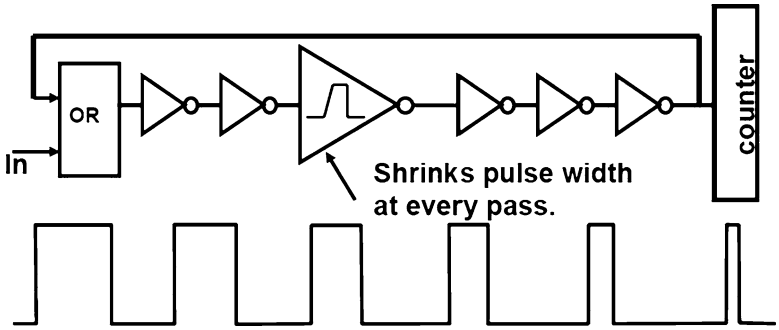


Fig. 8.97 Starving pulse time-to-digital converter [245]

clock is counted during the interval of interest. In case this interval becomes too small, such a simple technique is not practical as the counting frequency is too high. Various structures as in Fig. 8.96 allow to subdivide the fast clock pulse and the resulting set of time-shifted pulses is used to clock the pulse P_{in} at a resolution of, e.g., $1/32$ of the clock period. This method of quantization is often applied in phase-locked loops. The accuracy is limited to the jitter in this system. Power supply variations and substrate interference can also influence the quality. An accuracy in the range of 3–10 ps_{rms} is possible [244].

An elegant implementation is the starving pulse converter [245]. The pulse that has to be measured is entered into a ring of inverters. If the inverters show perfectly symmetrical rising and falling edges without delay, the pulse would travel indefinitely in the inverter ring. One inverter is deliberately modified. Its rising edge is slow, so at each pass the pulse will become a time fraction shorter. The original pulse width is measured by counting the number the pulse before the signal is extinguished; see Fig. 8.97.

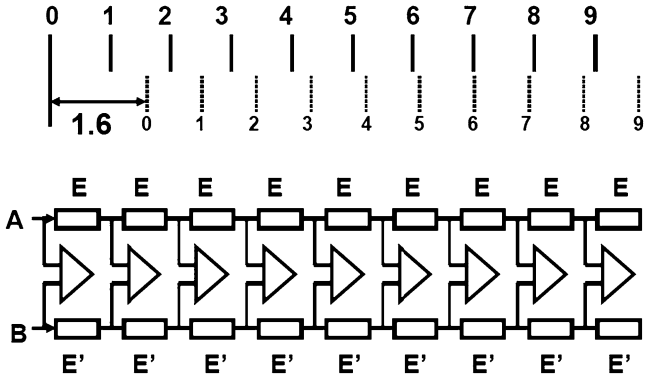


Fig. 8.98 The Vernier or Nonius principle

8.10.5 Vernier/Nonius Principle

The need for higher resolution is not unique to the field of analog-to-digital conversion. In mechanics the Nonius or Vernier scale (after sixteenth- and seventeenth-century Spanish and French mathematicians) is widely used to determine accurately the subdivision in a primary scale. Figure 8.98(upper) shows a primary scale and a secondary scale (dashed). The secondary scale has a subdivision of 0–9 and spans 90% of the primary scale. The unknown distance offsets the zero point of the primary scale and the zero point of the secondary scale. The distance equals the entire number of primary scale units (1 in this example) plus that fraction which is denoted by the number in the secondary scale where the marks of the primary and secondary scale are in line (in this example 6). This principle can be used in electronic designs as is shown in Fig. 8.98(lower). The chains with elements E and E' form the primary and secondary scales while the comparators determine the position where both scales are "in-line." This principle can be used to convert a time period [246]. The elements are implemented as timing cells with slightly different delays. On terminals A and B the start and stop of the interval under measurement are applied. The same technique can also be used with elements E implemented as resistors forming a flash-like converter [247].

8.10.6 Floating-Point Converter

Most analog-to-digital converters operate on the assumption that over the entire range the same resolution is required. In some systems such as sensors and signals with a high crest factor, the required resolution varies with the amplitude of the signal; see Sect. 5.3.2. In computing, this sort of problems is addressed by means of floating-point arithmetic. Also in analog-to-digital conversion floating-point

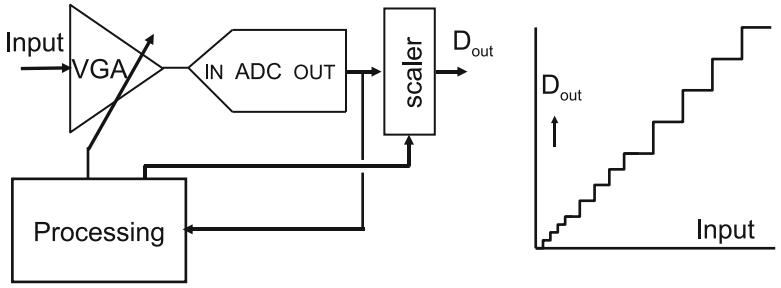


Fig. 8.99 The floating-point principle realized with a variable-gain amplifier (VGA)

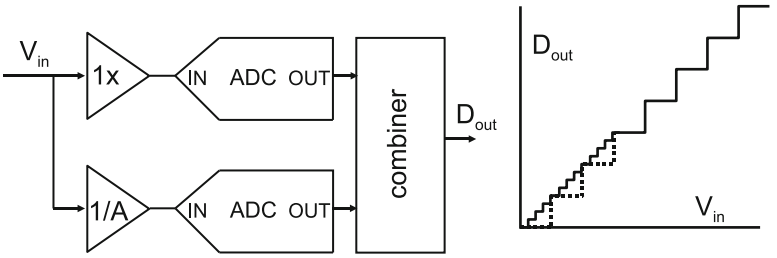


Fig. 8.100 The floating-point principle implemented with two parallel converters

conversion is possible, although most system engineers prefer a fixed-point converter. Figure 8.99 shows an example of a floating point analog-to-digital converter. The actual analog-to-digital converter can use any architecture. The floating-point mechanism is around the converter and consists in its basic form of an analog pre-scaler like a variable gain amplifier and a digital post-scaler. A processing unit detects whether the signal is sufficiently large to use the analog-to-digital converter optimally. If the signal is too large or too small, the processing unit will adapt the input and output scaling. If both these units run with inverse amplifications, the transfer curve will show a resolution-amplitude ratio that remains within certain limits. The difficult point in this design is the accuracy of the pre-scaler. The output level with a gain of "2A" should be the exactly double of the gain "A." Offsets and gain errors are limiting this concept. A more detailed analysis is found in, e.g., [248]. The application of this sort of converters is in sensor interfaces.

The floating-point analog-to-digital converter in Fig. 8.100 uses two parallel converters. The upper converter acts on the small signal levels while an attenuated version of input signal is applied to the lower converter. The advantage with respect to the VGA solution is that no time is lost when a range switch must occur. Moreover, the logic in the combiner can easily adjust for undesired gain and offset errors between both signal paths while making use of those signal levels that trigger both converters.

Similar to other multiplexed circuits, the timing of the sample pulses must be accurately controlled as well as the matching of the bandwidths for large and small signals. Matching the $1\times$ buffer with the $1/A$ attenuator is a challenging task.

Exercises

8.1. In a 65 nm process, the input transistors of the comparators are designed with $\mathrm{W/L} = 5/0.1\,\mu\mathrm{m}$. The effective gate-drain capacitance is 0.2 fF/µm. Estimate the maximum ladder disturbance, if a 7-bit full-flash converter with a total ladder impedance of 1 kΩ is designed.

8.2. Deduce from Fig. 8.60 what is the maximum comparator offset that can be tolerated.

8.3. In a 6-bit full-flash 1 Gs/s analog-to-digital converter the wires of the clock lines must be kept as equal as possible. What is the maximum wireline difference that can be tolerated if the converter must operate at Nyquist frequency? Assume a propagation speed of 10^8 m/s.

8.4. Rank the following design parameters for achieving a high BER in order of importance: the gate width of the latch transistors, the length, the current, the gate oxide thickness, and the gate-drain overlap capacitance.

8.5. Repeat the example of Table 8.2 with 0.25 µm technology data and an input range of 2 V. What is surprising?

8.6. Design a decoder for a 5-bit flash converter based on a Wallace tree summation network.

8.7. Show that for a sinusoidal signal the digital output power of an N-bit parallel output port is smaller than for a serialized single pin output.

8.8. At the input of an 8-bit analog-to-digital converter a ramp-type signal rising at 1 LSB per sample period is applied. What is the power consumption at the digital output compared to the maximum power? What happens to the power in case of 1 LSB DNL errors, and what in case of an 1 LSB INL error?

8.9. How can comparator mismatch in a multiplexed successive approximation converter affect the performance?

8.10. A 7-bit flash converter uses 128 resistors of 25 Ω each with a 50 fF parasitic capacitance to each comparator. If the internal signal swing of the comparator is 1 V, calculate the kickback amplitude. Does the kickback vary with input signal level? Where is the worst case level?

8.11. A sine wave must be converted with good absolute accuracy (without DC offsets). No auto-zero or calibration mechanism is available. Give a reason why a flash converter is a better choice than a successive approximation converter.

8.12. In Fig. 8.6 exchange the connections of the $\overline{clock}$ signal and the signals coming from the pre-latch. Does this solve the hysteresis problem and what is the cost?

8.13. Draw a transfer curve of a 2-bit coarse and 4-bit fine analog-to-digital converter. Add the transfer curve in case one of the coarse comparators has an offset of 1% of the input range. Do the same if this offset applies to a fine comparator.

8.14. A 1.6 Gs/s analog-to-digital converter is build by multiplexing 64 successive approximation converters. If offsets are normally distributed calculate σ_{comp} for a 50 dB performance of 95% of the dies. The bandwidth of the T&H circuits is 1.5 GHz. How much variation is allowed on this bandwidth?

8.15. A 1 LSB difference produces 10 mV voltage swing on the nodes of a latch in a comparator with parasitic capacitances of 100 fF. The maximum current in each branch of the latch is 100 µA. The current factor for a square transistor is 200 $\mu A/V^2$. Calculate the BER for a maximum decision time of 1 ns.

8.16. A comparator generates 50 fC of kickback charge. The nodes of a ladder have a parasitic capacitance of 150 fF each. If the ladder can consume 1 mA from a 1 V reference source and the converter must run at 2 Gs/s, what is the maximum resolution?