Chapter 4
Analog and Mixed Signal Design

The demand for Digital processing of data is seamlessly increasing for various day to day applications around us. It is because of the easier, faster and cheaper way of processing and storing data in digital format, yet efficiently. This in-turn has resulted in demand for Mixed Signal processing systems to interface with the analog and digital world. The challenges in designing a Mixed Signal system are to suppress phase noise, higher switching speeds and optimum conversion capabilities with least power dissipation. PLL, OPAMP, DAC, ADC, etc. are some of the key building blocks in an Analog and Mixed Signal System.

In this chapter a Two Stage OPAMP is designed and modeled using SPICE based on the specifications provided for 180 nm technology. The simulations are carried out using LTspice tool to extract and verify the design parameter. A layout is designed for the OPAMP. DRC and LVS debug tools are used to verify the design rules and connectivity of the layout. Parasitics are also extracted and analyzed for the design. All these processes are carried out using Cadence Virtuoso Schematic and Layout editor tool for 180 nm technology.

The prerequisite to approach this chapter would be an adequate knowledge of CMOS designs in Analog domain and basic knowledge of layout designs and SPICE modeling.

4.1 Schematic Design of OPAMP

4.1.1 Introduction

An Operational Amplifier is a DC coupled high gain electronic voltage amplifier with differential inputs and usually a single output [1]. A two stage OPAMP consists of three major blocks – Differential Amplifier stage, Gain Stage with Compensation capacitor to lower the gain at high frequencies and Buffer. An OPAMP is used in a variety of applications in linear circuit applications: Differential amplifier, inverting

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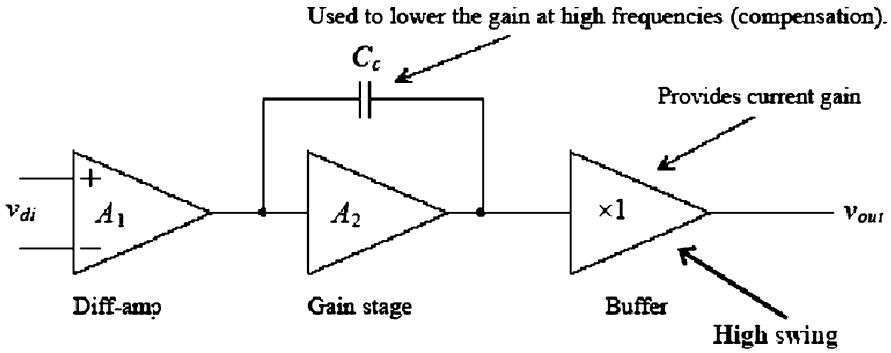

Fig. 4.1 The functional block diagram of a two stage OPAMP

and non-inverting amplifier, Integrator, Differentiator, Comparator, Voltage follower, etc. and in non-linear circuit applications: Peak detector, logarithmic, exponential outputs, PLL, ADC, DAC, etc. The functional block diagram of a Two Stage OPAMP is shown in Fig. 4.1 [2].

4.1.2 Two Stage OPAMP Design

A Two Stage OPAMP is designed and simulated in this section [2]. The design is done using SPICE modeling and the simulations are carried out using LTspice to extract and verify the design parameters against the designed values. The model file obtained from MOSIS-TSMC library for 180 nm technology [3] is used in the OPAMP modeling and simulations.

4.1.2.1 Specifications

The Two Stage OPAMP is designed for TSMC 180 nm technology for the following specification:

- Open Loop Gain, **Av** >100 V/V (40 dB)
- Power Supply, **VDD** = −**VSS** = 2.5 V
- Gain Bandwidth at −3 dB gain, $\mathbf{f}_{3db}$ >5 MHz
- Load Capacitance, $\mathbf{C}_L = 10$ pF
- Slew Rate, **SR** > 10 V/μs
- Output Voltage Swing, $\mathbf{V}_{out} = \pm 2$ V
- Input Common Mode Range, **ICMR** = −1 V to +2 V
- Maximum Power Dissipation, $\mathbf{P}_d \leq 2$ mW
- Phase Margin, $\mathbf{\Phi}_m \geq 60°$
- Channel Length , **L** = 180 nm

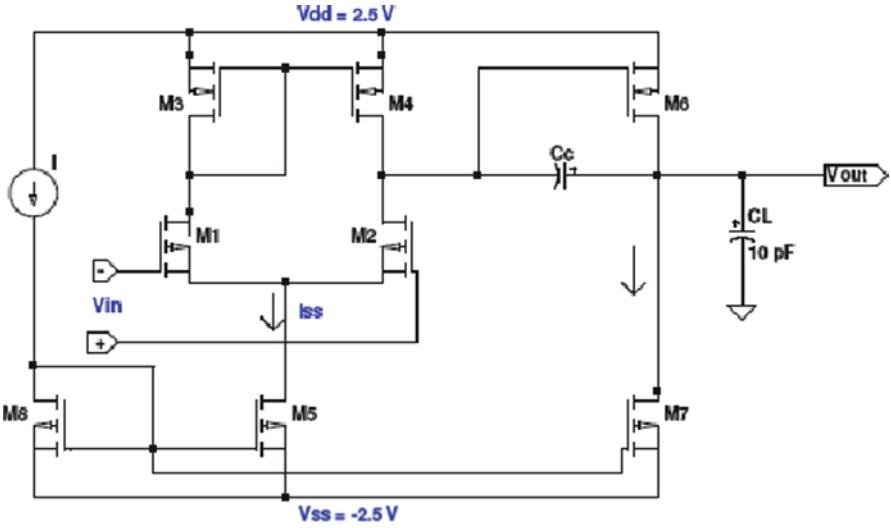

Fig. 4.2 The schematic diagram of two stage OPAMP

For 180 nm technology, the MOS device parameters obtained from MOSIS-TSMC fabrication process lab is as follows:

For NMOS:

- $\mathbf{K_n'} = (\mu_n C_{ox})/2 = 177.2\ \mu A/V^2$
- $\mathbf{V_{tn}} = 0.35\ V$
- $\boldsymbol{\lambda_n} = 0.09/V$

For PMOS:

- $\mathbf{K_p'} = (\mu_p C_{ox})/2 = -35.6\ \mu A/V^2$
- $\mathbf{V_{tp}} = -0.39\ V$
- $\boldsymbol{\lambda_p} = 0.1/V$

4.1.2.2 Schematic of OPAMP

The schematic diagram of Two Stage OPAMP for which aspect ratios for MOS transistors and compensation capacitance values is required to be calculated is shown in Fig. 4.2 [4].

4.1.2.3 Design Calculations

The Two Stage OPAMP is designed as per the specifications listed in Sect. 4.1.2.1. The end results of the design calculations are the channel width of each of the MOS

transistor and Compensation capacitor value for the OPAMP. The design procedure followed is mentioned below [4]:

1. *Calculation of Compensation capacitance* (Cc):
   It is known that placing the output pole 2.2 times higher than the Gain Bandwidth permitted a 60° Phase Margin. From the specifications, required Phase Margin is 60°. Hence we have,

$$\begin{aligned} &Cc > (2.2/10)C_L \\ &Cc > (0.22)\times 10\ \text{pF} \\ &Cc > 2.2\ \text{pF} \\ &Cc = 3\text{pF} \end{aligned}$$

2. *Calculation of Tail Current* (Iss):
   The tail current, Iss or I_5 is given by,

$$\begin{aligned} &\text{Iss} = \text{SR} \times \text{Cc} \\ &\text{Iss} = 10\ \text{V}/\mu\text{s} \times 3\ \text{pF} \\ &\text{Iss} = 30\mu\text{A} \end{aligned}$$

3. *Calculation of Aspect ratios* $(W/L)_3$ and $(W/L)_4$ for M3 and M4:
   The aspect ratio for M3 is calculated based on the ICMR (max) given in the specification.

$$\begin{aligned} &(W/L)_3 = (2\times I_5)/\left[K_p'\left(V_{DD} - V_{in-max} - |V_{tp}| + V_{tn}\right)\right]^2 \\ &(W/L)_3 = \left(2\times 30\times 10^{-6}\right)/\left[2.5-2-0.39+0.35\right]^2 \\ &(W/L)_3 = 3.98 \\ &(W/L)_3 = (W/L)_4 = 4 \end{aligned}$$

4. *Calculation of Aspect ratios* $(W/L)_1$ and $(W/L)_2$ for M1 and M2:
   The aspect ratio for M1 is calculated based on the Gain specification given.

$$Av = [2/(\lambda n + \lambda p)]\times\left[(2\times K_n'\times W)/(\text{Iss}\times L)\right]^{1/2}$$

   Given Specification, Av > 100 V/V
   Substituting and solving the values in the above equation, we get,

$$\begin{aligned} &(W/L)_1 = 7.64 \\ &(W/L)_1 = (W/L)_2 = 8 \end{aligned}$$

5. *Calculation of Aspect ratios* $(W/L)_5$ and $(W/L)_8$ for M5 and M8:
   The aspect ratio for M5 is calculated based on ICMR (min) specification.

$$V_{ds5} = V_{in}(\min) - V_{ss} - \left[I_5 / \left(K_n' (W/L)_1 \right) - Vtn \right]$$

   Substituting the values from the specification data and previous calculations, We get,

$$V_{ds5} = 1.005 \text{ V}$$
$$(W/L)_5 = (2 \times I_5) / \left[K_n' \times (V_{ds5})^2 \right]$$

   Substituting the values in the above equation, we get,

$$(W/L)_5 = 0.34$$
$$(W/L)_5 = (W/L)_8 = 1$$

6. *Calculation of Aspect ratio* $(W/L)_6$ for M6:
   The Transconductance of the input transistor M1 is given by,

$$g_{m1} = \text{(Gain Bandwidth) x (Compensation Capacitance)}$$
$$g_{m1} = 2\pi \times 5 \times 10^6 \times 3 \times 10^{-12}$$
$$g_{m1} = 94.25 \mu S$$

   The Transconductance of the transistor M6 is calculated for the given specification of Phase Margin $\geq 60°$

$$gm6 \geq 10 gm1$$
$$gm6 = 942.5 \mu S$$

   The aspect ratio for M6 is calculated as follows:

$$(W/L)_6 = g_{m6} / \left[K_p' \times V_{ds6}(\text{sat}) \right]$$

   Substituting values in the above equation, we get,

$$(W/L)_6 = 54$$

7. *Calculation of Aspect ratio* $(W/L)_7$ for M7:
   The current flowing through transistor M6 is given by

$$I_6 = (g_{m6}) / \left[2 \times K_p' \times (W/L)_6 \right]$$

Table 4.1 Channel width of MOS transistors designed for 180 nm technology OPAMP

MOS transistor	Aspect ratio (W/L)	Channel width (μm)
M1	8	1.44
M2	8	1.44
M3	4	0.72
M4	4	0.72
M5	1	0.4
M6	1	0.4
M7	54	9.72
M8	8	1.44

Substituting the values in the equation,

$$I_6 = 230\mu A$$

The aspect ratio for M7 is given by the following equation:

$$(W/L)_7 = (W/L)_5 \times (I_6 / I_5)$$

Substituting values in the above equation, we get,

$$(W/L)_7 = 8$$

4.1.2.4 Design Calculation Results

The maximum power dissipation for the design is verified against the specification as follows:

Power Dissipation,

$$\begin{aligned} Pd(max) &= (I_5 + I_6) \times (VDD + |VSS|) \\ Pd(max) &= (30\mu + 230\mu) \times (2.5 + |-2.5|) \\ Pd(max) &= 1.3 \text{ mW} \end{aligned}$$

Max. power dissipation for the design is less than the specified limit of **2 mW**.

The channel width required for each of the MOS transistors for the OPAMP designed is calculated from the aspect ratios. For 180 nm process technology the channel width is tabulated as shown in Table 4.1

Other important parameters calculated in the design steps are as follows:

- Compensation Capacitance, $\mathbf{C_c = 3\ pF}$
- Load Resistance (Arbitrary value), $\mathbf{R_L = 100\ k\Omega}$
- Current flowing through M5 (Tail Current), $\mathbf{I_5 = 30\ \mu A}$
- Current flowing through M6, $\mathbf{I_6 = 230\ \mu A}$

4.1.2.5 Definition of Design Parameters

Definition of design parameters that are extracted from the simulation of TS-OPAMP are as follows:

1. *Open Loop Gain*: The Gain of the OPAMP for the input at positive input terminal without feedback and negative terminal input grounded
2. *Gain Bandwidth*: The frequency Bandwidth of the system at which the gain drops to −3 dB gain
3. *Phase Margin*: It is the difference measured in degrees between the absolute phase angle of OPAMP output signal and 180°
4. *Input Common Mode Range (ICMR):* The range of input voltage where the OPAMP has approximately unity gain
5. *Input Offset Voltage*: The input required to make the output of the OPAMP to zero volts
6. *Output Voltage Swing*: The range of the maximum voltage points till which the OPAMP output can swing
7. *Slew Rate*: It is the maximum rate of change of output signal at any point of time
8. *Transfer Function*: It is a function of Output of the OPAMP with respect to the Input
9. *Output Impedance*: The Impedance offered by the OPAMP at the output terminal
10. *Power Dissipation*: The total power dissipated by the OPAMP during its operation

4.1.2.6 Simulations and Verification

The Two Stage OPAMP designed for 180 nm process technology is simulated using LT Spice and the design specifications are verified against the extracted values [5]. The model file obtained from MOSIS-TSMC library for 180 nm technology is used in the OPAMP modeling and simulations.

- Extraction of Open Loop Gain, Gain Bandwidth and Phase Margin at 0db Gain AC analysis done to extract the above mentioned parameters. The simulation waveform obtained (Bode Plot) is shown in Fig. 4.3.

  Configuration: Open Loop (Extracted parameters at 0 dB gain)
  - *Gain*: 28 dB
  - *Bandwidth*: 4 MHz
  - *Phase Margin*: $(180° + \Phi) = 180° - 102° = 78°$

- Extraction of Open Loop Gain, Gain Bandwidth and Phase Margin at -3db Gain AC analysis done to extract the above mentioned parameters. The simulation waveform obtained (Bode Plot) is shown in Fig. 4.4.

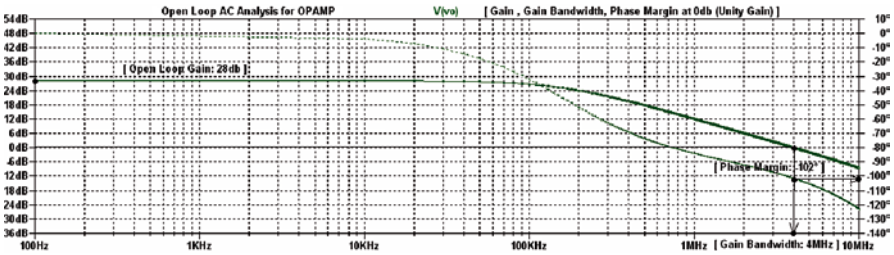

Fig. 4.3 Simulation of TS-OPAMP to extract AC analysis parameters at 0 dB gain

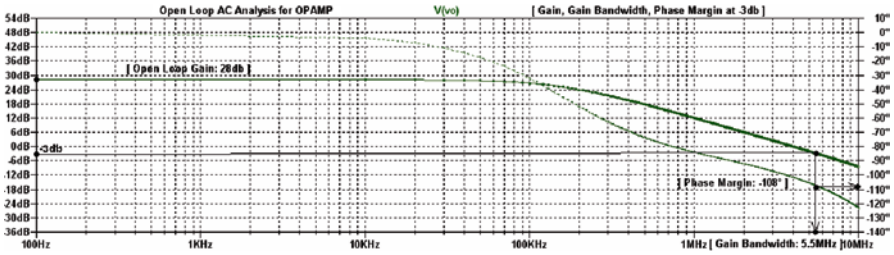

Fig. 4.4 Simulation of TS-OPAMP to extract AC analysis parameters at 3 dB gain

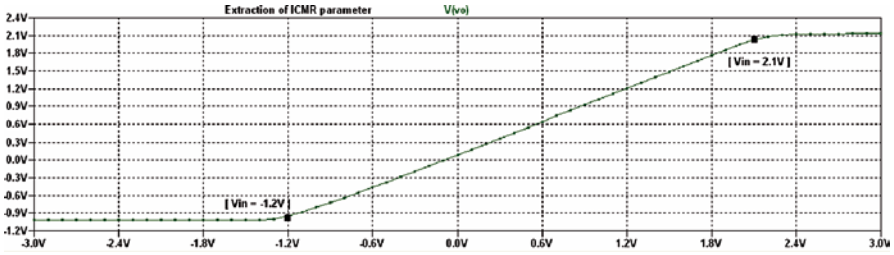

Fig. 4.5 Simulation of TS-OPAMP to extract ICMR for the design

Configuration: Open Loop (Extracted parameters at −3 dB gain)
- *Gain*: 28 dB
- *Bandwidth*: 5.5 MHz
- *Phase Margin*: $(180° + \Phi) = 180° - 108° = 72°$

- Extraction of ICMR
  The simulation waveform obtained to extract ICMR is shown in Fig. 4.5.

  Configuration: Unity Gain Feedback
  - *ICMR*: −1.2 V to +2.1 V

- Extraction of Input Offset Voltage
  The simulation waveform obtained to extract Input Offset Voltage is shown in Fig. 4.6.

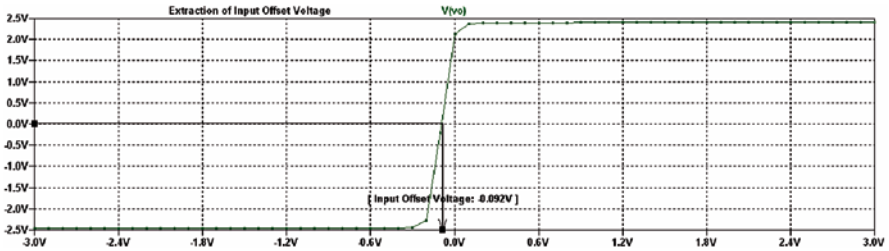

Fig. 4.6 Simulation of TS-OPAMP to extract input offset voltage for the design

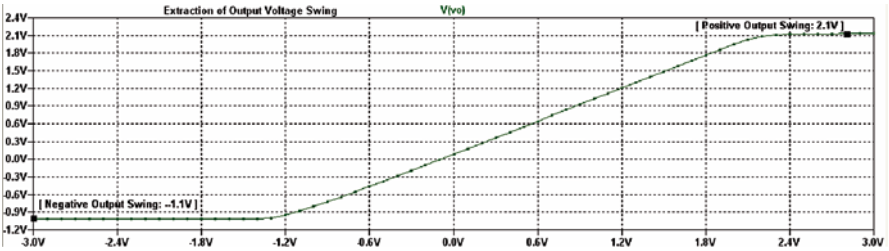

Fig. 4.7 Simulation of TS-OPAMP to extract output voltage Swing

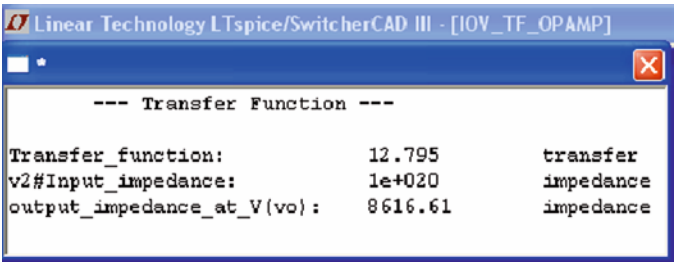

Fig. 4.8 Snapshot of the transfer function computed for TS-OPAMP design

Configuration: Open Loop
– *IOV*: –92 mV

- Extraction of Output Voltage Swing
  The simulation waveforms obtained to extract Output Voltage Swing is shown in Fig. 4.7.

  Configuration: Open Loop
  – *OVS*: –1.1 V to 2.1 V

- Extraction of Transfer function and Output Impedance
  The simulation results obtained to extract Transfer function and Output Impedance of the design is shown in Fig. 4.8.

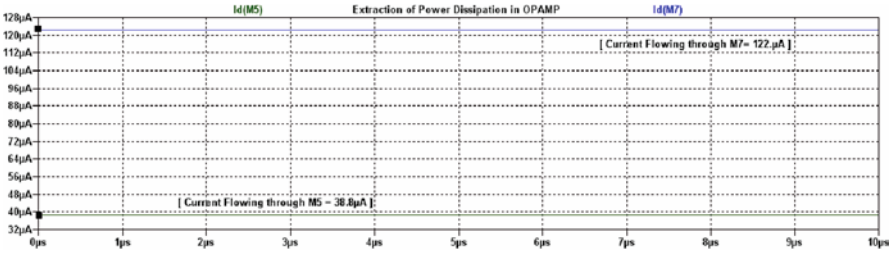

Fig. 4.9 Simulation of TS-OPAMP to extract max. Power dissipation of the design

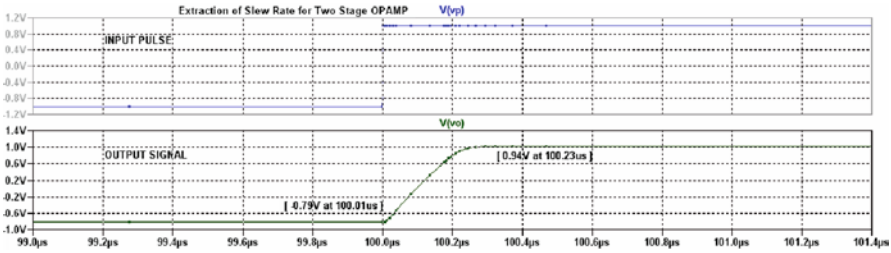

Fig. 4.10 Simulation of TS-OPAMP to extract slew rate for the design

Configuration: Open Loop
- Transfer Function: 12.795
- Output Impedance: 8.6 kΩ

- Extraction of Maximum Power Dissipation
  The simulation waveform obtained to extract maximum Power Dissipation of the TS-OPAMP designed is shown in Fig. 4.9.

  Configuration: Unity Gain Feedback
  - Max. Power Dissipation,

$$P_d = (38.8\mu A + 122\mu A) \times (2.5\ V + |-2.5\ V|)$$
$$P_d = 0.804\ mW$$

- Extraction of Slew Rate
  The simulated waveform obtained to extract Slew Rate for the design is shown in Fig. 4.10.

  Configuration: Unity Gain Feedback
  - Slew Rate (SR) $= (V_2 - V_1)/(T_2 - T_1)$

$$SR = \left[0.94V - (-0.79V)\right] / (100.23\mu s - 100.01\mu s)$$
$$SR \approx 8V/\mu s$$

Table 4.2 Comparison of design specification against results obtained for TS-OPAMP design

Parameters	Design specification	Results obtained
Open loop gain (Av)	100 V/V (40 dB)	28 dB
Band width (BW) at		
0 dB	–	4 MHz
3 dB	5 MHz	5.5 MHz
Phase margin (Φ) at		
0 dB	–	72°
3 dB	≥ 60°	78°
ICMR	−1 V to +2 V	−1.2 V to + 2.1 V
Slew rate	10 V/μs	8V/μs
Output voltage swing	−2 V to +2 V	−1.1 V to +2.1V
Input offset voltage	–	−92 mV
Max. power dissipation	≤ 2 mW	0.804 mW
Transfer function	–	12.795
Output impedance	–	8.6 κΩ

4.1.3 Results

The result obtained from the simulations carried out for TS-OPAMP is verified against the specification. The comparison results are tabulated as in Table 4.2.

4.2 Layout Design of OPAMP

4.2.1 Introduction

The Two Stage OPAMP designed in Sect. 4.1 is implemented to obtain the layout with optimal area and least parasitics for 180 nm technology. A schematic of TS-OPAMP is also drawn along with the layout. Cadence Virtuoso tool is used to draw schematic and layout for the design. After obtaining the layout with clean DRC and LVS, the netlist along with the parasitics is extracted with the help of the tool. Post layout simulation is carried out using this netlist to verify the design specifications.

4.2.2 Layout Design

In this section, the procedure for schematic and layout design of TS-OPAMP is illustrated.

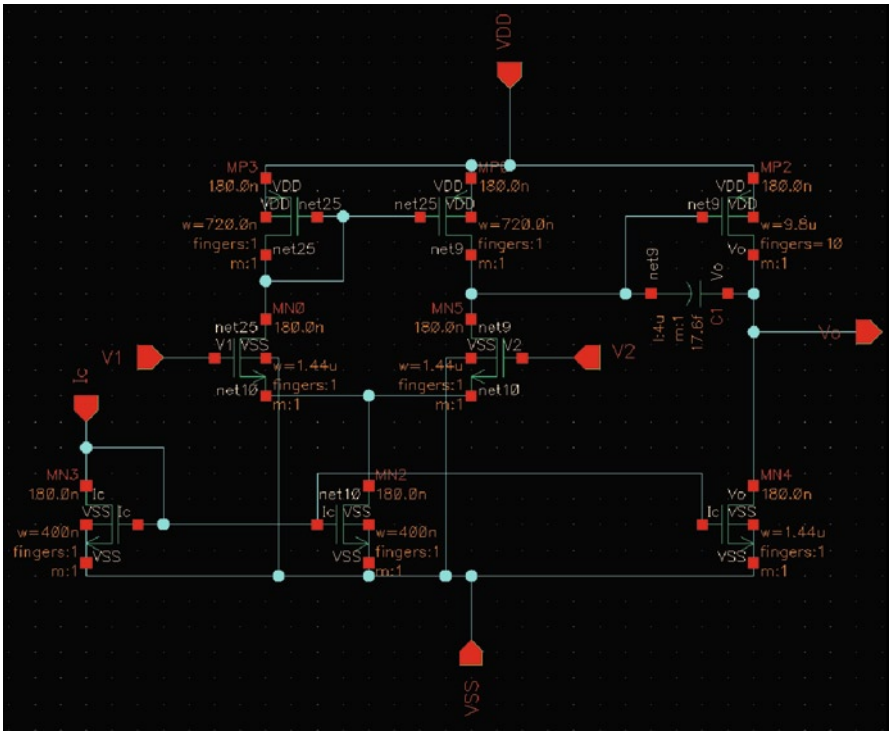

Fig. 4.11 Schematic of TS-OPAMP

4.2.2.1 Schematic Design of OPAMP

The schematic design is required to carry out LVS after drawing the layout section to verify the connectivity of the circuit. The screenshot of the schematic design of TS-OPAMP is shown in Fig. 4.11. The components are chosen as per the designed results available in Table 4.2. Metal plate capacitor is selected for the layout design for compensation capacitor.

4.2.2.2 Layout Design of OPAMP

The Layout of OPAMP is drawn as per the schematic in Fig. 4.11. From the Table 4.2 it can be noted that MOSFET M7 has very large channel width. In order to avoid delays and other parasitic effects caused due to large channel width, fingering is done to break up the MOSFET into 10 MOSFETs of equal channel width [6]. The screenshot of MOSFET M7 with finger – 10 is shown in Fig. 4.12.

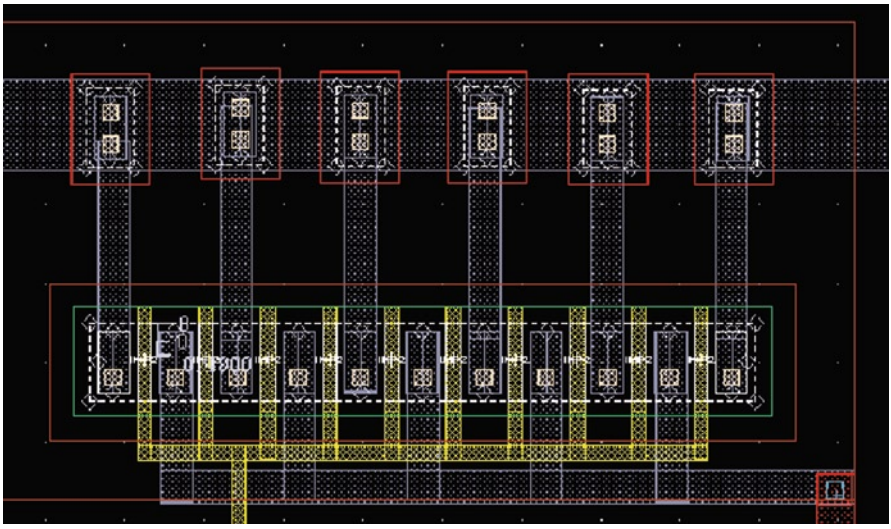

Fig. 4.12 Screenshot of MOSFET with finger-10

Since the finger for M7 is 10, the total channel width of 9.8 μm is divided into 10 MOSFETs with channel width of 0.98 μm each. The Fig. 4.12 shows the alternate connections made to the source of MOSFET to connect it to the VDD power line. Similarly, alternate connections are done for the drain as well.

The screenshot of completed layout design of TS-OPAMP is shown in Fig. 4.13.

The completed layout of TS-OPAMP is verified for DRC. Once the layout is DRC clean, LVS is performed against the schematic to verify the connectivity of the design. LVS match is obtained for the design. The screenshot of LVS match indicator for the design is shown in Fig. 4.14.

For the LVS matched layout design, the SPICE netlist along with parasitics is extracted using RCXT tool in Cadence Virtuoso. Graphical view of the parasitics such as, resistance and capacitance in the layout design is also observed. Some of the screenshots obtained to illustrate the parasitics in the layout design are shown in the following figures.

The screenshot of the complete TS-OPAMP layout with parasitics identified is shown in Fig. 4.15.

The parasitics existing at poly of MOSFET having 10 fingers is shown in Fig. 4.16.

The parasitics identified in metal plate compensation capacitor is shown in Fig. 4.17.

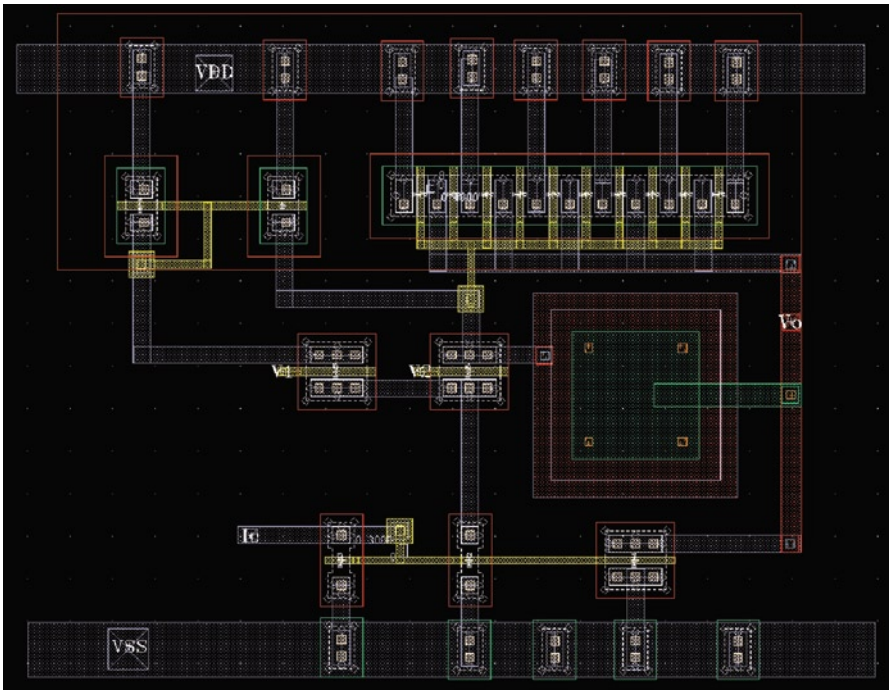

Fig. 4.13 Screenshot of completed layout design of TS-OPAMP

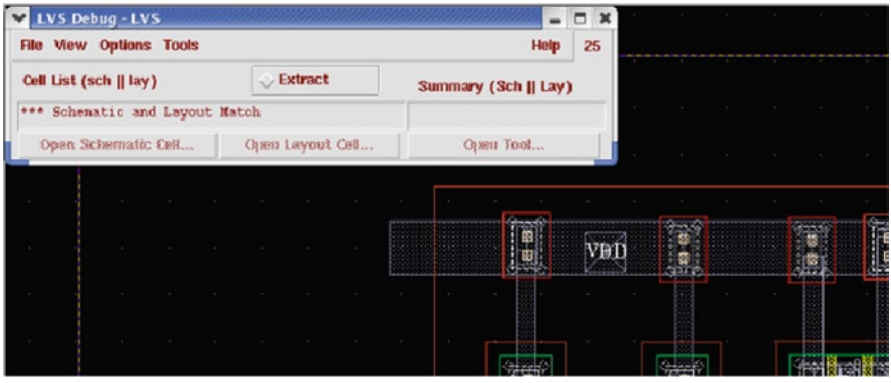

Fig. 4.14 Screenshot of LVS match for TS-OPAMP design

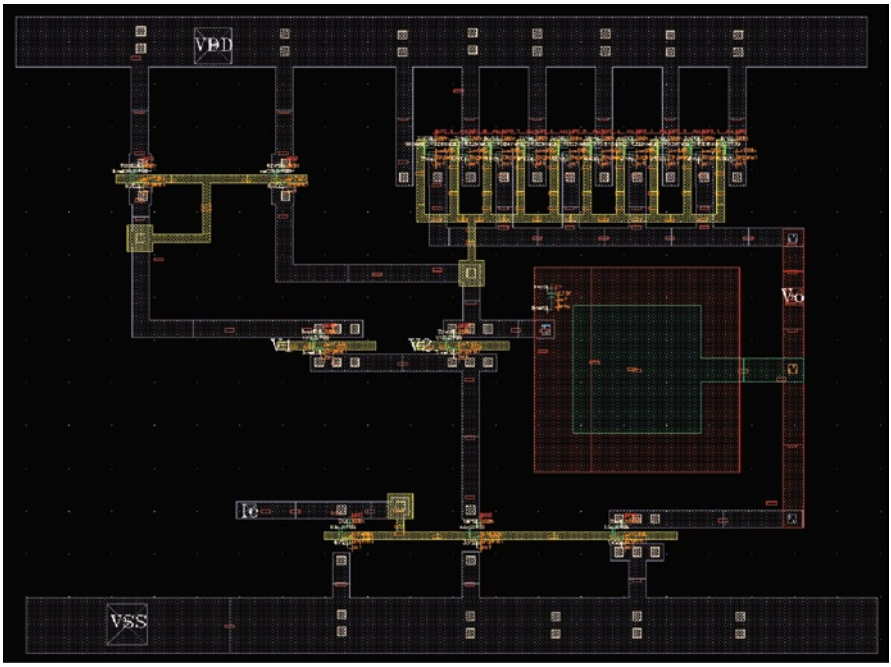

Fig. 4.15 Screenshot of TS-OPAMP layout with parasitics identified in the design

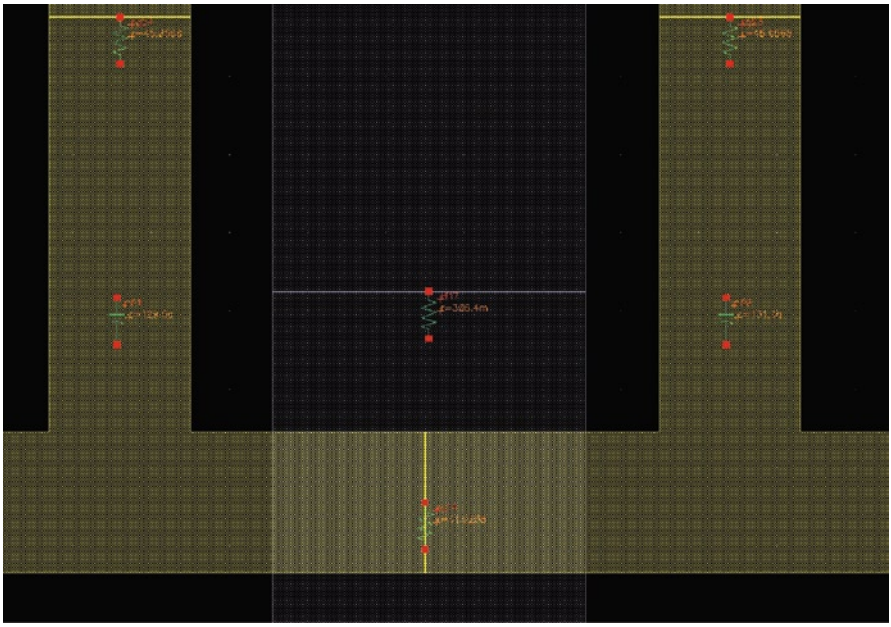

Fig. 4.16 Screenshot of parasitics in MOSFET layout having 10 fingers in TS-OPAMP layout design

Fig. 4.17 Screenshot of parasitics identified in layout of compensation capacitor

4.2.3 Summary and Results

The DRC clean and LVS match layout design of TS-OPAMP obtained have parasitics that affect the function of the design. Post layout simulation using the generated SPICE netlist for the design is carried out in LTspice to verify the specification parameters. The layout design has approximately 67 Resistances and 68 Capacitance parasitics. The area of the layout of TS-OPAMP is calculated as follows:

$$\text{Approximate Height of the Cell (H)} = 10\mu\text{m}$$

$$\text{Approximate Width of the Cell (W)} = 12\mu\text{m}$$

$$\text{Area} = \text{H} \times \text{W} = 10\mu\text{m} \times 12\mu\text{m} = 120\mu^2\text{m}^2$$

The total area used by the TS-OPAMP layout designed cell including unused area is approximately **120 μ^2m^2**

The layout can be improved by meticulously planning the placement of MOSFETs to obtain optimized area with least parasitics. The unused area in the design can be effectively used to reduce the area metrics for the layout design. The width of the OPAMP cell is an arbitrary value as there is no reference cell with least width available. This applies also to the height of the OPAMP.

Appendix

A. SPICE code to verify Open loop gain, Phase margin and Bandwidth using Bode plot for the OPAMP

```
* SPICE code to extract DC Gain, Phase Margin of
* Two Stage Unbuffered OPAMP @ Open Loop Configuration

.include 180nm_model.txt

M1 D13 GND SS  SS  nmos L=0.18u W=1.44u
M2 D24 Vp  SS  SS  nmos L=0.18u W=1.44u
M3 D13 D13 VDD VDD pmos L=0.18u W=0.72u
M4 D24 D24 VDD VDD pmos L=0.18u W=0.72u
M5 SS  CS  VSS VSS nmos L=0.18u W=0.4u
M6 Vo  D24 VDD VDD pmos L=0.18u W=9.72u
M7 Vo  CS  VSS VSS nmos L=0.18u W=1.44u
M8 CS  CS  VSS VSS nmos L=0.18u W=0.4u

C1 Vo  D24 3p
C2 Vo  GND 10p

I1 VDD CS 30u

R1 Vo  GND 100k

VDD VDD GND  2.5
VSS VSS GND -2.5

* Offset Voltage to adjust the output of OPAMP "0V" for
* Input voltage of 0V
VOF Vof  Vp 92m


* Verifying Input Offset Voltage @
*Vin Vof GND 0
*.dc Vin 0 .5 10m

* Openloop gain (Av), Phase Margin @ Unity Gain (0db) and 3db
Vin Vof GND sine(0 1 1k 0 0 0 20) AC 1
.ac lin 1k 1 10000k

.END
```

B. SPICE code to verify ICMR for the OPAMP

```
* SPICE code to extract ICMR for
* Two Stage Unbuffered OPAMP @ Unity Gain
  Feedback Configuration

.include 180nm_model.txt

M1 D13 Vo  SS  SS  nmos L=0.18u W=1.44u
M2 D24 Vp  SS  SS  nmos L=0.18u W=1.44u
M3 D13 D13 VDD VDD pmos L=0.18u W=0.72u
M4 D24 D24 VDD VDD pmos L=0.18u W=0.72u
M5 SS  CS  VSS VSS nmos L=0.18u W=0.4u
M6 Vo  D24 VDD VDD pmos L=0.18u W=9.72u
M7 Vo  CS  VSS VSS nmos L=0.18u W=1.44u
M8 CS  CS  VSS VSS nmos L=0.18u W=0.4u

C1 Vo  D24 3p
C2 Vo  GND 10p

R1 Vo  GND 10k


I1 VDD CS 30u

VDD VDD GND  2.5
VSS VSS GND -2.5

* ICMR: Range for which the Gain is unity
* Linear curve range
Vin Vp GND 0
.DC Vin -3 3 .1

.END
```

C. SPICE code to verify Input offset voltage and output impedance for the OPAMP

```
* SPICE code to extract Input Offset Voltage, Output
  Impedence of
* Two Stage Unbuffered OPAMP @ Open Loop Configuration

.include 180nm_model.txt

M1 D13 GND SS  SS  nmos L=0.18u W=1.44u
M2 D24 Vp  SS  SS  nmos L=0.18u W=1.44u
M3 D13 D13 VDD VDD pmos L=0.18u W=0.72u
M4 D24 D24 VDD VDD pmos L=0.18u W=0.72u
M5 SS  CS  VSS VSS nmos L=0.18u W=0.4u
M6 Vo  D24 VDD VDD pmos L=0.18u W=9.72u
M7 Vo  CS  VSS VSS nmos L=0.18u W=1.44u
M8 CS  CS  VSS VSS nmos L=0.18u W=0.4u

C1 Vo  D24 3p
C2 Vo  GND 10p

I1 VDD CS 30u

R1 Vo  GND 100k

VDD VDD GND  2.5
VSS VSS GND -2.5


* Input Offset Voltage: Input voltage for which Vo is
  Zero Vin Vp GND 0
.DC Vin -3 3 0.1
.measure DC IOV when V(vo)=0

* Transfer Function and Output Impedence
*V2 Vp GND sine(0 1m 1k 0 0 0 20)
*.TF V(Vo) V2


 .END
```

D. SPICE code to verify Power dissipation for the OPAMP

```
* SPICE code to extract Power Dissipated by
* Two Stage Unbuffered OPAMP @ Unity Gain
  Feedback Configuration

.include 180nm_model.txt

M1 D13 Vo  SS  SS  nmos L=0.18u W=1.44u
M2 D24 GND  SS  SS  nmos L=0.18u W=1.44u
M3 D13 D13 VDD VDD pmos L=0.18u W=0.72u
M4 D24 D24 VDD VDD pmos L=0.18u W=0.72u
M5 SS  CS  VSS VSS nmos L=0.18u W=0.4u
M6 Vo  D24 VDD VDD pmos L=0.18u W=9.72u
M7 Vo  CS  VSS VSS nmos L=0.18u W=1.44u
M8 CS  CS  VSS VSS nmos L=0.18u W=0.4u

C1 Vo  D24 3p
C2 Vo  GND 10p

R1 Vo  GND 10k

I1 VDD CS 30u

VDD VDD GND  2.5
VSS VSS GND -2.5

* Power Dissipation = (I5+I7)*(2.5 + |-2.5|)
.tran 1u 10u
.measure TRAN I5 FIND Id(M5) AT=5u
.measure TRAN I7 FIND Id(M7) AT=5u
.measure TRAN Pd   PARAM (I5+I7)*5

.END
```

E. SPICE code to verify Slew rate for the OPAMP

```
* SPICE code to extract Slew Rate
* Two Stage Unbuffered OPAMP @ Unity Gain Feedback

.include 180nm_model.txt

M1 D13 Vo  SS  SS  nmos L=0.18u W=1.44u
M2 D24 Vp  SS  SS  nmos L=0.18u W=1.44u
M3 D13 D13 VDD VDD pmos L=0.18u W=0.72u
M4 D24 D24 VDD VDD pmos L=0.18u W=0.72u
M5 SS  CS  VSS VSS nmos L=0.18u W=0.4u
M6 Vo  D24 VDD VDD pmos L=0.18u W=9.72u
M7 Vo  CS  VSS VSS nmos L=0.18u W=1.44u
M8 CS  CS  VSS VSS nmos L=0.18u W=0.4u

C1 Vo  D24 3p
C2 Vo  GND 10p

R1 Vo  GND 10k

I1 VDD CS 30u

VDD VDD GND  2.5
VSS VSS GND -2.5

* Slew Rate: [d(Vo)/Vin]/d(t) V/us
V2 Vp GND pulse(-1 1 0 .1n .1n 10u 20u)
.measure TRAN V2 FIND V(vo) AT=100.23u
.measure TRAN V1 FIND V(vo) AT=100.01u
.tran 1u 200u

.END
```

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