Chapter 2
Design Metrics of SRAM Bitcell

2.1 Standard 6T SRAM Bitcell: An Overview

This section gives a brief overview of the standard six-transistor (6T) SRAM bitcell and its operation. A standard 6T SRAM bitcell consists of two identical CMOS inverters (INV-1 and INV-2) connected in a positive feedback loop. It forms a basic unit, that is, a flip-flop or latch to create a bi-stable circuit allowing the storage of one-bit of information, either '1' or '0'. The internal nodes (Q and QB) of the bitcell always contain complementary values, as shown in Fig. 2.1. The cross-coupled inverter pair itself consists of two PMOS pull-up devices (M_3 and M_5) and two NMOS pull-down devices (M_4 and M_6). Two NMOS pass-gate or access devices (M_1 and M_2), which are controlled by the wordline (WL), serve as switches between the inverter pair and the complementary pair of bitlines (BL, BLB) also called datalines, used to read in or write to the bitcell, as shown in Fig. 2.1. The data in SRAM bitcell is stored as long as the power is maintained to the bitcell. The cross coupled inverter pair can be in one of the two stable states of an SRAM bitcell, which corresponds to the data stored '1' and '0', as shown in Fig. 2.2a, b, respectively. The basic operations of a bitcell as a storage device are reading or writing new data to the bitcell.

The read and write operations in a standard 6T SRAM bitcell are performed in the following ways.

2.1.1 Read Operation

Without loss of generality, it is assumed that the internal data storage nodes Q and QB are at '0' and '1', respectively, which correspond to Fig. 2.2b. To read the bitcell contents, the following sequence of steps are performed:

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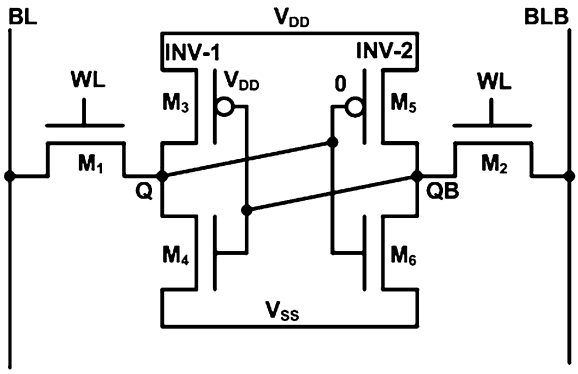


Fig. 2.1 Schematic diagram of a standard 6T SRAM bitcell. Internal data storage node Q at '0' and QB at '1'

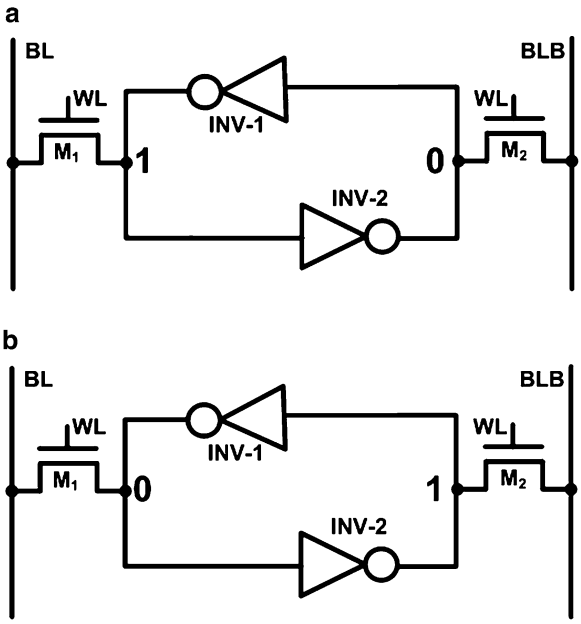


Fig. 2.2 Standard 6T SRAM bitcell under different stable states. (**a**) SRAM bitcell '1' stored. (**b**) SRAM bitcell '0' stored

- Conventionally to read a bitcell, the bitlines (BL and BLB) are precharged to the supply voltage (V_{DD}). In some SRAM designs these bitlines are precharged to intermediate level of 0 and V_{DD}.
- The wordline (WL) is asserted to high.
- Rise the WL from '0' to '1', result, one of the bitcell sides (node) stores the logical '0'; that side of the bitline is discharged through the pass-gate and pull-down transistors. In standard 6T, as shown in Fig. 2.1, devices M_1 and M_4 discharges the precharged bitlines BL.
  - If BLB goes to low (or discharges), then the bitcell holds a logic '1' value, which correspond to Fig. 2.2a.

  - If BL goes to low (or discharges), then the bitcell holds a logic '0' value, which correspond to Fig. 2.2b.

- Depending upon whether the bitline BL or BLB is discharged, the bitcell is read as a logical '1' or '0'. A sense amplifier converts the differential signal exists on BL and BLB to a logic-level output.
- De-assert the wordline (WL) back to 0.

During a read operation, the internal node (say Q) of the bitcell that holds a logical '0' will pull its bitline (BL) low through the pass-gate transistor, M_1 and pull-down transistor, M_4. It is important that the low internal node (Q) should not rise above the trip-point (switching threshold voltage) of the inverter INV-2, as shown in Fig. 2.1, to avoid a destructive read operation. A destructive read operation can be prevented by ensuring a large enough bitcell ratio (β), in other words, pull-down transistors (M_4 and M_6) must be stronger than the access transistors (M_1 and M_2). For a symmetric bitcell, bitcell ratio (β) is defined as:

$$\beta = \frac{W_4/L_4}{W_1/L_1} = \frac{W_6/L_6}{W_2/L_2} \tag{2.1}$$

In general, the bitcell ratio can be varied from 1.25 to 2.5 depending on the target application and desired static noise margin (SNM). A larger bitcell ratio makes the bitcell robust and provides higher SNM and read current I_{read} (and hence – the speed), at the expense of increased silicon overhead and leakage current. A smaller bitcell ratio, whilst maintaining an adequate speed and noise margin, makes the bitcell compact for a high density cache design but more vulnerable to process variation induced failures.

2.1.2 Read SNM Measurement

The best measure to quantify the stability of an SRAM bitcell during the read cycle and in hold state is the Static Noise Margin (SNM). The SNM is defined as the maximum amount of DC noise (V_N) that can be tolerated by the cross-coupled inverter pair such that the bitcell retains its data [94]. The read SNM is extracted from the read voltage transfer characteristics (VTC). The read VTC can be measured by sweeping the voltage at the data storage node Q (or QB) with both bitlines (BL, BLB) and wordline (WL) biased at V_{DD} while monitoring the node voltage at QB (or Q).

Figure 2.3 shows a conceptual schematic diagram of the bitcell for the SNM definition. The bitlines (BL and BLB) induced noise is modeled with the two DC voltage noise sources (V_N), and they are introduced at each of the internal nodes

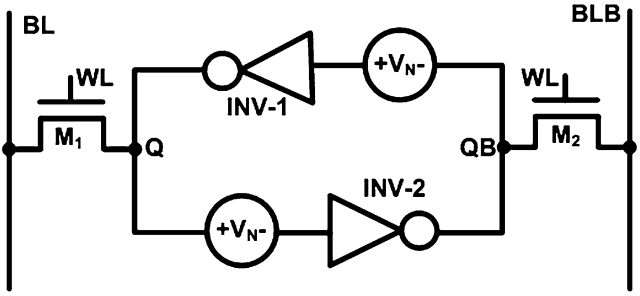


Fig. 2.3 Schematic diagram of a standard 6T SRAM bitcell showing the worst case polarity noise sources for modelling the static noise margin

in the bitcell in worst case polarity. As V_N increases the stability of the bitcell changes. The bitcell stability during active operation (read cycle) represents a more significant limitation to SRAM operation than the hold state. Specifically, at the onset of a read cycle, the wordline is activated and bitlines are precharged to V_{DD}. The internal storage node of the bitcell that represents a logic bit value '0' gets pulled upward through the access transistor due to voltage dividing phenomenon across the access transistors (M_1 and M_2) and pull down transistors (M_4 and M_6). This increase in voltage severely degrades the SNM during the read operation (read SNM), which is primarily determined by the ratio of the pull down transistor to access transistor, known as bitcell ratio.

As shown in Fig. 2.3, the noise sources are included with worst-case polarity to model the read SNM. When a worst case static noise is applied, this causes the inverse voltage transfer characteristics (VTC^{-1}) for INV-2 to move downward and the VTC of INV-1 to move to the right direction. Once both curves move by the SNM value, the meta-stable point coincides with one of the stable points and curves meet at only two points, as shown with dotted lines in Fig. 2.4. Any further noise applied to the VTC's has only one intersect point and the bitcell content flips. The voltage transfer characteristics (VTC's) and inverse VTC's (VTC^{-1}) of the two cross-coupled inverters during the read cycle are shown Fig. 2.4 for determining the worst case read SNM graphically. The SNM is estimated graphically as the length of a side of the largest square that can be embedded inside the lobes of the butterfly curve [94].

Apart from the read SNM obtained from the VTCs, the same phenomena can also be observed during transient read operation. Figure 2.5 shows the 6T SRAM bitcell read operation. The bitlines BL and BLB initially floated high. Without loss of generality, it was assumed that node Q is initially at '0' and thus QB is initially at '1'. When both the bitlines are pre-charged and word-line WL is enabled, BL should be pulled down through transistor M_1 and M_4, since both M_1 and M_4 form

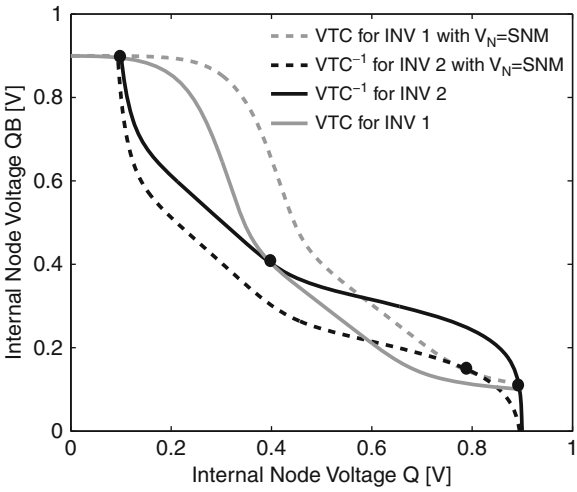


Fig. 2.4 The VTC's and inverse VTC's of the cross-coupled inverter pair during the read cycle for the estimation of worst case read SNM

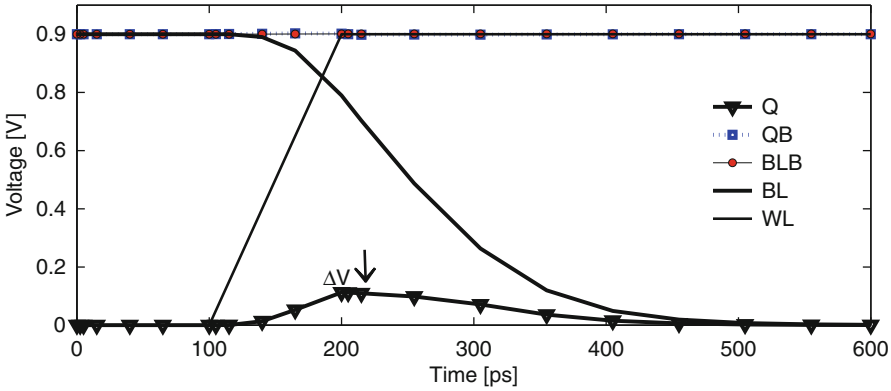


Fig. 2.5 The read operation of a standard 6T SRAM bitcell showing the stability constraint

a potential divider and raise node Q potential to ΔV. If node Q potential rises above the trip-point of inverter 2, as shown in Fig. 2.1, than there will be a read failure. This stability constraint is referred to as a 'read destructive operation'. In this case, wordline is kept high for longer period as a result bitline (BL) is pulled to ground, however, wordline pulse width is usually kept enough smaller that can develop a small differential voltage on the bitlines (BL and BLB). This small differential voltage overcomes the offset voltage of a sense amplifier in order to latch the correct data from the bitlines.

2.1.3 Write Operation

The write operation or flipping the bitcell contents when initially assuming that the internal data storage nodes Q and QB are at '0' and '1', respectively, as shown in Fig. 2.2b, consists of the following sequence of steps:

- Initially, wordline (WL) = 0.
- Precharge the bitlines (BL and BLB) to the supply voltage (V_{DD}).
- After prechrage, both the bitlines (BL and BLB) are disconnected from the supply voltage (V_{DD}).
- Wordline (WL) is activated to high (data enters the bitcell during this step).
- Place the data value on the BL and the complementary data value on BLB.
- The bitline BLB connected to the data storage node QB via M_2, is driven to the ground potential by a write driver through the M_2 pass-gate transistor, while the BL is remained held at V_{DD} to pull node Q to high via M_1 pass-gate transistor.
- As node Q and QB flip their states de-assert the wordline (WL) back to 0.

As a result, node QB pulled well below the trip-point of the INV-1, as shown in Fig. 2.1, so that, the feedback loop in the cross-coupled inverter starts to work and the bitcell is flipped. It is important that a successful write operation primarily depends upon the properly sized pass-gate transistors and pull-up transistors. Hence, the pull-up ratio (PR) for a symmetric SRAM bitcell is defined as:

$$PR = \frac{W_3/L_3}{W_1/L_1} = \frac{W_5/L_5}{W_2/L_2} \tag{2.2}$$

During write operation fight occurs between pass-gate transistors (M_1 and M_2) and pull-up transistors (M_3 and M_5) mainly when the value of the data to be written into the bitcell is the opposite of the value that is currently stored in the bitcell. For instance, assumed that the bitcell currently holds a logic '1' and it is intended to write a logic '0' into the bitcell. Then, the situation correspond the following biasing conditions; BLB, WL and bitcell supply voltage is biased at V_{DD} and BL is biased at V_{SS} in Fig. 2.2a. For a successful write operation, node QB must be pulled above the trip point of the inverter "INV1" and node Q must be pulled down below the trip-point of the inverter "INV2". In this mode, fight occurs between M_1 and M_3. Since M_1 will try to bring node Q to down while M_3 will try to keep node Q to high. Therefore, M_1 must win the fight for a successful write operation. Once an inverter switches, it creates a self-reinforcing positive feedback action that continue until the bitcell has been fully placed into a new stable state.

A successful write operation can be guaranteed by choosing a lower PR value (generally, PR = 1), that can be achieved by employing the wider or stronger pass-gate transistors (M_1 and M_2) instead of pull-up transistors (M_3 and M_5). However, increasing the width of the pass-gate transistors threatens the stability of the bitcell during the read cycle, or in other words reduces the read SNM of the bitcell.

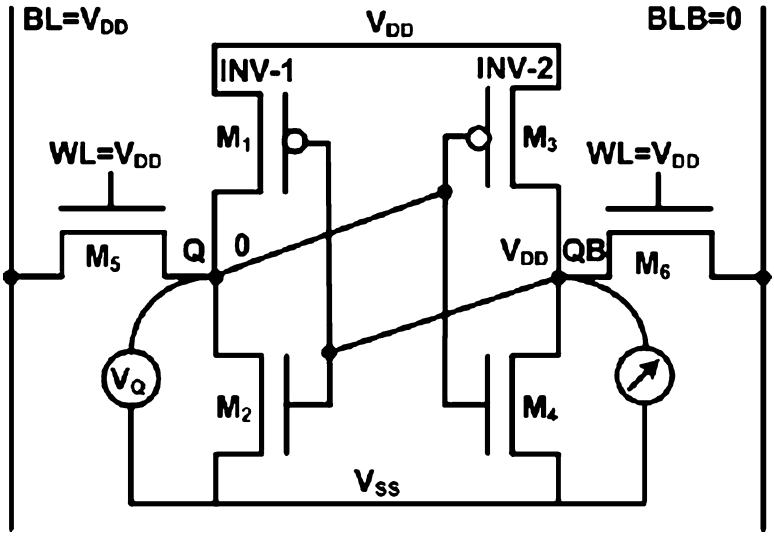


Fig. 2.6 Experimental set-up for extracting the write static noise margin

2.1.4 Write SNM Measurement

Figure 2.6 shows the experimental set-up for measurement of write static noise margin (WSNM). During write operation M_1 (or M_3) and M_5 (or M_6) form a resistive voltage divider for the falling BL (or BLB) and storage node Q (or QB). If the voltage divider pulls Q below the trip-point of inverter 2 (INV-2), a successful write operation occurs. The write-ability of a SRAM bitcell can be gauged by the write SNM [12, 13]. The write SNM is extracted by a combination of read voltage transfer characteristics (VTC) and the write VTC. The read VTC is measured by sweeping the voltage at the storage node QB while monitoring the node voltage at Q. The write VTC is measured by sweeping the voltage at the storage node Q with BL and WL biased at V_{DD} and BLB is biased at V_{SS} while monitoring the voltage at node QB. The WSNM can be quantified by the side of the smallest square fitted inside the read and write VTCs, as shown in Fig. 2.7. When WSNM fall negative, the read VTC and write VTC intersects each other suggesting the inability to write into the SRAM bitcell.

The write-ability of an SRAM bitcell can also be characterized by the write trip-point-voltage, which is defined as the maximum amount of voltage needed on the bitline to flip the bitcell content [36, 40]. The Write Static Noise Margin (WSNM) is measured through the write-trip point defined as the difference between V_{DD} and the maximum bitline voltage required to flip the data storage nodes Q and QB, as shown in Fig. 2.8.

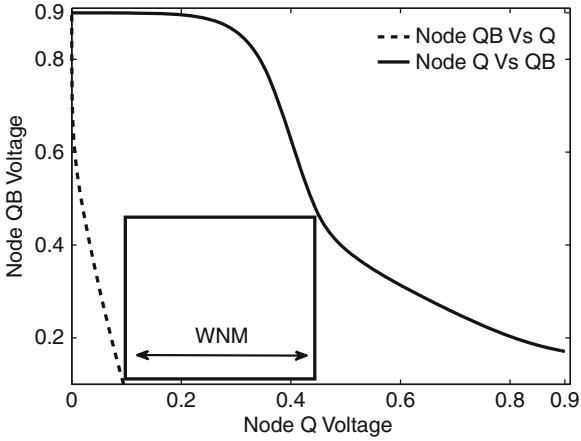


Fig. 2.7 Measurement of write static noise margin (WSNM) of an SRAM bitcell obtained from read and write VTCs

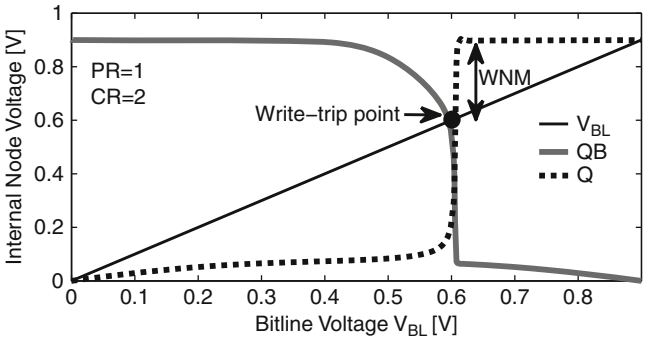


Fig. 2.8 The write noise margin (WNM) of an SRAM bitcell defined as write-trip point

2.1.5 Relationships Between Transistor Drive Strengths

A concern associated with the read operation is that both BL and BLB are kept high at the beginning of the read operation must not corrupt (un-intended flip) the value stored in the bitcell. In order to avoid the un-intended flip of the value, it is desirable to keep the voltage at the internal node which has a stored value of '0' from rising above the trip point of the inverter, i.e. more of the voltage drop between bitline and ground should occur across the access transistors (M_1 and M_2) than across the pull-down transistors (M_4 and M_6), refer Fig. 2.1. In other words, the strength of the access transistors should be less than the strength of the pull-down transistors for a non-destructive read operation.

Similarly, for a successful write operation, it is desirable to bring down the voltage of the internal data storage node Q (or QB) which has a stored value '1' below the trip point of the inverter, INV-2 (or INV-1), refer Fig. 2.1. Therefore, access

transistors (M_1 and M_2) must be stronger than the pull-up transistors (M_3 and M_5) for a successful write operation. Combining these constraints, yield the following relation:

strength(PMOS Pull-up) $<$ strength(NMOS Access) $<$ strength(NMOS Pull-down).

2.2 Other SRAM Bitcell Stability Metrics

In the recent past there has been substantial efforts were made to understand and model the stability of an SRAM bitcell. Many analytical models have been developed for the static noise margin (SNM) of an SRAM bitcell to optimize the bitcell design, to predict the effect of parameter variations on the SNM [95] and to access the impact of intrinsic parameter variations on the SRAM bitcell stability [10]. Some of the recent methods for measurement of SRAM stability are N-curve and bitline measurement techniques. SRAM stability metrics can broadly be classified into two categories: static and dynamic. In static SRAM stability metrics, a DC voltage is applied or swapped to estimate how much DC noise an SRAM bitcell can tolerate. The static stability metrics are further divided into two categories: conventional and large scale metrics, as shown in Fig. 2.9. Conventional metrics are based on butterfly curves and N-curves. These metrics require access of internal nodes of an SRAM bitcell for measurement of stability and provides limited data for stability analysis. Access of internal nodes of all the SRAM bitcells is not feasible because of metal spacing constraints and area overhead associated to provide switch array. On the other hand, large scale metrics do not require access of internal data storage nodes for stability analysis, therefore, these metrics are suitable for dense large scale SRAM designs. In theses metrics, measurement of stability is done by accessing the bitlines (BL or BLB), wordline (WL), and bitcell supply (V_{CELL}).

2.2.1 N-Curve Stability Metrics

The stability of an SRAM bitcell is commonly defined by the *SNM* as a maximum value of DC noise voltage that can be tolerated without changing the internal storage node state [1, 41, 103]. A successful data retention during hold and functional operations read and write are determined by hold *SNM*, read *SNM* and write trip voltage, respectively. These three metrics are widely used for design and performance analysis of SRAM bitcell but none of the metrics carry the *current flow* information which is having extensive importance. For example, in hold state the hold *SNM* is highly dependent on the driving capability of the pull down NMOS transistors, whereas read *SNM* is strongly dependent on the driving capability of the NMOS access and pull down transistors.

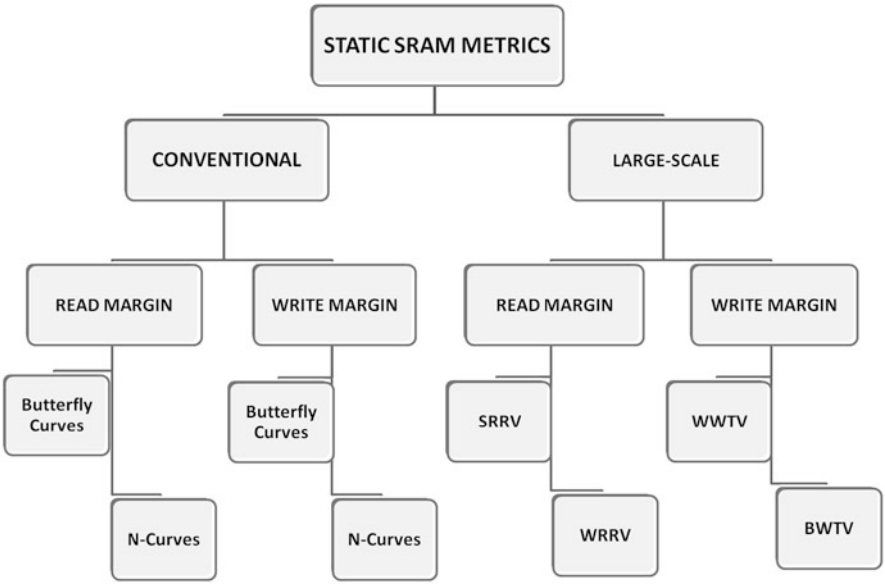


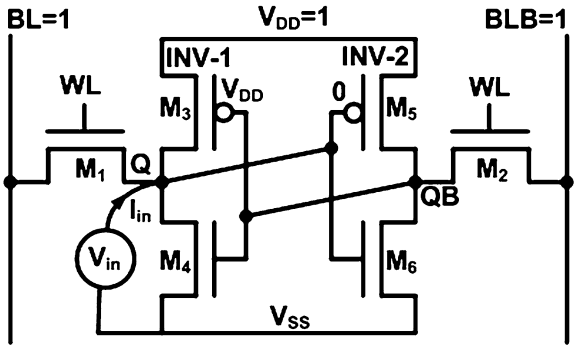
Fig. 2.9 Classification of static stability metrics of a standard 6T SRAM bitcell

The major drawbacks of *SNM* metric obtained from butterfly curves are as follows:

- The ideal voltage transfer characteristic (VTC) obtained from the butterfly curve delimits to a maximum $0.5V_{DD}$,
- Inability to measure it with a automatic inline tester, due to the fact that after measuring the butterfly curves of the bitcell, SNM still has to be derived by mathematical manipulations of the measured data,
- Inability to generate statistical information of SRAM failures, due to indirect availability of SNM, and
- Separate analysis is required for read and write stability measurement,
- It does not provide *current flow* information which is equally important for stability analysis.

An alternative approach for stability analysis that satisfies the above requirements is the use of N-curve for an SRAM design [114].

Figure 2.10 shows the experimental setup for extracting the N-curve of a standard 6T SRAM bitcell. The same setup can also be extended for other SRAM bitcell topologies. At the beginning of read access both bitlines (BL and BLB) are precharged to '1' and wordline is activated to '1'. Without loss of generality, it is assumed that the internal storage nodes QB and Q are at '1' and '0', respectively. A voltage sweep V_{in} from 0 to V_{DD} is applied at the node Q and corresponding current supplied by the sweep voltage source V_{in} is measured as I_{in}. The resulting relationship is plotted between V_{in} on x-axis and I_{in} on y-axis is



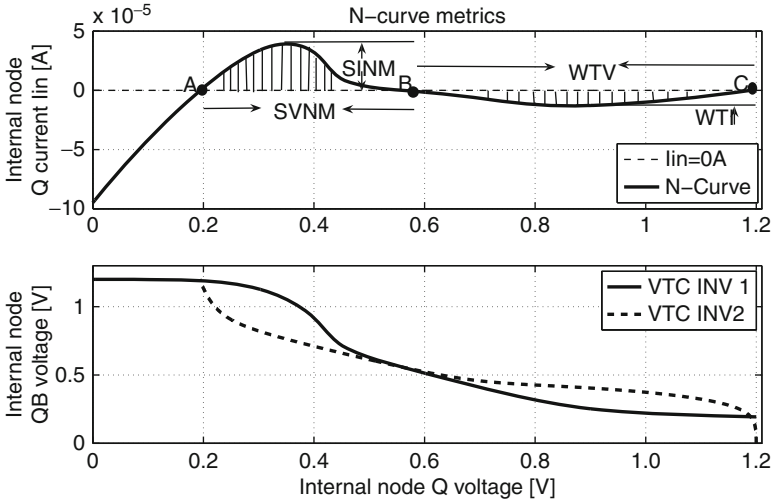


Fig. 2.10 Experimental set-up for extracting the N-curve of a standard 6T SRAM bitcell

Fig. 2.11 Extracted N-curve and corresponding butterfly curves for read operation of a standard 6T SRAM bitcell

called the N-curve, as shown in Fig. 2.11. As an attractive approach, N-curve contains information for both read stability and write stability. There is no need of mathematical manipulation on the measured data as N-curve directly provides the functional information of SRAM bitcell. N-curve contains information for both voltage and current. Thus, allowing a complete functional analysis of the SRAM bitcell stability for both read and write operations with only one N-curve. However, major limitations of the N-curve based stability analysis is that it also requires the access of internal nodes of the SRAM bitcell similar to butterfly curves.

The extracted N-curve has three intersection points A, B, and C; point A and C correspond to stable state points while point B is a meta-stable point, these points corresponds to the butterfly curves plotted below the N-curve, as shown in Fig. 2.11. At these points current supplied by the sweep voltage source V_{in} is zero. At the

beginning, when both V_{in} and node Q at 0 V, the access transistor M1 and transistor M4 are in velocity saturation and linear region, respectively. Therefore, drain current of M1 is larger than the drain current of M4. Thus, the difference of these currents according to Kirchoff's current law, I_{in} flows into the sweep voltage source in order to maintain node Q at 0 V. It can be observed in negative direction from origin to point A. When the difference of these currents is equal to 0 A (i.e. $I_{in} = 0$ A), which is corresponding to point A. The voltage at A is determined by the pull-down to access transistor ratio or bitcell ratio. Further increase in sweep voltage V_{in}, increases I_{in} as indicated by the change in sign and devices operation region remain unchanged up to SINM. The voltage at B is related to the pull-down to pull-up ratio and access transistors of the bitcell. At SINM, M4 moves from linear region to velocity saturation region. Between SINM and WTI, M3 is now active and working regions of all the devices M1, M4 and M3 moved to saturation region. At WTI, both M1 and M3 are in linear region while M4 moves from active to cut-off region. The voltage at C is defined by the pull-up to access transistor ratio or in other words pullup ratio of the bitcell. Read and write stability metrics are marked in different regions of the N-curve obtained from the SRAM bitcell.

2.2.2 Static Voltage and Current Metrics

The stability metrics derived from the N-curve are based on the combined voltage and current information for a SRAM bitcell. Figure 2.11 shows static voltage noise margin ($SVNM$), static current noise margin ($SINM$), write trip voltage (WTV), and write trip current (WTI). The $SVNM$ is defined as a maximum tolerable DC noise voltage at internal nodes of the bitcell before its content flips and it is measured as a voltage difference between point B and A. Similarly, $SINM$ can be defined as a maximum tolerable DC noise current injected at internal nodes of the bitcell before its content changes and it is measured as a peak current located between point A and B. These two metrics $SVNM$ and $SINM$ are used to characterize the bitcell read stability.

However, bitcell's write stability can be characterize the with the help of WTV and WTI. For this purpose N-curve has to be analyzed from right to left because for write operation, pulling down of precharged bit line (BLB) to ground so that the internal node QB get discharges. The WTV is the minimum voltage drop needed to change the internal nodes of the bitcell, which can be measured as a difference between point C and B. The WTI is defined as a minimum amount of the current needed to write the bitcell which can be measured as a negative current peak between point C and B as shown in Fig. 2.11. An overlap of points A and B or point B and C means the bitcell is at the edge of stability loss, as a result, destructive read operation can easily occur. Similarly, overlapping of these points may lead to failure in write operation.

2.2.3 Power Metrics

The N-curve as shown in Fig. 2.11 is used to derive the power metrics which includes both the voltage and current information for read stability and write stability. So, instead of using four metrics obtained from N-curve to analyze the stability of an SRAM bitcell, it would be easy to combine them in two power metrics, static power noise margin (*SPNM*) and wtite trip power (WTP) [97]. The *SPNM* is used to characterize the read stability which is measured as the area below the curve between point A and B. The *SPNM* is defined as the maximum tolerable DC noise power by the internal data storage nodes of the bitcell before its content changes. Furthermore, as the shaded part of N-curve between point A and B has formally a unit of power which is given by Eq. 2.3,

$$SPNM = \frac{1}{B-A} \sum_{n=A}^{n=B} I_{in}(n) * V_{in}(n). \tag{2.3}$$

The WTP, characterizes the write stability of a bitcell and which is measured as the area above the curve between point B and C. The WTP is defined as the minimum amount of power required to flip the data storage nodes and which is given by Eq. 2.4:

$$WTP = \frac{1}{C-B} \sum_{n=B}^{n=C} I_{in}(n) * V_{in}(n), \tag{2.4}$$

where V_{in} is the sweep voltage source and I_{in} is the current supplied by the V_{in}. The successful write in the bitcell is quantified with the help of this metric. From Fig. 2.11 it is clear that for a successful read and write operations *SPNM* should be positive (i.e. $SPNM > 0$) and WTP should be negative (i.e. $WTP < 0$).

2.2.4 Dependencies of SPNM and WTP

The stability of the bitcell degrades with lowering supply voltage V_{DD}, minimum bitcell size and process variability which will limit advanced technology node to operate at lower voltage due to degraded read *SNM* and reduced write margin. Read *SNM* degradation results in destructive read operation whereas reduced write margin cause unsuccessful write operation. To observe the dependency of different parameters, SPICE simulation results are presented in this section for a standard 6T SRAM bitcell, these results are based on the predictive technology model (PTM) 65 nm node.

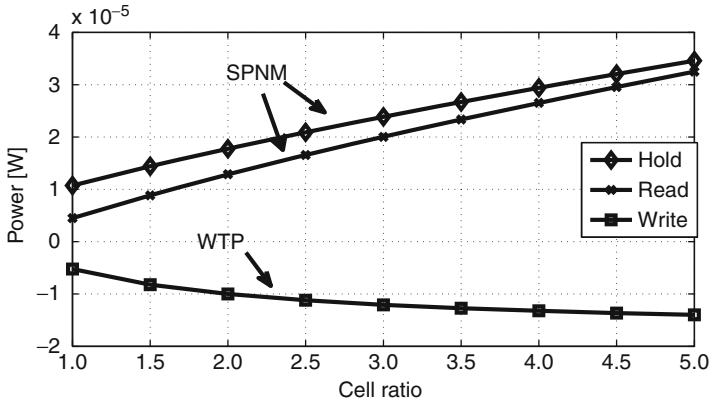


Fig. 2.12 Cell ratio dependency of SPNM and WTP at $V_{DD} = 1.2\,\text{V}$

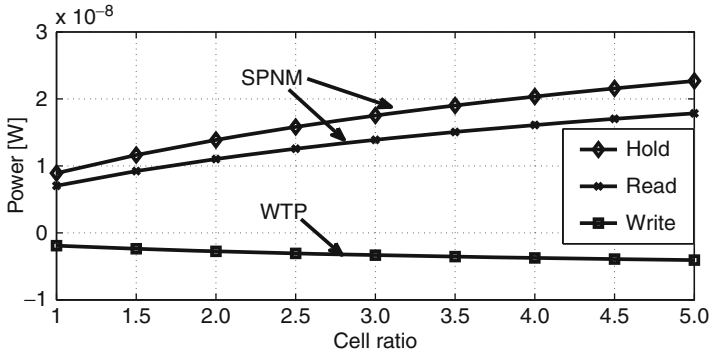


Fig. 2.13 Cell ratio dependency of SPNM and WTP at $V_{DD} = 0.3\,\text{V}$

2.2.5 Dependence on the Bitcell Ratio

The stability as well as the size of the SRAM bitcell is primarily determined by the bitcell ratio, which is the defined as the ratio of pull down transistor's (W/L) to the access transistor's (W/L). Figure 2.12 shows the impact of bitcell ratio on *SPNM* and WTP at $V_{DD} = 1.2\,\text{V}$ during hold, read and write operations. As shown in Fig. 2.12, the *SPNM* is almost linearly increases with the bitcell ratio. The linear dependence of *SPNM* on bitcell ratio is because of the drain current of the pull down transistors and access transistors increases linearly with the bitcell ratio. Figure 2.13 shows that the bitcell ratio has clear impact on *SPNM* at subthreshold $V_{DD} = 0.3\,\text{V}$ during hold, read and write operations. In subthreshold, the dependence of *SNM* obtained from the butterfly curve has very little (unnoticeable) impact of bitcell ratio [17]. However, power metric *SPNM* and WTP obtained from N-curve at subthreshold $V_{DD} = 0.3\,\text{V}$ shows the consistent trend as it is at $V_{DD} = 1.2\,\text{V}$. Hence, the

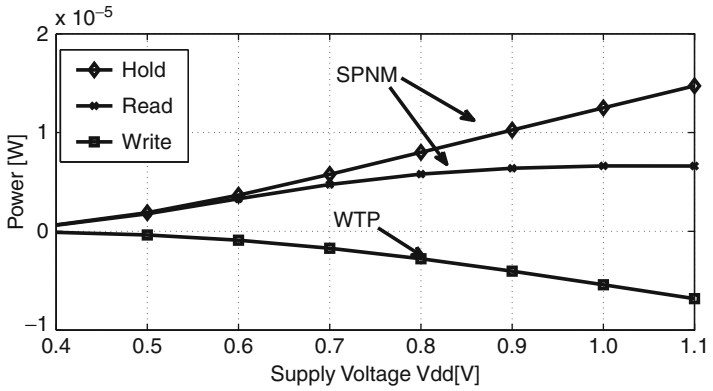


Fig. 2.14 Supply Voltage V_{DD} dependency of SPNM and WTP

proposed metrics provides better information compare to *SNM* at ultra low voltage and can be useful for stability analysis under subthreshold regime.

2.2.6 Dependence on the Supply Voltage V_{DD}

The *SNM* obtained from the VTC delimits to a maximum $0.5V_{DD}$ because of the two sides of the butterfly curve [17]. Figure 2.14 shows the dependence of power metrics *SPNM* and WTP on V_{DD} for a standard 6T-SRAM bitcell. The power metrics *SPNM* and WTP for hold, read and write operations reveals that V_{DD} scaling no longer limits the SRAM bitcell stability to the ideal value of $0.5V_{DD}$. Thus, the proposed metrics dependency on V_{DD} as shown in Fig. 2.14 will not limit the stability analysis and can be used at a very low voltage.

2.3 Bitline Measurement Design Metrics

The conventional DC read and write static noise margin (SNM) metrics presented in the previous section have some major drawbacks such as inability to measure them in dense functional SRAM arrays due to metal spacing constraints and area overhead associated to provide switch array. As a result, it produces inadequate number of data points for failure analysis of large size cache memories. In bitline measurement, SRAM read and write stability is characterized by accessing only the bitlines, wordline, and the bitcell supply voltages [38]. It increases the number of data points for failure analysis, while the SRAM array kept intact. Bitline measurement can be used for analysing the functional stability of an SRAM bitcell for read and write operations. In contrast to butterfly curve based stability

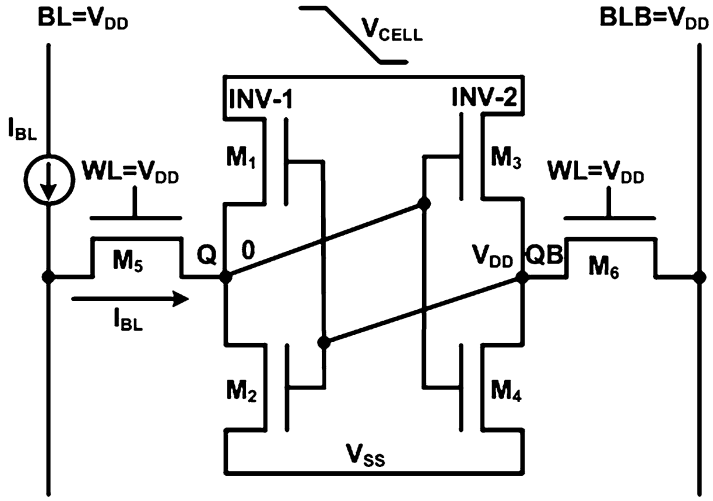


Fig. 2.15 Schematic diagram for extracting the supply read retention voltage (SRRV)

analysis, bitline measurement directly provides the functional stability without mathematically manipulating the measured data. Bitline measurement has also been previously applied to detect and isolate the faulty SRAM bitcells in cache memory array [116].

2.3.1 Read Stability Measurement

Supply Read Retention Voltage (SRRV): The read stability of an SRAM array can also be measured in terms of SRRV. For read stability measurement, both bitlines (BL and BLB) are kept floating around V_{DD} while the wordline (WL) is driven high, and the bitcell state is retained by keeping the bitcell supply sufficiently high. Therefore, SRAM bitcell read stability in functional SRAM array can be gauged by the minimum bitcell supply needed for data retention during read operation, which is referred as the supply read retention voltage (SRRV).

Figure 2.15 shows the schematic setup for extracting the SRRV. To extract the read stability using SRRV, both bitlines (BL and BLB) are tied to V_{DD} and wordline is also driven to operating voltage V_{DD} to emulate the read operation. The bitline (BL) current, I_{BL}, is monitored at the '0' storage node, while ramping down the SRAM bitcell supply (V_{CELL}) voltage. When the V_{CELL} is ramped down sufficiently low, the SRAM bitcell loses its stability for data retention and makes nodes Q and QB monostable. At this point, M_5 dominates M_2 so that node Q, originally holding '0' rises above the trip point of inverter (INV-2) and flips the bitcell state. It is also signified by the sudden drop in bitline current, I_{BL}, as shown in Fig. 2.16. Sudden

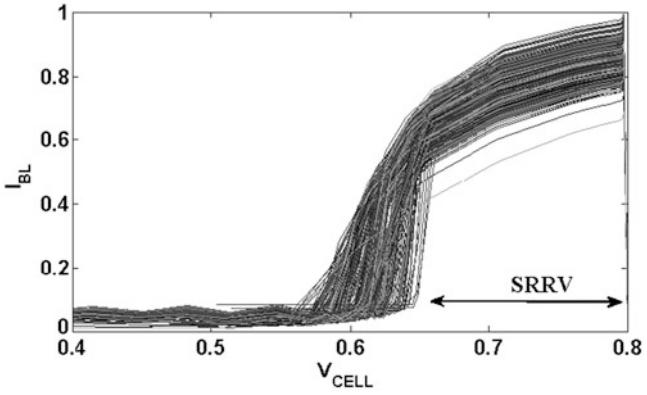


Fig. 2.16 Definition of SRRV from the measured transfer characteristics between I_{BL} and V_{CELL}. The bitcell supply (V_{CELL}) voltage is ramped below the V_{DD} causes sudden drop in bitline current

drop in I_{BL} is mainly due to rise in the potential of node Q storing '0' when it reaches to meta-stable state or bitcell state flips due to drop in V_{CELL}.

The transfer characteristics plotted between I_{BL} versus V_{CELL}, are shown Fig. 2.16 for measurement of SRRV. The SRRV of an SRAM bitcell can be defined as the difference between V_{DD} and the value of the V_{CELL} causing I_{BL} to suddenly drop, as shown in Fig. 2.16. Initially, when $V_{CELL} = V_{DD}$ (i.e. SRRV = 0), the SRAM bitcell is biased for a nominal read operation with BL, BLB, WL and V_{CELL} all are biased at V_{DD}. If the SRRV is greater than zero, it indicates that bitcell supply voltage (V_{CELL}) can be dropped below V_{DD} without disturbing the bitcell state. Therefore, SRRV represents the maximum tolerable DC noise voltage at the bitcell supply before causing the destructive read operation.

Wordline Read Retention Voltage (WRRV): During read or write operation, wordline is driven high causes read stress to SRAM bitcells having direct read access and all the unaccessed SRAM bitcells. This read stress can be further exacerbated by boosting the wordline voltage above the V_{DD}. Hence, the read stability of an SRAM bitcell can also be measured from the largest wordline boost without flipping the bitcell contents, defined as word line read retention voltage (WRRV).

Figure 2.17 shows the schematic setup for extracting the WRRV. To extract the read stability using WRRV, both bitlines (BL and BLB) are tied to V_{DD} and bitcell supply (V_{CELL}) is also driven to operating voltage V_{DD} to emulate the read operation. The bitline (BL) current, I_{BL}, is monitored at the '0' storage node, while ramping up the wordline voltage above the supply voltage (V_{DD}). However, keeping the wordline voltage below the gate-oxide breakdown voltage set by the technology. When the wordline voltage is boosted adequately high above V_{DD}, the SRAM bitcell state is flipped due to an exacerbated read stress which causes M_5 to dominate over M_2, so that node Q, originally holding '0' rises above the trip point of inverter (INV-2) and flips the bitcell state. It is also signified by the sudden drop in bitline

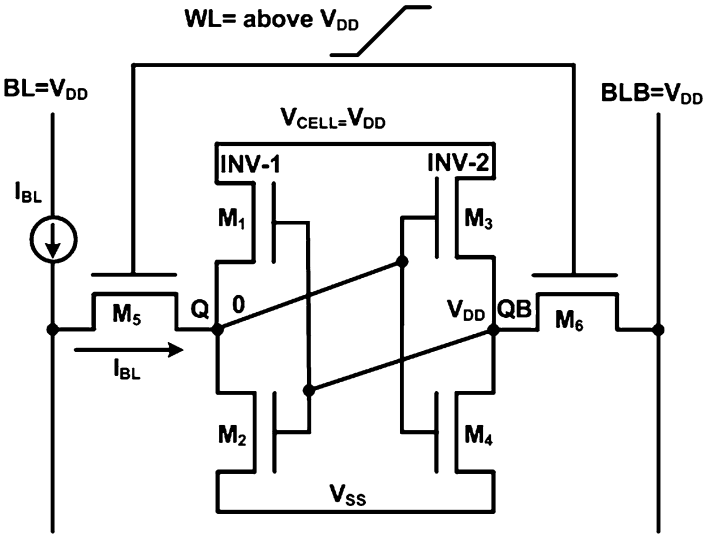


Fig. 2.17 Schematic diagram for extracting the wordline read retention voltage (WRRV)

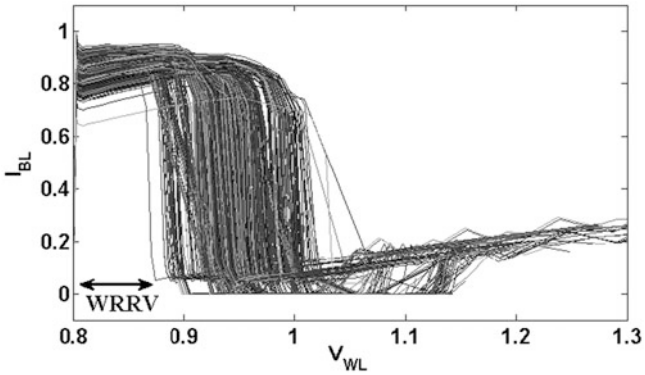


Fig. 2.18 Definition of WRRV from the measured transfer characteristics between I_{BL} and V_{WL}. The wordline voltage (V_{WL}) is ramped above the supply voltage causes sudden drop in bitline current

current, I_{BL}, as shown in Fig. 2.18. This phenomena is observed due to the potential drop between BL and node Q when rising wordline potential causes the bitcell to meta-stable state or bitcell state flips.

The transfer characteristics plotted between I_{BL} versus V_{WL}, are shown Fig. 2.18 for measurement of WRRV. The WRRV of an SRAM bitcell can be defined as the difference between V_{DD} and the boost in the wordline voltage causing I_{BL} to suddenly drop, as shown in Fig. 2.18. Initially, when $V_{WL} = V_{DD}$ (i.e. WRRV = 0), the SRAM bitcell is biased for a nominal read operation with BL, BLB, WL and

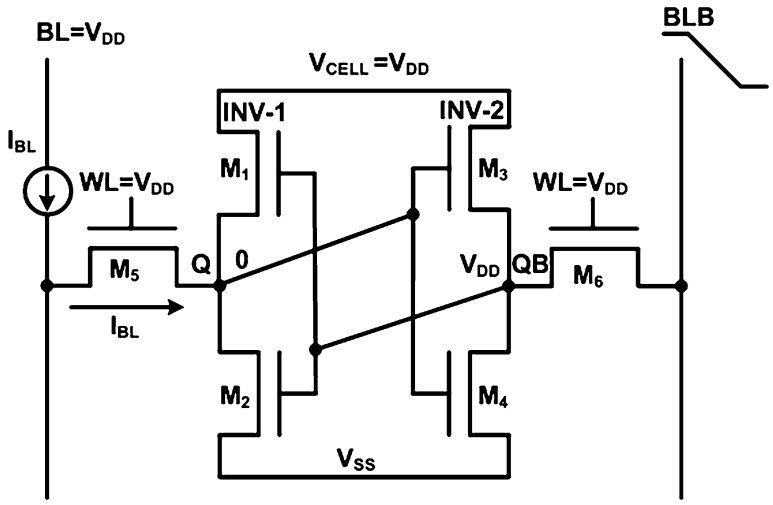


Fig. 2.19 Schematic diagram for extracting the bitline write trip voltage (BWTV)

V_{CELL} all are biased at V_{DD}. If the WRRV is greater than zero, it indicates that wordline can be boosted above V_{DD} without disturbing the bitcell state. Therefore, WRRV represents the maximum tolerable DC noise voltage at the wordline before causing the destructive read operation.

2.3.2 Writeability Measurement

Bitline Write Trip Voltage (BWTV): Figure 2.19 shows the schematic setup for extracting the BWTV. The bitcell is configured according to the new data which has to be written under write operation. In this scenario, bitline (BL) and wordline (WL) are tied to V_{DD} while complement bitline (BLB) voltage, V_{BLB} is ramped from V_{DD} to ground potential to emulate the write cycle. The writeability of an SRAM bitcell in a functional SRAM array can be gauged by the maximum bitline voltage (V_{BLB}) at the '1' storage node (QB), able to flip the bitcell state during a write cycle [33, 34, 37, 41]. To extract the BWTV of an SRAM bitcell, the bitcell supply (V_{CELL}), BL and WL are biased at V_{DD}. The bitline current (I_{BL}) is monitored while ramping down the bitline (V_{BLB}) voltage. As the V_{BLB} dropped low enough, the pass-gate M_6 overcome M_3 and the node QB is dropped below the trip-point of inverter, INV-1. As a result, a successful write operation is observed which is signified by the sudden drop in I_{BL}, as shown in Fig. 2.20. The BWTV is quantified from the transfer charactristics of I_{BL} versus V_{BLB}, as the V_{BLB} dropped low that causes the sudden fall in I_{BL}. When BWTV is zero (BWTV $= 0$) the SRAM bitcell is biased for a nominal write operation. If the BWTV is greater than zero,

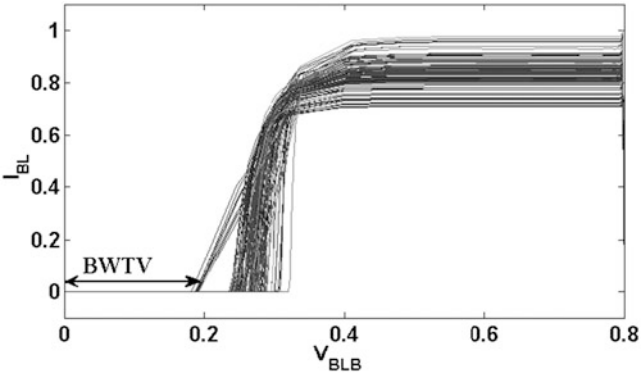


Fig. 2.20 Definition of BWTV from the measured transfer characteristics between I_{BL} and V_{BLB}. The complement bitline (V_{BLB}) voltage is ramped down the supply voltage causes sudden drop in bitline current

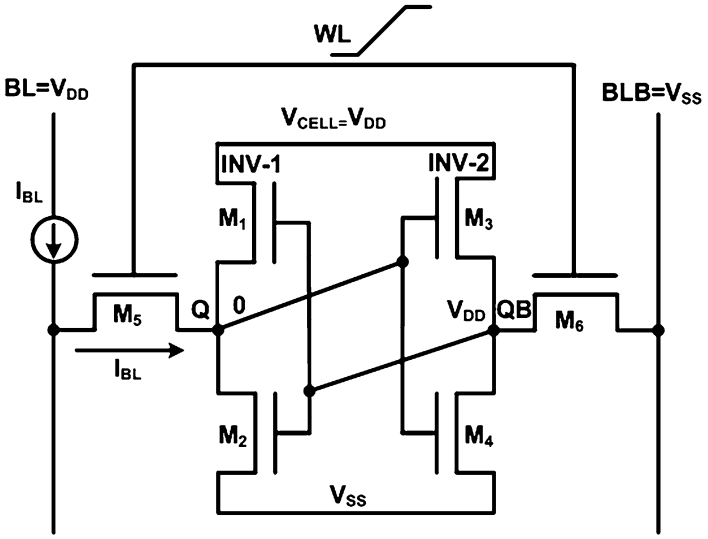


Fig. 2.21 Schematic diagram for extracting the wordline write trip voltage (WWTV)

it indicates that bitline voltage (V_{BLB}) can be dropped below V_{DD} for a successful write operation. Therefore, BWTV represents the maximum tolerable DC slack on the bitline to successfully write the bitcell.

Wordline Write Trip Voltage (WWTV): The WWTV is defined as the minimum wordline voltage needed to flip the bitcell content during a write cycle and it can be used to gauged the writeability of an SRAM bitcell in an SRAM array. Figure 2.21 shows the schematic setup for extracting the WWTV by first configuring the bitlines to write the data and then ramping the wordline. The bitcell supply (V_{CELL}) and BL

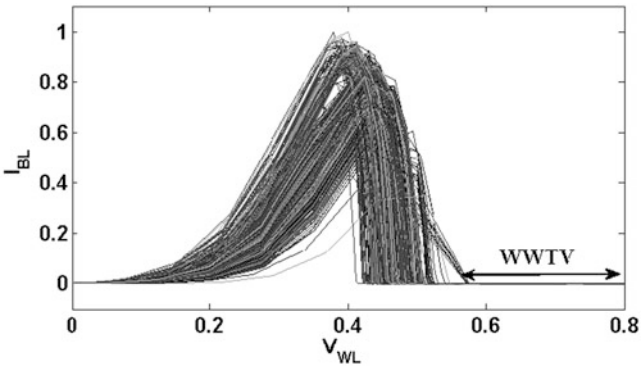


Fig. 2.22 Definition of WWTV from the measured transfer characteristics between I_{BL} and V_{WL}. The wordline (V_{WL}) voltage is ramped down the supply voltage causes sudden drop in bitline current

are biased at V_{DD} while BLB is biased and V_{SS}. The bitline current (I_{BL}) at the '0' storage node (Q) is monitored while ramping up the wordline (WL) voltage. As wordline voltage ramped high, the monitored current initially resembles the I_D-V_G charactristics of pass-gate transistor M_5. When the ramped up voltage of the WL is sufficiently high, the bitcell content flips, signified by the sudden drop in the I_{BL} magnitude as shown in Fig. 2.22.

The WWTV is quantified from the transfer charactristics of I_{BL} versus the V_{WL} voltage, as shown in Fig. 2.22. The WWTV is defined as the difference of V_{DD} and the V_{WL} voltage which causes the sudden drop in the I_{BL}. When WWTV $= 0$, the SRAM bitcell is biased for a nominal write operation with WL, BL and V_{CELL} are biased at V_{DD} and BLB is biased at V_{SS}. If the WWTV is greater than zero, it indicates that wordline voltage can be dropped below V_{DD} for a successful write operation. Therefore, WWTV represents the maximum tolerable DC slack on the wordline to successfully write the bitcell.

2.4 Dynamic Stability Analysis

Static stability analysis has been extensively used to characterize the SRAM bitcell failures. The most commonly used failure criteria are SNM for read failure and WNM for write failure [12, 95]. All (SNM, WNM and N-curve) static failure analysis are steady state in nature and assume the wordline (WL) is turned ON indefinitely and the bitlines (BL and BLB) are driven to V_{DD} indefinitely. These metrics are known to be optimistic in write stability and pessimistic in read stability from comparison between static and actual dynamic access [55, 82, 105, 117]. The read SNM is usually overestimates the read failure. For example, an unstable bitcell

might not have enough time to flip with a finite WL pulse width for a noise magnitude larger or equal to SNM. Similarly, WNM usually underestimates the write failure. It is due to the fact that a bitcell might be too slow to be written in a finite duration of the WL pulse width even with a bitline voltage is larger or equal to WNM. It is well known that both SNM and WNM, in general, are not capable of capturing different effects such as coupling, charge sharing, transient, and other dynamic bitcell behaviour under read and write operations. Therefore, dynamic stability analysis of a SRAM bitcell is must to determine the functionality or a successful read and write operation in time domain.

2.4.1 Dynamic Read Stability

Figure 2.23a shows an SRAM bitcell under read access for different pulse widths T_A and T_B. It illustrates the importance of pulse width during read access and shows that how insufficient pulse width can lead to latch a wrong value. The schematic setup for simulation of read access is shown in Fig. 2.23a in which bitlines are precharged to V_{DD} before the read access cycle and wordline is active high during read access. In Fig. 2.23b, wordline pulse width T_A is too short, therefore, bitline capacitance is not discharged sufficiently to overcome the offset in the sense amplifier. As a result, wrong value is latched by the sense amplifier. Similarly, a successful read access operation is shown in Fig. 2.23c for a wordline pulse width T_B. The wordline pulse width T_B is good enough to discharge the bitline (BL) and causes sufficient differential voltage to overcome the offset or trigger the sense amplifier. As a result, it latches the correct value of the data stored in the bitcell. It emphasize that there should be a critical wordline pulse width, T_{access} ($T_A < T_{access} < T_B$), for which sense amplifier is on the threshold of a successful read access that is defined as the read access time. This is similar to dynamic read access failure defined in [55, 82, 105]. Thus, size of wordline pulse width has a significant role in performing the correct read operation.

Under dynamic read stress, standard 6T SRAM bitcell's bitlines (BL and BLB) are precharged to V_{DD} and wordline is activated with different pulse widths (T_A and T_B), as shown in Fig. 2.24. The wordline pulse width T_A is short enough so that the internal nodes Q and QB return back to their original levels after the wordline pulse is deasserted, as shown in Fig. 2.24b. This is a desirable feature in order to avoid the destructive read operation. However, wordline pulse width should not be shorter than the pulse width of a successful read access operation, as shown in Fig. 2.23c. A longer wordline pulse width T_B is applied to put the SRAM bitcell under heavy stress, causing the bitcell to flip to an opposite state before the wordline pulse is deasserted. It is corresponding to the destructive read failure (i.e. read upset) because bitcell's content changed during read access which is not desirable. The destructive read failure, therefore, can be defined as a bitcell is unstable if the voltage of the node storing a '0' (Q) reaches the trip point of the inverter (INV2) during the pulse width

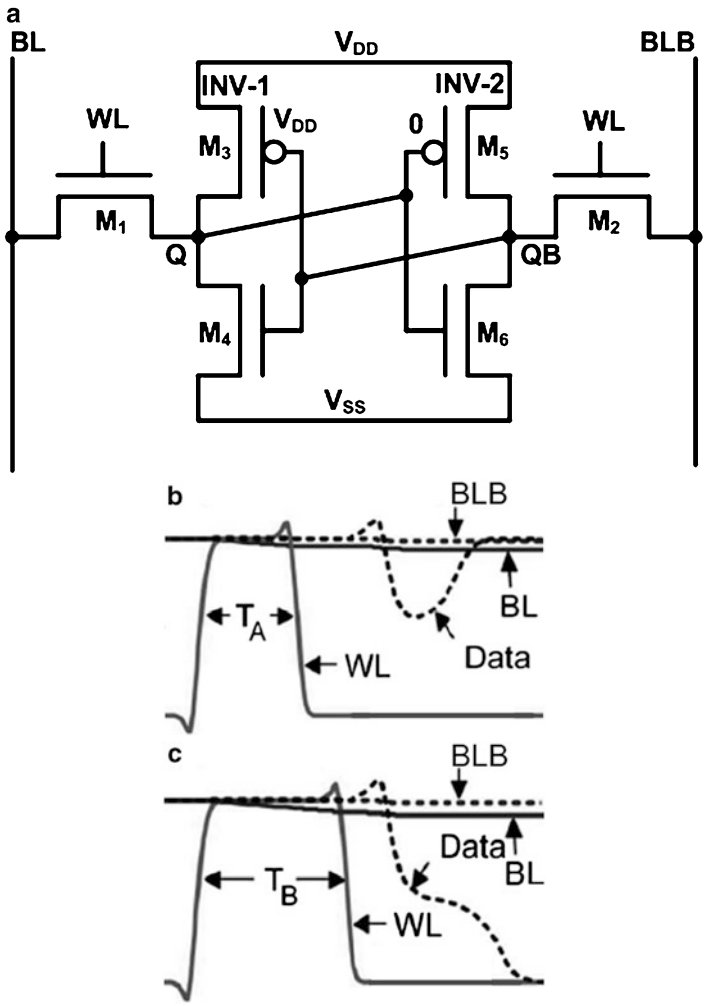


Fig. 2.23 SRAM bitcell under read access for different wordline pulse widths. (**a**) Schematic diagram of a standard 6T SRAM bitcell under read access (i.e. bitlines are precharged to V_{DD} and wordline is active) storing '0' on the left internal node Q. (**b**) Different simulated waveforms showing failed read access with wordline pulse width, T_A. The output of the sense amplifier (Data) resolves to the wrong value. (**c**) Different simulated waveforms showing successful read access with a longer wordline pulse width, T_B. The output of the sense amplifier (Data) resolves to the correct value

T_B is shown in Fig. 2.24c. The bitcell stress applied with different wordline pulse widths have significant role in determining the dynamic read stability. Therefore, there should be a critical pulse width T_{read} ($T_A < T_{read} < T_B$), for which the bitcell is on threshold of destructive read operation or read upset.

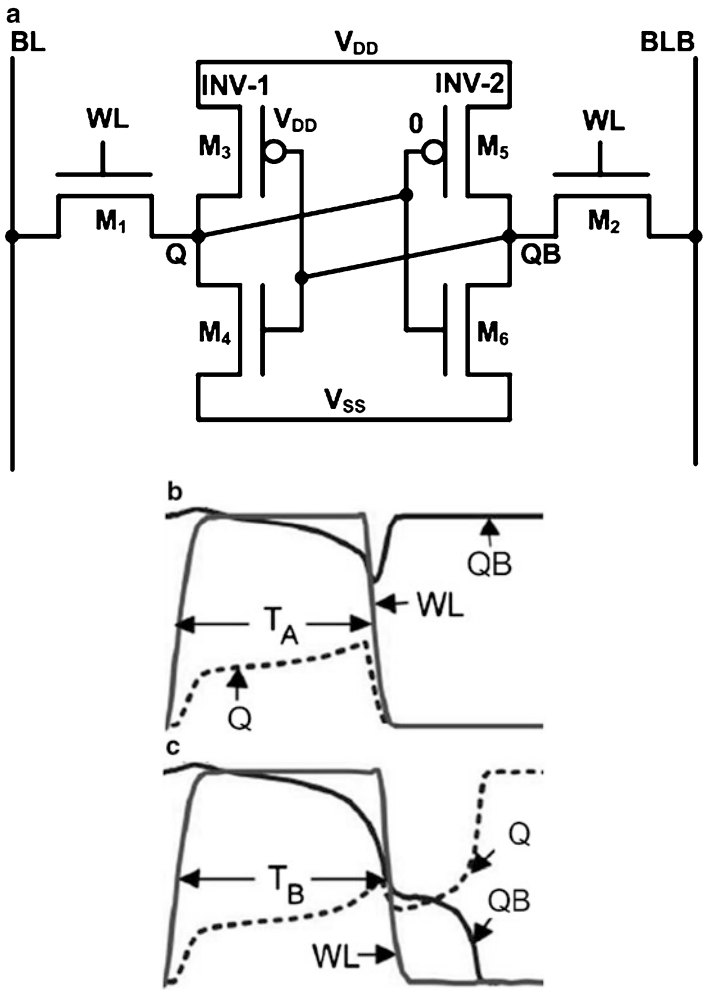


Fig. 2.24 SRAM bitcell under read access for different wordline pulse widths. (**a**) Schematic diagram of a standard 6T SRAM bitcell under dynamic read stress (i.e. both bitlines are precharged to V_{DD} and wordline is active with different pulse widths). (**b**) Different simulated waveforms showing a successful read operation with wordline pulse width, T_A. The internal data storage nodes Q and QB retained their states after read operation. (**c**) Different simulated waveforms showing destructive read operation with a longer wordline pulse width, T_B. The internal data storage nodes Q and QB accidentally flipped their states after read operation

2.4.2 Dynamic Write Stability

Dynamic write failure of a standard 6T SRAM bitcell, as shown in Fig. 2.25a can be studied under following biasing conditions that are correspond to a write operation. The bitline (BL) is charged to V_{DD} and its complementary bitline (BLB) is tied to

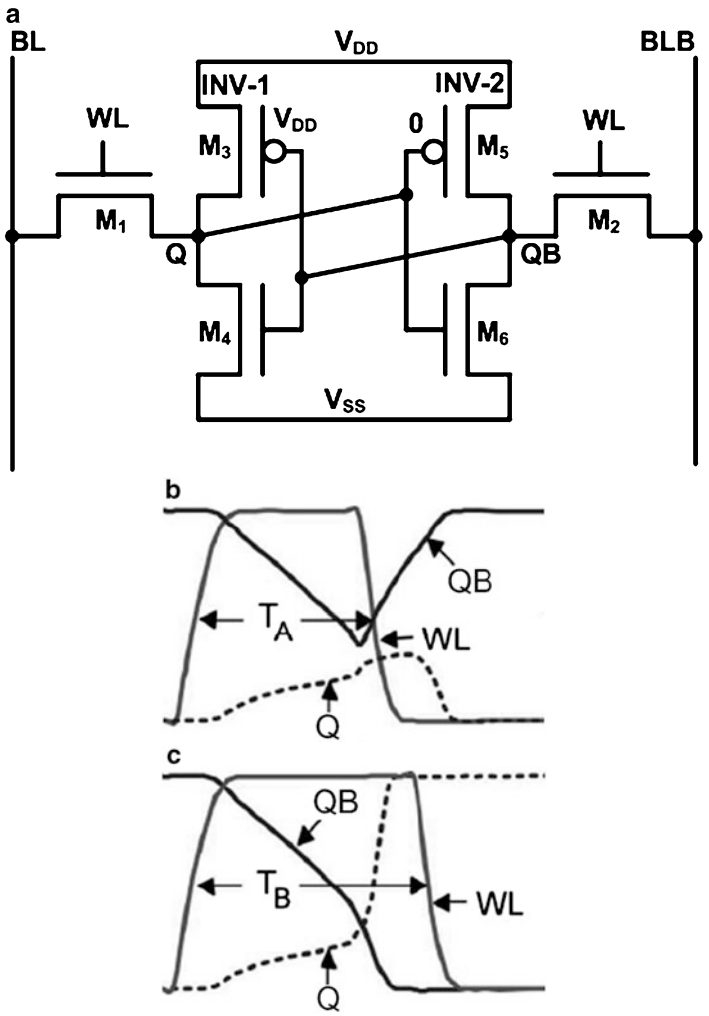


Fig. 2.25 SRAM bitcell under read access for different wordline pulse widths. (**a**) Schematic diagram of a standard 6T SRAM bitcell under read access (i.e. bitlines are precharged to V_{DD} and wordline is active) storing '0' on the left internal node Q. (**b**) Different simulated waveforms showing failed read access with wordline pulse width, T_A. The output of the sense amplifier (Data) resolves to the wrong value. (**c**) Different simulated waveforms showing successful read access with a longer wordline pulse width, T_B. The output of the sense amplifier (Data) resolves to the correct value

V_{SS} and the wordline (WL) is activated with different pulse widths (T_A and T_B). The wordline pulse width T_A is too short to overwrite the internal data storage nodes Q and QB of the SRAM bitcell. As a result, node Q and QB return back to their original states after the wordline pulse T_A is deasserted, as shown in Fig. 2.25b. It is corresponding to the write failure because bitcell's content are not changed during

write access which is not desirable. The dynamic write failure, therefore, can be defined that if the voltage on the node initially storing '1' (QB) could not reach the trip point of the opposite inverter (INV1) during the wordline (WL) pulse then the bitcell will not successfully be written. In Fig. 2.25c, pulse width T_B is sufficient to complete the write operation, that is, node Q and QB change their states before the deassertion of wordline pulse width T_B. Therefore, there should be critical pulse width T_{write} ($T_A < T_{write} < T_B$), for which the bitcell is on threshold of a successful operation.

2.5 Summary

The functionality of a SRAM bitcell can be ensured by analysing different stability criterion, therefore, static and dynamic stability analysis techniques have been exhaustively studied and presented in a comprehensive manner. Simulation setups for different stability techniques are illustrated along with simulation results. Limitations of static stability analysis techniques and how they are pessimistic and optimistically estimates the write and read SNM for failure analysis emphasize the need of dynamic stability analysis. For large size cache memories, where butterfly curve and N-curve approaches do not provide adequate number of data point for stability analysis, bitline measurement techniques play a significant role and provides large number of failure points for statistical analysis of stability are also presented. The dynamic stability analysis approach for a successful read and write operations and the importance of wordline pulse width are also explained.