Surface Modification of Semiconductor by Simultaneous Thermal Oxidation and Nitridation

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Abstract

Integration of high-quality functional thin layer of oxides on semiconductor, in particular wide-bandgap silicon carbide, is of extreme importance in order to realize near future generation of metal-oxide-semiconductor (MOS)-based

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devices for high-power, high-temperature, and/or high-radiation applications. Although nitrided SiO_2 on SiC produced acceptable results, limitations and issues have been reported. Therefore, evolution and justification of changing this type of oxide to high dielectric constant oxide (high-κ) on SiC are being reviewed. This chapter presents the current understanding of simultaneous thermal oxidation and nitridation of sputtered Zr-semiconductor interfaces as the most promising technique for achieving device-quality interfaces required for commercial applications. It is mainly focused on the technological methods of producing oxidized/nitrided Zr on SiC. An exceptional section is devoted to the recent developments of nitrided high-κ gate dielectrics on SiC. It starts with a detailed discussion of high-κ gate dielectric characteristics and the current knowledge of simultaneously oxidized and nitrided Zr film as high-κ dielectric on SiC. Via this technique, the role of N_2O gas ambient on oxidizing and nitriding Zr film on SiC, coupling with physical and electric characteristics of oxidized/nitrided Zr film on SiC, is discussed. A growth mechanism of simultaneous thermal oxidation and nitridation of Zr film on SiC is subsequently presented. Finally, the properties of oxidized/nitrided Zr thin films based on Si and SiC substrates are compared.

Introduction

The advent of technology boom has motivated the use of wide-bandgap (WBG) semiconductors as alternative substrates to replace silicon for high-power, high-temperature, and/or high-radiation metal-oxide-semiconductor (MOS)-based switching devices (Dimitrijev et al. 2004). Of WBG semiconductors, silicon carbide (SiC) has developed into one of the leading contenders due to its commercial availability and ability to grow native oxide (SiO_2) (Dimitrijev et al. 2004). SiC exists in different polytypes (Casady and Johnson 1996). 4H-SiC is one of the polytypes that provides a wide bandgap of 3.26 eV, high breakdown field strength of ~3 MV cm^{-1}, high saturation electron drift velocity of ~2×10^7 cm s^{-1}, and high thermal conductivity of ~3.7 W cm^{-1} °C (Afanas'ev et al. 2004). These properties promisingly enable operation of SiC-based devices under harsh conditions.

In order to realize next-generation SiC-based MOS devices, a high-quality gate oxide must be deposited or grown between a metal electrode and the semiconductor substrate to sustain a high transverse electric field and a low gate leakage current in the devices (Cheong et al. 2008a). To date, thermally nitrided SiO_2 is regarded as the best gate oxide on SiC due to its low interface and slow trap densities and high reliability (Jamet and Dimitrijev 2001; Jamet et al. 2001; Cheong et al. 2003, 2007, 2008b, 2010). Nonetheless, there are problems associated with the SiO_2 thin film or gate based on SiC. In SiC-based MOS devices, the low-κ value of 3.9 in SiO_2 compared to SiC with κ value of 10 limits the permissible electric field in SiC-based devices (Lipkin and Palmour 1999). As a result, the gate oxide may electrically break down prior to the SiC substrate, thus defeating the purpose of using SiC as the primer substrate for high-power and high-temperature applications. In short, the

integration of high-κ oxides on SiC is to lower the electric field being imposed on the gate oxide itself.

Although nitrided SiO_2 on SiC produced acceptable results, limitations and issues have been reported. Evolution and justification of changing this type of oxide to high dielectric constant oxide (high-κ) on SiC and recent development of nitrided high-κ gate dielectrics on SiC are being reviewed. The recent developments of nitrided high-κ gate dielectrics, in particular on nitride ZrO_2, on SiC, with a detailed discussion of high-κ gate dielectric characteristics and the current knowledge of simultaneously oxidized and nitrided Zr film as high-κ dielectric on SiC are presented. Through this technique, the role of N_2O gas ambient on oxidizing and nitriding Zr film on SiC, coupling with physical and electric characteristics of oxidized/nitrided Zr film on SiC, is reviewed. The final section presents a growth mechanism of simultaneous thermal oxidation and nitridation of Zr film on SiC.

Nitrided High-κ Dielectric on SiC

Up-to-date, nitrided SiO_2 on SiC is regarded as the first choice gate dielectric owing to its acceptable low interface and slow trap density, high reliability, and low leakage current (Dimitrijev et al. 2004; Jamet and Dimitrijev 2001; Jamet et al. 2001; Cheong et al. 2003; 2010; Wong and Cheong 2012a). Nevertheless, there are woes associated with nitrided SiO_2 as gate dielectric based on SiC, namely, insufficient stability at elevated temperature and high electric field (Lipkin and Palmour 1999). The low dielectric constant (κ) value of nitrided SiO_2 of 3.9, as compared to SiC with κ value of 10, could cause oxide breakdown and reliability issues. As stated by Gauss law (Lipkin and Palmour 1999; Wong and Cheong 2012a):

$$E_{ox} \bullet \kappa_{\mathrm{ox}} = E_{SiC} \bullet \kappa_{\mathrm{SiC}} \quad (1)$$

The high electric field strength in SiC of ~3 MV cm^{-1} would give a high electric field of ~7.69 MV cm^{-1} in SiO_2, in which it is a multiple of ~2.56 times higher electric field being imposed on the gate oxide than on the SiC. As a result, the low-κ gate oxide may electrically break down much earlier than the SiC substrate, thus diminishing the purpose of using SiC as the potential substrate for high-power, high-temperature, and/or high-radiation applications (Wong and Cheong 2012a). Therefore, in order to lower the electric being imposed on the gate oxide, superseding the low-κ nitrided gate oxide with high-κ nitrided gate oxide on SiC is an approach to circumvent the problem (Choyke et al. 2004).

High-κ Gate Dielectric Characteristics

Unlike Si-based devices, downscaling of device dimensions is not the driving force for development of SiC-based power devices. Instead, the motivation for the

investigation of alternative high-κ dielectrics on SiC is to extend the performance capabilities in high-power, high-temperature, and/or high-radiation applications. To select a promising high-κ material to replace SiO_2 as dielectric based on SiC, some criteria in terms of dielectric constant, band alignment, interface quality, and thermodynamic and kinetic stabilities need to be satisfied (Robertson 2004; Wong and Iwai 2006; Wilk et al. 2001a; Wong and Cheong 2010). Different deposition techniques produce different characteristics and quality of high-κ gate dielectric. By taking an example of ZrO_2, as a potential high-κ gate dielectric, the crucial general characteristics and quality of ZrO_2 thin film produced by different deposition techniques will be elucidated.

Dielectric Constant

The κ value is the first criteria to be taken into account to select a material for gate dielectric application. An MOS structure can be modeled as a parallel-plate capacitor. Hence, its capacitance is governed by the dielectric constant of the oxide layer and can be related by the following equation (Robertson 2004; Wong and Iwai 2006; Wilk et al. 2001a; Wong and Cheong 2010):

$$C_{ox} = \kappa\varepsilon_o A/t_{ox} \tag{2}$$

where C_{ox} represents capacitance of oxide layer, ε_o is permittivity of free space (8.85×10^{-12} F m^{-1}), A is area of capacitor, and t_{ox} is thickness of oxide layer.

As mentioned earlier, Gauss law (Eq. 1) demonstrates that the electric field scales with the materials dielectric constant and requires that $E \bullet \kappa$ be in equivalence at the interface of two adjacent materials. When effective electric field in SiO_2 is ~2.56 times higher than that in SiC, consequently, the SiC substrate cannot be deployed to its maximum potential, deteriorating its advantage in high-power, high-temperature, and/or high-radiation applications. Alternatively, a material with κ value equal to or higher than that of SiC is desirable. According to Lipkin et al. (1999), $E_o \bullet \kappa$ is a critical measure of a material's applicability for high-power devices, where E_o is the highest safe operating field for the dielectric. However, E_o is typically limited to about 20 % of the critical field by electrons tunneling from the substrate into the gate dielectric. The safe operating field in SiO_2 is less than 2 MV cm^{-1}, which corresponds to a field in SiC of 0.78 MV cm^{-1}, about 3.85 times less than its avalanche breakdown field. A device's blocking voltage scales with electric field squared, thereby resulting in a tenfold drop in blocking voltage capability owing to the limitations of the thermal SiO_2. Therefore, as a promising candidate for gate dielectric application, a material must have a higher κ value, preferably greater than 10.

Numerous researchers across the world are intensively looking for an alternative oxide with high κ properties for gate dielectric to supersede SiO_2 in Si-based MOS devices. As the device dimensions scale down, it is necessary to reduce the thickness of the gate oxide in order to maintain the capacitance. However, electron tunneling increases exponentially as the oxide thickness reduces. Superior properties of SiO_2 allowed the fabrication of properly working MOS devices with SiO_2

gate layers as thin as 1.2 nm (Wong and Cheong 2010; International Technology Roadmap for Semiconductors 2011); thinner than that will be problematic, for instance, (1) the occurrence of relatively huge leakage current through the oxide, due to direct tunneling of carriers, is highly possible; thus, the device performance will be substantially degraded; (2) difficulty in fabricating such a thin layer of film; and (3) reliability of SiO_2 films against electric breakdown declines in thin films (Robertson 2004; Wong and Iwai 2006; Wong and Cheong 2010). Hence, the use of high-κ gate oxide enables a physically thicker dielectric layer to attain the similar or better MOS characteristics that are equivalent to the SiO_2. Referring to Eq. 2, it tells that, in order to attain the same capacitance for the same area, the ratios of the dielectric constants to the thicknesses of two materials must be equal. In MOS structure, all dimensions scale proportionally without affecting the electric designs (Robertson 2004; Wong and Cheong 2010). Therefore, it is convenient to define an equivalent oxide thickness (*EOT*), which allows direct comparison of high-κ oxide and SiO_2 films based on their dielectric constants (Wilk et al. 2001a; Wong and Cheong 2010):

$$EOT = t_{\text{high}-\kappa} = \left(\frac{k_{\text{high}-k}}{k_{\text{SiO}_2}} t_{\text{SiO}_2} \right) \tag{3}$$

where $t_{\text{high}-\kappa}$ and t_{SiO_2} are the thicknesses of high-κ dielectric material and SiO_2, respectively, while $\kappa_{\text{high}-\kappa}$ and κ_{SiO_2} are the dielectric constants of the high-κ dielectric material and SiO_2, respectively. In short, a hypothetical high-κ oxide film with a much thinner *EOT* can be achieved. Although the aforementioned principles are commonly applied in Si-based MOS technology, they can be applicable for SiC-based MOS devices as well and serve as an essential platform to the understanding of the potential of high-κ materials. Though many transition metal oxides offer significantly higher κ values than SiO_2, however, not every high-κ oxide can be employed as dielectric in MOS device. If the κ value of a material is too high, for example, TiO_2, which offers its κ value of 80 (Robertson 2004; Wong and Iwai 2006; Wilk et al. 2001a; Wong and Cheong 2010), it will cause fringing field from the drain through the gate dielectric. This fringing field can deteriorate the source-to-channel potential barrier, thus giving undesirably poor subthreshold performance (Wong and Iwai 2006; Wong and Cheong 2010; Mohapatra et al. 2002). As a promising candidate for gate dielectric application, ZrO_2 provides high enough κ value of about 22–25 (Robertson 2004; Wong and Iwai 2006; Wilk et al. 2001a; Wong and Cheong 2010, 2011a, b, c, 2012b; Kurniawan et al. 2011; Wong and Cheong 2012c), to be used for a reasonable number of years of scaling.

Band Alignment

A potential candidate for high-κ dielectrics must have large band offsets. Band offset between an oxide and semiconductor substrate can be defined as the barrier for holes or electrons to be injected into the oxide, and it is closely related to bandgap of a material, whereby a material with larger bandgap will correspond to a larger band offset (Wong and Cheong 2010; Robertson and Peacock 2004).

With large band offsets (high barriers) at the oxide/semiconductor interface, the carrier generation and conduction can be minimized (Wilk et al. 2001a; Wong and Cheong 2010), thus suppressing the leakage current (Wong and Iwai 2006). According to the periodic table of elements that have been known, as the atomic number of an element increases, the ionic size (radius) of an element increases but the ionic bonding force (cohesive force) decreases. This leads to a high dielectric constant but a narrow bandgap (Wong and Cheong 2010; Boer 2002). Subsequently, material with higher κ value will possess undesirable smaller band offset value. Based on Clausius-Mossotti equation, the inverse relationship between energy bandgap and dielectric constant can be depicted (Wong and Cheong 2010; He et al. 1999):

$$E_{\mathrm{g}} \approx 20 \left(\frac{3}{k+2} \right)^2 \tag{4}$$

where E_{g} defines energy bandgap and κ defines dielectric constant value.

Integration of gate dielectric in Si-based MOS devices requires valence and conduction band offsets at the oxide/semiconductor interface of larger than 1 eV to minimize carrier injection into its bands thus reducing leakage current (Wong and Cheong 2010). If this criterion is applied to 4H-SiC, with its E_{g} of 3.26 eV (Afanas'ev et al. 2004; Wong and Cheong 2012b; Kurniawan et al. 2011), by assuming a symmetric band alignment, the high-κ oxide bandgap must be of minimum 5.3 eV.

ZrO_2 has reasonably high band offsets of 5.8–7.8 eV (Robertson 2004; Wong and Cheong 2010; Wilk et al. 2001b), with its electron offset or conduction band offset (ΔE_{c}) values of 1.3–2.3 eV, by assuming a symmetric band alignment. Hence, ZrO_2, with $\Delta E_{\mathrm{c}} > 1$ eV, can avoid carrier generation (electron transport), either from enhanced Schottky emission, thermal emission, or tunneling, thus minimizing leakage current (Wong and Cheong 2010). Figure 1 illustrates a simple schematic of bandgap and band offsets of ZrO_2 by assuming a symmetric band alignment carrier injection mechanism in its band states.

Interface Quality

In an MOS device, charge carriers induced by the metal gate electrodes are significantly influenced within the nanometers of the interface of the oxide and the semiconductor (Robertson 2004; Wong and Cheong 2010). This has pointed that the quality of the interface of the oxide and the semiconductor is the determining factor for carrier mobility, as well as device functionality. Hence, the oxides must form a good quality interface with semiconductor, with minimal or no interface states or defect states within the semiconductor bandgap (Robertson and Peacock 2004). With a good quality of interface, an MOS device can perform very well electrically as the current can flow in the semiconductor channel next to the interface.

To date, exponentially higher interface trap densities have been observed at energy levels beyond the Si bandgap yet within the SiC bandgap. It would be desirable to achieve interface trap density (D_{it}) of less than 10^{11} cm^{-2} eV^{-1} for

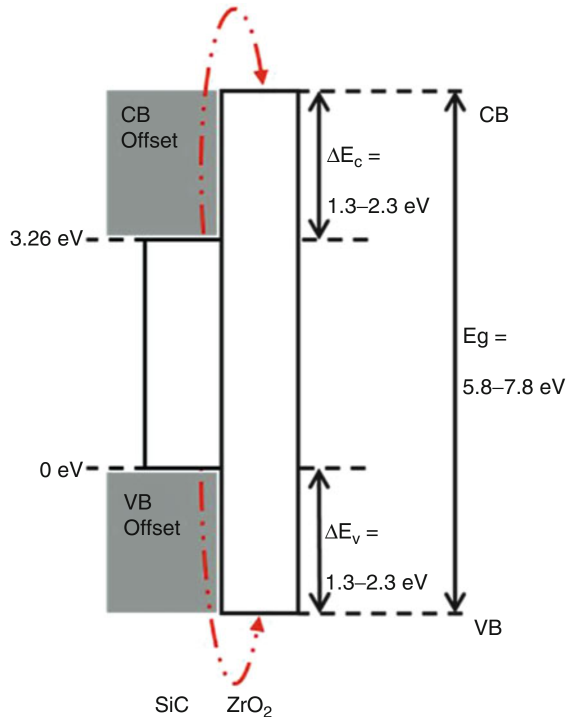

Fig. 1 Simple schematic of bandgap and band offsets of ZrO_2 and carrier injection mechanism in its band states. *CB* conduction band, *VB* valence band

high-κ gate dielectric based on SiC MOS devices. As compared to the state of the art for SiO_2 on SiC, gains in field strength would make the high-κ oxide, for example, ZrO_2, a preferable dielectric for SiC power devices.

Thermodynamic and Kinetic Stabilities

Basically, the objective of thermodynamics is to provide a description of a system of interest (high-κ oxide/SiC) in order to investigate the nature and extent of changes in the state of that system as it undergoes spontaneous change toward equilibrium and interacts with its surroundings. On the other hand, the goal of kinetics is to describe the rate of a reaction to reach equilibrium, which means input of energy (sufficient activation energy) is necessary to enable the reaction to proceed in the forward direction (turning reactants to products) (Wong and Cheong 2010).

Ideally, thermodynamic stability is achieved if there is no reaction between high-κ oxide and SiC under equilibrium condition to form an undesirable interfacial layer. On the contrary, if there are interface reactions between the oxide and the semiconductor substrate driven by thermodynamics, these reactions will lead to substrate oxidation and the formation of hybrid compounds, which are generally detrimental to interface quality and device performance. The interfacial layer, in general, has a lower κ value than that of the bulk oxide due to the formation of silicates. A high-κ oxide is considered as kinetically stable on SiC if it is able to

Table 1 The properties of ZrO_2 compared with other high-κ oxides

Oxides	Dielectric constant (κ) values	Bandgap (E_g)
Al_2O_3	9–10	8.8
CeO_2	26	6.0
Gd_2O_3	12	5.0
HfO_2	20	5.6–5.7
La_2O_3	27	5.8
Pr_2O_3	26–30	3.9
Y_2O_3	15	6.0
ZrO_2	22–25	5.8–7.8

Data from Wong and Iwai (2006), Wong and Cheong (2010), Lim et al. (2010), and Nigro et al. (2006)

perform operation at high temperature and withstand the rigors of MOS device processing, which typically requires temperatures of 900–1,000 °C for drive-in annealing, field oxidation, and dopant activation. The high-κ oxide must not degrade or react with the substrate. In addition, for high-temperature applications, there must be minimal impurity diffusion or electric conduction through the oxide during prolonged use. Of several high-κ oxides, ZrO_2 is stable with underlying Si and 4H-SiC substrates up to a certain high temperature (900–1,000 °C), thus making it to be considered as a potential candidate. Table 1 demonstrates the properties of ZrO_2 as a potential candidate compared with other high-κ oxides.

Deposition Techniques

Several thin-film deposition techniques have been investigated for the growth of gate oxide, such as thermal evaporation, electron beam evaporation (EBE), pulsed laser deposition (PLD), cathodic arc deposition, atomic layer deposition (ALD), metal-organic chemical vapor deposition (MOCVD), and sputtering.

Sputtering is the preferred deposition technique of high-quality gate oxide on Si and SiC. This deposition technique involves ejection of material from the surface of a solid due to the momentum exchange associated with surface bombardment by energetic particles (Wong and Cheong 2010; Dwbrowski and Mussig 2000). A source of deposited material, either Zr or ZrO_2 target, is placed into a vacuum chamber along with the substrates, and the chamber is evacuated to a pressure typically in the range 5×10^{-4} to 5×10^{-7} Torr. The bombarding species are generally ions of a heavy inert gas. Argon is most commonly used. Direct current (DC) sputtering and radio frequency (RF) sputtering are two most common modes in sputtering. DC sputtering is generally used when the target material is a good electric conductor, for instance, Zr target. RF sputtering is used when the target material is a poor conductor or an insulator, for example, ZrO_2 target (Wong and Cheong 2010).

Sputtering offers high homogeneity (Wong and Cheong 2010; Ben Amor et al. 1998), good uniformity (Wong and Cheong 2010; Ben Amor et al. 1998), and low impurity contents (Wong and Cheong 2010; He et al. 2005) in the sputtered film. Additionally, it favorably offers high deposition rate (Wong and Cheong 2010;

Hembram et al. 2007). Thus, employment of this technique can easily be scaled up from the small-sized substrates used in laboratory experiments to large-scale industrial applications. Sputter deposition of ZrO_2 thin films on Si and SiC can be achieved in three routes: (1) by direct sputtering when the substance to be sputtered is ZrO_2, (2) by reactive sputtering when Zr metal is sputtered in the presence of an oxygen atmosphere with an inert gas (Ar gas is commonly employed), and (3) by nonreactive sputtering when Zr metal is sputtered in an inert gas ambient (Ar gas is commonly employed), followed by an oxidation process. Of these routes, the third route enables control of the stoichiometry of the deposited films (Wong and Cheong 2010, 2011a, b, c, 2012b, c; Hembram et al. 2007; Wong and Cheong 2011d). On the contrary, when metallic target atoms react with the active components of the gas (oxygen), the film stoichiometry is difficult to control and generally presents numerous pinholes and low density (Wong and Cheong 2010; Chaneliere et al. 1998).

Nitridation Process

Si- and SiC-based devices tend to suffer from severe degradation of the electron mobility due to high density of interface traps close to the conduction band edge at the high-κ oxide/Si and high-κ oxide/SiC interface. It has been found that nitridation can greatly reduce the interface traps and effectively passivate the oxygen vacancies in the high-κ oxide (Dimitrijev et al. 2004; Chen et al. 2010). Therefore, nitridation process is advantageous and regarded as one of the effective processes to improve the interface properties of Si- and SiC-based MOS devices. Nitridation can be defined as the formation of nitride by the high-temperature exposure of a surface to nitrogen-contained environment (Zant 2004). In semiconductor industry, this process consists of an oxidation or a reoxidation in a mixture of O- and N-containing gases such as NO and N_2O and is also termed oxynitridation. This process is analogous to the diffusion of oxygen in the classical Deal-Grove picture (Wong and Cheong 2010); nitrogen diffuses into a film, with or without interacting with the oxide network. Nitrogen can react at the near-interface region with unoxidized or partially oxidized Si atoms from Si and/or SiC substrates.

Gupta et al. (1998) and Enta et al. (2006) reported on the formation of Si-oxynitride in N_2O, and they proposed that at elevated temperature, N_2O can decompose into oxygen, nitrogen, and oxygen-nitrogen compounds, and the nitrogen-related compound acts as the nitridation source. As proposed by Gupta et al. (1998), the decomposition of N_2O is based on a 5-step reaction. The initial decomposition step of N_2O is stated in Eq. 5:

$$N_2O \rightarrow N_2 + O \tag{5}$$

The atomic oxygen reacts further with N_2O based on the following steps in Eqs. 6 and 7:

$$N_2O + O \rightarrow 2NO \quad (6)$$

$$N_2O + O \rightarrow N_2 + O_2 \quad (7)$$

In addition to these reactions, the other essential reactions are stated in Eqs. 8 and 9:

$$NO + O \rightarrow NO_2 \quad (8)$$

$$NO_2 + O \rightarrow NO + O_2 \quad (9)$$

Miller and Grassian (1997) reported that ZrO_2 is an effective catalyst for the decomposition of N_2O, whereby N_2O will decompose exclusively to N and O compounds. The same study also found that Zr cations were involved in the decomposition reaction of N_2O. Zhu et al. (2005) reported that a complete catalytic decomposition of N_2O on ZrO_2 happens at a temperature of 700 °C, while Petrucci et al. (2002) reported that there is no free energy change-temperature dependence in the decomposition of N_2O into N and O compounds. Therefore, the decomposition is spontaneous at all reaction temperatures.

In nitrogen-contained environment, Si atoms from Si and/or SiC substrates can react with nitrogen and form silicon nitride (Si-N) (Jamet and Dimitrijev 2001; Jamet et al. 2001; Cheong et al. 2003; Cheong et al. 2010). Meanwhile, as reported by Reddy et al. (2007), it is reported that the zirconium nitride (Zr-N) can be formed by reacting nitrogen with sub-stoichiometric ZrO_2. Ngaruiya et al. (2004) reported that the nitrogen atoms can occupy oxygen sites within crystalline phase of Zr-O, resulting in an almost unchanged ZrO_2 structure with a sevenfold metal-nonmetal coordination and interatomic distances around 2.04–2.27 Å. The reported interatomic distances have assured Zr tetravalency when nitrogen has been incorporated into stoichiometric Zr-O layer. Therefore, Zr-O compound remains stoichiometric at the topmost surface. In this study, Si-N, Zr-N, and/or Zr-O-N were formed, in the bulk of the film and/or at the interface region sandwiched between the film and the substrate when Zr films were subjected to N_2O gases at higher than 700 °C.

Role of N_2O Gas Ambient on Oxidizing and Nitriding of Zr Film on SiC

In general, the interfaces of high-κ gate oxide/semiconductor are often regarded as nonideal due to the presence of interface defects. These defects may be originated from surface-structural defects, oxidation-induced defects, or radiation-induced defects (Wong and Cheong 2011b, 2012b; Schroder 2006). The interface trap has a significant influence on the reliability and lifetime of an MOS device because it is a main source causing leakage current besides the characteristics of the oxide itself.

It is therefore crucial to control the thickness and composition of interfacial layer in between the gate oxide and semiconductor, so that the interface trap density can be minimized to an acceptable level and good electric characteristics of an MOS device can be achieved (Wong and Cheong 2011b, 2012b).

Numerous studies have been carried out to improve the MOS characteristics and the oxide-semiconductor interface quality. Researchers have reported on the influence of pretreated Si substrate with N_2O and NH_3 gas in order to suppress formation of interfacial defect by controlling the growth of IL thickness (Chen et al. 2007; Choi et al. 2011). Moreover, post-deposition annealing of ZrO_2 film in nitrogen ambient was also studied in order to improve its electric properties (Lin et al. 2003). It was found that incorporation of nitrogen into the film may retard the growth of interfacial layer and improved electric properties of the film. This improvement may be attributed to two factors (Wong and Cheong 2011a). Firstly, the presence of nitrogen is postulated to passivate the oxygen vacancies by forming Zr-N, Si-N, and/or Si-O-N bonds, thus reducing amount of interfacial traps. Additionally, these particular bonds are believed to effectively suppress crystallization that may enhance thermal stability of the film. Secondly, dangling bonds of Si surface may be passivated by the nitrogen-rich species generated during nitridation process (de Almeida and Baumvol 2003). In short, incorporation of nitrogen in the film is a possible solution.

In order to improve the SiC-based MOS characteristics and the oxide-SiC interface quality, it has been found that oxidation and/or post-oxidation annealing in a nitrogen-containing ambient has two beneficial effects, i.e., enhanced removal of carbon and passivation of silicon dangling bonds (Dimitrijev et al. 2004). The utilization of nitrous oxide (N_2O) gas has contributed to the growth of thermally nitrided SiO_2 as gate oxide on SiC with low leakage current and low interface trap density (Jamet and Dimitrijev 2001; Cheong et al. 2010). At high temperature, N_2O gas is decomposed exclusively into N and O compounds, which are indispensable in performing oxidation and nitridation processes on the gate oxide (Cheong et al. 2010; Wong and Cheong 2011a). In general, the beneficial effects of utilizing N_2O gas in growing thermally nitrided SiO_2 gate on SiC-based MOS structure have been highlighted.

According to the accumulated knowledge (Dimitrijev et al. 2004; Jamet and Dimitrijev 2001; Jamet et al. 2001; Cheong et al. 2003, 2007, 2008b, 2010) from thermally nitrided and oxidized Si on SiC to form nitrided SiO_2 gate, nitrogen source may enhance removal of carbon that has been accumulated at the interface during thermal oxidation and may improve passivation of dangling bonds on surface of the semiconductor depending on the equilibrium rate of oxidation and nitridation that has been achieved by diluting the oxidation and nitrogen sources (Dimitrijev et al. 2004). The most effective gases in achieving these effects are nitrous oxide (N_2O) and nitric oxide (NO) (Dimitrijev et al. 2004). The former gas is more preferable due to its nontoxic property (Cheong et al. 2003, 2010; Wong and Cheong 2011a; Enta et al. 2006).

A Case Study: General Manufacturing Processes in Laboratory Scale

Substrate Cleaning Process

First of all, Si and SiC wafers must undergo a cleaning process. This process consists of ultrasonic cleaning, RCA cleaning, and HF dipping. A step-by-step cleaning process is depicted as follows:

Step 1: Ultrasonic cleaning

Objective: To remove small particles from the substrate surface.

Procedures:

(i) Substrates were placed in a Teflon holder and placed in a container containing deionized (DI) water.
(ii) Then, the container was placed into ultrasonic bath for 5 min.
(iii) After that, substrates were rinsed with DI water.

Step 2: RCA-1

Objective: To remove organic residues from the substrate.

Procedures:

(i) Ingredients for RCA-1 (NH_4OH: H_2O_2:H_2O) were prepared with the ratio of 1:1:5.
(ii) 100 ml of DI water was placed in a beaker and heated to 90 °C on a hot plate.
(iii) 20 ml of NH_4OH was added into heated DI water at 90 °C.
(iv) 20 ml of H_2O_2 was then added into the mixture, and the temperature of the solution was decreased to 80 °C.

Step 3: HF dipping

Objective: To remove native oxide from the substrate.

Procedures:

(i) HF was prepared in DI water with ratio 1:50 (HF:H_2O).
(ii) Substrates in Teflon holder were immersed in HF solution for 10 s and then cleaned with DI water.

Step 4: RCA-2

Objective: To remove the metal ions from the substrate.

Procedures:

(i) Ingredients for RCA-2 (HCl: H_2O_2:H_2O) were prepared with the ratio of 1:1:6.
(ii) 120 ml of DI water was placed in a beaker and heated to 90 °C on a hot plate.

(iii) 20 ml of HCl was added into heated DI water at 90 °C.
(iv) 20 ml of H_2O_2 was then added into the mixture and the temperature of the solution was decreased to 80 °C.
(v) It was observed that the solution started to bubble vigorously after about a minute.
(vi) The substrates were then soaked in the solution for 15 min and the temperature was maintained at 80 °C on the hot plate.
(vii) After 15 min, the substrates were cleaned with DI water and dried with air gun.

Sputtering Process in Laboratory Scale

All Zr thin films were sputter-deposited by a magnetron-assisted RF sputtering system (Edwards Auto 500) in a high vacuum chamber with working pressure of 1.6×10^{-7} mbar and RF power of 170 W.

Prior to sputtering process, sputtering machine parts were cleaned by using Decon 90 and acetone. After cleaning, the parts were fixed into the machine. Zr target was fixed at the target holder, while Si and SiC substrates were attached to the rotating substrate holder for deposition. At atmospheric pressure, after the target and substrates were loaded into the chamber and locked, the chamber was pumped to high vacuum (low pressure), i.e., 1.6×10^{-7} mbar within 30 min. When the desired pressure (working pressure) was reached, an inert Ar gas plasma was struck using an RF power source (170 W), causing the gas to become ionized. At this time, pre-sputtering was done for about 2 min to remove the native oxide on the Zr target surface. The deposition rate was controlled at 2 Å s^{-1}. After pre-sputtering, the substrate holder was rotated so that a uniform film can be formed on the substrate. Shutter was then opened and allowed the ions to accelerate toward the surface of the target, causing atoms of the source material to be ejected from the target in vapor form and condensed on Si and SiC substrate surfaces. A 5-nm-thick Zr thin film was formed.

Simultaneous Oxidation and Nitridation Process

Simultaneous oxidation and nitridation process was carried out in N_2O ambient in the quartz tube placed in the horizontal tube furnace. Beforehand, quartz tube, quart boat, gas inlet, and gas outlet must be cleaned with HF solution (1 HF:9 H_2O) in order to remove the undesirable impurities and particles to avoid samples from contamination. After the apparatuses had been washed, quartz tube was first inserted into a horizontal tube furnace. Samples were then arranged on a quartz boat and placed into the quartz tube, as shown in Fig. 2.

The following describes the design of experiments (DOE):

(i) Effects of oxidation/nitridation durations on sputtered Zr based on Si substrate
Samples were heated up from room temperature to 700 °C in an Ar flow ambient and the heating rate was set at 10 °C min^{-1}. Once the set temperature was achieved, N_2O gas was purged in with a flow rate of 150 ml min^{-1} for a

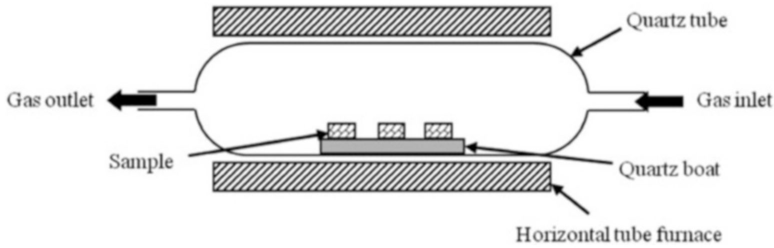

Fig. 2 Setup for oxidation/nitridation process

set of durations (5, 10, 15, and 20 min). The samples were withdrawn from the furnace after the furnace was cooled down to room temperature in an Ar ambient.

(ii) Effects of oxidation/nitridation temperatures on sputtered Zr based on Si substrate
Samples were heated up from room temperature to a set of temperatures (500 °C, 700 °C, 900 °C, and 1,100 °C) in an Ar flow ambient, and the heating rate was constant at 10 °C min^{-1}. Once the set temperature was reached, N_2O gas was then purged in with a flow rate of 150 ml min^{-1} for 15 min. Samples were eventually taken out at room temperature after the furnace was cooled down to room temperature in an Ar ambient.

(iii) Effects of oxidation/nitridation temperatures on sputtered Zr based on SiC substrate
Samples were heated up from room temperature to a set of temperatures (400 °C, 500 °C, 700 °C, and 900 °C) in an Ar flow ambient, and the heating rate was set constant at 10 °C min^{-1}. Once the set temperature was achieved, N_2O gas was then introduced with a flow rate of 150 ml min^{-1} for 15 min. Samples were then taken out at room temperature after the furnace was cooled down to room temperature in an Ar ambient.

(iv) Oxidation/nitridation of sputtered Zr based on SiC substrate in diluted N_2O
Samples were then inserted into a horizontal tube furnace at atmospheric pressure and heated up from room temperature to 500 °C in an Ar flow ambient, and the heating rate was set constant at 10 °C min^{-1}. Once the set temperature was achieved, a set of different concentrations of N_2O gas was introduced, i.e., 10 %, 30 %, 70 %, and 100 % N_2O mixed with 90 %, 70 %, 30 %, and 0 % of high-purity N_2 gas, for duration of 15 min, with a flow rate of 150 ml min^{-1}. Once completed, the furnace was cooled down to room temperature in an Ar ambient, and the samples were withdrawn from the furnace at room temperature.

Metallization and Photolithography Processes

For the purpose of electric characterization, the oxidized/nitrided Zr films were fabricated into MOS capacitors. Al layer of ~100 nm thick was first thermally evaporated on top of the film as gate electrode by using a turbo thermal evaporator

K950X. W wire was made into a coil and fixed at the particular holder. After that, samples were located on the sample holder and ready for thermal evaporation. The chamber was locked and pumped to high vacuum condition at ~6×10^{-6} mbar. The vacuum is required to allow the atoms (Al) to evaporate freely in the chamber and subsequently condense on sample surfaces. Once the particular condition has been reached, current was regulated at about 20 ampere (A). This is done in order to heat the tungsten coil. Source material (Al) was concurrently heated as well. When the source material was heated to its boiling point, it started to evaporate and eventually condensed on the sample surfaces.

Photolithography was conducted after Al was successfully evaporated (deposited) on top of the oxidized/nitrided Zr films. A layer of primer solution was coated on the Al surface at 2,500 rotation per min (rpm) by using a spinner, followed by coating of a layer of photoresist solution on the Al surface by using the same spinner and same rotation speed. After that, a soft-bake in an oven at 100 °C for 15 min was performed before the ultraviolet (UV) exposure. A patterned mask with 11 by 11 squared cells, defined at 2.5×10^{-3} cm^2 each cell, was used and aligned on top of Al surface. It was then exposed under UV light for 30 s. After the exposure, the sample was immersed in developer solution until all the defined windows (cells) were clearly seen, followed by a thorough DI water rinse. Sample was then blow-dried with an air gun and brought to hard-bake in an oven at 120 °C for 20 min. The Al gate electrode was etched with aluminum etchant. The aluminum etchant was prepared by mixing phosphoric acid (H_3PO_4), acetic acid (CH_3COOH), and nitric acid (HNO_3) together, with ratio of 20:4:1. The etching was done within 10 s as the etching rate was high. The photoresist was eventually stripped by photoresist remover. The capacitor area was 2.5×10^{-3} cm^2.

For back contact fabrication, a ~100-nm-thick Al layer was thermally evaporated onto the backside of the Si substrate. The formation of back contact was similar to the process adopted for front contact as discussed in the earlier paragraph. In order to obtain a better back contact (Ohmic contact), the native oxide on the Si backside surface was removed by diluted HF solution (1 HF:50 H_2O). Figure 3 shows an overview process of metallization (front and back contact) and photolithography applied in this work.

Physical Characteristics of Oxidized/Nitrided Zr Film on SiC

Compositional and depth profile analysis is a formidable challenge to retrieve compositional information in ultrathin high-κ dielectric films, of homogeneous layer, of multilayers, or of layers with a gradient in their composition. None of the characterization techniques covers the whole range of sensitivity or depth resolution needed. In order to determine the composition and/or composition variation in an ultrathin film up to a few nanometers, only a few characterization techniques have the potential to achieve the needed depth resolution, i.e., time-of-flight secondary ion mass spectrometry (TOF-SIMS), elastic recoil detection

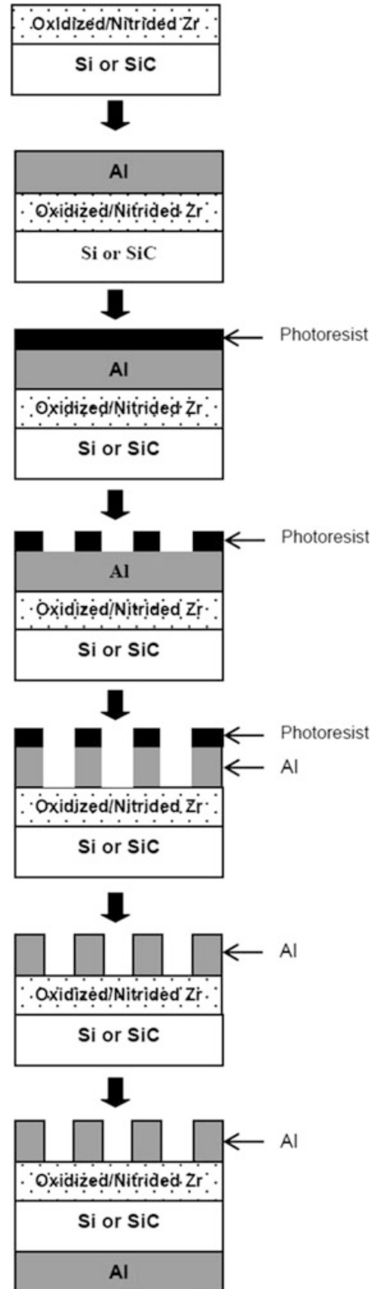

Fig. 3 Overview process of metallization (front and back contact) and photolithography

analysis (ERDA), medium-energy ion scattering (MEIS), and X-ray photoelectron spectroscopy (XPS) (Conard et al. 2007).

Of these techniques, XPS was used to determine the composition and depth profile of thin oxidized/nitrided sputtered Zr film of approximately 20 nm based on SiC substrate, as reported by Wong and Cheong (2011d). Figure 4 shows an atomic composition depth profile obtained by XPS. It depicts that Zr-oxynitride was formed with nitrogen incorporated into the Zr-O network (ZrO_2) of the film. Due to the vast growth kinetics of thin oxide of Zr on SiC, it is of importance to determine the amount of nitrogen and its distribution related to its interface, as shown in Fig. 4e. From this figure, it is demonstrated that the nitrogen in the sample oxidized/nitrided at 500 °C is distributed more uniformly throughout the entire film, including interfacial layer, as compared to other samples.

Figures 5, 6, and 7 elucidate the Zr 3*d*, Si 2*p*, and N 1s spectra, respectively, as a function of etching time for different oxidation/nitridation temperatures of 400–900 °C, obtained from XPS analysis. From the analysis, it was identified that Zr-oxynitride film of Zr-O, Zr-N, and/or Zr-O-N and its interfacial layer comprised of mixed Zr-O, Zr-N, Zr-O-N, Zr-Si-O, Si-N, and/or C-N compounds were formed on SiC substrate.

To attain high-quality high-κ dielectric films with very low *EOT* and high dielectric constant, one of the critical issues being focused is by controlling the interfacial layer. Ideally, no interfacial layer should be present, as this will affect the available capacitance budget for the high-κ dielectric film. However, as reported by some researchers (Conard et al. 2007; Choi et al. 2005), the presence of interfacial layer can provide positive effects on the growth of high-κ dielectric film and on the enhanced mobility obtained with the stack. Therefore, thickness and composition of interfacial layer are regarded as a crucial part of high-κ dielectric film analysis. Transmission electron microscopy (TEM) was utilized to observe the cross section of the oxidized/nitrided Zr films, as displayed in Fig. 8. Patches of lattice fringes with interplanar spacing, *d*, of 0.258–0.305 nm, indicate that polycrystalline structure of bulk oxide was formed and the range of *d* values matched with ZrO_2 (Wong and Cheong 2011a). By comparing the results obtained from XPS and TEM, it is inferred that Zr-N and Zr-O-N may be in amorphous structure which embedded in the polycrystalline ZrO_2. Besides, it is also inferred that interfacial layer of mixture of sub- or nonstoichiometric Zr-O, Zr-N, Zr-O-N, Zr-Si-O, Si-N, and C-N, which are in amorphous structure.

In monitoring any deposition or growth process, either in a production line or for process development, thickness control is a key parameter (Conard et al. 2007). This is practically true for gate dielectric thickness monitoring, as it is a fundamental parameter to control to attain high device performances. TEM provides a direct measure of the physical thickness. The physical thickness of the bulk Zr-oxynitride decreases as the oxidation/nitridation temperature increases (Fig. 9). Conversely, interfacial layer thickness that formed in between the bulk Zr-oxynitride and SiC substrate increases with the increasing oxidation/nitridation temperature. In general, the total thickness of the combined oxide (bulk and interfacial layer) reduces with the increase of oxidation/nitridation temperature. Qualitatively, from the

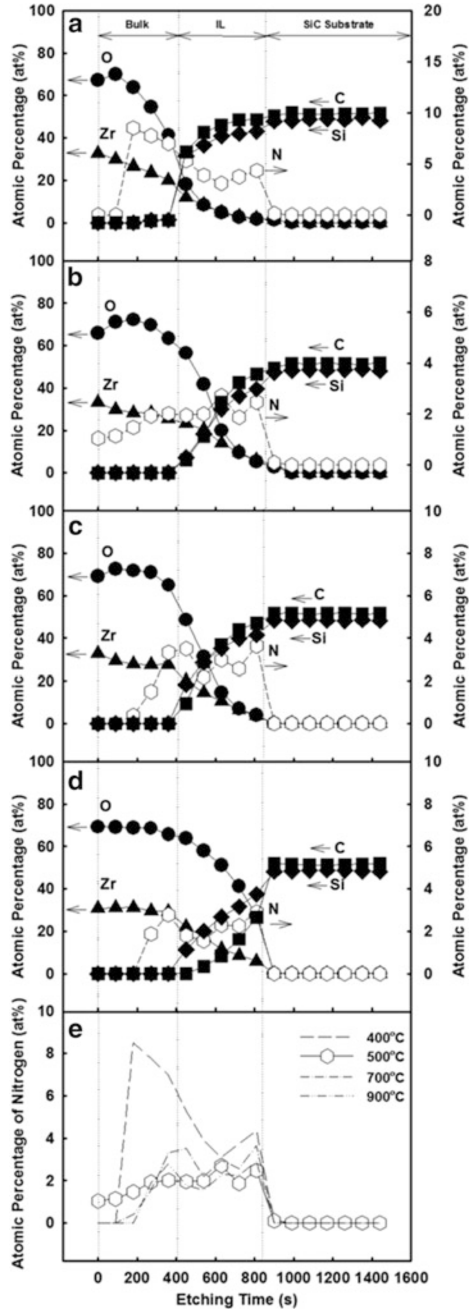

Fig. 4 Atomic percentage of Zr, Si, O, N, and C as a function of etching time for sample oxidized/nitrided samples at (**a**) 400 °C, (**b**) 500 °C, (**c**) 700 °C, (**d**) 900 °C, and (**e**) nitrogen depth profile of all investigated samples

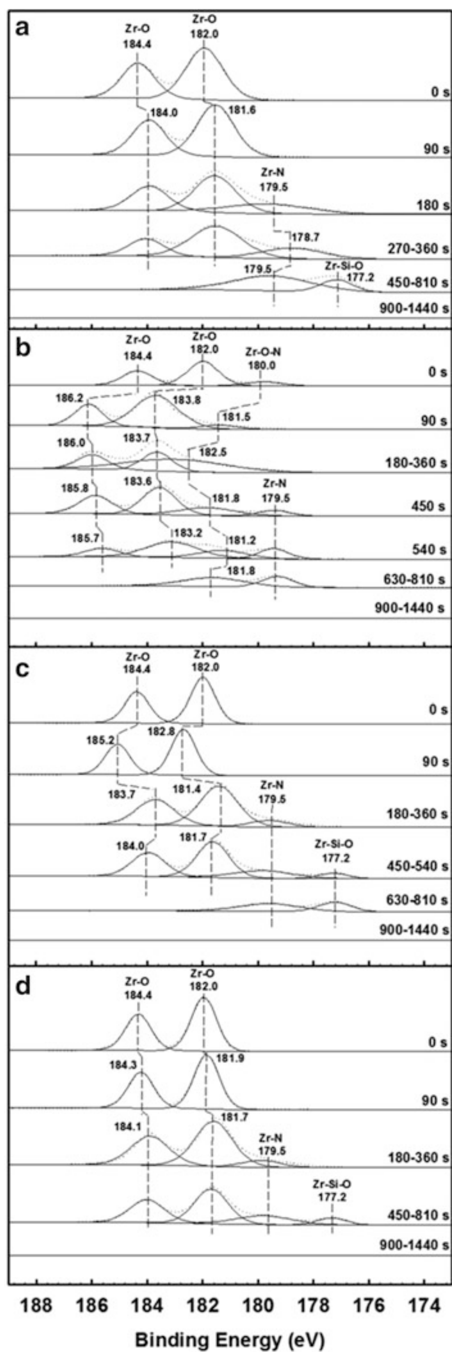

Fig. 5 Evolution of Zr 3*d* core level XPS spectra as a function of etching time for different oxidation/nitridation temperature samples: (**a**) 400 °C, (**b**) 500 °C, (**c**) 700 °C, and 900 °C

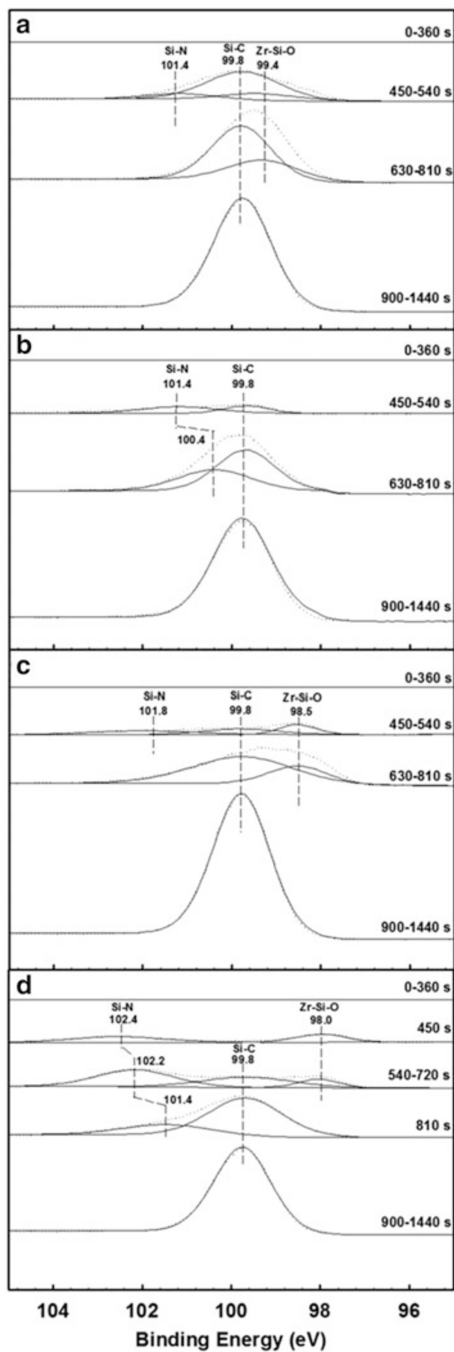

Fig. 6 Evolution of Si 2*p* core level XPS spectra as a function of etching time for different oxidation/nitridation temperature samples: (**a**) 400 °C, (**b**) 500 °C, (**c**) 700 °C, and 900 °C

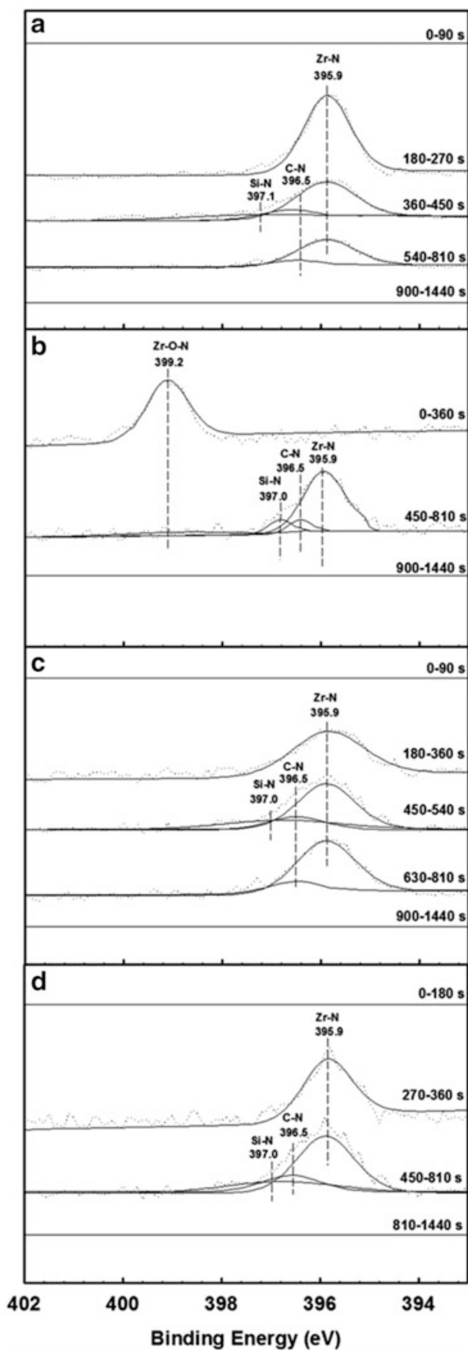

Fig. 7 Evolution of N 1*s* core level XPS spectra as a function of etching time for different oxidation/nitridation temperature samples: (**a**) 400 °C, (**b**) 500 °C, (**c**) 700 °C, and 900 °C

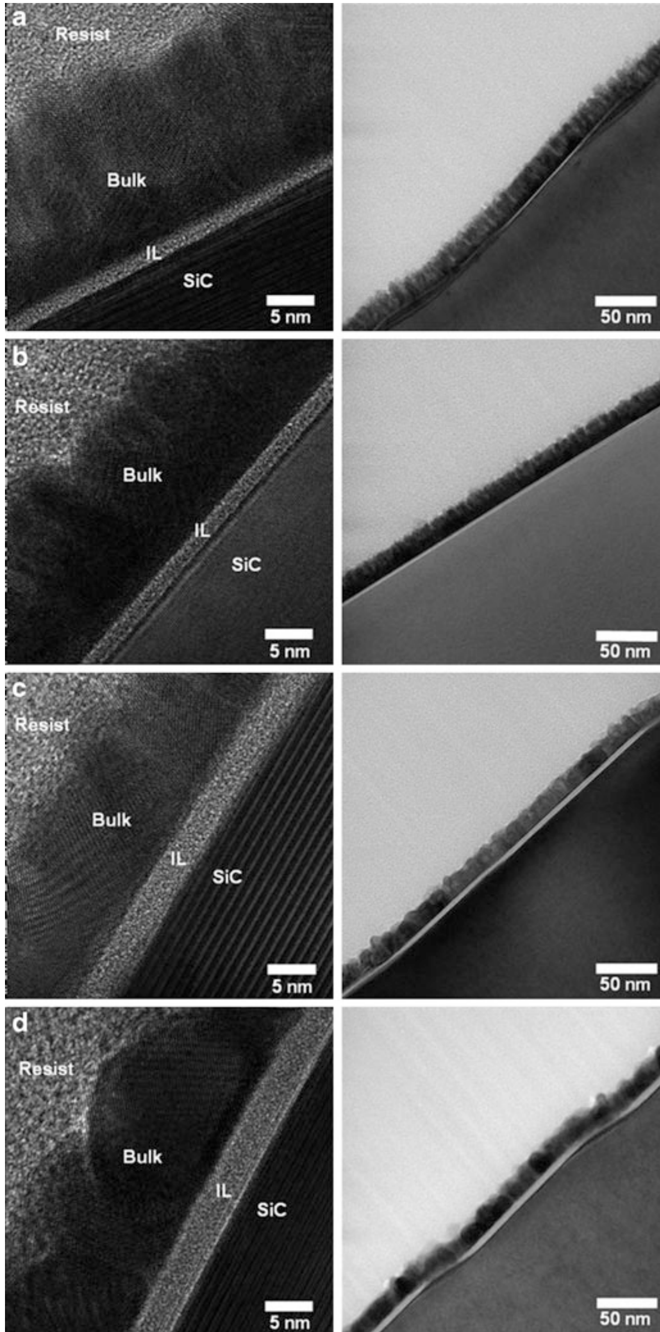

Fig. 8 Cross-sectional EFTEM images of the investigated samples at different oxidation/nitridation temperatures: (**a**) 400 °C, (**b**) 500 °C, (**c**) 700 °C, and (**d**) 900 °C. Lower magnification of each of the investigated samples is shown on the right side respectively

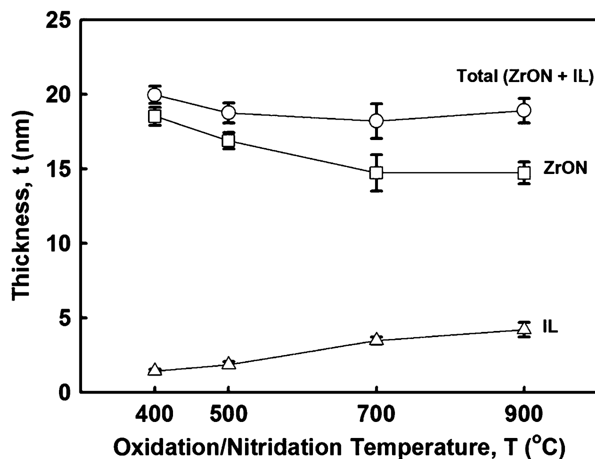

Fig. 9 Average thicknesses of Zr-oxynitride, IL, and total (Zr-oxynitride + IL) for the investigated samples. Error bars define the maximum and minimum thicknesses obtained

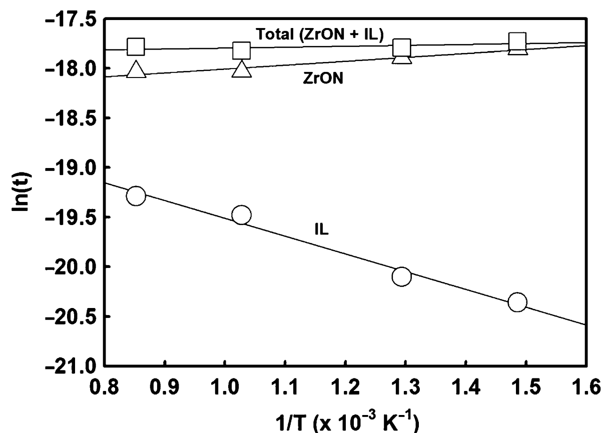

Fig. 10 Arrhenius plots of Zr-oxynitride, IL, and total (Zr-oxynitride + IL) growth in the N_2O ambient

images with lower magnification (Fig. 8), the oxidized/nitrided Zr film at 500 °C has the smoothest surface. Quantitatively, it has the smoothest surface with RMS roughness value of 2.45 nm with wavy topography, as reported by Wong and Cheong (2012b).

It is known that Zr-oxynitride thin film, along with its interfacial layer, can be formed on SiC substrate at processing temperatures of 400–900 °C for a duration of 15 min. However, the activation energies for the formation of Zr-oxynitride thin film and its interfacial layer still remain a question. In order to answer this question, Wong and Cheong (2012b) extrapolated Arrhenius plots of Zr-oxynitride, interfacial layer, and total (Zr-oxynitride + interfacial layer) growth in the N_2O ambient, as shown in Fig. 10. The calculated E_a for the Zr-oxynitride, interfacial layer, and total growth are –0.0335, 0.1543, and –0.0078 eV, respectively. The negative signs of E_a indicate that the rate of reaction decreases as the oxidation/nitridation

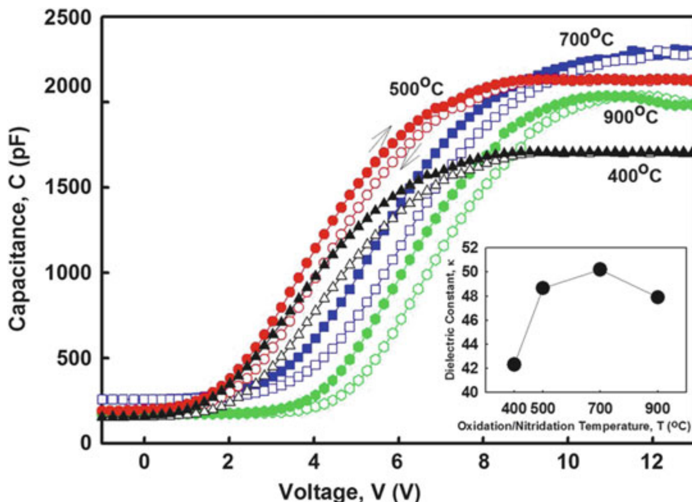

Fig. 11 *C-V* characteristics of MOS capacitors with Zr-oxynitride oxidized/nitrided at various temperatures (400–900 °C). The inset shows effective dielectric constant of the investigated samples deduced from the *C-V* measurement as a function of oxidation/nitridation temperatures (400–900 °C)

temperature increases. In a nutshell, the densification happens with increasing temperature. The positive sign of E_a indicates an increment of reaction rate as the temperature increases. It may indicate an expansion of the investigated layer happens as the temperature increases. On the other hand, the tendency of a reaction or growth to happen can be determined by the magnitude: a small magnitude indicates a fast growth, while a large magnitude indicates a slow growth.

Complementarily, the aforementioned physical characteristics of oxidized/nitrided Zr film on SiC substrate can be further supported by XRD and Raman analyses, as reported by Wong and Cheong (2012b). From both XRD and Raman analyses, they concluded that ZrO_2 was in tetragonal phase, while the remaining undetected compounds are in amorphous structure.

Electric Characteristics of Oxidized/Nitrided Zr Film on SiC

After discussing the physical effects of simultaneous oxidation and nitridation technique on sputtered Zr film on SiC, it is now to explore the practicality and functionality of the film as high-κ dielectric in MOS devices. In order to examine the main MOS characteristics, the capacitance-voltage (*C-V*) and leakage current density-electric field (*J-E*) measurements are the most commonly applied techniques. According to the report byWong and Cheong (Wong and Cheong 2012b), from a correctly obtained high-frequency C-V curve, as demonstrated in Fig. 11, several parameters such as dielectric constant, flat-band voltage, gate accumulation,

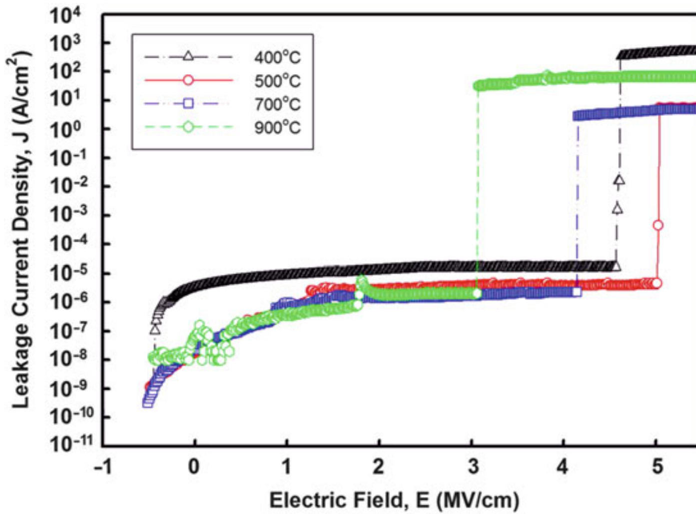

Fig. 12 *J-E* characteristics of investigated samples oxidized/nitrided at various temperatures (400–900 °C)

gate depletion, effective oxide charge, slow trap density, and interface trap density can be extracted. On the other hand, the *J-E* characteristics of the oxidized/nitrided Zr films on SiC were investigated, as shown in Fig. 12. It verifies that 500 °C oxidized/nitrided Zr film on SiC yielded the best result, owing to the highest electric breakdown field of 5.05 MV cm^{-1} at 10^{-6} A cm^{-2}. This is ascribed to the reduction in interface trap density, total interface trap density, effective oxide charge, and increment of barrier height between conduction band edge of the film and semiconductor. The oxidized/nitrided Zr film on SiC yielded its capacitance of 2,147 pF, effective oxide charge of -5×10^{13} cm^{-2}, slow trap density of 6×10^{12} cm^{-2}, total interface trap density of 3.7×10^{13} cm^{-2}, and dielectric constant of 49.68.

Growth Mechanism of Simultaneous Thermal Oxidation and Nitridation of Zr Film on SiC

Based on the report by Wong and Cheong (2011d), a possible model of oxidation and nitridation mechanisms of sputtered Zr on SiC substrate using N_2O gas at temperatures of 400–900 °C can be deduced and is summarized as follows. Due to the fast initial oxidation of Zr at room temperature, a very thin monolayer (~1 nm) of ZrO_2 is formed on the topmost surface. Since Zr cations in ZrO_2 is an effective catalyst for the decomposition of N_2O above 350 °C, hence, N_2O may decompose exclusively to N and O compounds. In the decomposition of N_2O into N and O compounds, there is no free energy change as a function of temperature. Therefore, the decomposition is a spontaneous reaction at those investigated temperatures.

At 400 °C, Zr cations as catalytic ions help to decompose N_2O into N and O compounds. As oxygen atoms are easily being sensed and absorbed by metallic Zr, the absorbed O atoms may react with Zr to form Zr-O compound. This process may proceed further inward, depending on the availability of oxygen produced at this temperature. A stoichiometric Zr-O (ZrO_2) is formed when sufficiently high concentration of oxygen is supplied. As the thickness of ZrO_2 increases, less oxygen may diffuse in and cause an incomplete reaction between Zr and O. Thus, a sub-stoichiometric Zr-O compound is formed toward the interfacial layer between the stoichiometric Zr-O (ZrO_2) compound and the SiC substrate.

Simultaneously, nitridation process happens. Since N atoms are smaller than O atoms, N atoms may diffuse faster than O atoms at the same processing temperature and duration. Since Zr-O involved is sub- or nonstoichiometric, the formation of Zr-N is more favorable. N atoms may diffuse further inside and react with sub-stoichiometric Zr-O to form Zr-N compound by releasing oxygen or react with unreacted Zr to form Zr-N compound. The Zr-N compound may be embedded in the Zr-O layer toward the interfacial layer. Hence, Zr-oxynitride layer consists of Zr-O and Zr-N, with Zr-O-rich compound located at the topmost surface and Zr-N-rich compound located at the near-interface region. The released O atoms from the formation of Zr-N compound and an inward diffusion of O atoms from the ambient may react with the unreacted Zr and bridge to the topmost Si layer (dangling Si bonds) of the bulk-terminated SiC surface, thus forming Zr-Si-O compound. Alternatively, O atoms in the sub-stoichiometric Zr-O may react and bridge to the Si dangling bonds of the bulk-terminated SiC surface, forming Zr-Si-O compound. In other words, the O atom in Zr-Si-O compound helps to passivate the dangling Si bonds and functions as a connector to connect Zr-oxynitride network with SiC substrate.

The excessive N atoms which diffuse further inside toward the interfacial layer also help to passivate the dangling Si bonds by forming Si-N compound. In addition, minute amount of Si atoms from the SiC substrate may diffuse out to form Si-N compound as well.

Due to the catalytic effect offered by Zr and/or ZrO_2, SiC may be slightly decomposed at low temperature of 400 °C. As a result from the minute out-diffusion of Si atoms from SiC substrate, there are minute C atoms that diffuse out as well. These out-diffusing C atoms will react with N atoms in the interfacial layer, forming C-N bonds. The formation of C-N bonds essentially removes the carbon and the formed carbon clusters.

As the oxidation/nitridation temperature is elevated at 500–900 °C, stoichiometric Zr-O (ZrO_2) can also be formed when sufficiently high concentration of oxygen is supplied. Moreover, more O atoms are produced and able to diffuse further inside; hence, more Zr-O bonds (sub-stoichiometric Zr-O) are formed toward the interfacial layer. Concurrently, more N atoms are able to diffuse in and react with sub-stoichiometric Zr-O to form Zr-N compound by releasing oxygen or react with unreacted Zr to form Zr-N compound toward the interfacial layer. Excessive N atoms may also diffuse further inside toward the interfacial layer to passivate the dangling Si bonds by forming Si-N compound. Minute out-diffusing Si and C atoms

from the SiC substrate may react with inward-diffusing N atoms to form Si-N bonds and C-N bonds, respectively. On the other hand, bridging O atoms in Zr-Si-O compound are formed at elevated temperatures of 700–900 °C.

At a specific temperature of 500 °C, it is postulated that a mixture of sub-stoichiometric Zr-O and Zr-N compounds is in the midst of exchanging and balancing the O and N atoms among themselves in order to achieve thermodynamic equilibrium condition. As a result, Zr-O-N compound is formed. During the process of exchanging O and N atoms among Zr-O and Zr-N compounds, there are also N atoms from the ambient that diffuse in and incorporate substitutionally and/or interstitially into stoichiometric Zr-O (ZrO_2) region, forming Zr-O-N compound. Hence, Zr-oxynitride layer formed at this temperature consists of Zr-O and Zr-O-N, with Zr-O-rich compound located at the topmost surface and Zr-O-N-rich compound located at the near-interface region.

Comparison of Oxidized/Nitrided Zr Thin Films on Si and SiC Substrates

After the experiments of simultaneous thermal oxidation and nitridation of sputtered Zr on Si and SiC substrates in 100 % N_2O were conducted, the optimized parameters in terms of oxidation/nitridation temperatures and duration were obtained. The optimized parameters are tabulated in Table 2. For Si-based samples, the oxidation/nitridation temperature was optimized at 700 °C, whereas for SiC-based samples, the temperature was optimized at 500 °C, with their durations of 15 min for both samples.

Structural and Chemical Properties

Structural and chemical properties of oxidized/nitrided Zr thin films on Si and SiC substrates in 100 % N_2O are compared in Table 3. It shows that ZrO_2 was formed with IL of Zr-silicate oxynitride (ZrSiON) on Si-based substrate, while Zr-oxynitride (ZrON) was formed with an IL comprised of ZrSiON and carbon nitride (CN) on SiC-based substrate. In both Si-based and SiC-based samples, IL of ZrSiON was produced with different combinations of mixed compounds. Distribution of nitrogen in the SiC-based sample is more uniform, with higher maximum atomic percent, as compared to Si-based sample. However, the conduction band offsets (ΔE_c) of SiC-based sample is lower than Si-based sample, owing to the

Table 2 Optimized parameters of simultaneous oxidation and nitridation of sputtered Zr on different semiconductor substrates of Si and SiC in 100 % N_2O

Base substrate	Optimized temperature (°C)	Optimized duration (min)
Si	700	15
SiC	500	15

Table 3 Comparison of structural and chemical properties of oxidized/nitrided sputtered Zr based on Si and SiC substrates

Characterization tools	Properties	Unit	Si based	SiC based
XPS	Chemical composition of bulk	–	ZrO_2 (Zr-O)	Zr-oxynitride (Zr-O and Zr-O-N)
	Chemical composition of IL	–	Zr-O, Zr-N, Zr-Si-O, and Si-N	Zr-O, Zr-N, Zr-O-N, Si-N, and C-N
	Distribution profile of nitrogen	–	Relatively less uniform	Relatively more uniform
	Maximum atomic percent of nitrogen	at%	2.20	2.71
	E_g of bulk extracted from XPS	eV	6.40	5.00
	E_g of IL extracted from XPS	eV	8.80	8.50
	ΔE_c extracted from XPS	eV	3.40	2.00
EFTEM	Thickness of bulk	nm	6.00	16.90
	Thickness of IL	nm	4.00	1.86
	Total thickness (Bulk + IL)	nm	10.00	18.76
AFM	RMS value	nm	0.50	2.45
XRD	t-ZrO_2 planes	–	(101) and (002)	(011) and (002)

combination of relatively narrower bandgaps of Zr-oxynitride and IL. This could lead to a reduced breakdown field of the sample. Through EFTEM analysis (Fig. 13 and Table 3), a thicker Zr-oxynitride, with a thinner IL, was produced on SiC-based substrate as compared to Si-based substrate. This could help in enhancing the oxide capacitance (C_{ox}) and κ value of the film on SiC-based sample. There are two different two-dimensional (2D) surface topographies of ZrO_2 and Zr-oxynitride on Si and SiC substrates, respectively, as shown in Fig. 14. The produced Zr-oxynitride is in wavy topography on SiC substrate, while ZrO_2 is in non-wavy topography. With that, it was found that the ZrO_2 thin film on Si substrate has smoother surface, with lower RMS value, as compared to Zr-oxynitride thin film on SiC substrate. The crystalline planes of t-ZrO_2 on Si-based sample are (101) and (002), whereas on SiC-based sample are (011) and (002).

Electric Properties

Table 4 compares the electric properties of oxidized/nitrided Zr thin films on Si and SiC in 100 % N_2O, in terms of *C-V* and leakage current density-electric field (*J-E*) characteristics. It shows that SiC-based sample has higher C_{ox} than Si-based

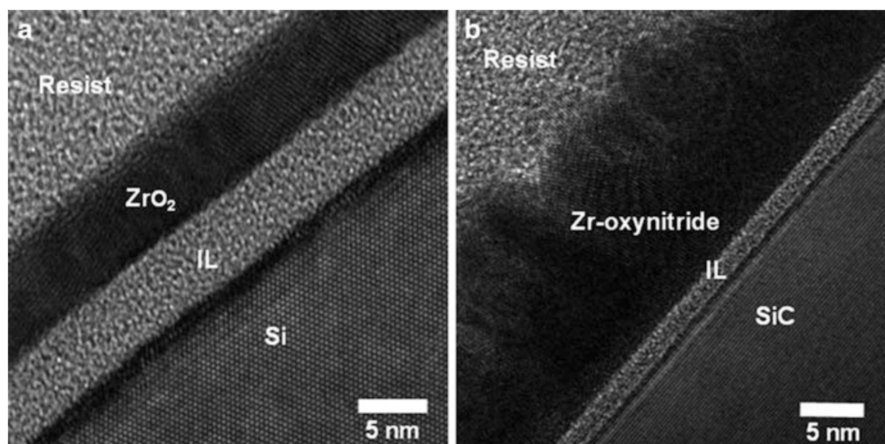

Fig. 13 Cross-sectional EFTEM images of (**a**) ZrO_2 on Si substrate and (**b**) Zr-oxynitride on SiC substrate

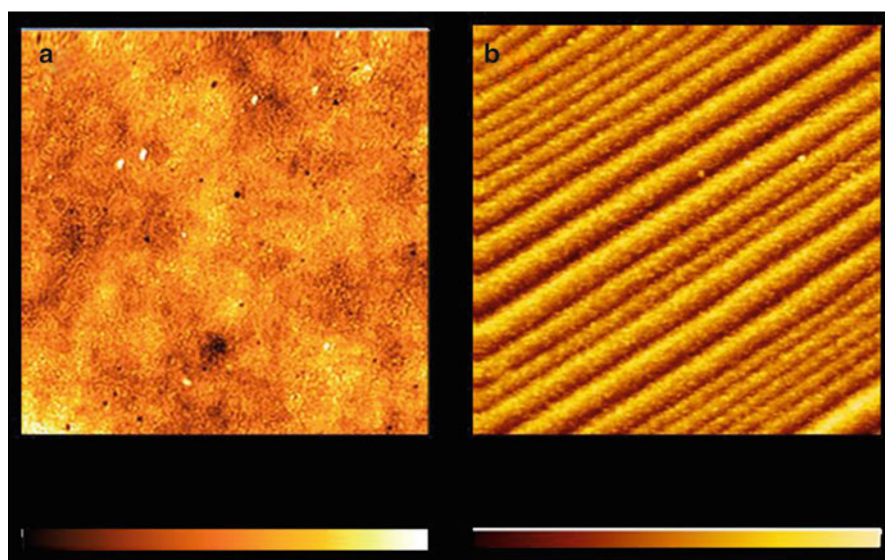

Fig. 14 Two-dimensional AFM surface topography of (**a**) ZrO_2 on Si substrate and (**b**) Zr-oxynitride on SiC substrate

sample. This is attributed to the higher κ value and/or reduced IL thickness. As possessed in the table, the κ value of the film in SiC-based sample is double the κ value of the film in Si-based sample, while the IL thickness in the SiC-based sample is half the IL thickness in the Si-based sample. SiC-based sample showed an

Table 4 Comparison of electric properties of oxidized/nitrided sputtered Zr based on Si and SiC substrates

Measurements	Properties	Unit	Si based	SiC based
C-V	C_{ox}	pF	1,731	2,147
	Q_{eff}	cm^{-2}	$+4.50 \times 10^{11}$	-5.00×10^{13}
	STD	cm^{-2}	4.62×10^{11}	$+6.00 \times 10^{12}$
	D_{it} at $(E_c–E) = 0.15–0.25$ eV	eV^{-1} cm^{-2}	Mid $10^{12}–10^{13}$	10^{14}
	D_{total}	cm^{-2}	7.00×10^{12}	3.70×10^{13}
	κ	–	21.82	49.68
J-E	E_{HDB}	MV cm^{-1}	13.60	5.05
	J	A cm^{-2}	10^{-6}	10^{-6}
	ϕ_B	eV	1.33	1.67

enormous *C-V* curve shift to the positive voltage. This has been affirmed by the presence of enormous amount of negative effective oxide charge (Q_{eff}) in the oxide. As for Si-based sample, the *C-V* is shifted slightly to the negative voltage; thus, a lower positive Q_{eff} was recorded. A relatively larger hysteresis, with higher STD of one order of magnitude, was identified as compared in SiC-based sample to Si-based sample. Interface trap density (D_{it}) and total interface trap density (D_{total}) in SiC-based sample are higher than in Si-based sample. According to *J-E* characteristics, SiC-based sample has lower breakdown field (E_{HDB}) than Si-based sample. This could be due to higher Q_{eff}, STD, D_{it}, D_{total}, and lower ΔE_c (Table 3) in the SiC-based sample. The barrier height between the oxide and the semiconductor (ϕ_B) obtained in SiC-based sample is higher than in Si-based sample. The difference in ΔE_c and ϕ_B may be ascribed to the following reasons and assumptions (de Almeida and Baumvol 2003). First, by using Fowler-Nordheim (FN) plot, the calculated ϕ_B takes into account the barrier height lowering and quantization of electrons at the semiconductor surface, and it is not strictly constant. Second, it could be attributed to the electron and oxide effective masses.

Summary

Evolution and justification of substituting nitrided-SiO_2 to high-κ oxide on SiC have been reviewed, with a detailed discussion of high-κ gate dielectric characteristics and the current knowledge of simultaneously oxidized and nitrided Zr film as high-κ dielectric on SiC. Via this technique, the role of N_2O gas ambient on oxidizing and nitriding Zr film on SiC, coupling with physical and electric characteristics of oxidized/nitrided Zr film on SiC, has been discussed. Finally, a growth mechanism of simultaneous thermal oxidation and nitridation of Zr film on SiC is presented. Physical and electric properties of oxidized/nitrided Zr thin film on 4H-SiC substrate in N_2O ambient for different oxidation/nitridation temperatures

(400–900 °C) were presented. Bulk Zr-oxynitride was formed, which consists of a tetragonal phase of polycrystalline ZrO_2 with embedment of amorphous Zr-N and/or Zr-O-N. The IL may be comprised of sub- or nonstoichiometric Zr-O, Zr-N, Zr-O-N, Zr-Si-O, Si-N, and C-N, which are in amorphous structure. These properties were subsequently related to the electric characteristics of the films evaluated by MOS structures. From the electric characteristics, it was verified that 500 °C oxidized/nitrided sample gave the best result, owing to the highest electric breakdown field of 5.05 MV cm^{-1} at 10^{-6} A cm^{-2}. This is attributed to the reduction in interface trap density, total interface trap density, effective oxide charge, and increment of barrier height between conduction band edge of the film and the semiconductor.

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