Chapter 8
Feedback Control of the DC/DC Converters for PV Source Emulation

8.1 Negative Feedback Classical Control

In general, the aim of a voltage source like a DC/DC converter consists in obtaining a voltage equal to a desired value assumed as the reference value.

As explained in Chap. 7, in practical cases, the output of a DC/DC converter is different from the theoretical value. Several factors contribute to this phenomenon, some of these are tied to the parasitic parameters of the converter components, they are quite constant during operation but can vary from one device to another and should be measured. Other parameters as the duty cycle and the load value normally vary and modify the output value as well.

For these reasons, the open-loop operation is not satisfactory and a feedback action is required. In this case, the output is continuously measured and its value is compared to the reference one. Depending on the difference between them, a correction action is imposed to the converter.

Moreover, for a PV source emulation, in which the output voltage has to follow a reference that is related to the source to be emulated, a feedback action allows the desired dynamical behavior of the real source to be obtained too.

8.1.1 Closed-Loop Gain

Figure 8.1 shows a block diagram of a closed-loop system. The original system has a transfer function A; a feedback network with transfer function β is added.

The input of the closed-loop system is the desired output value V_{ref}; the obtained output V_o is processed by the feedback network, then the difference with the reference value, that represents the error signal, is the input of the system to be controlled.

M. C. Di Piazza and G. Vitale, *Photovoltaic Sources*, Green Energy and Technology,
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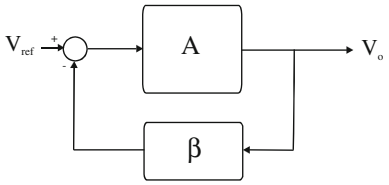


Fig. 8.1 Block diagram representation of a closed-loop system

The closed-loop transfer function is given by:

$$\frac{V_o}{V_{\text{ref}}} = \frac{A}{1 + \beta A} \tag{8.1}$$

The open loop transfer function is defined as:

$$L = \beta A \tag{8.2}$$

Some considerations are worth being considered. Firstly, if the open loop gain is sufficiently high, Eq. (8.1) becomes:

$$\frac{V_o}{V_{\text{ref}}} \approx \frac{1}{\beta}\bigg|_{A \gg \beta} \tag{8.3}$$

In this case, the behavior of the feedback system depends only on the feedback network.

Usually, the denominator of Eq. (8.1) depends both on the system and feedback network transfer functions. Some frequencies could nullify the value of $1 + \beta A$; for these values, the Eq. (8.1) would not be defined. In practice, this lead to a system instability. This situation must be avoided; to this aim, some techniques as compensation networks, or pole placement are adopted. They will be explained in the following.

8.1.2 Stability Analysis

The loss of stability for a system, defined by Eq. (8.1), can be described by the following conditions:

$$\begin{cases} |\beta A| = 1 \\ \text{phase}(\beta) + \text{phase}(A) = 180^\circ \end{cases} \tag{8.4}$$

In this case, the denominator of Eq. (8.1) has a zero that lies in the imaginary axis. From a physical point of view, if the conditions expressed by Eqs. (8.4) occur, the input signal of the feedback system goes through the loop formed by the block described by transfer function A, the feedback network β, then it is rotated of 180° by the minus sign and it is superimposed to the original signal with the same amplitude and phase. A new signal with an amplitude twice of the original is obtained and so on, until a nonlinearity occurs. In such a condition, oscillations, high amplitudes, and the loss of the small signal hypothesis make the system uncontrollable.

Moreover, Eqs. (8.4) express a limit condition that can be reached during normal operation due to several factors as noise, ageing, etc. For these reasons, it is preferable to design the feedback system so to work quite far from Eq. (8.4). This is known as *relative stability* of the system. Two parameters are introduced to characterize the relative stability of the system; they represent how much the system is far from the conditions expressed by Eqs. (8.4).

The first parameter is the *gain margin*, it is defined as the gain, calculated on the open-loop transfer function L, to drive the system into instability. In other words, it is the amount of gain needed to obtain a unitary gain of L when its phase is equal to 180°. Usually the gain is expressed in dB, as a consequence the gain margin is the quantity to be added to the gain of L to obtain 0 dB, when its phase is 180°.

The second parameter is the *phase margin*, it defined as the opposite of the phase shift necessary to make the phase of L equal to −180°, when the gain is 0 dB.

To ensure stability, usually a gain margin of 6 dB and a phase margin of about 45° have to be assured; when this is not provided directly from the open loop transfer function, an additional network must be designed.

Both the gain and phase margins can be deduced by the Bode plot of the open-loop transfer function.

As an example of a stable system, the open-loop transfer function defined by Eq. (8.5) can be considered. The feedback network transfer function is supposed unitary for simplicity.

$$L_1(s) = \frac{0.4}{s(s^2 + s + 1)} \tag{8.5}$$

Its bode plot can be drawn by the following MATLAB® script:

```
**********************************************
    %transfer function parameters

    a=1;
    b=1;
    gain=0.4;


    s=tf('s');

    L=gain/(s*(s^2+a*s+b));

    MARGIN (L);

    hold
**********************************************
```

where the use of the command MARGIN allows both gain and phase margins to be calculated (Fig. 8.2).

It can be noted that, when the gain curve reaches the value of 0 dB (unitary gain condition), the phase is about 61°; when the phase is equal to 180° the gain is about −7.9 dB. These conditions characterize the system defined by Eq. (8.5) as stable.

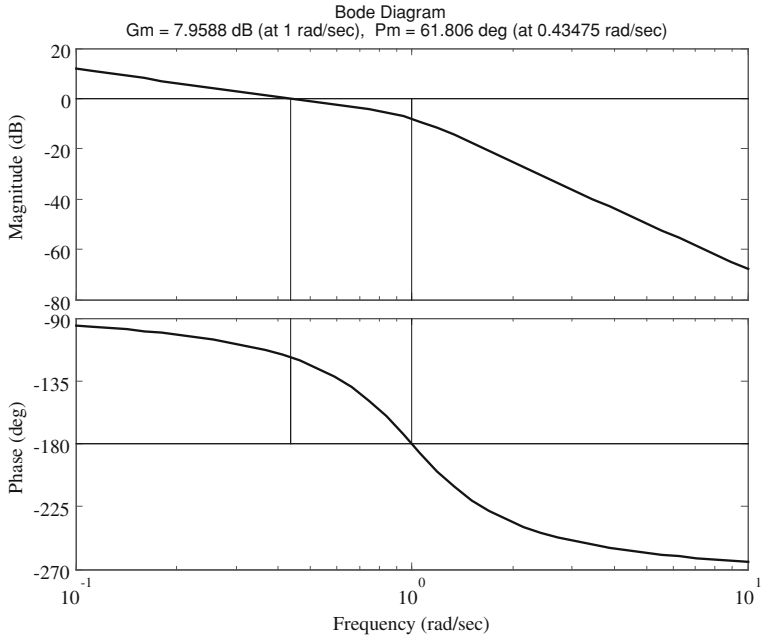


Fig. 8.2 Bode plot of the transfer function defined by Eq. (8.5)

The pole position of the transfer function described by Eq. (8.5) can be obtained by POLE function in MATLAB®

```
************************************************
    >> pole(L)

    ans =

            0
      -0.5000 + 0.8660i
      -0.5000 - 0.8660i

************************************************
```

The system has one pole at the origin and a couple of complex conjugate poles with negative real part.

The system defined by the open-loop transfer function in Eq. (8.6) is now considered. The Eq. (8.6) has a pole at the origin and two real negative poles equal to $p_1 = -9.899$ and $p_2 = -0.1010$. By observing its bode diagram, it can be noted that the system, nevertheless the presence of two real and negative poles, when operated in a closed loop with a unitary feedback ($\beta = 1$ in Fig. 8.1), is unstable. As a matter of fact, the gain margin is negative and the phase margin approaches 0°, it corresponds to superimpose, inside the feedback loop, signals with the same phase and equal amplitude (Fig. 8.3).

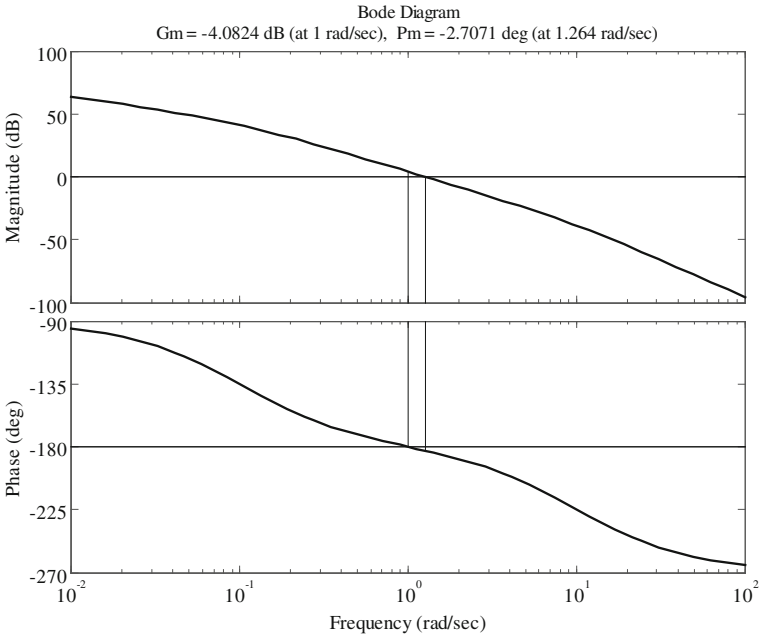


Fig. 8.3 Bode plot of the transfer function defined by Eq. (8.6)

$$L_2(s) = \frac{16}{s(s^2 + 10s + 1)} \tag{8.6}$$

Finally, the open loop transfer function in Eq. (8.7), characterized by a pole at the origin and two complex conjugate poles $p_{1,2} = -0.0500 \pm \text{j}0.9987$, represents a critical system in which the mere calculus of gain and phase margin would give a stable system; on the other hand, by the bode plot it is evident that a resonance occurs and the related peak reaches the unitary gain when the phase is 180°. In this condition, the system can become unstable (Fig. 8.4).

$$L_3(s) = \frac{0.08}{s(s^2 + 0.1s + 1)} \tag{8.7}$$

From what explained above, the bode diagram of the open-loop transfer function allows the stability to be studied without the calculus of the closed-loop transfer function. This is usually more complicated; for example, for the system defined by Eq. (8.6), the closed-loop transfer function is given by

$$C_2(s) = \frac{L_2(s)}{1 + \beta L_2(s)} = \frac{\frac{16}{s(s^2+10s+1)}}{1 + \beta \frac{16}{s(s^2+10s+1)}} \tag{8.8}$$

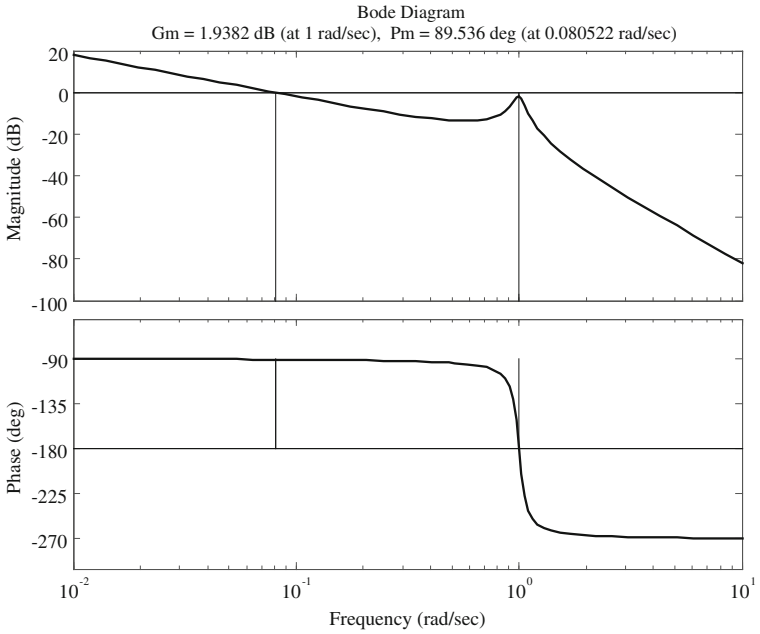


Fig. 8.4 Bode plot of the transfer function defined by Eq. (8.7)

The pole values of $C_2(s)$, for $\beta = 1$ can be calculated by the command RLOCUS in MATLAB®, where L is the open-loop transfer function.

```
************************************************
    >> R=RLOCUS(L,1)

    R =

     -10.0587
       0.0294 + 1.2609i
       0.0294 - 1.2609i
************************************************
```

It can be noted that the feedback system has a couple of complex conjugate poles with positive real part.

In general, the β value can be considered as a parameter, in this case the poles of the closed-loop transfer function describe a locus known as *root locus*. It can be plotted by using the command RLOCUS (H) in MATLAB®.

From what is shown above, a system having an open-loop transfer function with all negative real part poles can become unstable in a feedback connection or its gain and phase margin can be unsatisfactory. In this case, the open-loop transfer function needs a correction obtained by a properly designed compensation networks.

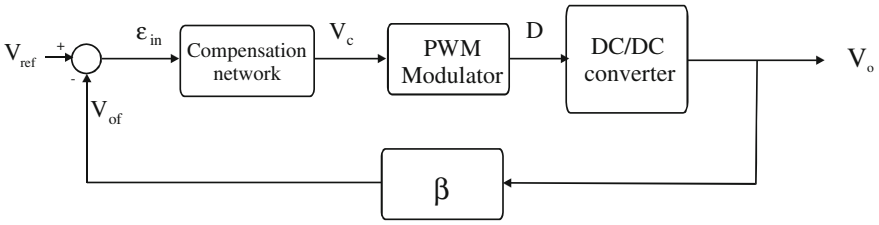


Fig. 8.5 Feedback structure of a DC/DC converter

8.2 Feedback Structure of a DC/DC Converter

A DC/DC converter in a feedback structure can be represented as in Fig. 8.5.

An error signal ε_{in} is obtained by subtracting the output voltage V_o, processed by the feedback network, from the desired voltage signal V_{ref}. A compensation network, having ε_{in} as input, provides the control voltage V_c that is applied to the modulator from which the duty cycle is obtained.

The DC/DC converter transfer function (for the case of buck, boost and buck-boost topologies) has been calculated in Chap. 7, here the other parts are deduced.

8.2.1 Feedback Network Transfer Function

The feedback networks can be formed by a voltage transducer or simply by a voltage divider (see Sect. 7.2.1); their aim is to manage a reduced signal compared to the output value. In the case of a voltage divider, the transfer function is given by:

$$V_{of} = \frac{R_2}{R_1 + R_2} V_o \tag{8.9}$$

8.2.2 Pulse Width Modulator Transfer Function

The pulse width modulation (PWM) provides the duty cycle D obtained, for example, by comparing a sawtooth signal with the control voltage V_c. This operating mode is called voltage mode control.

The duty cycle ranges from zero to unitary value. The sawtooth frequency corresponds to the DC/DC converter switching frequency. When the control voltage equals the maximum value of the sawtooth, the duty cycle approaches 1. The modulator gain is given by:

$$G_{\mathrm{PWM}} = \begin{cases} 1 & V_c \geq V_{\mathrm{sw}} \\ \frac{1}{V_{\mathrm{sw}}} & 0 > V_c > V_{\mathrm{sw}} \\ 0 & V_c < 0 \end{cases} \tag{8.10}$$

Therefore, any duty cycle value can be obtained by the product of the modulator gain G_{PWM} and the control voltage V_c.

The first and the last conditions in Eq. (8.10) must be avoided to maintain the linear operating conditions.

In current mode control, the duty cycle is obtained by comparing the inductor current with a reference one. This operating mode is not treated here.

8.2.3 Compensation Networks

The aim of a compensation network is to assure the stability of the feedback system by a suitable gain and phase margin. Moreover, a correct design allows the closed-loop system poles to give the desired transient time-domain response.

A great part of compensating networks are based on a linear combination of the error signal of its integral and of its derivative. Among them, the proportional-integrative (PI) network and the proportional-integrative-derivative (PID) network are commonly used.

The design of a compensation network comes from a trade-off among several constraints. The three main system characteristics are:

1. Steady-state performance: they are usually expressed in terms of the maximum error for a given input (step or ramp) and are improved by the presence of integrators.
2. Transient performance: the system is required to satisfy the constraint in terms of rise time, settling time, bandwidth, frequency oscillation, and damping in time and frequency domain, respectively. The increase of the gain or the presence of a derivative action improve the dynamic performance, on the contrary the presence of an integrator has the opposite effect.
3. Stability: by increasing the gain or by adding integrators the stability margins are diminished, on the contrary a derivative action increase the damping of the system, supporting stability.

Since all constraint cannot be contemporarily satisfied, first the stability must be guaranteed, then the others parameters are considered according to the main interest of the designer.

The main components of a compensation network perform proportional (P), derivative (D), or integrator (I) action. It is possible to employ a linear combination of them.

The use of a mere proportional action reduces the steady-state error as its gain is increased but it can lead the system to instability; to reduce this error an integrator action can be introduced so that, when the error is different from zero, the

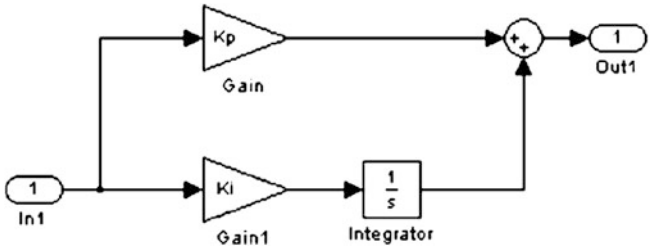


Fig. 8.6 Structure of PI compensating network

integrator increase its contribution. The overall effect of a proportional-integral controller (PI) is to maintain a high gain only at low frequencies.

By using a proportional-derivative-integral (PID) controller, the designer can use three parameters to satisfy the system requirements. The derivative effect reduces the rise time and increases the overshoot of the system response; however, high frequency noise is amplified.

8.2.3.1 PI Compensation

The PI compensation is obtained by adding the input signal, multiplied for a gain K_p, to an other signal obtained by the integration of the input signal multiplied for a gain K_i. A simple block diagram of a PI implemented in Simulink® implementation is given in Fig. 8.6.

The corresponding transfer function has a pole at the origin and a zero whose value is given by $z = K_i/K_p$.

$$\frac{V_c}{\varepsilon_{\text{in}}} = \left(K_p + \frac{K_i}{s}\right) = K_p \frac{s+z}{s} \tag{8.11}$$

It can be noted that Eq. (8.11) exhibits a constant gain for high frequencies. On the other hand, in the case of a DC/DC converter, it is mandatory that, near to the switching frequency, the open-loop gain is sufficiently low to reduce the ripple at the switching frequency. In this case, and additional low pass filter is added to the PI as shown in Fig. 8.7. The obtained transfer function is given by Eq. (8.12).

$$\frac{V_c}{\varepsilon_{\text{in}}} = K_p \frac{s+z}{s(s+p)} \tag{8.12}$$

Figure 8.8 shows the bode diagram of both a PI compensator with $K_p = 3.16$ (corresponding to 10 dB), $z = 1000$ rad/s, and the same compensator with an additional high frequency pole $p = 20000$ rad/s. To compensate the attenuation due to this pole, in this last case, the value of K_p is equal to 63200.

It should be noted that both the networks show a decrease of the gain due to the pole at the origin and a flat zone with 10 dB gain in the region between the zero and the pole. The additional high frequency pole causes a further decrease of the

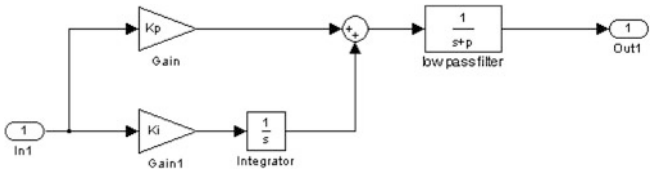


Fig. 8.7 Structure of PI compensating network with additional low pass filter

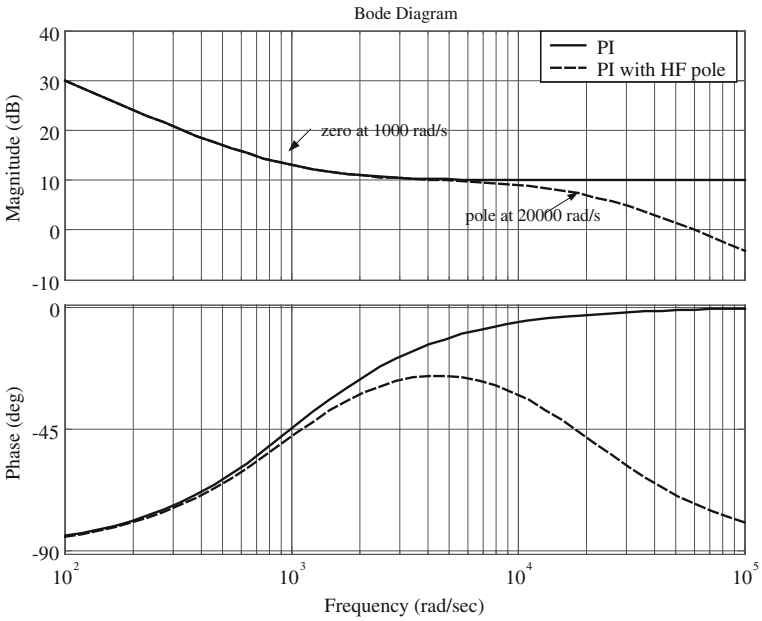


Fig. 8.8 Bode diagram of both a PI compensator and the same compensator with an additional high frequency pole

gain that reaches the value of 0 dB at a pulsation of 60000 rad/s (the pulsation where the gain is 0 dB is usually known as the crossover pulsation). The corresponding crossover frequency, of about 9500 Hz, assures a correct operation for switching frequencies greater than about 40kHz. As a matter of fact, it is necessary to have a switching frequency 4–5 times greater than the crossover frequency to avoid its circulation in the control feedback loop.

Finally, a PI compensator can be realized by a network with capacitors, resistors, and operational amplifiers. In this case, the additional pole presence cannot be avoided because a system physically realizable must have the number of poles greater than the number of zeros. However, if the open-loop transfer function has a satisfactory crossover frequency, the additional pole can be designed so to

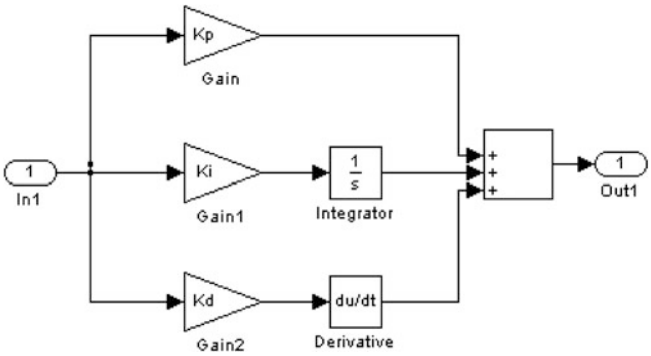


Fig. 8.9 Structure of PID compensating network

have a frequency much greater than the switching frequency. In this case, its presence does not affect the system behavior.

8.2.3.2 PID Compensation

The PID compensation is obtained by adding three signals: the first one is the input signal multiplied for a gain K_p, the second is the integral of the input signal multiplied for a gain K_i , and the last is the derivative of the input signal multiplied for a gain K_d.

A simple block diagram of a PID implemented in Simulink® is given in Fig. 8.9.

The corresponding transfer function has a pole at the origin and two zeros.

The corresponding transfer function is:

$$\frac{V_c}{\varepsilon_{\text{in}}} = \left(K_p + \frac{K_i}{s} + sK_d\right) = \frac{K_d s^2 + K_p s + K_i}{s} = K_d \frac{(s+z_1)(s+z_2)}{s} \tag{8.13}$$

To obtain a suitable crossover frequency, two high frequency poles can be added. In this case, Eq. (8.13) becomes:

$$\frac{V_c}{\varepsilon_{\text{in}}} = K_d \frac{(s+z_1)(s+z_2)}{s(s+p_1)(s+p_2)} \tag{8.14}$$

Figure 8.10 shows the bode diagram of both a PID compensator with $K_d = 3.16$, $z_1 = 100$ rad/s, $z_t = 1000$ rad/s and the same compensator with two additional high frequency poles $p_1 = 5000$ rad/s and $p_2 = 20000$ rad/s and a gain $K_d = 3.16\ 10^8$.

It should be noted that both the networks show a decrease of the gain due to the pole at the origin and a flat zone in the region between the two zeros. After the second zero, the gain increases with a slope of 20 dB/decade, in the case of a PID

with additional poles, the gain trend becomes again flat for the presence of the first pole and finally it decreases with a slope of 20 dB/decade due to the second pole.

8.3 Complete State Feedback (Pole Placement Technique)

As it is known, the poles position is related to the transient response of the system, then, by the knowledge of the time-domain characteristic response, it is possible to determine the system poles which have caused that response.

The complete state feedback technique is based on the sensing of all the state variables of the system that are multiplied for a suitable gain; it allows the poles to be assigned. This last characteristic is of particular importance for system emulation. As a matter of fact, a correct system emulation requires the matching of transient response of the emulator with that of the system to be emulated. In the case of PV emulation, this matching can be achieved by imposing the closed-loop poles to the DC/DC converter used for the source emulation.

A continuous-time linear system is described by the following state space representation (see also (Eq. 7.93)):

$$\dot{\boldsymbol{x}} = \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}\boldsymbol{u} \tag{8.15}$$

where the input vector $\boldsymbol{u}$, that coincides with the control variable, can be expressed as the product of a matrix $\boldsymbol{F}$ multiplied for the state vector $\boldsymbol{x}$, so that:

$$\boldsymbol{u} = -\boldsymbol{F}\boldsymbol{x} \tag{8.16}$$

By substituting Eq. (8.16) in Eq. (8.15), it becomes:

$$\dot{\boldsymbol{x}} = (\boldsymbol{A} - \boldsymbol{B}\boldsymbol{F})\boldsymbol{x} \tag{8.17}$$

The closed-loop poles are the solutions of the characteristic equation:

$$\det[s\boldsymbol{I} - \boldsymbol{A} - \boldsymbol{B}\boldsymbol{F}] = 0 \tag{8.18}$$

It should be noted that the choice of the $\boldsymbol{F}$ matrix allows the closed-loop poles to be arbitrarily assigned.

For a DC/DC converter, the matrices deduced by the state-space averaging can be used. Equation (7.107), here rewritten concisely, can be considered.

$$\dot{\tilde{\boldsymbol{x}}} = \boldsymbol{A}\,\tilde{\boldsymbol{x}} + \boldsymbol{B}\,\tilde{\boldsymbol{u}} + \boldsymbol{E}\tilde{d} \tag{8.19}$$

Supposing that the perturbations act only on the duty cycle, Eq. (8.19) becomes:

$$\dot{\tilde{\boldsymbol{x}}} = \boldsymbol{A}\,\tilde{\boldsymbol{x}} + \boldsymbol{E}\tilde{d} \tag{8.20}$$

By the second of Eq. (8.10) and considering that the control voltage V_c equals the peak of sawtooth, used to obtain PWM, multiplied by the duty cycle, it follows that:

$$\tilde{d} = \left(\frac{D}{V_c}\right)\tilde{v}_c \tag{8.21}$$

The control voltage $\tilde{v}_c$ can be expressed as the product of a matrix $\boldsymbol{\Phi}$ multiplied for the state vector $\tilde{\boldsymbol{x}}$, so that:

$$\tilde{v}_c = -\boldsymbol{\phi}\tilde{\boldsymbol{x}} \tag{8.16a}$$

Now by substituting Eq. (8.21) in Eq. (8.20) and using Eq. (8.16a),

$$\dot{\tilde{\boldsymbol{x}}} = \left(\boldsymbol{A} - \boldsymbol{E}\frac{D}{V_c}\Phi\right)\tilde{\boldsymbol{x}} \tag{8.22}$$

In this case, $\boldsymbol{\Phi}$ is a row vector with two coefficients that have to be determined to assign the poles. These coefficients can be calculated by the MATLAB® command:

```
**********************************************
>> F=PLACE(A, B, P);
**********************************************
```

where A and B are the matrices of the state space representation and P is the vector of the poles to be assigned.

For the buck converter with closed-loop matrix defined by Eq. (8.22), the coefficients of $\boldsymbol{\Phi}$ are calculated by the MATLAB® command:

```
**********************************************
>> F=PLACE(A,E*D/Vc, P);
**********************************************
```

Other two useful MATLAB® commands are:

```
**********************************************
% the vector poles contains the eigenvalues of the A matrix
>> poles = eig(A)
**********************************************
```

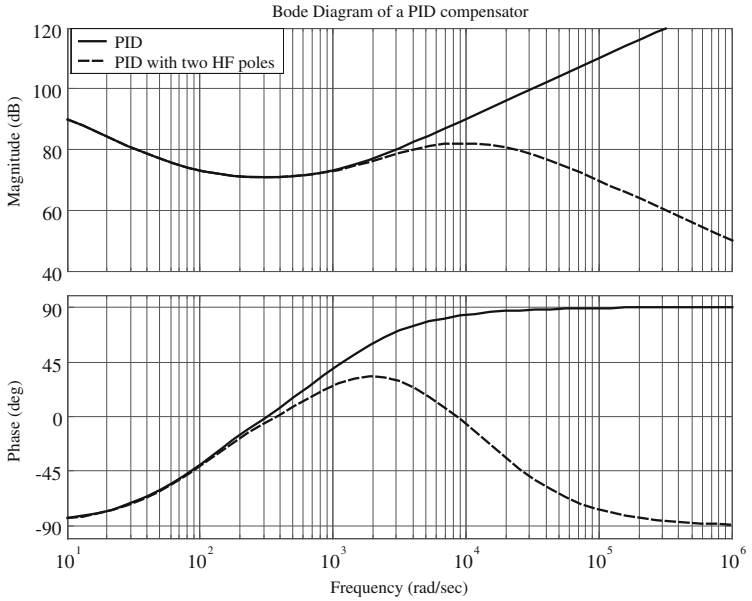


Fig. 8.10 Bode diagram of both a PID compensator and of the same compensator with two additional high frequency poles

and

```
************************************************
% sys command defines the state space model
% step command calculates the step response of the system
>> sys = (A, B, C, 0)
>> step(sys)
************************************************
```

In practise, after the definition of the system poles vector $\boldsymbol{P}$, the coefficient of $\boldsymbol{\Phi}$ are calculated, then the step response can be plotted for the feedback system to verify if the curve matches with that of the source to be emulated.

8.4 Enhanced Pole Placement for Buck Converter

Figure 8.11 shows a buck converter similar to that analyzed in Sect. 7.4 with an additional current generator in parallel to the resistive load. It models the current supplied to an inverter connected to its output. The variable w is the mean voltage supplied by the generator V_s.

The buck converter can be considered as supplied by a generator:

$$w = DV_s \tag{8.23}$$

that represents the control variable.

The circuit is described by equations similar to Eqs. (7.38) and (7.39) slightly modified for the presence of the generator I_{o1}.

$$\begin{cases} w = L\frac{\mathrm{d}i_L}{\mathrm{d}t} + r_L i_L + V_o \\ V_o = v_c + r_c i_c \\ i_L = i_c + I_o + I_{o1} \end{cases} \tag{8.24}$$

$$V_o = R\left(i_L - C\frac{\mathrm{d}v_c}{\mathrm{d}t} - I_{o1}\right) \tag{8.25}$$

The Eqs. (8.24) and (8.25) can be solved for the time derivative of the state variables, i_L and v_c.

$$\begin{cases} \dfrac{\mathrm{d}i_L}{\mathrm{d}t} = -\dfrac{Rr_c + Rr_L + r_c r_L}{L(R + r_c)} i_L - \dfrac{R}{L(R + r_c)} v_c + \dfrac{1}{L} w + \dfrac{Rr_c}{L(R + r_c)} I_{o1} \\ \dfrac{\mathrm{d}v_c}{\mathrm{d}t} = \dfrac{R}{C(R + r_c)} i_L - \dfrac{1}{C(R + r_c)} v_c - \dfrac{R}{C(R + r_c)} I_{o1} \end{cases} \tag{8.26}$$

Considering that $R \gg r_c$, the following state space representation is obtained:

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} -\dfrac{r_c + r_L}{L} & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{CR} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} & \dfrac{r_c}{L} \\ 0 & -\dfrac{1}{C} \end{bmatrix} \begin{bmatrix} w \\ i_{o1} \end{bmatrix} \tag{8.27}$$

where:

$$\begin{cases} \boldsymbol{A} = \begin{bmatrix} -\dfrac{r_c + r_L}{L} & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{CR} \end{bmatrix} \\ \boldsymbol{B} = \begin{bmatrix} \dfrac{1}{L} & \dfrac{r_c}{L} \\ 0 & -\dfrac{1}{C} \end{bmatrix} \end{cases} \tag{8.27a}$$

It should be noted that the introduction of the variable w allows the state-space averaging to be directly determined and the matrices $\boldsymbol{A}$ and $\boldsymbol{B}$ to be obtained with constant coefficients.

A new additional state variable is introduced, i.e., the integral of the error on the output voltage (approximated as the capacitor voltage).

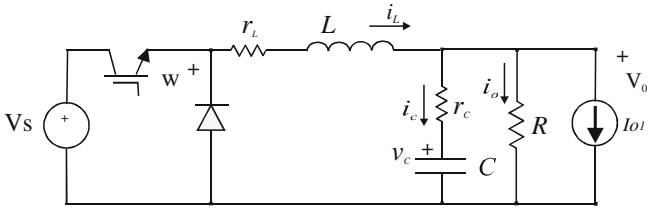


Fig. 8.11 Buck converter with additional current generator as load

$$x_1 = \int (v_C - V_{\text{ref}})\mathrm{d}t \tag{8.28}$$

The other two state variables are the capacitor voltage and one to be chosen between the inductor current and the capacitor current.

It will be demonstrated, hereinafter, that the use of the capacitor current as a state variable is more advantageous.

Assuming that the state variables are the integral of the error on output voltage, the capacitor voltage and the capacitor current, the circuit of Fig. 8.11 is described by the equations:

$$\begin{cases} \dfrac{di_c}{dt} = -\dfrac{1}{RC} i_c - \dfrac{v_c}{L} + \dfrac{w}{L} - \dfrac{dI_{o1}}{dt} \\ \dfrac{dv_c}{dt} = \dfrac{i_c}{C} \\ \dfrac{dx_1}{dt} = v_c - V_{ref} \end{cases} \tag{8.29}$$

The first of Eq. (8.29) is obtained by the first of Eqs. (8.24).

The control variable given in Eq. (8.23) can be expressed as the product of a matrix multiplied for the state vector, as explained in Eq. (8.16):

$$w = -\begin{bmatrix} g_1 & g_2 & g_3 \end{bmatrix} \begin{bmatrix} i_c \\ v_c \\ x_1 \end{bmatrix} = -g_1 i_c - g_2 v_c - g_3 x_1 \tag{8.30}$$

where g_1, g_2, and g_3 are three gains to be determined to impose the position of the closed-loop poles.

By transforming Eqs. (8.29) and (8.30) in the Laplace domain:

$$\begin{cases} W(s) = -g_1 I_c(s) - g_2 V_c(s) - g_3 X_1(s) \\ sI_c(s) = -\frac{1}{RC} I_c(s) - \frac{1}{L} V_c(s) + \frac{1}{L} W(s) - sI_{o1}(s) \\ sCV_c(s) = I_c(s) \\ sX_1(s) = V_c(s) - V_{\text{ref}}(s) \end{cases} \tag{8.31}$$

After some manipulations, and eliminating $W(s)$, $X_1(s)$, and $I_c(s)$ in Eq. (8.31), a third order polynomial in s is obtained:

$$-s^2\frac{I_{o1}(s)}{CV_c(s)}+\frac{g_3}{LC}\frac{V_{ref}(s)}{V_c(s)}=s^3+s^2\left[\frac{1}{RC}+\frac{g_1}{L}\right]+s\left[\frac{1}{LC}+\frac{g_2}{LC}\right]+\frac{g_3}{LC} \tag{8.32}$$

By setting $I_{01}=0$ in Eq. (8.32), the closed-loop transfer function is obtained:

$$\frac{V_c(s)}{V_{ref}(s)}=\frac{g_3}{LC}\frac{1}{s^3+s^2\left[\frac{1}{RC}+\frac{g_1}{L}\right]+s\left[\frac{1}{LC}+\frac{g_2}{LC}\right]+\frac{g_3}{LC}}=\frac{g_3}{LC}\frac{1}{p(s)} \tag{8.33}$$

By setting $V_{ref}=0$ in Eq. (8.32), the output impedance is obtained:

$$Z_o(s)=\frac{V_c(s)}{I_{o1}(s)}=-\frac{s^2}{C}\frac{1}{p(s)} \tag{8.34}$$

where *p(s)* is the characteristic polynomial of the system:

$$p(s)=s^3+s^2\left[\frac{1}{RC}+\frac{g_1}{L}\right]+s\left[\frac{1}{LC}+\frac{g_2}{LC}\right]+\frac{g_3}{LC} \tag{8.35}$$

Finally, it is possible to obtain the relationship between the closed-loop poles of the system and the gains g_1, g_2, and g_3, by equating Eq. (8.35) with the general expression of a three poles polynomial.

$$(s+p_1)(s+p_2)(s+p_3)=s^3+s^2\left[\frac{1}{RC}+\frac{g_1}{L}\right]+s\left[\frac{1}{LC}+\frac{g_2}{LC}\right]+\frac{g_3}{LC} \tag{8.36}$$

The obtained gains are given by:

$$\begin{cases} g_1=L\left(p_1+p_2+p_3-\frac{1}{RC}\right) \\ g_2=LC(p_1p_2+p_3p_2+p_1p_3)-1 \\ g_3=LC(p_1p_2p_3) \end{cases} \tag{8.37}$$

The same calculation can be performed by assuming that the state variables are the integral of the error on output voltage, the capacitor voltage, and the inductor current. In this case, the circuit of Fig. 8.9 is described by the equations:

$$\begin{cases} W(s)=-g_1I_L(s)-g_2V_c(s)-g_3X_1(s) \\ I_L(s)=I_c(s)+\dfrac{V_c(s)}{RC}+I_{o1}(s) \\ sI_c(s)=-\frac{1}{RC}I_c(s)-\frac{1}{L}V_c(s)+\frac{1}{L}W(s)-sI_{o1}(s) \\ sCV_c(s)=I_c(s) \\ sX_1(s)=V_c(s)-V_{ref}(s) \end{cases} \tag{8.38}$$

The open-loop transfer function is:

$$\frac{V_c(s)}{V_{ref}(s)}=\frac{g_3}{LC}\frac{1}{s^3+s^2\left[\frac{1}{RC}+\frac{g_1}{L}\right]+s\left[\frac{1}{LC}+\frac{g_1}{LCR}+\frac{g_2}{LC}\right]+\frac{g_3}{LC}}=\frac{g_3}{LC}\frac{1}{p_1(s)} \tag{8.39}$$

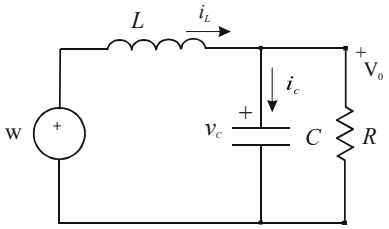


Fig. 8.12 Simplified scheme of buck converter

The output impedance is given by:

$$Z_o(s) = \frac{V_c(s)}{I_{o1}(s)} = -\frac{s(sL + g_1)}{LC}\frac{1}{p_1(s)} \tag{8.40}$$

The relationships between the poles and the gains are:

$$\begin{cases} g_1 = L\left(p_1 + p_2 + p_3 - \frac{1}{RC}\right) \\ g_2 = LC(p_1p_2 + p_3p_2 + p_1p_3) - 1 + \frac{L}{R}\left(\frac{1}{RC} - p_1 - p_2 - p_3\right) \\ g_3 = LC(p_1p_2p_3) \end{cases} \tag{8.41}$$

By comparing Eqs. (8.34) and (8.37) with Eqs. (8.40) and (8.41), respectively, it can be noted that, by choosing the inductor current as state variable, a higher output impedance is obtained and both g_1 and g_2 depend on the load value.

Moreover, since the steady-state mean capacitor current is zero, a smaller volume and cheaper coil sensor, compared with a current sensor placed on the inductance (whose peak-to-peak current is higher and mean value is different from zero) can be used. Finally, the capacitor current can be estimated on the basis of the load voltage using the same sensor required for the measurement of the output voltage. For these considerations the use of the capacitor current as a state variable is preferred.

It should be noted that the possibility to impose the poles allows a fast dynamical response to be obtained. This characteristic avoids interference between the control of the DC/DC converter (used to emulate the PV source) and the load supplied by the source, usually an inverter.

8.4.1 Simulink® Implementation

With reference to the simplified circuit of the buck converter drawn in Fig. 8.12, the state variables can be expressed as in Eq. (8.42).

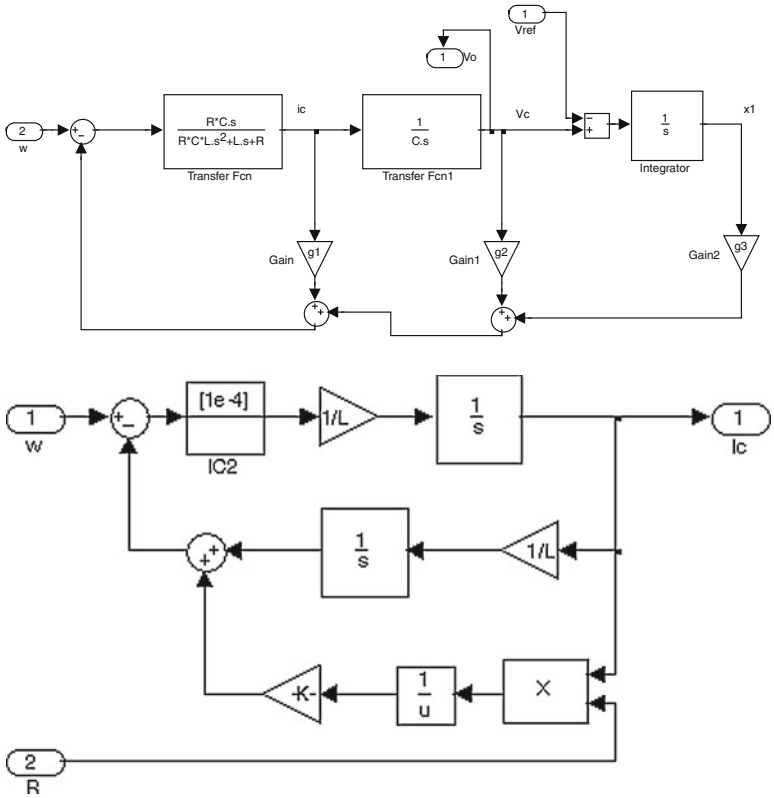


Fig. 8.13 Simulink® implementation of buck converter with pole placement control technique (*top*); Simulink® implementation of the transfer function i_c versus. w allowing load variation (*bottom*)

$$\begin{cases} i_c = \dfrac{sRC}{s^2RLC + sL + R} w \\ v_c = \dfrac{1}{sC} i_c \\ x_1 = \dfrac{1}{s}(v_c - V_{\text{ref}}) \end{cases} \tag{8.42}$$

This formulation can be implemented in Simulink® as shown in Fig. 8.13, top scheme, where the gains are calculated by Eq. (8.37). It should be noted that the use of the block "transfer function" does not allow the parameters to be modified.

The transfer function i_c versus w can be rearranged as in Fig. 8.13, bottom scheme, to simulate load variations.

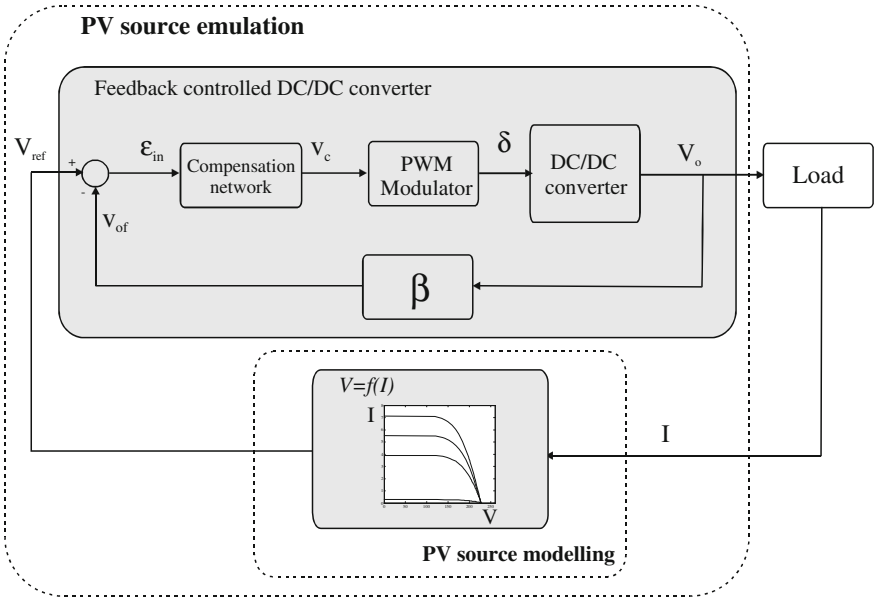


Fig. 8.14 General block diagram of a PV source emulator

8.5 DC/DC Converter-Based Emulation of a PV Source

The block diagram shown in Fig. 8.14 summarizes the concept of a PV source emulation, where the feedback structure of a DC/DC converter and the $V = f(I)$ block are highlighted.

The feedback controlled DC/DC converter is that described in the previous section. It realizes an output equal to that delivered by the I–V relationship. Its output voltage is applied to the electrical load and the obtained current is used as an input for the $V = f(I)$ block.

Figure 8.14 synthesises the content of the two parts of this book as well.

In particular, the block indicated as "PV source modelling" is the result of the I–V characteristic representation, obtained with one of the techniques described in part I.

On the other hand, the block indicated as "Feedback controlled DC/DC converter" is the controlled PV emulator's power stage, whose selection and design derives from the concepts explained in part II.

With specific reference to the DC/DC converter, the issues related to its design constraints and the appropriate selection of its best topology and control, are given in the following.

8.5.1 DC/DC Power Converter Design Constraints

8.5.1.1 Current and Voltage Output

The maximum output current and voltage deliverable by the PV emulator have to be defined on the basis of the operating conditions of the considered PV generator.

It should be observed that the maximum output current is the short circuit current at the highest solar irradiance, while the maximum output voltage is the maximum open circuit voltage.

Once these design constraints are fixed, the maximum allowable load variation must range from the infinity impedance (open circuit condition) to an impedance as much as low to permit approaching the above described short circuit condition.

It is worth noting that the mere short circuit condition, corresponding to a null load is not compatible with the converter operation as deduced by the transfer functions given in Sect. 7.13.

Finally, the electrical load must be able to correctly dissipate the power delivered by the PV emulator.

8.5.1.2 Dynamic Response and Arbitrary Load Problem

Two different issues have to be handled when the PV emulator is required to correctly reproduce the dynamic behavior of a PV generator. The former is related to the need of following the response to rapidly changing environmental conditions or applied load. The latter is known as the arbitrary load problem and it is tied to the use of the PV emulator in a power conversion chain where it is connected to a power converter, intended as an electrical load.

With reference to the first issue, the response of the PV emulator should exhibit a time constant faster than the dynamic response of the model. This is achieved by suitably setting the emulator bandwidth and by setting a switching frequency much higher than the cut-off frequency of the emulator bandwidth.

It should be noted that these constraints are not cumbersome for reproducing varying environmental conditions, since the corresponding time constants are generally high. Anyway, rapid load variations in a stand alone configuration, represent a more critical situation due to the related smaller time constants in terms of voltage response of the PV emulator. For this reason, the assessment tests on the PV emulator model, carried out in part I, are performed using load step variations.

If the minimum rise time of the output voltage is equal to τ_r, the power amplifier bandwidth must be set greater than $1/(\pi\ \tau_r)$.

With reference to the arbitrary load problem, it should be considered that the primary benefit of the PV emulators consists on their use in testing the performance of PV inverters and MPPT algorithms. Therefore, they should be as flexible as possible to properly operate independently from the loading converter.

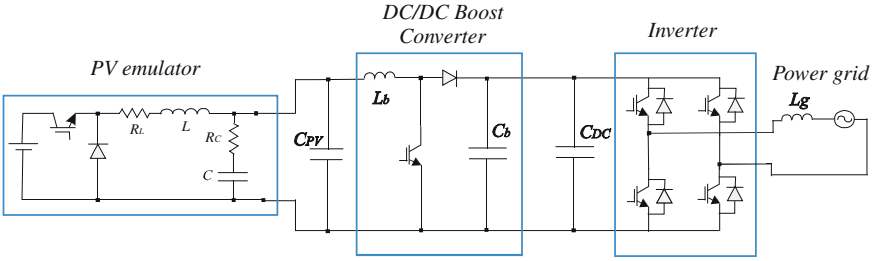


Fig. 8.15 Conversion chain for the grid connection of a PV source emulator

In detail, the loading converter can exhibit different values of the capacitance seen at the emulator terminals and requires a high frequency current (whose fundamental harmonic is equal to the switching frequency).

These parameters are not a priori known.

The output impedance of the PV emulator gives information on the range of frequencies in which it behaves like an ideal voltage source.

A low impedance value is desirable in order to correctly reproduce the current demand coming from the loading converter.

As an example, Fig. 8.15 shows a possible application of a PV emulator, used to test a complete conversion chain for the grid connection of a PV source. Here, the PV emulator replaces a real PV generator, permitting to accurately investigate the whole PV system behavior, including the influence of weather conditions, partial shading and dynamics, without the use of a real outdoor installation, thus reducing the time and the cost of the experiments.

The DC/DC boost converter performs the boosting of the voltage coming from PV source and it can be integrated with the MPPT.

Finally, the single-phase grid-connected inverter, controlled as an active rectifier, is able to maintain the DC link voltage and to properly manage the active and reactive power supplied to the grid.

8.5.2 Selection of the Best Topology

On the basis of the analysis developed in Chap. 7, the considered DC/DC converter topologies, i.e., the buck converter, the boost converter, and the buck-boost converter, are all, in principle, possible candidates to be used for the power amplifier stage of a PV emulator.

Anyway, the following practical considerations suggest the employment, when possible, of the buck topology.

- The DC voltage level for supplying the PV emulator can be easily obtained by the grid voltage through a simple bridge rectifier both in the case of single-phase grid and three-phase grid. In this last case, the obtained DC voltage of about

Table 8.1 Main features under standard test conditions (*stc*) of the PV plant for the emulator design

Parameter	Symbol	Value
Number of assemblies	N_P	2
Number of modules per assembly	N_S	6
Peak power	P_{PV}	1450 W
Open circuit voltage	V_{oc}	228.6 V
Short-circuit current	I_{sc}	9.2 A
Maximum power voltage	V_{MP}	186 V
Maximum power current	I_{MP}	8 A

500 V is suitable to be reduced, via the buck converter, to the rated voltage of a common PV plant of a power up to tens of kW.

- The use of a buck topology permits a simpler control implementation, because the corresponding transfer functions are not dependent on the operating point, for a given electrical load, as illustrated in Table 7.2.

With reference to the first aspect, it is worth observing that the boost converter does not permit to obtain an output voltage less than the supply voltage; this means that operating conditions close to the short circuit are not reproducible.

Furthermore, high output voltages imply high input currents. This last disadvantage is also present in the buck-boost scheme, which, however, allows low voltages to be reproduced.

Regarding to the second aspect, it should be noted that both the boost and the buck-boost converters, show a nonlinear dependence on the duty cycle and the load value as well, thus making difficult a fixed parameter control strategy.

8.6 Example of a PV Source Emulator Design

This section is dedicated to the design and practical setup of a PV emulator, devised by the authors, which is used to reproduce, in a laboratory frame, the electrical behavior of a real PV plant, previously modeled according to a single diode four parameter scheme. The PV generator's I–V relationship is expressed by Eqs. (3.13) and (3.14).

The considered PV plant has been described in detail in Sect. 4.4.2.3, where the parameter identification for the corresponding model has been performed, as well. In particular, the adopted PV model uses a regression law to relate temperature and solar irradiance, as explained in Sect. 4.6

Here, the PV plant specific features are summarized in Table 8.1, for the sake of convenience.

Figure 8.16 shows the PV plant configuration.

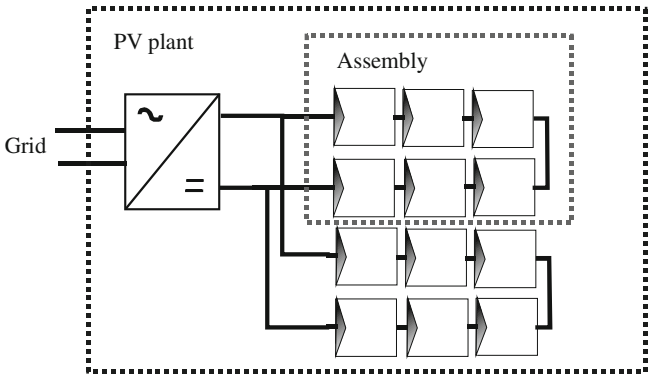


Fig. 8.16 PV plant configuration

8.6.1 Power Stage Design

A switching DC/DC buck converter topology is chosen. The DC/DC converter is operated at a constant switching frequency and input DC voltage, while the regulation of the output voltage is obtained by varying the converter duty cycle (D).

The scheme of the DC/DC buck converter circuit is that illustrated in Fig. 7.13. In such a scheme, the resistive components r_L and r_C represent the parasitic resistance of the output filter inductor and capacitor, respectively.

The design of the converter output LC filter is carried out on the basis of the following conditions:

- continuous-current conduction operation of the converter;
- ripple on the output voltage not exceeding few percent.

The above-mentioned conditions can be obtained from Eqs. (7.23) and (7.19), respectively. Rearranging these equations, the inductance and the capacitance values are calculated on the basis of the design constraints, according to:

$$L \geq \frac{V_s T_s}{2 I_{\mathrm{Lt}}} D(1 - D) \tag{8.43}$$

$$C \geq \frac{T_s^2}{8L} \frac{V_o}{\Delta V_o} (1 - D) \tag{8.44}$$

where I_{Lt} is the limit current between continuous and discontinuous conduction mode, T_s is the switching period, and V_o is the output voltage of the DC/DC converter.

The rated power of the prototype is about 3 kW.

The switching frequency of the DC/DC buck converter, is chosen equal to 10 kHz.

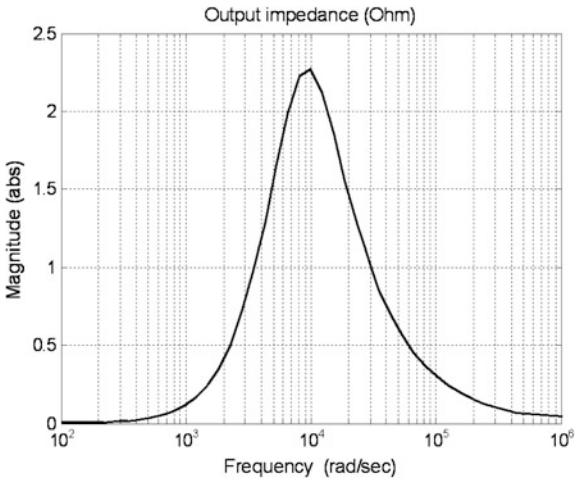


Fig. 8.17 DC/DC converter output impedance versus frequency [From Di Piazza and Vitale (2010)]. Used with kind permission from Elsevier

The maximum voltage output of the PV emulator is fixed to 235 V, in consideration of the electrical features of the PV source. Therefore, an input voltage $V_s = 350$ V is chosen.

According to Eqs. (8.43) and (8.44), the following values of capacitance and inductance of the low pass output filter are adopted, respectively:

- $C = 33$ μF;
- $L = 3.7$ mH.

This last value gives $I_{Lt} = 1.18$ A for $T_s = 10^{-4}$ s.

8.6.2 Pole Placement Voltage Controller

As previously highlighted, a good dynamic behavior is required in order to take into account the loading effect of the power converter supplied by the PV emulator.

The possibility to impose the closed-loop poles, by using the pole placement technique, described in Sect. 8.4, permits to obtain a fast dynamical response.

The output impedance of the DC/DC converter gives information on the range of frequencies in which the PV emulator behaves like an ideal voltage source.

As previously said, a low impedance value is desirable in order to correctly reproduce the current demand coming from the loading converter.

The closed-loop poles are chosen as a pair of complex and conjugate and a real one. The corresponding k_i coefficients are chosen equal to $k_{1,2} = 2\pi(500 \pm j500)$ and $k_3 = 2\pi500$. This choice assures a dynamical response with a rise time in the order of milliseconds.

The equivalent output capacitance corresponds to about 10 μF that is smaller than a typical expected load capacitance.

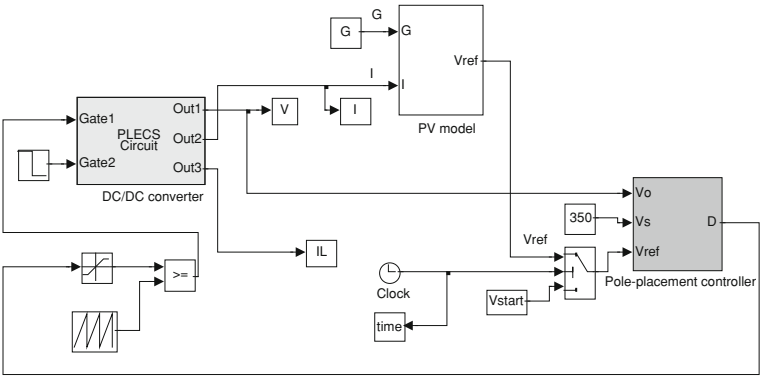


Fig. 8.18 Implemented model of the PV emulator

The obtained output impedance versus frequency curve, calculated by Eqs. (8.34) and (8.35), is shown in Fig. 8.17. It is possible to observe that it exhibits a maximum equal to 2.25 Ω at 1.6 kHz (10^4 rad/s).

8.7 PLECS-Based Simulation of PV Source Emulator

In order to evaluate the performance of the PV emulator, developed according to the previously described design constraints, a simulation analysis is carried out. It exploits the association of Matlab/Simulink® environment and PLECS® (Piece-wise Linear Electrical Circuit Simulation for Simulink) toolbox.

As specified in Chap. 5, PLECS® allows an actual plant, for example a power electronic circuit, to be implemented, as subsystem, while the related control is developed using standard Simulink® blocks. Its main advantage is the very short simulation time.

As for the considered application, the DC/DC buck converter has been built using PLECS® libraries, while the control algorithm has been implemented in Simulink® and directly interfaced to the circuit-based simulation model.

Figure 8.18 shows the whole implemented model, including the PV model, the DC/DC converter, and the pole placement controller.

It can be noted that, at the beginning of simulation, a constant value of reference voltage is given to the controller in an open loop mode to avoid handling high voltage error signals. This constant voltage is indicated as V_{start}; after a short transient of 0.02 s the closed-loop operation is enabled.

The PV model implementation is done using the form $V = f(I)$, to obtain the voltage reference for the DC/DC converter.

In order to correctly reproduce partial shading conditions, the whole PV model is represented as the composition of the single module models. In particular, each module is considered with its own temperature and solar irradiance.

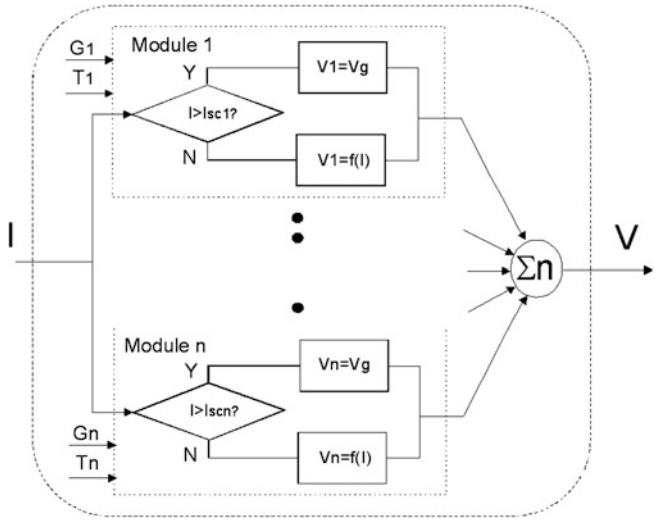


Fig. 8.19 Implemented algorithm for obtaining the I–V characteristics of a PV assembly. (From Di Piazza and Vitale (2010)). Used with kind permission from Elsevier

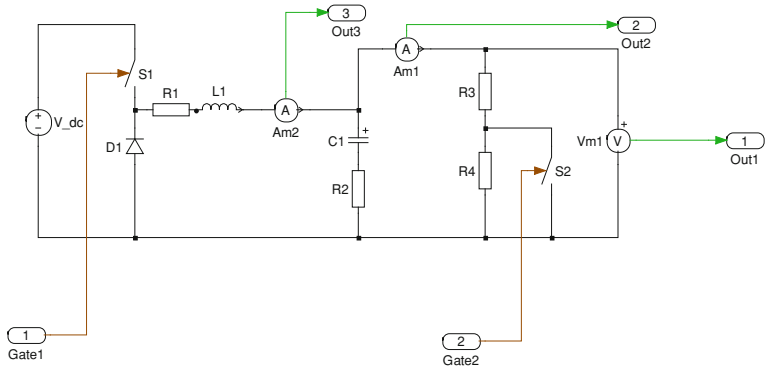


Fig. 8.20 Circuit scheme of the DC/DC converter implemented in PLECS®

In this way, the PV plant behavior is implemented by summing the voltages of each module and the currents of parallel connected assemblies. Moreover, with reference to a single assembly, as shown in Fig. 8.16, if the current is greater than the short-circuit current of a module, the module output voltage is set to the threshold voltage of the bypass diode (V_g), otherwise the voltage is obtained by the model. This approach allows the PV assembly to be accurately analyzed under partial shading conditions.

The above described rules are summed up on the flow chart drawn in Fig. 8.19.

Figure 8.20 illustrates the PLECS® model of the DC/DC buck converter; it encompasses the output filter and its parasitic parameters. In particular, the load is

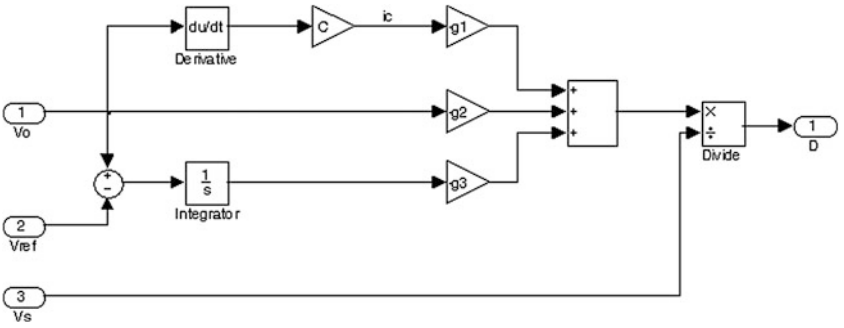
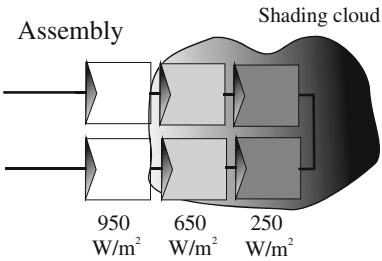


Fig. 8.21 Detail of the pole placement controller block

Fig. 8.22 Representation of the assembly under partial shading condition



realized by two series connected resistors where a switch, parallel connected to one of them, is used to impose a sudden variation of the load.

The PLECS® model has two inputs and three outputs. The inputs are the switching command for the IGBT, modeled as an ideal switch, and the command for the switch used to obtain the load step transition. The outputs give the inductor current, used to assess the continuous conduction mode, the output voltage, and the output current of the PV emulator.

The scheme shown in Fig. 8.18 is conceived for testing the PV emulator behavior with step load transitions and constant solar irradiance.

Other testing conditions are obviously possible, for example, step transitions of irradiance or load/irradiance variations according to a chosen profile.

The pole placement controller block is shown in detail in Fig. 8.21.

It should be observed that the values of the three gains g_1, g_2, and g_3 are calculated according to Eq. (8.37). This calculation is done by a MATLAB® script, run before operating the PV emulator for tests.

As an example, the static I–V characteristics of a PV assembly are determined both under uniform solar irradiance of 950 W/m^2 and under the partial shading condition represented in Fig. 8.22. This condition is given by two modules with an irradiance of 950 W/m^2, two modules with an irradiance of 650 W/m^2, and the last two with an irradiance of 250 W/m^2. The obtained I–V curves are shown in Fig. 8.23.

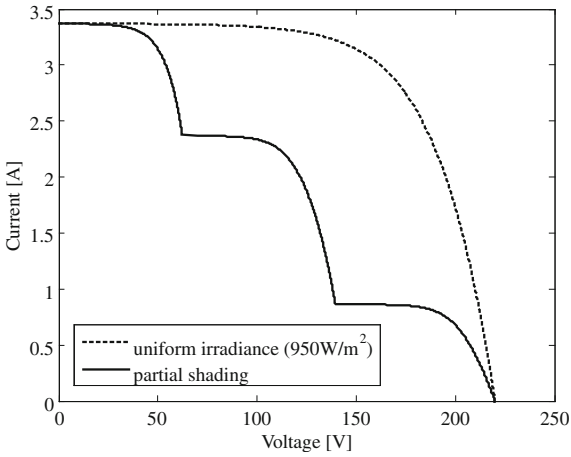


Fig. 8.23 I–V characteristics with uniform irradiance and under partial shading condition, reproduced by the PV model

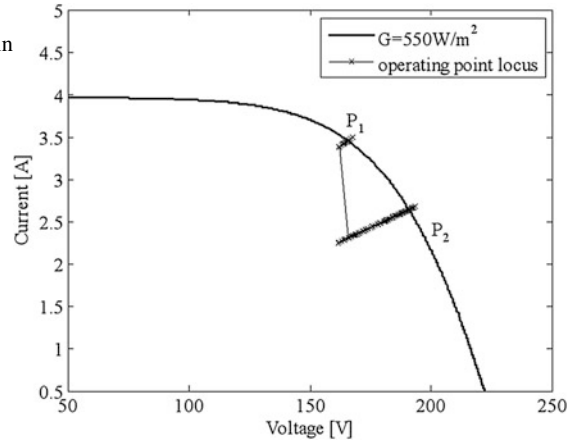


Fig. 8.24 Operating point locus in Test #1

The following tests are carried out:

- Test #1: step load transition with constant solar irradiance;
- Test #2: irradiance step transition with constant load resistance.

In Test #1 solar irradiance is set equal to 550 W/m^2, while the load is switched between an initial value of 50 Ω, nearly corresponding to the MPP, to a final value of 75 Ω. Due to this transition, the operating point goes from P_1 to P_2 on the I–V curve corresponding to $G = 550$ W/m^2, as illustrated in Fig. 8.24. Here, it can be noted that the sudden variation of the load resistance produces an initial quasi-vertical trajectory in which the operating point jumps from the straight line corresponding to the load resistance of 50 Ω to the straight line corresponding to the final resistance load of 75 Ω. Then it continues toward the final point remaining on the same line. The slight deviations from points P_1 and P_2 exhibited in the operating point locus are due to the switching operation of the emulator.

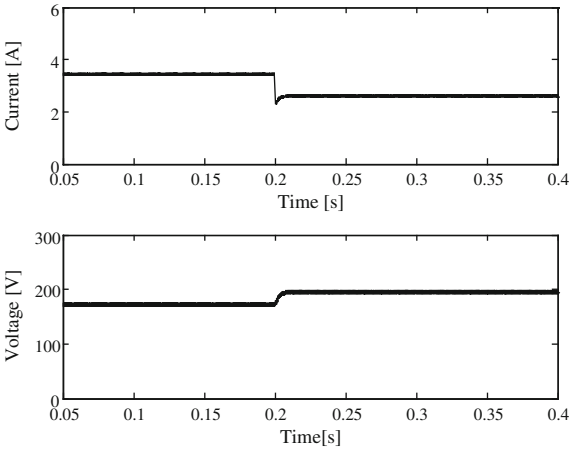


Fig. 8.25 Current and voltage transition, corresponding to Test #1, versus time

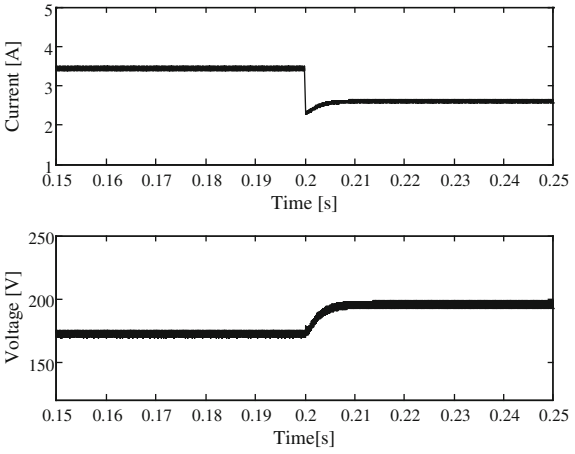


Fig. 8.26 Zoom of the current and voltage transitions, corresponding to Test #1, versus time

Figure 8.25 shows the voltage and current transitions, corresponding to Test #1, versus time. A zoom of these transitions is drawn in Fig. 8.26, where it can be noted the sudden current variation due to the step load variation and the current and voltage response whose dynamics is dominated by the choice of the emulator poles. As indicated in Sect. 8.6.2, these poles are fixed to $p_{1,2} = -2\pi(500 \pm j500)$ and $p_3 = -2\pi500$, on the basis of the PV plant to be emulated.

As previously explained, the suitable selection of the emulator poles, thanks to the pole placement technique, allows the desired dynamic behavior to be reproduced.

In order to put in evidence the effect of the poles position on the emulator dynamics, Test #1 is repeated with three different settings in which the real pole assumes the following values:

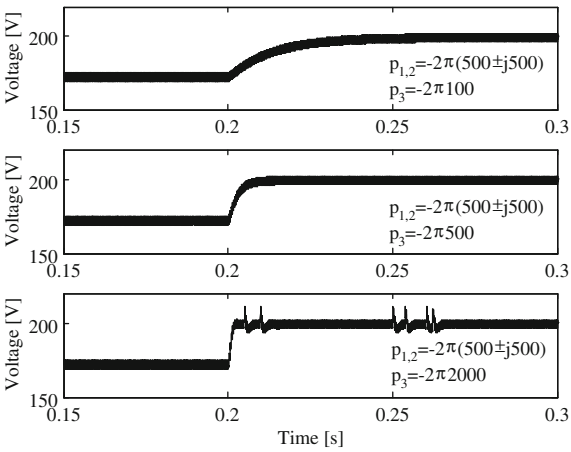


Fig. 8.27 Voltage transitions, with different poles configurations (Test #1)

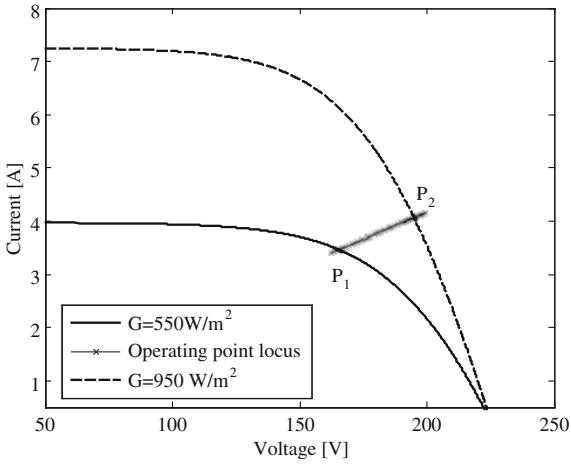


Fig. 8.28 Operating point locus in Test #2

- $p_3 = -2\pi 100$ rad/s
- $p_3 = -2\pi 500$ rad/s
- $p_3 = -2\pi 2000$ rad/s

while the complex conjugate pair of poles remains unchanged.

The voltage transition has been observed in all cases, whose corresponding time domain waveforms are given in Fig. 8.27.

It is possible to observe that the first choice implies an over-damped response with a slower dynamics.

The second choice leads to an over-damped behavior and a faster dynamics.

Finally, with the third choice, additional oscillations appear.

In Test #2 the load resistance is kept constant and equal to 50 Ω, while a step variation of the solar irradiance from 550 to 950 W/m^2 is imposed.

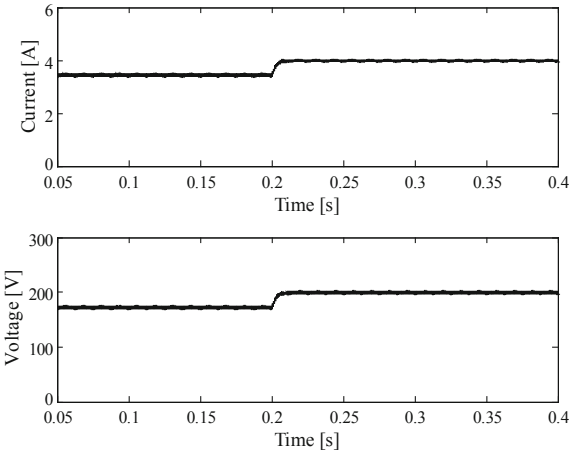


Fig. 8.29 Current and voltage transition, corresponding to Test #2, versus time

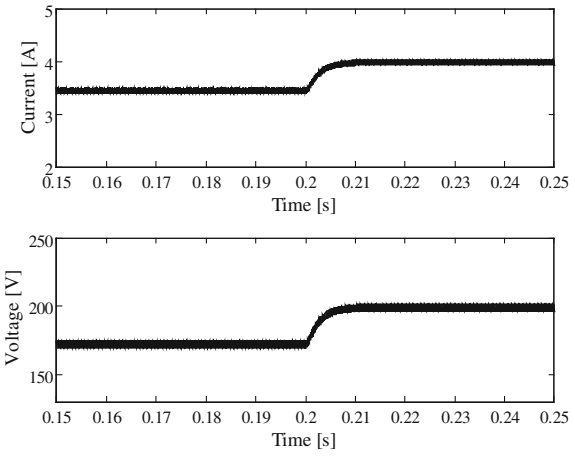


Fig. 8.30 Zoom of the current and voltage transitions, corresponding to Test #2, versus time

In this case, the trajectory of the operating point goes from the I–V curve corresponding to 550 W/m^2 to the I–V curve corresponding to 950 W/m^2, remaining on the straight line imposed by the load resistance.

This trajectory is shown in Fig. 8.28, where the slight deviations from points P_1 and P_2 exhibited in the operating point locus are due to the switching operation of the emulator.

The voltage and current transitions in Test #2, versus time, are plotted in Fig. 8.29.

A zoom of these transitions is drawn in Fig. 8.30, where, differently from Test #1, it can be noted both the current and voltage variations follow practically the same variation trend with a rise time of about 10 ms.

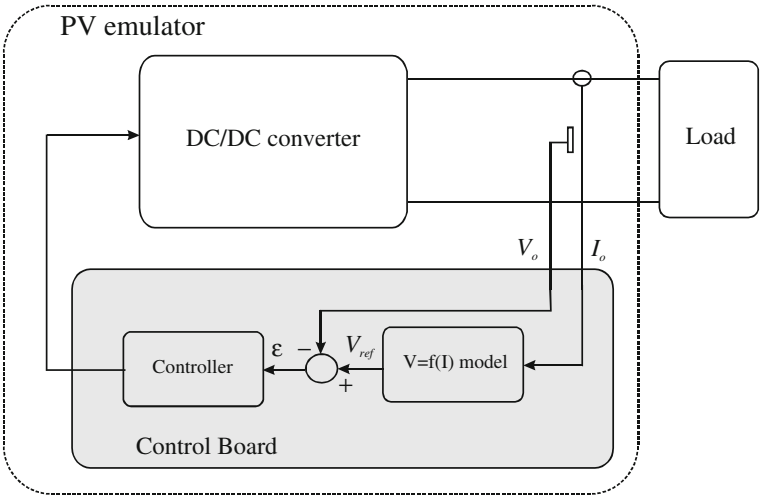


Fig. 8.31 Principle block diagram of the PV emulator

8.8 Experimental Implementation of the PV Source Emulator

The principle block diagram of the PV emulator is represented in Fig. 8.31.

It encompasses the DC/DC buck converter and a control board, whose inputs are the converter output voltage and current and whose output is the control signal of the buck converter.

The control board implements both the PV model and the control algorithm.

On the basis of the output current, the PV model calculates the reference voltage which is compared with the actual output voltage of the DC/DC converter.

The error signal is processed by the controller that outputs the command for the switching device.

In the following subsections, the experimental set-up of the whole PV emulator equipment is described in detail.

8.8.1 DC/DC Buck Converter

The DC/DC buck converter is supplied by the TDK-Lambda GEN600-5.5 DC power supply because, with this solution, the maximum deliverable current can be electronically limited and the PV emulator is galvanically isolated from the power grid.

As an alternative, an isolation transformer and a bridge rectifier can be used to obtain the supply voltage for the PV emulator.

The DC/DC converter employs the SKM50GB123D power IGBT whose rated current is equal to 40 A at 80° C. This high current value allows to manage powers up to 10 kW.

Fig. 8.32 REO load 302 three-phase resistive load bank

The used driver circuit is the hybrid dual MOSFET driver SKHI22AR.

A snubber circuit is realized by using a 0.22 μF polypropylene capacitor, i.e., the MKPC4BS, suitable for high-frequency applications.

As previously indicated, the output filter of the buck converter is composed of a 3.7 mH inductor and a 33 μF capacitor. The corresponding parasitic components, experimentally evaluated, are, respectively, $r_L = 0.4\ \Omega$ and $r_c = 2.06\ \Omega$.

The output voltage is sensed by a LEM LV25-P transducer, while the output current is measured by a closed-loop current sensor, i.e., the Honeywell CSNP661. Both these sensors exhibit a wide bandwidth and their range can be varied by a suitable setting of an external precision resistor.

As for the current transducer, its maximum range is equal to 50 A, coherently with the chosen IGBT. For the emulation of the considered plant this value has been lowered to 10 A by winding five turns around the sensor core.

Finally, the resistive load is realized by a REO load 302 three-phase resistive load bank.

A view of the resistive load is given in Fig. 8.32.

8.8.2 Control Board

The PV emulator control is experimentally implemented using the DSP-2 board developed at the Institute of Robotica of Faculty of Electrical Engineering and Computer Science in Maribor, Slovenia.

The DSP-2 board is a high performance, floating-point digital signal processor-based inverter controller. This board, in combination with DSP-2 library, can be successfully used for several industrial applications.

In general, the DSP-2 board allows control algorithms, set up in Matlab/Simulink® environment, to be implemented and verified in suitable development systems, at a significantly low cost.

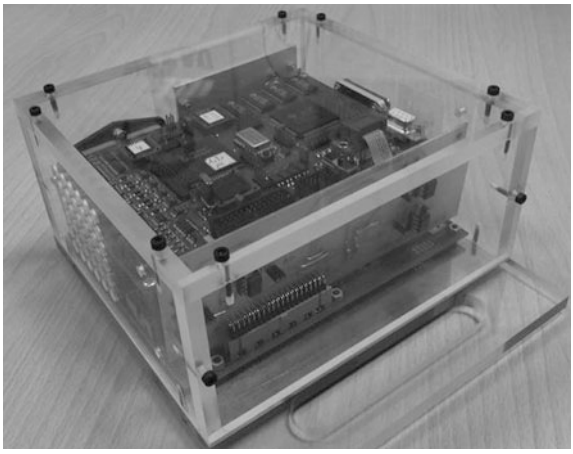


Fig. 8.33 Picture of the DSP-2 board

The board is based on the Texas Instruments TMS320C32 DSP and the FPGA XCS40-4PQ240C, member of Xilinx Spartan family. It is equipped with 4 × 12 bit simultaneous A/D converters with serial output and a two channels 12 bit D/A converter with serial input and unipolar output from 0 to 4 V.

DSP-2 library for Simulink® enables rapid transition from the simulation in Simulink® to the real time operation on the DSP-2 board.

DSP-2 library in combination with DSP-2 Terminal interface enables online changing of the Simulink® block parameters, by the parameter inspector window, while the code is executed.

In Fig. 8.33 a picture of the DSP-2 board is shown.

In general, for the implementation of the PV emulator control, it is necessary to use four inputs, i.e., current, voltage, solar irradiance, and temperature. In particular, current and voltage are those sampled at the emulator output, while solar irradiance and temperature are set by the operator or given by external sensors. In the specific case, since a PV model using a regression law to relate temperature and solar irradiance is adopted, only the solar irradiance values are given as input via software to the control board, according to the test to be performed.

The output of the board is the duty cycle generated by PWM block, taken from the DSP-2 library. When the output of the PWM is set to "1", the power device is active.

In Fig. 8.34 the block diagram of the emulator control, including the PV model, the pole placement-based controller and the PWM modulator, is sketched.

The current and voltage are acquired by two analog inputs indicated as DSP-2 AI.

The solar irradiance G is set by software either if constant or if following a given profile.

The block indicated as DSP-2 PWM is a three-phase pulse width modulator suitably handled to give the switching command for the IGBT (only one input is used). Finally, the blocks indicated as DSP-2 TT allow the corresponding variables to be displayed in the DSP-2 Terminal interface.

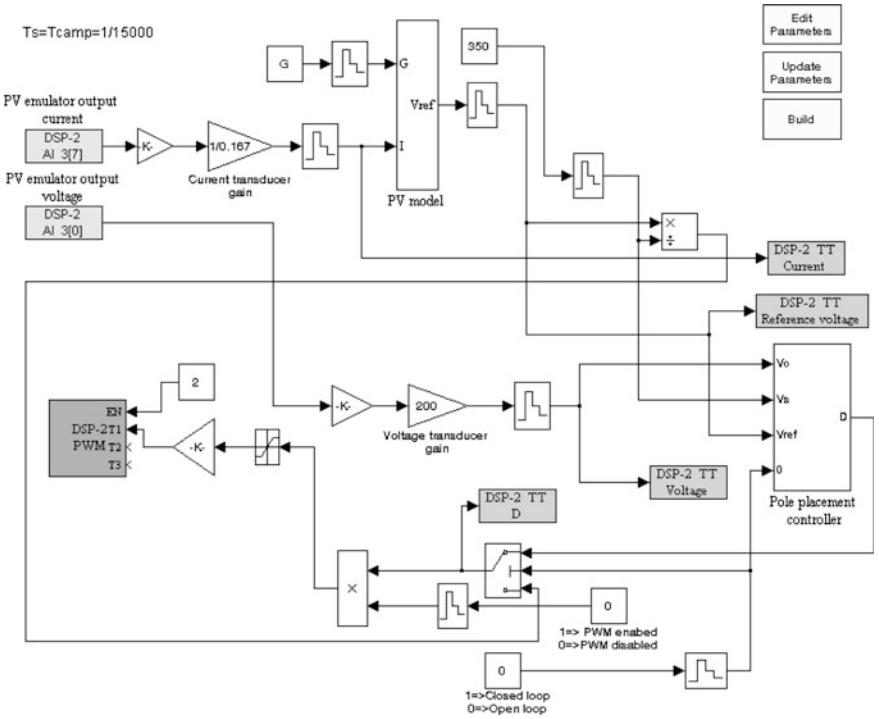


Fig. 8.34 Block diagram of the PV emulator control

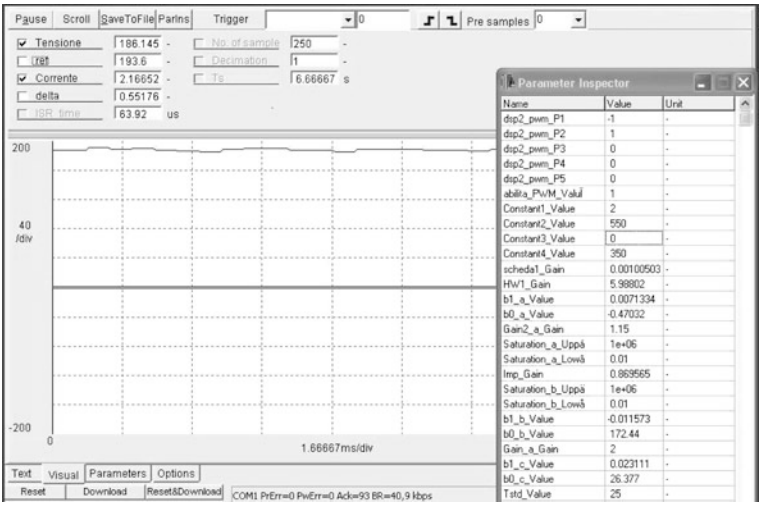


Fig. 8.35 DSP-2 Terminal interface

In Fig. 8.35 Terminal interface, with superimposed the parameter inspector window is shown, as an example.

8.8.3 DC/DC Boost Converter for the MPPT

The optimal exploitation of a PV source is obtained by maximizing the delivered power. This means that the optimal resistance load must be set to V_{MP}/I_{MP}. Since the MPP is variable with environmental parameters, the load value should be continuously changed to follow this optimal operating condition.

A possible way to realize a variable load is to use a further power converter connected to the output of the PV source.

If a DC/DC boost converter is used for this purpose, on the basis of (7.46) and (7.47), its input resistance is given by:

$$R_i = \frac{V_s}{I_s} = \frac{V_o}{I_o}(1-D)^2 = R(1-D)^2 \tag{8.45}$$

It can be noted that the boost input impedance can be regarded as a variable load resistance controlled by the duty cycle D for the PV source. In this case, the task of the MPPT algorithm is to properly impose the value of the duty cycle, at any one instant.

In our case, a boost converter has been devised to test the PV emulator behavior with an electronic load, which corresponds to most of the actual practical configuration of PV plants.

Once the PV emulator behavior is assessed, the whole system composed of the PV emulator and the boost converter is useful to test MPPT algorithm performance. In addition, if an inverter is included in the conversion chain, as illustrated in the example of Fig. 8.15, the inverter control algorithm can be tested, as well.

It is important to observe that, compared to a purely resistive load, an electronic load requires a high frequency current, in addition to the DC component, due to the switching operation. Hence, the high-frequency output impedance of the PV emulator should match the one of the real PV plant to achieve a realistic profile of delivered current and voltage.

The design of the boost converter is carried out imposing the conditions of continuous-current conduction operation and ripple on the output voltage lower than few percent.

The following values for the inductance and capacitance are fixed to: $L_b = 2$ mH and $C_b = 23.5$ μF.

In the case of a grid connection, by an active rectifier, the DC link voltage is mantained at a constant value, then it is possible to control the input voltage of the boost converter, and consequently the output voltage of the PV emulator, so to track the MPP.

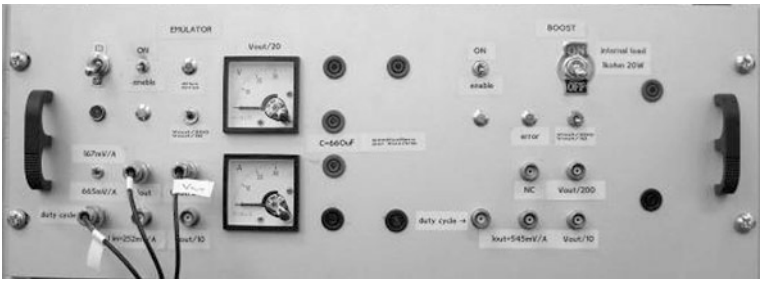


Fig. 8.36 Front panel of the PV emulator

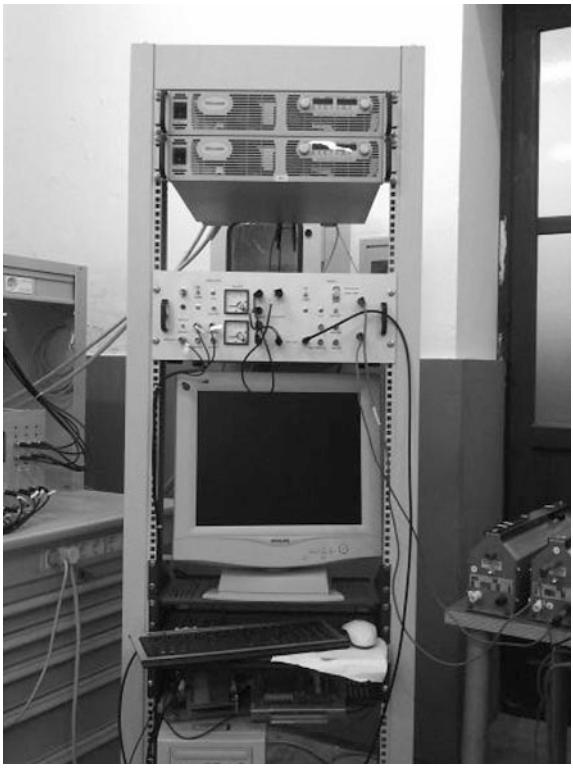


Fig. 8.37 Rack containing the PV emulator

The power switch is a SKM50GB123D power IGBT, switched at 10 kHz, as well as the sampling frequency of the control system.

A decoupling capacitance $C_{PV} = 650$ μF is placed between the PV emulator and the boost converter in order to prevent oscillations toward the emulated PV source.

The boost circuit is allocated in the same case containing the power stage of the PV emulator. As shown in Fig. 8.36, the boost signal and power connectors are positioned in the right part of the front panel of the whole equipment.

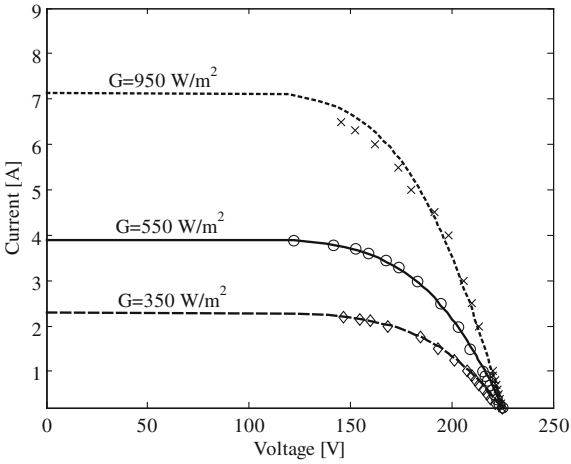


Fig. 8.38 Theoretical I–V curves with superimposed experimental points obtained by the PV emulator

8.9 Experimental Results

Figure 8.37 shows a picture of the experimental rack containing the PV emulator. At the top of the rack the DC power supply can be observed.

The operation of the PV emulator has been tested by laboratory measurements. The used measurement system is composed by:

- a digital oscilloscope with a bandwidth of 1 GHz and a maximum sampling frequency of 2.5 GHz, 20 GS/s, i.e., the TEKTRONIX TDS7254B;
- a 100 MHz high voltage differential probe, i.e., the TEKTRONIX P5205;
- a current measurement system, including an amplifier, i.e. the Tektronix TCPA 300;
- a current probe, i.e., the Tektronix A6303.

First, the static I–V characteristics of the PV plant (described in Table 8.1 and Fig. 8.16) are determined under different uniform solar irradiance values. In particular, the irradiance levels of 350, 550, and 950 W/m^2 are considered. The static experimental points on the I–V characteristics are obtained by imposing a constant solar irradiance value on the DSP board and by suitable values of the resistive load.

In Fig. 8.38 the I–V characteristics of the PV generator, deduced by the model with superimposed experimental points, obtained by the PV emulator, are shown. It is possible to observe that the PV emulator reproduces appropriately the theoretical operation of the PV generator. A slight deviation of the experimental points from the I–V curve is observed at higher irradiance.

Another test has been performed to show the ability of the PV emulator to reproduce the theoretical behavior of the PV generator even under partial shading conditions. In particular, the assembly drawn in Fig. 8.39 has been emulated, according to the method explained in Sect. 8.7.

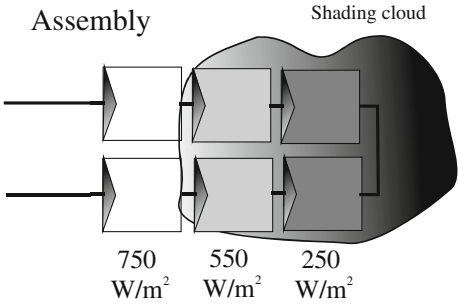


Fig. 8.39 Representation of the assembly under partial shading condition, reproduced by the PV simulator

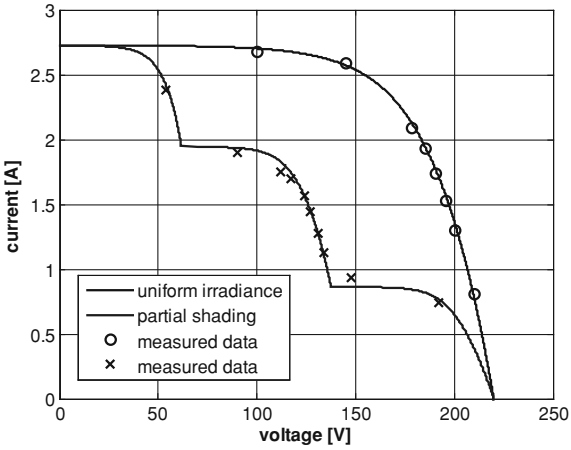


Fig. 8.40 I–V characteristics with uniform irradiance and under partial shading condition with experimental points superimposed [From Di Piazza and Vitale (2010)]. Used with kind permission from Elsevier

Figure 8.40 illustrates the I–V curves obtained by the model with the static experimental points superimposed. A good matching can be noted.

The transition between the two points belonging to the same I–V curve has been realized using the PV emulator. In particular, Test #1 described in Sect. 8.7 has been performed. In this test, solar irradiance is set equal to 550 W/m^2, while the load is switched between an initial value of 50 Ω, nearly corresponding to the MPP, to a final value of 75 Ω. This load step variation is obtained by an abrupt commutation of the resistance load value using the resistive load bank.

The corresponding experimental current and voltage time domain waveforms are shown in Fig. 8.41. The obtained experimental results are in good agreement with those obtained by simulation with PLECS®. This is evident comparing Fig. 8.41 with Fig. 8.26. It should be noted that, to put in evidence the voltage variation, a scale of 20 V/div has been used in the oscilloscope and a DC offset has been set; for this reason, the reference level is not visible.

The transition between the two points belonging to different I–V curves has been realized using the PV emulator. In particular, Test #2 described in Sect. 8.7 has been performed. In this test, the load resistance is kept constant and equal to

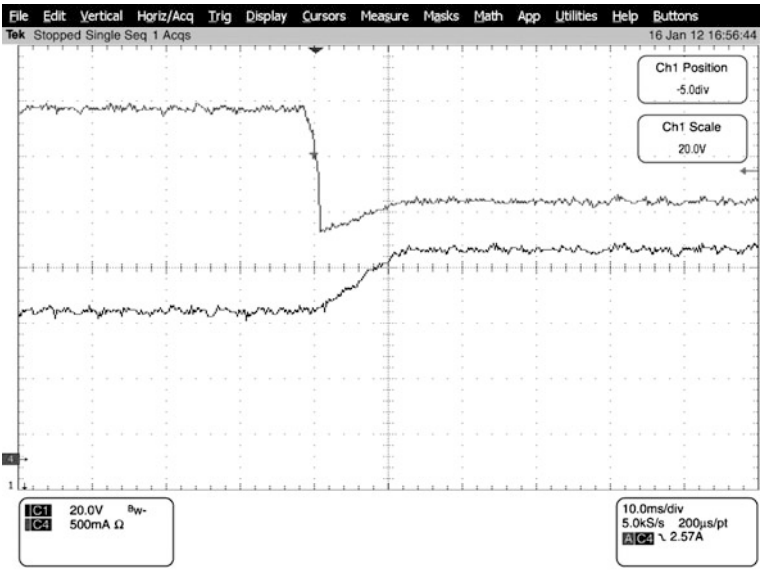


Fig. 8.41 Current (top trace) and voltage (bottom trace) transition, corresponding to Test #1 obtained by the PV emulator

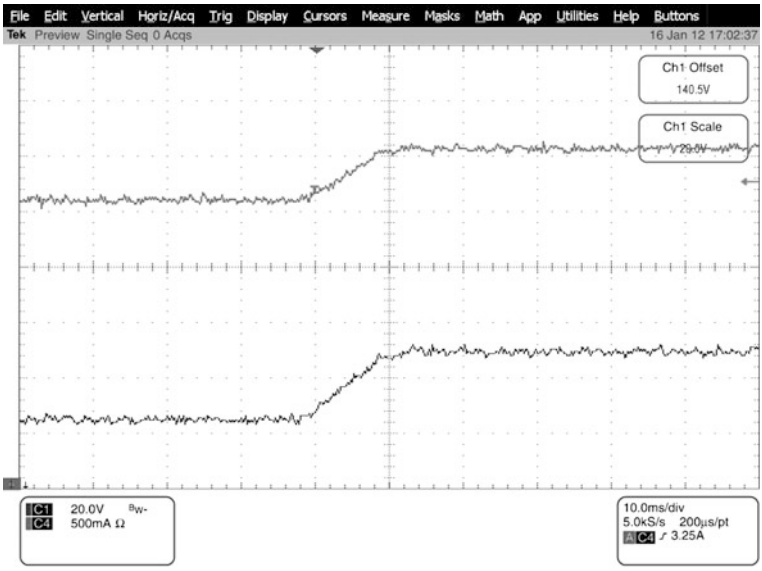


Fig. 8.42 Current (top trace) and voltage (bottom trace) transition, corresponding to Test #2 obtained by the PV emulator

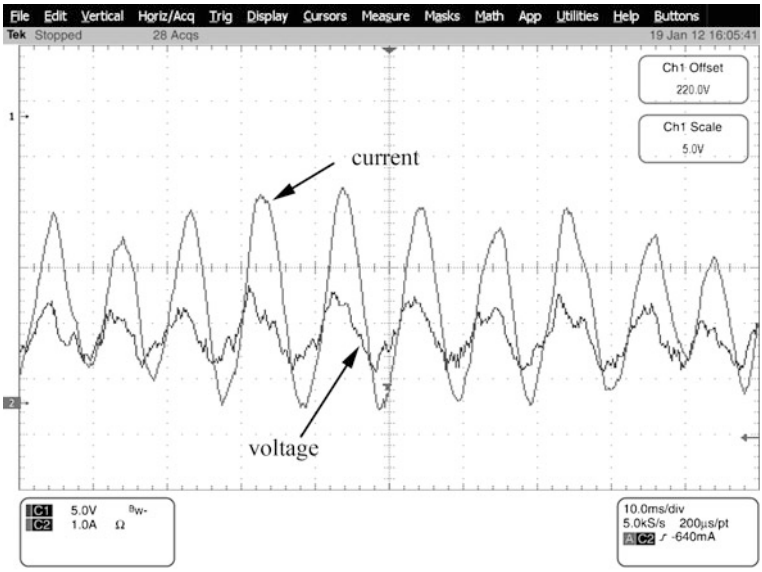


Fig. 8.43 Current and voltage AC components supplied by the PV emulator in grid-connected configuration

50 Ω, while a step variation of the solar irradiance from 550 to 950 W/m^2 is imposed via software by the DSP-2 Terminal interface.

The corresponding experimental current and voltage time domain waveforms are shown in Fig. 8.42. Even in this case, the obtained experimental results are in good agreement with those obtained by simulation with PLECS®. This is confirmed by the comparison of Fig. 8.42 with Fig. 8.30, where the same rise time is noticeable.

A further assessment on the PV emulator operation is done to demonstrate that it is able to reproduce the typical fluctuations due to the power injected into the grid by a single-phase inverter. Such a power is expressed as:

$$p(t) = P_0[1 + \sin(2\omega t)] \tag{8.46}$$

where ω is the grid frequency in radians per second and P_0 is the average power delivered at the fundamental frequency of the grid.

In order to perform this test, the PV emulator is connected to a grid inverter by a DC/DC boost converter, according to the scheme shown in Fig. 8.15. In particular, the boost converter is that described in Sect. 8.8.3; the grid inverter is a commercial device, i.e., the Sunny Boy 1100.

Figure 8.43 shows both the current and voltage AC components supplied by the PV emulator. It can be noted that the frequency of the two waveforms is equal to 100 Hz, i.e., twice the fundamental of the grid frequency ($f = 50$ Hz). In order to

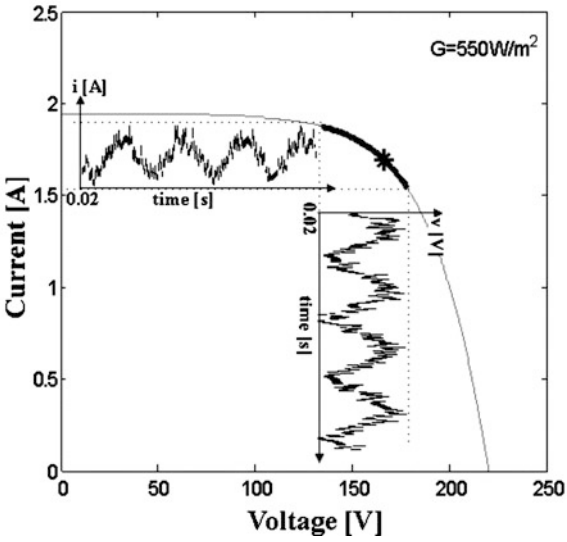


Fig. 8.44 Current and voltage fluctuations superimposed to a static I-V characteristic (From Di Piazza and Vitale (2010)). Used with kind permission from Elsevier

show the two waveforms superimposed, a suitable DC offset has been set in the oscilloscope. The voltage fluctuation is lessened by the presence of a DC link capacitor at the PV emulator output as it occurs in real operating conditions.

Finally, Fig. 8.44 shows the current and voltage fluctuations in grid-connected configuration, superimposed to a static I–V characteristic. It is shown in particular, the effect of the grid connection on the operating point, whose position varies with pulsation 2ω around the MPP. In this test, to highlight the voltage fluctuation, a lower DC link capacitance is used.

8.10 Conclusions

This Chapter presents an analysis of the fundamentals of feedback control for DC/DC converters and an example of emulator design realized by a buck converter.

The choice of the buck scheme is justified on the basis of the possibility to implement an appropriate control strategy for the emulation purpose.

Both the PV model and the power converter, used for the emulator set up, are first simulated in Matlab-PLECS® environment, then the practical implementation of the control algorithm on a DSP board and the overall PV emulator equipment are described.

Experimental results show that the developed PV emulator is able to reproduce correctly the electrical behavior of a real PV source under any environmental situation, including partial shading and rapidly changing conditions.

The pole placement control technique allows to achieve a dynamics and an output impedance that makes the emulator suitable to be properly used in

association with any converter connected at its output. All these features are obtained by a quite cheap equipment.

The whole equipment can be used to test MPPT algorithm performance and PV inverters both in stand alone and grid-connected operation.

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