Chapter 3
Silicon Carbide Electronics

One of the major benefits of silicon carbide for harsh environment microsystems is the ability to create high temperature electronics from a corrosion resistance base material. Because silicon carbide is a wide band semiconductor, it is more robust to high temperature excursions. But silicon carbide electronics requires the ability to create a substrate and thin-film layers that are high purity and can be doped in a controlled manner. The materials developments outlined in Chapter 2 lay the foundation for developing silicon carbide electronics. Besides being able to create doped, high-purity films, silicon carbide electronics requires a way to create localized doped regions in order to create specific transistor topologies as well as a metallization scheme for routing signals. This chapter will begin with a generalized process flow for creating silicon carbide electronics, followed by discussions on ion implantation doping and electrical contacts for silicon carbide. Then different electrical device topologies explored in silicon carbide will be described in the context of high power switching, high temperature amplifiers, and wireless communication.

3.1 General semiconductor process flow

A semiconductor process flow for SiC electronics fabrication is very similar to that of silicon and similar techniques are used. A run-down of the major process steps to create a SiC Junction gate Field-Effect Transistor (JFET) follows. Figure 3.1 schematically illustrates the process layers in a representative n-channel JFET fabrication process flow. But the processes are similar for other types of electronics devices or circuits. The n-channel JFET process begins with an n^+-doped substrate upon which epitaxial layers of p, n, and p^+ SiC are grown. If so desired, these epi-layers can be specified when ordering the SiC substrate. This defines the base doping levels used to create different features of the JFET. Next, a photolithographic process is used to first etch back the p^+ layer except to define the gate. This can be accomplished directly with photoresist as the etch mask or the pattern is first transferred from the photoresist pattern to a "hard mask" material such as nickel. The

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latter is typical for SiC. Using a "hard mask" allows finer feature resolution and minimizes shape changes due to mask erosion during the SiC etch. The mask material is cleaned from the wafer after the etch so as to not trap the mask material under subsequent depositions.

Another hard mask material, for instance silicon dioxide, is deposited and patterned to define the regions of doping using ion implantation. Ion implant will be discussed in more detail in the subsequent section. After the ion implant, the hard mask material is removed from the surface. This completes defining the doped regions of the device. Drawing parallels from silicon processing, it may be beneficial to follow this with a light nitrogen doping to reduce the series resistance at the gate-to- drain or gate-to-source, although this is omitted from the basic process flow in Figure 3.1. A thermal cycle to 1200 °C is used to activate the implanted dopant.

Next, another dielectric film is grown or deposited and again patterned to provide contact vias. Vias are needed to complete the routing of the interconnect layer to the source, gate, and drain of the JFET. Current device research may sometimes grow silicon dioxide on the SiC surface using a high temperature furnace; however, silicon dioxide films grown from SiC substrates tend to be of poor quality. This will be more fully explored in Section 3.2. As will be pointed out in more detail, alternate dielectrics are strong contenders for use with SiC. In particular sputtered α-AlN and LPCVD silicon nitride are both good insulators and have CTE relatively close to SiC, which is beneficial from a thermal stress perspective. In a research environment, the dielectric may simply be deposited, but no further processing to planarize the resulting surface is pursued (see Section 2.6, Planarization). This step is not technically necessary for research because lithographic resolution to increase device intensity is not critical when trying to make just a handful of functioning devices. As density and cost become important, planarization becomes crucial in order to optimize lithographic pattern size of subsequent steps. The dielectric is patterned to allow electrical access to the underlying transistor features.

The electrical contact metal is deposited and lithographically patterned. A range of metals are used, ranging from aluminum to nickel to platinum. After the photodefined mask material is removed, the most basic version of a SiC electrical device is defined and can be tested. If additional routing is not needed, another dielectric is deposited over the substrate and again patterned to provide electrical contact to the circuit. However, as devices begin to be connected, the process can be extended to provide a second metal routing layer following the same sequence of metal deposition, inter-metal dielectric deposition, and final dielectric passivation and patterning to provide bond wire access. As circuitry repeats, additional metal routing layers can be added. For example, commercial silicon semiconductor processes may have 3 to 7 metal routing layers. Making good electrical contact to SiC, especially for high temperature applications, has been a challenging area of research and will be discussed in Section 3.3.

Some special features may be added to this generic process flow depending on the particular device being created. For instance, to make an insulated gate transistor, a trench needs to be formed between the n^+ regions to form a physical way of separating source nodes. Also, most power devices operate using a substrate contact

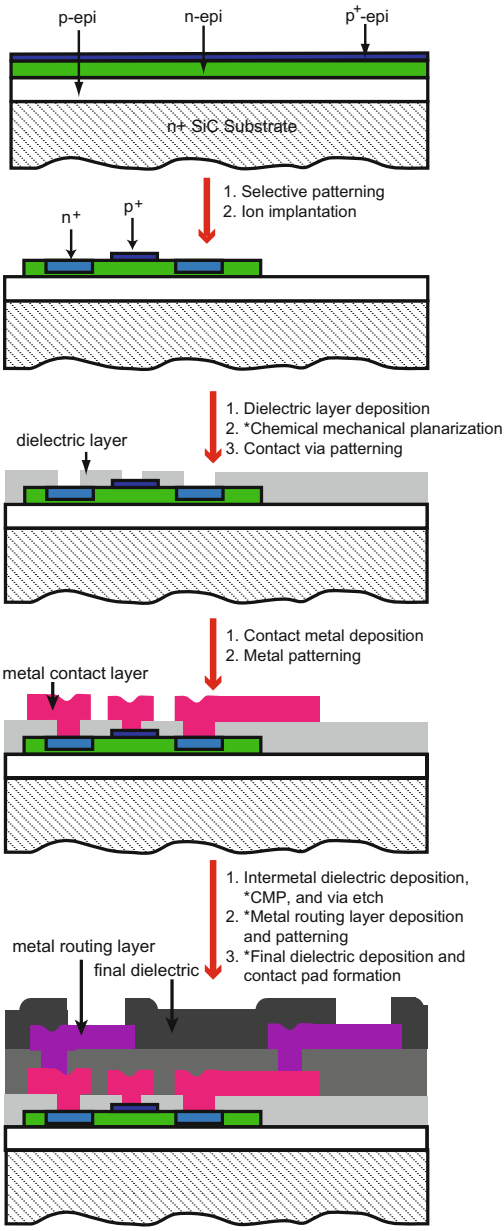

Fig. 3.1 Generic cross-section schematic process flow for a n-channel junction gate field-effect transistor with two metal layers.

as the cathode or collector node of the device, which requires an additional metal deposition and patterning on the backside of the wafer.

Table 3.1 Penetration depth of common donor and acceptor ions with respect to ion-energies [4]

Ion Type	Penetration Depth (μm)	Ion energy (MeV)
n^+ (donor)	2.3	4
p^+ (donor)	2.0	4
B+ (donor)	1.3	1
Al+ (donor)	0.9	1

Although etching and epitaxial film growth have been well covered in Chapter 2, ion implantation doping and electrical contacts are special issues in SiC and require additional detail. After these aspects of SiC electronics are discussed, the chapter will explore various transistor topologies in the context of three specific application areas.

3.2 Ion implantation doping

SiC device fabrication requires creation of laterally patterned p^+ and n^+ doping regions. In silicon technology, p^+ (acceptor) and n^+ (donor) regions are created using diffusion or ion implantation doping. In the case of SiC, the diffusion coefficients of most impurities are negligible below 1800 °C making the conventional diffusion techniques using standard masking materials impractical. Thus, the ion-implantation technique is generally implemented for selective doping SiC.

Selective ion implantation is a three step process that starts with patterning of a masking layer to define the doping region followed by ion implantation to incorporate donor or acceptor ions into the SiC lattice. Finally, the masking layer is stripped and the ion implanted sample is annealed at a high temperature in order to activate the dopant and heal lattice damage caused by the ion bombardment. When compared to ion-implantation of silicon, SiC requires high ion-energy, robust masking materials, and higher temperature post-implantation annealing.

The density of SiC is relatively high in comparison to silicon; therefore, it requires higher ion-energies compared to silicon in order to create an equivalent doping profile [1]. The energy range starts from a few tens of keV for shallow doping to as high as a few MeV for deep implant [2]. Figure 3.2 shows how ion energy affects the dopant distribution at various depth profiles for phosphorus ion implantation into 6H-SiC [3]. Typically, a few ion implantation cycles with varying energy are employed to obtain a uniform vertical doping profile. The specific energy profile used for fabricating a particular device can be based on many factors. They include device-architecture-imposed doping profile constraints as well as the type of the ion. With regards to the type of the ions, penetration depth is higher for the smaller ions than that of larger ions at the same ion energy. The predicted penetration depth of common donor and acceptor ions are presented in Table 3.1.

Generally, nitrogen and phosphorus ions are used in ion implantation of SiC to form the n-type region while aluminum and boron are used as the p-type dopant. The

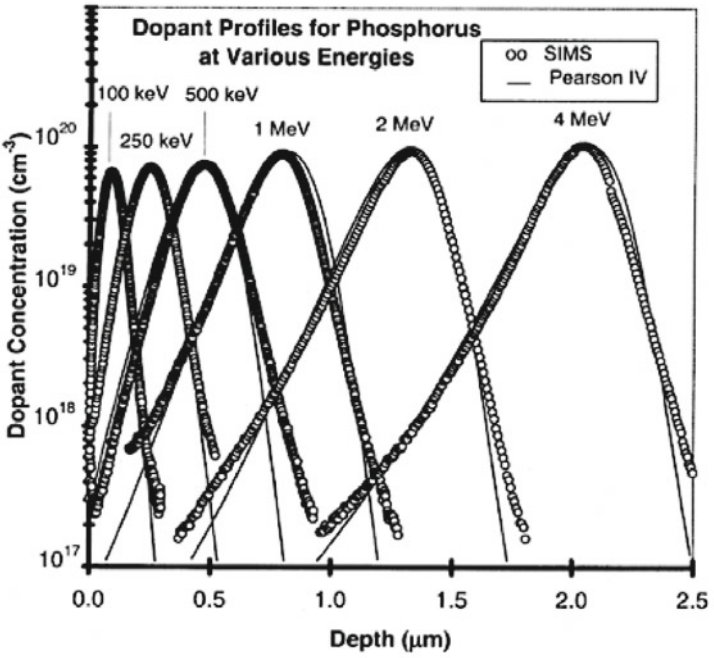

Fig. 3.2 [3] Experimental depth profile for phosphorus ion implantation into 6H-SiC at various energy (©Springer 1999), reprinted with permission.

shallowest ionization energy for these dopants for 4H-SiC and 6H-SiC are listed in Table 3.2 [5, 13]. The high ionization energy of these donors and acceptors in SiC limits the achievable carrier concentration in devices operating at room temperature. This also demands a higher concentration of dopant atoms to be implanted, causing greater lattice damage. Phosphorus has an advantage over nitrogen when high donor concentration is required because of its high solubility in SiC. Aluminum ion implantation is preferred for forming a low-resistance p-type region because the ionization energy of aluminum is shallower than that of boron; however, boron ion implantation is effective for ion implantation in deeper regions because of its higher penetration depth due to its low atomic mass. Efficient activation of p-type dopant in a wide bandgap semiconductor is relatively difficult. Nonetheless, p-type doping is routinely done because it is extremely important for many device applications.

As previously discussed, the higher ion energy and larger implantation dose required for SiC ion implantation causes increased lattice damage compared to silicon. To repair this ion-induced lattice damage and electrically activate the dopant by migrating implanted ions from interstitial to lattice sites, a post-implantation anneal is required. The annealing temperature varies with ion dose and ion energy because these factors are directly related to the crystal damage. The annealing tem-

Table 3.2 The shallowest ionization energy for dopants in 4H-SiC and 6H-SiC [5, 13].

Dopant	Ionization energy (meV) for 4H-SiC	Ion energy (MeV) for 6H-SiC
Nitrogen	45	85
Phosporus	80	80
Boron	285	300
Aluminum	190	240

perature typically ranges from 1200-1800 °C, higher than that needed for silicon. Even though post-implantation annealing is a required step, it creates several unwanted problems. First, this very high temperature annealing causes preferential silicon evaporation from the SiC surface leading to surface roughening. However, it can be mitigated by maintaining silicon overpressure (silicon-rich ambient) during the anneal. This is typically done by placing the implanted wafer in a SiC crucible with SiC powder inside or flowing silane during the annealing process [7]. Second, if ion implantation causes the formation of fully or nearly amorphous SiC, it is difficult to fully restore the crystal structure. The very high temperature conditions required for anneal lead to segregation of carbon and silicon leading to non-stoichiometric regions and formation of multiple polytypes. These factors adversely affect the electrical characteristics of the doped regions making them unsuitable for device fabrication. Therefore, it is desired to keep lattice damage to a minimal level during the ion implantation process, which in turn allows lowering the post-implant anneal temperature. For this reason, ion implantation of SiC is generally carried out at elevated temperatures (500-1000 °C) [1]. The elevated-temperature assists some crystal restructuring during the implantation process and reduces the lattice damage and segregation of displaced silicon and carbon atoms [8, 9].

The high energy and the high temperature conditions of SiC ion implantation impose extra requirements on the masking materials. First, the high ion-energy requirement demands that masking materials be thicker or denser than masking materials used for obtaining a similar doping profile in silicon. The elevated temperature during implantation requires a mask layer that withstands these conditions. Currently, either a thick silicon dioxide layer or refractory metal such as nickel is used as the robust masking material [1].

3.3 Contacts to SiC

SiC microsystems require metal to SiC electrical contacts for both MEMS and electronics. Both ohmic and Schottky contacts are necessary to transfer signals in and out from sense electronics, MEMS, and communication circuitry. Schottky contacts are particularly required for SiC electronics that provide switching and rectification. To fully exploit SiC for harsh environment microsystems, electrical contacts between SiC and metal must be reliable for operation in extreme conditions such

as high temperature and high power. Even though several promising advances have been made in forming both ohmic and Schottky contacts, reliability and long-term stability of metal-semiconductor contacts are key limiting factors that hinder operating SiC-based electronics in extreme conditions.

3.3.1 Ohmic contacts

Electrical connections between a metal and a semiconductor that have a linear current-voltage (I-V) response curve with very low specific contact resistance are called ohmic contacts. In order to create these conditions, negligible Schottky barrier height (SBH) is needed. Wide-bandgap semiconductors have relatively large SBH when compared to narrow-bandgap semiconductors due to the larger work function difference between the metal and semiconductor. Each SiC polytype has a slightly difference band gap height. The work function of different metals also vary. Therefore, both SiC polytype and contact metal influences the SBH. There are many other parameters that affect the SBH as well. Dopant concentration, type of dopant (n or p), pre-metal-deposition surface preparation, metal deposition process, and post-deposition annealing conditions, all have an impact on the electrical characteristics of the SiC-metal interface [10, 11, 12].

In general, almost every metal-SiC interface exhibits Schottky (rectifying) behavior when the metal is in the as-deposited state [13]. However, certain process steps such as post-deposition annealing can be implemented to convert rectifying contacts to ohmic contacts. Annealing typically creates a reaction layer between the metal and SiC, which helps to reduce the SBH. The reaction layer consists of metal-silicide, -carbide, or both. Post-deposition annealing is typically performed between 950-1100 °C. Optimizing annealing conditions is highly critical for each different combination of metal, SiC polytype, and dopant in order to obtain the lowest contact resistance possible. Figure 3.3 shows the I-V Characteristics of a TiW/3C-SiC contact as a function of annealing temperature and heating method: vacuum oven or rapid thermal annealing (RTA) [15].

Dopant concentration and type both heavily influence the resulting contact resistance. For instance, specific contact resistance values for nickel on n-type SiC range between 10^{-2} and 10^{-6} Ωcm^2 for the same annealing and deposition conditions. Lower contact resistance is achieved if the dopant concentration exceeds 10^{19} cm^{-3} [12]. For most metals, p-type SiC exhibits higher SBH at the metal-semiconductor interface and requires higher annealing temperatures in order to form ohmic contacts. Furthermore, lowering contact resistance when forming a contact on p-type SiC requires a higher dopant concentration than that the equivalent n-type SiC [12]. Typically, ohmic contacts to p-type SiC contain aluminum because aluminum enhance the p-type concentration at the SiC surface, which in turn reduces the SBH.

Many different metals have been investigated. Nickel is one of the widely used metals for creating ohmic contacts to n-type SiC. Nickel contacts to n-type SiC achieve low specific contact resistance and exhibit excellent electrical and physical

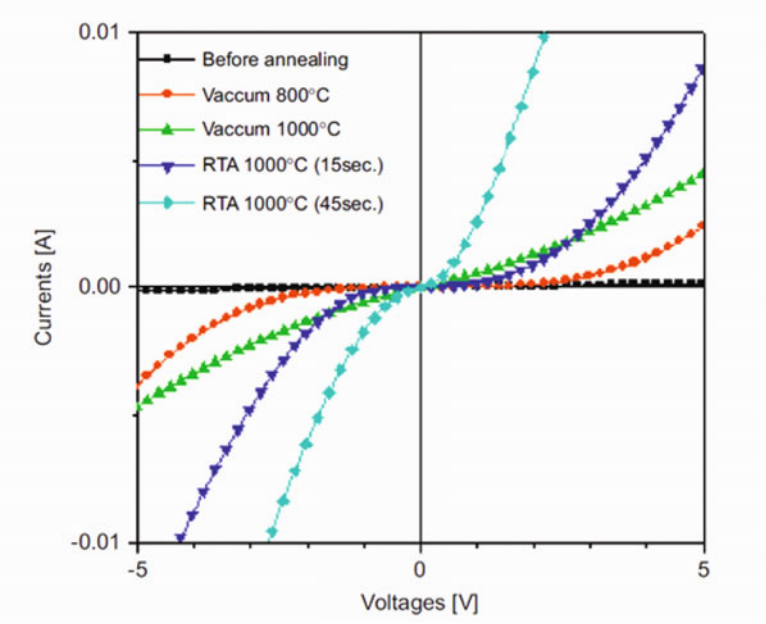

Fig. 3.3 [15] I-V Characteristics of TiW/3C-SiC contact depending on annealing temperature and conditions: vacuum oven or rapid thermal annealing (©Springer 2008). Reprinted with permission.

stability, making them a good choice for long-term operation of high power devices. Additionally, many refractory metals such as titanium, molybdenum, tantalum, and chromium as well as multi-layered structures have been successfully implemented. Multi-layered stacks include titanium/tungsten, titanium/tungsten/nickel, and titanium/titanium silicide/platinum (Ti/$TaSi_2$/Pt) [12, 16]. For ohmic contact to p-type SiC, generally, aluminum and aluminum-based alloys such as AlTi, AlTiW are used [11, 12].

Most ohmic contacts developed to date provide sufficiently low ($< 10^{-6}$) contact resistance needed for device operation. These contacts have been experimentally validated for long-term operation up to 300 °C [13]. However, some harsh environment SiC microsystem applications require contacts that can reliably withstand 500-600 °C ambient. To date, the reliability of contacts is the limiting factor for high temperature operation of SiC devices. Many contact metals tend to further react with SiC during high temperature operation, resulting in an increased reaction layer, which eventually impacts contact performance. Furthermore, oxidation and electromigration also degrade the electrical quality of the metal-SiC interface.

Both single- and multi-layer metallization schemes have been investigated for creating stabile ohmic contacts for high temperature operation. Single-layer metal contacts exhibit increased specific contact resistance when operating temperatures exceed 300 °C. Multi-layer metallization schemes show greater promise. Recent work also investigates creating a nanocrystalline carbon interfacial layer on the SiC surface before depositing a Pt contact metal [14]. This contact is tested up to 540 °C with negligible increase in contact resistance. One of the notable multi-layer schemes, Ti/$TaSi_2$//Pt, developed at NASA Glenn Research Center, has shown to operate over 1000 hours in air at 600 °C without significant changes to contact resistance[16]. Later, this Ti/$TaSi_2$/Pt metallization was successfully implemented in the fabrication of SiC JFET devices that have demonstrated stable operation for over 10,000 hours at 500 °C [35]. Despite these successes, many aspects of forming metal contacts to SiC have to be investigated. These include identifying thermodynamic, reaction kinetic and dominant failure mechanisms of the metal-SiC interface at elevated temperatures in oxidative environments.

3.3.2 Schottky contacts

Schottky contacts are vital for many SiC devices including the widely used high-frequency metal-semiconductor field-effect transistor (MESFET) and fast-switching rectifiers. The larger SBH and thermal stability of the contact are key parameters for high temperature operation and low power loss. The SBH depends on many parameters, including the work function of the metal. According to Schottky-Mott theory, high work function metals are required for larger SBH. Pt, Ni, Au, and Pd are preferred Schottky contacts to SiC because of their relatively high work function [18, 19]. The pre-metal deposition surface preparation also can cause dramatic changes in the resulting SBH. For instance, Teraji *et al.* has shown drastic SBH changes for the same contact metal, titanium, when two surface cleaning procedures are used [20]. Furthermore, SBH strongly depends on chemical reactions at the metal-SiC interface. Therefore, interfacial physics and chemistry aspects must both be considered in order to fabricate reliable Schottky contacts.

Although almost all metal-SiC contacts exhibit Schottky (rectifying) behavior in the as-deposited state SiC, they tend to form either a silicide or carbide interlayer, or possibly both, at high temperatures, reducing the SBH. This leads to an increase in reverse-bias thermionic leakage of carriers over the junction barrier. State-of-the art SiC Schottky diodes typically are limited to operation below 400 °C because of the reverse-bias (off-state) leakage current [13]. Similar to ohmic contacts, there are few examples of thermally stable Schottky contacts at high operating temperatures. For instance, some limited success in creating thermally stable contacts has been reported using tungsten carbide deposited at high temperature. Tungsten carbide deposited on p-type 6H-SiC exhibits a high rectification ratio with a low reverse current density (6.1×10^{-5} A cm^{-2}, -10 V) up to 500 °C [21]. Recent reports shows refractory metal borides are also very promising for forming stable high temperature

Schottky contacts to SiC [22]. However, more research focusing on this issue is needed.

3.4 Electronics for high power applications

A special application space for electronics is regulating high power devices. Vacuum tube components were replaced with silicon transistors in the 1950s. Specialized topologies requiring non-standard microfabrication compared to microprocessor and memory are often utilized (substrate trenching, multi-level doping profiles, and backside contacts). The added cost from not using the most standardized processes is well compensated by the important applications enabled by these high power switches and rectifiers. Power applications are plotted in Figures 3.4 and 3.5 [23]. Figure 3.4 plots applications as a function of frequency and power rating. As can be seen by the graph, high frequency applications tend to have lower power handling demands compared to low frequency applications. Figure 3.5 makes a similar distinction, but this time between voltage and current handling capabilities. The device topology differs depending on operating frequency, required voltage and current capability, or blocking capability. For instance, applications below 100 V are well served by silicon Schottky diodes. However, above this voltage, bipolar topologies are used [23].

Silicon carbide has been investigated for high power switching and rectifying applications because it is a wide-band semiconductor. This enables extending the higher performance of unipolar devices to operating voltages as high as 5000 V instead of needing to switch to bipolar device topologies [23]. As will be discussed in more detail, the higher blocking characteristic of the silicon bipolar device comes at the cost of switching transients. These transients are inefficient periods compared to ideal behavior, resulting in power loss and an effective degradation in switch frequency. Furthermore, high power switching generates significant heat that needs to be dissipated. Silicon carbide has nearly three times the thermal conductivity as silicon, which aids in heat dissipation. But being a wide-band semiconductor also allows silicon carbide devices to operate to higher temperatures without thermally-induced leakage due to intrinsic carrier concentration variation with temperature. The major device topologies and design tradeoffs in the context of high power handling will be discussed in subsequent sections.

3.4.1 Schottky Rectifier

The Schottky rectifier is a popular unipolar device because its basic fabrication requirements are simple, it offers fast switching speed, and it has a relatively low on-state resistance. The one-dimensional representation of the structure is shown in Figure 3.6. The basic Schottky rectifier is created by depositing a metal onto the

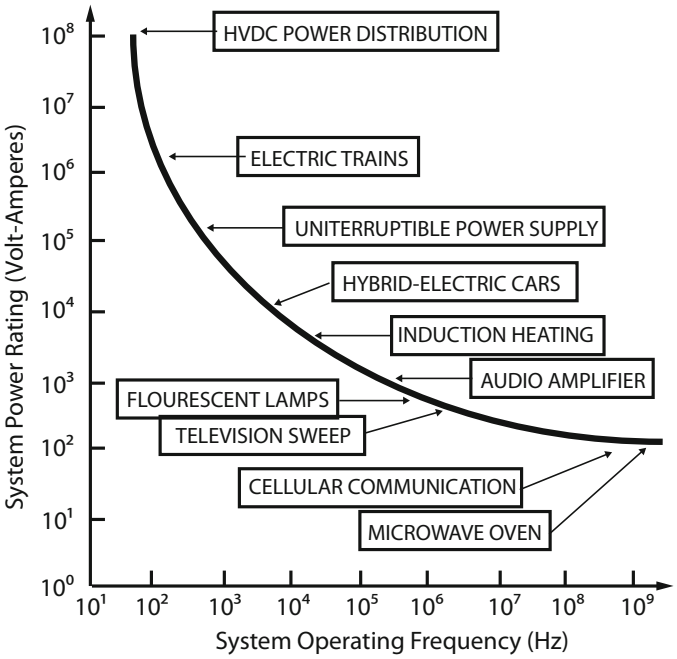

Fig. 3.4 [23] High power applications versus operating frequency and power handling requirements (©Springer 2009). Reprinted with permission.

substrate surface. The metal becomes the anode region while the backside of the wafer is the cathode. The applied voltage between the anode and cathode creates a drift region within the substrate, next to the anode. By applying a negative bias to the cathode, current flow occurs by electrons migrating from the metal-semiconductor interface through the substrate. While in the on-state, current is sustained using majority carriers. This means few minority carriers build up within the drift region. This enables rapid switching to the off-state by establishing a depletion region inside the drift region. Silicon devices of this type can support blocking voltages of 100 V.

The Schottky rectifier can obtain a larger barrier height in SiC because of the increased band-gap compared to silicon. This allows supporting even higher blocking voltages. The majority of applications shown in Figure 3.4 require fast switching, low on-resistance, and blocking voltages of 500 V or less. SiC Schottky rectifiers can be used to span a large region of the application space since it is possible to extend the breakdown voltage to 3000 V if using SiC [23].

The drawback of the Schottky rectifier is large off-state (reverse bias) leakage current. Because of the present state of achievable n^+ substrate doping for SiC, the substrate resistance becomes a concern for power dissipation: Si can be as low as 1 mΩ-cm, compared to SiC, which is typically 20 mΩ-cm. The barrier height and saturation current is also a strong function of operating temperature in silicon,

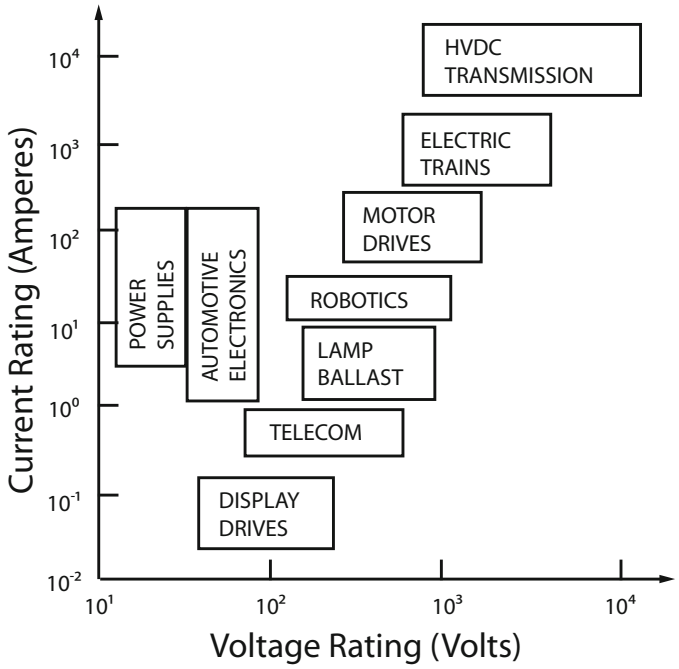

Fig. 3.5 [23] High power applications versus voltage and current requirements (©Springer 2009). Reprinted with permission.

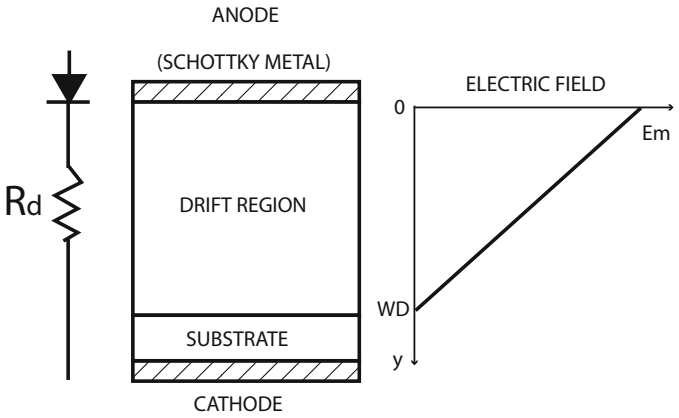

Fig. 3.6 [23] Electrical field distribution in a Schottky rectifier (©Springer 2009). Reprinted with permission.

which increases both the on-state resistance and off-state leakage current. However, the net impact of increased temperature on a SiC Schottky rectifier is smaller. SiC Schottky rectifiers can also leverage the larger barrier height to create a rectifier that is designed to maintain an acceptable power dissipation in the reverse blocking

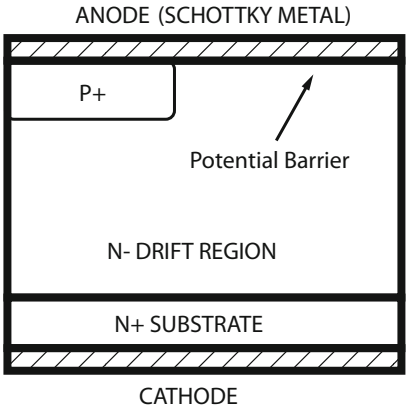

Fig. 3.7 [23] Schematic silicon carbide Junction Barrier controlled Schottky (JBS) rectifier structure (©Springer 2009). Reprinted with permission.

mode even though the leakage current increases more significantly with increased reverse voltage compared to silicon. For example, a particular 3kV 4H-SiC Schottky rectifier at room temperature exhibits less than 1 W/cm^2 in the off-state compared to 100 W/cm^2 of dissipation in the on-state [23].

To combat the leakage current problem with the Schottky rectifier configuration, various approaches to shield the metal-semiconductor interface from directly sustaining a large electric field, such as utilizing a p-n junction or introducing a second metal with an even larger barrier height, have been introduced. These two methods are known as the Junction Barrier controlled Schottky (JBS) and Trench Schottky Barrier controlled Schottky (TSBS) rectifier schemes, respectively. These methods will be discussed in more detail next.

3.4.2 JBS Rectifier

Schottky rectifiers balance on-state power loss with reverse blocking power loss through reduction in Schottky barrier height until the reverse blocking power loss dominates. This in turn reduces the maximum operating temperature. However, as was discussed in the previous section, this reverse blocking power loss occurs because of the high electric field across the metal-semiconductor interface. The Junction-Barrier controlled Schottky (JBS) rectifier attempts to prevent creating a high electric field when in the off-state by injecting closely spaced p^+ regions, creating local p-n diodes, directly under the anode (Figure 3.7). These p^+ regions create a potential barrier to shield the contact. A smaller separation and larger junction depth improves the electric field reduction. However, the p^+ regions impede conduction during the on-state. Hence, the spacing must be optimized to meet both on-state and off-state performance specifications.

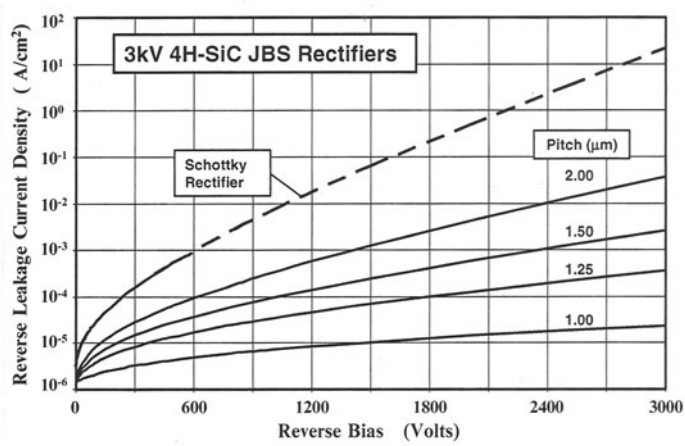

Fig. 3.8 [23] Leakage current suppression in a JBS rectifier as a function of p-region pitch (©Springer 2009). Reprinted with permission.

Since the reverse blocking leakage current is more significantly influenced by a high voltage because of the more efficient generation of current through thermionic field emission (tunneling), the JBS rectifier structure can improve the performance of silicon carbide devices significantly. In SiC devices, the p-type dopants are introduced using ion-implantation, with the mask spacing dictated by the space needed to make the Schottky contact. The same metal layer used to make the Schottky contact to the n- region is typically used to make contact to the p^+ region for processing convenience [23].

The influence of the pitch of the p^+ region on reverse blocking leakage current is shown in Figure 3.8. Reducing the pitch down to 1.5 to 1.25 μm reduces the electric field at the metal-semiconductor interface by about half. However, this results in a 10^5 reduction in leakage current. This pitch range also demonstrates excellent on-state conduction when the p^+ region depth is 0.5 μm and is paired with a 20 μm drift region in order to support blocking 3kV in the off-state. Further decreasing the pitch increases the on-state power loss compared to a standard SiC Schottky diode of the same dimensions [23]. It should be noted that this pitch is fortunate from a practical perspective. Because of the current SiC wafer sizes (100mm diameter or less), equipment for handling substrates in this size range can have difficulty producing highly-repeatable, sub-micron dimensions.

Although this approach is popular for SiC rectifiers because it creates a dramatic reduction in off-state leakage current and small increase in resistive loss in the on-state without the need to resort to a bipolar configuration. A drawback though is the additional ion-implantation requires an activation anneal and creates additional lattice damage. This results in the need for very high temperature annealing (approximately 1600 °C). Thus, another method to create a similar shielding of the Schottky contact will be explored next that does not rely on an additional ion-implantation.

3.4.3 TSBS Rectifier

The drawback of the Schottky rectifier for high voltage applications is the high leakage current in the off-state due to thermionic emission from the metal-semiconductor interface when it is supporting a large electric field. Another method of shielding the Schottky contact from having to support a large electric field is to place a second high barrier Schottky metal within a vertically-walled trench. This device topology is known as the Trench-Schottky-Barrier controlled Schottky barrier (TSBS) rectifier.

The device topology essentially replaces the p^+ doped region buried under the anode with a physical region refilled with a metal that has a higher barrier potential than the anode metal. For example, a 4H-SiC device with blocking voltages of 300 V that uses titanium as the main Schottky contact and nickel in the trenches has been successfully demonstrated [24]. This additional processing complexity compared to ion-implantation removes the need for a post-implantation anneal at 1600 °C, which tends to roughen the SiC surface, degrading the anode-semiconductor contact. The net effect of the TSBS rectifier topology is similar to the JBS rectifier and similar design implications apply. Deeper, narrower trenches with close pitches on the order of 1 to 1.5 μm provide better shielding of the anode metal to semiconductor interface, reducing the resulting leakage current in the off-state while maintaining nearly equivalent on-state performance. This comes at a compromise in breakdown voltage characteristics, reducing it to approximately 80 percent of the ideal parallel plate due to edge termination [23]. However, this is equivalent to the JBS rectifier as well.

In the Si rectifier, the on-state voltage drop versus the reverse leakage current are very similar for a JBS configuration versus a TSBS configuration designed for 50 V. However, performing the same analysis for a 3 kV SiC rectifier, the TSBS configuration exhibits approximately 0.2 V lower on-state voltage drop compared to the JBS configuration (Figure 3.9). This is attributed to a larger depletion width under on-state operation in the JSB rectifier structure in 4H-SiC because the built in potential for the p-n junction is much larger than the contact potential for the metal in the trenches of the TSBS rectifier [23].

3.4.4 P-i-N Rectifier

The TSBS and JBS topologies work well for certain voltage ranges. However, for motor control applications, much higher voltage blocking and current carrying capability are required. In these applications, the on-state voltage drop of these topologies becomes significant. For these applications, silicon p-i-n rectifiers were developed. The i-region in this case is a low doped n- region between a highly doped p^+ and n^+ region, essentially silicon at its intrinsic carrier doping level. When very large voltages are applied to this structure, conduction through the intrinsically doped region is dominated by injection of minority carriers.

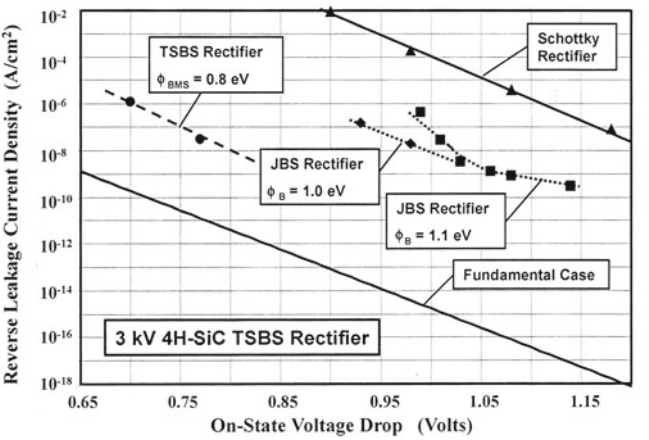

Fig. 3.9 [23] Trade-off curve for a 3 kV 4H-SiC TSBS rectifier compared to a JBS and Schottky rectifier (©Springer 2009). Reprinted with permission.

Because the device physics utilized in this structure injects a large number of free carriers into the drift region during on-state current flow, switching the p-i-n rectifier to the off-state to the point where the rectifier can again support a high voltage requires removing these carriers. Figure 3.10 presents simulation results of free carrier density versus distance into the drift region. Each contour represents time after the rectifier is switched to the off-state. Removing free carriers results in effectively slowing down switching from the on-state to the off-state compared to the previously discussed rectifiers. This is known as reverse recovery. This switching time equates to a power loss during switching. Additionally, this loads the other components of the circuit, making it necessary to increase their breakdown voltages as well.

The SiC p-i-n rectifier has a much narrower drift region for the same breakdown voltage capability compared to the silicon equivalent. This enhances the switching speed characteristics of a SiC p-i-n rectifier. However, the same large bandgap that enables the high breakdown voltage increases the on-state voltage drop by a factor of four compared to silicon. The design trade-off between speed and on-state resistance favors SiC p-i-n rectifiers over Si p-i-n rectifiers or SiC Schottky diodes when the voltage ratings exceed 10 kV.

3.4.5 MPS Rectifier

The p-i-n structure has been shown to be effective for very high power applications; however, it suffers from slow switching speed because it relies on minority carriers. These minority carriers must be dissipated before full reverse bias block-

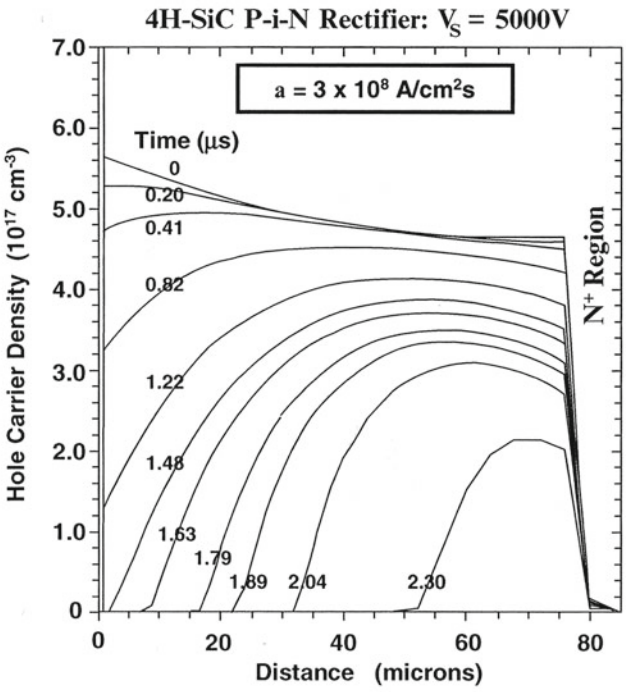

Fig. 3.10 [23] Carrier distribution in a 10 kV 4H-SiC p-i-n rectifier during the reverse recovery transient (©Springer 2009). Reprinted with permission.

ing is achieved. This delay limits the maximum switching speed and also creates a switching power loss during the on-to-off transient. In order to reduce the transient, a structure that reduces the conductivity during the on-to-off transition period is needed. Although the topology can be schematically represented identically to the JBS rectifier (Figure 3.7), the Merged Physics Structure (MPS) rectifier substitutes the n^- drift region of the JBS rectifier with a drift region that is operating as an intrinsic semiconductor, identical to the p-i-n drift region. The MPS rectifier can also be seen as putting a p-i-n rectifier in close proximity to a Schottky rectifier. However, assuming the structures do not interact would lead to the conclusion that the MPS structure would yield the worst performance of each topology. But in fact MPS works because of an interaction between these structures. Like the JBS and TSBS rectifier topologies, the pitch of interleaving the p-i-n rectifier and Schottky rectifier influences the overall device performance. With careful design, the MPS structure will outperform the p-i-n structure for a given current handling and blocking voltage design point.

The Schottky rectifier portion of the MPS structure has a lower potential barrier than the p-n junction in the p-i-n region, which aids in reducing on-state resistance (forward voltage drop) compared to a standard p-i-n (Figure 3.11). This reduced bar-

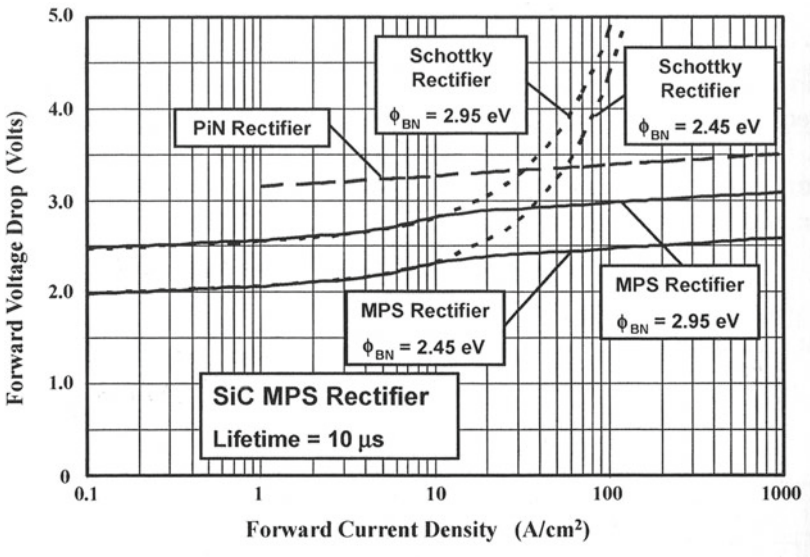

Fig. 3.11 [23] On-state characteristics of 10 kV SiC MPS rectifiers of different barrier heights as well as comparative curves for equivalent p-i-n and Schottky rectifier designs (©Springer 2009). Reprinted with permission.

rier path results in up to a 10 fold decrease in stored energy in the rectifier in the on-state. In the reverse blocking mode, the Schottky rectifier region causes larger leakage current under high applied voltages. This is combated by reducing the Schottky contact width significantly compared to the p-i-n region. However, switching speed is improved because the Schottky contact portion of the MPS enables supporting some voltage immediately when the rectifier is commanded to the off-state. During the transient while the injected minority carriers associated with the p-i-n structure are dissipated, the Schottky rectifier portion reduces unwanted power dissipation. This results in a 10 kV SiC MPS rectifier having approximately half the peak reverse recovery current and half the overall reverse recovery time compared to an equivalent p-i-n rectifier according to numerical simulations [23].

3.4.6 BJT

As was discussed in Section 3.4.1, unipolar rectifiers are preferred because they exhibit acceptable power dissipation and faster switching speed for lower voltage applications — this limit is 300 V for Si and 3000 V for SiC. Hence, SiC is seen as providing an overall performance improvement compared to silicon-based technologies between 300 V and 3 kV. However, exceeding 3 kV, bipolar SiC topologies need to be considered.

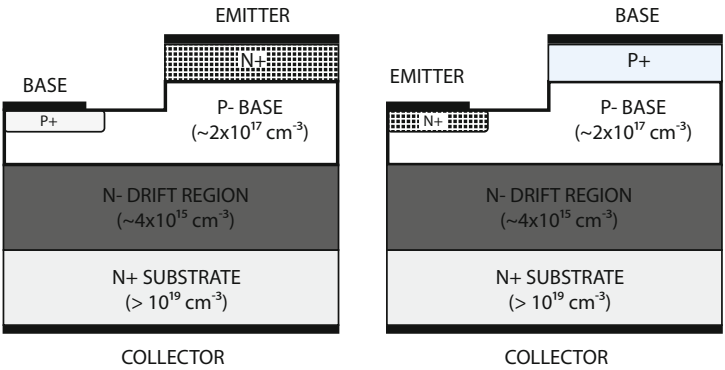

Fig. 3.12 [26] Schematic cross-section of (left) an epitaxial and (right) implanted emitter SiC bipolar junction transistor (©Springer 2004). Reprinted with permission.

The Bipolar Junction Transistor (BJT) is one such topology (Figure 3.12). Bipolar devices typically exhibit lower breakdown voltages compared to their p-n junction equivalents due to current gain; however, the *npn* configuration has been shown to be more rugged, so is more common [26]. As was discussed for the SiC JBS configuration, an ion-implanted p^+ region requires a very high temperature anneal that is best to avoid. Hence, the majority of SiC *npn* BJT topologies rely on a non-planar structure that utilizes an epitaxially grown layer to create the p^+ base region and create the n^+ emitter region through ion-implantation.

A BJT designed for high power applications will have a lightly-doped collector region and greater substrate thickness than low-voltage BJTs in order to prevent punch-through. This lightly-doped collector region reduces output current and slows down switching speed for the same reasons discussed for the p-i-n rectifier. Along with current crowding effects, the realized current gain can be significantly degraded. Hence, the power BJT can be fabricated in a two-stage configuration, referred to as a Darlington configuration, which results in an effective current gain that is the square of the individual gain stages [26]. This lightly-doped region also results in a quasi-saturation current response at high voltages. Furthermore, using an ion-implanted emitter region results in degraded current gain compared to devices that use an epitaxially grown n^+ emitter and perform a p^+ ion-implantation for the base region. This is presumably due to degradation of the SiC surface at the contact region. As with other topologies that rely on minority carrier injection during the on-state to reduce the voltage drop, the BJT does not switch to the off-state quickly. Hence, BJT rectifiers are not good choices when power cycling above 10-20 kHz is required for a given application. The BJT is also a current controlled device, which is less favorable in terms of integration with other circuitry than a voltage controlled topology.

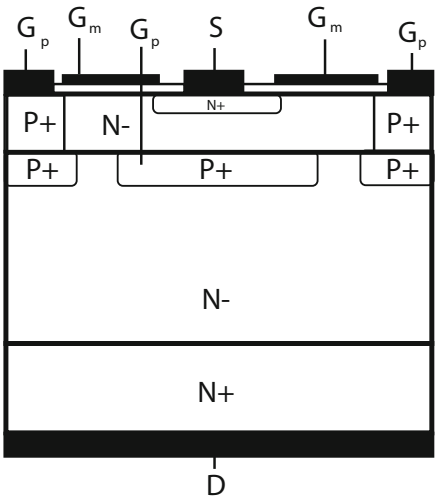

Fig. 3.13 [26] Schematic cross-section of a 4H-SiC SIAFET structure (©Springer 2004). Reprinted with permission.

3.4.7 SIAFET

Figure 3.13 is a schematic cross-section of a Static Induction Injected Accumulated Field Effect Transistor (SIAFET), also known as a bipolar-mode JFET. This structure integrates a JFET with a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) structure such that during the on-state the junction gate is over-driven beyond the turn-on voltage. By forward biasing the gate junction, minority carrier injection from the gate improves the conductivity of the channel and drift regions.

The SIAFET configuration has been experimentally demonstrated up to 6 kV using 4H-SiC. This device consists of a lateral accumulation MOS channel and a vertical JFET channel. By forward biasing the junction gate, the devices operate in a bipolar mode. Bipolar operation of a 2 kV SIAFET rectifier reduces the on-resistance to 172 mΩ-cm^2 compared to 1200 mΩ-cm^2 for unipolar operation [27]. Even higher blocking voltage designs (6.1 kV) still exhibit acceptable on-resistance, 732 mΩ-cm^2, when operated in bipolar mode.

3.4.8 Power MOSFET

The Power MOSFET is of interest because of it has significantly higher switching speed than other topologies and is voltage controlled, which is easier to implement. Furthermore, the on-state current exhibits a negative temperature coefficient, which enables parallel device configurations for additional current carrying capability. The Power MOSFET was first successfully developed using SiC in what is referred to as

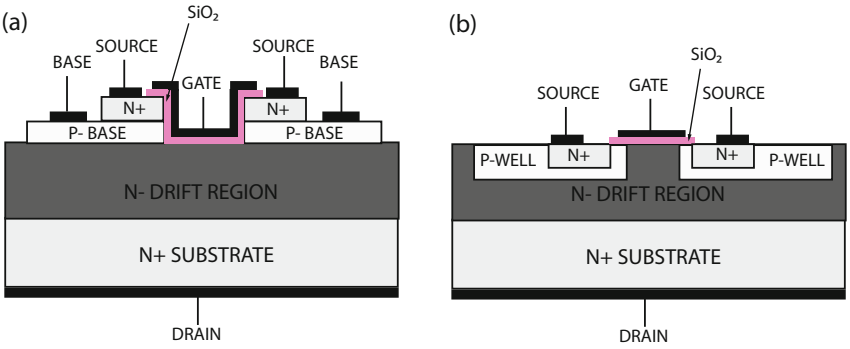

Fig. 3.14 [31] Schematic cross-sections of (a) UMOS and (b) DMOS power transistors in SiC (©Springer 2004). Reprinted with permission.

the U-shaped groove MOSFET (UMOSFET) [28]. This configuration can be made entirely from epitaxially grown layers to define the different doping regions. This in turn requires a trench be cut through the n^+ and p base region. The gate is formed by first oxidizing the trench and then coating it with the gate metal (Figure 3.14a). The reactive ion etch surface of the trench is rough and the oxide grown on SiC is of poor quality compared to thermally-grown oxide on silicon. Additionally, the growth rate is different on a Si-face surface versus a C-face surface of SiC, resulting in a thinner oxide at the base of the trench. The trench geometry also causes field crowding at the corners, causing repeated high fields being sustained by the trench oxide, which degrades device lifetime.

A more elegant solution, known as the Double-diffusion MOSFET (DMOSFET), was developed in 1998 [29]. This more planar structure eliminates the concern of poor oxide growth uniformity (Figure 3.14b). However, it added the need for ion-implantation to create the p base region and n^+ wells. This requires high-temperature annealing, which can be as high as 1600 °C and causes surface state degradation due to preferential evaporation of Si at these temperatures.

The SiC DMOSFET has been demonstrated as a 2.4 kV blocking device that operates in a normally-off condition. Up to 10 A current-carrying capability and 42 $m\Omega$-cm^2 on-state resistance has been experimentally demonstrated using a 3.3 by 3.3 mm sized device [30]. Devices able to block up to 1 kV have also been shown to operate up to 100 kHz. The interested reader is directed to [31] for details on design of a DMOSFET device.

3.5 Sensor interface electronics for high temperature applications

SiC electronics promise to open up additional application areas by potentially allowing reliable operation between 450–600 °C. Additionally, being able to operate

at high temperatures would allow more conventional applications in the realm of 300 °C, such as for automotive engine monitoring, without the need for an active cooling system for the electronics. This significantly reduces the size and cost of such systems.

Because silicon carbide is a wide bandgap semiconductor as well as has a low intrinsic carrier concentration, silicon carbide electronics are well suited for significantly higher temperature operation. Increasing temperature increases intrinsic carriers exponentially. However, SiC has an intrinsic carrier level that is four orders of magnitude lower than silicon at room temperature (10^{-6} cm^3 for 6H-SiC, compared to 10^{10} cm^3 for Si). Thus, around 300 °C, intrinsic carrier levels in Si are approaching dopant levels for low doped regions, resulting in uncontrolled device behavior. Silicon carbide also has a very low rate of diffusion compared to silicon. Hence, dopant diffusion in silicon carbide electronics is not a concern for operating temperatures below 600 °C,whereas silicon circuitry, even when built on a SOI substrate, is limited to operating below 300 °C to avoid diffusion degradation of the electronics. This section focuses on the design of sensor interface electronics in the context of high temperature operation.

3.5.1 MOSFET and MESFET considerations

SiC MOSFET and Metal-Semiconductor Field-Effect Transistor (MESFET) device topologies are prevalent in high-frequency switching, moderate voltage blocking power electronics (Section 3.4.8) and RF communication components (Section 3.6). These topologies are desired for applications requiring fast switching speeds. However, they are not well suited for high temperature operation with the current state of dielectric processing for transistor applications. MOSFETs require a much higher quality silicon dioxide layer than other topologies. SiC does not grow a high quality thermal oxide, and this oxide further degrades with increased temperature [13]. This for instance leads to -14 mV/°C degradation in V_T above 200 °C [36]. Alternate dielectrics are an area of research that may open up the use of MOSFET structures for high-temperature operation. Deposited silicon dioxide for instance may be a workable alternative [37], but as with all deposited films, thickness uniformity comparable to grown oxide is a challenge. Switching instead to a deposited dielectric opens up a wide range of material options. Other materials that also have better CTE matching or better electrical stability with temperature may be possible. Additional research is needed in this area. Although there have been early reports of 500 °C operation of MESFET devices in the past [38], MESFET technology suffers from gate-to-channel leakage currents from Schottky diodes, limiting usable operation to around 400 °C [13]. Hence, these device topologies require further development if they are to be used for high temperature sense interface electronics.

3.5.2 JFET

The SiC JFET device is a promising device for MEMS sensor interface electronics. As was described in Section 3.1, the basic device can be fabricated in a non-planar configuration primarily from epitaxially grown layers with the exception of the n^+ source and drain regions, removing the need for very high temperature annealing. Furthermore, this structure does not rely on a high quality dielectric layer for proper operation. This topology is also a high-impedance input structure. This is well suited as a MEMS sensor interface, which primarily relies on detecting changes in capacitance through driving a sinusoidal signal onto the sense capacitor plates. This requires an amplifier with a high-impedance input.

SiC electronics are still primarily based on 4H- and 6H-SiC polytypes in part due to availability of quality substrates. 4H-SiC has a wider bandgap and higher electron mobility at room temperature compared to 6H-SiC. However, 4H-SiC does not perform as well at higher temperatures. There are more transistor designs that operate at very high temperatures using 6H-SiC [32, 33]. This is because the mobility drops off more rapidly with increasing temperature in both cases, but donor levels are lower in 4H-SiC.

A single-stage, single-ended transimpedance amplifier utilizing a JFET configuration has recently been demonstrated in 6H-SiC [34]. Devices were fabricated on 2 inch diameter 6H-SiC substrates. Since hole mobility is always less than electron mobility at any temperature, this device uses a n-channel. Thus, an aluminum doped p-type substrate is used. The device was formed primarily by etching back epitaxially grown layers to form a non-planar device structure (Figure 3.15). This limits the need for only one n^+ ion-implant step. However, in reality multiple doses at different energies were used to create a box profile. The post-implantation anneal was performed at 1200 °C. A 25 nm thermal oxide was grown to passivate the device before metallization. Different contacts were tested: Ti/Al and Ti/$TaSi_2$. The contacts were annealed at 600 °C in a forming gas. The Ti/$TaSi_2$ contacts performed better at high temperature. The amplifier demonstrated a bandwidth of approximately 10 kHz up to 450 °C. However, transimpedance gain increased with temperature. This was expected because sheet resistance increases with temperature. This early work, however, paves the way for future work in high-temperature sensor interface electronics. Alternate designs, including differential designs, may yield better overall consistency with temperature. This remains an open area of research.

Recently, operation at 500 °C of 6H-SiC JFET electronics for up to 7000 hours have been reported (Figure 3.16). These devices show a high degree of stability, with g_m variation less than 10 % and V_T only 1 % [35]. However, the same testing indicates other failure modes may be of concern. Although individual JFET, digital logic elements, and epitaxial resistors remained operational over prolonged exposure to high temperature, circuits of JFET devices stopped functioning at much shorter times. This suggests that the metal interconnects are more susceptible to failure even though the JFET structure is rugged. Examination points to the metal-dielectric interface as the weak point in these fabricated devices, presumably due to CTE mismatch between the materials.

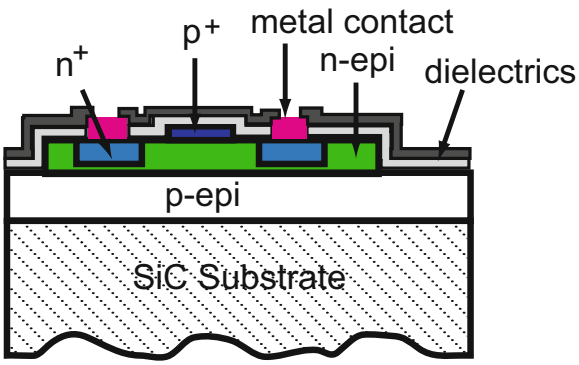

Fig. 3.15 Schematic cross-section of a n-channel JFET.

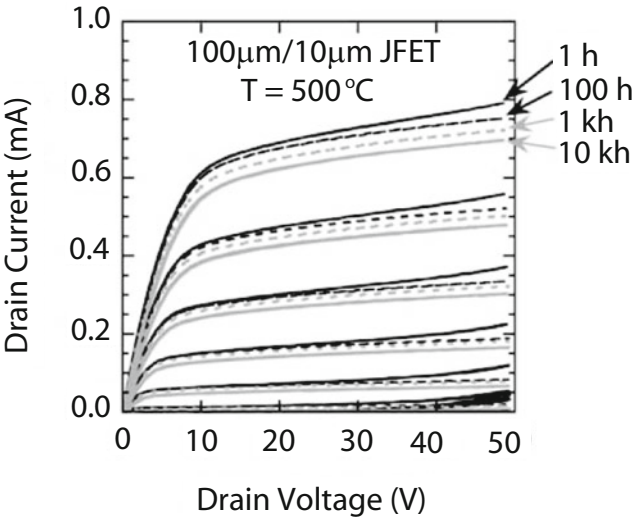

Fig. 3.16 [35] Drain I-V characteristics of packaged 100 μm/10 μm NASA 6H-SiC JFET measured during the 1^{st}, 100^{th}, $1{,}000^{th}$, and $10{,}000^{th}$ hour of electrical operation at 500 °C. Gate voltage steps are 2 V starting from $V_G = 0$ as the topmost sweep of each curve (©2009 Wiley-VCH), reprinted with permission.

3.5.3 BJT

The BJT topology is another interesting case for prolonged high temperature operation. Like the JFET, it utilizes a p-n junction, avoiding the need for high-quality dielectrics and buried metal features. A BJT device is expected to offer better on-state performance at higher temperatures than an equivalent JFET design, overcoming increased switching losses compared to a JFET [39]. Difficulty producing repeatable characteristics and lower stability in a minority-carrier device at operation

above 300 °C have favored JFET designs over BJT [40]. For instance, BJTs require high quality metal contacts to both n- and p-type SiC regions, while JFETs are tolerant of non-ideal contacts. To date, there has been a lack of research using BJT high-temperature electronics because of these issues; however, operation at moderate temperatures have been proven out. For instance BJT-based transistor-transistor logic (TTL) built in 4H-SiC were successfully operated at 300 °C with little shift in logic characteristics [41]. Development of high quality contact metal stacks will open up further research using BJT circuitry for high temperature operation.

3.6 Electronics for communication electronics

Besides high temperature operation of power regulating circuits and sensor amplifiers, the harsh environment microsystem needs communication electronics. As has been discussed earlier, whenever possible, wireless is preferred. Assuming on-board power is an option (see Section 6.2), relying on wires for signal transmission adds extra levels of packaging and development of high temperature wire shielding and connectors.

Wireless electronics is typically divided into digital circuits for low frequency and analog circuits for high frequency operation. Silicon switching is currently used for up to 1 MHz operation and can be used to drive up to 1 MW, useful enough television broadcasting. SiC switches are being explored for these high power broadcast applications because both heat dissipation is enhanced in SiC components and SiC can withstand higher temperature operation. Together, this potentially reduces the need for expensive cooling systems used in commercial silicon switching installations.

Even when dealing with modest power transmission using SiC circuitry, significant issues need to be overcome. Deep levels are created in a wide bandgap semiconductor from metals or other defects incorporated into the material, which contain much more energy and have discharge times orders of magnitude longer than in silicon. Additionally, when being used for high power circuits, larger voltages are applied across the SiC structure. These two conditions together lead to a large population of electrons getting trapped in these deep levels, leading to unstable behavior at radio frequencies [42]. Hence, even higher purity base materials are needed compared to silicon. Furthermore, to date the successful power SiC topologies tend to rely on minority carrier injection, which slows down overall switching performance. MOSFET and MESFET technologies will be preferable for high frequency operation once the issue of poor dielectric layer formation is solved. Trying to borrow from successful silicon designs, heteroepitaxial configurations are also of interest. These topologies seem most promising by combining multiple SiC polytypes. However, this requires the substrate to be made from 3C-SiC for the junction to perform as desired, and high quality 3C-SiC substrates are a challenge to produce currently. Therefore, available topologies do not favor high frequency operation. Substrate cost is also a limitation for commercial applications such as cell phones.

Although harsh environment applications are less restricted in terms of overall device cost, harsh environment operation presents additional challenges for communication electronics. From a corrosion perspective, these electronics need to rely on contact metals that are not prone to oxidation or erosion. Tungsten, molybdenum, chromium, aluminum, nickel, titanium, gold, and platinum have all been explored as contact metals, but many of these readily oxidize. Creating a metal-oxide or metal-carbide capping layer can help protect the metal, but often these oxides and carbides degrade at high temperature. Hence, titanium, gold, and platinum are favored from a corrosion perspective. However, these metals can be difficult to deposit with low stress, which may cause mechanical failure under high temperature cycling. Additionally, high temperature operation may cause reduced transmission efficiency because resistivity increases and mobility decreases with increased temperature. Furthermore, discrete inductors are often used in communication circuitry. These devices would also need to be made to withstand high temperature or a highly corrosive environment as well.

These issues should be looked at as opportunities for further research. Solutions may well exist. However, research into the specific combination of high temperature and wireless power transmission has not been fully explored to date. For instance, further work in optimizing metal stacks for not only electrical contact stability but also general mechanical adhesion should lead to the desired reliability in metal interconnects. Dielectric development will improve the reliability of faster switching speed device topologies. Additionally, high temperature designs using low frequency transmission may be the preferable solution for harsh environment microsystems. SiC power devices have made significant development in the relatively short time that high quality substrates and epitaxial layer growth has been available. So it is not unreasonable to assume a similar pace can happen for high temperature SiC circuitry for sensor interface and signal transmission as well.

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