

Chapter 4

In-Use Failures

4.1 Introduction

This chapter addresses in-use failures of MEMS, with an emphasis on the physics of failure. [Chapter 3](#) dealt with eliminating failures from a design and manufacturing perspective. In this chapter we focus on how a well-designed, fabricated and packaged device can fail in use. There is a tight link between the design, manufacturing and in-use failures. Understanding the physics of failure (e.g., creep, fatigue) and the properties of materials used and the link to the process flow (e.g., yield strength of poly-silicon following HF release) lead to improved design rules to ensure the device will operate reliably in the expected operating environment. A concurrent design of the package is often required, but is not addressed in this chapter.

The chapter is organized into sections dealing with failures of mechanical origin (shock, fatigue, creep), electrical origin (dielectric charging, ESD), and related to environmental effects (radiation, anodic oxidation). For each case, the underlying physics are summarized, followed by several examples, mostly from commercial MEMS, showing the trade-offs required to obtain high reliability.

Different devices will have different predominant failure modes. As the device matures, this mode will change as successive changes in materials, geometry, process flow, packaging, actuation or sensing waveforms, increase the device reliability. Efficiently designing a MEMS device to be reliable while ensuring rapid time to market requires concurrent engineering practices, as presented in [1] by S. Arney. Understanding the physics of failure, which allows accelerated testing to be performed with high confidence, is one key element of such an approach, illustrated in [Fig. 4.1](#).

4.2 Mechanical Failure Modes

In this section, fracture, creep (plastic deformation) and fatigue are discussed as failure modes. We do not address wear here, as it affects very few MEMS devices, since almost all designs go to great lengths to avoid rubbing MEMS parts. Due to the large surface to volume ratio for MEMS devices, and the dominance of surface forces

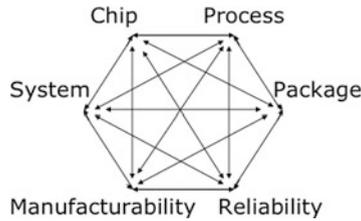


Fig. 4.1 Design for reliability approach, illustrating the interdependence of MEMS product development activities. Reference [1] reproduced by permission of the MRS Bulletin, Copyright 2001 Materials Research Society

over inertial forces at the μm size scale, wear can be a particularly acute problem for MEMS. It has been extensively studied by Sandia National Laboratories, and comprehensively documented in [2]. We do not cover it here as it can be avoided for nearly all types of MEMS by careful design to avoid rubbing parts. Stiction is a related but more widespread failure mode, and has been covered in [Chapter 3](#).

4.2.1 Fracture

Fracture can be an important failure mode for MEMS devices, which, by definition, include micromachined mechanical components. There is the widespread perception outside the MEMS field that silicon MEMS are fragile devices, because silicon is a brittle material. Yet Silicon is a beautiful mechanical material, as long as one designs the device to operate well below the fracture strength, as illustrated in [Fig. 4.2](#) for SOI micromirrors from Alcatel-Lucent USA Inc., which were externally deformed in ways that would never happen in normal use to show the elastic behavior of well-engineered silicon suspensions designed with large safety factors.

An important element distinguishing the mechanical design of MEMS from the mechanical design of macroscopic sensors and actuators is that the properties of thin films can differ significantly from that of bulk samples, because the film thickness is comparable to grain size, or because of process-related damage or modifications.

For this reason, there has been a large body of work to measure the mechanical properties of the thin films used in MEMS: polysilicon, SiN, metals, etc. The properties measured, e.g., Young's modulus, fracture strength, yield strength, fracture toughness, Poisson ratio, have been reported for all main elements and films used in MEMS, for instance in [Chapter 3](#) of the MEMS Handbook (CRC press, 2002) [3] and the MEMSNET website [4].

Figures [4.3](#) and [4.4](#) illustrate schematically the stress-strain curves of brittle and ductile material. In both cases the slope of the linear (elastic) regime is the Young's modulus. But for brittle materials, behavior is elastic up till fracture, while ductile materials exhibit a larger region of plastic deformation.

We shall limit our brief discussion to silicon, whose fracture strength, as for all brittle materials, is distributed following Weibull statistics (see [Chapter 2](#)), as fracture initiation relies on a pre-existing defect or crack. [Figure 4.5](#) shows the influence of surface area of a polysilicon beam on Tensile strength. There are

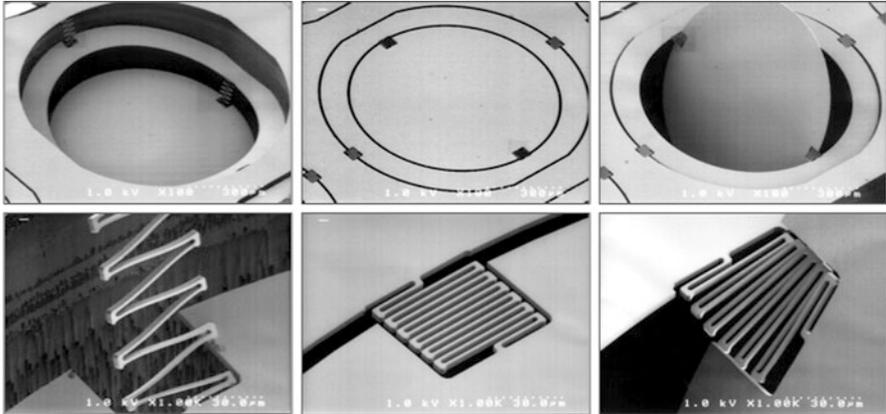


Fig. 4.2 Single crystal silicon micro-mirrors from Alcatel-Lucent showing the impressive mechanical properties of silicon. *Center:* mirror at rest position. The *right* and *left* images were taken after using a probe needle to move the mirrors to positions where the stress in the springs is one order of magnitude larger than what would be encountered in normal (electrostatic actuation) operation, yet because of careful engineering and large safety margins, the springs deform elastically and do not fracture. Reprinted with permission of Alcatel-Lucent USA Inc.

Fig. 4.3 Schematic stress-strain curve for a brittle material. The elastic limit corresponds to the ultimate strength, beyond which the device fractures

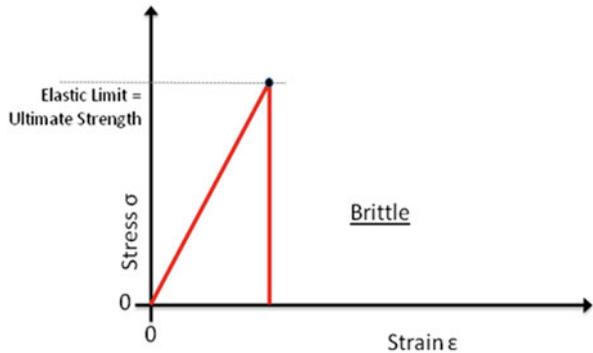
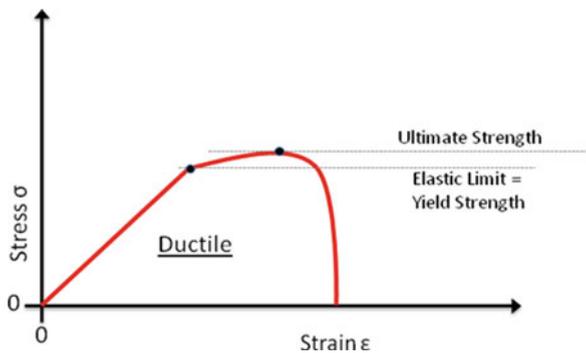


Fig. 4.4 Schematic stress-strain curve for a ductile material. The elastic limit corresponds to the yield strength, after which the material deforms plastically. The ultimate strength is the maximum of the stress-strain curve, and fracture occurs at the breaking strength



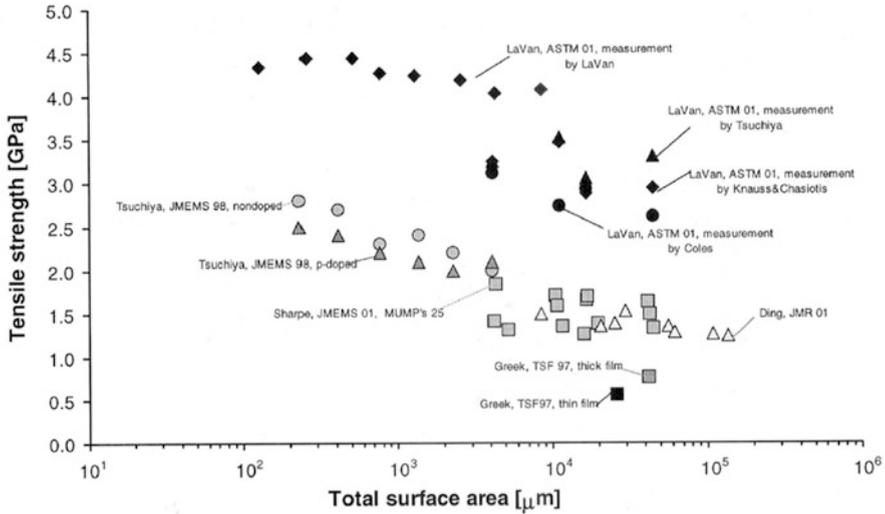


Fig. 4.5 Tensile strength of polysilicon vs. beam area, showing large differences between different fabrication techniques, and also showing higher fracture strengths when smaller or areas are involved, indicating that surface defects rather than volume defects are the initiating points for fracture. Reference [8] reprinted with permission Copyright 2003 IEEE

two important observations: (1) smaller area beam have a higher tensile strength (because there is a smaller area for pre-existing cracks or damage), and (2) the properties of polysilicon differ widely depending on growth conditions, doping, grain size, surface roughness, etc.

To ensure sufficient design margin, it is essential to know the properties of the films one is using, though this is easier for single crystal silicon. Figure 4.6 from [5] plots the Weibull failure probability for each of the five layer of Sandia's SUMMiT VTM process, showing both that within a layer there can be nearly a factor of two range in failure stresses, and that the average failure stress varies by a factor of 2. It is important to use a large safety margin, and obtain test data on the specific polysilicon layer one is using.

Processing play a large role in fracture of brittle materials, as it leads to the formation of initial cracks (for instance, see the example of pitting of polysilicon in Fig. 5.17, leading to stress concentration). It depends also on crystal orientation. The data in Table 4.1 from Chen et al. [6] is for single crystal silicon, showing Weibull reference strength ranging from 1.2 GPa for mechanically ground <100> silicon wafers to 4.6 GPa for the same silicon once etched by DRIE. This variation must be taken into account when designing a MEMS device, to ensure the correct yield strength is used. Simply looking up the generic value for a given material is not sufficient if high reliability is sought after. Very conservative design margins, as was the case for the Alcatel-Lucent micromirrors shown in Fig. 4.2, is another route to ensure devices will not fracture.

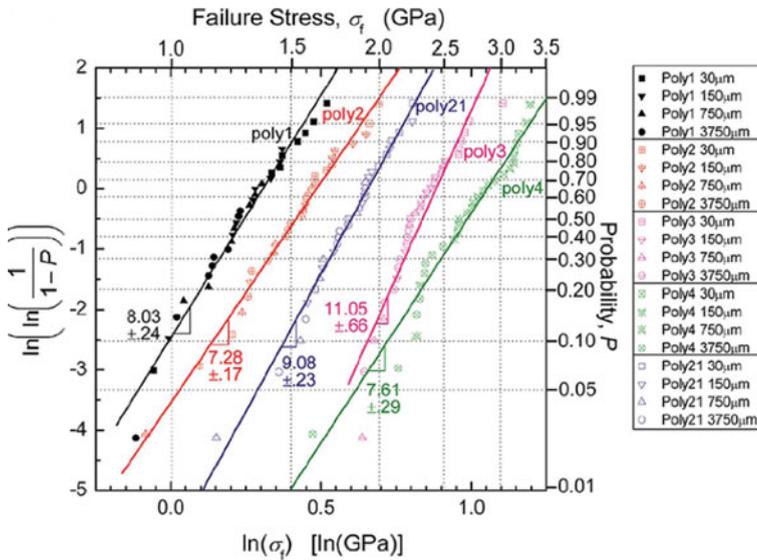


Fig. 4.6 Weibull failure probability plot for each of five SUMMiT V™ layers. Reference [5] reprinted with permission Copyright 2007 IEEE

Table 4.1 Table of strength characteristics of single crystal <100> silicon with different surface conditions

	Mechanically ground (A)	Mechanically ground (B)	KOH-etched silicon (C)	STS DRIE silicon (D)	Chemically polished
Sample size	19	30	25	20	10
Specimen thickness (μm)	500	280	280	230	280
P-P surface roughness (μm)	~3	~1	~0.3	~0.3	~0.1
σ ₀ (GPa)	1.2	2.3	3.4	4.6	>4
Weibull modulus <i>m</i>	2.7	3.4–4.2	7.2–12	3.3	?
Effective <i>R_v</i> for uniaxial volume specimen (mm)	0.383	0.284–0.215	0.12–0.102	0.295	
Effective <i>R_A</i> for uniaxial surface specimen (mm)	1.94	1.266–0.857	0.421–0.487	1.339	

†Note: The volume of the equivalent uniaxial volumetric flaw specimen is $\pi R_v^2 h$, where $h = 300 \mu\text{m}$. The surface area of the equivalent uniaxial surface flaw specimen is $2\pi R_A h$. Adapted from [6] reprinted with permission Copyright 2000 John Wiley and Sons.

Brittle materials exhibit a transition to ductile behavior as the temperature is increased and dislocation motion becomes possible. The data generally reported for MEMS materials is measured at room temperature. For harsh conditions (e.g., a pressure sensor near combustion chamber) where high temperatures are expected, there will be a marked reduction in yield strength, see Fig. 4.7 for polysilicon. Sharpe et al. [7] have shown that Si can exhibit large ductility when heated to over 700°C, as shown the in the stress-strain curve in Fig. 4.8.

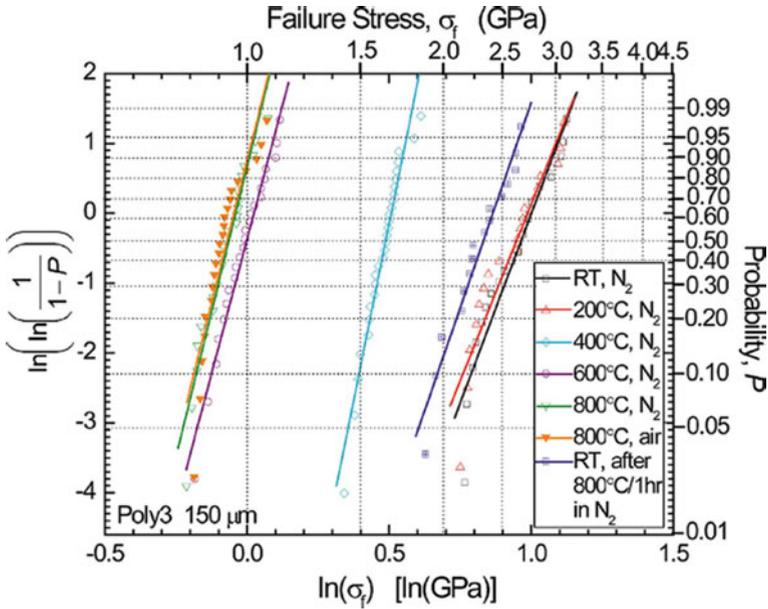


Fig. 4.7 Weibull failure probability plot for one SUMMiT V™ polysilicon layer for several temperatures up to 800°C, showing a strong reduction in failure stress at elevated temperature. Adapted from [5] reprinted with permission Copyright 2007 IEEE

4.2.2 Mechanical Shock Resistance

4.2.2.1 Introduction

Shock is a sudden acceleration. Rather than using SI units of ms^{-2} , shocks are commonly described by the peak acceleration, in units of “g”, where $1 \text{ g} = 9.81 \text{ ms}^{-2}$, the acceleration in Earth’s gravity.

While the normal operating environment for most consumer devices is 1 g, these devices actually need to withstand large shocks in order to have an acceptable lifetime, i.e., in order to be reliable. Devices can be accidentally shocked, for instance being dropped (e.g., a mobile phone falling out of a pocket, a component

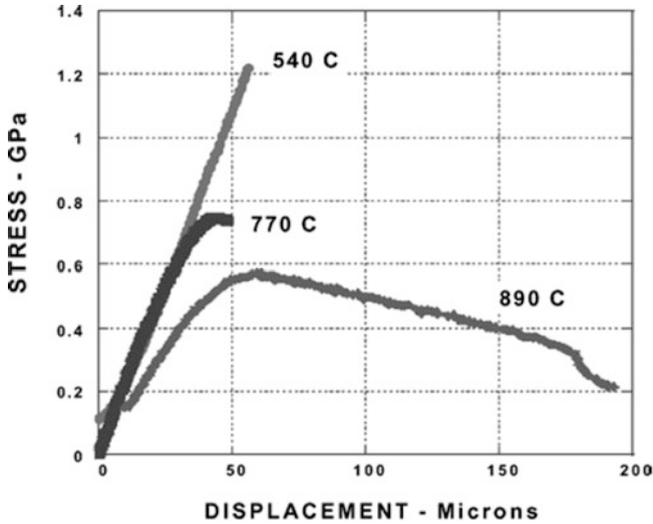


Fig. 4.8 Stress-strain curve for Polysilicon at high temperatures, showing brittle behavior at 540°C, but ductile behavior at 890°C. Reference [7] reprinted with permission Copyright 2003 Springer

falling on the floor during assembly, roughly 500 g for a 1.5 m fall on a hard surface), handled roughly (a mechanical wristwatch worn while playing tennis). Some devices are designed to operate in high shock environments, such as accelerometers in cars which might need to sense shocks of up to 100 g. More extreme examples involve devices on spacecraft, which may need to survive the shock of pyrotechnic bolts used for stage separation (>10,000 g) or of landing (of order 30 g for airbag landing on Mars), and for arming and safeing devices for ammunition fired from a gun or artillery, where shocks of up to 100,000 g are reported.

The failure modes induced by shock include:

- Fracture due to exceeding the yield strength of the material because of a large shock-induced deflection. This is the most obvious failure mode, and will be the main one discussed in the section
- Stiction due to parts coming into contact that would not do so under normal operation. This is termed in-use stiction.
- Delamination, e.g., due to die attach failure, or between layers in a surface micromachined structure
- Particulates being generated or being displaced, leading both to the short circuits between neighboring electrodes, as well as mechanical blockage, e.g., micron-size particles blocking or short-circuiting a comb drive.
- Short-circuits due to parts at different potentials (e.g., comb fingers) coming into contact because of mechanical shock.

From a scaling perspective, MEMS are much more shock tolerant than larger devices for failures due to fracture. A dimensional analysis shows the critical shock scales as $1/L$, where L is a typical dimension (e.g., length). The force on a proof mass due to an acceleration a is simply $F=ma$, and for micron-scale devices, the mass is extremely small. We shall return to this in more detail in [Section 4.2.2.4](#). The situation is slightly more complicated than simply stating the masses are small: in order for an inertial sensor to have a useful sensitivity, it must move by at least a few nm under the applied acceleration, which implies a sufficiently compliant suspension, hence possibly susceptibility to mechanical shock. Similarly MEMS actuators (such as micromirrors) cannot have overly rigid suspension, as this would require an overly large driving force, which would lead to very high drive voltages in the case of electrostatic actuation. Selecting a compliant suspension to increase sensitivity can lead to higher shock susceptibility.

The package of course plays a central role in transmitting shock from the environment to the device. The type of die attach (solder, glue) and the way the package itself is mounted to the shock tester provide different transfer functions generally attenuating the shock but possibly amplifying it at a resonance, and also changing the shock duration. The package and die-attach can fail too (often more likely to fail than MEMS because of larger mass), as discussed further below.

It is important from a product perspective to distinguish between *shock survival* which is the maximum shock that a device can support before complete failure, and *shock resistance* which is the maximum shock it can support without degrading the specifications beyond what is described in the data sheet (for instance the shift of the scale factor or shift of the bias). Shock resistance will correspond to a lower acceleration than shock survival, for instance because shocks could lead to a shift in the die attach and hence to stress on a sensor chip, changing the calibration.

Since MEMS can withstand, when suitably designed and packaged, very large shocks, testing them can be a challenge. Shock levels of up to 6000 g are readily achieved with standard drop-test shock testers and hammers, but larger shocks require specialized equipment, for instance Hopkinson bars (e.g., [9]) and ballistic tests are needed to reach the 10,000–100,000 g levels. One might test devices at shocks higher than the maximum expected operating level in order to have sufficient safety margin and in order to find out at what shock level the devices fail, and how they fail.

The very high shock levels tend only to be of concern for military applications dealing with smart munitions guidance (inertial sensors) or arming and safing. For the later, a safe and arm mechanism is a means to ensure ordnance only explode after being fired: to prevent warhead explosion prior to firing, the munitions are only armed once a longitudinal acceleration of, for instance, 20,000 g is detected, and a radial acceleration due to the spin of the projectile of 10,000 g is sensed. Axun Technologies, Billerica, MA, USA, has developed LIGA MEMS structures that, when assembled, only latch into position following such large accelerations [10].

4.2.2.2 Response to Shocks

Shock Modeled Using the Half-Sine Wave Approximation

Shocks are described by acceleration versus time curve, which for real-world shocks will be a complex shape. As described in [11], shock pulses can be approximated by a series of half-sine pulses. The peak acceleration a_{peak} is often referred to as the shock level, and the duration τ of the half-sine is taken to be the duration of the shock, see Fig. 4.9. Figure 4.10 plots measured acceleration versus time for two shock testing equipment at Sandia national laboratories: a shock table at 500 g, and a Hopkinson bar at 22,000 g.

The higher the peak acceleration, the shorter its duration. Several testing and qualification standards are discussed in Chapter 6 for shock and vibration. Table 4.2 shows the test conditions for mechanical shock testing according to MIL standard 883, showing a clear reduction in pulse duration with increased g level. The same relation can also be seen when comparing Fig. 4.10a, b. Reported durations range from 50 μ s to 6 ms [11].

Fig. 4.9 Half-sine acceleration pulse, the acceleration is zero at time zero, reaches a maximum at time $\tau/2$, and is zero for times larger than τ

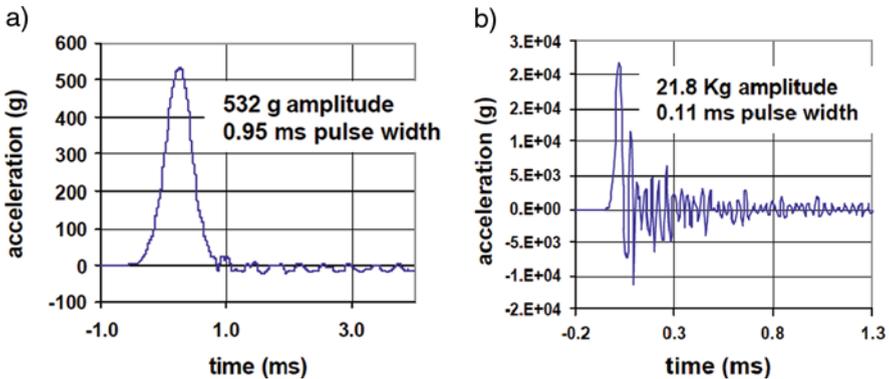
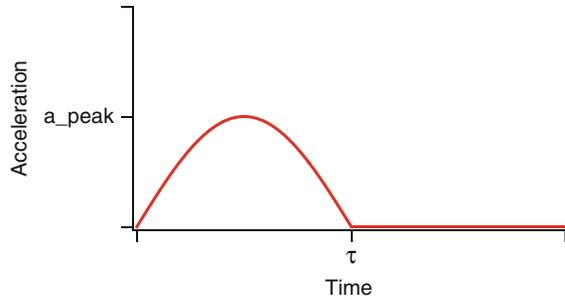


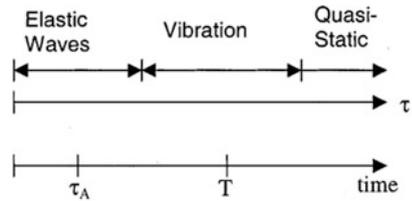
Fig. 4.10 Measured shocks on: (a) a shock table, and (b) using a Hopkinson bar. Reference [9] reprinted with permission Copyright 2000 IEEE

Table 4.2 Test conditions for mechanical shock testing per Mil-Std-883 Method 2002

Test condition	g Level (peak)	Pulse duration (ms)
A	500	1
B	1500	0.5
C	3000	0.3
D	5000	0.3
E	10,000	0.2
F	20,000	0.2
G	30,000	0.12

Srikar and Senturia [11] showed that shock response is governed by the relative magnitude of three time frames: (1) the acoustic transit time $t_{acoustic}$, (2) the time of a vibration T_{vib} (generally much larger than $t_{acoustic}$), and (3) the rise time of the applied shock τ . For $\tau < t_{acoustic}$, the system response is described by superposition of traveling elastic waves. When $\tau \sim T_{vib}$, the system response is best described using normal mode solutions. When $\tau \gg T_{vib}$, the response is quasistatic, as illustrated in Fig. 4.11.

Fig. 4.11 Relevant times scales for shock loaded MEMS, from [11] reprinted with permission Copyright 2002 IEEE



$t_{acoustic}$ is the time taken for an elastic waves to propagate through the microstructure. If we consider a simplified microstructure of length L the speed of sound is c we have $t_{acoustic} = L/c$. The fundamental resonant frequency $\omega_0 = 2\pi / T_{vib}$. For typical silicon MEMS, $t_{acoustic}$ is typically less than $0.1 \mu s$, T_{vib} ranges from $0.1 \mu s$ to $0.1 s$, and τ from $40 \mu s$ to $6 ms$. In view of these timescales, elastic wave propagation does not play a role in the reliability of MEMS in response to mechanical shocks.

Srikar and Senturia [11] define three possible cases depending on the relative magnitudes of T_{vib} and τ .

- $\tau < 0.25 T_{vib}$: *Impulse response*. The MEMS device responds as if it had an initial velocity equal to the integral of the acceleration pulse, i.e., the momentum of the mass is equal to the impulse of the force. The frequency of the device dictates the dynamics, and the exact value of τ does not play a role.
- $0.25 T_{vib} < \tau < 2.5 T_{vib}$: *Resonant response*. The shock can excite a resonance of the device, and the acceleration of the microsystem can exceed the peak applied acceleration, depending on the quality factor of the mode.

- $\tau > 2.5 T_{\text{vib}}$: *Quasistatic response*. The frequency of shock force dictates the dynamics, as the device simply tracks the applied load, given that it can respond much faster than the load varies.

Figure 4.12 illustrates these three different cases for a number of accelerometers, showing that most of the devices are in the quasistatic regime. Understanding the device dynamics is essential for understanding failure modes: if one can predict the maximum displacement for shock along any axis, one can determine whether fracture, stiction, or delamination will be an issue. Particulate motion is more difficult to compute, but avoiding impacts due to shock also avoids particulate generation from those impacts.

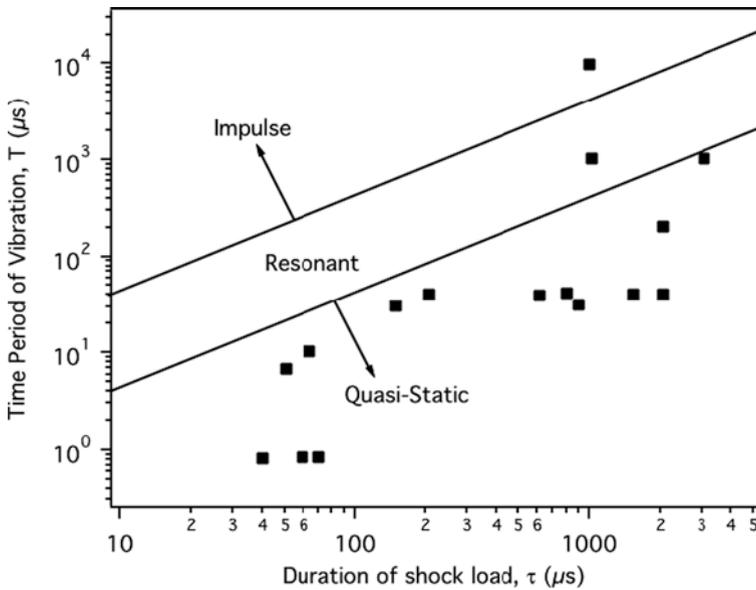


Fig. 4.12 Mechanical response of shock-loaded MEMS (principally accelerometers), from [11] reprinted with permission Copyright 2002 IEEE

For the simple (but instructive) case of a mass-spring-damper system attached to a support, the response of the mass to a half-sine shock pulse to the support can be solved analytically [12]. Consider a mass $mass$, a spring constant k , damping coefficient c_{damper} , with natural resonant frequency $\omega_{\text{res}} = \sqrt{k/mass}$ (see Fig. 4.32 in Section 4.2.3). The Damping constant is $\zeta = \sqrt{c_{\text{damper}}/4m\omega_{\text{res}}}$. Let the half-sine pulse acceleration of the support be given by:

$$\ddot{y}(t) = \begin{cases} a_{\text{peak}} \sin \frac{\pi t}{\tau}; & 0 < t < \tau \\ 0; & t > \tau \end{cases}$$

where a_{peak} is the peak acceleration and τ is the duration of the half-sine pulse. y is the displacement of the support. We assume the mass starts from rest, and solve for

the relative motion of the mass $z(t)=x(t)-y(t)$, which we write as:

$$z(t) = \begin{cases} R(t) & ; & 0 < t < \tau \\ R(t) + R(t - \tau) & ; & t > \tau \end{cases}$$

For compactness of the final equation for $R(t)$, we define the following intermediate variables:

$$a = \pi^2/\tau^2, \quad b = 2\zeta\omega_{\text{res}}, \quad c = \omega_{\text{res}}^2, \quad \omega_d = \omega_{\text{res}}\sqrt{1 - \zeta^2} \quad (\text{only for } \zeta < 1)$$

$$l = \frac{-b}{(a - c)^2 + ab^2}; \quad m = \frac{c - a}{(a - c)^2 + ab^2}; \quad n = \frac{b}{(a - c)^2 + ab^2}; \quad p = \frac{b^2 - c + a}{(a - c)^2 + ab^2}$$

$u(t)$ is the unit step (or Heaviside) function.

The exact solution depends on the value of the damping constant and is hence split into three cases: under-damped ($\zeta < 1$), critically damped ($\zeta = 1$) and over-damped ($\zeta > 1$). One obtains:

1. For an *underdamped* system ($\zeta < 1$), $R(t)$ can be written as:

$$R(t)_{\text{underdamped}} = -a_{\text{peak}} \frac{\pi}{\tau} \left(l \cos\left(\frac{\pi}{\tau}t\right) + \frac{m\tau}{\pi} \sin\left(\frac{\pi}{\tau}t\right) + e^{-\zeta\omega_{\text{res}}t} \left(n \cos(\omega_d t) + \frac{p - n\zeta\omega_{\text{res}}}{\omega_d} \sin(\omega_d t) \right) \right) \cdot u(t) \quad (4.1)$$

2. For a *critically-damped* system ($\zeta = 1$), $R(t)$ can be written as:

$$R(t)_{\text{crit.damped}} = -a_{\text{peak}} \frac{\pi}{\tau} \left(l \cos\left(\frac{\pi}{\tau}t\right) + \frac{m\tau}{\pi} \sin\left(\frac{\pi}{\tau}t\right) + e^{-\omega_{\text{res}}t} (n + (p - n\omega_{\text{res}})t) \right) \cdot u(t) \quad (4.2)$$

3. For an *overdamped* system ($\zeta > 1$), $R(t)$ can be written as:

$$R(t)_{\text{overdamped}} = -a_{\text{peak}} \frac{\pi}{\tau} \left(l \cos\left(\frac{\pi}{\tau}t\right) + \frac{m\tau}{\pi} \sin\left(\frac{\pi}{\tau}t\right) + J e^{-(\zeta - \sqrt{\zeta^2 - 1})\omega_n t} + K e^{-(\zeta + \sqrt{\zeta^2 - 1})\omega_n t} \right) \cdot u(t) \quad (4.3)$$

$$\text{where } J = -\frac{n\omega_{\text{res}}(\zeta - \sqrt{\zeta^2 - 1}) - p}{2\omega_{\text{res}}\sqrt{\zeta^2 - 1}} \quad \text{and } K = \frac{n\omega_{\text{res}}(\zeta + \sqrt{\zeta^2 - 1}) - p}{2\omega_{\text{res}}\sqrt{\zeta^2 - 1}}$$

The above equations allow the maximum mass displacement to be computed vs. shock level and pulse duration for simple systems, and hence provide a first tool to judge whether for instance stiction is possible (do two parts collide?) and determine the kinetic energy of MEMS parts at collision. Figure 4.13 illustrate the displacements for different damping conditions using (4.1) to (4.3).

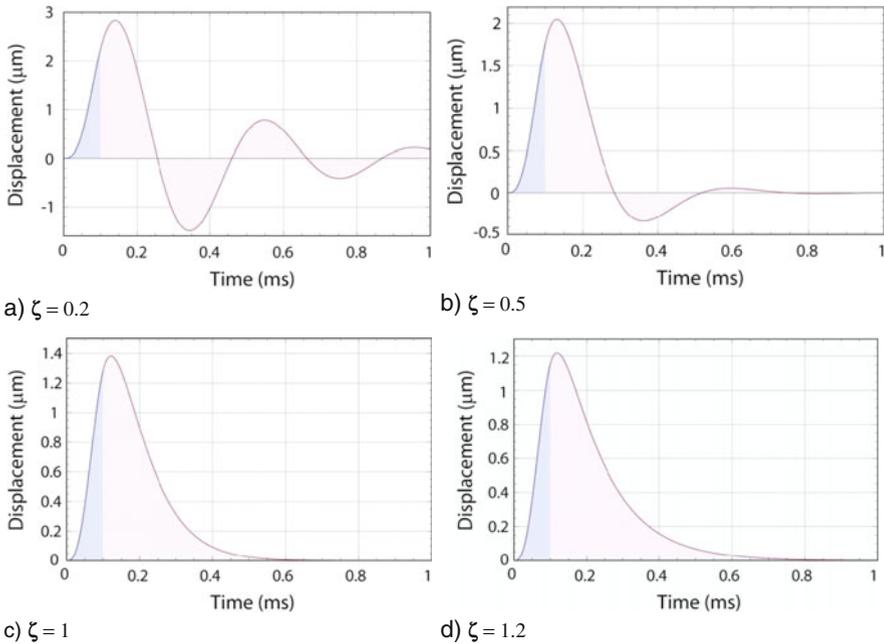


Fig. 4.13 Displacement of mass relative to substrate for an 100 μs long, 100 g peak amplitude shock pulse, for a device with an undamped resonant frequency of 2.5 kHz, for damping coefficient of (a) 0.2, (b) 0.5, (c) 1, (d) 1.2. Displacement was determined using equations (4.1) (a, b), (4.2) (c) and (4.3) (d). The change in shading indicates the end of the shock pulse at $t=100 \mu\text{s}$. Note the larger maximum displacement for devices with less damping

High-g Shock Data on Silicon MEMS

Sandia National Laboratories have published extensively on the shock testing of their micro engine devices, which are complex and rather large surface micromachined polysilicon devices incorporating comb drives, gears, linkages, masses, and springs. In [9], Tanner et al. report a variety of failure modes in response to shocks ranging from 500 to 40,000 g, applying the shocks on all three axes. At 1000 g, no damage was observed. At 4000 g debris (small particulates) on the surface of the die were observed to move slightly. At 10,000 g, 90% of the 19 devices were still operational. The observed failures were due to delamination: the die attach failed, because it had been weakened by the coupling agent used to prevent stiction in the MEMS release step. Only at 20,000 g did the MEMS devices begin to fail due to fracture of polysilicon components. Debris also move at the shock levels and can lead to short-circuits as shown in Fig. 4.14. At 40,000 g the packages failed, see Fig. 4.15. Amazingly several die that were removed from the fractured packages were operational when placed under a probe station. This data shows that even large MEMS devices can be very shock tolerant. This report also indicates that the direction of the shock is a key parameter.

Fig. 4.14 Particulate contamination following 20,000 g shock on a Sandia National laboratories micro engine [9] reprinted with permission Copyright 2000 IEEE

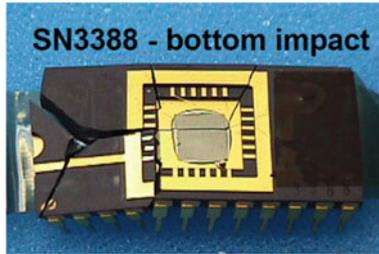
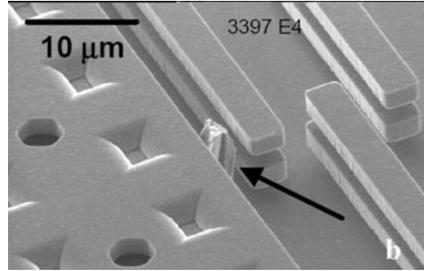


Fig. 4.15 ceramic package following 40,000 g impact. The die attach is visible at the center of the recess. The die was removed and found to still be functioning despite the large amount of debris [9]. Reprinted with permission Copyright 2000 IEEE

The fracture of brittle materials under tension or bending depends on defects initiating the crack, and thus generally follow a Weibull distribution, as reported for instance in [13] and shown in Fig. 4.6. The same statistics should therefore hold for fracture due to applied shocks. Indeed Wagner et al. [14] have investigated the response of epi-polysilicon to mechanical shocks, and reported an excellent fit to Weibull statistics of the measured cumulative failure probability versus peak acceleration, see Fig. 4.16. This data shows the wide range of forces that lead to

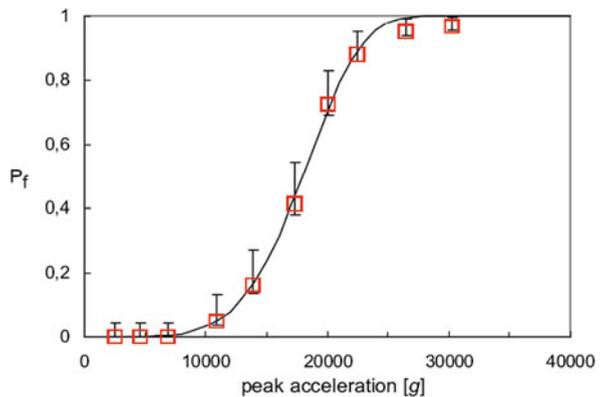


Fig. 4.16 Weibull plot of cumulative failure frequency vs. peak acceleration, for epi-polysilicon MEMS device consisting of a 10 μm thick 1 mm² proof mass suspended by beam of width less than 5.6 μm subjected to tensile load by repeated shocks [14]. Reprinted with permission Copyright 2003 IEEE

fracture for brittle materials, and emphasize the need for suitably large number of samples for testing, or suitably large safety margins to account for the range in fracture strengths of a given brittle material.

4.2.2.3 Increasing Shock Resistance

Recalling the main failures modes related to mechanical shock (fracture, stiction, delamination, particulates, short-circuits), what can be done to increase the shock tolerance of the device?

A commonly implemented solution that addresses fracture and delamination is the use of stoppers to limit the deflection of the moving parts. Figure 4.17 illustrates the use of a stopper to provide 2-D displacement limits for an Analog Devices accelerometer. A stopper is generally made from the same material as the MEMS mass, and is easy to implement, as it requires simply a mask change.

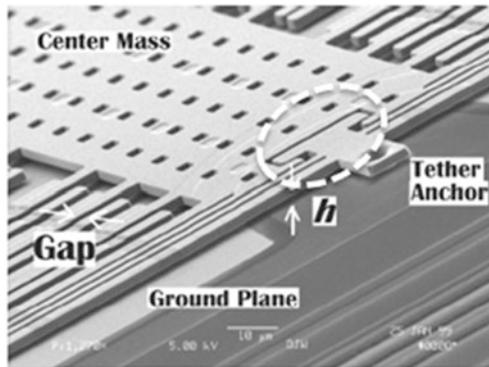


Fig. 4.17 (Left) SEM image of one suspension of the Analog Devices ADXL76 accelerometer. Capacitive sense comb-finger are visible on both sides of the center mass. The stopper is the T-shaped structure in the dashed circle, and limits the in-plane motion of the center mass to avoid contact between fingers of the comb drives. Reference [17]. Reprinted with permission. Copyright 1999 IEEE

By limiting the motion, the stopper avoids fracture by ensuring the stress in the device is below the fracture strength (or the elastic limit). It similarly reduces delamination. The range of motion allowed by the stopper determines the maximum kinetic energy E_c of the mass which was shown in reference [9] to be simply $E_c = mad$, where m is the mass of the moving object, a is the acceleration, and d the gap at rest between stopper and moving mass. To avoid chipping and particulates generation, one should minimize E_c , and hence select as small a gap as is possible given the fabrication technology and required displacement of the device under normal operation. Figure 4.18 is an SEM image of a silicon stopper, showing debris due to impact. The debris are particularly worrisome in the shock environments in view of their mobility.

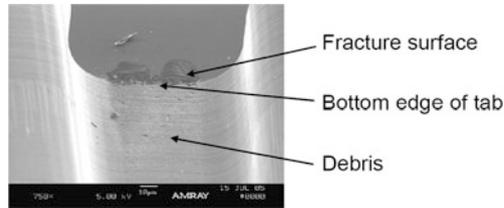


Fig. 4.18 Chipping on silicon stopper following impact, showing fracture surface and accumulated debris [18]. Reprinted with permission Copyright 2008 Society of Photo Optical Instrumentation Engineers

Two limitations of the use of stoppers are stiction and particulate generation. Since hard shock stops can lead to impact, debris and oscillations there has been some modeling of softer stoppers, either using non-linear springs to minimize impact, or adding coatings with low coefficient of restitution such as polymers or metals including gold and copper [15]. More elaborate stoppers based on the techniques used in watchmaking, such as the Incabloc[®] system, can be adapted MEMS and provide much greater safety margin.

Anti-stiction coatings as discussed in [Chapter 3](#), are routinely employed to ensure reliable operation of devices where services may come into contact, such as surface micro-machined accelerometers, of which an Analog Devices model was presented as a case study in [Chapter 2](#). For the Analog Devices accelerometers, the final step before the sensor element is released is the LPCVD (vapor phase) deposition of an organic anti-stiction coating approximately 0.8 nm thick (the process is self-limiting). The coating greatly reduces surface energy, and hence increase the likelihood that parts will not stick should they come into contact (which they should not under normal circumstances), yet is thin enough that it does not affect the mechanics of the devices. Texas instruments also use vapor-phase deposited anti-stiction coatings in its DMD chips, self-assembled monolayers of $\text{CF}_3(\text{CF}_2)_8\text{COOH}$ have been reported [16]. Several anti-stiction coatings are discussed in [Chapter 5](#), illustrating analytical methods for failure analysis.

We now discuss briefly by way of example an accelerometer designed for operation at high shocks (20,000 g according the to the data sheet [19]), the Colibrys SA (Neuchâtel, Switzerland) model HS8030, similar to the MS 8000 shown in [Fig. 4.19](#). Colibrys had developed several generations of capacitive accelerometers, packaged in ceramic multichip modules, with full-scale ranges from 2 to 200 g. In order to ensure high performance the MEMS sensor chip must be attached to the ceramic carrier with a compliant die-attach so as not to apply stress to the sensing chip from mounting the package, or internally due to CTE mismatch between silicon chip and ceramic package as the device needs to operate without bias change over a temperature range of -55°C to $+125^\circ\text{C}$.

Compared to the conventional product, with stoppers designed to limit motion of the proof mass with respect to the MEMS chip, it was necessary, because of the compliant die attach, to also implement stoppers limiting the motion of the MEMS

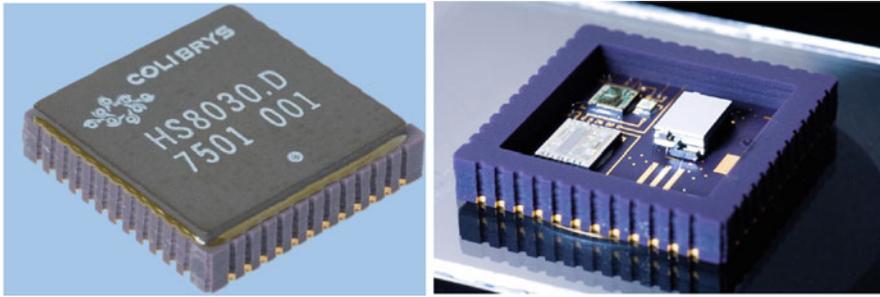


Fig. 4.19 Colibrys HS 8000 series accelerometer. (Left) packaged, (right) MS 8000 without package lid, showing the sensor chip and analog and digital signal conditioning circuits. Courtesy Colibrys SA

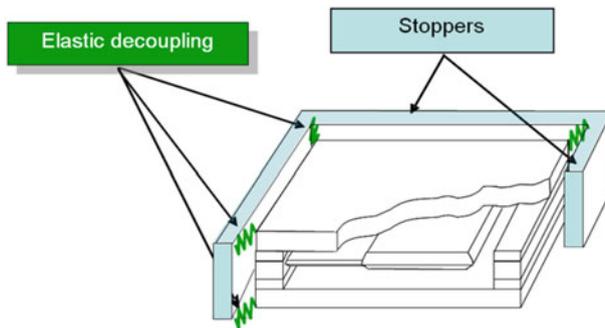


Fig. 4.20 Schematic isometric diagram of the Colibrys HS8000 accelerometer. The proof mass moves vertically in response to acceleration. Stoppers are implemented to limit motion of the chip. Courtesy Colibrys SA (patent pending)

chip itself [20], see Fig. 4.20. The main challenge was not the shock resistance of the sensor, which was shown to survive 40,000 g, but the need to combine Colibrys' existing patented stress isolation technique (required to meet the demanding performance specifications) with stoppers to form a hybrid shock protection solution [21], see Fig. 4.21.

Standard testing equipments are generally not capable to reproduce extreme conditions. Certain harsh conditions can be replicated by a combination of standard tests, for instance combining a hammer test with a centrifuge to simulate a gun hard shock. To test the accelerometers at high g levels (gun hard, 20,000 g, 10 ms), Colibrys used a shock test equipment known as an aerobutt tester at BAE Systems, depicted in Fig. 4.22, which provides much longer duration pulses than the Hopkinson bar data in Fig. 4.10b.

Colibrys tested 124 accelerometers (model HS8030, 30 g full scale) in the Aerobutt tester. The resulting shift in bias had a 3σ variation of under 50 mg, thus demonstrating the effectiveness of the hybrid mounting solution to increase shock resistance of the packaged device to 20,000 g.

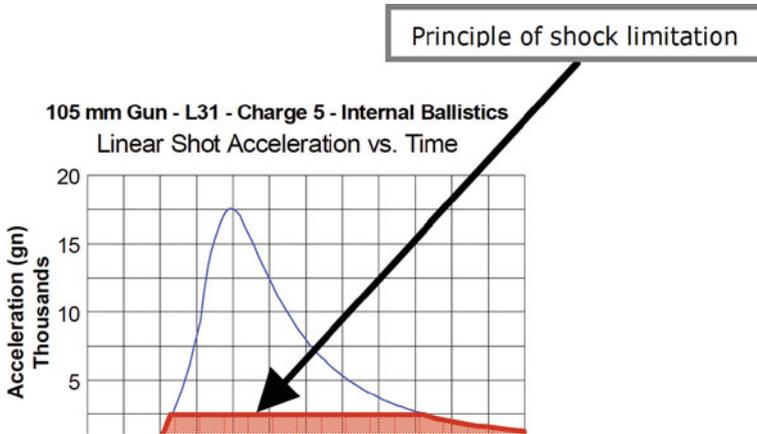
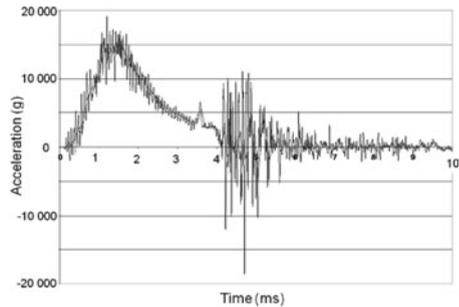


Fig. 4.21 Principle of a shock limitation by a combination of the elastic decoupling and stoppers, to limit the shock at the chip level to 2500 g while the package is accelerated to over 17,000 g. Courtesy Colibrys SA



(a)



(b)

Fig. 4.22 (a) Aerobut shock tester at BAE Systems, from [22] Reprinted with permission copyright 2006 IEEE, (b) measured shock pulse, showing the complexity of real testing compared to the simple half-sine description, Courtesy Colibrys SA

Reliability of Low-G Sensors

There is increasing interest in extremely sensitive inertial sensors capable of operating in the nano-g regime (below 10^{-8} ms^{-2}), for instance for seismic sensing as well as for some in-orbit applications. Because the suspension of such a device must be extremely compliant in order to get at least a few nanometers deflection due to the desired stimulus, the critical acceleration (at which fracture occurs) for these devices is only of order 10 g. So merely handling such a device during fabrication can lead to failures, since picking up an object and putting it down easily generates accelerations of over 20 g.

Such devices generally have springs that are highly compliant only in one direction, and much stiffer in the other two. These devices need suitable stoppers to prevent excessive motion, but the challenge is integrating stoppers on three axes prior to packaging but after release. The solution implemented first at Sandia National Laboratories and then at the EPFL were to package the chip prior to final release, so that the proof mass is either locked in place by silicon oxide, or constrained by stoppers, and hence can be handled safely at all steps of the fabrication and after final release (here release means etching of the sacrificial silicon oxide holding the proof mass in place).

Figure 4.23 shows a schematic cross-section of the final assembly and HF vapor etch, and an optical micrograph of a completed inertial sensor to measure the gravity gradient vector [23]. The wafer is diced by a vapor HF step following front and backside DRIE. The chip is then bonded to a Pyrex chip to provide a bottom stopper. The top stopper is fabricated from overhangs in the top device layer. The 4 cm long MEMS proof mass is only released (another HF vapor etch) after the bottom Pyrex chip is bonded. Despite have a 1 mm long and only 5 μm wide beam suspending a 0.35 g silicon proof mass, the device can safely be handled with no special care thanks to the stoppers integrated in the 0-level package.

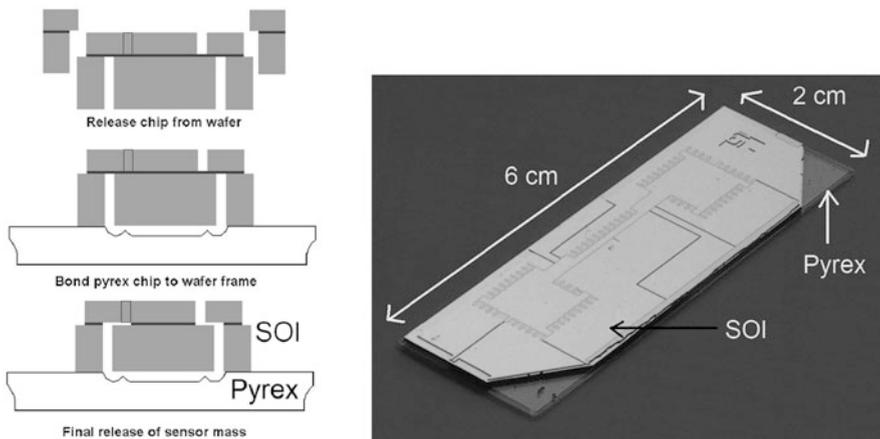


Fig. 4.23 Inertial sensor for measuring the gravity gradient in Earth orbit. The large ($1 \times 4 \text{ cm}^2$ footprint) proof mass is suspended by a very soft spring, and a_{critical} is only 2 g. Yet by suitable constraints in 3 axes prior to final HF release the device can easily be handled. Reference [23] reprinted with permission Copyright 2009 IEEE

4.2.2.4 Simple Model for Critical Acceleration and Case Study on SOI Micro-Mirrors

In this section we will develop a simple model to estimate the maximum acceleration that MEMS devices can sustain, assuming failure occurs due to beam fracture (ignoring stiction, short circuits, delamination, etc). Using basic mechanics

will calculate the strain in suspension beam as a function of acceleration. Knowing the yield strength of typical MEMS materials then allows for a quick determination of the maximum acceleration the system can take. The model developed in this section is more appropriate for static high-G loading in a centrifuge than for shock testing, as it ignores rise time and time period of vibrations, but provides an easy way to compare different geometries. Since we have seen above that many MEMS devices respond quasi-statically to shock (when $T_{\text{vib}} < 0.4 \tau$), the calculation does hold general interest. A similar calculation is given by Tanner et al. in ref [9].

It is recognized that the dynamic stress, and not simply the maximum acceleration as a better criterion for determining dynamic strength [24]. A correct calculation will take into account the mode of the device that is excited, and hence the coupling of energy into this mode as a function of the duration of the shock pulse, see equations (4.1), (4.2), and (4.3) above for different damping conditions. The effect of the package must also be taken into account, in particular for a device falling onto a hard surface. For simplicity we shall ignore these issues and focus on finding order of magnitude values that serve as starting points for a more complete calculation. The “Shock and Vibration Handbook”, in particular Chapter 8 on transient response to step and pulse functions [25] provides a good framework for a more complete solution.

We will show that the model fits well data on some micro mirrors from Alcatel-Lucent USA Inc. but also show how the model fails for other micro mirrors when the model is overly simplistic. We shall give some examples showing how springs can be re-engineered to deal with stress concentration and illustrate how shock on all three axes must be considered to come up with a reliable design.

Cantilever Beam with Mass at the End

Suppose we have a mass m suspended at the end of a cantilever beam, as shown in Fig. 4.24, and that this simple device experiences an acceleration a . A shock is indeed not a constant acceleration, as discussed in the section above, but a static calculation is much simpler and still allows a good approximation of the maximum stress in the beams. We shall ignore the mass of the cantilever.

There are two forces on the mass: the restoring force of the cantilever, and the force due to the acceleration $F = ma$. Rather than deriving all the equations, we

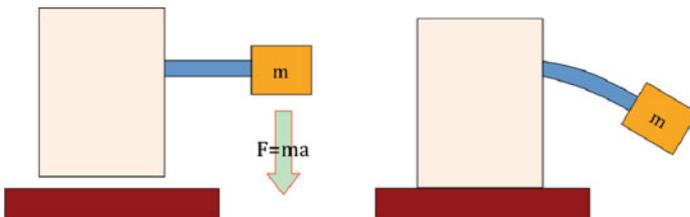


Fig. 4.24 Mass m at the end of a cantilever deforming under the influence of acceleration

will use the formulas that are very conveniently given in the helpful reference book “Roark’s Formulas for Stress and Strain” [26].

The stress σ in a beam is given by $\sigma = \frac{Mz}{I}$ where M is the bending moment of the applied force, z is the distance measured from the neutral plane, and I is the moment of inertia of the section of the beam. For a beam of rectangular cross section, we have:

$$I = \frac{1}{12}t^3w$$

where t is the thickness, and w the width, and the bending is in the direction of the thickness. The maximum stress will be on the top and bottom of the beam, at $z = \pm t/2$, see Fig. 4.25.

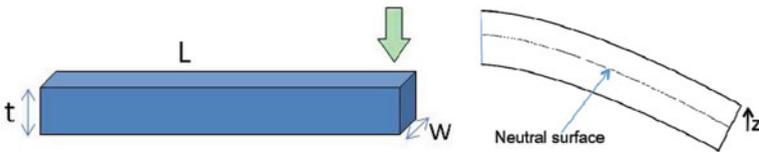


Fig. 4.25 Geometry of the cantilever, with the load applied as indicated by the *arrows*, so the neutral plane is located at $t/2$

The maximum moment for a beam of length L is:

$$M_{\max} = -FL$$

$$= -mal$$

The maximum stress is then:

$$\sigma_{\max} = \frac{M}{I} \frac{t}{2}$$

$$= -maL \frac{6}{wt^2}$$

Neglecting fatigue, creep and stiction, we expect failure when σ_{\max} is equal to the yield strength (keeping in mind that fracture of brittle materials follows a Weibull distribution and therefore a significant safety margin is needed, see the section on fracture earlier in this chapter). One can then determine the acceleration a_{critical} when the beam fractures:

$$a_{\text{critical}} = \sigma_{\text{yield}} \frac{wt^2}{6 mL} \tag{4.4}$$

From (4.4), it follows that to be able to withstand higher accelerations, the beam must be made shorter, thicker and wider. In view of the t^2 scaling, increasing the thickness of the cantilever can be the most effective technique.

For polysilicon the yield strength ranges from approximately 1 to 3 GPa, and is roughly 5 to 8 GPa for single crystal silicon [27]. As an example, 1 μg mass (e.g., a

silicon cube $80\ \mu\text{m}$ on a side) at the end of a $400\ \mu\text{m}$ long polysilicon beam, $2\ \mu\text{m}$ wide and $2\ \mu\text{m}$ thick, has a maximum acceleration $a_{\text{critical}} = 10,000\ \text{m/s}^2 = 1000\ \text{g}$.

Or, more realistic as comparable to some commercially available bulk micromachined accelerometers, a silicon proof mass, $1 \times 1\ \text{mm}^2 \times 0.5\ \text{mm}$ thick, suspended from $50\ \mu\text{m}$ long, $50\ \mu\text{m}$ wide $20\ \mu\text{m}$ thick suspension, has a maximum acceleration $a_{\text{critical}} = 250,000\ \text{m/s}^2 = 25,000\ \text{g}$. In practice, such a system would have stoppers to limit the motion and hence the kinetic energy, and the mass would hit those hard stops.

Note that while the deflection Δh at the end of the beam depends on the Young's modulus E as:

$$\Delta h = \frac{maL^3}{3EI}$$

the critical acceleration does not depend directly on E , but only on yield strength. a_{crit} and E are nevertheless indirectly related, via the geometry of the device, since the suspension dimensions (i.e., choice of beam geometry to achieve a given stiffness) is strongly dependent on the material's Young's modulus.

Doubly Clamped Cantilever with Mass at Center

Most MEMS designed to sustain reasonable shock have a symmetrical design and spread load over at least two anchors, leading to an s-shaped beam deflection. So we shall redo the computation above, but now for a mass suspended by 2 anchors. The motivation is to compute the magnitude of the maximum vertical load (hence acceleration) that micromirrors such as the one in Figs. 4.26 and 4.27 can handle. The mirror in Fig. 4.26 is suspended by two poly-silicon springs from a gimbal, which is suspended by two poly-silicon springs from the frame.

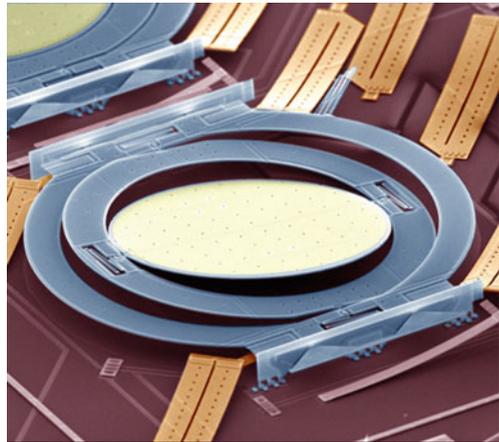


Fig. 4.26 Polysilicon micromirror from Alcatel-Lucent. Two $2\ \mu\text{m}$ wide serpentine springs attach the mirror to the gimbal, which is attached by two more $2\ \mu\text{m}$ wide serpentine springs to the frame (outermost ring). Reprinted with permission of Alcatel-Lucent USA Inc.

Fig. 4.27 FEM response to a vertical shock, showing the mirror and the gimbal rising up. Displacement is not to scale to emphasize motion. Reprinted with permission of Alcatel-Lucent USA Inc.

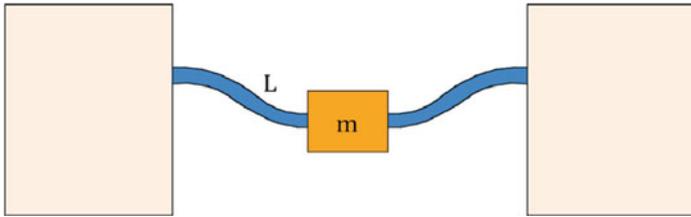
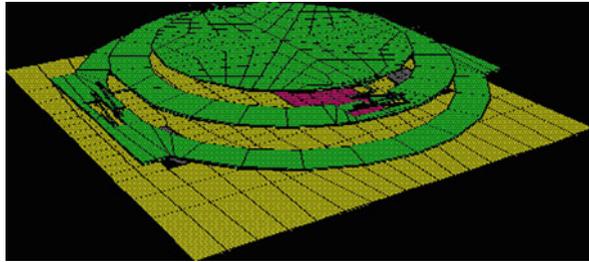


Fig. 4.28 Schematic cross-section of a symmetrically suspended micromirror

The simplified model of the mirror is shown in Fig. 4.28, where two beams of length L , thickness t , and width w are bent as the acceleration moves the mirror vertically.

The maximum moment for each of the two beams of length L for this doubly-clamped configuration, neglecting any bending of the mass, is:

$$M_{\max} = -\frac{F}{4}L$$

$$= -\frac{maL}{4}$$

The maximum stress is:

$$\sigma_{\max} = \frac{M_{\max}}{I} \frac{t}{2}$$

$$= -\frac{3}{2} \frac{maL}{wt^2}$$

So the critical acceleration for fracture for the 2-spring device in Fig. 4.28 is:

$$a_{\text{critical}}^{2\text{-springs}} = -\frac{2}{3} \frac{wt^2}{mL} \sigma_{\text{critical}}$$

For a device like the one in Fig. 4.26 with a gimbal (so 4 springs in all: 2 from frame to gimbal, 2 from gimbal to mirror), the maximum sustainable acceleration is roughly the same, assuming the gimbal does not deform, as the two springs

supporting the gimbal also bend, leading to twice the displacement, and hence the same maximum strain in each spring as for without the gimbal.

$$a_{\text{critical}}^{4\text{-springs, gimbale}} = -\frac{2}{3} \frac{wt^2}{mL} \sigma_{\text{critical}} \quad (4.5)$$

We shall now apply equation (4.5) to three micromirrors, one made from polysilicon, and two from SOI. Two of these designs have folded (serpentine) springs. For these folded beams, we shall use in the calculations for L the length of one segment. This leads to a slight overestimate of maximum sustainable shock, but is more accurate than using the full unfolded length of the spring. Finite Element Modeling taking into account the exact shape of the spring would lead to a more accurate number. For the micromirror in Fig. 4.26, for which the polysilicon mirror is $2.6 \mu\text{m}$ thick, $250 \mu\text{m}$ radius, and hence a mass of $1 \mu\text{g}$, with beams with $t = 2.6 \mu\text{m}$, $w = 2.0 \mu\text{m}$, arm length of each serpentine beam segment of $50 \mu\text{m}$, and a total length of $400 \mu\text{m}$, we obtain $a_{\text{critical}} = 1.8 \times 10^5 \text{ m/s}^2 = 18,000 \text{ g}$.

These micro mirrors were shocked tested in a specially built setup, which allowed shock testing up to 25,000 g. For shocks in the vertical (pushing the mirror “up”), failures were seen starting near 5,000 g with many mirrors surviving higher shock levels [136]. In view of the approximations in the model above and the variations in fracture strength for brittle material, there is reasonable agreement between the experimental data on shock susceptibility and the prediction.

Now consider the SOI mirror from Alcatel-Lucent in Fig. 4.29, based on $100 \mu\text{m}$ long, $3 \mu\text{m}$ thick and $1.2 \mu\text{m}$ wide torsion beams [135]. The mirror mass is $4 \mu\text{g}$, and applying equation (4.5) leads to a predicted $a_{\text{critical}} = 1.1 \times 10^5 \text{ ms}^{-2} = 11,000 \text{ g}$.

The SOI mirror from Alcatel-Lucent in Fig. 4.30 is a design that is very tolerant to residual stress and to vertical forces during release because it is based on serpentine beams. The folded suspension beams segments are $60 \mu\text{m}$ long, $1.1 \mu\text{m}$ wide

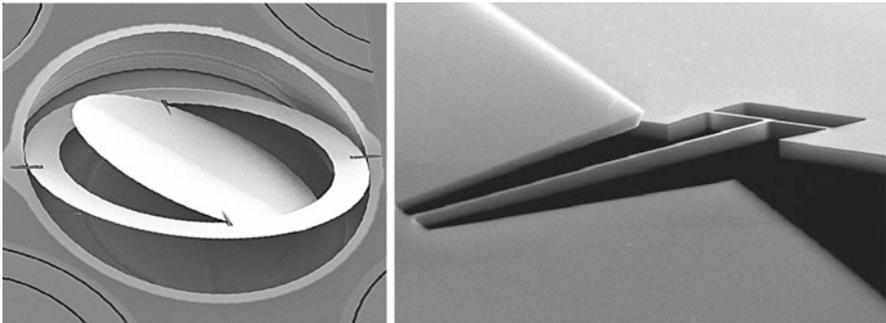


Fig. 4.29 $875 \mu\text{m}$ diameter SOI mirror, suspended by $1.2 \mu\text{m}$ wide, $3 \mu\text{m}$ thick torsion beams [135]. Reprinted with permission Copyright 2003 IEEE

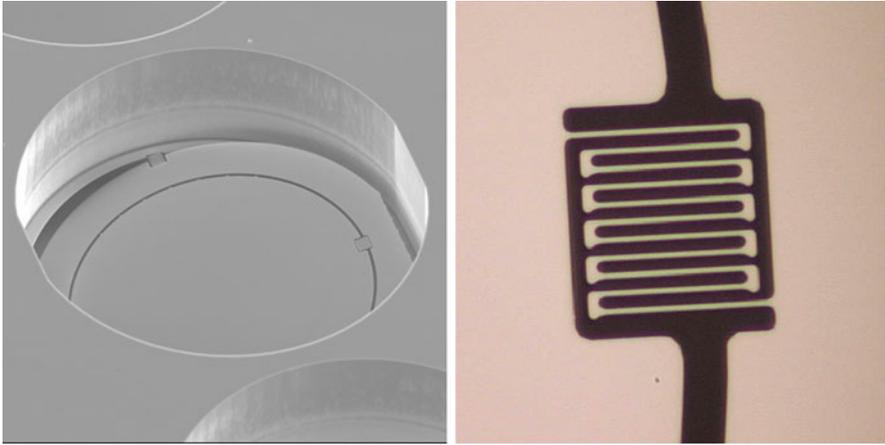


Fig. 4.30 (Left) 875 μm diameter SOI mirror from Alcatel-Lucent suspended by 1.1 μm wide, 5 μm thick serpentine beams (operating in torsion). Reference [28] reprinted with permission Copyright 2003 IEEE. (Right) Optical micrograph of the silicon suspension spring (high-shock resistance design). Reprinted with permission of Alcatel-Lucent USA Inc.

and 5 μm thick [28]. The mirror mass is 7 μg . Applying equation (4.5) leads to a predicted $a_{\text{critical}} = 2.6 \times 10^5 = 26,000 \text{ g}$.

When these SOI mirrors were shocked tested some of them failed by spring fracture at only 200 g, though those in Fig. 4.30 only fail at shocks well above 1000 g. To explain this, and to explain how the design was improved in order to exceed the thousand g shock levels required for Telcordia Generic Requirements for Single-Mode Fiber Optic Switches (GR-1073, discussed in more detail in Chapter 6), one must leave our simplistic static calculation and take the details of actual geometry into account, namely including:

- Stress concentration
- Surfaces coming into contact, stiction (i.e., failure may not be due to fracture)
- Ringing and different modes, and hence the duration of the shock pulse
- Shocks coming from arbitrary directions (the model above only considered the vertical piston mode)

Figure 4.31 shows the evolution of the serpentine spring design that allowed progressing from failures occurring at 200 g due to stress concentration at sharp corners to a design that withstands shocks of greater than 1000 g on all three axes. 73 mirrors with the final design were shocked tested repeatedly on all three axes and no failures were observed. It is worth emphasizing that failures need not be due to fracture suspension beams but can also be due to stiction of parts that are normally would not come into contact or to delamination. With careful engineering, even large MEMS structures can be made highly shock resistant.

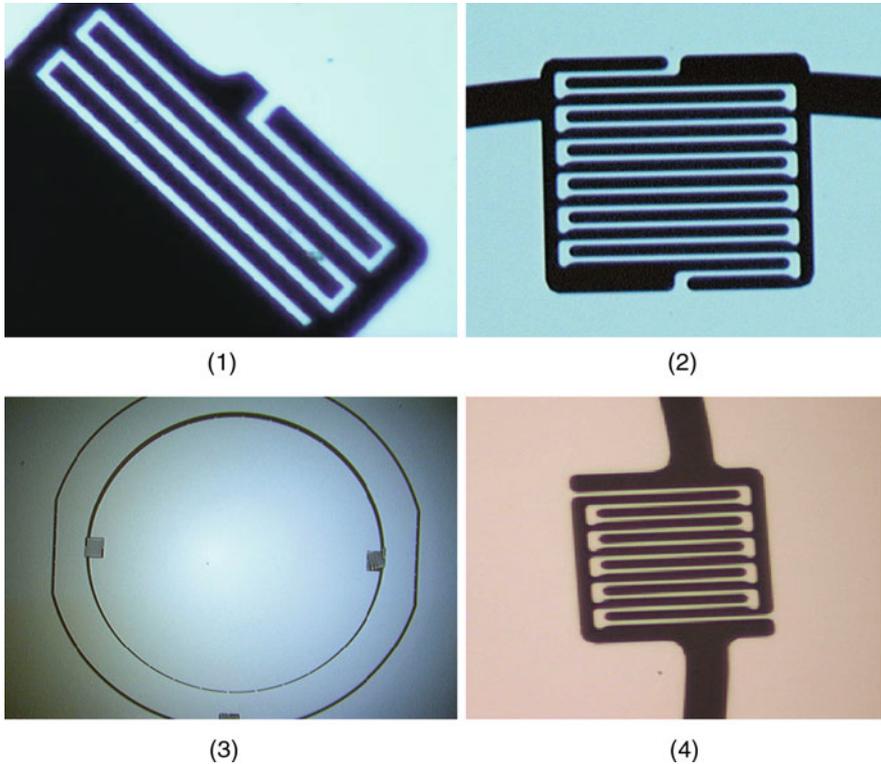


Fig. 4.31 Changes in spring design on Lucent Technologies SOI micromirrors to go from 200 g to $\gg 1000$ g shock survivability. Reprinted with permission of Alcatel-Lucent USA Inc. 1. First generation of SOI mirrors failed at 200 g. Failure mode: cracking of the spring at the 90° corner. The image shows the fractured beam after vertical shock. 2. So the sharp corner where stress was concentrated were eliminated, see image above. Failure then occurred at 400 g, *not by fracture*, but by stiction from lateral motion of the mirror. 3. Mirror with spring as in (2) after lateral shock: the mirror “slid” under the gimbal, and stuck. Failure mode is stiction. 4. “Rotated” serpentine beam providing enhanced lateral stiffness for the same torsional stiffness as in (3), but allowing the mirror to survive repeated shocks in all axes for shock levels greater than 1000 g, 0.5 ms half-sine

4.2.2.5 Conclusions on Shock

We summarize some general conclusions on making MEMS more shock resistant.

- By virtue of the small mass of MEMS devices, shocks of a few g are easy to accommodate.
- Shocks of up to 1000 g can readily be dealt with by spring design (avoiding stress concentration, symmetrical designs, . . .)
- Shock of 10,000 g require more careful design (of MEMS but also of attachment and package)
- No fatigue has been observed from shocks.

- “Stoppers” are a widely used technique to mechanically limit motion of beams. This approach is very effective as it minimizes displacement and kinetic energy, but stiction can be an issue.
- One must design the suspension to uniformly spread loads, for all 3 axis, and testing must be done on all three axes.
- To avoid current spikes that could damage the device, one must ensure that surfaces which might come into contact are at the same electrical potential
- Cleanliness is essential to avoid any particulates that could move and the two short-circuits or mechanical blockage.
- The die attach material must be carefully chosen, balancing strength with induced stress.
- Use the package to dissipate the shock load.
- Keep in mind that fracture is not the only failure mode (stiction can play a large role).

4.2.3 *Vibration*

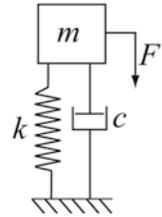
In this section, we describe a general methodology to determine a lower limit on vibration level expected for failure as a function of frequency.¹ The objective is to estimate the vibration acceleration needed to bring parts into contact or to reach fracture stress, prior to vibration testing, in order to avoid surprises and to serve as a tool for the designer. Vibration testing is discussed in [Chapter 6](#), from a qualification perspective and then presenting an example of vibration testing of a polysilicon MEMS micro-engines from Sandia.

The procedure to determine a lower limit on maximum safe vibration levels involves three steps.

1. List the possible failure modes due to vibration: i.e., list the displacement in 3 axes that could lead to stiction or short circuit or to fracture. For instance, for a SOI micromirror suspended 2 μm over the handle layer, with a 10 μm clearance around the periphery, a 2 μm motion in the -z axis could lead to stiction, and a 10 μm motion in the xy plane could lead to stiction.
2. Measure device response vs. frequency (in plane & out of plane) to obtain resonant frequencies and quality factor (damping). This will allow the dynamics of the device to be determined.
3. Use method below to generate plot of safe lower limit of vibration below which contact will not occur, and therefore below which failure is not expected. This plot is merely a lower limit, since contact does not automatically lead to stiction.

¹ This procedure was developed by Subramanian Sundaram at the EPFL.

Fig. 4.32 Forced vibration model, with fixed support. The MEMS mass is driven directly (e.g., electrostatically actuated mirror)



For the purpose of shock and vibration characterization, most MEMS devices in air or in vacuum can be accurately modeled as a single degree of freedom mass spring system, as in Fig. 4.32, with mass m , spring constant k , damping constant c , driving force F . The displacement x can be written as a function of frequency ω and first resonance mode ω_{res} as:

$$x(\omega) = \frac{x(\omega = 0)}{\sqrt{\left(1 - \left(\frac{\omega}{\omega_{res}}\right)^2\right)^2 + \left(2\xi \frac{\omega}{\omega_{res}}\right)^2}} \tag{4.6}$$

where $\xi = \frac{c}{4m\omega_{res}}$.

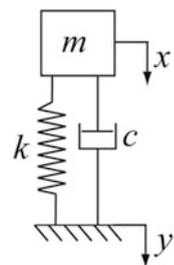
Now consider instead Fig. 4.33, which shows a model for the case of a mass excited at the base (i.e., using a shaker). The parameter of interest for vibration testing is the motion x of the mass relative to the motion y base can be written as:

$$z(t) = x(t) - y(t)$$

Using the coordinate system depicted in Fig. 4.1 and summing all the forces that act on the mass, the equation of motion for the system can be written as

$$m\ddot{x} + c\dot{x} + kx = c\dot{y} + ky \tag{4.7}$$

Fig. 4.33 Support vibration model, where the support is being vibrated. The MEMS mass motion $x(t)$ is due the support motion $y(t)$. The motion of interest is the relative motion $x-y$

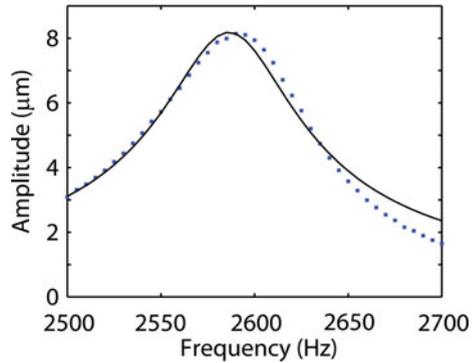


Solving the equation for the steady state and rearranging the terms, we can write a displacement function as a ratio of the amplitudes of the motion of the mass and the excitation base in the form:

$$\frac{z}{y} = \frac{\left(\frac{\omega}{\omega_{res}}\right)^2}{\sqrt{\left(1 - \left(\frac{\omega}{\omega_{res}}\right)^2\right)^2 + \left(2\xi\frac{\omega}{\omega_{res}}\right)^2}} \tag{4.8}$$

To proceed, one needs ω_{res} , $\xi=1/(2Q)$ and $x(\omega=0)$. This must be obtained experimentally, for instance from Laser Doppler vibrometer data or from stroboscopic video microscopy. Figure 4.34 is an example of amplitude vs. frequency for an in-plane mode of an SOI electrostatic MEMS device taken with a Veeco Wyko NT1100 using stroboscopic video microscopy. From the fit to (4.6), ω_{res} , Q and $x(\omega=0)$ are extracted.

Fig. 4.34 Frequency response of an MEMS device (data points) and fit to (4.6), giving $\xi=0.0135$, and $\omega_{res}=2.59$ kHz

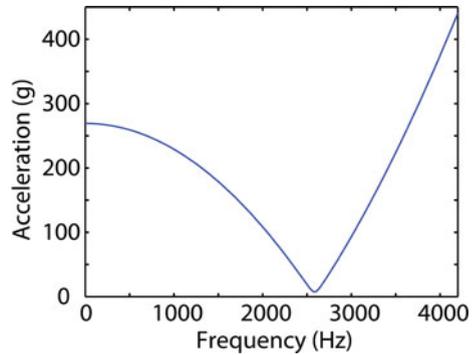


Using (4.8) one can then determine the input acceleration at the shaker necessary to produce failure as a function of the excitation frequency, having previously determined the displacement that could lead to stiction or fracture. We shall call this the critical acceleration $a_{crit}(f)$, below which vibration cannot lead to failure (for the given mechanical mode). It is possible that the device operates reliably above acceleration $a_{crit}(f)$, since contact between two parts does not necessarily imply stiction or fracture.

$$|a_{crit}| = y\omega^2 = z\omega_n^2 \sqrt{\left(1 - \left(\frac{\omega}{\omega_n}\right)^2\right)^2 + \left(2\xi\frac{\omega}{\omega_n}\right)^2}$$

An example is shown in Fig. 4.35; the input acceleration has a minimum for an excitation frequency equal to the resonant frequency of the device. For this example, the data from Fig. 4.34 was used, and failure was assumed to occur at a displacement

Fig. 4.35 Computed minimum critical acceleration a_{crit} vs. frequency to obtain $10\ \mu\text{m}$ motion, using the parameters extracted from Fig. 4.34. Vibration levels below the curve will not lead to failure



of $10\ \mu\text{m}$. One obtains a critical acceleration of $7.6\ \text{g}$ at resonance for that in-plane resonant frequency.

This procedure is to be repeated for the different vibration-induced possible contacting surface for a device. Generally, only a two or three failure modes need to be considered as one will dominate for each axis. The use of a Laser Doppler vibrometer and stroboscopic video microscopy is discussed in more detail in Sections 5.5 and 6.3.5.

This approach assumes the MEMS device is unpowered during the vibration. If the device is being actuated while being vibrated, the critical acceleration for failure could be greatly reduced for instance because snap-in could occur, and because of electrostatic spring softening.

4.2.4 Creep

4.2.4.1 Introduction

Creep is the time-dependent increase in strain in a solid at constant temperature and stress, i.e., creep is plastic deformation under applied strain. By definition, creep occurs only in ductile materials, so what follows applies to metal thin films, not to silicon, (except at temperatures above 600°C). There is one exception for MEMS: polysilicon which has been galvanically corroded by HF during release has shown creep [29, 30]; this can be avoided by proper etch procedure, as described in Section 4.4.2 and references therein.

Creep was introduced in Chapter 2 (Section 2.5.1), in the context of the case study of plastic deformation of the TI DM mirrors, and the deformation mechanism map of homologous temperature versus normalized shear stress was introduced. Creep is generally a consequence of dislocation motion, and depends on: Temperature, Stress (intrinsic, thermal, or applied) and Time. It is expressed as $d\epsilon/dt$, where ϵ is the strain and t the time. Temperature plays a key role in atomic diffusion and dislocation mobility. The Homologous temperature (ratio of operating

to melting temperature T_{melt}) provides a good guide as to dislocation mobility. The following three temperature regimes are often used:

$0 < T < 0.3 T_{\text{melt}}$: no creep observed

$0.3 T_{\text{melt}} < T < 0.9 T_{\text{melt}}$: dislocation motion leading to creep

$0.9 T_{\text{melt}} < T < T_{\text{melt}}$: diffusion creep (nearly liquid flow)

A commonly used criterion is that creep is appreciable (relatively fast deformation, accelerating with time) for temperatures larger than $0.5 T_{\text{melt}}$, and is slower (and with a rate that is decreasing) below this threshold. The threshold of $0.5 T_{\text{melt}}$ serves merely as a guide to give an order of magnitude of what a suitable operating temperature will be. The value of $0.5 T_{\text{melt}}$ is given for a few materials in Table 4.3. Due to their low melting temperature, solders generally exhibit creep near room temperature. One should also note that the device temperature can be significantly higher than ambient, for instance in RF MEMS switches carrying a few 100 mW of power the membrane can reach 200°C [31], and in projector applications spatial light modulators near the incandescent light source can exceed 100°C if no precautions are taken.

Table 4.3 Temperature at which $T_{\text{homologous}}=0.5$ for several materials

Material	$T_c=0.5 T_M$ (in Kelvin)
60% Sn – 40% Pb (solder)	–45°C
Pb	27°C
Al and Al alloys	190°C
Ti	700°C
Si (brittle)	570°C
W	1600°C

4.2.4.2 Reducing Creep in MEMS

Increasing the creep resistance of a MEMS device can follow 3 paths: (1) reduce the operating temperature), (2) reduce the applied stress levels, (3) change the material. We shall see in the following example from TI that all three approaches were needed to reach the desired operating life.

A complete change in material may not be possible from a process point of view, but often only a small change in film composition is needed. The purpose of a material composition change is to block dislocation motion, which can be achieved by pinning of dislocations by solute atoms, impeding dislocation motion by short-range order, and increasing dislocation density to tangle them (work hardening). Defects and grain boundaries can trap or pin dislocations. This is done most easily by introducing tiny particles of a second phase into a crystal lattice, for instance Fe_3C in steel, or Al_2Cu in Al.

Creep is currently an important failure mode for RF MEMS switches, and was initially an important failure mode for Texas Instruments' DMD micromirrors. TI

refers to creep as “hinge memory”, because creep leads mirrors that have been tilted for extended periods in one direction more than the other to exhibit a small residual tilt. The residual tilt increase the required drive voltage to tilt in the “less-used” direction, eventually leading to pixel failure when the voltage margin is used up.

Factors that TI identified as contributing to hinge memory were temperature and duty cycle [32]. By replacing the original Al torsion bars by another material (an aluminum alloy with increased creep resistance or that allowed for lower maximum stress), they were able to obtain a fivefold increase in lifetime. To obtain a further factor of 5 improvement in lifetime, TI did not reduce the creep rate (i.e., did not change the peak stress or the spring material), but implemented a different electrical waveform that allowed reliable operation with larger residual tilt. Finally, to reach the reliability level need for a consumer product, they implemented a thermal management (a system-level fix as well as a packaging-level fix) to keep the mirror array temperature below 45°C under normal conditions, operating only 7–10°C above ambient temperature. With these three changes, they predict array lifetime in excess of 100,000 h for failure due to hinge memory, see Fig. 4.36 [32].

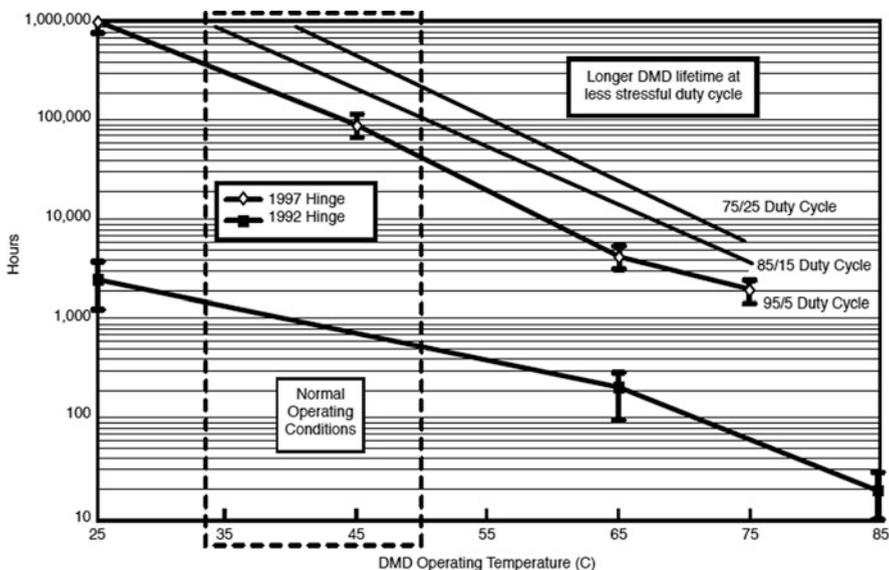


Fig. 4.36 DMD lifetime estimate for failures from hinge memory (creep), for two hinge generations (1992, 1997) as a function of temperature, and duty cycle, with 95% being an accelerated test condition. From [32] reprinted with permission Copyright 1998 IEEE

Another example of reducing creep in MEMS comes from IMEC, regarding the choice of metal for membranes in RF switches [33, 31]. They compared 5 different Al alloys for creep resistance ($\text{Al}_{98.3}\text{Cu}_{1.7}$, $\text{Al}_{99.7}\text{V}_{0.2}\text{Pd}_{0.1}$, $\text{Al}_{99.6}\text{Cu}_{0.4}$, $\text{Al}_{99.6}\text{Cu}_{0.4}$, $\text{Al}_{93.5}\text{Cu}_{4.4}\text{Mg}_{1.5}\text{Mn}_{0.6}$), and correlated the microstructure, determined from SEM and TEM images (principally precipitate size and distribution, as well

as direct imaging of pinned dislocation), with the creep rate. They observed much lower creep in films with small (nm size) and highly dense particles, which were most effective at pinning dislocation and hence slowing creep. Up to 110°C, they showed that dislocation glide limited by obstacles (the precipitates) is the dominant creep mechanism.

The IMEC groups also showed that annealing and quenching can change the grain interior by changes the precipitate size and dispersion, thus allowing fine tuning of creep resistance by a hardening process, as used in the processing of many metals for macroscopic use.

The choice of film depends on the desired resistivity (slightly higher for the Al alloys), stress as deposited (higher for the alloys), thermal budget for annealing, material availability, and acceptable creep rate.

4.2.4.3 Metal Films on Silicon MEMS

Silicon is in principle immune to creep, as a brittle material. For optical MEMS devices, or for improved electrical conduction, silicon is often coated with a thin metal film. It is essential for long-term creep-resistance to ensure there is no metal on the suspension element or elements under high stress, as the metal can creep, thus applying stress to the underlying silicon, making it look like the silicon MEMS is creeping. One must distinguish between metal on silicon beams (where it is generally only needed for the case of thermal actuators) and metal on optical reflectors, where the metal is always needed.

A silicon beam a few μm thick that is beam covered with few hundred nm of Al can lead to appreciable creep (or hinge memory). By way of example, an early generation of Lucent Technologies SOI micromirrors had the 5 μm thick silicon suspension beams coated with approximately 100 nm of Al. Following accelerated testing (high applied stress) for 5 days at 85°C, a residual tilt of 0.1° was observed. By contrast, after 2 months of accelerated testing, micromirrors whose beams did not have the metal coating showed no residual tilt.

Reflective coatings on micromirrors cannot be eliminated, as they are required for the desired optical performance. This type of micromirror is presented in [Section 5.3.1](#), with a discussion of curvature. A big challenge these mirrors pose is during annealing (e.g., during packaging, die attach, wirebonding) when the mirror deforms due to the CTE mismatch, but when the metal then plastically deforms and leads to a flat reflector at the bonding temperature, often of order 150°C. When cooled to the ambient temperature, the mirror can have a significant curvature due to the CTE mismatch between silicon and metal. This curvature will slowly decrease if the metal creeps at room temperature, though this process can take many months. Single-sided metallization will thus generally relax to a flatter state, as the metal creeps but not the underlying silicon. If both sides have been metalized to create a symmetrical and thus initially flatter mirror, there is however the potential for an uncontrolled increase in mirror curvature if the creep occurs differently for the two metals films, which is quite likely given that they were not deposited under identical conditions.

One can of course obtain flatter metalized mirrors by making the silicon thicker, but this decreases the resonance frequency, increasing response time and susceptibility to mechanical shock, or leads to very high drive voltages, with associated dielectric breakdown and dielectric charging issues.

4.2.4.4 Conclusions on Creep

Silicon MEMS are not affected by creep below roughly 600°C, as long as there is no metal on the suspension. This holds for SiN_x and SiO_x flexures too.

For metal MEMS, creep can be an important failure mode, which can be mitigated by reducing the applied stress (by geometry of material change), reducing operating temperature (better heatsink, different package), or a change of material (either to a brittle materials, or more commonly to an alloy with much higher creep resistance).

4.2.5 Fatigue

Since MEMS have moving parts, fatigue was initially thought to be an important failure mode, especially for parts requiring many operation cycles. Fatigue has not turned out to be a lifetime limiting factor in any commercial MEMS device. For silicon, the material most commonly used in MEMS, fatigue occurs only for applied stresses greater than half the single-cycle fracture strength, i.e., at stress levels close to fracture, and thus any reasonable design will not have stress levels sufficiently high for fatigue to be relevant. For metal MEMS, fatigue can occur at lower relative stress levels, but is generally much less problematic than creep (plastic deformation) or other failure modes such as charging.

In view of the extensive research carried out on silicon MEMS, it is now well known how to avoid fatigue (by controlling the maximum stress and the relative humidity). The topic will therefore be briefly addressed for silicon. Metal MEMS, because of their lower melting point, are more susceptible to fatigue.

4.2.5.1 Introduction to Fatigue in Brittle and Ductile Materials

Fatigue is the cycle-dependent decrease in yield strength, i.e., a slow crack growth leading to failure due to a periodically applied stress. The maximum stress at each cycle is below the single cycle fracture strength, yet at each cycle of alternating stress, the crack grows, reducing the strength of the material, and eventually leading to failure.

The key concept for fatigue is that fluctuating loads can lead to failure when monotonic loads do not. Some materials, such as steel, display an endurance limit: a critical stress level below which failure does not occur regardless of number of cycles. Aluminum and polymers do not show such a limit. Fatigue data is often plotted as a stress-life (S/N) curve, plotting the maximum applied cyclic stress vs. the number of cycles to failure (see Fig. 4.38 for data on micromachined silicon).

Ductile materials (e.g., most metals) and brittle materials (e.g., silicon, ceramics) exhibit very different fatigue behavior. For ductile materials, fatigue generally occurs due to plastic deformation at the crack tip involving dislocation motion, leading to alternating blunting and sharpening of an existing crack tip. Fatigue can therefore occur over a large range of stresses. Brittle materials do not plastically deform at ambient temperatures as they lack dislocation mobility, so for brittle materials the crack progresses by cycle dependent degradation of the toughness of the material in the wake of the crack, and thus fatigue only occurs for stress levels near the yield strength [34].

For macroscopic materials the mechanisms of fatigue crack propagation are well summarized in reference [35]. For MEMS devices, with their large surface to volume ratio, and critical dimensions comparable to grain size, the surface and microstructure play an essential role in fatigue properties.

4.2.5.2 How to Measure Fatigue in MEMS

In view of the small size of MEMS devices, standard test structures commonly used on macro-scale samples for fatigue measurements cannot be used. For silicon (poly-crystalline and single crystal) the most widely used test device is the one first proposed by Van Arsdell and Brown at MIT [36], and shown in Fig. 4.37. It consists of a free-standing silicon proof mass, roughly triangular with 300 μm sides, suspended by a single notched beam. Two comb drives are used, one to electrostatically drive the mass at resonance (in plane, roughly 20–40 kHz), and the other to capacitively measure displacement in order to determine the resonance frequency. The stress is maximum at the notch, which can be pre-cracked with a nano-indenter. As the crack grows at every cycle, the resonant frequency decreases. By measuring the evolution of the resonant frequency with time and environmental conditions the crack growth can be determined. These resonators allow crack growth rates of down to 10^{-12} m/s to be measured [36]. See also in Chapter 5 for the use of laser Doppler vibrometry to measure resonance frequency.

4.2.5.3 Silicon MEMS

Silicon is a prototypical brittle material, in which fatigue has never been observed in air at room temperature for bulk samples. Dislocation activity not observed at low homologous temperatures ($T_{\text{ambient}} / T_{\text{melt}} < 0.3$), and there is no evidence of extrinsic toughening mechanisms, such as grain bridging, nor of stress corrosion cracking (environmentally induced cracking). So fatigue was not expected in silicon in air room temperature.

Yet, as reported by Van Arsdell et al [36], Muhlstein et al. [37, 38, 27], and Kahn et al. [39, 40] polysilicon films from both the MUMPS and SUMMiT™ processes show failures due to fatigue after 10^6 to 10^{12} cycles when operated in ambient air at stresses as low as 1/2 of single-cycle fracture strength, see Fig. 4.38 for stress-life (S/N) curves from several authors.

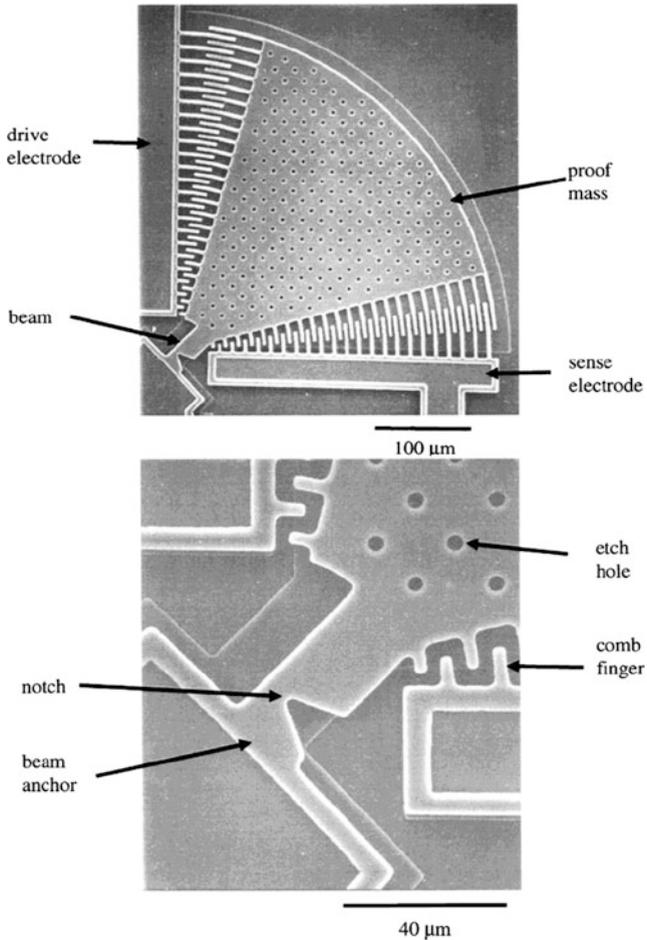
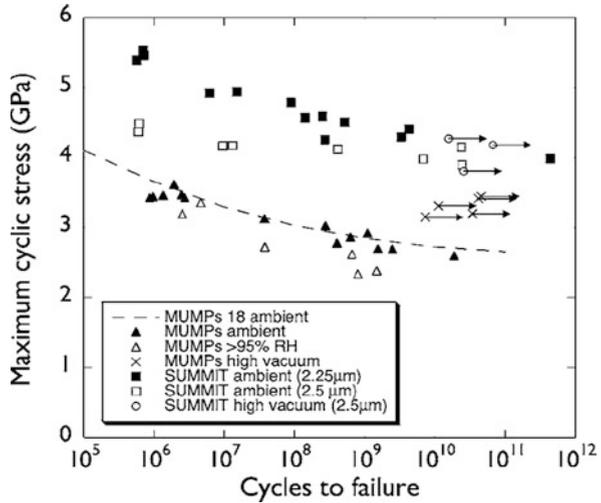


Fig. 4.37 Resonator with stress concentrator at the suspension to measure crack growth due to fatigue [36]. Reprinted with permission Copyright 1999 IEEE

Relative humidity plays a key role in fatigue lifetime for silicon. Muhlstein et al. [37, 38] and Alsem [41] have shown that fatigue in silicon MEMS is due to a reaction-layer fatigue process, occurring in two steps. First, at locations where cyclic stresses are maximum, the post-release oxide is thickened. Second, this oxide undergoes moisture-assisted cracking, leading to sub-critical cracks growth. Once fresh Si is exposed at the crack tip, it expands upon oxidizing, further driving the crack growth at each cycle. The presence of moisture is required for this crack growth.

The data in Fig. 4.38 shows clearly the effect of humidity on the fatigue life of polysilicon MEMS: in high vacuum, no fatigue is observed at cyclic stresses of over 4 GPa after 10^{11} cycles. For ambient air (roughly 30–40% RH) fatigue is clearly

Fig. 4.38 Combined maximum cyclic stress-lifetime (*S/N*) data for polysilicon MUMPS and SUMMiT V™ devices, different types of devices are tested in ambient air (25°C, 30–40% RH), high relative humidity (25°C, 95% RH), and very high vacuum (25°C, <2.10⁻⁷ mbar). Reference [41] reprinted with permission Copyright 2006 American Institute of Physics



seen for large stresses, and at 95% RH, the stress leading to fatigue failure is lower than for ambient air.

Even single crystal silicon shows high-cycle fatigue in air [27], with the tested samples showing lives from 10⁵ to 10¹¹ cycles before failure for stress amplitudes from 4 to 10 GPa.

While the research groups discussed above have clearly shown the existence of fatigue in silicon MEMS, and experimentally plotted a *S/N* curve, one should note obtaining this data required carefully designed test structures that can only reach the required stress levels at resonance.

As a general rule, if either (a) the maximum cyclic stress is less than 20% of single-cycle fracture and if humidity is not controlled, or (b) maximum cyclic stress is less than 40% of single-cycle fracture and the device is hermetically packaged in an ultra-dry ambient, high-cycle fatigue of silicon parts will not occur.

Since silicon is a brittle material and thus exhibit a range of fracture strength, the conservative MEMS designer will tend to limit the maximum designed stress to below 20% of yield strength, thus avoiding at the same time fatigue. Single-crystal and poly-silicon micromirrors from Lucent Technologies for instance have not shown any fatigue effects after over 10¹⁰ cycles in ambient air, because the maximum stress levels in the suspension beams is only a few percent of yield strength, which is also why they survive the very large externally imposed displacement in Fig. 4.2.

4.2.5.4 Metals

Metal films are used in a variety of commercial MEMS, notably Texas Instruments DMD mirror array. Since metals are ductile and have mobile dislocations at ambient

temperature, plastic deformation and hence fatigue can be a life-limiting factor. Care must be taken to remain in a “safe” section of the S/N curve.

As for silicon, special test structures were devised to test MEMS metal films, in view of the length-scale dependence of material properties, which for Al films was found to be very important. The two main metals are LIGA electroplated Nickel, and Aluminum.

TI mirrors have a lifetime estimate of over 100,000 h with no pixel failure [42]. At a mirror modulation frequency of 7 kHz, each micromirror needs to switch about 2.5×10^{12} cycles. TI therefore extensively studied fatigue, but do not report observing any failures, running an array of 307,000 micromirrors up to 10^{12} cycles with no failures, corresponding to 2×10^{18} total mirror movements [32].

TI had expected to observe fatigue failures, based on standard models for Al bulk samples. In macroscopic samples, the initial crack forms at the surface grain boundaries due to dislocation pile-up, leading to a crack when the dislocation density is high enough. The crack then grows by further dislocation motion at the tip, with the associated plastic deformation. The Al alloy films used by Ti for its suspension are however only one grain thick (approximately 100 nm). M. Douglas proposes that the two free surface of each grain are effective at relieving stresses due to dislocations, preventing the accumulation of a high enough dislocation density to form fatigue cracks [32].

Electroplated Nickel, used in the LIGA process, has been studied for fatigue by several groups (e.g., [43, 44, 45, 46]), and the properties for thin films is found to be similar to that of macroscopic bulk annealed samples, with an endurance limit of order 200 MPa, which is two orders of magnitude less than for silicon. Figure 4.39 is a S/N plot for electroplated Nickel.

Since fatigue in metals is associated with plastic deformation, the same precautions to minimize creep are also effective at minimizing fatigue related failures: (1) re-engineering the suspension to minimize stress levels (avoiding stress

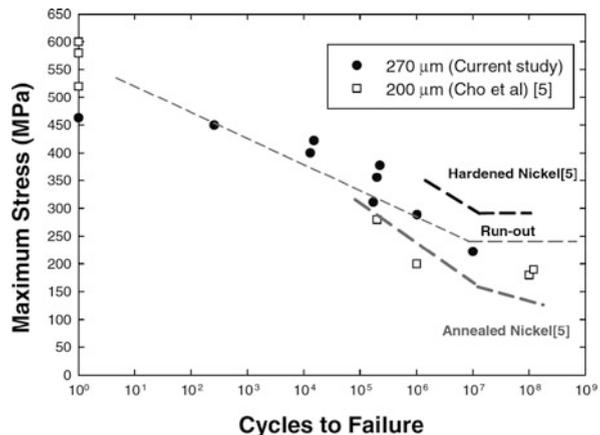


Fig. 4.39 S/N curve for 270 μm thick LIGA Nickel for $R=0.1$, showing an endurance limit at 200–250 MPa, [43]. Reprinted with permission Copyright 2007 Springer

concentration); (2) reducing the operating temperature; (3) choosing a more creep-resistant material, such as an alloy rather than a pure metal.

4.3 Electrical Failure Modes

Because MEMS devices, unlike integrated circuits, have moving parts, their failures are often thought to be mechanical in origin. This is an overly simplistic assumption, which might have been true in the early days of MEMS, but is no longer the case. As design rules for MEMS have matured, mechanical failures have become increasingly uncommon, and electrical failures can play a large role in MEMS lifetime.

4.3.1 Charging in MEMS

4.3.1.1 Introduction to Dielectric Charging

Dielectric charging is only a concern for MEMS devices that are sensitive to charge, namely principally electrostatically driven or sensed MEMS devices. MEMS using electromagnetic or thermal actuation or sensing principles are generally insensitive to dielectric charging.

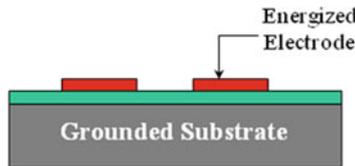


Fig. 4.40 Schematic cross-section of a MEMS electrode, consisting of a substrate (e.g., Silicon), a dielectric (e.g., SiN_x or SiO_x) and electrodes (e.g., Al or Si)

Electrostatic MEMS devices often require high operating voltages (50–200 V) applied across small gaps (0.1 to a few μm), resulting in electric fields of order 10^8 V/m across the dielectric. A simplified cross-section is shown in Fig. 4.40. The high fields across both the bulk and along the surface of the dielectric can give rise to charge injection that contributes to several possible failure modes. These bulk and surface leakage currents, and associated trapped charge, are a strong function of voltage, temperature and relative humidity. In MEMS devices, the dielectrics often also serve a structural role, and their stress must be carefully tailored. This is general done at the expense of electrical properties (e.g., reduced breakdown field, increased trap density).

For fixed applied electrode voltages, the electrostatic force on a MEMS actuator or sensor is assumed to be constant in time. This situation however only holds in the ideal scenario where the dielectric contains no mobile charges or charge traps,

so that all electric fields are uniquely determined by the voltages applied to the electrodes. Charging of the dielectrics in MEMS structures gives rise to undesired and difficult to predict time-varying electrostatic forces which are a serious performance issue for a wide range of electrostatically driven or sensed MEMS devices including microphones, displays, micromirrors, and RF switches.

The failure modes related to dielectric charging are drift in applied electrostatic force as a function of time, leading to a gradual shift in actuation voltage (e.g., calibration change), or a gradual change in rest or actuated position, or a gradual shift in release voltage. For a micromirror, this leads to a time dependent tilt angle, which can lead to large insertion loss or snap-down of the mirror and associated stiction concerns. For an RF switch, this can lead to a device which eventually is stuck in the “down” state, when the trapped charge provides a larger holding force than the restoring force of the suspension, or a device stuck in the “up” state, when the trapped charge screens the applied voltage (see case study in [Chapter 2](#) for MEMtronics RF switches). Minimizing dielectric charging is also important so that MEMS devices can be operated in “open loop”, i.e., without the need for complex and possibly bulky or power-hungry feedback electronics and sensors.

Sensors such as some accelerometers and gyros that use a capacitive read-out scheme can also be very susceptible to charging, and the stability of the output is greatly enhanced by the same techniques that minimize actuator drift. Designs that eliminate charging are usually radiation hard, as charges in dielectrics due to ionizing radiation will not affect device performance. We shall return to this point in the section on radiation effects.

There are a number of very effective techniques to eliminate or mitigate charging, but they often entail reliability trade-offs, as will be discussed below.

Origin of Charging

When a DC bias is applied across a dielectric, charge carriers from the electrodes can be injected into various charge traps in the bulk or on the surface of the dielectric. Leakage currents can occur on the surface of the dielectric between electrodes on the dielectric held at different potentials, or through the bulk of the dielectric when there is a potential drop across the dielectric. This charge injection leads to the buildup of a quasi-static charge on the surface or in the bulk of the dielectric. In addition, mobile ions (such as Na^+) can migrate on the surface of the dielectric, and this situation is significantly worsened by the presence of any adsorbed water layers on the surface, as occurs in the presence of humidity.

The charging and discharging times to fill or empty the traps can be different by orders of magnitude, and are typically much longer than the mechanical response of the MEMS device (typically minutes or hours to charge the traps, vs. milliseconds response of the MEMS device). Unless the dielectrics are suitably electrically shielded from the actuator, the time-dependent charge on or in the dielectric gives rise to a time-dependent electrostatic force on the actuator, whose equilibrium position or force then changes with time. This “drift” of the actuator position is of

electrical, not mechanical, origin (i.e., it is not due to plastic deformation of the supporting springs).

Because of the high fields ($\sim 10^8$ V/m) applied across dielectrics in electrostatically actuated MEMS devices, conduction is typically non-ohmic, and is dominated by conduction via traps in the dielectric, and by charge injection and tunneling. For applications where the relative dielectric constant is not an important parameter (e.g., when the dielectric is used for electrical insulation rather than to make a capacitor), the most common materials in MEMS are silicon nitride and silicon oxide.

It is not clear what happens on an atomic scale for charging and dielectrics. Different behavior (charge/discharge time constants, trap densities) is observed for slightly different deposition or growth techniques (such as CVD, PECVD) and a strong dependence is seen on annealing conditions and film stoichiometry.

The two main conduction mechanisms through those dielectrics are the Frenkel-Poole (FP) and Fowler-Nordheim (FN) models. FP conduction describes charge transport dominated by traps, and so very accurately models conduction in Si-rich SiN films commonly used in surface micromachining. FN conduction, which does not rely on defects or traps, describes tunneling of electrons from the electrode conduction band into the dielectric conduction band through part of the potential barrier at the conductor-dielectric interface. The FN model is most appropriate for conduction through silicon oxides.

While the details of the charge accumulation process are not well understood, it is generally accepted that the total trapped charge is the integral of the injected current. This is why it is important to understand the leakage current.

The Frenkel-Poole current is proportional to:

$$j_{F-P} \propto \exp \left[\frac{q (\beta \sqrt{E} - \phi)}{k_B T} \right] \quad (4.9)$$

where $\beta = (q/\pi n^2)^{1/2}$, q is the electronic charge, n the index of refraction, E the electric field across the dielectric, and ϕ the activation energy for conductance mechanism.

The Fowler-Nordheim current scales as:

$$j_{FN} \propto \frac{E^2}{\Phi_B} \exp \left[-\frac{8\pi \sqrt{2qm} (\Phi_B)^{3/2}}{3hE} \right] \quad (4.10)$$

Where Φ_B is the potential barrier for electron injection into the oxide (for Si/SiO₂ interface $\Phi_B \approx 3.2$ eV), m the electron mass, and h is Planck's constant.

As an illustration that Si-rich SiN_x follows very accurately the Frenkel Poole model, Fig. 4.41 shows leakage current measured through 0.6 μ m thick silicon nitride (from a MUMPS run at Cronos in 2002, now MEMSCAP). By measuring the leakage through different films one can get an order of magnitude estimation of the amount of charging.

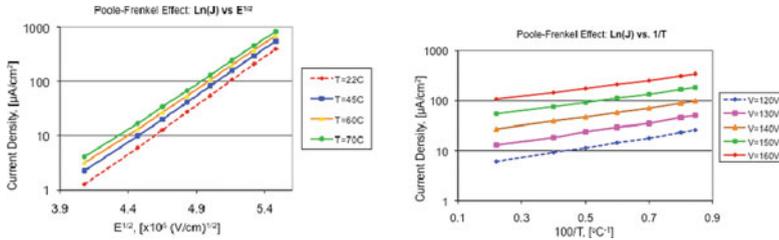


Fig. 4.41 Scaling of leakage current through the dielectric as a function of inverse temperature and square root of the electric field for Cronos (now MEMSCAP) SiN_x , showing clear Poole-Frenkel scaling. (Data courtesy of A. Gasparyan). Reprinted with permission of Alcatel-Lucent USA Inc.

4.3.1.2 Mitigation of Charging Effects

In this section, we focus on two devices to illustrate the effect of charging due to high applied electric fields: silicon micromirrors with SiN_x and SiO_x dielectric under the actuation electrodes, and metal RF capacitive switches with SiN_x and high- k dielectrics. In the section on radiation effects, we shall focus mostly on polysilicon accelerometers as examples devices failing due to charge buildup from ionizing radiation.

As is generally the case for reliability issues, there is a trade-off between performance and reliability. Many of the solutions below, in particular those related to redesigning the device, come at the cost of increased fabrication complexity or packaging cost. For instance charging can be greatly reduced by hermetic packaging, but hermetic packaging can cost of up to \$1000 per package for large arrays of micromirrors. It should be noted that traps will charge and discharge faster at higher temperature and that therefore charging can be less of a problem at higher temperatures. Since most failure modes are accelerated by temperature, following an Arrhenius model, heating the device to influence dielectric charging is not a generally acceptable solution because of the lifetime penalty associate with higher temperature operation.

We list some possible solutions to charging, then delve into more detail for the effect of geometry, charge dissipation layers and carefully engineered voltage levels.

There are a number of documented ways to solve or minimize the “charging” problem, including:

- Bipolar AC drive voltage
- Geometry changes to
 - minimize area of exposed dielectric, or pattern the dielectric
 - shield movable parts (sense mass, actuators) from electric fields due to trapped charge.
 - Selectively remove dielectric to avoid charging

- Charge Dissipation Layers to remove surface charge and provide shielding
- Change dielectric or change composition to reduce amount of trapped charge or decrease discharging time constants (e.g, SiO_x instead of SiN_x)
- Reduce electric fields (e.g., thicker dielectric or with higher dielectric constant, redesigned springs to operate at lower voltages)
- Optimized drive voltage (multi-level: one to actuate, one to hold), or charge monitoring
- Control of packaging ambient to minimize humidity and contaminants

Using a bipolar ac rather than dc voltage drive seems at first like the perfect simple solution, for instance as proposed by Reid and Webster [47]. It does indeed greatly reduce charging effects, but does not completely eliminate it, due to different time constant for filling and emptying traps of different polarity and of different types (surface, bulk, etc.). Since AC actuation requires more complex drive electronics and has significantly higher power dissipation, other approaches are often preferred. De Groot et al. provide a good overview in [48].

4.3.1.3 Geometry Changes

As a concrete example, and following closely reference [49], let us consider the SOI micromirrors developed by Lucent Technologies in 2000–2002, for which a schematic cross-section of a MEMS micromirror shown in Fig. 4.42. The bottom wafer (“electrode wafer”) consists of a Si substrate covered by a dielectric (here SiO_x) on which electrodes (Al or poly-silicon) are patterned (over one or more wire routing layers). The small black dots represent trapped charges. A polyimide spacer is patterned on top of the electrode wafer, and an SOI wafer is flip-chip’ed onto the spacer. The micro-mirrors and supporting springs are etched out of the 5 μm thick Si layer in the SOI wafer. Applying a voltage to one or more electrodes tilts the mirror. Figure 4.43 is an SEM micrograph of one such mirror.

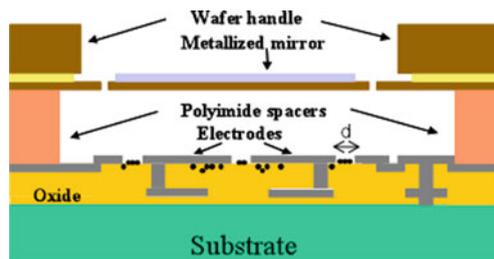


Fig. 4.42 Schematic cross-section of an electrostatically driven MEMS micromirror. Mirror and electrode wafers are fabricated separately and then assembled. The black dots between and under electrodes represent trapped charge in the dielectric, as well as slowly moving mobile charges on the surface of the dielectric. The substrate is grounded while the electrodes can be grounded or held at a fixed potential. Reference [49] reprinted with permission Copyright 2004 IEEE

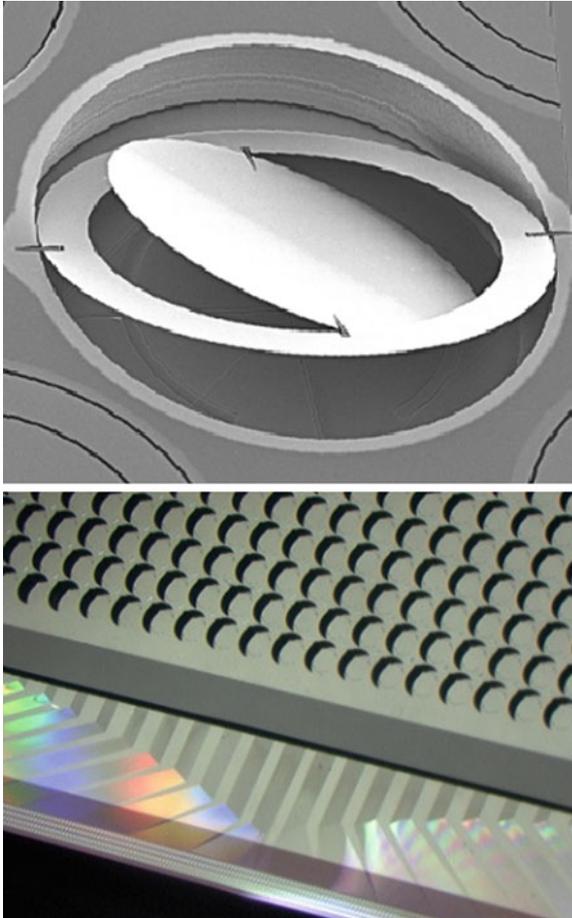


Fig. 4.43 (left) SEM micrograph of an Alcatel-Lucent two-axis MEMS micromirror fabricated from $5\ \mu\text{m}$ thick single crystal silicon. The mirror diameter is $875\ \mu\text{m}$. The cross-section of this mirror is schematically illustrated in Fig. 4.42. Reference [135] reprinted with permission Copyright 2003 IEEE (right) optical micrograph of the assembled device, the wire routing is clearly visible on the lower part of the bottom chip. Reprinted with permission of Alcatel-Lucent USA Inc.

The advantage of this 2 chip approach for studying charging is that one has direct access to the electrodes and dielectric prior to bonding, allowing for more anti-charging techniques to be tried than for surface micromachined MEMS.

Once can mitigate the effects of dielectric charging by controlling the electrode and dielectric geometry: principally the width of the gaps with exposed dielectric between electrodes, the thickness of the electrodes, and selective etching of the dielectric. Approaches to minimize drift by changing the electrode geometry include creating overhanging electrodes to shield the actuator from the dielectric

(though this may present a fabrication challenge and decrease the breakdown voltage).

The width of the exposed dielectric (i.e., the gap d between neighboring electrodes in Fig. 4.42) plays two roles: first, the larger the exposed area of dielectric there is under the actuator, the larger the electrostatic force that surface charge can exert on the actuator. This is a strong motivation for narrow gaps. Second, it is known that the dynamics of charge transport on the surface of dielectrics can be characterized using a diffusion model [49, 50]. This model suggests that to first order the saturation time t_s scales with gap size d and surface diffusion coefficient D as $t_s \sim d^2/D$. For silicon oxide, D is of order 10^{-11} cm²/s. Narrower gaps not only reduce the area of exposed oxide thus decreasing the magnitude of charging induced drift, but also shorten the saturation time. Therefore, small gaps between electrics are helpful for reducing the adverse effect of charging on mirror tilt angle stability. Note however that minimizing anodic oxidation (see Section 4.4.2) and increasing in-plane breakdown voltage (see Section 4.3.2) calls for larger gaps: a careful consideration of packaging and operating voltages and environment is required before deciding on the ideal gap size for a given application.

In Fig. 4.44 the drift (due to dielectric charging) in micromirror tilt angle is plotted for two Lucent Technologies MEMS micromirrors of similar geometry but with different gaps between electrodes. For a 10 μm gap, over 0.1 degree drift are observed in 15 h (with a saturation time is of order 100 h). For a 2 μm gap only 10 millidegree of drift are observed, with full saturation after 1 h [1]. Reducing the gap from 10 to 2 microns should to first order reduce the saturation time by 25 times, not out of line with what was observed.

A more effective and radical solution is to simply remove the dielectric from regions where the field from trapped charge in the dielectric can exert an electrostatic force on the MEMS device, as reported in [49]. In Fig. 4.42, the trapped

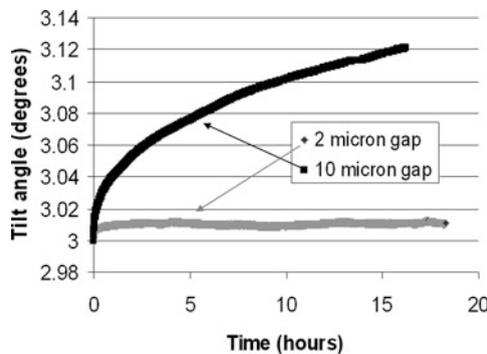


Fig. 4.44 Tilt angle vs. time for two Lucent micromirror test vehicles. The same dc voltage was applied to both at time $t=0$, but one mirror had a 10 μm gap between the actuation electrodes, and the other a 2 μm gap. The smaller gap show much shorter saturation time, and much less charging (hence less change in tilt angle with time). Reference [49] reprinted with permission Copyright 2004 IEEE

charge under the electrodes is not of concern, since it is shielded by the electrodes. The trapped charge between the electrodes however will give rise to undesired electrostatic forces. Starting with an electrode design with $2\ \mu\text{m}$ wide gaps between electrodes, the mirror is shielded from the dielectric by undercutting the oxide in the gaps around the electrodes with a wet etch that stops on the underlying polysilicon shield layer, as shown schematically in Fig. 4.45. After the undercut, the mirror “sees” only conductive surfaces, thus eliminating charging induced tilt angle drift. Charge may build up in the remaining dielectric, but because of the geometry, these charges cannot give rise to any electric field at the mirror. Figure 4.46 is an SEM micrograph of an electrode chip where the oxide has been etched away: the undercut is clearly visible.

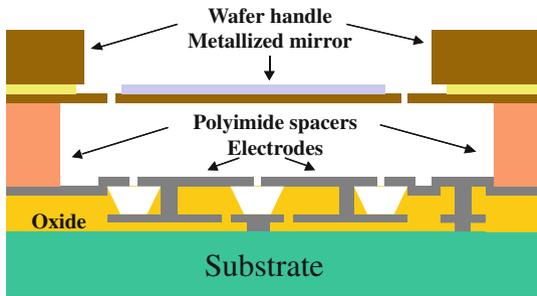


Fig. 4.45 Schematic cross-section of a MEMS micromirror device similar to the one shown in Fig. 4.42, but with the oxide selectively etched under the electrodes so that the mirror is fully electrically shielded from any trapped charge in the remaining oxide. Figure 4.46 is an SEM micrograph of the bottom chip of such a device after the isotropic oxide etch. Reference [49] reprinted with permission Copyright 2004 IEEE

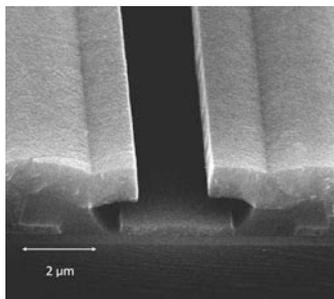


Fig. 4.46 SEM micrographs of the gap between 2-level poly-Si electrodes, with the exposed oxide between levels removed by wet etch. The electrodes (overhanging structures) are spaced by $2\ \mu\text{m}$. Rather than leaving oxide between the electrodes, the bottom of the gap between electrodes is covered by a grounded strip of poly-Si (running up the center of the image). The electrical potential of all surfaces is well defined, and the MEMS mirror is shielded from trapped charge in any remaining oxide. Drift in tilt angle due to dielectric charging is completely eliminated. Reference [49] reprinted with permission Copyright 2004 IEEE

This technique was found to be highly effective and led to micro mirrors with drift of less than 10 millidegree per day when held at a 5-degree tilt (i.e., below the measurement accuracy, and at level where drift in mirror tilt angle added less than 0.1 dB to the loss of the optical cross-connect in which an array of 256 or 1196 such micromirrors were used). Etching away the dielectric is a very effective solution, but care must be taken not to overetch the dielectric, which might lead to lower breakdown voltages, and not to damage the electrodes, which typically are made from poly-silicon in order to survive the oxide etch. This solution would be very challenging to implement with Al electrodes because of their susceptibility to attack by HF, but is ideal for use with poly-Si electrodes when 2 or more levels are available.

4.3.1.4 Charge Dissipation Layers

Following [49], there may be cases where it is not feasible to etch away the dielectric as shown in Fig. 4.45, for instance when fabricating electrodes on top of CMOS circuits, or due to common limitations of the process flow, or when using a multi-user or standardized foundry process. In that case increasing the conductivity of the dielectric can be an effective means to control charge build-up in the dielectric.

A well-known solution to the charging problem is to deposit or grow a thin conductive layer on top of the dielectric in order both to bleed off surface charge and to screen bulk charge from the reflector. This Charge Dissipation Layer (CDL) must not contain charge traps, and must be a good enough conductor to efficiently drain charge and provide electrostatic screening, while not being so conductive as to short out the electrodes by drawing too much current. The CDL typically consists of a thin film of a poor conductor such as a doped oxide. Lithium Niobate modulators have a similar charging problem to MEMS (though no moving parts). For instance, US Patent # 5,949,944 describes a CDL for LiNbO₃ modulators.

Figure 4.47 is a plot of tilt angle drift for two identical Lucent Technologies micromirror devices, except that the electrodes of one device were coated with

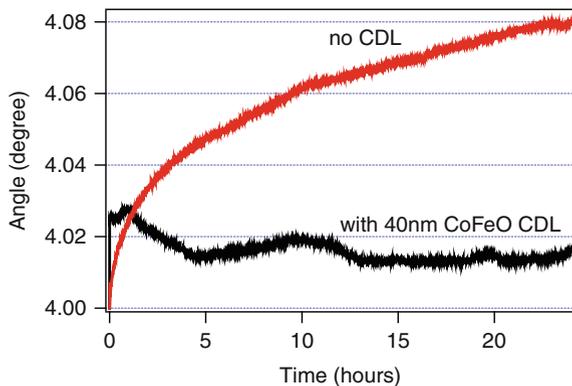


Fig. 4.47 Tilt angle drift for two Lucent Technologies SOI mirrors, on with and one without CDL, showing how the CDL effectively mitigates the effect of dielectric charging. Reference [49] reprinted with permission Copyright 2004 IEEE

40 nm of CoFe_2O_4 [49]. The Co-Fe-O CDL reduces both the magnitude and time constant of charging related drift by a factor of more than 10. The major advantage of Co-Fe-O is also its main potential problem: the conductivity the Co-Fe-O layer can be tuned over several orders of magnitude by annealing in oxidizing or reducing atmospheres. This allows for great flexibility in tuning of the CDL conductivity, allowing the Co-Fe-O films to be used for many different MEMS geometries and designs. The tunability however opens questions about the impact of high temperature packaging steps and about long-term stability of such coatings, which have not yet been studied, and would need to be carefully studied and acceleration factors identified before it could be used on a commercial product.

Rather than depositing a CDL over the dielectric, the dielectric material itself can act as a CDL if its electrical transport properties are suitable: dielectric materials with larger coefficient of surface diffusion and higher bulk mobility of charge carriers are less prone to static charge build up. However these more “conductive” dielectrics have lower breakdown electrical fields. This raises an interesting reliability vs. performance issue: extremely insulating dielectrics have larger breakdown fields, and thus offer higher protection against shorting through the dielectrics. Since electrostatically operated MEMS devices typically operate at voltages as high as 300 V, this is not a negligible issue. Slightly “leaky” dielectrics can make for devices where charging is much less of an issue, but lifetime may be limited by breakdown of the dielectric. For capacitive RF MEMS switches, Raytheon patented the approach of leaky SiN to control charging [52].

Figure 4.48 is a plot of tilt angle stability for 3 Lucent Technologies surface-micromachined mirrors of identical geometry, each fabricated on a different wafer by Cronos (now MEMSCAP). Each wafer has a slightly different composition of the Si-rich SiN_x dielectric under the electrodes. Small changes to the composition

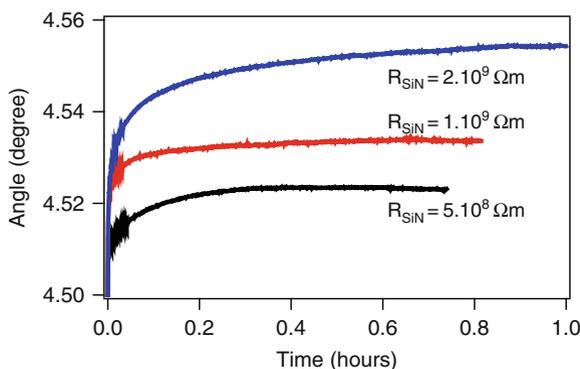


Fig. 4.48 Dependence of the charging-induced tilt angle drift of two Lucent Technologies surface micromachined mirrors on the resistivity of the underlying SiN dielectric layer: devices with lower resistivity dielectric films have less drift because charge is more readily drained away or screened. Reference [49] reprinted with permission Copyright 2004 IEEE

of the SiN change the film’s conductivity, approximately $2 \times 10^9 \Omega\text{m}$, $1 \times 10^9 \Omega\text{m}$ and $5 \times 10^8 \Omega\text{m}$ for the three samples. The higher the conductivity of the SiN, the smaller the angular drift, in line with the above argument that “leaky” dielectrics reduce dielectric charging (since charge leaks out), but at the expense of lowered electrical reliability.

A common model of dielectric breakdown is the “charge to failure” model [53]: the resistance of a dielectric in a large electric field remains very high even though electrons and holes are injected. These charge carriers damage the dielectric, creating more defects and charge traps. Once a critical amount of damage has been done, a conductive path is created through the dielectric, which has then broken down. So the higher the leakage current, the faster the critical charge will be reached. The thickness and conductivity of the dielectric must be carefully considered, trading off dielectric breakdown vs. charge mitigation.

4.3.1.5 Multi-Step Voltage Drive for RF MEMS Switches

This section addresses mostly charging in RF MEMS switches, very promising devices in terms of performance and integration, but whose commercialization is limited by its reliability issues. There are two main classes of RF MEMS switches: contact (or ohmic) and capacitive. We discuss here only the capacitive type, since the root cause of the main failure modes of such capacitive RF MEMS switches is dielectric charging.

The design and operation of RF MEMS switches are well described in [54] and [55], and was introduced in Chapter 2 for the third case study of a MEMtronics RF switch. Figure 4.49 is a schematic cross-section of the capacitive RF MEMS switch, which generally operates in two states. As seen in Fig. 4.50 it consists of a metallic bridge or membrane suspended above a conducting line or coplanar waveguide. There is a thin layer of high dielectric constant dielectric on the bottom trace to prevent a short-circuit when the membrane is deflected downwards electrostatically by applying a potential difference between the grounded membrane and the lower trace. In the “up” state (low capacitance state, C_{off}) with the top metal membrane

Fig. 4.49 Schematic cross-section of a capacitive RF MEMS switch, *top*: undeflected (no dc bias), *bottom*: snapped down (bias voltage larger than $V_{\text{pull-in}}$). In this geometry the metal trace serves both as DC actuation electrode and as RF transmission line

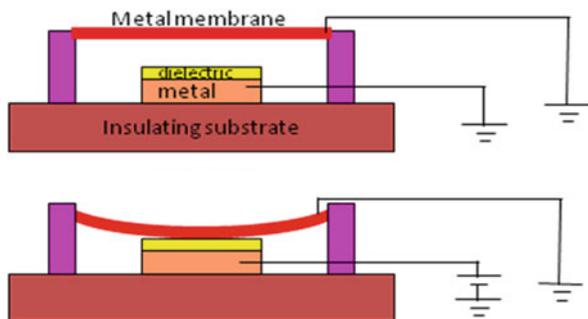
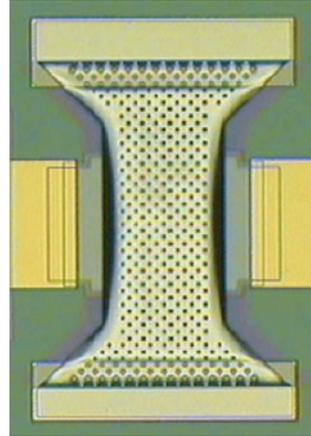


Fig. 4.50 Top view of a Raytheon capacitive RF switch [54]. Reprinted with permission Copyright 2001 IEEE



undeflected, the RF signal on the lower conductor propagates unaffected. In the “down” state (high capacitance state, C_{on}) the top metal membrane is deflected downwards by a DC bias on the central line, and signals in the lower conductor in the gigahertz range are shunted to ground or reflected.

A performance metric for RF MEMS switches is the $C_{\text{on}}/C_{\text{off}}$ ratio. C_{off} is defined simply by the geometry and permittivity of the dielectric, but C_{on} depends both on the dielectric constant of the dielectric, and on the flatness of the dielectric as the membrane will never be in perfect contact with it and there is an effective air gap remaining due to the roughness of the lower surface of the membrane and the dielectric.

Capacitive RF MEMS switches might be expected to be reliable because, unlike ohmic contact switches, there is no direct metal to metal contact. They fail primarily due to parasitic charging of the dielectric which leads to a drift in both the voltage required for actuation (pull-in voltage $V_{\text{pull-in}}$) and, more critically, the voltage below which the membrane return to the up position ($V_{\text{pull-out}}$), see Fig. 2.32. $V_{\text{pull-out}}$ is much smaller than $V_{\text{pull-in}}$, typically 1–4 V compared to 30–80 V.

The dielectric is typically less than 300 nm thick (to achieve large C_{on} of order 1 pF), and capacitive switches usually require 30–80 V for actuation. In the down-state therefore there is a very large electric field (greater than 10^8 V/m), and hence charge will be injected into the dielectric. For silicon nitride films, which are often preferred because they can be deposited at low temperature over metallization, Frankel-Poole type charge injection is observed. For high- k materials, different charge transport mechanisms may come into play.

Depending on the location of the trapped charge, the trapped charge can either increase or decrease the voltage required to pull the membrane in. Bulk charge, injected from the bottom electrode, reduces $V_{\text{pull-in}}$, while surface charge, on the top of the dielectric, screens the applied voltage and increases $V_{\text{pull-in}}$. [56, 57].

Regardless of the polarity of the trapped charge, when the membrane is in the down-state the trapped charge provides an electrostatic holding force when the voltage is removed.

In normal operation, when the applied voltage is reduced below the pullout voltage, the membrane snaps back to its up position, assuming that the restoring force of the spring is larger than any stiction forces. However if $V_{\text{pull-in}}$ reduced below 0 V, the switch is stuck in the down position and hence has failed.

Fundamental work was done by Wibbeler et al. [58], modeling the shift in actuation voltage for a simple electrostatic parallel plate actuator due to trapped charge on and electrode. They also found that air discharge can be an important source of trapped charge.

Van Spengen et al. [59] measured and modeled charging in RF MEMS switches. They described in more detail the more complex effect of charged relation and provide a detailed model of the critical amount of charge required for failure of a capacitive MEMS switch, in particular taken into account the mechanical response speed of the switch which is generally much slower than the switching speed of the control signal. They find that there are critical positive and negative charge densities for failure, and that measurements are complicated by the slow discharging of the traps.

A key observation of van Spengen et al [59] is that the lifetime of an RF switch does not depend on the actuation frequency but on the total actuation time, as shown in Fig. 4.51. The key parameter is simply the total time spent in the downstate i.e., the time spent injecting charge into the dielectric, not the number of up/down cycles. The amount of accumulated charge, and hence lifetime, depends on the duty cycle and the applied voltage. The duty cycle is important because of the discharging that occurs when the actuation voltage is removed. Because fatigue had initially been

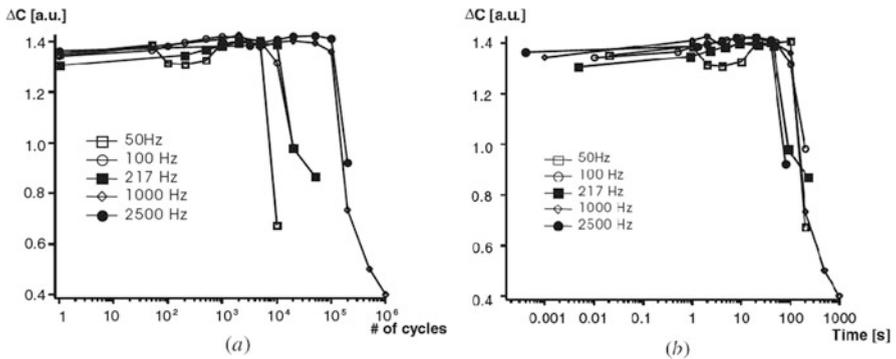


Fig. 4.51 Plot of the change in capacitance (essentially $C_{\text{on}}-C_{\text{off}}$) for RF MEMS test structures at IMEC, plotted as a function of the number of cycles (*left plot*), and as a function of total time in the down state (*right plot*). The device fails when the capacitance change per cycle decreases. It is obvious from these figures that the lifetime does not depend on the actuation frequency but rather on the total actuation time. Total actuation time is directly related to the total amount of charge injected in the dielectric. Reference [59] reprinted with permission Copyright 2004 IOP

a failure mode, and because MEMS manufacturers love reporting large numbers, much data on RF MEMS switches has been reported as a number of cycles to failure. It is important to note that it is really the time in the down state that is the key parameters that dictates lifetime.

Goldsmith et al. [60] have reported that the lifetime of a capacitive switch increases exponentially as the actuation voltage is decreased. This is shown in Fig. 4.52 for Goldsmith et al., and in Fig. 4.53 for van Spengen et al. The exponential dependence of lifetime on actuation voltage is reasonable in view of the exponential

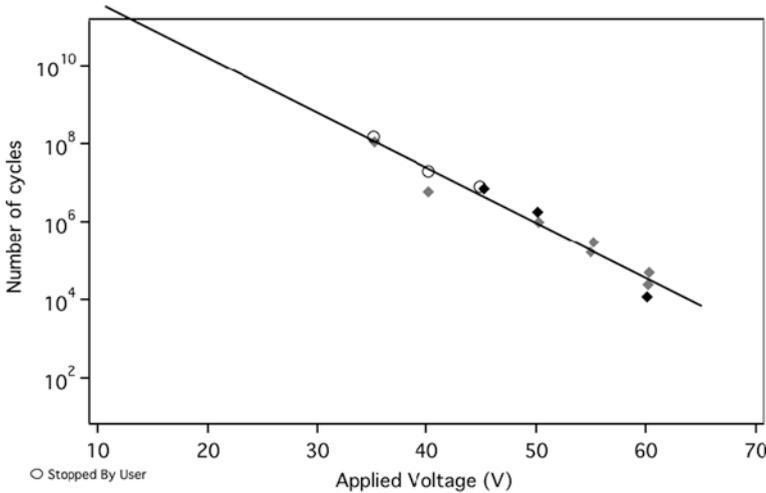


Fig. 4.52 Number of cycles to failure versus drive voltage for the switch of Goldsmith et al., showing an exponential decrease in lifetime vs. drive voltage. Adapted from [60] reprinted with permission Copyright 2001 IEEE

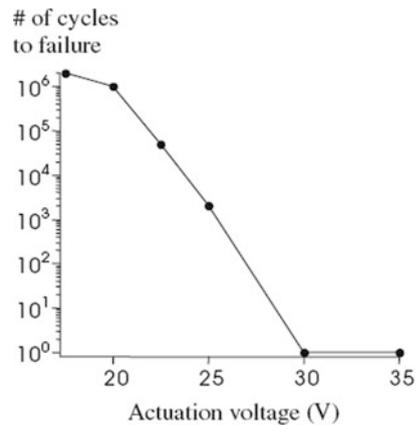


Fig. 4.53 Number of cycles to failure versus drive voltage for the switch of van Spengen et al., showing a roughly exponential decrease in lifetime vs. drive voltage. Adapted from [59] reprinted with permission Copyright 2004 IOP

dependence on the square root of the voltage of the Frankel-Poole leakage current (see [equation 3.1](#)).

Van Spengen et al. developed a model for the time to failure:

$$t = -\tau e^{aV} \ln \left(\frac{\sigma_{\text{critical}}}{N_0 q} - 1 \right)$$

where V is the drive voltage, σ_{critical} the critical charge density at failure, N_0 the total trap density in the dielectric, q the electron charge, and τ the charging time constant, a is a constant. N_0 and τ depend on the dielectric, and σ_{critical} depends on the switch design (geometry and materials mechanical properties). This model allows the lifetime to be predicted for different geometries and materials.

In view of the data above there are several possible solutions to increase the lifetime of RF MEMS switches that are failing due to dielectric charging.

- Use a dual voltage drive (unipolar, see [Fig. 4.54](#))
- Use a bipolar drive (but power hungry)
- Design for lower voltage operation
- Change the dielectric to one with fewer trapped charge
- Modify the dielectric geometry (e.g., dielectric posts instead of a film) [[56](#)]
- Modify the electrode geometry (e.g., separate RF and DC electrodes)

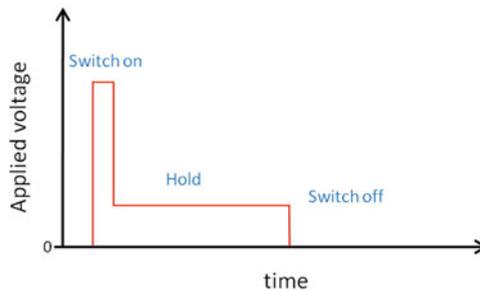


Fig. 4.54 Typical 2-level voltage drive scheme for an RF switch: first a high voltage pulse (30–80 V, lasting of order 1–100 ms) is applied to ensure the device has switched. Then a much lower holding voltage is all that is needed to keep the switch in the “down” state

All the changes imply a performance penalty, or a more complicated fabrication sequence. For instance, replacing the dielectric film with an array of dielectric posts as implemented by MEMtronics significantly reduces the total trapped charge, but also reduced the “on”-state capacitance, degrading switch performance.

Redesigning switch to work at a lower voltage is not trivial, though very appealing in view of the 10 fold increase in device lifetime (number of cycles, proportional to operating time for a given frequency) for every 5–7 V reduction in drive voltage [[59](#)]. More compliant springs reduce the actuation voltage but increase susceptibility to self-actuation, stiction, and vibration and shock. A larger electrode area also

reduces the actuation voltage but takes up more chip real-estate, and requires larger membranes where residual stress and stress gradients can deform the membrane. A smaller gap reduces actuation voltage but also increases the off-state capacitance, and reduces maximum power handling due to self-actuation.

The generally implemented solution is to use a so-called dual pulse actuation waveform: apply a voltage larger than the pull-in voltage for the first 2 ms to actuate the device, then apply a much lower voltage (possibly only a few volts) to hold down the switch for the ms to hours or days that the switch is required to stay in the down position, as illustrated in Fig. 4.54. This solution allows keeping the stiff geometry with its associated performance benefits (large restoring force, high switching speed), but greatly minimizes the charge injection since the device is usually operating at the much lower hold voltage. The driver electronics are slightly more complicated, but this is not an important issue since the main cost driver in the control electronics for such switches is the charge pump required to get the 50–80 V needed for actuation.

One could also replace the dielectric with one that has fewer charge traps (e.g., SiO_2 instead of SiN_x). One must be careful with such a solution because the time constants may be significantly longer for oxides than for nitrides, but also because one pays a price in terms of possibly lower dielectric constant, and hence lower performance than due to lower capacitance. An important driver in this case is process compatibility: high-quality oxides are challenging to grow on metallization, nitrides are often chosen for ease of process integration. MEMtronics has reported switching from SiN to SiO , with an order of magnitude reduction in surface charging [56, 61].

MEMtronics obtained an important increase in lifetime (but at the expense of slightly reduced $C_{\text{on}}/C_{\text{off}}$ ratio) by etching the sputtered SiO dielectric to form an array of pillars rather than a continuous film (see Fig. 2.37).

Finally one should mention that RF MEMS switches must generally be hermetically sealed to reach an acceptable lifetime, to avoid charge accumulation due to moisture and stiction. Humidity play an important role in surface charging, and has led to nearly all RF MEMS switches adopting a wafer-level packaging.

4.3.2 Electrical Breakdown and ESD

We shall distinguish between electrical breakdown through a solid dielectric (e.g., an insulator such as silicon nitride or silicon oxide film) and through a gas (e.g., arcing between neighboring electrodes). We shall also distinguish between electrical breakdown due to the sudden voltage and current pulse from an electrostatic discharge (ESD) event, and the lower but longer-lasting voltage from the normal drive signal for a MEMS device.

These distinctions lead to the organization of the section: first discussing breakdown through a gas, then through a solid, and finally the effect of ESD discharge on MEMS, for which the mechanical time constant is generally much longer than the pulse duration.

While the failure modes described here can be applied to any MEMS actuation or sensing principle, electrical breakdown occurs principally for the electrostatically operated MEMS devices, since electrostatic actuation often requires voltages of order 100 V.

4.3.2.1 Electrical Breakdown in a Gas for Micron-Scale Gaps

Electrodes for electrostatically operated MEMS are often spaced by as small gap as is possible given the fabrication technology. This is in particular true for comb drives where the electrostatic force scales inversely with the gap between comb fingers, with gaps of order $2\ \mu\text{m}$ being common with actuation voltages up to 200 or 300 V.

One can distinguish several types of breakdown between two conductors [62] due to: (1) stressing of the electrode surface (also known as vacuum breakdown, related to vaporization of the electrode, i.e., vapor arc), (2) insulator breakdown (internal or external flashover), and (3) via the gas path (Paschen curve, i.e., avalanche ionization).

For MEMS, the Paschen curve (described below) was thought to provide a good description of breakdown. However, the limitation of the Paschen curve at micron-scale gaps at atmospheric pressure have become clear in the past few years [63–68]. The importance of the role of field emission and vapor arc have been demonstrated for gaps smaller than 10 microns, leading to the description of the “modified” Paschen curve, as discussed initially in [66], and illustrated in Fig. 4.55, plotting breakdown voltage vs. gap at fixed pressure of one atmosphere. The general conclusion has been that a maximum safe voltage is 300 V for gaps 4 microns or larger at a pressure of one atmosphere, and that the breakdown voltage decreases rapidly for smaller gaps. We return to these conclusions after a discussion of the Paschen curve.

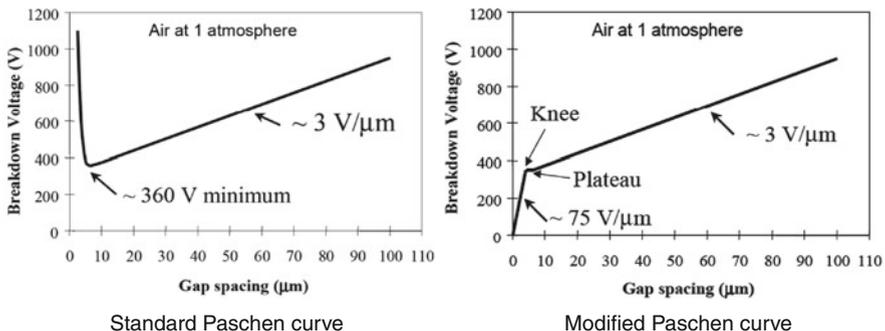


Fig. 4.55 (left) Theoretical Paschen curve in air at one atmosphere, plotting breakdown voltage vs. gap. (right) modified Paschen curve, showing a reduction in breakdown voltage (absence of vacuum isolation) at μm -scale gaps. From [66] reprinted with permission Copyright 2003 Society of Photo Optical Instrumentation Engineers

In 1889, F. Paschen published a paper [69] which laid out what has become known as Paschen's Law. This law expresses the breakdown voltage V_{bd} of a dielectric gas as a function of the reduced variable $P_{red} = P \cdot d$, where P is the pressure and d is the gap between the two electrodes. His work was developed to understand the breakdown voltage between large metal plates at low pressure with macroscopic gaps.

Later work by J. Townsend [70] led to the understanding that the breakdown is an avalanche effect caused principally by the ionization of gas molecules by electrons accelerated by the electric field. If the electron gains sufficient energy between collisions to ionize gas atoms or gas molecules, then each collision gives rise to two electrons and an ion, allowing an avalanche effect eventually resulting in a spark. This avalanche can only occur when there are sufficient gas molecules between the electrodes, i.e., if the mean free path between collisions λ is much smaller than the distance d between electrodes: when $\lambda \ll d$. If the pressure is too low, or if the gap is too small, the avalanche breakdown (Townsend theory) cannot take place.

This absence of atoms or molecules is what gives the minimum in the Paschen curve. At large gaps or pressures, a linear relation breakdown voltage and electrode gap is found (reflecting the constant breakdown electric field of the gas), while at very small gaps one has a "vacuum isolation", where there are not enough gas atoms or molecules for the avalanche to occur. Another way to look at the breakdown is to consider the electron mean free path $\lambda_{electron}$ in the direction of the applied field. Like λ , $\lambda_{electron}$ scales inversely with the pressure (neglecting the Ramsauer effect) and so the product $P_{red} = P \cdot d$ is proportional to $d/\lambda_{electron}$, giving an indication of the number of collisions an electron undergoes when crossing the gap. The breakdown voltage V_{bd} then simply depends on the $P \cdot d$ product, all parameters except gap and pressure being fixed.

Later work led to the understanding that the Paschen curve also depends on secondary electrons emitted from the negative electrode when impacted by the positive ions. These electrons further accelerate the breakdown process. The secondary electron yield, γ depends on the cathode material. The Paschen curve can be obtained by computing the voltage required for the process of electron emission and multiplication to become self-sustaining [71]. One obtains:

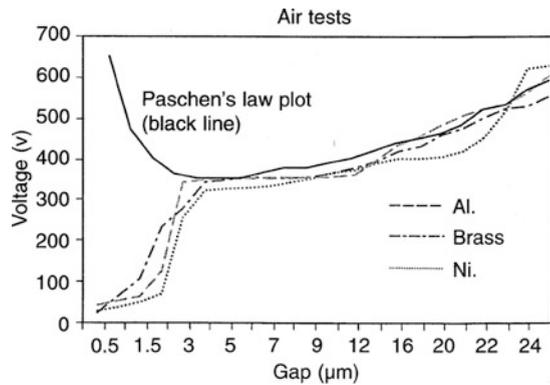
$$V_{bd} = \frac{B \cdot P \cdot d}{\ln(A \cdot P \cdot d) - \ln\left(\ln\left(1 + \frac{1}{\gamma}\right)\right)} \quad (4.11)$$

where A and B are properties of the gas, and γ is a property of the electrode material.

The Paschen curves were developed for macroscopic electrodes at operating pressures from a few Pa to one atmosphere. The generality of the scaling of V_{bd} with P_{red} led researchers to apply it to MEMS devices operating in a variety of gases at one atmosphere, for which a minimum breakdown voltage of order 360 V is predicted at a spacing of 8 microns (the exact voltage and minimum gap depend on the gas). This seemed like great news: regardless of design, the breakdown voltage in air at one atmosphere would be greater than 360 V.

Yet as reported in [63, 64, 67, 68], when the gaps are less than 10 μm for micro-machined structures operated at laboratory air at one atmosphere ($P_{\text{red}} < 1 \text{ Pa}\cdot\text{m}$), important deviations are seen from the Paschen curve. This regime is one where the mean free path is of order the gap, and thus where the Townsend breakdown cannot occur. Other types of breakdown are however possible. As presented for instance in [66] and in [68], field emission can become important at gaps order 5 microns, leading to a “modified” Paschen curve, which agrees with the “standard” Paschen curves at gaps larger than 10 microns ($P_{\text{red}} > 1 \text{ Pa}\cdot\text{m}$), exhibits a plateau of constant V_{bd} between 4 and 10 microns, and a linear drop in V_{bd} at lower gaps. Field emission can lead to local heating at micro-asperities on the surface the cathode, with in turn facilitates field evaporation of the cathode, leading to a cloud of atoms and ion in which an avalanche breakdown process can start [72]. Figure 4.56 shows data from Torres and Dhariwal for metal electrodes in air for gaps from 0.5 to 25 μm [73].

Fig. 4.56 Measured breakdown data for metal electrodes in air at one atmosphere, clearly showing the modified Paschen curve behavior [73]. With kind permission from Springer Science+Business Media: Microsystem Technologies, Volume 6, Number 1, November, 1999, pp. 6–10, Torres et al., Fig. 3



In addition to the nature of the gas (reflected in the constants A and B of equation (4.11)) and the nature of the electrode (in the form of parameter γ), relevant parameters that must be taken into account are the mean free path of gas atoms species, the surface roughness (which has a strong influence on the field emission), work function of the electrode, and the overall geometry of the electrodes, especially for planar geometries as found in MEMS and integrated circuits, which do not match the conditions of uniform electric field for which the Paschen curves were developed.

Different authors report in differences in the detailed behavior of breakdown voltage at small gaps. This is probably due to the dependence on electrode material, as mentioned above, and on surface cleanliness, which plays a large role. Nevertheless, one can roughly define a safe operating region for MEMS devices at one atmosphere, as illustrated by Strong et al. in Fig. 4.57. If one needs to operate above 300 V for gaps below 2–4 μm , careful testing must be done to ensure arcing or breakdown will not occur.

It is well known that different gases have different breakdown voltages, with the minimum in the breakdown voltage occurring at different reduced pressures (or, if operating at one atmosphere, at different gaps sizes) Of the commonly used gases,

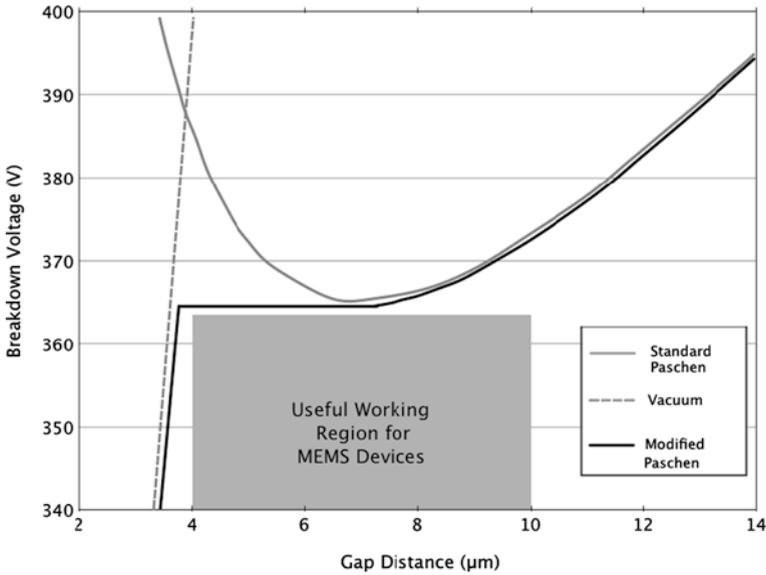
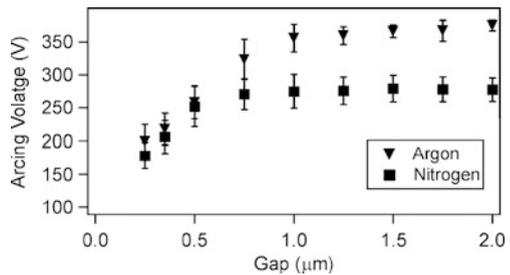


Fig. 4.57 Standard Paschen curve, modified Paschen curve, Vacuum breakdown curve, and safe operating region for MEMS for air at one atmosphere. Adapted from [68]. Reprinted with permission Copyright 2008 IOP

Neon and Helium have one of the lowest breakdown voltages, while Nitrogen has one of the highest. This is important when choosing the atmosphere for hermetically packaged MEMS, since a partial pressure of Helium is often used to aid in leak detection. Shea et al. showed that the breakdown voltage between polysilicon electrodes with gaps between 1 μm and 2 μm can be nearly 100 V higher in Nitrogen than in Argon [49], see Fig. 4.58. Ensuring sufficient margin to avoid arcing during device operation therefore requires careful selection of the packaging gas.

While most work on breakdown in small gaps serves to determine safe operating conditions for MEMS in air at one atmosphere, some MEMS devices operate at lower pressures, and thus have a different modified Paschen curve than the one

Fig. 4.58 Breakdown voltage vs. gap for polysilicon electrodes packaged under 1 atmosphere of argon and of nitrogen, showing the larger operating voltage possible with Nitrogen [49]. Reprinted with permission Copyright 2004 IEEE



discussed above. The motivation may be micron-scale plasmas, in which case one generally seeks to minimize the breakdown voltage, or actuation in low pressures (e.g., MEMS scanner to be used on Mars) where one seeks to maximize the breakdown voltage. Carazzetti et al. [74] report on breakdowns in micron scale gaps for pressures between 1 and 800 mbar, and find for low pressures deviations from the Paschen curve for gaps even as large to 500 μm , which they explain principally by the planar geometry of typical interdigitated electrodes, that leads to the superposition of several Paschen curves and hence to a large flat region in the breakdown voltage vs. reduced pressure curve. They conclude that pressures well below 1 atmosphere, care must be taken when applying the Paschen formula to gaps on the 2–100 μm range, while for operation at 1 atmosphere Paschen behavior is observed for gaps larger than 10 μm .

4.3.2.2 Electrical Breakdown Across Solid Dielectrics

Electric breakdown across insulators is generally a two step process: (1) *wear out*: accumulating enough damage in dielectric to create a conductive path, followed by (2) Thermal damage from high current flow (*thermal runaway*).

In this simplified model, during the wear out phase, charge traps and defects accumulate in the dielectric and at the interface between conductor and dielectric. When the defect density reaches a critical level, the resistivity of the insulator plummets, a large current flows, and the device fails due to localized Joule heating.

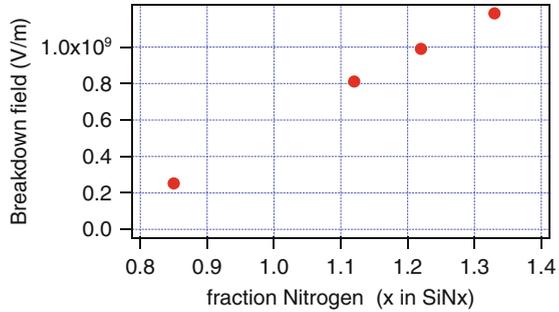
Breakdown is extensively discussed in the semiconductor literature, for instance in ref [53]. The key concept is that of a critical charge to breakdown: Q_{BD} , with the assumption that the defect density increases linearly with current flowing through the insulator. It is for this reason that the leakage current through the dielectric is a key factor for dielectric breakdown. We discussed leakage current through dielectrics in the section on charging (Section 4.3.1.1), and refer the reader back to the section for discussion of leakage through oxide and nitrides.

The critical charge to breakdown concept is really shorthand for describing a critical defect density N_{bd} , above which the resistance of the device decreases markedly, leading to failure.

At first glance, for MEMS devices we are generally dealing with the same dielectrics as in the integrated circuit world. However there are two important differences: (1) the voltages may be higher than in typical CMOS, and (2) the insulator films used for MEMS often have compromised electrical properties to achieve better mechanical properties. The most common example is the silicon rich SiN film used in the poly-MUMPS (MEMSCAP Inc.) process. In order to minimize stress in the silicon nitride film, the film is made silicon rich. This leads to much higher leakage currents through the dielectric, and to lower breakdown voltages. This is well described in [49].

The reduction in breakdown voltage for SiN thin films is shown in Fig. 4.59 from stoichiometric $\text{SiN}_{1.33}$ to silicon-rich $\text{SiN}_{0.85}$ (based on experimental data in ref [75]).

Fig. 4.59 Breakdown electric field for SiN_x films of different Silicon volume fraction. Determined from data in Fig. 2 and in Table 1 of [75]



4.3.2.3 ESD and EOS

Electrostatic Discharge (ESD) is a sudden transfer of charge between two objects, for example between a MEMS device and either a person handling the device, or a piece of equipment. Electrical overstress (EOS) is very similar, but occurs at lower voltage levels. Voltage pulses of kilovolts are typical for ESD, while EOS occurs generally at tens to hundreds of volts. EOS often occurs because the device was incorrectly wired, or incorrectly inserted into a socket; the voltage comes from a power supply. ESD in contrast generally occurs during handling: a person walks on a carpet in a dry environment easily charging up to 20 kV on a dry winter day and then touches the pin of an electronic device, discharging through the device.

An ESD event typically has large voltages (kV) occurring in a short pulse (10 ns risetime, 150 ns decay) and with a large current (>1 A). Tribo-electric effects are an important cause of ESD as they result in static charge buildup: either charging of a human, or friction between a chip and the plastic tube from which it is being removed. While protection for CMOS and bipolar ICs is well established (see e.g., ref [76]), the literature is much sparser for MEMS. The first report of ESD on MEMS was by Walraven et al. in 2000 on Sandia's micro-engines [77]. There have been a number of reports on RF MEMS switches [78, 79], as well as a report on micro mirror arrays [80]. The reports generally agreed that MEMS devices can be very susceptible to ESD, and that suitable handling precautions must be taken.

An ESD event can cause both electrical and mechanical damage. Electrical damage includes: destroyed transistors, melted wires, weakened dielectric layers (hidden damage), evaporated electrodes, charge accumulation in dielectrics. Mechanical damage generally appear to be stiction failures, where surfaces not designed to come into contact collide due to a sudden much static force possibly sticking using or breaking.

The two most common models used to simulate ESD events are the human body model (HBM) and the machine model (MM). The human body model simulates the discharge occurring when a person handles a device, while the machine model simulates a more rapid and severe electrostatic discharge from a charged machine, fixture, or tool (i.e., a metallic connection rather than through a poorly conducting finger). HBM simulates a person as a 100 pF capacitor that discharges through a 1.5 kΩ resistor, while MM simulates a machine as 200 pF capacitor discharging

this capacitor directly into the device being tested through a 500 nH inductor with no series resistor.

The rise time of the HBM ESD pulse, is between 5 and 9 ns, with a decay of order 150 ns. For a 400 V pulse, the current is 0.3 A. The rise time of the MM ESD pulse, is similar to HBM 6–8 ns, but the peak current at 400 V is 6 A, 20× greater than for HBM.

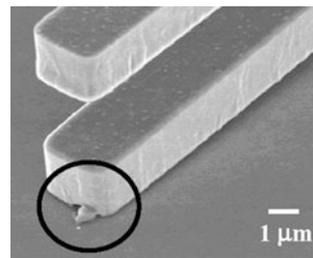
The timescales of these pulses are important because they must be compared to the typical resonant frequencies of MEMS devices. The reasoning here is similar to the one for shocks (see Section 4.2.2.2 in this chapter). The duration of the voltage pulse is much shorter than the typical mechanical response time of a MEMS device (at least for larger MEMS where stiction or impact is an issue; MEMS resonators can have GHz resonance frequencies, but are so stiff that electrostatically induced motion will not lead to failure), so the mechanical response of the MEMS device is that of an impulse: the device acts as if it had initial velocity given by the integral the acceleration pulse, and the dynamics of the device then simply follow from its resonance frequency and damping.

MEMS failure from ESD is often a combination of electrical and mechanical modes. Pure electrical failure has been reported, where the ESD pulse led to the breakdown of an insulator, or the evaporation of an electrical lead. Tazzoli et al [79] applied ESD pulses to RF switches and when applying the pulse along the signal line observed failures due to electromigration and electrically-open vias. When applying the ESD pulse between ground and the actuator, the observed sparking between the lines leading to failed leads. For both these cases the failures were not due to mechanical motion of the device.

Walraven et al. [77] report a number of failure modes, which involve a combination of electrical and mechanical failures following HBM and MM testing. Principally they observe that the ESD pulse leads to mechanical motion of a beam (comb finger in their case), which then comes into contact with a conductor a different potential, and fuses or “spot welds” (Fig. 4.60). They also report on comb fingers getting stuck on surfaces without any potential difference (stiction). So while the failure mode may appear to be stiction the root cause is the motion imparted by the voltage pulse. Failures occur at voltages less than twice the normal operating voltage.

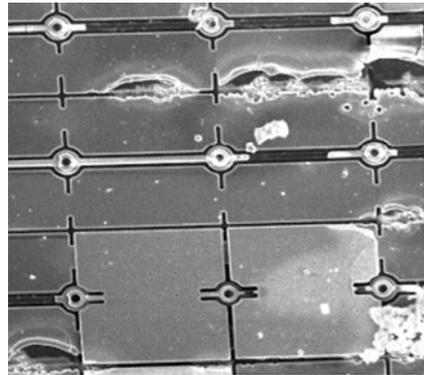
A group from IMEC reported HBM and MM the ESD testing of arrays of polycrystalline Silicon Germanium micro mirrors [80]. The main failure mode if

Fig. 4.60 Polysilicon comb finger welded to ground plane following 150 V ESD pulse (black circle around the weld) [77] Reprinted with permission Copyright 2000 Society of Photo Optical Instrumentation Engineers



they observe is irreversible pull-in, i.e., stiction or welding of the mirror in its completely tilted state. This occurs because under overvoltage conditions the mirror tilts and touches the actuating electrode, to which it then welds. This occurs at 40 V, which is only three times larger than the normal actuation voltage. ESD discharges at such low voltages can occur extremely easily, and would not be noticed by a person handling the device. Figure 4.61 illustrates an extreme case of mirrors being melted or blown off following an ESD pulse. This is explained by Joule heating due to the very large currents flowing through the mirrors. An interesting observation from this group is that HBM and MM discharges give very similar failure levels, which is never the case for CMOS devices. The high impedance of the electrostatic MEMS devices explains the very similar response to HBM and MM pulses. Such a device would require ESD protection being implemented in the drive circuitry, and will require very careful handling to avoid ESD damage.

Fig. 4.61 SiGe micromirror array, showing extensive damage following ESD pulses up to 120 V. Mirror dimensions: $16 \times 16 \mu\text{m}^2$ [80]. Reprinted with permission Copyright 2008 ESD Association



Short of implementing protection diodes, design changes can be made to MEMS devices to make them less sensitive to ESD. Electrical failures can be addressed by using a wider spacing between leads increases the voltage required for arcing, and wider leads that can tolerate larger currents before failing. Mechanical failures can be minimized by making the devices stiffer. Electromechanical failures can be mitigated by ensuring that moving parts only land on parts at the same potential, for instance an electrostatically actuated micromirror should have landing pads that are at the same potential as the mirror, and not land directly on the actuating electrodes.

These mitigation strategies all of course come at a cost, for instance higher actuation voltage for stiffer devices, or more complex electrode design. Trade-offs needs to be made between reliability, process complexity, and operating conditions.

4.3.3 Electromigration

Electromigration is the migration of metal atoms under an applied electric field. One must distinguish electrolytic (metal ions in solution) from solid-state (atom

motion in a metal wire or trace due to electron momentum transfer) electromigration (EM) [81]. Electrolytic EM occurs generally on the printed-circuit board level when sufficient moisture is present to allow surface conduction between neighboring conductors by ionic transport, leading to failures by dendritic bridging. Solid state EM occurs in microfabricated wires, in which the momentum from electrons can cause atomic displacement of the conductors when the current density and temperature are sufficiently high, leading to voids and dendrites. Solid-state electromigration is an important failure mode for microelectronics in view of the very high current densities ($>10^{10}$ A/m²) in IC circuits, and does not depend on ambient moisture.

We shall not cover electrolytic electromigration in this book, as it occurs mostly for silver under non-condensing conditions. It can occur for all metals when visible moisture is present, but we shall not consider this as a MEMS specific failure. In what follows we shall focus on solid-state electromigration, which has been a reliability problem in integrated circuits for over 40 years.

Because of the excellent thermal conductivity of silicon compared the substrates generally used for printed circuit boards or chip carriers, much higher current densities are possible in the thin-film interconnects of typical IC than in electrical motors or on printed circuits, with current densities of over 10^9 A/m² being common. The conventional physical explanation for electromigration is that the “electron-wind” force at high current densities transfers sufficient momentum to metal atoms to lead to a net mass transport.

Current-density driven electromigration results in momentum transfer to atoms with atom movement in the direction of the electron wind, which is opposite of the current flow. Thus voids will form where the where the electrons are injected, and hillock of metal atoms will accumulate where electrons are extracted. The grain structure plays a very important role in EM rates because diffusion of metal ions is roughly 6 orders of magnitude larger along grain boundaries than through bulk metal. Thus “bamboo” structure (interconnects only 1 grain wide) can carry significantly more current before showing failure due to EM than a wire several grains wide.

The accelerating factors for electromigration are: current density, temperature, and stress in the films. Temperature is accounted for in the typical Arrhenius manner, see [Chapter 2](#). Black [82] is credited with the following equation:

$$\frac{1}{MTTF} = Bj^2 \exp \left[-\frac{E_a}{k_b T} \right]$$

where j is the current density, E_a the activation energy, k_b the Boltzmann constant, T the temperature and B a fitting parameter. For very high current densities the exponent of the current increases from 2 to larger values. The activation energy depends on metal species, as well as on grain size and purity. Typical values range from 0.4 to 1 eV, with 0.7 eV often used for typical Al-Cu IC interconnects. EM is well covered in IC reliability books, the reader is referred for instance to “Reliability and Failure of Electronic Materials and Devices” by M. Ohring for a more detailed

discussion [53]. Much work has been reported on different metallizations to increase lifetime due to electromigration. Copper was added to Al to exceed the solid solution concentration for precipitation at the grain boundaries, (θ phase precipitates), and reduce surface energy. Ti-based underlayers can increase lifetime by an order of magnitude. When copper interconnects were introduced as a lower resistance alternative to Al-Cu, lifetime increased as copper can handle much higher current densities.

For integrated circuits such as microprocessors, EM can be a leading failure cause. For most MEMS devices, which do not have parts with high current densities, EM is not a critical issue. However for micromachined hotplates, used for instance in gas sensors, infrared emitters or membrane-type microreactors, EM can be an important failure mode. It can also be observed in thermal actuators. Micro-hotplates consist of metal traces usually on a low-stress silicon nitride membrane to minimize thermal losses, and can operate at temperatures as high as 400°C. Electromigration occurs at the points of highest current density, or more correctly EM damage accumulates in areas of “flux divergence”, where geometry or film thickness changes quickly. Figure 4.62 left is a top view of a micromachined hotplate [83], and Fig. 4.62 right is a SEM image following accelerated aging tests at 120 mW. The voiding due to EM is clearly seen. Lifetime can be increased by careful choice of metal and grain size.

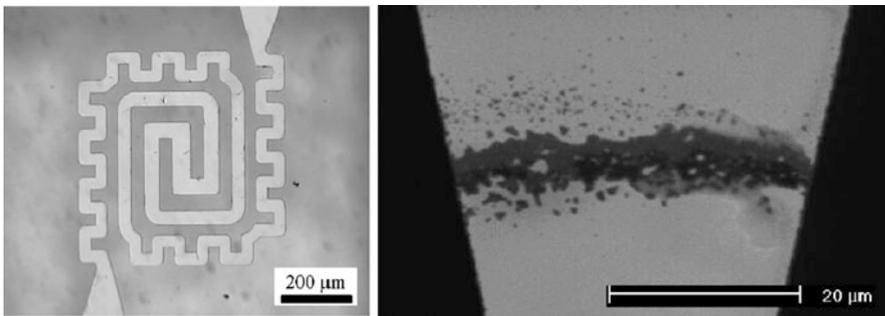


Fig. 4.62 230 nm thick Pt heater on a 250 nm thick low-stress silicon nitride membrane. *Left*, optical micrograph. *Right*, SEM image after operation under accelerated conditions, showing voiding due to EM. Adapted from [83] reprinted with permission Copyright 2008 Elsevier

4.4 Environmental

The failure modes in this section involve degradation due to factors external to the MEMS device. Packaging plays a particularly crucial role when dealing with the interplay between environment and device. We shall address first the effect of radiation on MEMS, then anodic oxidation and galvanic corrosion of poly-silicon, as examples of MEMS-specific corrosion issues. Finally metal corrosion due to airborne humidity or ionic contaminants or atmospheric pollutants is covered as an issue affecting all microelectronic devices.

4.4.1 Radiation

This section is largely based on [91], to which the reader is referred for more details, in particular for different possible applications of MEMS on spacecraft (inertial sensing, propulsion, etc), also discussed in [133]. For reliability issues specific to operation in space, the reader is referred, for example, to [85], [86], and [132]. Qualification procedures for Space are discussed in Section 6.5.3.

Considerable effort has been expended over the past 50 years to devise techniques to test the suitability of electronics components for use in high-radiation environments, as well as design techniques to develop radiation tolerant electronics and optics. The physics of how different energetic particles interact with matter, the types of damage that are caused, and the influence on most electronic devices, optical components, and mechanical parts is well understood [87], and there exist well established test procedures for space applications, for instance [88] and [89]. Due in part to the relative immaturity of the MEMS field, but primarily due to the vast range of materials, technologies and applications that MEMS cover, there is no standard test procedure for the effect of radiation on MEMS, though there are some proposed approaches [85].

Even at the high end of space mission doses, the mechanical properties of silicon and metals are mostly unchanged (Young's modulus, yield strength not significantly affected). Silicon as a structural material can be viewed as intrinsically radiation hard. This makes most MEMS devices mechanically radiation tolerant by default. For MEMS devices operating on electrostatic principles, the main failure mode is the accumulation of charge in dielectric layers due to ionizing radiation. The trapped charge leads to device failure, for instance large changes in calibration of capacitive accelerometers, or device failure due to stiction initiated by electrostatic forces from the trapped charge. Of concern are also the drive/control electronics, which may need to be shielded or built with radiation-tolerant technologies.

4.4.1.1 Typical Doses for Space Applications

Consisting primarily of trapped electrons, trapped and solar protons, cosmic rays, and of bremsstrahlung (created when energetic particles strike the spacecraft), the space radiation environment is strongly time and position dependent. The dose received by the spacecraft (SC) thus depends by orders of magnitude on the SC orbit/trajectory, time of launch and duration of the mission. Although the radiation environment is complex, there exist excellent software tools (e.g. [90]) to model the dose and type of radiation a SC will encounter in its lifetime.

The radiation environment in space is complex, and is concisely described in [92–93]. Software models are available for the different types of radiation that can be encountered. Software packages (e.g., SPENVIS [90]) exist that combine these different models allowing rapid determination of the dose and type of radiation exposure for Earth orbits. Models also exist for deep space, but have less data to support them. The main types of radiation encountered near earth consist of:

- Trapped radiation: energetic electrons and protons magnetically trapped around the earth (Van Allen belts). They consist of electrons of energy up to a few MeV, and protons of up to several hundred MeV.
- Solar Energetic particles: mostly highly energetic protons, up to 300 MeV. The intensity varies greatly in time, especially the 11 year solar cycle, since the proton flux is associated with solar flares. UV and X-ray burst are also produced, as well as solar cosmic rays.
- Galactic cosmic-rays: continuous low flux of highly energetic (1 MeV to 1 GeV) particles, mostly protons, alpha particles, but also include heavy ions.
- Secondary radiation: radiation generated when the above radiation interacts with materials in the spacecraft, notably with shielding. Includes primarily electron-induced bremsstrahlung, but also secondary electrons, and other particles such as secondary neutrons.

The global effect of the many different types of radiation on components can be summarized by the quantity of energy deposited by the radiation. The SI unit is the Gray (1 J/kg), but the unit rad (1 rad = 10^{-2} Gray) is still in common use.

The energy deposited varies as a function of time and location of the SC. Accurate models can predict the quantity of energy deposited as a function of the trajectory. Table 4.4 gives approximate values of energy deposited in a component for a low Earth orbit (LEO) and for a geostationary orbit (GEO), without shielding and with shielding equivalent to 4 mm thickness of aluminum.

Table 4.4 Representative annual radiation doses for LEO and GEO orbits

Trajectory, shielding	Predominant particles	Dose deposited per year
LEO, outside SC	Trapped electrons	> 100 krad
LEO, 4 mm Al equivalent	Trapped protons	1 krad
GEO, outside SC	Trapped electrons	> 10,000 krad
GEO, 4 mm Al equivalent	Bremsstrahlung + solar protons	10 krad

Unshielded components obviously face a much harsher radiation environment than shielded ones. The spacecraft itself acts as a shield for components mounted internally (for a 5 tons satellite, this can be very significant shielding). The highest deposited dose is on solar panels and the external surfaces of the SC. On large spacecrafts, it is unlikely that MEMS will be directly exposed to space so that much lower radiation values will be expected (with the exception of sun sensors and thermal control louvers [94]).

Space missions typically last several years, and operate in a radiation environment with dose rates of order 1 rad/h. Testing however must be done in hours or days (dose rates from 36 rad/h to 36 krad/h are commonly used for ^{60}Co irradiation).

Despite the complexity of the actual space radiation environment, accelerated radiation testing methods have been developed using mono-energetic particles whose relevance and suitability has been amply demonstrated for microelectronic devices. There is however no standard testing procedures established for MEMS, though studies are ongoing.

4.4.1.2 Damage Mechanisms

The effect of radiation on materials is well described in several books such as [87]. We briefly summarize in this section the main degradation processes and effects on different materials to serve as a foundation for a MEMS-centered analysis in the following section.

4.4.1.3 Degradation Processes

Energetic particles and photons cause damage by transferring energy to the materials they penetrate. The energy loss mechanisms are complex, but the type of damage can be classified in two consequences: (a) atomic displacement and (b) ionization. Figure 4.63 provides an overview of the effects that radiation can have on devices.

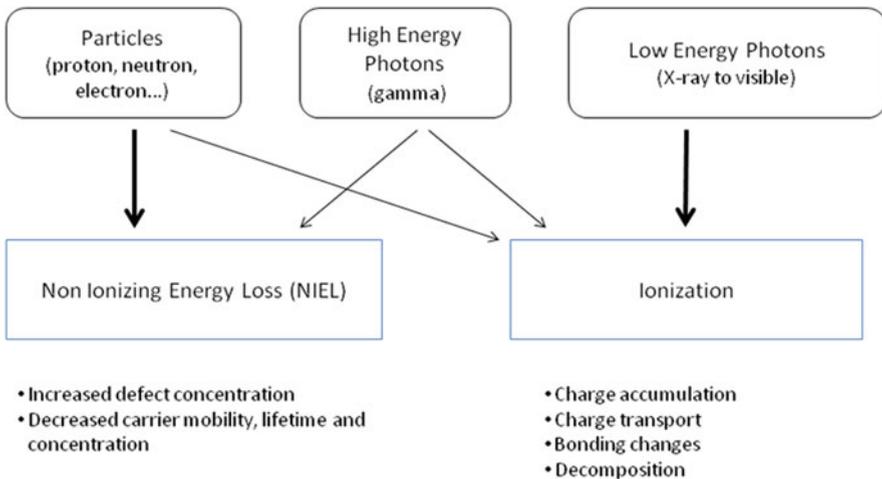


Fig. 4.63 Summary of radiation induced degradation effects, ignoring transient effects, adapted from Table 5.1 of [92]

Non-ionizing Radiation Loss (NIEL)

A fraction of the energy transferred to the target from energetic particles or even from photons results in the transfer of momentum to atomic nuclei, which can result in atoms being moved from their rest position in the lattice, leaving vacancies or

defects behind. The process of atomic displacement is referred to as “bulk damage” [87]. Even photons of sufficient energy can give rise to this non-ionizing radiation loss (NIEL), or displacement damage, component of radiation. Displacement damage dose (DDD) is defined as displacement energy per unit mass, equal to NIEL time fluence.

The most relevant consequence of displacement damage for electronic devices is the reduction in minority carrier lifetime, the reduction of carrier mobility, and the removal of carriers (by interaction with defects). The damage caused by most particles is of the same general type.

Ionization

Most of the energy lost from radiation interacting with an absorber is ultimately converted to electron-hole pairs (the energy required is only 18 eV for SiO_2). Electrons and holes have very different mobilities. The electrons and holes increase the conductivity of the sample (even of insulators), and the holes can become trapped in insulators (SiO_x , SiN_x), leading to serious degradation of MOS and MEMS devices. This Total Ionizing radiation Dose (TID), defined as the Ionization energy per unit mass, leads to an accumulation of electrically active defects. The biasing of a sample is important because the electric field from the bias will drive the electrons and holes, and thus change the effect on the device of ionizing radiation. This will be seen below to be the driving factor in the radiation tolerance of MEMS.

Single Event Effects (SEE)

Single Event Effects are not a damage mechanism, but are an important consequence in microelectronics circuits of the effect of energetic particles, including Single Event Upsets and Single Event Latch-ups, which we do not discuss them further as they do not apply to MEMS devices (but do apply to the control/sense electronics).

4.4.1.4 Degradation Effects

The consequences of damage depend on whether the damage is due to atomic displacement or to ionization, whether the effects are transient or long-lived, and what type of material absorbed the radiation (we will distinguish between metal, semiconductor, and insulator). Additionally, one can also distinguish between changes in the mechanical vs. electrical properties of the materials.

Metals

There are no reports of important metal degradation by radiation in space [92]. In nuclear reactor cores the neutron fluxes are high enough to significantly reduce the mechanical strength of metals, or render them brittle. For space missions, metals are deemed to be radiation tolerant.

Semiconductors

Displacement damage leads to electrical and mechanical changes. The electrical changes are due to the change in minority carrier lifetime and concentration, which can have an important effect on p-n junctions (rectifiers and bipolar transistors, as well as solar cells). FET and MOS devices are much less sensitive to this effect.

Concerning mechanical changes, even at the high end of typical doses for space (Mrad), the amount of damage to silicon is rather small (defects, clusters), and the Young's modulus is not markedly changed. For electronics and packaging the effect can be ignored. For MEMS devices such as resonators, which are sensitive to ppm change in Young's modulus, further investigation is required.

Insulators

In optical materials displacement damage lead to color centers. For electronic or structural materials, displacement damage leads only to very small effects (compared to semiconductors) because dielectrics are typically glassy (amorphous), and there is thus no ordered lattice to disrupt with defects, clusters or dislocations. So the dielectric can retain its insulating properties even when a few atoms are displaced.

For dielectrics, ionizing radiation leads to both (1) direct charge injection from ionizing radiation, and (2) the creation of deeper traps and possibly more defects, thus making the dielectric even more susceptible to charging from non-radiation related sources. The influence of the trapped charge depends on the actuation scheme (electrostatic is much more sensitive), and on the geometry, such as the presence or absence of conductive shields to screen the trapped charge.

4.4.1.5 Review of Published Data on MEMS Radiation Tolerance

MEMS devices can operate on wide variety of physical principles for sensing and for actuation, the most common being electrostatic, thermal, magnetic, and piezoelectric. Other principles that are less widespread include chemical reactions, electrophoresis, and capillary force. The wide variety of materials and physical principles used make it difficult to make general statements about MEMS reliability and radiation sensitivity. Different sensing and actuation principles are shown below to very different in their radiation tolerance.

Few radiation tests have been performed on MEMS devices (less than twenty published papers), see Table 4.5 for an overview of minimum dose for failure and failure mode for different MEMS devices. Most radiation tests on MEMS have focused on the effects of radiation on the MEMS sensor or actuator, but have often been limited by failure of the electronics.

On the low-tolerance end, one finds that most electrostatically operated MEMS devices degrade between 30 and 100 krad, unless special steps are taken to shield

Table 4.5 Review of published sensitivity of MEMS devices to radiation. Failure modes are grouped below as mechanical related to displacement damage, mechanical related to ionization, and electrical due to charge trapping [84]

MEMS device	Actuation type	Minimum dose for failure	Radiation type	Failure mode	References
Analog device ADXL 150	Electrostatic (comb-drive)	27 krad (Si)	Co-60 γ	Not investigated	[97]
Analog device ADXL 150	Electrostatic (comb-drive)	Highly tolerant (no failures seen)	Infrared laser, 5.5 nJ (SEE)	Not investigated	[97]
Analog Devices ADXL 50	Electrostatic (comb-drive)	25 krad (Si)	Co-60 γ	Dielectric charging in device	[98]
Analog Devices ADXL 50	Electrostatic (comb-drive)	>50 krad (Si)	SEM localized e-beam 30 keV	Dielectric charging in device	[98]
Analog Devices ADXL 50	Electrostatic (comb-drive)	100 krad (Si)	5.5 MeV protons	Dielectric charging in device	[98]
Analog Devices ADXL 50	Electrostatic (comb-drive)	100 krad (Si)	155 MeV protons	Proton displacement in reference circuit	[98]
Analog Devices ADXL 50	Electrostatic (comb-drive)	20 krad (Si)	65 MeV protons and heavy ion	Dielectric charging in device	[99, 100]
Motorola XMMAS40G	Electrostatic	4 krad (Si)	Co-60 γ	Failure of CMOS readout circuit	[98]
Sandia microengines	Electrostatic (comb-drive)	1–100 Mrad (SiO ₂) bias dependent	2 MeV protons, 5–25 keV electrons, 10 keV X-rays	Dielectric charging	[101]
Endevco accelerometer 7264B-500T	Piezoresistive	>30 Mrad	Co-60 γ	Trapped charge, depletion of minority carriers	[102]
Kulite pressure transducers XTE-190-25A	Piezoresistive	7 Mrad to >20 Mrad, sample dependent	Co-60 γ	Trapped charge, depletion of minority carriers	[102, 103]
DSTO / Analatom Si strain gauge	Piezoresistive	10 ¹⁶ protons/cm ²	3.5 MeV protons	decrease in carrier density and mobility (NIEL)	[104]
Sercalo 1×2 optical switch	Electrostatic (comb-drive)	>22.5 krad (Si)	Co-60 γ	No failures seen	[105]
Boston Micromachines Co	Electrostatic (parallel-plate)	3 Mrad (Si)	Co-60 γ	No failure seen	[106]
Poly-Si Micromirrors array					

Table 4.5 (continued)

MEMS device	Actuation type	Minimum dose for failure	Radiation type	Failure mode	References
Rockwell Scientific Co RF switch	Electrostatic (parallel-plate)	30 krad (GaAs)	Co-60 γ	Dielectric charging in device (strongly geometry dependent)	[107]
FBK-IRST ohmic RF switch	Electrostatic (parallel-plate)	10 Mrad (SiO ₂) proton 1 Mrad (SiO ₂) X-ray	2 MeV protons 10 keV X-ray	Both NIEL and ionizing damage	[108]
VTI SCA 600 accelerometer	Electrostatic (parallel plate)	50 krad (Si)	Co-60 γ	Not investigated	[97]
VTI SCA 600 accelerometer	Electrostatic (parallel plate)	Not quantified, but low	Infrared laser, 5.5 nJ (SEE)	due to latch-up in CMOS electronics	[97]
NASA /GSFC Microshutter array	Electrostatic & electromagnetic	10 to >200 krad (Si) depending on drive voltage	Co-60 γ at 60 K	Charge trapping (dielectric charging)	[109]
Polysilicon electrothermal actuator and bimorph cantilevers	Electrothermal and CTE mismatch	> 1 Mrad (Si)	Co-60 γ and 50 keV X-ray	No failure seen	[110]
Purdue wireless microdosimeter	Electrostatic (parallel plate)	Tested up to 650 Mrad	Co-60 γ TID	No failure seen	[111]

or remove the dielectric materials so as to render the device insensitive to charge build-up in dielectric layers. Tests on accelerometers and RF switches showed a marked change in calibration at doses above 30 krad [98, 100, 107]. Those failures were attributed to trapped charge in dielectric films. These doses are for unpackaged devices so that the sensor element is directly irradiated. Similar doses on packaged devices would lead to significantly less damage.

On the other extreme, micro-engines from Sandia National Labs in Albuquerque, NM, USA were reported to only change their behavior at doses of order 10 Mrad, in some cases over 1 Grad [101]. Those devices did contain dielectrics (SiO_2 and SiN_x), but not in a geometry where charging could directly influence device operation.

Electrostatic MEMS Sensors and Actuators

For electrostatic MEMS devices the main failure mode at high radiation doses is the accumulation of charge in dielectric layers, which leads to failures as described in the earlier section on dielectric charging of this chapter. Therefore many of the same solutions to mitigate charging are applicable. While the failure may appear mechanical (e.g., a RF MEMS switch stuck in the actuated position, drift in tilt angle of an electrostatically actuated micromirror) the root cause is electrical. For a given device, total ionizing dose (TID) is the main radiation parameter that quantifies the amount of charging.

Accelerometers, in particular the monolithic comb-drive polysilicon devices manufactured by Analog Devices, which are readily commercially available, have been investigated for TID effects [98, 99, 97]. The devices operate by sensing the change in capacitance as a suspended proof mass moves in response to external accelerations. It is thus very sensitive to any static charge in exposed dielectrics, and Knudson et al. [99] showed the radiation-induced output voltage shift was due to charging of a dielectric under the proof mass. The devices tested under high energy proton and gamma-rays show degradation in the 50 krad range (ADXL 50 and ADXL 150). For similar devices where a conducting polysilicon film was placed over the dielectric (ADXL 04), thus effectively electrically shielding any trapped charge from the active device, no radiation induced degradation was observed up to a dose of 3 Mrad [99]. The XMMAS40G accelerometer from Motorola tested by Lee et al [98] failed after only 4 krad. It is proposed that the failure is due to failure of the CMOS output circuitry rather than the sensor element.

SOI bulk micromachined accelerometers from VTT, Finland, operating by measuring the capacitance between suspended parallel plates were subjected to gamma-rays, and failed at 50 krad [97]. The sensor was packaged with a readout-ASIC, which was found to latch-up at low doses of infrared laser pulses. It was not determined if the failure at 50 krad was due to the sensor or the ASIC. A non-monolithic approach (i.e., separate sensor and readout/control ASIC chips in one package) is an appealing approach to rapidly developing radiation tolerant sensors, as it allows choosing a radiation-tolerant ASIC (an easier task since

radiation hard CMOS technology is mature), and focusing the research solely on radiation-hardening the MEMS component.

Comb-drive actuators carefully designed with no exposed dielectric between or under moving parts (such as the Sercalo Microtechnology 1×2 optical switch [105] or the Sandia microengines [101]) have been shown to operate with no change after doses of more than 20 krad and 10 Mrad respectively.

Capacitive RF MEMS switches require a dielectric film to separate a fixed electrode from movable membrane. An RF switch from HRL Laboratories was successfully operated dynamically up to a dose of 1 Mrad [112]. RF switches from Rockwell Scientific Company reported in [107] showed no change in static characteristics at doses of up to 150 krad for design specifically developed to reduce dielectric charging. For a more conventional design, the device's calibration started to change at doses of 10 krad, although the device continued to operate after doses of 300 krad, but with an 80% increase in required drive voltage. The difference in dose required for degradation between the two devices is due to the (unspecified) different location of the dielectric layers. The configuration that is more radiation-tolerant has no dielectric between the moving parts.

Non-electrostatic MEMS Actuators

A piezoelectric mirror array developed by JPL and Pennsylvania State University based on PZT (lead-zirconate titanate) was functional up to 1 Mrad, but at 20 krad started exhibiting changes in mirror deflection compared to unirradiated samples, as well as an important increase in leakage current though the PZT [106]. The authors developed a model attributing the change in device characteristics to charge trapped in the PZT film.

Polysilicon thermal actuators and gold/polysilicon bimorph cantilevers were investigated by Caffey et al. [110] under ^{60}Co gamma-rays and 50 keV X-rays. No degradation of the devices was observed at 1 Mrad, the maximum dose used. This is in line with the understanding that electrothermal devices are for the most part insensitive to dielectric charging, as long as there is no exposed dielectric near the active element.

Piezoresistive Sensors

The radiation sensitivity of micromachined piezoresistive silicon accelerometers and pressure sensors are reported in [102, 104, 103, 113]. In all cases, an increase in resistance of the piezoresistive elements are observed. Marinaro et al. [104] find a nearly linear relation between the resistance of the piezoresistor in their single-crystal silicon strain gauge and the fluence of 3.5 MeV protons. They observed changes for fluences of the order of 10^{16} cm^{-2} , corresponding to roughly 10 years in MEO (Medium Earth Orbit). They attribute the increase in resistance to the NIEL component of the radiation, leading to majority charge removal due to displacement damage serving as trapping centers, and to a reduction in carrier mobility.

Holbert et al. [102] and McCready et al. [103] studied the response of piezoresistive MEMS accelerometers and pressure sensors to high gamma-ray doses and pulsed neutrons. They observed a gradual shift in output of Endevco 7264B-500T accelerometers with gamma-ray doses up to 73 Mrad, with no catastrophic failures, and were able to recalibrate the devices post-irradiation. Results were less consistent for Kulite XT-190-25A pressure transducers, with two devices failing suddenly at 7 and 25 Mrad, and four others still operating at after 20 Mrad, with a shift in output voltage. Holbert et al. [102] correlate the increase in resistance of the piezoresistors to the formation of trapped hole charges. They show how this trapped charge in oxide layer surrounding the piezoresistor can induce a depletion region in the semiconductor, thus increasing the device resistance. They conclude that n-type piezoresistors with the largest cross-section will be the most radiation tolerant, though there may be a tradeoff of sensitivity vs. radiation tolerance.

4.4.1.6 Suggestions for Radiation-Hardening MEMS

The difference in sensitivity of MEMS devices to radiation is due primarily to the different impact that trapped charge in dielectric layers has on different actuations schemes and geometries. MEMS operating on electrostatic principles are the most sensitive to charge accumulation in dielectric layers. In contrast, thermally and electromagnetically actuated MEMS are much more radiation tolerant. MEMS operating on piezoresistive principles, while not showing any threshold for radiation sensitivity, do not fail catastrophically until doses of several Mrad are exceeded.

Techniques that eliminate or minimize charging effects were discussed in the section on charging above, and as discussed in the RF MEMS case study in [Chapter 2](#), include:

- Ensuring that all conductors be at well-defined potentials and not be allowed to float to avoid undesired electrostatic forces (due to charging of conductors)
- Change of dielectric material to one with lower trap density, see e.g. [114].
- Adding a charge dissipation layer on the dielectric [49].
- A geometry change to eliminate the dielectric from between moving surfaces, and from under moving surfaces.
- A geometry change to minimize the exposed area of dielectric, or replacing the dielectric films with arrays of dielectric posts [56]
- A geometry change to reduce the sensitivity to trapped charge, e.g., stiffer restoring springs.
- Electrical shielding, by covering exposed dielectric with a conductor as at well-defined potential, as in [99].

Since electrothermal and electromagnetic actuation principles are intrinsically more radiation tolerant than electrostatic operation, these actuation principles should be considered for applications where high radiation doses are expected.

4.4.2 Anodic Oxidation and Galvanic Corrosion of Silicon

4.4.2.1 Origin of Anodic Oxidation

Because of its electrical and mechanical properties as well as its relative ease of processing, poly-silicon has become the material of choice in surface-micromachined MEMS. Single-crystal silicon (often SOI) is the standard material for bulk micro-machined devices. In dry ambients, such as the atmosphere found inside a package hermetically sealed in a dry and inert environment, poly-Si and single-crystal electrodes show truly impressive longevity: no signs of degradation or corrosion are observed after several months at fields close to dielectric breakdown (i.e., at fields well above those encountered during normal device operation).

Many commercial MEMS devices operate in an ultra-dry ambient in a hermetically sealed package so that the chip operates in a dry ambient even if the package is subjected to high relative humidity. If the package is non-hermetic (e.g., plastic packaging as is now most commonly the case for cost reasons), there can be leakage currents on the dielectric between neighboring electrodes, which are often unpassivated for simplicity, and to avoid dielectric charging.

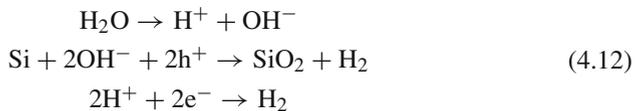
If the ambient is not perfectly dry there will be several monolayers of water on any hydrophilic surface, such as the native oxide on silicon. This adsorbed water on the surface of the dielectric between electrodes provides a leakage path for current to flow. The surface current is given by [115]:

$$j_{\text{water}} \sim A \exp [b.RH] \exp \left[\frac{-E_{\text{activation}}}{k_{\text{B}}T} \right]$$

where RH is the percent relative humidity, A and b are constants, $b \sim 0.1\text{--}0.3$, $E_{\text{activation}} : 0.4\text{--}1.1$ eV, T is the temperature. Effectively no leakage occurs for humidity levels below 50%.

Anodic oxidation occurs when there is a finite surface leakage current between neighboring poly-Si electrodes on the surface of the insulator *in the presence of moisture*. The poly-Si at the anode reacts with OH^- to form SiO_2 [115].

The reaction governing anodic oxidation is:



As can be seen from (4.12), only the positively biased electrode (supplying holes, labeled h^+) is oxidized, and hence increases in volume, whereas the negatively biased electrode (supplying electrons, e^-) is unaffected.

If a poly-Si wire is allowed to fully oxidize it becomes an open circuit, and the electrode it drives becomes non-functional. Partial oxidation of the electrodes can lead to a change in the capacitance between the electrode and the electrostatically actuated part, and thus to a change in the device characteristics (e.g., mirror tilt vs.

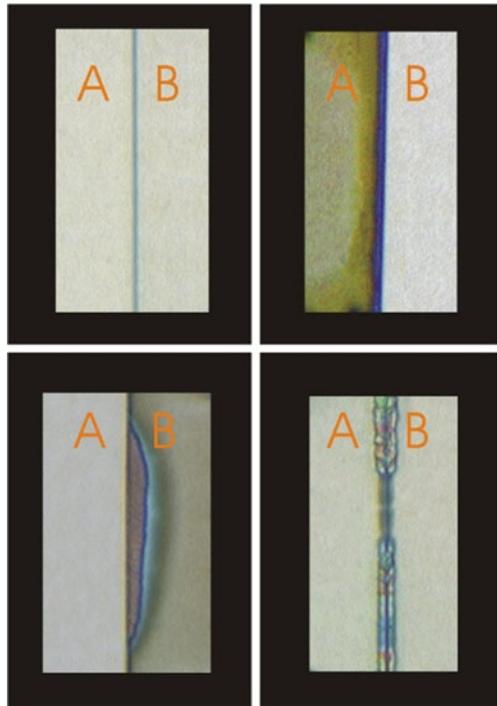
voltage). Another reported failure mode related to anodic oxidation is delamination of poly-silicon electrodes from the dielectric [116].

4.4.2.2 Observations and Mitigation

Several groups have observed anodic oxidation in a number of MEMS geometries, including microshutter arrays [117], test structures on the SUMMiT VTM process [118], and PolyMUMPS (Multi-User MEMS Process, provided by MEMSCAP)-based micromirror arrays and test structures [119] and [49].

Shea et al. report that when polysilicon test chips are operated in ambients with a RH of greater than 50%, the most positively biased unpassivated poly-Si electrodes anodically oxidize within hours or minutes, as illustrated in Fig. 4.64 for different bias conditions at 88 %RH for a 100 V bias and a 2 μm gap between the electrodes [119].

Fig. 4.64 Optical micrographs of two poly-Si electrodes on SiN_x , labeled A and B, with a 2 μm gap between them, showing the effect of different voltage drives at 88% RH and 23°C after 20 h of stress. *Top left:* 0 V to A&B. *Top right:* A: +100 V dc, B: grounded. *Bottom left:* A: -100 V dc B: grounded. *Bottom right:* A: 110 V rms, 50 Hz square wave (bipolar), B: grounded. Adapted from [119] reprinted with permission Copyright 2000 Society Of Photo Optical Instrumentation Engineers



To determine the acceleration factors, Shea et al [49] subjected unsealed poly-Si test structures to both high relative humidities and high voltages. The test structures consisted of two several-hundred micron long poly-Si electrodes separated by either a 2 or a 3- μm gap. The poly-Si is the Poly0 level of the MEMSCAP MUMPS process, 500 nm thick, n^+ doped from a sacrificial phosphosilicate glass layer. The electrodes are electrically insulated from the substrate wafer by 600 nm of Si-rich

silicon nitride. There are no moving poly-Si structures on the test chip, but the chip was released in hydrofluoric acid (HF) as are most standard surface micromachined parts (see the next section for the influence of HF on galvanic corrosion of poly-silicon).

The amount of anodic oxide that grew on the positively biased electrodes was measured after 24 h and is plotted in Fig. 4.65 (top) for four RH levels. There appears to be a threshold in relative humidity ($\sim 50\%$) below which anodic oxidation does not occur. No such threshold is observed for voltage. Figure 4.65 (bottom) is a plot of the total charge that flowed to an electrode over 24 h. In view of the strong correlation between the total charge flow and the measured anodic oxide height, the rate of anodic oxidation can be determined by simply measuring the surface leakage current.

It also follows from (4.12) that the rate of anodic oxidation is proportional to the leakage current between electrodes on the surface of the SiN insulator. This provides a very quick way to gauge whether anodic oxidation is occurring by simply

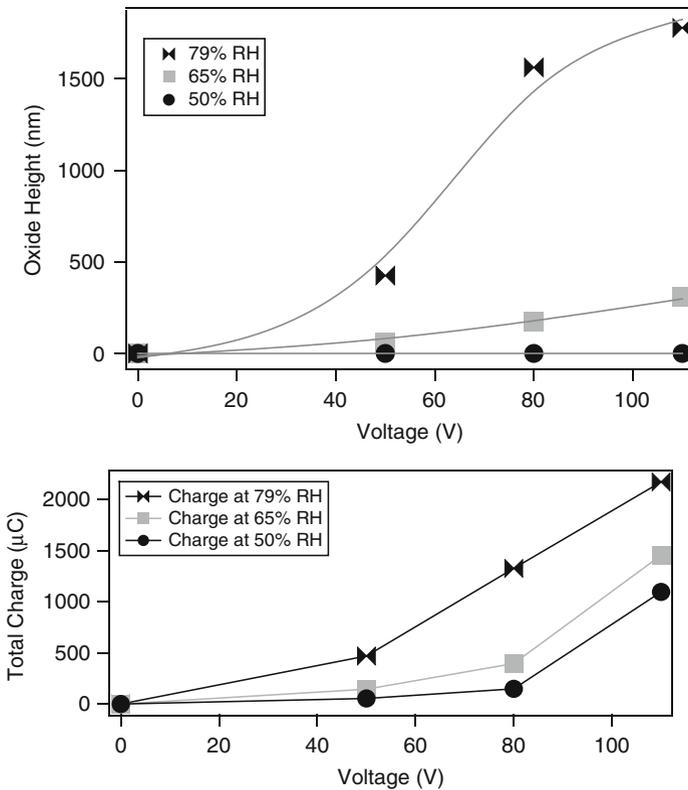


Fig. 4.65 Height of anodic oxide on anode (*top graph*) and integrated leakage current (*bottom graph*) vs. applied voltage and relative humidity, showing how the anodic oxidation is accelerated by both factors. Adapted from [49] reprinted with permission Copyright 2004 IEEE

measuring the surface leakage current. Experimentally the efficiency of this process is of the order of 2% (i.e., one SiO_2 molecule is formed for every 100 electrons that flow). The total amount of oxide grown is proportional to the total charge flow (the time integral of the surface leakage current).

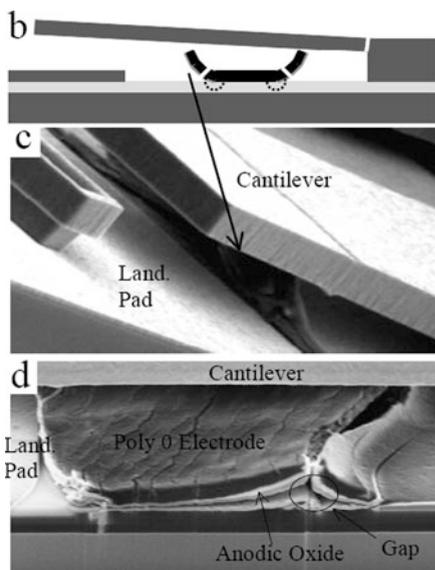
Relative humidity is an accelerating factor because the higher the humidity, the more water is adsorbed on the surface, and thus the larger the surface leakage current will be (there will also be more water available to supply the OH^-) [115]. The surface leakage current increases roughly exponentially with relative humidity, and we find that, with all other conditions kept constant, the rate of anodic oxidation scales similarly.

Voltage is a strong accelerating factor because the leakage current is roughly proportional to the applied voltage. The electric field is also an accelerating factor (at a fixed leakage current). Much more oxidation is seen at sharp corners where the field is concentrated. Changing the gap between electrodes or wires from 2 to 3 μm has a large effect on the rate of anodic oxidation.

A different anodic oxidation-based failure mechanism was reported by Plass et al. at Sandia National Laboratories [120]: the progressive delamination of Poly-silicon electrodes from silicon nitride layers. The authors were performing a study of dormancy-induced stiction by actuating polysilicon cantilever beams at 100 V and holding them for extended periods under different temperature and humidity conditions. The devices were made using the SUMMiT™ process.

It was observed, see Fig. 4.66, that positively-biased polysilicon actuation electrodes underneath the polysilicon cantilevers were the delaminating from the nitride, swelling and curling and fracturing the cantilever's above them. Because of the

Fig. 4.66 Sandia cantilever device, on which anodic oxidation delamination of poly-silicon from silicon nitride was observed, after being held at 50% RH for 50 day at 25°C at a 100 V bias. (b) Schematic cross-section, (c) SEM image (side view) of the cantilever, (d) SEM view of a FIB cut through the electrode. Reference [120] reprinted with permission Copyright 2003 Society of Photo Optical Instrumentation Engineers



volume increase during oxidation and because of curling from the induced stress, the delamination mechanically interfered with the device operation well before the electrode is fully oxidized. They noted that the delamination only starts at electrode edges directly under cantilevers, suggesting the oxidation rate also depends on the perpendicular electric field strength. In significant anodic oxidation was observed at 25% RH, but important oxidation was seen at 50% RH. Unlike Shea et al., Plass et al. see an important accelerating factor in temperature.

Hon et al. [84] report cathodic oxidation of polysilicon at high bias (>100 V) and high humidity, for the case where one of the polysilicon electrodes are in electrical contact with the substrate. They suggest that the cathodic oxidation is due to OH⁻ accumulation and a reduction in the surface potential.

Mitigating anodic oxidation requires either minimizing the operating voltages, careful choice of voltage polarity (cathodic protection), hermetic packaging or environmental control since anodic oxidation occurs extremely slowly at low humidity.

4.4.2.3 Galvanic Corrosion During Release in HF

HF is very commonly used as the final release step in processing MEMS devices because of its excellent selectivity towards silicon, and its rapid etch rate of silicon oxides. While it is known that 49% HF does not significantly affect the morphology and materials properties of single crystal silicon there have been numerous reports of HF affecting the material properties of polysilicon in particular when metallic layers are present on top of the polysilicon [29, 30, 96, 95, 121, 122].

Metal traces or coatings are often unavoidable on poly-silicon as they are required for electrical interconnections, as optical reflectors, RF antenna, or for stress control. The potential differences between the metal devices and the silicon results in galvanic corrosion. This corrosion occurs only in the HF bath and is therefore limited to the release step.

Galvanic corrosion of polysilicon is the process quite akin to the formation of porous silicon and in an HF bath, with the difference that for porous silicon the current is supplied by an external power supply, rather than by the unintended internal battery. Already in 1991 Walker et al. reported the degradation in burst strength of polysilicon membranes from varying exposures to HF [121]. A series of round robin experiments on both MCNC (now MEMSCAP) and Sandia multiuser MEMS process polysilicon found large variation in measured values of elastic properties and strength of polysilicon [123, 124]. This variation was attributed to inconsistencies in measurement techniques, variations in films growth and doping, but it is now clear that part of the differences were also due to galvanic corrosion during HF release.

The galvanic corrosion of polysilicon leads to a porous polysilicon layer, with high surface roughness (with a brown rather than shiny color). The grain boundaries in particular are etched. The Young's modulus and tensile strength of such coated polysilicon structures is greatly reduced in particular since the preferential etching at the grains leads to grooving. Figure 4.67 is a plot of tensile strength of polysilicon specimens as a function of etch time in HF [122]. The trend is

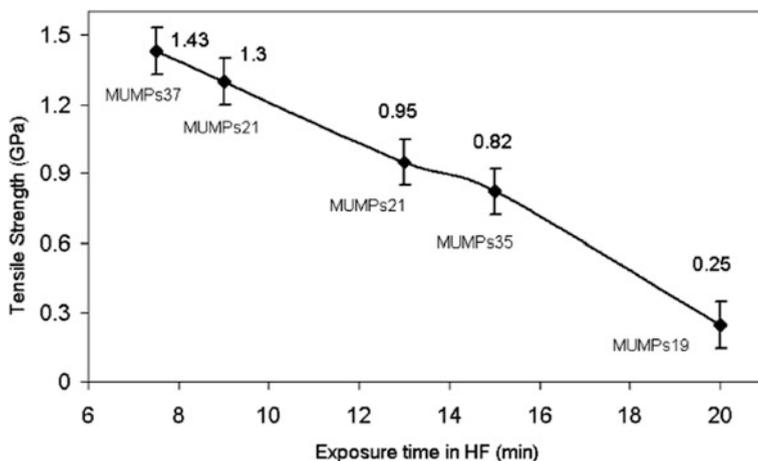


Fig. 4.67 Measured tensile strength of polysilicon test structures versus exposure time in 49% HF. Reference [122] reprinted with permission Copyright 2003 Elsevier

very clear and the effect is extremely important and can lead easily to premature device failure in view of the weakening of the polysilicon. The use of Electron Beam Scatter Detector is shown in [Chapter 5 \(Section 5.5.4\)](#) to allow determination of grain surface orientation, which for Polysilicon is a factor in fracture strength reduction.

While, as reported by Kahn et al., it is not clearly established whether corrosion occurs through a chemical oxidation followed by dissolution of the silicon oxide, or by direct formation of soluble $(\text{SF}_6)^{2-}$ species [29], it is clearly established that the etch rate depends on the level of p-doping of the polysilicon, the length of the HF release step, and the species of metallization as well as their area coverage.

A related effect reported by Kahn et al. is the growth of very thick (up to 70 nm) native oxides on polysilicon following HF release related to the galvanic corrosion of the polysilicon. They have shown that this is linked to the p-doping, and that the effect is not seen on all polysilicon films that depends on the growth conditions.

The reduction in Young's modulus of the galvanically corroded polysilicon brings about a softening of suspensions made from such springs and associated reduction in resonant frequency. Such an effect was noted for example on the first-generation polysilicon micromirrors made by Lucent Technologies, which were made using a three-level polysilicon process on top of which are two types of metal layers, Cr-Au to serve as a highly stressed layer on the lifting arms for self-assembly, and Ti-Au to serve as a low stress optical reflector, see [Fig. 4.68](#). The metallized chips were released in 49% HF bath for 3- 5 minutes. It was found that for springs with the expected low resistance contact (20Ω) to the substrate, the polysilicon had the expected stiffness, and showed no mechanical creep. However, if the substrate contact, due to a processing error, was high ($>1 \text{ M}\Omega$), then galvanic corrosion took place (see [Fig. 4.69](#)), and the current assisted etching of the polysilicon led to softer

Fig. 4.68 SEM image of polysilicon surface micro-machined micro mirror from Alcatel-Lucent. The lifting arms are coated with chrome gold, the central 0.5 mm diameter reflector is coated with titanium gold. Reprinted with permission of Alcatel-Lucent USA Inc.

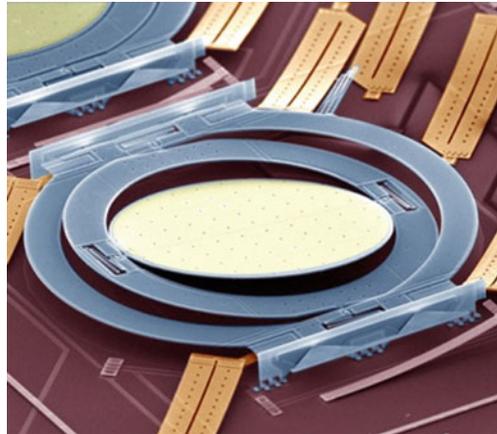
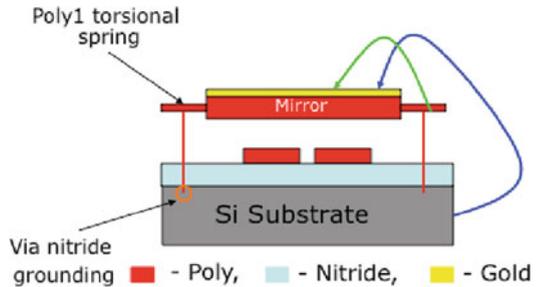


Fig. 4.69 Schematic cross-section of the micro-mirror in Fig. 4.68, showing (arrows) possible galvanic current paths leading to etching of the silicon



springs which were susceptible to mechanical creep (which is normally never seen below 450°C for silicon). The corrosion problem was resolved by improving the contact to the substrate, though other solutions were also found, such as reducing the pH of the HF bath.

Miller et al. studied the effect of adding acids or surfactants to the HF on the galvanic corrosion process. They found that reducing the pH of the bath by adding HCl (4:1 aqueous HF : HCl) was very effective at reducing the galvanic corrosion rate yielding polysilicon devices with roughness and Young’s modulus comparable to devices released without metal were released with metal but using HF vapor [96]. The effect of pH and of which reactions are favored is also discussed in [29].

Solutions to minimize galvanic corrosion include:

- Only metallize the polysilicon after the HF release (though this is often not a practical solution)
- Perform the release in vapor HF instead of liquid HF (this has the added benefit of avoiding stiction due to capillary forces when drying the device).
- Ensuring reliable substrate contacts to minimize redox potentials.

- Adding a small amount of acid (e.g., 0.1 molar HCl) to the HF bath to protect the polysilicon from corrosion.
- Minimizing the release time (which might entail changing the size and distribution of etch holes).

4.4.3 Metal Corrosion

Metal corrosion can be either chemical or electrochemical in origin. Electrochemical corrosion is more common, and is enabled by conduction through water monolayers in which contaminants have dissolved, and is driven by potentials which are either externally applied or galvanic. Corrosion is of particular concern for microelectronics and MEMS in view of the μm or sub- μm scale of metal traces: very small amounts of corrosion can lead to device failure. As many MEMS devices are sensors, some MEMS device may need to operate in harsh or corrosive environments, for instance pressure sensors for engine management or for turbine monitoring. Since, as we shall see below, corrosion can easily occur even in normal consumer application environments, we shall address primarily packaged MEMS devices that are not in direct contact with corrosive ambients.

Corrosion has three accelerating factors: (1) temperature, as temperature accelerates both diffusion and the kinetics of chemical reactions. (2) relative humidity as it provides the water surface film and, (3) concentration of trace contaminants and airborne pollutants of reactive compounds such as sulfides and chlorides that dissolve in the water surface film giving rise to high levels of corrosive ions.

Even hermetically sealed packages without getters can contain water vapor, either simply adsorbed on the surfaces, or from outgassing of water or generated from the reaction product of outgased oxygen and hydrogen. The most common packages for MEMS are plastics (e.g., overmolding on a lead frame) through which water can slowly permeate on the time scale of weeks. Most MEMS devices in use today therefore have several adsorbed monolayers of water on the surface. See also Fig. 6.21 and associated discussion.

The ionic contaminants which, when in water, lead to corrosion are of several sources [125]: (1) trace contaminants from chip processing, (2) contamination during assembly and manufacturing, (3) floods, spills, and other accidents, (4) airborne contaminants. This last category includes:

- Inorganic chlorine compounds (HCl , ClO_2 , Cl_2), which produce chlorine ions in the presence of water. Sources include seawater and many household and industrial cleaning compounds.
- Sulfur compounds (H_2S , mercaptans), which can rapidly corrode copper, aluminum, and iron alloys, and whose corrosion rate is greatly accelerated by inorganic chlorine compounds. Sources include natural gas and bacteria.
- Nitrogen oxides, which can form nitric acid. The main source is the combustion of fossil fuels.
- Ozone and other strong oxidants.

From a processing perspective, SC2 cleaning (Standard Cleaning 2, also known as RCA clean) contains HCl, and vapors can deposit on surfaces, or incomplete rinsing can result in Cl^- at surfaces. Other cleaning baths, such as piranha (mixture of sulfuric acid and hydrogen peroxide), can generate aerosols of H_2SO_4 which become airborne in fabrication facilities. Very important is the rinsing post bath use to remove the ionics at the surface.

Corrosion is either a chemical reaction, occurring with no current flow, or an electrochemical reaction, occurring when two metals are connected electrically via an electrolyte solution; as a current flows through the electrolyte, one metal is oxidized, and the other is reduced. The driving potential can be an externally applied voltage (see anodic oxidation of silicon in an earlier section), or, for galvanic corrosion, the potential is the electric potential difference between two metals (or even for one type of metal due to local differences in morphology or composition). The main metal corrosion types are: (a) uniform, (b) galvanic (c) pitting, (d) fretting, and (e) stress corrosion cracking.

As discussed in more detail in textbooks on corrosion or on IC reliability such as [53], a commonly used method to determine safe operating potentials is the Pourbaix diagram, which displays the stable phases of metals (e.g., oxides, ions, compounds) vs. the pH of the electrolyte solution. This allows the stable phases to be identified, but does not provide information on reaction rates.

For galvanic and anodic corrosion, the corrosion speed is given by the ionic current. Conduction can occur once only a few monolayers of water are present on a surface [126]. As shown in [127], currents of only 1 pA can cause the failure of 0.1 μm wide conductors in less than one minute from galvanic corrosion. This is particularly problematic when there are large differences in area between the two metals.

Acceleration factors are generally determined phenomenologically, with temperature and RH as the main variables. A very common test condition is 85°C at 85% RH. Table 2.3 lists several models for lifetime. The Peck model [127] can be written as:

$$MTTF = A_0(RH)^{-2.7} \exp\left[\frac{E_a}{k_b T}\right]$$

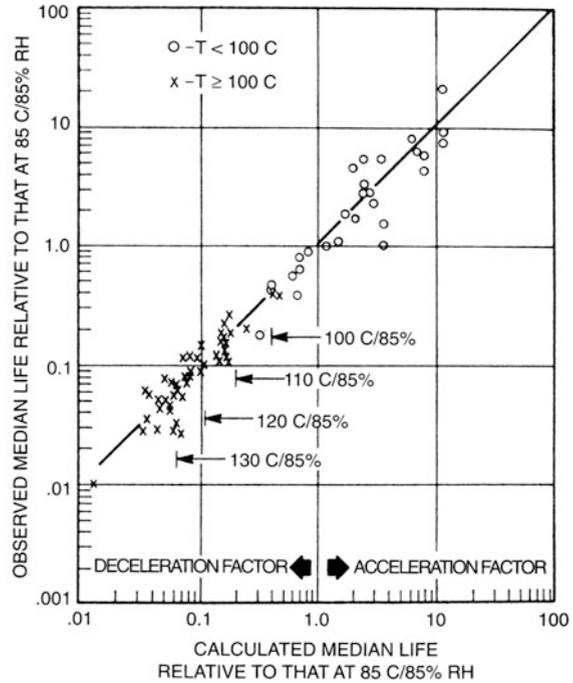
where typical activation energies E_a range from 0.7 to 0.8 eV for aluminum corrosion in the presence of chloride ions. Figure 4.70 is plot of the ratio of observed median lifetime relative to lifetime at 85°C/85%RH for aluminum in epoxy packages, showing how higher temperatures decrease lifetime.

For MEMS devices, corrosion can affect both the MEMS sensor/actuator, as well as the associated control electronics in the same package (monolithic or two-chip solutions). Approaches to minimize corrosion include:

- Passivation using barrier coatings (e.g., Parylene films, or coating with epoxy as in the “glob top” solutions), with low permeability to water, ions and gases, and excellent adhesion to avoid delamination.

Fig. 4.70 Ratio of lifetime of aluminum metallization in epoxy packages for different conditions relative to 85°C / 85% RH conditions.

Reference [127] reprinted with permission, Copyright 1986 IEEE



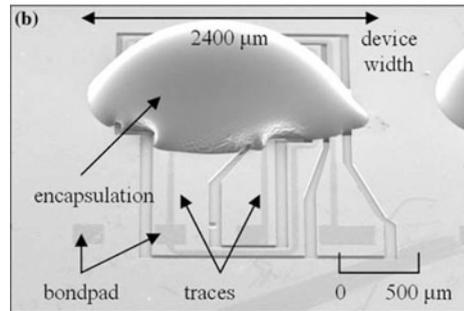
- Select metals with lower electric potential differences
- Select metals with better corrosion resistance
- Operate at temperatures higher than the ambient to reduce the amount of adsorbed water (e.g., TI's DMD chips are used at 10–20°C above ambient due to heating from the light source)
- Hermetic package
- Fabrication and handling changes to minimize ionic contaminants.

For MEMS pressure sensors, Bitko et al. [128] report on the reliability of Parylene (a chemical vapor deposited poly(p-xylylene) polymer) barrier coatings, which allows much lower cost packaging than using a stainless steel diaphragm and a silicone oil pressure transmission fluid, using electrochemical test methods to evaluate corrosion protection. Other encapsulants reported in [Chapter 6](#) for Motorola pressure sensors are Fluorogels and silicone, for which corrosive media testing is reported in [Section 6.5.2](#).

Glob top technology is popular with semiconductor overmold packaging technology for both stress relief and surface adhesion to eliminate the possibility of moisture migration at the surface to glob top interface. Chip-on-board attach methods use the glob top approach and the package itself is virtually eliminated. The glob top is often deposited over the die and wirebonds for semiconductor die, completely

covering the chip and the wirebonds, providing mechanical support as well as protection from corrosion. Figure 4.71 shows that the glob top can also be deposited and cured over a capped micromachined accelerometer structure itself, and not the traces or wirebond pads.

Fig. 4.71 Glob top on accelerometer [129]. Reprinted with permission, Copyright 2008 Springer



“Glob top” is a high viscosity epoxy, silicone or urethane or other material that is directly dispensed onto the component and surroundings (often including wirebonds). A related technique is the “dam and fill” in which a high viscosity filler is used to produce a ring around the component, that is then filled with a lower viscosity fill, often allowing better underfilling of parts. In both cases, the filler material protects the IC or MEMS component from the environment. The glob top materials typically have greatly reduced moisture permeability but key to high reliability is the adhesion of the glob top to the surface of the protected die, thus, the die must be clean prior to applying the glob top material. The use of glob tops is particularly important for dual-chip MEMS devices, MEMS that require a non-hermetic package such as pressure sensors and MEMS based microphones, and to enable lower cost packaging solutions in plastic packaging while protecting a MEMS capped structure such as the epoxy covered capped micromachined accelerometer in Fig. 4.71.

Glob tops can be applied to capped MEMS products for mechanical protection inside plastic overmolded packages. Hermetic packaging is much more expensive than plastic packaging. Capping of MEMS can provide a localized hermetic environment that also protects the delicate structure from microcontamination and handling (Fig. 4.72). This allows packaging in typical assembly environments which are generally too dirty for uncapped MEMS structures with their fine geometries. The ability to package a MEMS structure in a non-custom plastic overmold package will result in significant cost savings for high volume MEMS products.

MEMS packaging of the MEMtronics RF MEMS device (Chapter 2) uses a special glob top material (BCB) as an encapsulant with a SiN or Parylene sealant over it (Fig. 4.73). BCB is benzocyclobutene, also called Cyclotene (Dow Chemical). It can be spin coated for conformality and thickness control, and in this case, does not seep into the micromachined cage structure due to surface tension. As the BCB itself has finite moisture permeability, a moisture impermeable layer is sealed over

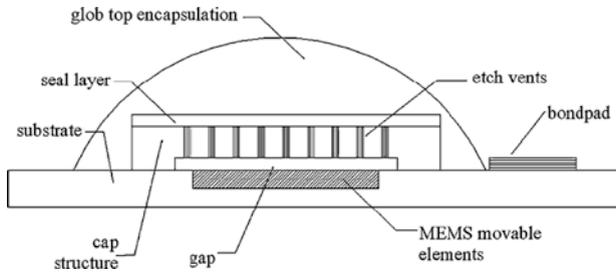
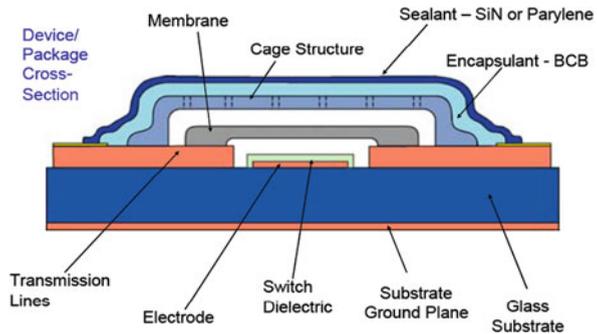


Fig. 4.72 Glob top over MEMS capped structure [129]. Reprinted with permission, Copyright 2008 Springer

Fig. 4.73 RF MEMS package using BCB as Encapsulant with sealant layer over it. Reference [130] reprinted with permission. Copyright 2005 ASME



it to provide the level of hermeticity required for the MEMS device, thus generating a hermetic package by sealing the caged structure over the RF MEMS device.

Testing of glob top package solutions is performed using temperature and relative humidity, as the primary failure mechanism eliminated by this technology is corrosion. Failure of a glob top can occur due to defects in the coating or sealant structure, and poor adhesion to the surface to be protected. Coefficient of thermal expansion mismatch can also be of concern with higher modulus materials. Moisture will wick into a poorly adhered interface through capillary action and corrosion will occur in a humid field application.

Parylene, previously mentioned, is a popular coating for MEMS due to its low moisture and gas permeability and the thin film deposition technique. Parylene is chemically vapor deposited at room temperature, which allows step coverage with a thin film protective layer that can be pinhole free at layers as thin as tens of nm. Typically, microns of Parylene are deposited virtually stress free at room temperature. The biocompatibility of certain Parylenes allows MEMS structures to use this material as more than a glob top; compliant implantable sensors are being developed with Parylene.

4.5 Conclusions

This chapter covered many possible failure modes of silicon and metal MEMS devices, along with the physics of failure. The physics of failure are essential for determining the accelerated testing conditions, once the root cause has been identified (see the next chapter). This can be tricky, as one wishes to accelerate only one failure mode at a time, while many failure modes share accelerating factors. For instance temperature accelerates creep, corrosion, and dielectric breakdown. For this reason, specific test structures are often designed to investigate in isolation one failure mode. This then helps guide a redesign, or a materials change, process change, etc, leading to enhanced reliability.

The device reliability can be determined from accelerated tests, and compared to customer requests or system needs. One should note that the package is a key aspect of the MEMS reliability, as it can control the ambient the chip experiences, especially moisture, and the latter accelerates charging, corrosion, fatigue, and stiction. Packaging is very device dependent must be considered early in the design process to ensure the expected failure modes can be controlled.

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