Semiconductor Manufacturing

7

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It was not so very long ago that people thought that semiconductors were part-time orchestra leaders and microchips were very, very small snack foods.

Geraldine Ferraro

Abstract

Semiconductor manufacturing, one of the fields of manufacturing in which the USA has played a dominant role for decades, is seen as a major consumer of resources and a source of environmental impact. The objective of this chapter is to introduce the basics of semiconductor manufacturing and, then, look at a detailed analysis of the energy and global warming impact of manufacturing one typical semiconductor product, the complementary metal oxide semiconductor (CMOS) chip. Process steps are reviewed, materials, consumables, and waste streams described, and then an example of applying life-cycle analysis to CMOS fabrication and use (including materials processing through transportation and use phases) is presented. The level of data detail required is illustrated along with trends in manufacturing and environmental impact over several technology nodes.

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7.1 Overview of Semiconductor Fabrication

The term "microfabrication" is used interchangeably to describe technologies that originate from the microelectronics industry as well as small tool machining for mechanical parts production. This chapter focuses on microfabricated semiconductor devices. These are principally integrated circuits ("microchips"), but similar technologies are used to fabricate a wide variety of other products such as microsensors (e.g., air bag sensors), inkjet nozzles, flat panel displays (FPDs), laser diodes, and so on. Similarly, the term "micromachining" is used for semiconductor processing as well as mechanical machining at the micron scale. Overall, microelectronic fabrication, semiconductor fabrication, MEMS fabrication, and integrated circuit technology are terms used instead of microfabrication, but microfabrication is the broad general term.

Modern semiconductor devices require hundreds of manufacturing process steps, using high purity materials in energy-intensive clean rooms. The high purity requirements of integrated circuit manufacturing extend from the starting material (silicon wafers), throughout the process flow to nearly all of the chemicals and materials used in production and the exacting specifications of the manufacturing clean room environments. Each wafer is processed to form layers of patterns using a repetition of the following three basic processes. First, thin films of conductive, insulating, or semiconductor materials are deposited on the wafer by physical or chemical means. This is followed by a lithography step, in which a pattern is transferred from a mask to a sacrificial photosensitive material. Finally, the thin films are etched through the pattern in the photosensitive material resulting in its transfer to the deposited film. Other processes are related to growing insulating layers (oxidation), introduction and control of dopants used to moderate transistor active regions (ion implant), chemical mechanical planarization (CMP) of films, and wafer cleaning. After processing, each wafer contains hundreds of individual devices called "dies," which are tested, diced, and packaged into chips. Fundamental processes for manufacturing modern silicon wafers are described in detail below. This chapter discusses the manufacture of integrated circuits, though some of the following process steps are also used in manufacturing FPDs, photovoltaics (PVs), and other semiconductor products.

Semiconductor production is highly resource intensive and generates a wide variety of emissions, some of which have global effects. The processes used to manufacture semiconductors emit several major classes of pollutants, including global warming gases (e.g., CF_4, NF_3, C_4F_8), ground level ozone-forming volatile organics (e.g., isopropyl alcohol, formaldehyde), hazardous pollutants (e.g., arsenic, fluorine), and flammable materials (e.g., silane, phosphine). Semiconductor fabrication facilities also consume large volumes of water and energy, and the high purity chemicals used in production are highly refined and thus have high "embodied energy." The upstream environmental effects due to chemicals manufacturing, as well as fabrication facility (fab) infrastructure and equipment, represent significant components of the environmental impact profile of semiconductor manufacturing. The use phase of semiconductor devices results in indirect

environmental and human health impacts resulting from energy-related emissions which, in the case of logic devices, has been shown to dominate impacts over the product life-cycle. The end of life of a semiconductor chip results in lead emissions if there is lead present in the chip's leadframe solder. After 2006, the EU's Restriction on Hazardous Substances, commonly known as RoHS, banned the use of lead in electronics and most manufacturers switched to lead-free solders worldwide to comply with this regulation. While other effects from end-of-life disposal of semiconductor devices may exist, they are not included in this discussion because they have never been specifically measured.

This chapter cannot cover this important subject in any real detail. Some examples of challenges and approaches to analysis are given. For a more extensive treatment of this topic readers are referred to [1] and [2].

7.2 Microfabrication Processes

Microfabrication refers to a set of technologies utilized to produce microdevices. Many of the technologies are derived from very different processes and "arts," often not connected to manufacturing in the traditional sense. For example, lithography derives from early printing techniques using etched plates to transfer patterns to paper. Planarization technology, formerly referred to as only polishing, comes from optics manufacturing dating back to the time of early astronomers and physicists. Much of the vacuum techniques also come from nineteenth century physics research. Electroplating is also a nineteenth century technique adapted to produce micrometer scale structures, as are various stamping and embossing techniques.

In the fabrication process for microdevices, a number of types of processes must be performed, in a defined sequence, often repeated many times. In the fabrication of memory chips, over 30 lithography steps, 10 oxidation steps, 20 etching steps, 10 doping steps, etc. are carried out as part of this process. Typical process steps include:

– Photolithography
– Etching (microfabrication), such as RIE (reactive-ion etching) or DRIE (deep - reactive-ion etching)
– Thin film deposition, see, e.g., sputtering, CVD (chemical vapor deposition), evaporation
– Epitaxy
– Thermal oxidation
– Doping by either thermal diffusion or ion implantation bonding
– Chemical mechanical planarization (CMP)
– Wafer cleaning also known as "surface preparation"

The complexity of microfabrication processes can be described using a number of measures, but "mask count" is typical. Mask count refers to the number of different pattern layers that will make up the final microelectronic device. Modern microprocessors are made with upwards of 30 masks while only a few masks may

be used for a microfluidic device or a laser diode. The fabrication process is not unlike multiple exposure photography in that many individual patterns (each on a mask) must be aligned with each other in the various layers of the process to create the final structure. In between the stages of fabricating these layers a number of other critical process steps occur (for example, etch/strip and CMP). The masks used in photolithography constitute a major portion of the cost of processing the microdevice and, recently, a number of so-called maskless techniques relying on writing processes without the mask have been discussed [3].

A few of the more prominent process steps are described in more detail below to illustrate the complexity.

7.2.1 Lithography

A major component of semiconductor fabrication is photolithography. The lithography process is the means whereby patterns are transferred onto a substrate (e.g., silicon, gallium arsenide, etc.). The pattern is used to isolate areas for subsequent etching to create trenches for interconnects and lines or to protect the substrate from etching. The patterns are written on glass plates called reticles, much like the glass slides used in earlier forms of photo presentations with projectors. These are the masks referred to in the previous section. Lithography is used because it allows exact control over the shape and size of the features created, and because it can create patterns over an entire surface simultaneously. The main disadvantages are that it is primarily used for creating 2D (i.e., "flat") structures, and, as with other semiconductor processes, requires extremely clean operating conditions. In a complex integrated circuit (for example, CMOS), a wafer will go through the photolithographic cycle up to 50 times. Lithography machines are designed to enhance throughput but necessarily require sophisticated mechanical structures, control, and metrology to maintain pattern quality at high exposure speeds.

Photolithography involves a number of steps in a series of often repeated combinations including:

- Substrate preparation
- Photoresist application
- Soft-baking
- Exposure
- Developing
- Hard-baking
- Etching

and various other chemical treatments (thinning agents, edge-bead removal, etc.) in repeated steps on an initially flat substrate.

A typical cycle of silicon lithography would begin with the deposition of a layer of conductive metal several nanometers thick on the substrate. A layer of photoresist—a chemical that hardens or softens when exposed to light (often ultraviolet)—is applied on top of the metal layer by spinning the substrate under a stream of photoresist. The mask, basically a transparent plate with opaque areas printed on it,

is placed between a source of illumination and the wafer, selectively exposing parts of the substrate to light. The photoresist is then developed during which areas of unhardened photoresist undergo a chemical change. After a hard-bake, a series of subsequent chemical treatments etch away the material under the developed photoresist, and then etch away the hardened photoresist, leaving the material exposed in the pattern of the original photomask.

A characteristic of photolithography clean room environments is that the filtered fluorescent lighting contains no ultraviolet or blue light to prevent accidental exposure of the photoresist. Most types of photoresist are available as either “positive” or “negative” resists. With positive resists the area that is opaque (masked) on the photomask corresponds to the area where photoresist will remain upon developing (and hence where conductor will remain at the end of the cycle). Negative resists will create the inverse—any area that is exposed will remain, while any areas that are not exposed will be developed. After developing, the resist is usually hard-baked before subjecting to a chemical etching stage which will remove the metal underneath.

7.2.2 Oxidation and Annealing

Thermal oxidation of silicon produces silicon dioxide, a high-quality insulator that can also be used as a gate oxide, as a stress barrier for nitride (pad oxide), or to prevent contamination in ion implant (screen oxide) and undoped silicate glass (USG) applications (barrier oxide). In this process, silicon on the wafer reacts with oxygen or oxidizing chemicals such as N_2O in a temperature range of 1,173–1,373 K, to form silicon dioxide. Vertical furnaces can be used to produce thicker oxide layers on batches of wafers, or Rapid Thermal Processing (RTP) equipment can be used to produce thinner oxide layers on individual wafers. Annealing is another high temperature process that can be performed in RTP chambers. Annealing is used to control the concentration profile of dopant and to reduce defects.

7.2.3 Wet Cleans

Wafer cleaning is the most frequently occurring category of process step in the production of a wafer due to the need for contamination removal and surface conditioning before sensitive deposition and thermal treatments. Wafers are cleaned after each photoresist (PR) removal and CMP step, and before nearly every oxidation, anneal, and deposition step. A brief summary of the main types of wafer cleaning steps is given in Table 7.1

Table 7.1 Wafer cleaning methods [1]

Clean name and components	Purpose	Usage
SPM or "Piranha" clean H_2SO_4:H_2O_2: UPW (1:1:6)	Removal of organic materials	SPM is used as the primary means of PR removal or to supplement plasma PR strip
SC1 (Standard Clean 1) NH_4OH:H_2O_2: UPW(1:1:6)	Removal of organic and some metal impurities	
SC2 (Standard Clean 2) HCl:H_2O_2:UPW (1:1:6)	Elimination of metallic and alkaline contaminants	
Hydrofluoric oxide strip HF:UPW (1:100)	Silicon dioxide ("oxide") layer removal	Before any metal deposition and as a part of, or after, most dielectric etch steps

7.3 Facility Systems

7.3.1 Resource Use

In addition to the specific chemicals used in processes such as cleaning and etching process steps vast volumes of other fluids, resources, and materials are used.

For example, ultra pure water (UPW) or deionized (DI) water are used for numerous cleaning steps in semiconductor manufacturing as seen in Table 7.1. A typical semiconductor fab uses two million gallons of water or more [4]. Out of that, about three quarters of the water is used for UPW and a single wafer may require 2,000 gallons of UPW. UPW is treated to remove minerals, colloids, and bacteria using reverse osmosis, ion exchange, and/or ultra filtration processes. UPW is expensive both to produce and to treat for release because of its use of water, energy, and consumable materials. However, used rinse UPW is typically much cleaner than municipal supply water and may be treated and reused in the UPW system or reclaimed for other uses in a fab. In certain cases, fabs that reclaim UPW water for cooling towers may eliminate the need to purchase municipal water for their cooling towers altogether.

Nitrogen is an inert gas that is used to purge chambers and pipes between processes. Nitrogen may also be used to condition other purge gasses to desired temperatures. Generally, it is produced onsite and piped into a fab rather than delivered in tanks. Argon, carbon dioxide, or clean dry air (CDA) may also be used for similar purposes. Use of CDA instead of nitrogen may represent significant cost and energy savings for a fab. CDA is likewise produced onsite via filtration and dehumidification. It is used for various purposes but particularly for drying wafers following wet clean steps.

Maintaining a clean room requires numerous energy-intensive components, including fans, filters, air conditioning, and dehumidifying. The air in a clean room must be filtered to remove particles corresponding to the clean room class, recirculated to provide a specified number of air changes per hour, and pressurized with make up air so that contaminants do not enter the room even as air or process gasses are exhausted out of the clean room. The class clean room refers to the max number of particles up to 0.5 μm in size allowed per cubic foot of air. The number of air changes per hour varies from double to triple digits with air grades varying from grade D to grade A (for explanation of grades of clean room see, for example [5]).

Process cooling water (PCW) systems are another energy-intensive component of a semiconductor fab. PCW is used to cool process chambers, pumps, and abatement equipment. PCW is either cooled via the cooling tower alone or chilled via an additional chiller. The energy intensity of PCW may be reduced by moderating the temperature differential between the supply and return PCW.

7.3.2 Abatement

The oldest and most fundamental of the facility abatement systems is the "house scrubber," an enclosed, water-sprayed matrix of inert mesh. This system captures gaseous inorganic emissions, largely acids, which are sent as liquid effluent to the acid waste neutralization (AWN) system, which continuously monitors and corrects the pH of the incoming liquid waste.

Gaseous ammonia is emitted in small quantities from most nitride CVD processes, either as unreacted precursor or as a byproduct emission. Fabs with gaseous ammonia exhaust are fitted with a separate ammonia exhaust system and scrubber in order to prevent particulate formation, clogging, and corrosion in the acid exhaust system. Gaseous ammonia waste is captured using a water scrubber similar in design to the facility acid scrubber but about a tenth of the size.

Complementary metal oxide semiconductor (CMOS) logic fabs use large quantities of both liquid ammonia and sulfuric acid in wafer cleaning processes. Liquid ammonia, collected via drain, may be recycled on site using membrane filtration or distillation, or treated using sulfuric acid to produce ammonium sulfate. In this model, the latter is assumed and thus ammonium sulfate, which results from the neutralization of ammonia and sulfuric acid effluents in the AWN system, is among the liquid wastes produced in the highest volume by wafer fabrication in this model.

There are several combinations of treatment methods that may be used to address the liquid effluent of copper CMP processes. Copper CMP waste treatment is described in the work of Krishnan [6, 7] as a sequence of ion exchange, microfiltration, activated carbon filtering, and filter pressing. An ion exchange resin bed removes copper and is regenerated at the fab using sulfuric acid, to produce $CuSO_4$ liquid waste. Slurry particles are filtered and pressed into a solid non-hazardous waste which is sent to a landfill. The remaining water contains less

than 2 ppm dissolved copper and is sent to the AWN system. The concentrated $CuSO_4$ liquid is sent offsite as hazardous waste to be electrowinned for copper recovery or possibly purified into a useable byproduct.

The fluoride waste system treats fluoride wastewater using CaOH and a flocculant material to produce non-hazardous solids containing calcium fluorite (CaF_2).

CVD steps emitting per-flouro-compounds (PFCs) require combustion and water scrubbing or plasma point-of-use (POU) abatement because water scrubbing alone does not break down these compounds (and in some cases may form reactive fluorinated byproducts). CVD steps emitting silane or hydrogen above flammable concentrations also require immediate combustion of their emissions in POU systems due to the risk of explosion in exhaust lines. Implant processes emitting phosphine and arsine are typically abated using cold bed adsorption systems.

7.4 Green Manufacturing in the Semiconductor Industry: Concepts and Challenges

The semiconductor manufacturing process is exceptional in the large variety of chemistries that it employs. As can be seen in the previous section, wafer processing involves a number of different acidic (the hydrofluoric and sulfuric acids used in wafer cleans), basic (wafer clean steps including ammonia), oxidizing (wafer cleans using peroxide), and other highly reactive chemistries (fluorine used in etching), as well as compounds which are extremely toxic (arsine and phosphine used in implant). The equipment used to administer these reactions must be designed to protect the manufacturing personnel, following safety rules outlined by government agencies such as OSHA and standards (e.g., SEMI S2) developed within industry groups such as Sematech.

As all mainstream semiconductor manufacturing equipment currently sold and used follows these regulations, the direct human health impacts and risks within the fab have been nearly eliminated in normal operation. (Though, hazards still exist in cases of catastrophic breakdown, fire, or earthquake.) Once these chemicals leave the equipment, they must be further handled and neutralized by the POU and facility abatement systems, in a safe and efficient way. While the guidelines and standards for equipment safety are enough to thoroughly guide and ensure the design of safe equipment, the design and operation of facility abatement is a much more complex undertaking. The abatement and neutralization of emissions is not as predictably efficient or controlled as the reaction of chemicals within the process equipment in part because the processes used to neutralize emissions to the extent necessary to make them safe for release into the environment do not need to be as precise as those used within the process chamber. Additionally, within the facility abatement systems (the house gaseous waste, fluorine abatement, and AWN systems), the chemistry of the combined emissions of the many processes running on site can be unpredictable. Facility abatement systems are designed to continuously measure the incoming waste stream and adjust the neutralization chemistry accordingly.

Nevertheless, neutralization of an unpredictable waste stream cannot be as efficient or controlled as that of a known waste stream.

When facility abatement systems are not operating ideally, or were not originally designed or built to sufficiently handle the current waste streams entering them, a variety of environmental impacts can result. For example, the “house scrubber” (facility gaseous abatement system) may be accepting significant concentrations of gaseous fluorine (F_2), either because no POU abatement is set up on plasma etching equipment or because POU systems are not sufficiently scrubbing the F_2 gas. This gaseous fluorine will react with water to a small extent to form OF_2, a reactive and highly toxic gas [8]. Another product of the reaction of fluorine with water is HF. When fluorinated compounds are effectively abated from processes at POU, the resulting liquid HF is sent to a fluorine waste treatment system which is separate from the house AWN system. Any HF captured in the house scrubber system could not be effectively treated before being released into the environment, as it would already be mixed in with the larger volume of non-hazardous waste. Ineffective abatement of fluorine and the consequent release of reactive fluorine species into the environment could result in human health and ecological impacts.

While the potential environmental and health impacts from semiconductor manufacturing are understood and, in most cases, successful efforts are made to eliminate or mitigate them, the global warming potential (GWP) impacts associated with certain PFCs were not recognized or controlled until many years after the introduction of their use.

PFCs are an important group of emissions from semiconductor manufacturing due to their high infrared absorption, long lifetimes, and consequential global impact. These compounds are used in wafer etching and include CF_4, C_2F_6, NF_3, and SF_6. For this reason, global warming impacts are an important impact category to consider in the production of ICs.

The abatement of some PFC emissions are regulated by the Kyoto Protocol (in Annex I and II nations) and, in 1999, the World Semiconductor Council (WSC), which includes the semiconductor industry associations of Japan, Europe, Korea, Taiwan, and the USA, issued a position paper which committed members to PFC emissions reduction by 10% of 1995 or 1999 baseline levels by the end of 2010. The China Semiconductor Industry Association (CSIA) joined the WSC in 2006 but did not sign on to the climate protection agreement at that time. In 2009, CSIA stated an intended plan to join the WSC agreement on PFCs but did not commit to a baseline year for that goal, and has not yet as of the year 2010 [9].

Although these two agreements have resulted in tremendous progress in the reduction of semiconductor PFC emissions, more than half of semiconductor production occurs outside of Kyoto Protocol Annex I and II nations, and, in 2008, almost 20% of semiconductor production capacity was held in China, Singapore, and Malaysia, where the industrial consortia have not committed to the WSC PFC goals. Semiconductor capacity has continued to grow in those countries where PFC emissions control is not required by any public agreement or national policy. NF_3 is not regulated by the Kyoto Protocol, but is among the PFCs which are used in highest volume in the semiconductor industry [10, 11].

7.5 Use-Phase Issues with Semiconductors

Most consumer products which consume more than a few watts in operation will have a use phase which dominates energy consumption impacts among all of the life-cycle stages. Depending on the electricity mix in the location of use, therefore, the use phase of an integrated circuit will in most cases be the largest contributor among its life-cycle stages to primary energy and water use, as well as GWP, acidification, ground-level ozone formation, and other impacts related to electricity generation. Even in the case of an IC with a low power consumption, the use phase is an important contributing stage to life-cycle impacts.

Most ICs are built into products which have a use phase which dominates energy consumption impacts among all of the life-cycle stages. The importance of the use phase has thus been no secret to those concerned with the environmental impacts of integrated circuits and computers in general. Indeed, the longest running and likely most well-known environmental initiative concerning electronics is Energy Star [12]. Energy Star is a labeling program operated in cooperation between the US Environmental Protection Agency and Department of Energy. The Energy Star program develops testing protocols, collects data, and sets thresholds for the definition of energy efficiency in a variety of categories of consumer electronics. Manufacturers who certify their product to the standard may then print the Energy Star label on their product or packaging. Computers and monitors became the first consumer products to carry the Energy Star label in 1995.

In addition to the improvement in efficiency related to hardware (e.g., lower power consumption in integrated circuit chips, more efficient battery technologies), power management through software applications has also played a significant role in improving the efficiency of laptops and other electronic products. For example, advanced, or “dynamic,” operating system-integrated chip power management allows software to shut down the central processing unit (CPU) when the user is inactive. Introduced in the early 2000s, this software was available as part of both the Windows 2000 and XP operating systems, but neither of these platforms had advanced power management settings enabled by default, and the functionality was often not enabled by the user. In 2007, when many used their computers with advanced power management features disabled due to the default Windows settings, a market research study found that as many as 60% of computer users in the USA did not shut down their computer at the end of the day. These computers which were left on (termed “zombie” computers), which would otherwise have been put to sleep via advanced power management, resulted in the needless emission of an estimated 14 million tons of CO_2 that year (Alliance to [13]). In Windows 7, the default settings for shipment were for lower power consumption, which supported wider use.

The Climate Savers Computing initiative is a more recent industry initiative concerning the use phase of computing which put a particular focus on software-integrated power management. Climate Savers has served as a platform for collaboration and technical standard-setting to improve efficiency in hardware as well as increase the adoption and consumer use of advanced power management.

More recently, other manufacturers and distributors have been working on labeling standards for indicating the consumption of consumer electronics. The Sustainability Consortium has an Electronics Sector Working Group that is focused on creating scientifically grounded and transparent metrics for measuring and reporting environmental and social impacts of electronics [14]. A large group of companies and organization representing the sector is working to create these metrics using a life-cycle based platform and will be in an ISO-certifiable and index-ready format.

7.6 Example of Analysis of Semiconductor Manufacturing

7.6.1 Introduction

The semiconductor manufacturing process is complex and, unsurprisingly, determination of the associated emissions and their impacts is not a straightforward task. Nevertheless, it is instructive to look at a detailed analysis of the life-cycle energy and global warming emissions of CMOS logic. This section is taken substantially from the doctoral thesis of one of the chapter authors, Sarah Boyd, and can be found in its entirety in [1] or [2].

Information and communication technology (ICT) has the potential to reduce the impact of human activities on the environment. In order to fully understand the environmental benefits of ICT, the life-cycle impacts of computer systems must be compared with those of the products and services they replace. The questions of whether reading news on a handheld device rather than newspaper or purchasing books from an online retailer instead of from a bookstore reduces environmental impact are two examples of this sort of comparison in the recent literature [15–17]. While, initially, the replacement of traditional products such as newspapers by a small fractional increase in the use of a handheld mobile device seems a winning environmental trade-off, there has been increasing concern over the large energy demands of the Internet infrastructure, with data center energy demand in the USA reaching 1.5% of the national total in 2006 and estimates of 2011 demand surpassing 10 billion kWh [18].

Among the numerous parts which compose the IT infrastructure, semiconductor chips are among the most resource intensive to produce as well as the most difficult to characterize for the purposes of life-cycle assessment (LCA). While it may be possible to estimate the environmental impacts of a cable or plastic computer housing knowing only their masses and material types, the impacts associated with a semiconductor chip are not represented well by the substance of the device itself. While a logic chip may weigh only a few grams, the chemicals and water required to produce it weigh many kilograms. There is a need for a more detailed and transparent life-cycle inventory (LCI) for semiconductor products.

CMOS is the dominant device structure for digital logic. The CPU in desktops, laptops, handheld devices, and servers, as well as nearly all embedded logic (the chips in appliances and toys) are CMOS-based. Every 1–3 years, a new generation

or technology node of CMOS is introduced, based on design laws which have been established through industrial collaboration. Due to the cooperation necessary to plan and achieve the goals for each generation, there is considerable homogeneity among the devices manufactured by the major logic producers at each technology node. A generic version of CMOS may thus be used to represent logic products from many different manufacturers.

This section provides a summary of a life-cycle energy analysis for CMOS chips over seven technology generations with the purpose of comparing energy demand and GWP impacts of the life-cycle stages, examining trends in these impacts over time and evaluating their sensitivity to data uncertainty and changes in production metrics such as yield. Chips of generic CMOS logic, produced at a semiconductor fabrication facility (fab) located in Santa Clara, California are evaluated at each technology node over a 15-year period, from the 350 nm node (circa 1995) to the 45 nm node (circa 2010). This study is composed of production-related LCA data, based on emission measurements, process formulas, and equipment electrical tests, combined with previously published LCA data for chemicals, electricity, and water, as well as publicly available use-phase data for computer chips. A hybrid LCI model is used. Wafer production, electricity generation, water supply, and certain materials are represented by process LCA data, while the remaining materials are described using economic input–output life-cycle assessment (EIO-LCA) methods [19]. While life-cycle energy and GWP of emissions have increased on the basis of a wafer or die as the functional unit, these impacts have been reducing per unit of computational power. Sensitivity analysis of the model shows that impacts have the highest relative sensitivity to wafer yield, line yield, and die size and largest absolute sensitivity to the use-phase power demand of the chip.

The methodology used in the study is detailed first, including the materials and other resource and production data sources covering the full range from material production to end of life of the CMOS device. The results of the study are then summarized. This example illustrates the level of detail necessary to adequately measure, or estimate, the impact in terms of energy use and GWP of such a complex production.

7.6.2 Methodology

The scope of this LCA includes materials production, wafer processing, die packaging, transportation, and use of the logic chip, Fig. 7.1. The LCA model is hybrid, using a combination of process-based LCA and economic input–output (EIO) LCA data (Table 7.1). The functional unit is one packaged die, but in order to allow further analysis and to investigate trends, results are also presented per wafer and per million instructions per second (MIPS). The stages of analysis cover from materials production through end of life.

At end-of-life, it is assumed that there is no recoverable energy value in the chip. Other end-of-life impacts are not included because the functional unit of this LCA is the chip alone and past studies of electronic waste impacts have generally

Fig. 7.1 Life-cycle stages with data source types [1]

concerned the computer as a whole. A great deal of effort has been focused on the end-of-life of computer systems because irresponsible recycling practices can produce dramatic and visible human health and environmental impacts. The major pollutants associated with e-waste (flame retardants, polychlorinated biphenyls, dioxins/furans, polycyclic aromatic hydrocarbons, lead, cadmium, and mercury) are largely emitted from the incineration or chemical breakdown of circuit boards, wiring, housing, and displays. Although there may be harmful emissions from the decomposition or combustion of a logic chip, these have not yet been measured in isolation, but remain an important topic for future work. Because there is no positive energy value and no global warming impacts at end-of-life, the net impact in this life-cycle stage is zero.

In order to clarify the model structure and in order to demonstrate the sensitivity of results to variation in model parameters, the inventory model is described algebraically. The contributors to the life-cycle energy requirements (e_{total}) and global warming potential (GWP) of life-cycle emissions (g_{total}) are illustrated in (7.1) and (7.2).

$$e_{total} = e_{up} + e_{inf} + e_{prod} + e_{trans} + e_{use} \tag{7.1}$$

e_{up}: energy for upstream materials;
e_{inf}: energy for infrastructure;
e_{prod}: energy for production;
e_{trans}: energy for transportation;
e_{use}: use-phase energy.

$$g_{total} = g_{up} + g_{inf} + g_{prod} + g_{trans} + g_{use} \tag{7.2}$$

g_{up}: GWP of emissions due to upstream materials;
g_{inf}: GWP of emissions due to infrastructure;
g_{prod}: GWP of emissions due to production;
g_{trans}: GWP of emissions due to transportation;
g_{use}: GWP of emissions due to use-phase energy.

A schematic of the mass and energy flows used in this analysis relative to the fab is shown in Fig. 7.2, from [1].

The compositions of these various terms from (7.1) and (7.2) are now described.

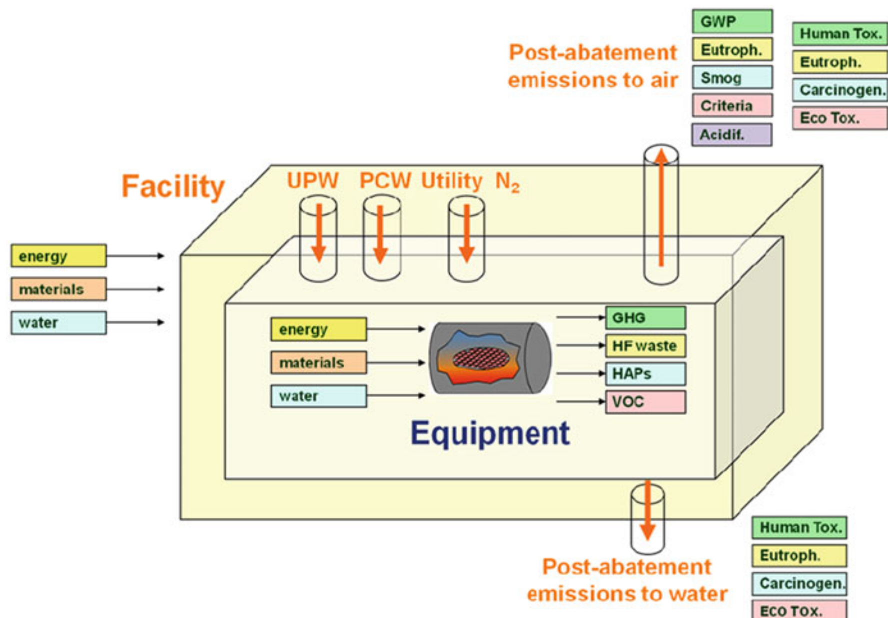

Fig. 7.2 Overview of mass and energy flows considered in the fab model [1]

7.6.3 "Upstream" Materials

7.6.3.1 Chemicals

Among the life-cycle impacts of semiconductor products, the importance of energy-related emissions from the production of high purity chemicals has been noted previously by a number of authors [20–23]. The limited LCA data available for exotic and/or high purity semiconductor process chemicals remains a challenge in quantifying these impacts. The formulas for advanced semiconductor processing materials such as CMP slurries are closely held intellectual property. Chemical textbooks and handbooks simply do not contain information about the production processes used to make them, and it is challenging to identify the dominant production method among patent filings, as enterprises will at times file multiple patents describing different production pathways or describe production recipes broadly. While LCA data are available for some basic chemicals used in wafer manufacturing, such as elemental gases, metals, and common acids, it is usually representative of the industrial grade, with a purity of 99% or lower, rather than ultra-high purity or semiconductor grade (99.9997–99.9999999% pure).

This example uses a method of LCA data collection by which data based on process descriptions are used where available, and data from the Carnegie Mellon EIO-LCA database are used where costs are known. When no process LCA data and no cost information are known, an estimate for the energy intensity of chemical manufacturing developed by Overcash is used [24]. In this study, the

Table 7.2 Summary of data sources [1]

Silicon	Process LCA
Chemicals	Process and EIO-LCA
Infrastructure and equipment	EIO-LCA
Fabrication	Process LCA
Electricity	Process and EIO-LCA
Water	Process and EIO-LCA
Transportation	Process LCA
Use	Process LCA

"pharmaceuticals and medicines" rather than "photographic film and chemicals" commodity sector (NAICS #325400) is used in the EIO analysis for those materials which are high value specialty chemicals (those with a purchase price over $1,000 per kg), since the economic value of these materials is represented more closely by the former sector. The organic chemicals (NAICS #325190) and inorganic chemicals (NAICS #325180) commodities are used for the remaining materials, as appropriate. Although additional impact categories are available for those materials analyzed using EIO-LCA, the inventory is limited to primary energy demand and the GWP of emissions. Data sources for all inventory materials are detailed in [1]. The uncertainty of EIO-LCA data is given as one order of magnitude for each result. The uncertainty of process data from textbooks and manuals is assumed to be zero, because it is unknown but assumed to be small as compared with other chemical LCA data sources. All data sources and impact values for materials using published process energy data are given in [1].

7.6.3.2 Silicon

Silicon is the purest substance used among all semiconductor process materials. There are several processing steps that raw silica takes to become a pure silicon wafer, the substrate of semiconductor devices. Raw silica is refined into metallurgical grade silicon, which is twice refined to produce a single crystal ingot that is then sliced into wafers. The high embedded energy of the final product (approx. 2,000 kg) is due not only to the energy intensity of these processes but also to a cumulative low yield caused by the losses at each step. Full descriptions of the energy requirements and environmental emissions of high purity silicon production are available from previous sources [21, 25]. The LCA data provided by Williams and used in this study [21] is duplicated here for clarity, Table 7.2.

7.6.3.3 Water

Since the focus of this example is the production of chips of generic CMOS logic at a fab located in Santa Clara, California, the environmental impacts associated with the Santa Clara water supply are modeled. Modeling is done using information from the Santa Clara Valley Water District and previous work on LCA of California water supplies by [26]. The Santa Clara Valley Water District infrastructure is composed of three treatment plants for local and imported water, one recycled

Table 7.3 Energy intensity of silicon production [21]

Process step	Electrical energy/kg Si out (kWh)	Si yield (%)
Refining Silica to Mg-Si	13	90
Mg-Si to trichlorosilane	50	90
Trichlorosilane to polysilicon	250	42
Crystallization of polysilicon to sc-Si ingot	250	50
Sawing Sc-Si ingot to Si wafer	240	56
Process chain from silica to wafers	2,127	9.5

Table 7.4 Global warming intensity of Santa Clara Water [1]

	Local supply	Imported	Recycled
Contribution of source (%)	45	51	4
kWh/l	0.0021	0.0019	0.0002

water treatment facility, 142 miles of pipelines, and three pumping stations. According to a report from the district board, approximately 51% of the water used in Santa Clara is imported, while 45% comes from local sources and the remaining 4% from recycled stocks [27]. Most water imported to Santa Clara comes from the Sacramento-San Joaquin River Delta via the South Bay Aqueduct, though a small fraction also comes from the Hetch-Hetchy reservoir via the San Francisco water system. Local water sources include groundwater basins and ten surface reservoirs. The life-cycle environmental impacts evaluated by Stokes for imported and recycled water from the Oceanside Water District in San Diego are applied, on a per volume basis, to the imported and recycled fractions of water in the Santa Clara system. Life-cycle environmental impacts associated with Santa Clara's locally sourced water are estimated based on the energy required for treatment and distribution of imported water in Stokes' model of Marin's water treatment works. The global warming emissions intensity for the power utility in Santa Clara (Pacific Gas and Electric), 280 g CO_2eq./kWh, is used. The energy intensity and percent contribution of each source is presented in Table 7.3. The resulting global warming emissions per liter of water provided in Santa Clara is 0.6 g CO_2eq.

7.6.3.4 Infrastructure and Equipment

The energy use and GWP for infrastructure and equipment are evaluated using EIO-LCA. Rock's Law (which says that the cost of a semiconductor chip fabrication plant doubles every 4 years) is used to estimate the total cost of the fabrication facility and the costs of wafer fabrication equipment are taken as 70% of the total cost of the fab, based on a commonly stated approximation. Expenditures are depreciated over a 10-year period, using a straight line schedule, yielding an annual cost which is corrected to 1997 dollar values using the average US inflation rate over the 1995–2008 period of 2.7%. Total costs for the building and equipment for each technology node are provided in Table 7.4.

Table 7.5 Cost of fab infrastructure and equipment [1]

Year	1995	1998	1999	2001	2004	2007	2010
Technology node	350	250	180	130	90	65	45
Equip. cost, depreciated ($M/year)	42	71	84	119	200	336	400
Construction cost, depreciated ($M/year)	18	21	25	30	36	43	51

7.6.3.5 Electricity

The emissions associated with electricity use at the different geographical locations of each life-cycle stage are reflected in the model. In the fabrication and use stages, emissions factors for electricity are specific to California, while the stages of chemical and infrastructure production are represented by each US industry average GWP emissions factors, via EIO-LCA [19].

The environmental impacts associated with electricity supplied to the California plant are evaluated using two previous LCA of electricity generation, data from the EPA and information from Santa Clara's electric utility, Pacific Gas and Electric. The electricity mix of Pacific Gas and Electric in 2008 was 47% natural gas, 23% nuclear, 13% large-scale hydroelectric, 4% coal, 4% biomass or other waste combustion, 4% geothermal, 3% small-scale hydroelectric, 2% wind, and 0.1% solar photovoltaic [28]. The life-cycle GHG emission factors (g CO_2eq./kWh) for natural gas, coal, large-scale hydroelectric, and solar photovoltaic power are taken from the work of [29], while that for nuclear electricity is taken from a study by [30]. Direct GHG emissions for geothermal and biomass combustion are taken from the EPA [31]. Small hydro is considered to have the same impacts as large hydro. A national average for the Chinese grid of 877 g CO_2eq/kWh, based on a previous LCA [32], is used for the production scenario in China.

In order to facilitate comparison with preceding studies, for most life-cycle stages, the convention of 10.7 MJ of primary energy per kWh electricity is used. This represents a worldwide average value for fuel consumption in electricity production [21]. The primary energy intensity of electricity supplied in Santa Clara is not documented, and since there have been no studies which provide net fuel intensity of nuclear, geothermal, wind, or the other non-combustion generation technologies used by the California grid, the fuel intensity of the electricity used in fabrication is taken as the worldwide average. In actuality, the primary energy intensity of Santa Clara electricity is estimated as the world average. Since most of the thermal generation in California is combined cycle natural gas combustion, and the contribution of renewables and nuclear are higher than the world average, the net primary energy demand for electricity production is somewhat lower than 10.7 MJ/kWh. For the purposes of this example, however, the global average is used.

The fuel intensity of electricity in China, however, is higher, with an average value of 12 MJ/kWh of electricity, due to an average lower conversion efficiency of power plants as well as higher losses in transmission and distribution [32].

7.6.3.6 Semiconductor Manufacturing

In this analysis the primary model for wafer manufacturing is located in Santa Clara, California, USA. A separate scenario for production in China is developed in order to demonstrate the environmental effects of using China's electricity supply mix and neglecting PFC abatement. Although PFC emissions may be abated in some fabs in China, the assumption is made that there are few if any controls on PFC emissions at the Chinese production site.

The mass and material flows are accounted at the level of the fab and equipment, see Fig. 7.2.

A complete summary of changes to the process flow for each device over the technology nodes covered in this example is given in [1]. The process change which has allowed the greatest reduction in GWP from one technology node to the next is the switch from in situ plasma generation to remote plasma generation for etch and post-dielectric deposition chamber cleaning.

Facility and Process Equipment Energy Demand. While device design, process complexity, and the length of the process flow grow continuously, total fab energy consumption has not increased at the same pace and has at times decreased in the past decade due in large part to facility efficiency improvements. These changes are reflected in the model; at each technology node, improvements are made to certain facility equipment, such as the water chillers or exhaust pumps, which allow reduced energy consumption. Rising energy costs as well as pressure to achieve GHG emission reduction goals set by the World Semiconductor Council have driven fabs to reduce their total energy consumption. These efforts are reflected in the industry goals set in the ITRS, which show an ongoing effort to reduce facility energy consumption on a kWh/cm^2 wafer area basis. The trend may be verified using an EIO perspective. By normalizing per unit of silicon area used, rather than by economic value of production, energy consumption can be analyzed independent from increases in off-shoring and outsourcing of fabrication by US companies or the increasing economic value of products. US Census data from 1995 to 2005 show that the total electricity consumed by the semiconductor industry in the USA, when normalized per area of silicon consumed by the industry, did not increase significantly from 1995 to 2005 [33, 34]. The energy consumption per area of silicon consumed increases and decreases slightly over time, but was roughly the same in 2005 as in 1995, approximately 1.5 kWh/cm^2 [21, 34].

Energy efficiency goals have largely been achieved through changes to fab facility systems. Throughout the industry, improvements have been made to the energy efficiency of nearly all of the major fab systems: water cooling, exhaust flow, water distribution, clean room air flow, CDA and facility nitrogen delivery systems, and chamber vacuum pumps. Facility energy efficiency improvements can be classified as advancements in both the technologies and in the techniques applied in fab design and operation. Higher efficiency pumps and fans, variable speed drives (VSDs), and improvements in ducting and clean room airflow arrangement such as mini-environments represent technological developments. Reduction of pressures in CDA and exhaust systems, optimization of clean room temperature

and air speed, and the use of larger cooling towers to allow reduced chiller size are examples of operational improvements.

These advancements are reflected in the model for each technology node in this study. At the 250 nm node, the pressure maintained in the CDA delivery system is increased to support stepper systems required for this generation's photolithography tools. (This change does not enhance energy efficiency but was necessary to enable pneumatic stepping for lithography.) At the 180 nm node, the air change-over rate (ACR) is reduced in the clean room heating ventilation and air conditioning (HVAC) system, allowing fans speed to be lowered, the scrubber exhaust pumps are upgraded, a smaller and more efficient chiller, using a VSD, is installed; chiller use is also reduced by increasing the size of the cooling towers. Total facility energy consumption is cross-verified against industry reports and published literature [35, 36].

The wafer yield (good chips per wafer), line yield (finished wafers per wafer starts), and chip size are key variables which influence the environmental impacts per chip. The values for these parameters at each technology node are based on industry average data [35].

Power data for process tools are based on measurements taken using three phase power measurement equipment, which have a maximum error of $\pm 2.6\%$. Power requirements for facility systems are determined using mass flow analysis and facility energy consumption models, which are developed based on data from industry and technical reports [37, 38]. Power and facilities requirements for process tools are from process equipment measurements [39] and requirements for abatement equipment are based on manufacturers' specifications, which have an undefined error.

Process Emissions. The abatement of some PFC emissions are regulated by the Kyoto Protocol (in Annex I and II nations) and, in 1999, the World Semiconductor Council (WSC), which includes the semiconductor industry associations of Japan, Europe, Korea, Taiwan, and the USA, issued a position paper which committed members to PFC emissions reduction by 10% of 1995 or 1999 baseline levels by the end of 2010. However, more than half of semiconductor production occurs outside of Kyoto Protocol Annex I and II nations, and, in 2008, almost 20% of semiconductor production capacity was held in China, Singapore, and Malaysia, where the industrial consortia have not joined in the WSC. Thus, although PFC emissions may be abated in some fabs in China, the assumption is made that there are no controls on PFC emissions at the Chinese production site.

GWG emissions from each process step have been determined, pre- and post-abatement, using in situ mass spectrometry and Fourier transform infrared (FTIR) spectroscopy analysis by a procedure which requires mass balance to be closed within 10% of chamber inputs. Each of these measurements thus has a maximum uncertainty of $\pm 10\%$ for each element. For most materials, the uncertainty of the total mass of emissions per finished wafer can be considered as a uniform distribution with variance equal to $(10\%)^2$ of the expected value. For NF_3 which is at more than 30 points during processing of a single wafer the uncertainty is reduced via the central limit theorem, and the total mass flow is modeled as a normal distribution with variance equal to $(3.3\%)^2$ of the expected value. GWPs are taken from [40].

Table 7.6 GWP intensity of transportation [1]

	Distance, fab. to assembly (miles)	Distance, assembly to use (miles)	CO_2 intensity (g CO_2eq./ton-mile)	Energy intensity (MJ/ton-mile)
Truck	50	200	187	2.7
Air freight	3,000	3,000	18	0.38

7.6.3.7 Transportation

Chips are typically cut and packaged at a facility separate from the wafer fabrication site, often in a different country or on a separate continent altogether. Semiconductor products therefore travel twice within the production phase: wafers are transported from the fab to an assembly plant, where they are cut into die, packaged into chips, and tested and finished chips are then transported to the place of eventual use.

The global industry of semiconductor packaging and testing, or "back-end" processing, is clustered in Vietnam, Malaysia, Costa Rica, Puerto Rico, China, and the Philippines. Costa Rica is the closest location to Santa Clara and is therefore the location of assembly designated in this study.

Travel from the wafer fab to the assembly facility is taken as 50 miles by truck and 3,000 miles by plane, and from assembly to the final POU, travel is 3,000 miles by air and 200 miles by truck. Energy consumption and GWP of emissions for truck and air freight are from [41]. The distance of each travel leg and its corresponding GWP impact and energy intensity is given in Table 7.5.

It is assumed that between wafer production and assembly, the finished wafer is transported in a wafer carrier and additional casing with a total weight of 500 g per 200 mm wafer or 700 g per 300 mm wafer. Between assembly and use, the product and packaging has an assumed weight of 20 g regardless of technology node. The total energy and GWP intensity of transport for each technology node is detailed in [1].

7.6.3.8 Use Phase

The use phase represents the power consumption of the chip assuming an average power supply efficiency of 70%. The lifetime of the chip is taken to be 6,000 h (3 years, being used 8 h a day, 5 days per week, and 50 weeks per year) in a 70% active state, representing a business user. An assumption of 3 years is consistent with the literature, which identifies the typical lifespan of personal computers as 2–3 years in business applications and 4–5 years in residential use [33, 42, 43]. The lifetime assumed in this study would also be equivalent to an 18-month lifespan of a data center processor, operating continuously, with 95% uptime, at a 30% activity rate.

The average power requirements for logic chips are taken from the 2001 to 2007 International Semiconductor Manufacturing Roadmap reports [4, 35, 44] and, for years previous, from manufacturer's specifications. These power values represent operation at full capacity or at a 100% activity rate (Table 7.7).

Table 7.7 Use-phase power by technology node [1]

Technology node (nm)	350	250	180	130	90	65	45
Year	1995	1998	1999	2001	2004	2007	2008
Power (W)	14	23	25	61	84	104	146

The average chip power demand has risen from 14 to over 140 W over the past 15 years. The steady increase in power requirements for logic chips is the main cause of rising energy-related life-cycle impacts, as will be shown in Sect. 7.6.4.

In order to compare impacts on a common basis of operational performance, the rate of instructions performed, usually denoted in million instructions per second, MIPS is used, rather than clock speed or transistor density, as a common metric of computational capacity. Transistor density is not ideal as a computational power metric because while increased transistor density usually results in increased computational power, the relation is not necessarily proportional. Although clock speed, which is dependent on transistor density, is used as a popular measure of a CPU performance, computational power is determined by the CPU's architecture, instruction set, cache size, and memory speed as well as clock rate. The rate of instructions in MIPS accounts for both the speed and design of the chip but remains highly dependent on the instruction sequences used to define the metric. Though instruction rate falls short of providing a perfect description of a CPU's performance as processors with different instruction sets or architectures are not comparable, instruction rate is a more representative metric than clock rate or transistor density and is a commonly reported measure of performance. MIPS is thereby used in this analysis as a metric for comparison based on computational performance.

7.6.4 Results and Discussion

As technology has progressed, life-cycle energy use and greenhouse gas emissions have in general been increasing per wafer and per die but decreasing when normalized by computational power. Figure 7.3 shows how total life-cycle energy demands per wafer, per die, and per 1,000 MIPS have changed over the period under study.

The increases in per-wafer and per-die life-cycle impacts have one dominant cause: the escalation of use-phase chip power. The growth in per-wafer impacts, however, is also due to the lengthening of the manufacturing process flow and concomitant expansion in manufacturing infrastructure and equipment, as shown in Fig. 7.4.

At each technology node, the complexity of device design has increased, and the number of process steps required to produce a finished wafer has escalated. In this model, for example, production of a finished wafer entails 147 process steps at the 350 nm node, while the process flow for a 45 nm device consists of a total of 251 process steps. The lengthening of the process flow follows from increasingly

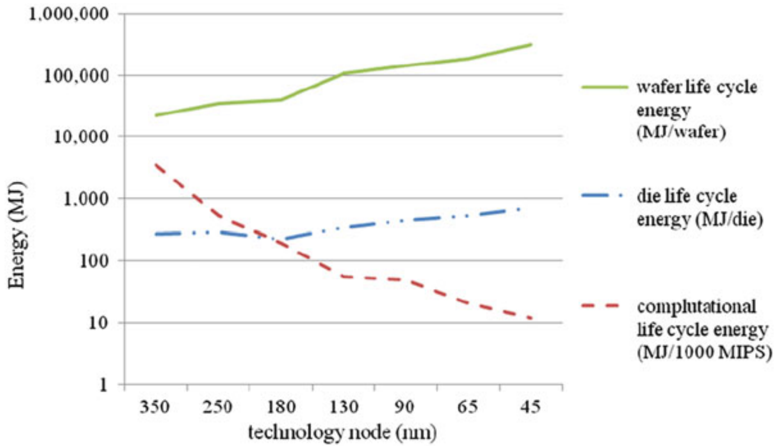

Fig. 7.3 Energy use per die, per wafer, and per 1,000 MIPS by technology node [1]

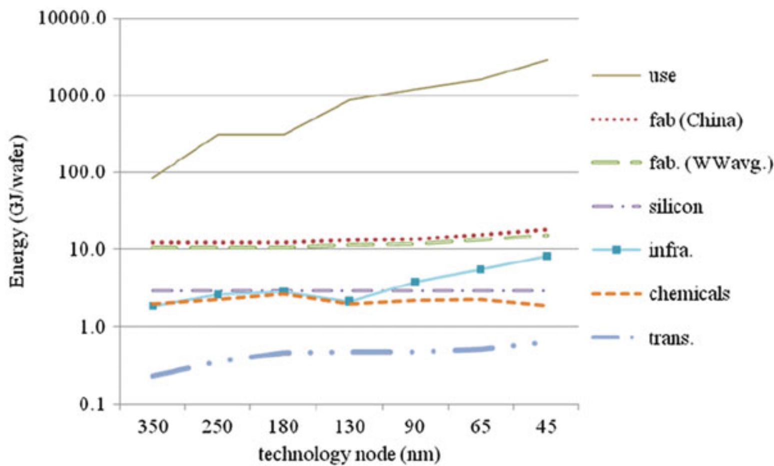

Fig. 7.4 Energy use per 300 mm wafer equivalent, by life-cycle stage, over seven technology nodes [1]

detailed construction necessary to scale down the device's transistors as well as additional interconnect layers to wire them together.

Growth in manufacturing and materials-related impacts over time has been counteracted by shrinking die sizes, which allow more die to fit on each wafer. Thus, use-phase power is the lone reason for increases in impacts per die. For all technology generations, the use phase represents the largest proportion of energy-related impacts per die among the life-cycle phases. The dominance of the use phase has also increased over time, with use contributing about 51% of life-cycle

GWP consumption per die at the 350 nm node, and over 95% per die at the 45 nm node. Despite the long distances that semiconductor wafers and chips are typically shipped during production and prior to use GWP of transportation is almost insignificant due to the small mass of the product.

The improvement of several production performance metrics has allowed reductions in the manufacturing energy and GWP per chip. Line yield reflects wasted processing used for process monitoring, testing, and wafer loss in the form of damage or breakage. Although wafer damage has remained the same over the years, at about 2%, the number of test or monitor wafers per finished wafer has been reduced over the last decade, resulting in higher average line yields [20, 45–47]. Although reduced feature sizes have made maintaining wafer yield difficult, industry reports indicate that wafer yields for full-scale production have not fallen with decreasing device dimensions. Mature wafer yield is assumed to be 75% for all technology nodes, based on ITRS reports [4, 35, 44].

The results of this study enable LCA practitioners to answer important questions concerning the energy-related environmental impacts of computing with greater certainty than ever before. The life-cycle impacts for energy and GWP of semiconductor chips presented in this analysis are more complete, accurate, and transparent than those of any previous study, and data are presented for chips spanning many generations, from 1995 to 2010. Energy and GWP impacts for semiconductor logic chips are clearly dominated by the use phase. Chip power demand and the GWP of use-phase electricity are thus the variables with the largest influence over energy-related life-cycle impacts. Production yield, die size, geographical location or electrical energy supply of the plant, and the choice to abate PFCs are the most important metrics and decisions to be made concerning energy and GWP impacts in the production stage.

7.7 Conclusion

Semiconductor manufacturing, a manufacturing sector which supports growth in many areas of the world economy, has been a major consumer of resources and source of environmental impacts. The industry has made great strides to improve efficiency of resource utilization (from energy to materials) motivated by both cost savings and environmental, health, and safety considerations. Hence, it is almost a "poster child" example of green manufacturing analysis and technology development. This chapter has introduced the basics of semiconductor manufacturing and, then, provided a detailed analysis of the energy and global warming impact of manufacturing one typical semiconductor product, the CMOS chip. This chip, ubiquitous in many consumer products today, offers an example of the benefits of technology advances as well as the challenges. The life-cycle analysis of CMOS fabrication and use (including materials processing through transportation and use phases) illustrated the level of data detail required and demonstrated trends in manufacturing over several technology nodes. This same approach, relating

environmental impact in terms of GWP, resource consumption, or other measures, is applicable to a wide variety of products. The LCA study presented in this chapter highlights the importance of identifying of the proper functional unit in semiconductor LCA, as impacts per die, per wafer, and per 1,000 MIPS may be applicable in different contexts, but yield contrasting trends over time.

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