Chapter 7
Substrate Technology

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Abstract A flip chip package started with a ceramic substrate at the beginning. A Low CTE chip (silicon: 3 ppm/°C) and a relatively low CTE substrate (alumina: 8 ppm/°C) with a ductile solder joint (high lead solder) provided a good reliable system for high density packaging. However, it has disadvantages such as high cost, low electrical property, largeness, and heaviness. In early 1990s, an organic substrate utilizing an epoxy base printed circuit board technology has emerged. An underfill resin fills a gap between a chip and substrate and resolves a stress issue by a large CTE mismatch of a chip and an organic substrate (17 ppm/°C). In this system, the stress at a flip chip joint is dispersed in to the total package entity. This technology opened a door to low cost, high electrical property, small and light package, and has spread throughout semiconductor packages. In this chapter, a major focus is put on the organic substrate technology. The material, process, and reliability influences to a package are described in detail. Particularly, it is emphasized that the basics why the organic substrate is designed in such a way as we see today. Though there are many variations in the organic substrate technology, the basics are common and very important for a productive and reliable package, and the future progress of a flip chip package is strongly dependent on the progress of such basics.

7.1 Introduction

In the beginning, the substrate of flip chip package was a ceramic material. The practical use of it started with SLT (Solid Logic Technology) package that was employed on IBM System/360 announced in 1964. A substrate size was a half inch square with PGA (pin grid array) configuration. A size of substrate has been enlarged

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within the next generation from a half inch square to the most popular size 35 mm square PGA that was MST (Monolithic System Technology) package. Its first version was announced in 1970. There were further larger sizes according to requirements, but the 35 mm PGA was predominantly used from the middle of 1970s and 1980s. Not only a size increase but also a multilayer construction has come in to satisfy a density increase requirement for higher system performance. The major peak of such an innovation was the emergence of TCM (thermal conduction module) employed in IBM System/308X series, 35 layers with 90 mm square substrate at the starting point that carried 131 chips at maximum case. The property and nature of ceramic substrate were well explored and good descriptions were provided in the past. One of the examples was a book "Microelectronics Packaging Handbook" edited by Tummala and Ymaszewski [1]. Due to such assets through history, this chapter does not touch in detail the description of ceramic substrates except some cases for comparison purpose, and puts emphasis on organic substrates.

Within the age of ceramic substrates, a flip chip technology was a valuable asset of packaging but usage was limited mainly in high performance area due to its high cost. In the meantime, a requirement for system usage has been shifted from high end to low end along with spread of network throughout the world, i.e., the so-called wave of computer downsizing. A major event that responded to such stream was the emergence of organic substrate for flip chip packaging technology announced from Yasu Technology Application Laboratory, IBM Japan in 1991 [2]. It consisted of two parts. One was an underfill reinforced flip chip bonding technology that enabled to attach bare chip to epoxy base substrate that has large CTE (*coefficient of thermal expansion*) mismatch to silicon chip [3] and the other was a build-up PCB substrate technology that enabled to accept high I/O of flip chip by the structure similar to a semiconductor with blind via hole, so called micro-via hole, for fine pitch wiring connection [4]. Today, after two decades from the emergence, these technologies are widely spread in low cost, small and light and high performance areas such as supercomputers. Also, significant numbers of derivative technologies are used in many applications. A production of total organic substrate group has reached to 20 % of world PCB production at the end of 2010 in financial basis. However, the technology is still exploring to adopt various situations. This chapter is intended to describe its basics and backgrounds to understand the nature of technology that makes it possible to handle future applications without facing a major reliability issue and with better efficiencies.

7.2 Type of Construction

There are basically two types of structure in organic micro-via substrate. One is a sequential build-up type shown in Fig. 7.1a and the other is Z-stack type shown in Fig. 7.1b.

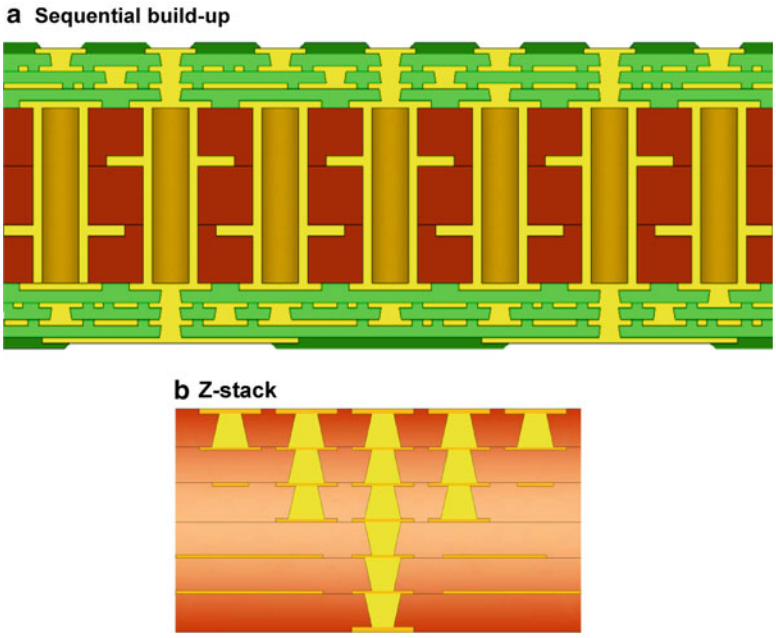

Fig. 7.1 Build-up substrate variations. (**a**) Sequential build-up, (**b**) Z-stack

7.2.1 Sequential Build-Up Structure

A sequential build-up type has a core at the center that employs ordinary PCB technology and build-up layers on both side of the core that employs micro-via hole for layer to layer connection. The role of core is to provide mechanical rigidity and power layers with containing thick Cu conductor plane. Build-up layers are processed sequentially put over on both side the core to provide high density wiring for flip chip bonding. Since the core provides mechanical stability during the fabrication process, a sequential build-up type has higher dimensional stability that is a key to achieve high density wiring. A weak point of sequential build-up type is at through holes that connect front and backside. The pitch of through hole is relatively low density since the bare hole is made by a mechanical drilling process. As the result, utilization of backside wiring layers is relatively low compared with front side though layers cannot be reduced to avoid an unbalanced structure that creates a warpage. A warpage is a common issue in organic substrate technologies due to low modulus of material and becomes an obstacle for assembly to the next level. Another weak point is an increasing process yield impact along with an increasing layer count. It is a predestinate nature of a sequential build-up. The total process yield of build-up layer fabrication follows a power-law degradation of each layer yield as formula (7.1).

$$\text{Through yield} = \text{layer 1 yield} \times \text{layer 2 yield} \times \cdots \times \text{layer } N \text{ yield} \quad (7.1)$$

where each layer field is an average of front side and back side yield.

For example, when the construction is "3 build-up layer + core + 3 build-up layer," the total yield is core yield × (average build-up layer yield)^3. By this nature, the yield degrades exponentially as increase of layer count. Therefore, reducing layer count by utilizing high wiring density per layer is a key to reduce the a cost of sequential build-up substrate.

7.2.2 Z-Stack Structure

Z-stack type is called as "any layer via" substrate. Each layer is fabricated with micro-via and a conductor pattern beforehand and stacked necessary layer numbers by press process to complete a substrate. The structure is uniform that can provide a good electrical property. The process is rather simple and possible to achieve low cost. However due to stacking process by high pressure mechanical press required, the alignment capability of circuit pattern and via hole is worse compared with a sequential build-up type. As the result, wiring density per plane is lower than that of sequential build-up type and layer numbers are increased. Other difficulty is that there is a difference in numbers of stacking count of via hole in a substrate. It creates stacking process window narrower. Since a dielectric layer is soft compared with metal in a via hole, a pressure at interface of low numbers stacking via is less compared with high numbers stacking via where a via to via contact force reaches earlier to the required level. It requires more pressure to low numbers stacking via reaches to the required level that impacts the registration degradation further.

The basic natures of fabrication process of these structures are a semiconductor wiring like structure in case of a sequential build-up type and an extension of conventional PCB but using micro-via in case of a Z-stack type. Such natures deliver a difference in a primary application such as a sequential build-up type for high density processor and ASIC chips and a Z-stack type mostly for consumer products.

7.3 Sequential Build-Up Substrate

Figure 7.2 shows a cross section photograph of a typical flip bonding on organic substrate. The substrate has a core at the center and high density build-up layers with micro-via hole are on both side of the core. The core provides power planes and the build-up layers provide flip chip fan-out wirings. On the surfaces of substrate, there are terminal pads for flip chip bonding on the front side and BGA

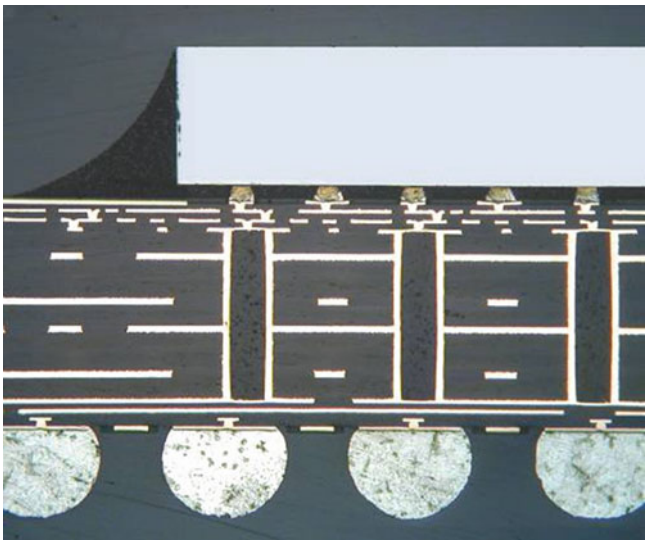

Fig. 7.2 Typical organic package cross section. After Tsukada, [5]

terminal pads on the back side. A gap between chip and substrate is filled with underfill resin to protect flip chip joints.

7.3.1 Process Flow

Figure 7.3 describes a fabrication process step of sequential build-up substrate. The figure shows a single side only but actual processes are implemented on front and back side simultaneously.

(a) The process starts from making a core with an ordinary PCB structure. Plated through holes are filled with resin contains some silica filler and capped by copper plating so that a via hole of the next layer can be placed directly on through hole.

(b) On both side of the core, a dielectric resin is applied by vacuum laminator and cured in a half way. Via hole are drilled by a laser. The surface of resin and inside of via hole is treated by permanganate to provide necessary roughness for copper plating and, at the same time, clean a resin smear in a via hole after laser drilling.

(c) A seed layer is formed with an electro-less copper plating on the surface and inside of via hole. A Pattern resist is applied, expose and develop to form a circuit pattern negatively. Then, an electro-copper plating is applied to make a conductor pattern. Via holes are plated at the same time. Pattern resist is removed after forming a conductor pattern. The dielectric resin is finally cured.

(d)–(g) Process is repeated to make necessary numbers of build-up layer.

(h) A solder mask resin is applied to cover entire surface and cured in a half way.

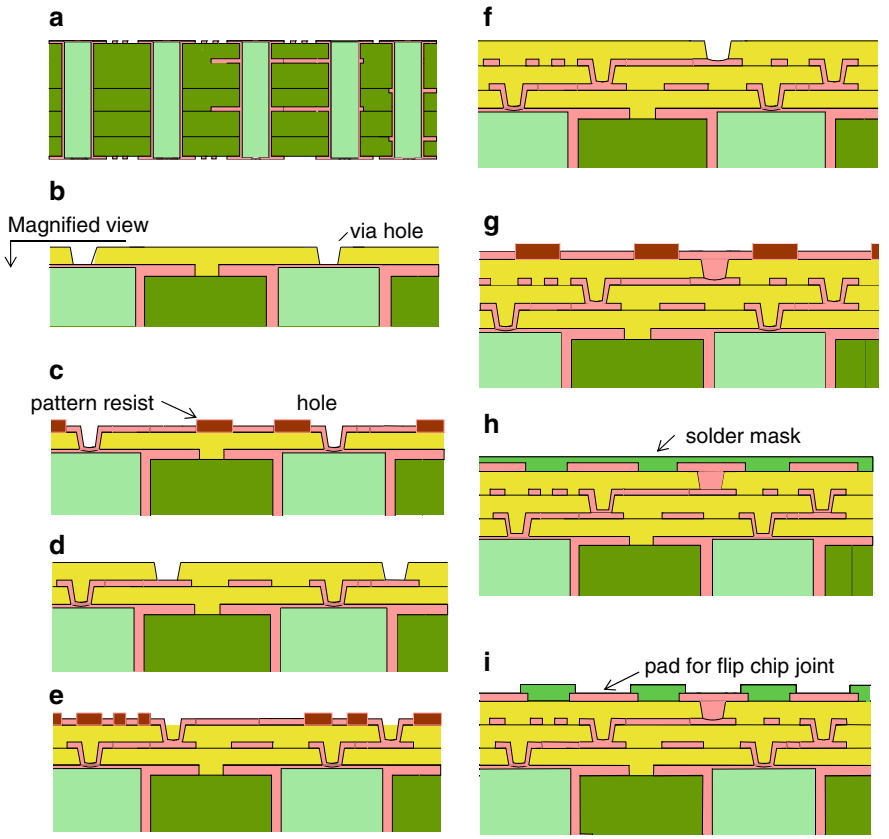

Fig. 7.3 Process flow of sequential build-up

(j) Pads for flip chip joint are formed by photo-etching of solder mask resin. A solder mask resin is cured completely.

7.3.2 Conductor Line

Since an organic substrate employs high definition photo-circuitizing process with a plated copper conductor, wiring density of organic substrate per layer is higher than ceramic substrate that employs a paste printing for conductor patterning. Figure 7.4 shows a concept of escape line design from flip chip bonding area to the area outside of a chip. The figure is assuming 150 μm pitch of flip chip joint and shows a substrate terminal and conductor wiring design in the case. Upper side of the figure is toward for chip center and lower side for chip perimeter. In 150 μm flip chip joint pitch, the dimension is shared 75 μm to a terminal pad and 75 μm to a space

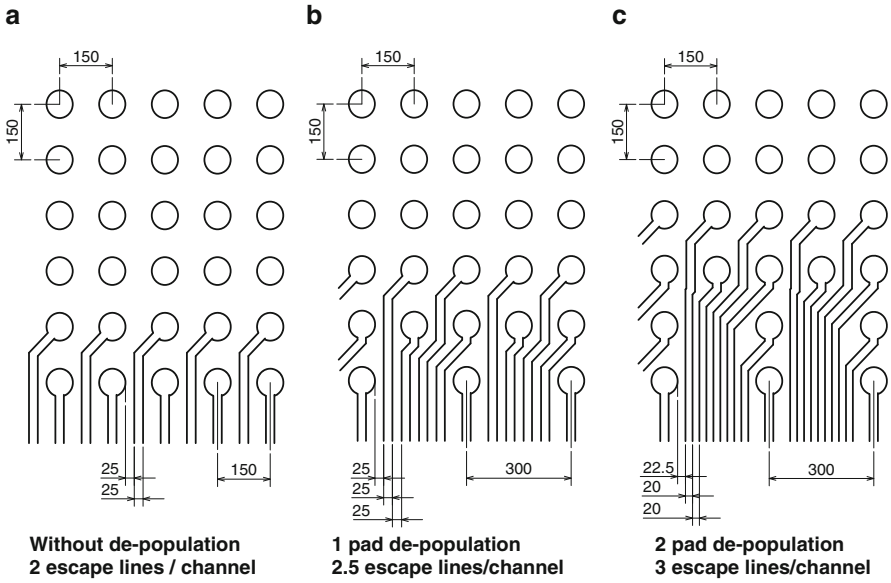

Fig. 7.4 Escape line design. (**a**) Without depopulation 2 escape lines/channel, (**b**) 1 pad depopulation 2.5 escape lines/channel, (**c**) 2 pad depopulation 3 escape lines/channel. After Tsukada [5], 2002

between pads. When there is a 75 μm space between pads, it can be divided to 25 μm space, 25 μm line and 25 μm space. i.e., one 25 μm line can escape between terminal pads. As the result, two lines can be drawn out simply from the first and second row as shown in (a) of the figure. Escape lines can reach to two rows inside from the chip perimeter. Taking some optional arrangement, following cases can be considered. If one pad is deleted from the first row that is the lowest row in the figure, four lines can escape between the first row pads with same 25 μm line and 25 μm space rule. As the result, five lines can escape from two pitch of flip chip joint. i.e., 2.5 lines escape per 150 μm is achieved. The deletion of one pad increased numbers of escape line and escape lines can reach deeper to the third row from the chip perimeter. If the capability of fabrication can provide a finer line width, more lines and more rows can be managed with repeating the same way. 20 μm line/20 μm space capability can provide three escape lines per 150 μm pitch and reach to four rows inside. Since this figure shows signal lines only, an actual design is much more complicated because many power pads must be placed among signal pads. But, this concept indicates an importance of design collaboration between a chip and a substrate designer. If the collaboration between a chip and a substrate is not maintained, a design may end up with higher cost and/or performance degradation.

High density organic substrate for flip chip bonding uses a pattern plating (semi-additive plating) to form copper conductor lines. Figure 7.5 shows pattern resist after development (a) and actual lines made by copper pattern plating (b). Lines are 30 μm

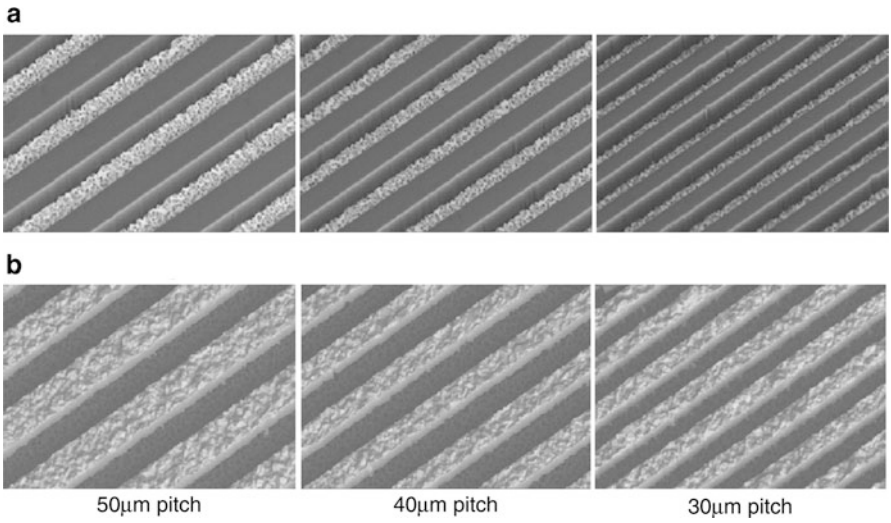

Fig. 7.5 Pattern plating. (**a**) After plating resist development, (**b**) after Cu plating. After Tsukada [5], 2002

pitch (15 μm line/15 μm space), 40 μm pitch (20 μm line/20 μm space), and 50 μm pitch (25 μm line/25 μm space). In between pattern resist lines, surface asperity to sustain an adhesion of copper to a dielectric material. It is actually seen an electro-less copper surface plated over a dielectric resin. In the meantime, a surface of copper conductor line after plating also shows asperity that is formed by granularity of copper plating.

Figure 7.6 shows a test result of copper adhesion to a dielectric material. The adhesion test is set by peel strength of 1 cm copper strip that is pulled perpendicular to the plated surface along with bake time of samples up to 240 h (10 days). In the figure, a peel strength trend of samples from four different lots (1 through 4) with $n = 30$ and 90 is shown. A peel strength is down about 20 % at the first reading but not degraded further, and slightly increased toward the end of test by aging.

The bake temperature is defined with a following formula.

$$t2 = 1.076(t1 + 288) - 273 \tag{7.2}$$

Where $t1$: maximum temperature of application.

$t2$: bake temperature of test.

The result of test is evaluated to a certain minimum peel strength of copper strip defined in a specification. This procedure is described in UL specification for organic material degradation by environmental aging. Though there is a formal aging test, this 10 days bake test that is a simplified version of the formal test is used

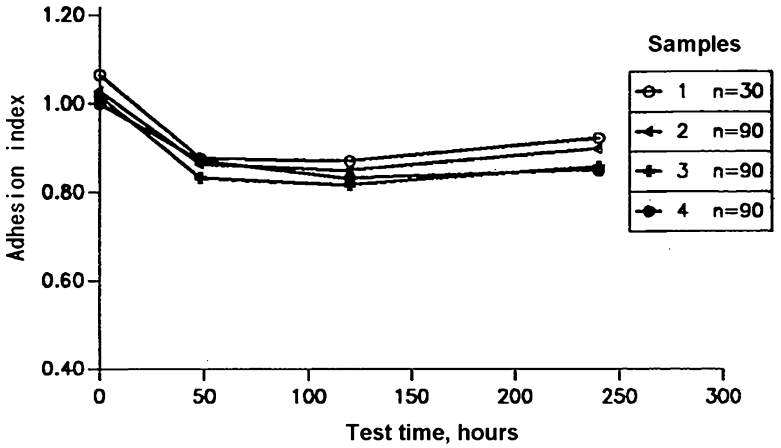

Fig. 7.6 Copper peel strength. After Tsukada [6], 1998

commonly. In case of ordinary PCB material (FR4), a minimum adhesion strength is normally more than 1 kgf per 1 cm copper strip (38 μm in thickness) peel at the initial value. In case of build-up substrate material, an adhesion strength is lower than that of ordinary PCB but enough to meet a degradation limit of the test. The difference in initial adhesion strength is due to a difference in anchor mechanism of copper. In ordinary PCB, a dielectric resin is pressed to copper foil that has an asperity for adhesion. In the meantime, in build-up substrate, copper is plated to asperity of resin surface created by an etching of the resin. There are two major requirements of UL to an organic substrate. One is this adhesion degradation test and the other is a flammability of dielectric material.

Figure 7.7 shows a cross sectional photograph of lines immediately after a pattern resist removal. There is a seed layer on dielectric material for providing a cathode in pattern plating. It is formed by electro-less copper plating that is adhered to roughened surface by permanganate etching. To maintain necessary adhesion of a line, a formation of good anchor mechanism is a critical point of pattern plating. In the photo, it looks the line width is a little wider than the space between the lines. This is intentionally designed such a way to keep a line dimension as designed after a seed layer etching. When a seed layer is etched, a surface of line is also etched and the line width becomes narrower to be a designed nominal value. The next figure describes the situation in more detail.

Figure 7.8 shows a magnified view of "50 μm pitch with 25 μm line and 25 μm space" cross section before a seed layer etching process. A surface of dielectric has irregular asperity formed by permanganate etching to provide mechanical anchor for copper plating adhesion. Electro-less copper covers the asperity surface. This photograph is a result of following processes such as permanganate etching of dielectric, electro-less copper plating, pattern resist apply, expose, develop, and electro-copper plating in sequence. In the middle of photograph, there is a pattern

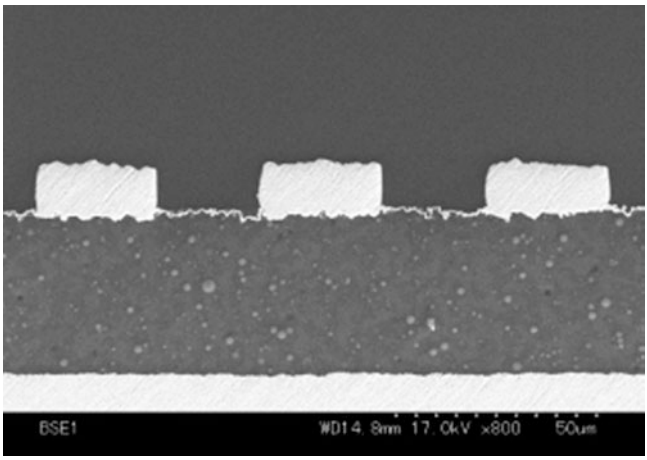

Fig. 7.7 Cross section of seed layer. After Tsukada [5], 2002

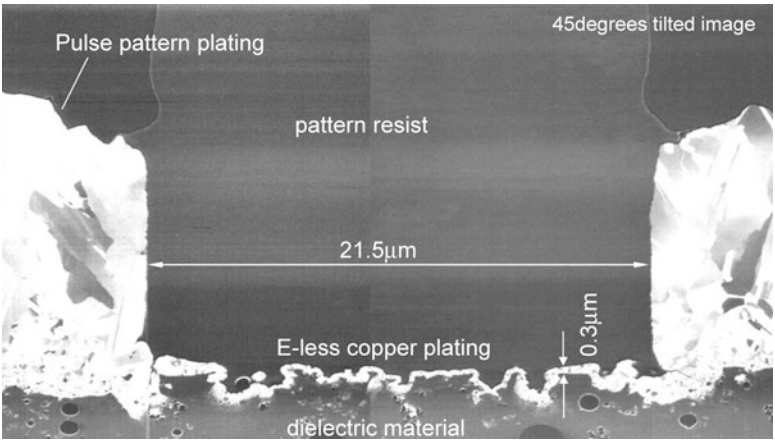

Fig. 7.8 Pattern plating cross section. After Tsukada [5], 2002

resist that occupies an area of space between lines. There are lines on both side of resist that are formed by an electro-copper plating. A space between copper lines is 21.5 μm in width. After resist removal, a seed layer etching removes electro-less copper plating on a dielectric material. At the same time, the surface of lines is etched and the space width becomes wider from 21.5 to 25 μm that is a nominal dimension of the design. In contrast, the line becomes narrower from 28.5 to 25 μm and also reaches to a design nominal. As this photograph, a line always must be wider for seed layer etching margin, a pattern resist in a space is always narrower for the size of etching margin. Therefore, the asperity of seed layer must be smaller when the line pitch is reduced. Otherwise, a yield of resist patterning is significantly deteriorated due to form too narrow resist with high aspect ratio. By this

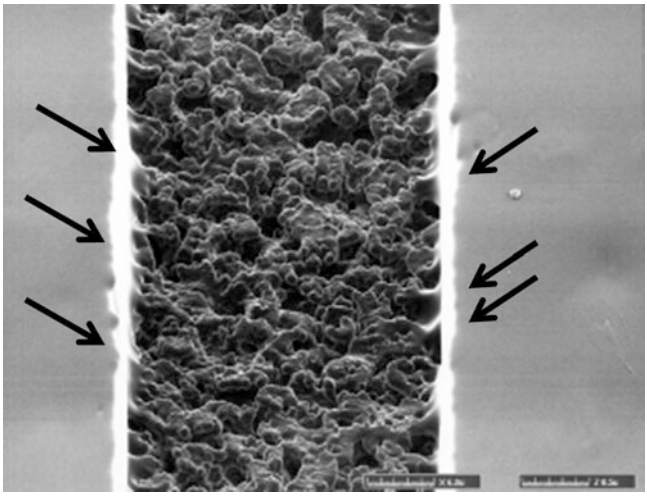

Fig. 7.9 Residual copper whisker at line edge. After Tsukada [5], 2002

dimensional issue, there is a strong demand to reduce a surface asperity of dielectric material with maintaining adhesion of copper plating to necessary level for processability and reliability.

There are other reasons that request a surface asperity of dielectric resin smaller. Figure 7.9 shows a residual copper whisker after seed layer etching. When a seed layer is etched, it takes longer time to etch out a copper in a large concave in surface asperity. In addition, since an adhesion of pattern resist to such asperity is not perfect, there is a narrow extrusion of copper under the edge of pattern resist occasionally remained as indicated by arrows in the photo. When a line pitch is reduced and a space becomes narrower, such phenomenon becomes more critical and sometimes violates a minimum space limitation. Also such extrusion becomes a starting point of copper migration due to a concentration of electrical field that eventually cause a reliability problem.

Another reason is that a skin effect describes later brings a major requirement to reduce such asperity. An original dielectric material shows 1–3 μm anchor depth and it is reduced to less than 1 μm these days by changing the resin formulation and filler size reduction. Other than such reduction of asperity, there are other activities to secure adhesion of copper without asperity by modifying surface property of resin [7] or providing molecular interface between copper and resin [8].

In addition to adhesion of copper on a dielectric resin, adhesion of a dielectric resin on copper is equally important. No matter where bottom or top of line, losing adhesion causes stress concentration at somewhere inside of a substrate and cause a crack during thermal cycle when in use. Conventional PCB uses oxidation of copper to form microscopic structure as shown in the figure (a). However, internal stress of flip chip substrate is much higher and other mechanism is required. Since a copper oxide is easily dissolved by acid, a defect called “pink ring” that is a separation of

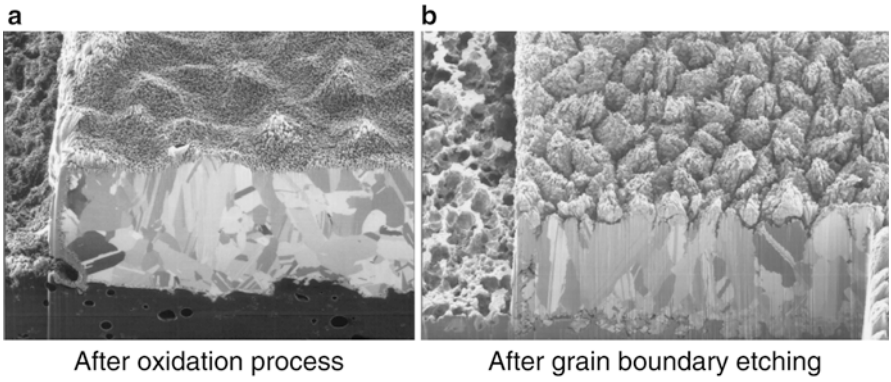

Fig. 7.10 Copper surface asperity. (**a**) After oxidation process, (**b**) after grain boundary etching. After Tsukada [5], 2002

dielectric from copper surface appears around laser drilled micro-via hole and propagate to area around by temperature excursion of thermal cycle. Figure 7.10 shows a view of anchor mechanism provided by etching of copper grain boundary of conductor line surface. The anchor size is a few microns. Eventually shown in the photo, there are asperity for anchor at the bottom and top of line as shown in the figure. There are activities also to reduce this side asperity of copper conductor that are to create finer asperity by a chemical reaction with maintaining required adhesion or add interface material or molecule layer similar described in the previous figure.

Besides pattern plating, a subtractive etching process is used for patterning a copper. It has its own improvement by anisotropic etching. Figure 7.11 shows an effect of etching chemical for this purpose. In the figure, line and space geometry of etching resist is 30/30 μm. An etching resist thickness is 10 μm and copper thickness is 20 μm. (a) Shows a result of copper geometry by a conventional etching solution. From top to bottom picture, etching of copper progresses isotropically that shows entire etching front is moving in semi-ellipse shape. As the result, top of the line becomes quite narrow compared with the bottom. In the meantime, (b) shows a progress in the case of anisotropic solution. From the beginning of the step, line wall is formed vertically and only an etching front at the bottom is showing semi-ellipse shape. It is noticeable that this is the result of anisotropic etching chemical used. The result shows almost complete rectangular shape of lines in cross section even though this is a subtractive etching.

Figure 7.12 shows how a chemical works for this anisotropic etching by steps (a) through (d). A chemical contains an etching inhibitor that selectively deposits on a side wall because a working solution flow is weak there compared with a bottom. As its progress, the inhibitor forms a film on the wall and a direction of etching is controlled by the inhibitor film. Finally, very high etching factor is obtained with forming vertical side wall.

Table 7.1 describes a property of dielectric material “ABF GX13” with other innovative versions from Ajinomoto Fine-techno Co., Inc. GX13 is a de facto

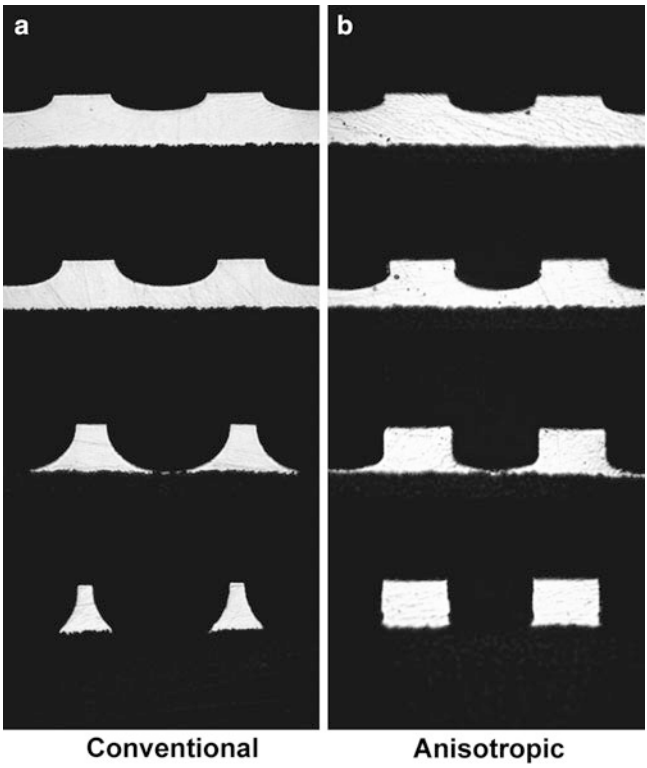

Fig. 7.11 Anisotropic etching. (**a**) Conventional, (**b**) anisotropic. Courtesy of MEC Co., LTD

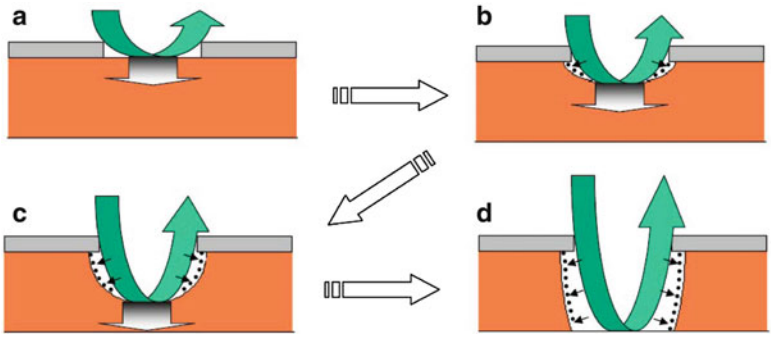

Fig. 7.12 Mechanism of anisotropic etching. After Toda, MEC Co., LTD. [9], 2011

standard material of dielectric resin for an organic substrate today. It is an improved version of the predecessor "GX3" that has a higher CTE as 60 ppm/°C. CTE is lowered to 46 ppm/°C by mainly increasing filler amount in the resin. Lowering CTE supports not only to reduce *X*–*Y* direction CTE but also, more importantly, to reduce

Table 7.1 Dielectric material, after Mago [10], 2011

Material name			G X 13	G X 92	G Z41
Features			Low CTE	Low profile	Low tan δ
CTE	ppm/°C	x–y, 30–150 °C	46	39	20
CTE	ppm/°C	x–y, 150–240 °C	120	117	67
Tg	°C	TMA	156	153	176
Tg	°C	TMA	177	168	198
Young's modulus	GPa	23 °C	4.0	5.0	9.0
Tensile strength	GPa	23 °C	93	98	120
Elongation	%	23 °C	5.0	5.6	1.7
Dielectric constant		Cavity resonance at 5.8 GHz	3.1	3.2	3.3
Dielectric loss		Cavity resonance at 5.8 GHz	0.019	0.017	0.0074
Water absorption	wt%	100 °C, 1 h	1.1	1.0	0.5

Z-direction CTE of the substrate as previously described. In the electrical property, a dielectric constant of GX13 is low as 3.1 because there is no glass in the film for electrical property and smaller via hole size capability. It is not provided in the table, but glass epoxy layer in an ordinary core has a dielectric constant around 4.2. A dielectric loss is 0.019 that is far higher than a ceramic substrate but it is offset by low resistivity of plated copper wiring in case of an organic substrate compared to a ceramic substrate with a paste wiring. Water absorption is 1.1 % but epoxy is essentially a hydrophobic material and there is no issue for electro chemical property as far as a material is cured appropriately. Instead, an attention must be paid a solder reflow in high humidity environment that may cause a delamination between a resin and copper conductor and sometimes with other resin material.

There is a low profile version in the table that covers a requirement for surface asperity lower to maintain a skin depth control and geometry issues that are also already described. Figure 7.13 shows a comparison of surface asperity profile of ABF by 3500× magnified SEM images. (a) Shows a regular profile of GX13 that is 600–700 nm in Ra with copper strength 0.7–0.8 kgf per cm peel in a test described previously. (b) Shows a profile of improved version reduced to 300–400 nm in Ra with slightly lower peel strength but maintained enough for required level.

In Table 7.1, there is a low tan δ version of ABF. It is very important to reduce a dielectric loss in an organic substrate for high performance area since a dielectric loss of epoxy is an order of magnitude higher than that of a ceramic (Alumina). Figure 7.14 shows a simulation of signal attenuation in an organic substrate. In this figure, a signal loss is calculated with a sum of resistive loss of copper conductor and dielectric loss. Two different dimensions of signal line that are 25 and 50 μm with 10 μm in thickness and three levels of dielectric loss are compared. If is clearly shown that a signal attenuation is improved when a line width is wider that lower the resistive loss and a dielectric loss of material lower. It is rather difficult to improve a dielectric loss than a change of line dimension since it requires a change of material composition that impacts an entire part of substrate manufacturing process and reliability. Since the figure shows signal attenuation per unit length of conductor

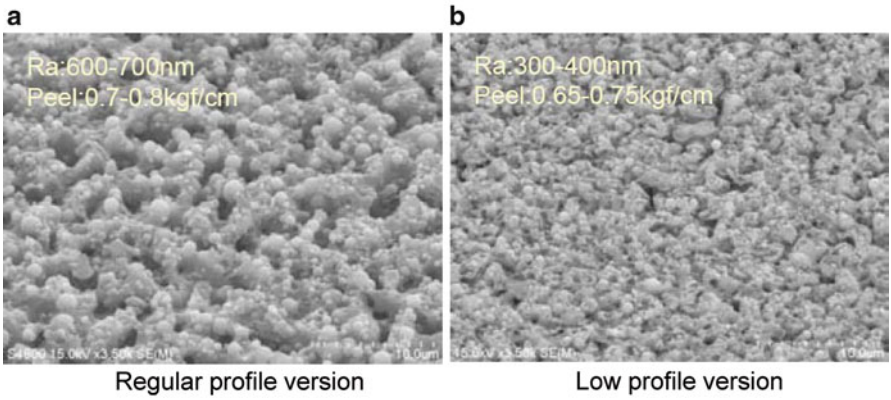

Fig. 7.13 Comparison of surface asperity profile. (**a**) Regular profile version, (**b**) low profile version. Courtesy of Mago, Ajinomoto Fine-Techno Co., Inc. [10], 2011

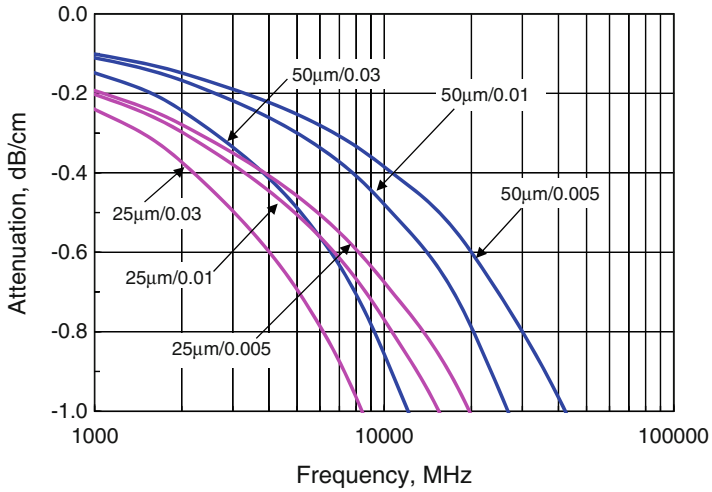

Fig. 7.14 Signal attenuation. After Tsukada, ref. [5], 2002

line, one may recognize that reducing a length of line has a direct effect to improve attenuation. Making substrate smaller directly improves situation even though a resistive loss increases due to a change in line width in the case.

There is other important property of a dielectric resin. Since a dielectric resin has to flow and fill a space between lines and micro-via holes after plating, the resin has to have a good flow nature when laminated to the previous layer. When a dielectric material is applied, there are copper conductor lines as shown in Fig. 7.7 and any other irregular space within a conductor pattern. Also any irregular asperity of dielectric surface and via holes on the previous layer must be filled. In the meantime, it has to be achieved with a low pressure since there is no glass fiber cloth inside of a dielectric

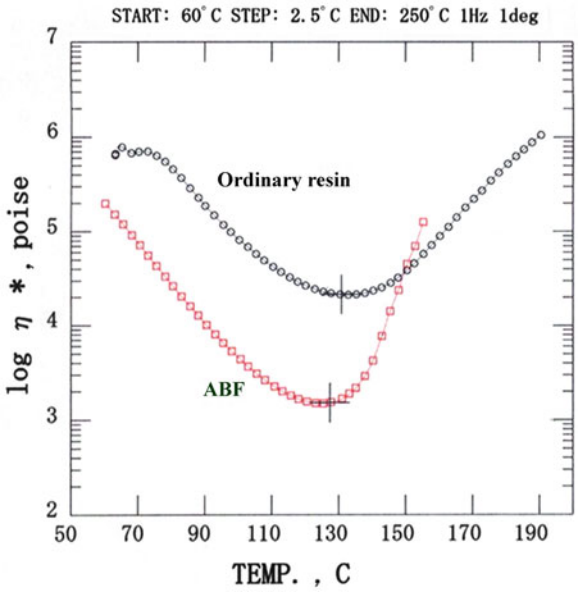

Fig. 7.15 Melt viscosity of resin. Courtesy of Mago, Ajinomoto Fine-Techno Co., Inc. [10], 2011

resin film. A high pressure used for ordinary PCB material like a glass epoxy prepreg flows a resin excessively and difficult to maintain a thickness, or flow out lines on the previous layer. Therefore, low pressure laminator with vacuum must be used. With such conditions, a good flow of resin becomes one of a key property of build-up dielectric resin. In Fig. 7.15, ABF reaches to a quite low viscosity compared with ordinary PCB resin (generally FR4).

7.3.3 Micro-Via Hole

After laminating a film of dielectric resin with low pressure vacuum laminator, the resin is cured in a half way for laser drilling. The reason that a resin is not cured completely is to provide an easier etching of surface at desmear process by permanganate for copper adhesion. In laser drilling, mainly two kinds of laser, CO_2 and UV-YAG, were used for micro-via drilling in a dielectric layer. Table 7.2 describes properties of each laser. In the case of UV-YAG, third harmonic laser, wavelength 355 nm, is listed. The nature of CO_2 laser is high power, low frequency, large beam, and small focus depth. In the meantime, UV-YAG is low power, high frequency, small beam diameter, and large focus depth compared with CO_2. Because of the size of beam diameter and power characteristics, CO_2 laser is used to drill a micro-via larger than 60 μm and UV-YAG for lesser diameters. In the case of CO_2 laser, a micro-via hole with a diameter larger than 60 μm is drilled with a few shots (2–5 shots for 35 μm dielectric thickness) in punching mode. In the meantime, YAG laser

Table 7.2 Laser comparison, after Tsukada [5], 2002

Parameters	UV-YAG	CO_2
Wavelength	355 nm	9.3 μm
Oscillator type	YAG solid	CO_2 gas
Power range	3–7 W	100–300 W
Pulse frequency	40–60 kHz	4–5 kHz
Pulse width	20–200 ns	10–200 μs
Beam diameter	20–80 μm	50–200 μm
Focus depth	100 μm	10 μm
Shot/via	40–70	2–5
Throughput	200–300 vias/s	200–300 vias/s
Work size (typical)	530 × 630 mm	530 × 630 mm
Shot numbers/via (typical)	40–70	2–5
Throughput	200–300 vias/s	200–300 vias/s
Focus depth	100 μm	10 μm

takes several, say ten, shots per via hole in normally tray-pan mode that is a circular shot with small beam to form a necessary via diameter. Due to each frequency, throughput is similar level eventually. In a production tool, multi-head is provided to achieve higher throughput for lowering the cost of drilling.

Figure 7.16 shows cross section photographs of laser drilled micro-via hole. Photo (a) is a drilled hole on a standard epoxy film for build-up layer that has no glass inside. YAG laser with 355 nm wavelength with Tray-pan mode is used in this case. A resulted via diameter is 48 μm at the top. Photo(b) is a drilled hole on a standard glass epoxy layer used ordinary PCB. CO_2 laser with punching mode is used in this case. Since standard glass epoxy layer is thick due to woven glass inside and CO_2 laser that has a larger beam diameter is used, a resulted via diameter is large around 90 μm at the top of via hole. In case of drilling a glass epoxy layer, CO_2 is preferred because an energy absorption to glass is low in case of 355 nm wavelength UV-YAG. Of course 355 nm UV-YAG can drill through a glass but the energy to do that level is high and a risk to punch out copper plane at via bottom increases.

A glass cross in prepreg has been innovated for laser micro-via hole. Figure 7.17 shows glass cross photographs. In case of regular glass cross, since the number of mono filament is large and its diameter is large that make the thread wide and thick, a woven cloth is observed as Photo(a) in the figure when it viewed from top. There are thick bundle area fiber and no fiber area clearly that make a major difference in laser abrasion. In side of drilled hole is rough in shape and diameter is not stable. Photo(b) in the figure shows a flat cross version. Threads are spread and there is no area where threads are vacant and views open like (a). Laser energy is absorbed uniformly and a hole diameter becomes stable. It allows more finer via hole size as a result. Photo(c) shows a cross section of ultrathin glass. The thickness is about 10 μm. Not only thin but threads are completely spread as a single layer of mono filament. This cloth can provide ultrathin substrate or thin build-up layer with a glass cross inside to reinforce a dimensional stability of substrate.

After laser drilling, a bare hole is cleaned with permanganate to remove a carbonated resin smear caused by laser heat. At the same time, the permanganate

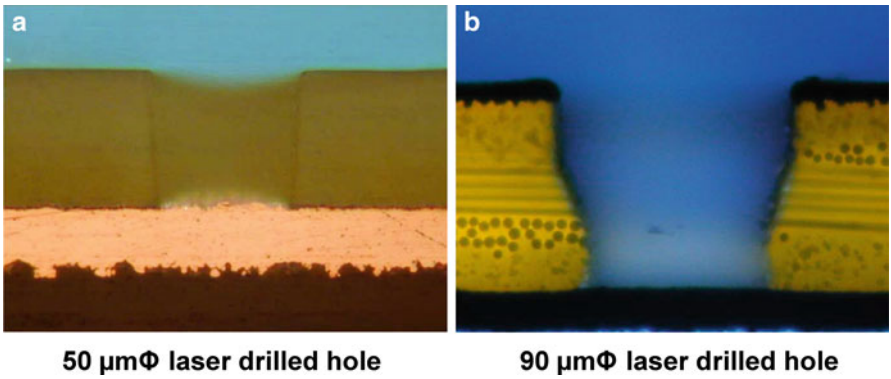

Fig. 7.16 Comparison of drilled hole. (**a**) 50 μm Φ laser drilled hole, (**b**) 90 μm Φ laser drilled hole. After Tsukada [5], 2002

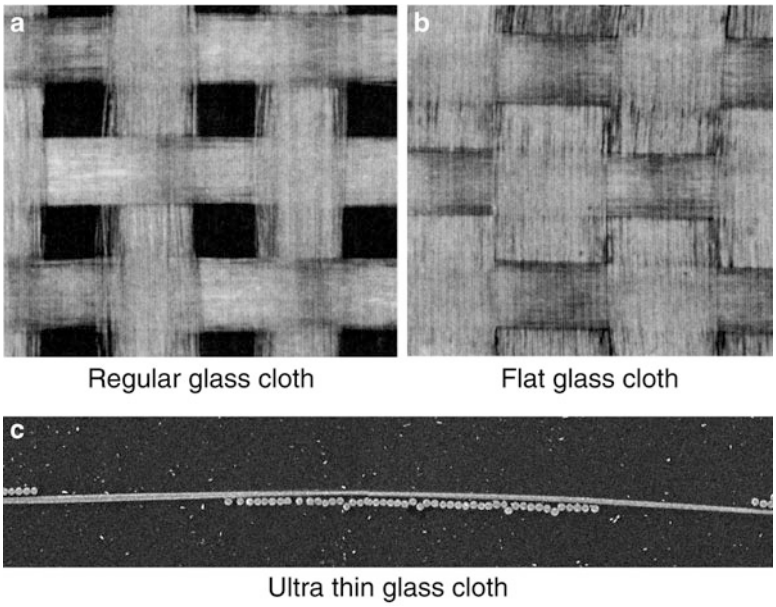

Fig. 7.17 Glass cloth for laser drilling. (**a**) Regular glass cloth, (**b**) flat glass cloth, (**c**) ultrathin glass cloth. Courtesy of Gondoh, Asahi Kasei E-materials Corp.

process works to etch the surface of a dielectric resin to form necessary anchor asperity for adhesion of copper plating. Figure 7.18a shows a bare hole on a standard build-up film after laser drilling by CO_2 laser. Photo(b) shows a hole after permanganate process. In a view of drilled hole Photo(a), there is a heavy smear at the bottom of hole. The smear is cleaned and removed in Photo(b). A surface granularity of copper is seen at the bottom of via hole. In photo(b), rough asperity of dielectric resin that is

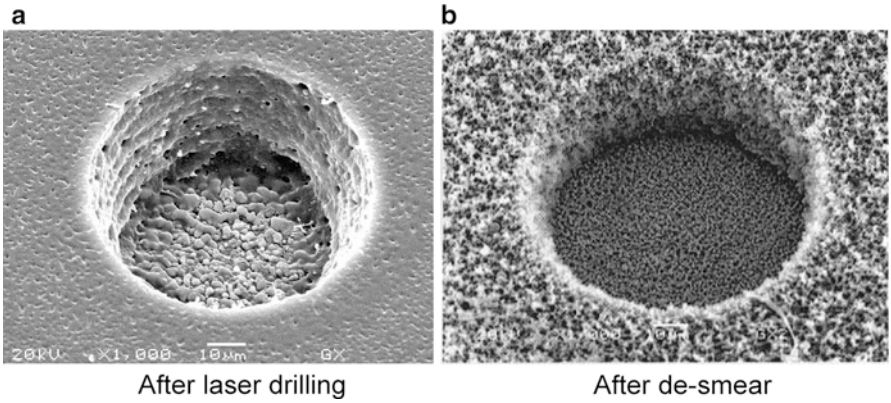

Fig. 7.18 Micro-via hole drilled by CO_2 laser. (**a**) After laser drilling, (**b**) After desmear. Courtesy of Mago, Ajinomoto Fine-Techno Co., Inc. [10], 2011

formed by a permanganate etching is shown at entire surface and via wall as well. When UV-YAG laser is used, a smear at the bottom is not heavy like CO_2 case, but it still remains at the bottom of base hole.

After laser drilling, via hole is cleaned with acid to remove resin smear in side of via, particularly, at the bottom. Permanganate for surface roughing also works to remove a smear. The next process is electro-less copper plating to provide a seed layer for subsequent pattern plating as described before. Electro-less copper is plated not only the surface but also inside of via hole. It is very important that electro-less copper plating securely cover the boundary between resin of via wall and copper at bottom of hole. Otherwise, there will be a trench at the boundary that may be separated with a stress in later. Pattern plating forms lines on the surface and plate inside of via hole at the same time. When via hole is plated in conformal mode, a pulse plating is used. Pulse plating can deposit the same thickness copper to surface and via hole by changing polarity of current with different pulse rates. Figure 7.19 shows an effect of pulse plating for making conformal plated via hole. In Photo(a), by initial plating, copper is deposited thicker at the surface than the bottom of via hole since less copper ions reached to the bottom of via hole. The point where electrical field is concentrated has more deposition. When polarity changed with denser pulse rate, the place where electrical field is higher, copper dissolve in higher rate. As the result, copper remains more at the bottom of via hole. By repeating such sequence, copper thickness at surface and via bottom becomes even shown in Photo(b) thorough (d).

Figure 7.20 shows via hole types used in an organic substrate. Photo(a) shows a conformal via hole. "conformal" means copper is plated in the same thickness along with a shape of via hole. Opening of inside of via hole after plating is eventually filled with next layer dielectric resin or solder mask resin if in the most outside layer. A conformal via hole is the most standard type of via hole. In recent days, a filled via hole is frequently used. A filled via hole is named because inside of via

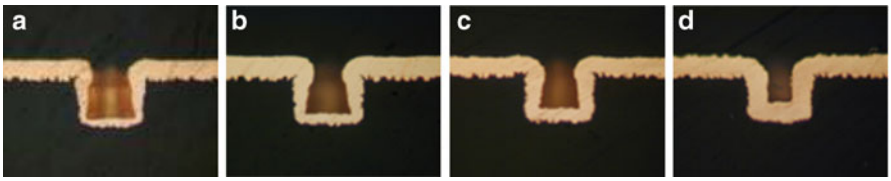

Fig. 7.19 Pulse plating of via hole. After Tsukada [5], 2002

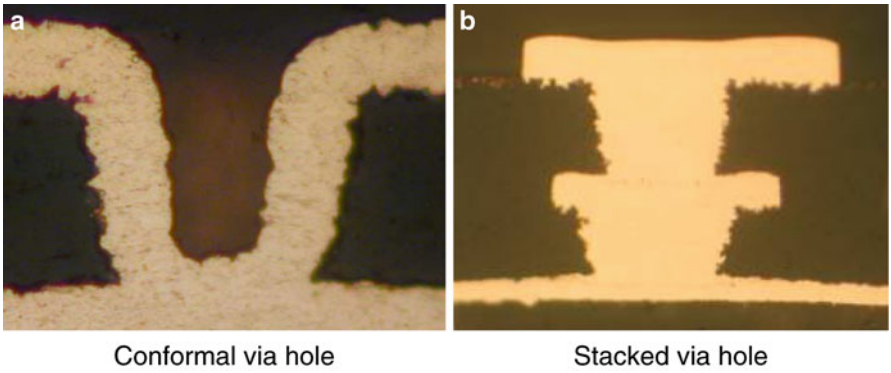

Fig. 7.20 Type of via hole. (**a**) Conformal via hole, after Tsukada [5], 2002. (**b**) Stacked via hole, Courtesy of Okuno Chemical Industries Co., LTD.

hole is filled with copper plating. A filled via hole is required to stack via holes as shown in Photo(b) of the figure. Stacked via hole is inevitably required for high density wiring of a substrate. To have via holes stacked, it is not impossible to use a conformal via hole. Upper via hole is simply just located on a previous layer via hole. Making laser drilling of upper layer deep is not difficult but a plating depth deeper takes a time much longer than ordinary depth. If a lower via is a filled via hole, next layer via hole can be processed with exactly the same process and total control is much easier.

Organic sulfuric compound (Brightener) is generally used in plating to make plated membrane shinny and give ductility by making deposited grain size finer. It also has a leveling effect as shown in Fig. 7.21 (a). Brightener is initially deposited uniformly on flat portion at surface and concave portion of via hole inside. After plating is started, it is not captured into the plating membrane and remains in the surface. As the result, the brightener density increases where the area reduces along with growth of plating thickness. Since a brightener has an acceleratory effect, plating of narrow concave area is promoted for resulting leveling effect. Since absorption activity of leveler is controlled by diffusion, the deposited density becomes low at low agitation area such as concave portion of via hole and high at high agitation area like flat surface as shown in (b). Since leveler has a suppression effect for electro-deposition, copper plating at surface is suppressed. Leveler is a quaternary amine compound and the nature is cation that is preferentially

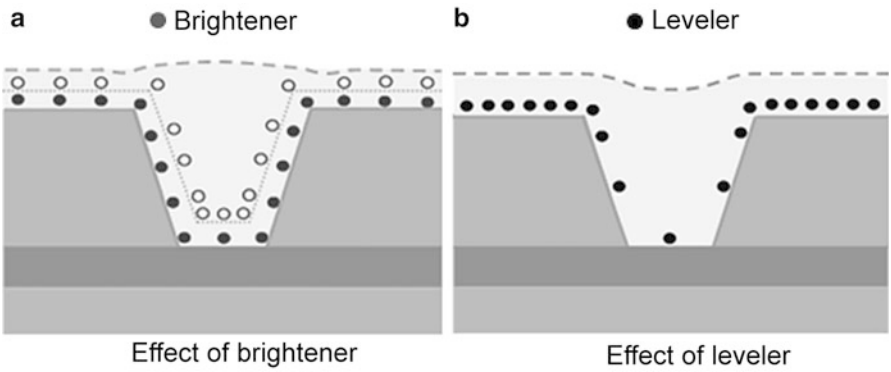

Fig. 7.21 Chemical effect for filled via hole. (**a**) Effect of brightener, (**b**) effect of leveler. Courtecy of Nishiki, Okuno Chemical Industries [11], 2009

absorbed at higher current portion to bring suppression effect there for leveling effect. With such basic leveling effect, chemical solution for filled via hole has its composition of solution and additives adjusted to obtain optimum filling effect for via hole.

A concept of component design of circuit in build-up layer is shown in Fig. 7.22. A required line width is defined as an average line width on the substrate global wiring with considering escape line design at the narrowest part as described previously and process capability for entire conductor layer of a substrate. When line width is defined, dielectric thickness is calculated with formula (7.3) to keep the characteristics impedance at 50 Ω. Before emergence of build-up PCB, ordinary PCB has higher characteristics impedance like 75–90 Ω. When build-up PCB is introduced as a flip chip substrate, it was decided to defined the structure as a substrate for direct chip attach and not as a PCB. Then, 50 Ω characteristics impedance was selected to match it with ordinary semiconductor output impedance with a consideration to expect the transmission line shorter by increasing the density for wiring in an organic substrate. As calculating by formula (7.3), a dielectric thickness is given with strip line structure as shown in upper right of the figure. When a dielectric thickness is defined, a via diameter is calculated with maintaining process capability of via hole plating. In this case, an aspect ratio is given as 0.7 that is considered with required via quality and process time shorter as possible. Aspect ratio is shown as lower right corner of the figure. Then, the base hole diameter is defined as 50 μm in this case. By expecting 2 μm removed by permanganate, a hole diameter to be delivered by laser drill becomes 48 μm.

$$Z_0 = \frac{377}{E_r} \frac{H}{W_{eff}} \frac{1}{2 + 2.8\ (H/W_{eff})^{3/4}} \tag{7.3}$$

where; Z_0: Characteristics impedance; E_r: Dielectric constant; H: Conductor height, μm; W_{eff}: Effective conductor width, μm.

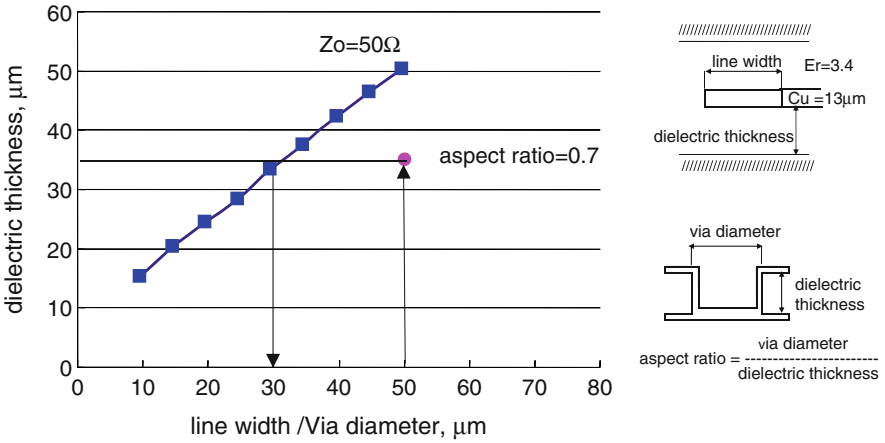

Fig. 7.22 Via hole geometry design. After Tsukada [5], 2002

Figure 7.23 shows an extraction image of copper grain boundary for a plated via hole by EBSP (electron backscatter diffraction pattern). The via hole diameter is about 60 µm. Copper plating is expected to connect upper circuit to lower circuit land by filled copper. When plating is perfectly done, copper grain grows on 111 plane of metallic lattice continued from lower land copper. Then, lower land copper and plated copper becomes to be unified metallic connection. However, in the figure, there is an obvious horizontal line of grain boundary between lower land copper and plated copper. In such connection, copper is not metallically connected but just fit a grain to grain mechanically. In this condition, when plated copper is pulled, it is separated from lower land relatively easy. And separated surfaces of upper side and lower side show concavo-convex shapes that perfectly matched to fit. If one make stacked via holes under such condition, there will be a high risk for separation due to *Z*-direction stress caused by CTE difference between stacked copper and surrounding resin. This level of via hole technology will have a high risk for future smaller via hole for higher wiring density of an organic substrate.

Figure 7.24 shows a cross section image of other via hole. In this image, copper grains grow across a top line of lower land where there are lined up micro voids (indicated by arrows) at a location of electro-less copper. It is an evidence that copper grains grow from copper grains at lower land. It means that a lower land and plated copper for via hole is metallically connected. This particular via hole in the photo has a diameter of about 25 µm and a good demonstration showing via hole plating integrity. Removal of oxide film and residue of organic material by chemical via clean process with maintaining enough turnaround of cleaning to get rid of dissolved chemicals inside of the hole. Other cleaning means, for example, a plasma cleaning, may also help to remove such materials.

A weak point of a standard sequential build-up substrate compared with other method is a through hole featured in a core. A plated through hole at a core connects front build-up layers and back build-up layers. A requirement of electrical connection

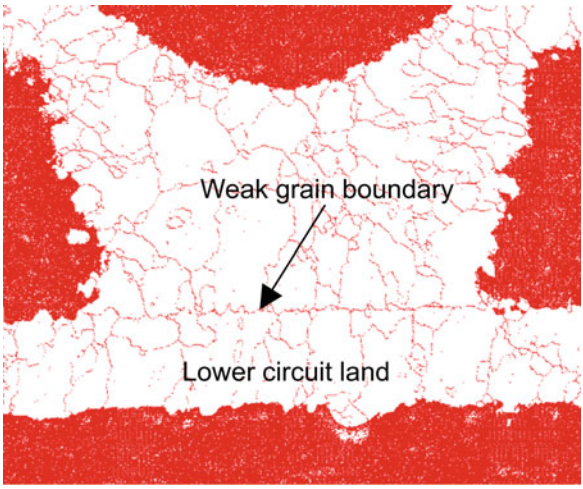

Fig. 7.23 Poor via hole connection. After Tsukada [12], 2008

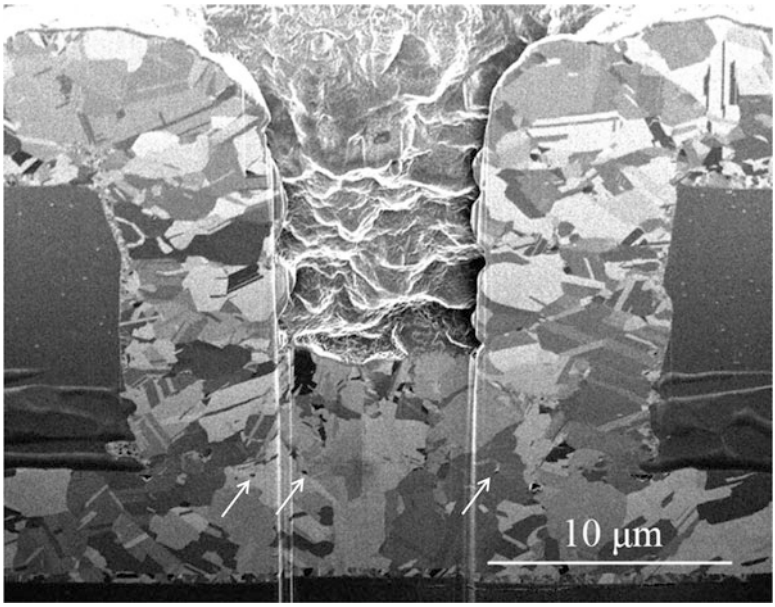

Fig. 7.24 Good via hole connection. Courtesy of KYOCERA SLC Technology Corp.

path from front to back of a flip chip substrate is, preferably, to have the same pitch with a flip chip joint pitch so that signal and power can be connected to a board level in straight through stacked via holes and through hole. However, current through hole drilling is using a mechanical drill. Though there is a small diameter mechanical drill like 60 μm, drill bit cost is significantly high and not practically used widely.

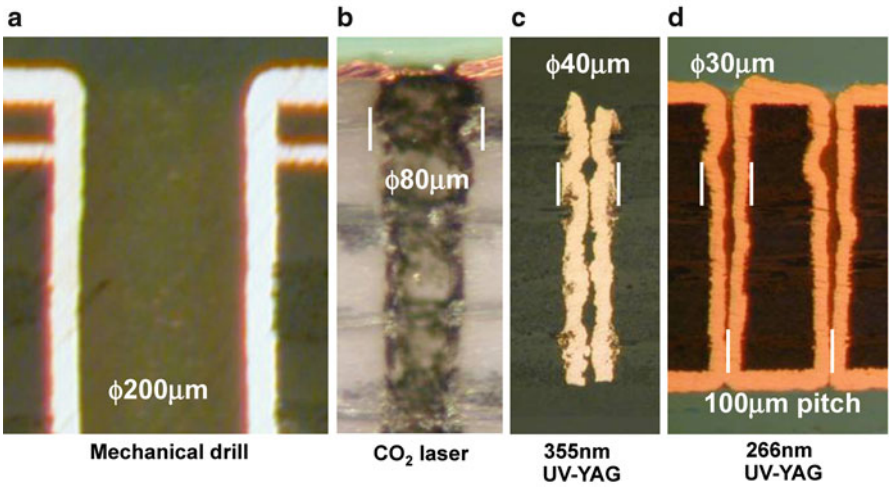

Fig. 7.25 Variation of through hole drilling. (**a**) Mechanical drill, (**b**) CO_2 laser, (**c**) 355nm UV-YAG, (**d**) 266nm UV-YAG. After Tsukada, ref. [13], 2005

Generally 100–200 μm diameter drill bit is used and not achieved the same pitch with flip chip joint pitch. For improving density of substrate and respond to a requirement for narrower flip chip joint pitch, laser drilling is a mandatory selection for the next step. Figure 7.25 shows a comparison of through holes made by various drilling method. In case of CO_2 laser, a diameter of drilled hole is large due to a laser beam size and is not be small enough for future requirement. And even though the energy absorption to glass is high but glass fiber is not sharply penetrated and showing very rough surface inside of the hole. Energy concentration of a beam is not sufficient. By using UV-YAG laser, a condition is improved significantly. However, using 355 nm UV-YAG is still not sufficient to have a clean drilled hole for a portion of glass fiber because an energy absorption rate to glass is low in case of 355 nm. This particular hole is drilled from both side of the core to try to obtain uniform diameter from front to back. With 266 nm UV-YAG, through hole drilling shows a good condition through a core with 0.4 mm in thickness. A drilled diameter is 30 μm and achieves 100 μm pitch through holes. There is a slight irregularity at the point of glass but no issue on quality and reliability. The result is enough. Though the through hole diameter varies from top to bottom, there is no sign of problem for copper plating. The integrity of through hole quality and pitch reduction for future is enough showed in this photograph.

Figure 7.26 shows energy absorption of related materials by a wavelength of laser. A dielectric resin has even absorption rate along wavelength. CO_2 and UV-YAG show a similar rate. In case of copper, an absorption rate is highly depending on a wavelength. UV-YAG is absorbed relatively high rate but not in CO_2 case. It is significantly low in case of CO_2. An absorption rate to glass is quite opposite. It is very high in case of CO_2 and not so high in case of 355 nm UV-YAG.

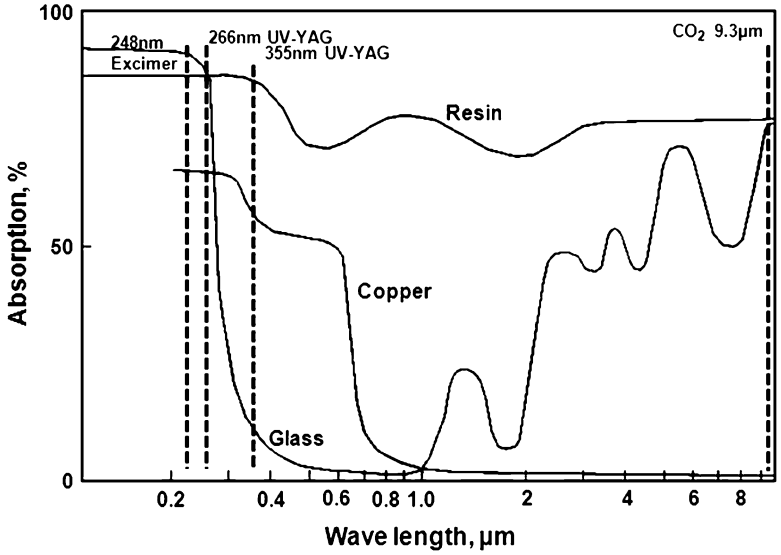

Fig. 7.26 Laser energy absorption by material. After Tsukada [13], 2005

Therefore, both CO_2 and UV-YAG have a similar effectiveness to drill a hole through a dielectric resin. If there is a glass, CO_2 works effectively. CO_2 has high absorption rate to resin and glass but not to copper. According to the figure, if one is intending to drill through a glass epoxy panel without an internal copper plane, CO_2 can work effectively and if there is an internal copper plane, 266 nm 4th harmonic of UV-YAG is the best selection considering absorption rate to resin, glass and copper. 248 nm KrF Excimer laser has a result similar with 266 nm UV-YAG. More importantly, as in the previous figure, a drilled through hole diameter that is different in each case must be primarily considered.

7.3.4 Pad Finish

Solder mask of substrate surface has a significant role to form flip chip joint. In PCB technology, solder mask is used to cover the surface of substrate to prevent solder at soldering process touches to conductor pattern and bridges a narrow space to cause a short defect. Since an outside of conductor layer of organic substrate for flip chip has lines and terminals with far finer pitch than regular PCB, the role of solder mask is significantly important. Figure 7.27 shows two types of solder mask design for flip chip terminal on a substrate and resulted flip chip joint shapes. In this particular design, the pitch of joint is 225 μm and terminal pad size is 125 μm. Lower side photographs are showing a view of solder mask opening from a chip side. Photographs up above show a cross-sectional view of resulted joint shape. (a) is

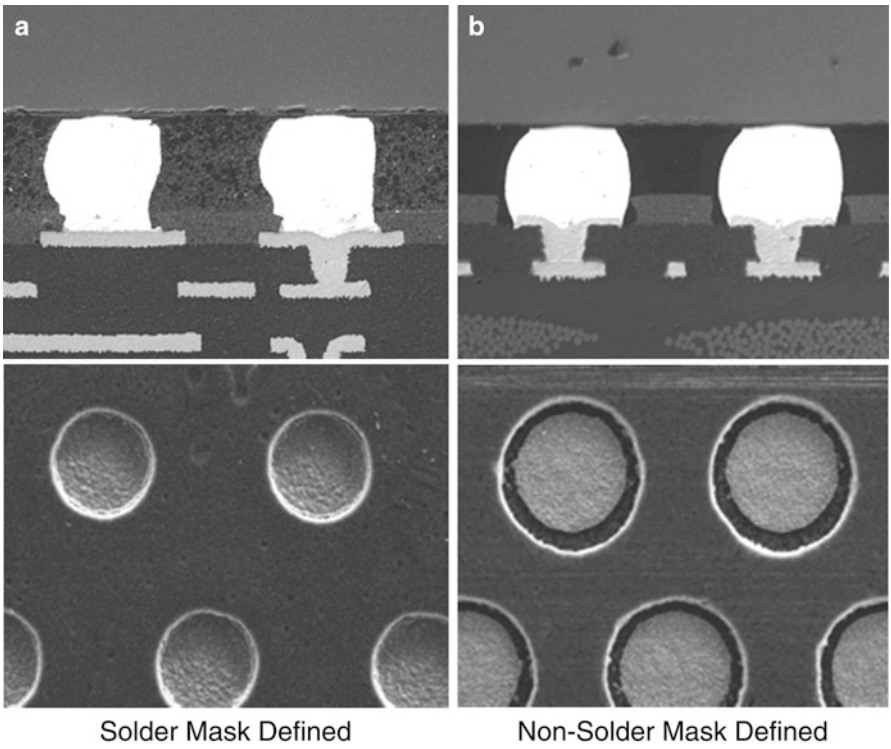

Fig. 7.27 Flip chip joint cross section. (**a**) Solder mask defined, (**b**) non-solder mask defined. After Tsukadaf [5], 2002

named as solder mask defined (SMD). The edge of terminal pad for flip chip joint is covered by solder mask and the size of opening processed by photo-etching is smaller than an actual pad. (b) is named as non solder mask defined (Non SMD). The opening is wider and a terminal pad is completely inside of it. Each type has pros and cons with relating this opening size. Non-SMD type has a large opening and a solder bump of chip is fitting easily inside of opening. In SMD type, the opening is much smaller and a bump of chip is sometime difficult to fit. Since the opening of solder mask is formed by etching, smaller is more difficult to form a opening completely without residue of resin remained inside. Occasionally invisible thin layer of resin is remained and cause a defect for gold plating which eventually cause non wet solder to the pad. When flip chip joint is formed, the joint height of Non-SMD is lower compared with SMD as appeared in upside photographs when solder volume is the same. Low joint height has disadvantages for the gap space cleaning and underfill flow. Both are the same level in terms of reliability. SMD has stress concentration due to narrow down the bottom of joint, but it is not an issue since flip chip joint life with underfill has a large safety margin to required product life. In Non-SMD case, a small dielectric resin crack appears

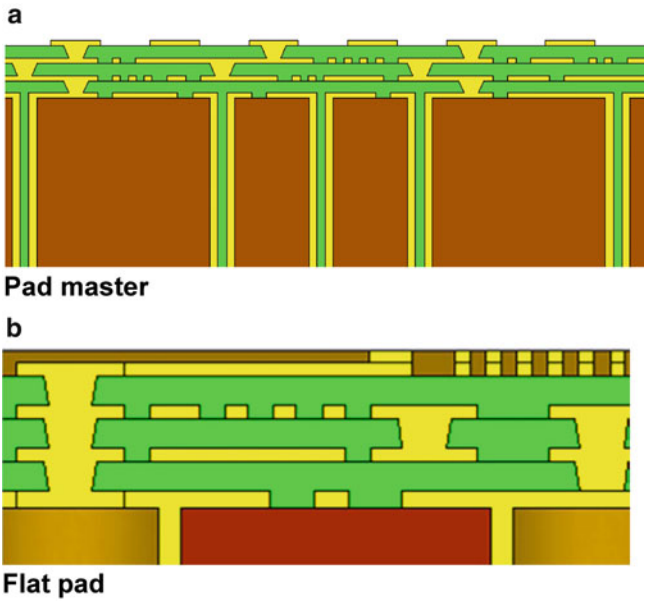

Fig. 7.28 Substrate terminal pad variation. (**a**) Pad master, (**b**) Flat pad

occasionally at the edge of terminal pad caused by *Z*-direction CTE mismatch of resin and solder but it does not extend after the stress is released by causing an unharmful crack.

Figure 7.28 shows an alternative design for flip chip pad on an organic substrate. Currently flip chip terminal design of substrate is SMD and Non-SMD as described. For future ground rule improvement, both types have a barrier to reduce a pitch. SMD will have a difficulty to form clear opening for the smaller diameter and a narrow area between opening will be break easily in case of Non-SMD. The surface conductor layer will be pad only eventually like a ceramic substrate. It is called as pad master that share one conductor layer for pad only as shown in (a) of the figure. In case of substrate for wire-bonding, flat pad structure that the top surface of terminal is leveled to the same with substrate surface is already implemented.

Various terminal finish is used for organic substrate. Au/Ni plating, Au/Pd/Ni plating, OSP (organic solderability preservative) and solder are generally used. In case of solder, plating, paste and ball attach are used. The most popular process is a paste bumping. The size of solder ball in paste varies to raise filling rate as shown in Fig 7.29. 150–200 μm pitch terminal is a processable range and 100 μm on challenge. To achieve fine paste printing, tool is improved such as to provide one direction squeeze by a rotary squeeze and air bag chamber that pressurize a mask surface after squeezing for clean release of printed solder from mask as shown in Fig. 7.30. Electroless AuNi plating is used with Ni thickness around 5–7 μm and Au thickness 0.4–0.5 μm. AuPdNi is also used with higher shear test result of solder ball compared with AuNi because a surface of Ni is oxidized while a substrate go

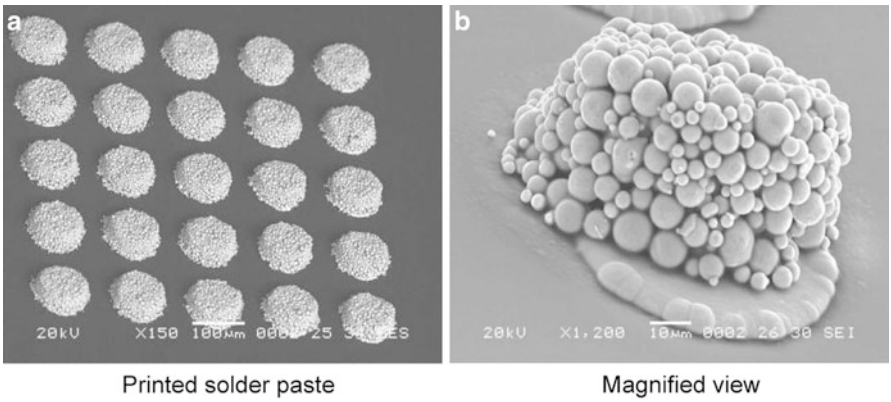

Fig. 7.29 Solder paste printing. (**a**) Printed solder paste, (**b**) Magnified view. Courtesy of Murakami, Minami Co., LTD.

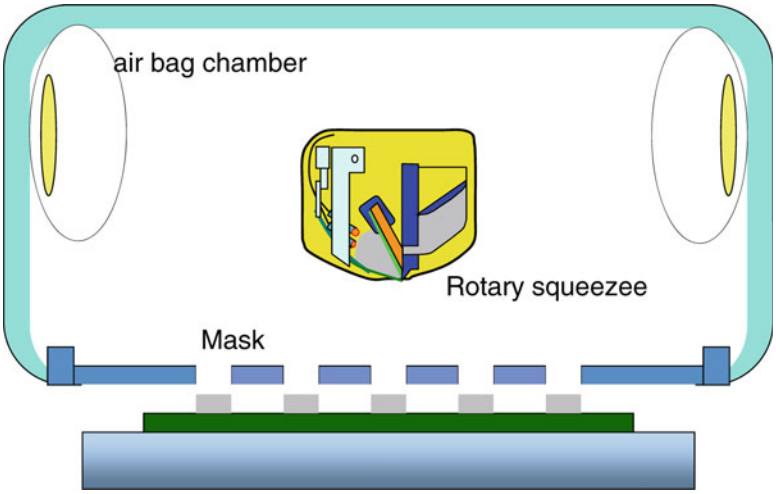

Fig. 7.30 Improved screen printer. Courtesy of Murakami, Minami Co., LTD.

through multi-reflow cycle and a interface with solder ball is occasionally separated. OSP is popular in PCB manufacturing and an enhanced version for Pb free solder is used, so called as pre-flux.

Figure 7.31 shows a cross section of solder, applied by paste, after reflow on a terminal pad where Ni/Au plated as pad finish. Before flip chip bump is placed, solder is flattened so that a placed bump do not move easily. The height of this carrier terminal bump is about 30 μm from a copper terminal surface and protruding 20–25 μm from a surface of solder mask. When the bump is flattened, the top is wider than the terminal pad opening and height from solder mask surface is depressed to 5–10 μm. However, it moves back to the original height when it is put to solder

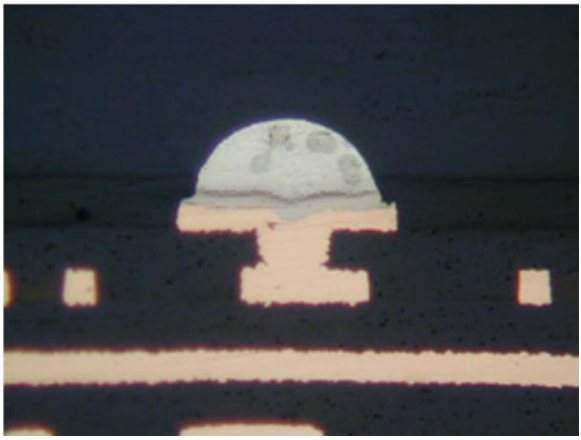

Fig. 7.31 Substrate terminal finishing. After Tsukada [13], 2005

reflow temperature. This step of solder height change creates 10–20 μm dimensional margin in *Z*-direction to formation of flip chip solder joint. In another words, the margin fills a space gap that is caused by height variations exists in parts of flip chip bonding. Possible variations are as follows.

Chip bump height variation that is a sum of a chip terminal height variation (up to 1 μm maximum) and chip bumping height variation (1–5 μm).

Equation (7.2) substrate terminal height variation (5–20 μm) that is caused by a remained topology of copper pattern. The topology is significantly depends on the substrate wiring design.

Since a solder finish on terminal pad compensates height variation of parts consist of flip chip joint, it is the most safe process in terminal finish in terms of dimension and solder wettability as well. One has to consider this issue of *Z*-direction height variation precisely when plans to squeeze a dimension and/or introduce other method and material in a flip chip joint construction. Otherwise, it will degrade chip join yield and remain a high risk in reliability of the joint.

Normally when a copper pad is wet with solder, the height of solder from copper pad surface is limited around 10 μm when the pad size is 100 μm. It is due to a wetting angle of solder to copper (23.5°) in case of Eutectic SnPb solder. The amount is far less than to form optimum solder joint with chip side bump since solder bump height at chip side varies by its applied process nature or deformation during transfer after bumping process. Also a substrate surface topology due to circuit pattern under a dielectric layer makes a pad height variation around 10, 20 μm in the worst case. Therefore a special effort is required to deposit required solder amount to form the bump height higher at certain level. Typical method is utilize "wet back" nature of solder that is to apply solder to large area than a pad by plating, screen printing and other deposit process with mask and form the bump height higher when solder is reflowed and excess solder applied wider than a pad area is wet back to the pad area to form higher bump eventually. However "wet back" required space around a pad so that to deposit excessive

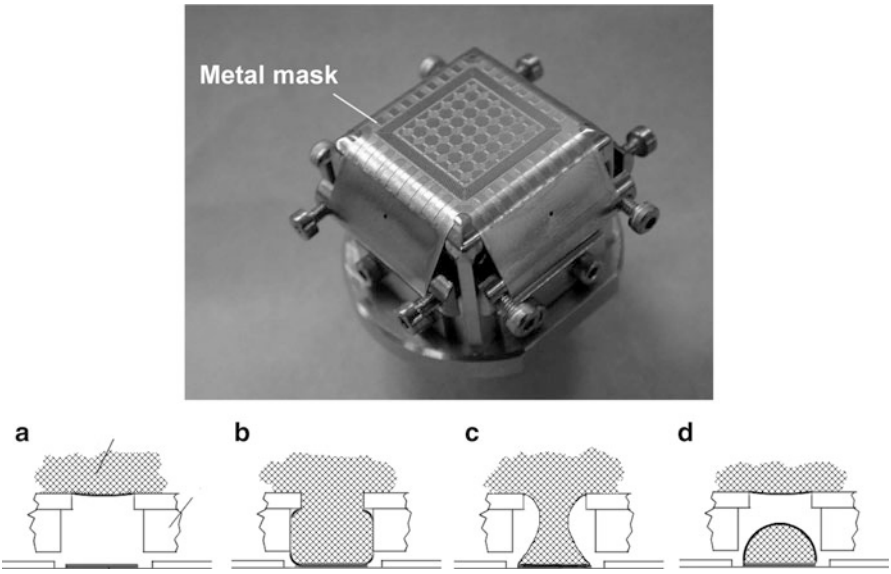

Fig. 7.32 Solder injection tool. After Tsukada, ref. [14], 2000

amount of solder. It is possible to apply a pad for low I/O chip case but not possible to use for high density logic chip where the bump pitch is tight and no room to deposit solder around.

Figure 7.32 shows a tool that was used to resolve this issue in an early stage of implementing a flip chip bonding on an organic substrate. Solder injection tool is used for bumping solder on a flip chip pad of substrate for high density logic chip. The head features a metal mask that has a hole pattern matching with required pad pattern of chip site on a substrate. A molten solder is in a reservoir of head. Operation sequence is as follows.

(a) Align a hole pattern of mask to identical pad pattern on a substrate.
(b) Pressurize the reservoir so that a molten solder is extruding from the hole of mask and a solder touch to a pad below.
(c) After a few seconds to allow solder wet the pad surface, apply negative pressure to the reservoir to draw back molten solder into it.
(d) Molten solder is pinched off and a good solder amount is remained on the pad.

The volume of solder can be designed by a pad size, mask hole size and height of the mask from a pad. One of major benefit of this type method is to be able to use any kind of solder as far as it melts. This tool can deposit a solder around 50 μm on 100 μm size pad. A disadvantage is that has to process each chip site on the substrate one by one.

Figure 7.33 shows scan solder tool that is an improved version of solder injection to use in continuous operation. Instead of mask with hole pattern, molten solder from reservoir is pushed out by pressure from a slit on the head to touch to a substrate

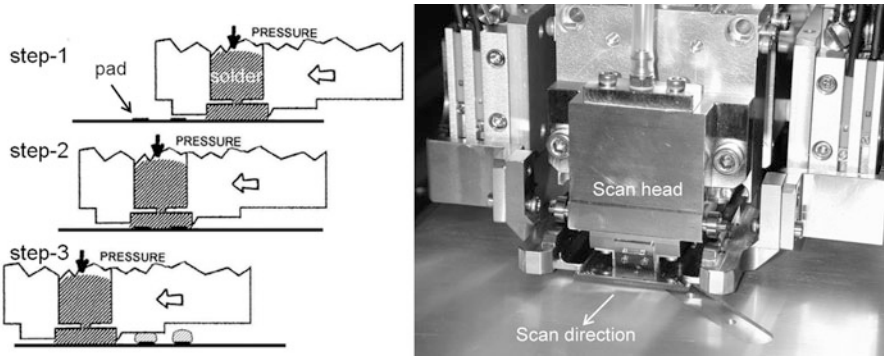

Fig. 7.33 Scan solder tool. After Tsukada [14], 2000

surface (step-1). When the head scans, solder is depressed between a head and substrate surface and touch to pads on the substrate to let solder wet to copper (step-2). As the result of head moving on a substrate surface, solder is split to each pad while still depressing by a part of head. When solder released to free from the depression, some wet back action works to form a round solder bump on a pad (step-3). In this method, the advantage is still to be able to use any kind of solder and quick scan to apply solder by continuous operation. There is some sensitivity to split solder to each pad that depends on the design of pad pattern and pressure control so that molten solder do not spilt out from the space between the head and a substrate.

Figure 7.34 shows an advanced tool that handles a molten solder. A mask made of organic film that has same pattern with pad pattern on a substrate is aligned to the substrate pad. A diameter of hole on a mask is smaller at top and wider at bottom so that extruded solder from the top does not move back to a solder reservoir. The head scans on the mask which has a hole pattern and solder is filled into mask holes to wet pads on a substrate. After cooling and solder freezes, mask is removed. A major advantage of this method is that the height of bumps is controlled by a thickness of mask. Therefore, height of solder is even if pad sizes are different on a mask pattern. 150 μm bump on 250 μm pitch is under production and 75 μm on 150 μm under qualification at the end of 2010. It is planned to move 25 μm on 50 μm for future.

Figure 7.35 shows a process flow of ball bumping that is both used for wafer bumping and substrate bumping. Operation steps are as follows.

1. Sucking balls with an arrangement plate by vacuum.
2. Removing excess balls by applying ultrasonic vibration.
3. Check balls sucked on the arrangement plate.
4. Align to position.
5. Ball placement.
6. Check balls on a substrate.
7. Repair ball placement errors.
8. Reflow and cleaning.

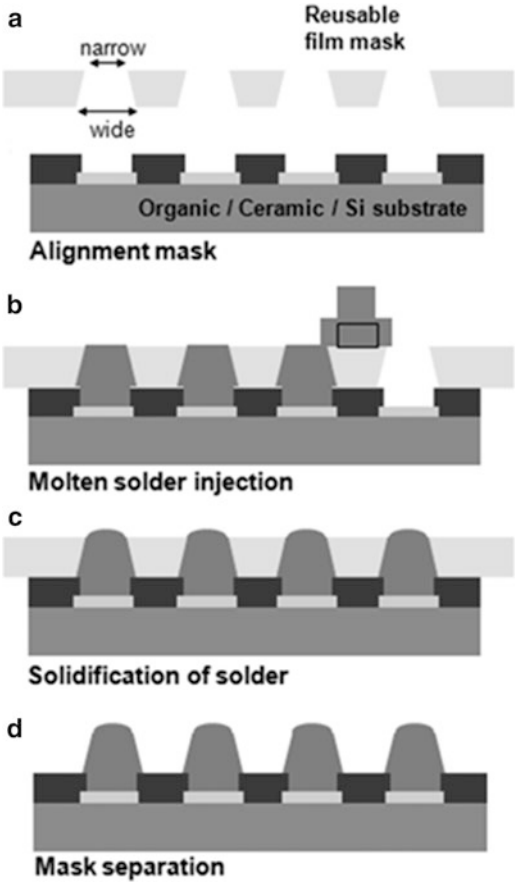

Fig. 7.34 Injection molded solder tool. After Orii [15], 2011

In case of wafer bumping, huge amount of balls is handled in one time. The process is set to allow a rework of missing and irregular bumps after a inspection so that 100 % of bumps is formed completely. If this process is used for a substrate bumping, a rework process may not be necessary since a number of bump may not be large numbers as on a wafer since the process may work on a singulated substrate or a sheet that contains a limited number of substrates.

Figure 7.36 shows a solder deposition by "Super Juffit" process from Showa Denko. Photo(a) shows a SEM photograph after solder powder is applied to fine pitch pads on a substrate. Pitch of pads reached to 50 μm that can accept a very fine pitch wire bond chip. In a magnified view at the corner of photo, it appears fine solder powder is deposited on a pad. Photo(b) shows a view after a reflow of deposited solder powder.

Figure 7.37 shows process steps of "Super Juffit."

(a) Clean a parts so that to remove any contamination and oxide layer of copper.
(b) A chemical with a proprietary composition is applied to entire surface of substrate. After a cleaning and drying, a tacky material is remained on only a copper surface and washing away from other area.

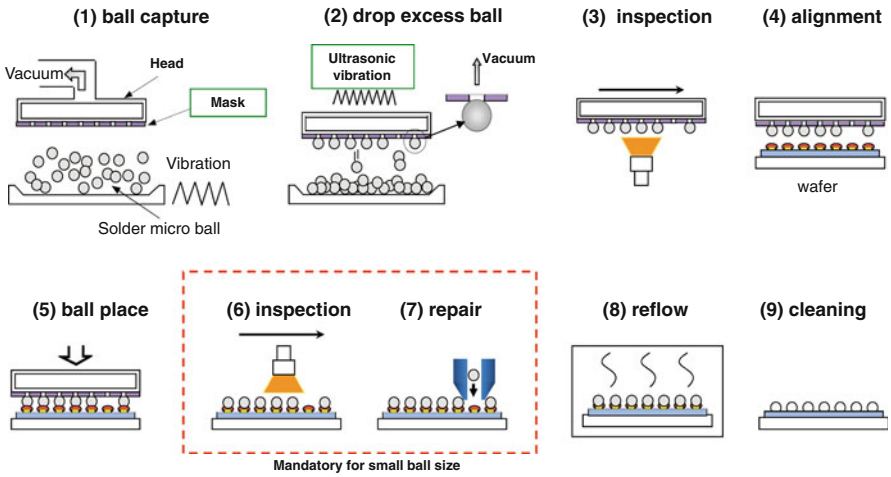

Fig. 7.35 Ball bumping process. (1) ball capture, (2) drop excess ball, (3) inspection, (4) alignment, (5) ball place, (6) inspection, (7) repair, (8) reflow, (9) cleaning. Courtesy of Ishikawa, Nippon Streel Corporation

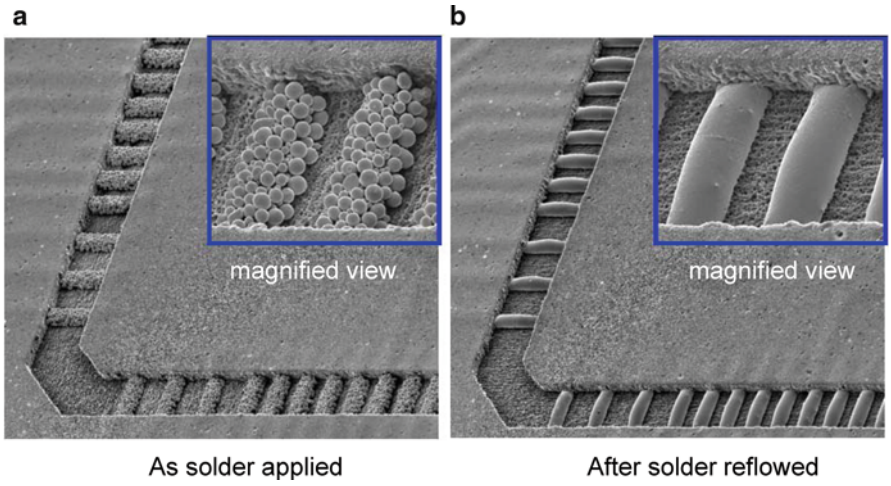

Fig. 7.36 Super Juffit process. (**a**) As solder applied, (**b**) after solder reflowed. Courtesy of Syoji, Showa Denko

(c) Solder powder is applied. Since a pad is covered by the tacky layer, powder sticks only a pad and others are easily put off from surface of a substrate.
(d) Apply a flux for solder wetting.
(e) Reflow solder powder.
(f) Washing out a flux.

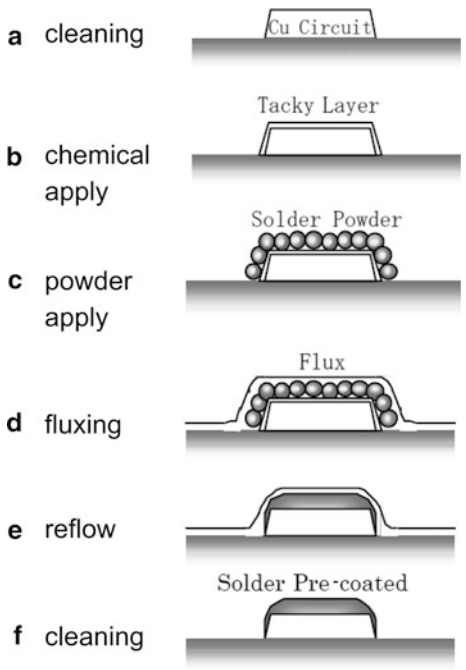

Fig. 7.37 Process steps. Courtesy of Syoji, Showa Denko

Since a process is utilizing the chemical property that reacts with copper only, there is no need of mask and other supplemental mean to deposit solder to very fine pitch pads on a substrate.

Figure 7.38 shows a chip bumping and a matched substrate bumping. By utilizing a solder bumping process on a substrate, a substrate can accept a hard metal pillar bump on a chip with a good yield at a chip bonding process.

7.3.5 Chip Package Interaction

One of major issue of flip chip bonding on an organic substrate is a stress at flip chip joint due to CTE mismatch between chip and substrate. Figure 7.39 shows a schematic of damaged wiring layer cross section of chip that uses low-k material as a dielectric material of chip wiring layer. When a chip is join to substrate, above melting point of solder, solder form a joint between chip and substrate terminal pads. While the temperature is above a melting point, there is no stress even though with CTE mismatch since solder is melting as (a) in the figure. When cooling down and after passing a melting point, solder becomes solidified. Since a substrate CTE is much higher than chip, a substrate shrinks faster than chip. Then a joint is deformed by shear stress due to displacement between terminal pads of chip and substrate as shown (b). By this deformation, a tensile stress is generated and low-k

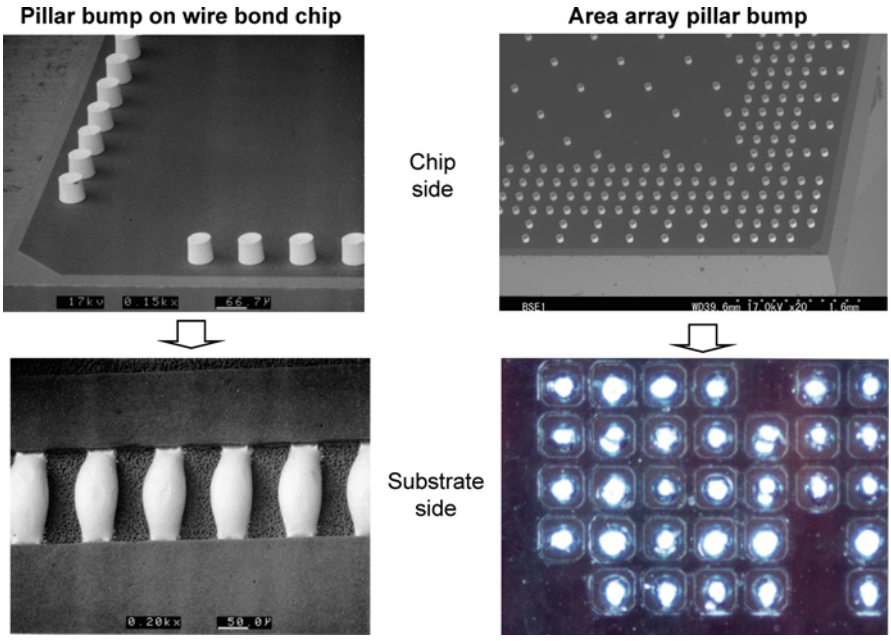

Fig. 7.38 Substrate bumping for chip side pillar. After Tsukada [14], 2000

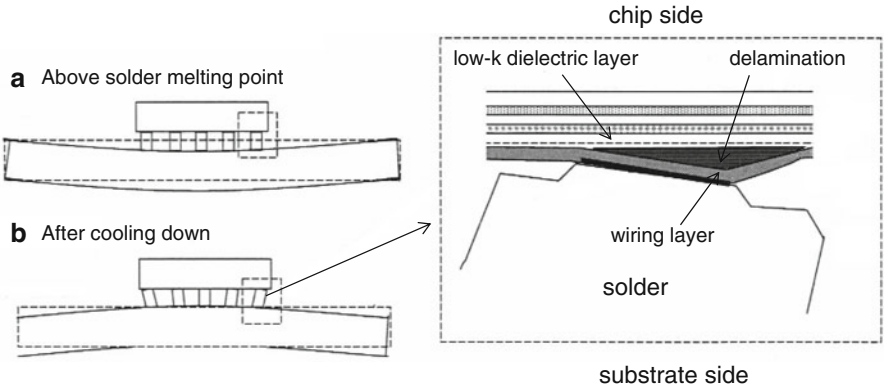

Fig. 7.39 Chip wiring layer damage. (**a**) Above solder melting point, (**b**) after cooling down. After Nishio [16] (2008)

dielectric layer is delaminated to resulted breaking of wiring as shown in the right side of figure.

This problem is essentially caused by CTE mismatch of chip and substrate. Normally chip CTE is 3–3.5 ppm/°C because a base material is a silicon. A CTE may vary depends on how thick a wiring layer is. In the meantime, CTE of organic substrate is 17 ppm/°C at standard, around 15 ppm/°C at low CTE version. It is

because a base core of organic substrate is essentially same with a printed circuit board that has CTE adjusted to 17 ppm/°C. The reason to adjust this level is to protect copper wiring inside of laminate that is established for printed circuit board technology. This adjustment is done by CTE balance of glass fiber woven cloth that employs E-glass with CTE 5–6 ppm/°C and epoxy resin with CTE 70–80 ppm/°C as described before. This technical issue is named as "white bump" since it viewed white by an analysis of SAM (scanning acoustic microscope) and the cause is named as "Chip Package Interaction" and being the most critical issue for low-k chip packaging in these years and also a major barrier for a finer pitch flip chip joint in future.

Figure 7.40 shows schematics of underfill effect when a chip is attached to an organic substrate. (a) in the figure shows when cooling down from a curing temperature of underfill resin to room temperature after a gap between a chip and substrate is filled with the resin. Since a chip and substrate are tightly adhered, displacement between chip and substrate terminal pads are very small. It made possible to extend a flip chip joint life significantly longer. Instead, a chip and substrate entity is bent due to CTE mismatch causes an effect like a bi-metal structure. This bending causes a dominant failure mode in case BGA package that is a failure of BGA joint at the center of package. It is important that CTE mismatch creates a stress but 30 % is converted to this bending when thickness geometries of parts are in a standard configuration, i.e., chip thickness is about 50 % of substrate thickness. Important thing is that remaining 70 % of stress is absorbed into a substrate since material modulus is quite low in case of an organic substrate compared with a ceramic substrate. This distributed stress in a substrate cause various failure inside of substrate when a package is not properly designed. Detail design rule that do not cause a local concentration of stress is very important.

Paring with (a) in the figure, (b) was disclosed when this technology was announced from IBM Yasu Laboratory in 1991. Within a technical disclosure after announcement, a following warning was made about a possible chip damage when a process is not properly handled. After applying underfill, a joint of this package is perfectly protected from the CTE mismatch, however the point after chip join to substrate and cooling down to a room temperature, a joint suffers a heavy deformation due to a displacement between chip and substrate terminal pads that is caused by the CTE mismatch. Since this deformation is very heavy, it was known that the point indicated by "A" has very high tensile stress in a chip wiring layer.

Figure 7.41 is photographs used with the technical warning at the announcement. (a) is a chip wiring crack that was located under the edge of barrier metal. Chip passivation had a crack and the crack extended to damage wiring. When passivation had a crack even if wiring was not broken and chip function does not fail immediately, moisture comes into chip wiring layer and cause a corrosion or metal migration in later day. It was recommended that chip should have a polyimide cushion layer on which a barrier metal can sit on. The technical description is closed by a statement that whether the chip is durable to a stress is the first thing to be confirmed in this technology. This failure mechanism is the same with one described today as chip package interaction. The warning has been made at the

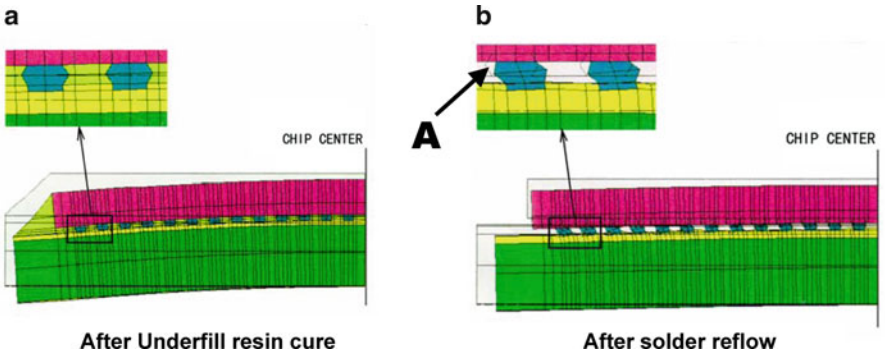

Fig. 7.40 Underfill effect on organic substrate. (**a**) After underfill resin cure, (**b**) after solder reflow. After Tsukada [6], 1998

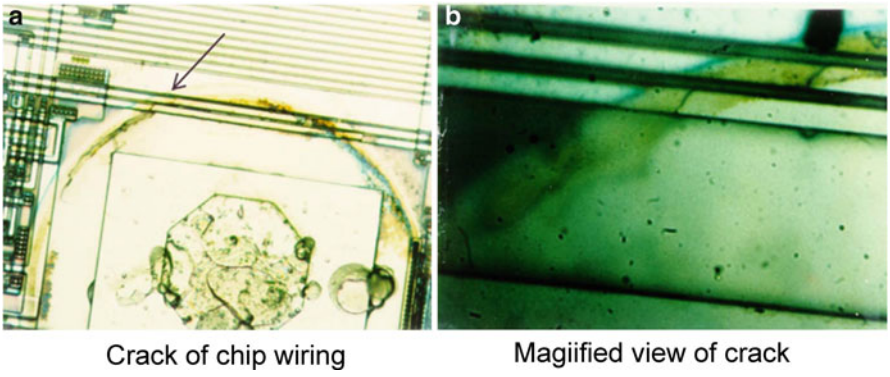

Fig. 7.41 Passivation crack on chip. (**a**) Crack of chip wiring, (**b**) magiified view of crack. After Tsukada [6], 1998

beginning of this technology introduction. It is important one should aware the basic of technology is not changed.

Early stage of flip chip with a ceramic substrate, Goldman issued a paper titled "geometric optimization of controlled collapse interconnections" in 1969. There described in the paper, a flip chip joint is deformed by shear force caused by CTE mismatch between a chip and a ceramic substrate. Due to deformation of joint solder, tensile stress is generated in a chip wiring layer at the edge of chip side terminal. And he indicated there as a critical point shown in Fig. 7.42. This means that the issue of chip wiring layer damage is not only by a usage of organic substrate but ceramic substrate either. A possibility of chip wiring layer damage is an essential thermal stress issue of flip chip joint. One should remind that a dielectric material of chip wiring layer is always under a risk of damage by looking for a density and performance increase. When a technology becomes mature, an issue

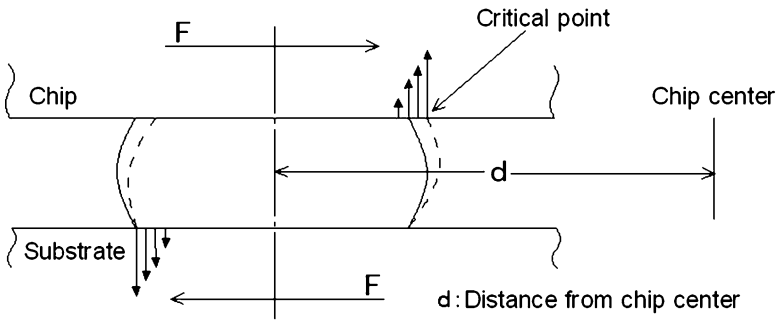

Fig. 7.42 Risk point at flip chip joint. After Goldman [17], 1969

seems to be settled down, but an issue in new step is revealed repeatedly when phase-in to a new technology.

As previously described, a chip and substrate entity bends when ambient temperature changes. Since solder of flip chip joint creeps, a chip and a substrate are both almost flat at the temperature for curing underfill. After cooling down from a curing temperature, the entity has an almost permanent bending. as shown in Fig. 7.43. It shows a bending mode when a 20 mm square chip is attached to 30 mm square substrate and cooling down to room temperature from a resin curing temperature around 130 °C. It shows smooth uniform concave shape. Bending of chip and substrate, i.e., a package bending, is repeated when a chip is heated by a system in operation. The figure shows a bending of just only a package not assembled to the next level board and a stress condition is more complicated when assembled.

When a chip and substrate entity forms BGA package, a state of BGA joint failure in thermal cycle test is shown in Fig. 7.44. (a) Shows a BGA joint pattern and dotted rectangular is the area a chip is attached. “A” through “J” are nets with BGA joints electrically measured a failure in this thermal cycle test. (b) Shows a log-normal chart to show cumulative failures of a measuring point each net. As the test result, Net-A that was located around the center of chip failed first. Then Net-B that was located at the edge of chip failed next. Net-C that was located at the corner of the chip failed third. At the point of time, all other NET distributed along with the substrate diagonal line had no failure. The result that BGA joint under a chip area failed earlier while others were safe means a bending stress was locally in the chip area and other area of substrate remained almost no bending since BGA joints supported each other. This result clearly indicated that an internal stress of substrate increases when the package is attached to a board while uninstalled package is bending freely showing natural concave shape. Also this test result is a main reason there are many packages today that are designed to remove BGA joints from a area under a chip.

A force of bending is significantly strong. It is bending a mother board when BGA package is installed. Figure 7.45 shows a test result when BGA packages are installed on both side of mother board symmetrically. The test result showed a BGA joint life

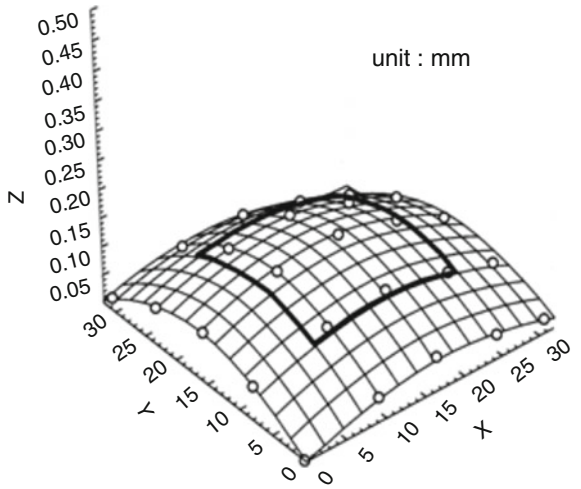

Fig. 7.43 Chip and substrate bending. After Tsukada [14], 2000

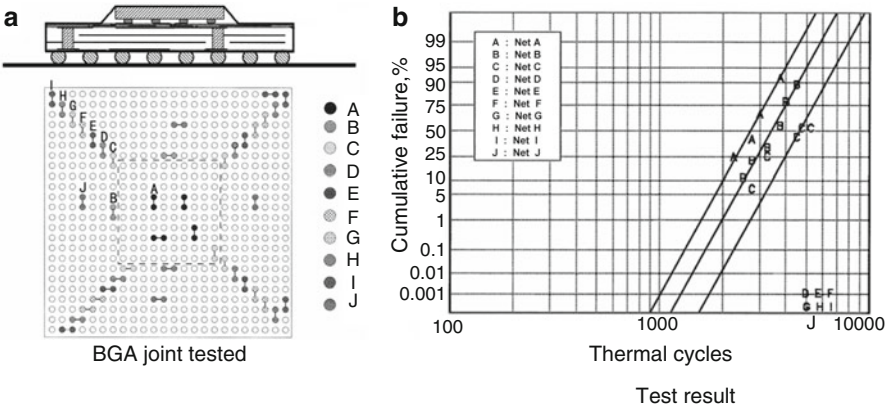

Fig. 7.44 BGA joint life with organic substrate. (**a**) BGA joint tested, (**b**) Test result. After Tsukada [14], 2000

in double side loading was shorter about 45 % than single side loading. Earliest fail of BGA joint was also a joint at the center area. This result tells us a bending of chip and substrate entity actually bends a mother board below when a BGA loading is on a single side. When BGA package loaded on double side, a mother board in between BGA packages on front and back is constrained and is not bend since there is a tension caused by a chip and substrate bending from both side. Therefore a BGA joint life becomes significantly shorter in case of double side loading that may violate a requirement of product. In case of flip chip loading on double side on a substrate, the life of the joint also became shorter but the rate was about 35 %. But a joint life has a large safety margin and the life though it is shorter is not the level to deteriorate a product life. In addition in this test, measurement was done with 10 mΩ threshold just

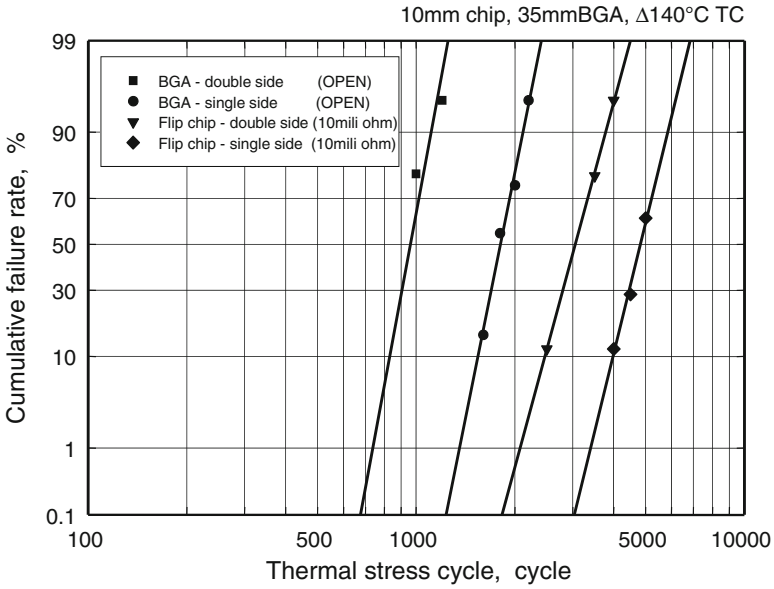

Fig. 7.45 Joint life in double side loading. After Tsukada [14], 2000

for technical comparison purpose. A series of these results tells us a stress condition of flip chip on organic substrate is significantly complicated and one has to analyze and test in a cautious manner when implementing an application.

Figure 7.46 shows examples of chip crack caused by a stress due to CTE mismatch. (a) Shows a crack runs across a chip indicated by arrow. Crack runs horizontally in the photo. An initiation point of crack is a small chipping at the edge of chip. A stress is concentrated at the chipping. The chip in the photo is originally a wirebond chip and attached to a substrate by flip chip bonding with using a gold stud bump. Normally a wirebond chip is singulated from a wafer by a single side dicing from functional side with leaving thin remained thickness of wafer and is braked the thin part finally. Therefore it is not abnormal for wirebond chip to have a chipping at a backside edge. A chip for flip chip is normally uses a double side dicing so that there is not chipping at any edge of chip where a stress is easily concentrated. (b) Shows a very unique crack. A crack propagated in a lateral direction and a silicon base was separated with the functional area of chip remained on the substrate. Since a silicon cracks along with a crystal interface rather easily, too hard substrate and underfill caused this crack by extremely high stress.

A thermal stress condition around a flip chip joint in an organic substrate is more complicated. Figure 7.47 shows a close up schematic of flip chip joint that is sitting on a stacked via placed onto a capped plated through hole in an organic substrate. It is a preferable structure regarding electrical performance since a straight vertical conductive structure from a chip terminal to other side of a substrate potentially a BGA joint. CTE of materials in this schematic are as follows. A chip CTE varies

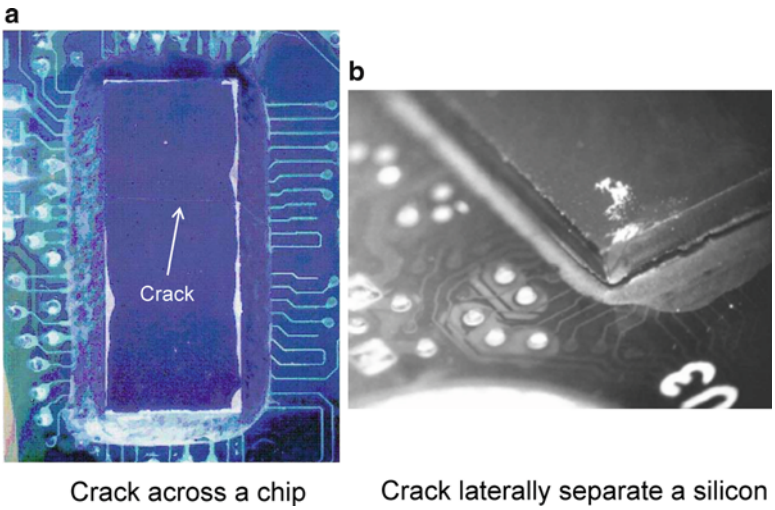

Fig. 7.46 Chip crack caused by stress. (**a**) Crack across a chip, (**b**) Crack laterally separate a silicon. After Tsukada [14], 2000

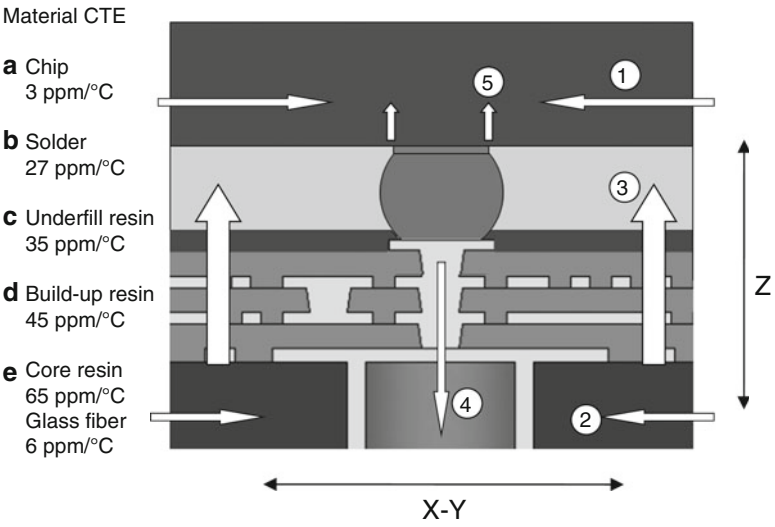

Fig. 7.47 Thermal stress around joint. Material CTE. (**a**) Chip 3 ppm/°C, (**b**) solder 27 ppm/°C, (**c**) underfill resin 35 ppm/°C, (**d**) build-up resin 45 ppm/°C, (**e**) Core resin 65 ppm/°C, glass fiber 6 ppm/°C. After Tsukada [12] 2008

with numbers of wiring layer but basically around 3 ppm/°C that is a CTE of silicon and isotropic. A solder CTE also varies with its composition and about 27 ppm/°C in case of eutectic solder with isotropic nature. Underfill resin is a mixture of epoxy and silica with a combined CTE around 35 ppm/°C and isotropic. Build-up resin is

also a mixture of epoxy and filler material with CTE around 35 ppm/°C and isotropic. A core of substrate is a composite of epoxy resin with CTE 65 ppm/°C and a glass with CTE 6 ppm/°C. Copper of conductor has CTE 17 ppm/°C. Most of materials in a substrate are isotropic material but a glass is a form of woven fabric and laminated laying in *X–Y* direction. Due to a very low CTE with very high modulus of chip and woven glass fiber with low CTE and high modulus compared with all resins that is low modulus with high CTE, a combined CTE in *X–Y* direction of this structure is dominated by a chip and woven glass fiber with force indicated by block arrows ① and ②. As the result, when temperature rises, majority of isotropic expansion of resins is converted to *Z*-direction as ③ in this schematic since X–Y is constrained with a chip and glass fabric. Since a stacked via and a through hole are copper that are relatively low CTE with high modulus, this part of structure connected to flip chip joint does not expand in *Z*-direction as other area between plated through holes. Consequently, a tensile stress is concentrated in stacked via that may bring a separation of stacked structure when metallurgical integrity of plating is not appropriate. Though, a solder of flip chip joint creeps to relax the stress, there is still a high risk of via separation exists. Therefore, to remain a bulk solder in a flip chip joint is important. If in case a solder of joint becomes intermetallic compound, the stress at ④ increases significantly. It will damage a via to via metallic interface and also create tensile stress in chip wiring layer as shown by block arrow ⑤. It is easily understood that the stress increases as a material of joint becomes harder. One has to be cautious when introduces a harder metal at flip chip joint like copper pillar. To avoid this stress concentration, an ideal solder for joint is a low stress and low melting point solder. One of the candidate is Indium that is very ductile to avoid stress concentration and the melting point is low as 151 °C that lowers a thermal stress when cooling from chip joining temperature.

Figure 7.48 shows overall CTE conditions in organic substrate applications. Current issues with a thermal stress are basically caused by a high CTE of a organic substrate that employs an ordinary PCB material set though there are some improvement done after an emergence of technology. No matter how the final figure of package is, there is a high internal stress distributed in a package. It creates risks during fabrication of a package with a concentrated stress at a part of component of the package. It is further complicated if we employ a stacked chip on an organic substrate. To improve this situation, essential CTE reduction of organic substrate materials are required. Activities are on-going in almost all area of organic substrate and its packaging components. Ideally, there are two cases. One is to use a substrate that has a CTE same as silicon. The other is an utilization of low and adjustable CTE construction for a substrate and a board so that one can design a thermal stress of entire package to minimize a stress concentration in any part of the package.

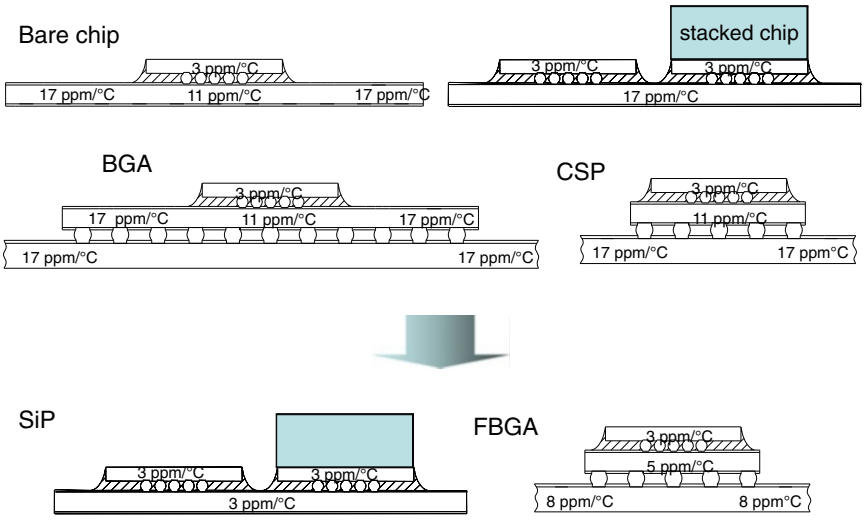

Fig. 7.48 Substrate CTE improvement. After Tsukada [12] 2008

7.3.6 Reliability

Table 7.3 describes typical stress test applied to an organic substrate when target application is cost/performance system such as work station, PC and high end consumer product. There are three categories as applied to other kind of packages. However, enough cautious has to be taken since an acceleration factor of a failure is different by a material. Particularly, some test that has been done for a ceramic substrate is too stringent for an organic substrate because it creates a stress that makes the test as destructive mode rather than a acceleration test. The most important thing is that a failure mode of acceleration test must be the same as presumed failure mode of an application in filed. One of typical example is $\Delta T = 180$ °C thermal cycle test. Traditionally $\Delta T = 180$ °C is used for a ceramic substrate since it is based on a inorganic hard material. In case of organic substrate, epoxy is a main material and eventually causes a crack by fatigue from aging effect. In $\Delta T = 180$ °C thermal cycle test, a crack appears earlier in an organic substrate and cause a conductor wire break down before 1,000 cycles that has been a target cycle in case of a ceramic substrate. However the acceleration factor of cracking is pretty high and extrapolated field life from acceleration test proved has no problem. It is preferable to use lower delta temperature in considering proper accuracy of an acceleration test, $\Delta T = 165$ °C, 1,000 cycle is used in case of organic substrate. If $\Delta T = 180$ °C is used by some reason, 750 cycles will be the most reasonable target cycle. In a lower delta temperature test as $\Delta T = 100$ °C, target cycle may be set to 3,000 cycles that is the same temperature range widely used for an application package assembly where an ordinary PCB is tested together. Occasionally, wet thermal cycle test is used to apply a stress to a metal portion of a substrate such as

Table 7.3 Stress test, after Tsukada [14], 2000

Stress	Condition	Target
Dry TC (Δ180 °C)	−55–125 °C	750 cycles
Dry TC (Δ165 °C)	−40–125 °C	1,000 cycles
Dry TC (Δ100 °C)	0–100 °C	3,000 cycles
Wet TC (ref.)	0–100 °C	3,000 cycles
THB	85 °C, 85 %, bias	1,000 h
PCBT (HAST)	109.8 °C, 85 %, bias, 1.2 atm.	264 h
PCT (ref.)	121 °C, 100 %, 2 atm.	96 h
HTS	150 °C	1,000 h

conductor wires, micro-via holes and plated through holes that are composed of copper. But it should not be applied to assess an epoxy material related failure mode because it too quick cycle and lose a duration for a time of creep of resin that is brought in low cycle fatigue. Since a creep of copper is low compared with epoxy, wet thermal cycle test can be used for a copper conductor related failure mode, it should be handled as reference test due to its accuracy. In a category of temperature and humidity influences, 85 °C, 85 % with bias voltage is a typical test. Since the target hours of this THB test is 1,000 h that takes about 2.5 months including reading time, HAST (high acceleration stress test) is used frequently. 109.8 °C, 85 %, bias and 1.2 atm. condition that is unsaturated water vapor is one of a typical setting. Occasionally higher temperature is used but the condition has to be unsaturated water vapor, otherwise the test lose a correlation to a failure in field. Even with 109.8 °C, 85 %, bias and 1.2 atm. condition, a corrosion type failure sometime loses correlation. For example, Chloride ion in an organic substrate is driven out and crystallized on surface. PCT (pressure cooker test) is also handled as reference since a saturated water vapor condition is a destructive test in case of epoxy base organic substrate. In HTS (high temperature storage test) with $\Delta T = 150$ °C 1,000 h, a substrate is burned out. But this test is to test a semiconductor related diffusion on a substrate and the burning is not a problem. It may be used to test electro migration or diffusion of any metal structure in a organic substrate in near future along with a density increase for miniaturization of design component. These stress tests are applied after a preconditioning treatment level three defined by JEDEC (joint electron device council).

Figure 7.49 shows a substantial nature of package test that employed an organic substrate for flip chip application. A suite of thermal cycle test was done with different delta temperature is applied to a group of BGA package joined to motherboard and N50 life in between $\Delta T = 180$ °C and $\Delta T = 100$ °C is obtained by extending the stress test until reaching to a failure. The data was extrapolated to temperature below $\Delta T = 100$ °C that is an operation range in field of majority applications.

In the figure, a failure of BGA joint life is indicated by "BGA joint life." As described before, it is caused by a chip and substrate entity bending and the first failure occurs at the joint located in the center of BGA package that became open. It

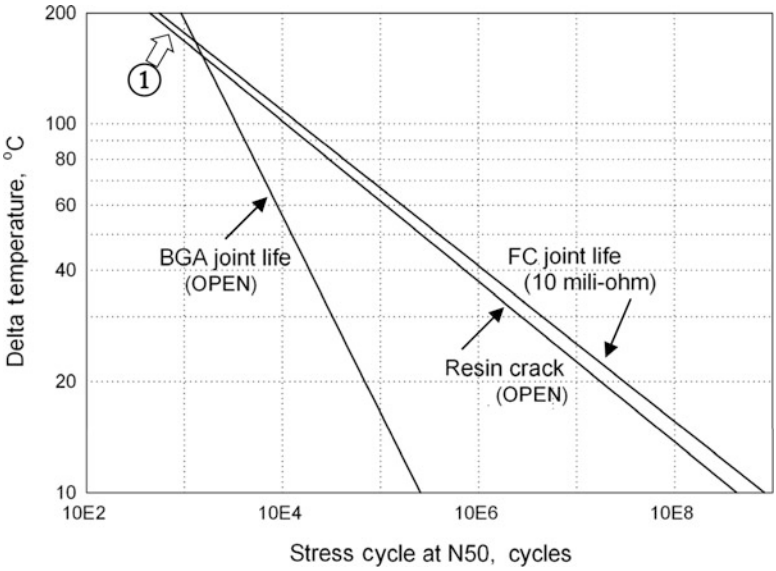

Fig. 7.49 Life estimation by failure mode. After Tsukada [14], 2000

is a fatigue failure of solder, eutectic Sn-Pb in this case, at BGA joint following the modified Coffin-Manson's formula that a life of joint follows inversely proportional to a strain at the point by square-root law. In the meantime, a failure by a line open in a substrate due to a dielectric resin crack indicated as "Resin crack" had significantly higher acceleration compared with a BGA joint and showed following approximately fifth-root law if applied Coffin-Manson's formula. These results were obtained by a different fatigue nature of solder and epoxy resin. A failure by resin crack brings a shorter life compared with BGA joint life above around $\Delta T = 160$ °C pointed by block arrow ①, but the life under $\Delta T = 100$ °C where most of application operates is much longer compared with a BGA joint life. Such result tells two important things.

1. A package life must be tested with loading to mother board, i.e., in an application condition.
2. When a material changed, a stress test to confirm an acceleration factor by failure mode has to be redone with a package loaded to mother board.

In the figure, flip chip joint life is shown as FC joint life. It was not actually a failure by reaching to the failure criteria but 10 mΩ resistance change was used by a way of experiment since it took too long test period if applied a formal failure criteria. Interestingly, as shown in the figure, FC joint life was matching with a curve of Resin crack. This indicates a flip chip joint is protected with underfill resin that is also epoxy and a degradation of joint occurs along with a degradation of resin by losing its protection.

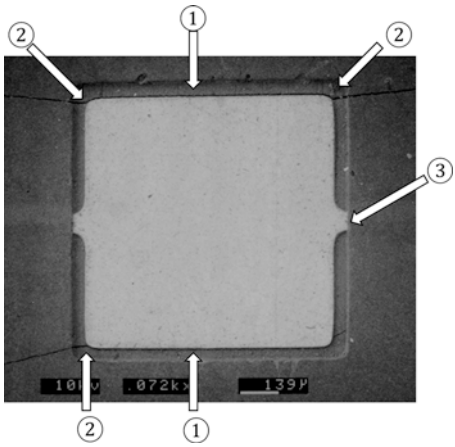

Fig. 7.50 Resin crack around pad. After Tsukada [6], 1998

One of typical failure mode of organic substrate is cracking of a epoxy resin. Even though the acceleration factor of cracking on epoxy is high as described before, it is an intrinsic failure mode and dominates a product life when stress design of a substrate is not properly performed in relation with acceleration test result. Figure 7.50 shows a typical nature of this failure mode that is revealed at certain point when a thermal cycle test is extended more than required for product life assurance. There is a crack along with a edge of large copper pad 1 mm square in size on a substrate surface, It is extended to solder mask from corners ②. Crack does not occur on an edge where there is an entry line to the pad that possibly relax the stress along the edge. This indicates a large copper structure in organic substrate should have a design feature to deconcentrate a stress around it.

Figure 7.51 shows a crack around internal conductor structure. It appears white lines around conductor pattern. When a thermal cycle test is extended more than a product life assurance, not only on surface of a substrate, a crack is possible to be found at internal dielectric layer along with a edge of copper structure such as line and land. As previously described, there is a high *Z*-direction movement in internal build-up layers that create a stress at the edge of internal copper structure. This indicates that there is a risk of such stress concentration anywhere in a substrate and one has to follow a detail design rule to avoid the stress concentration as much as possible. In addition, adding a filler to dielectric material and increase a modulus with making material harder has a certain level of effect to reduce *Z*-direction movement. It is the second benefit of adding a filler to dielectric material other than lowering the CTE. However, there must be an enough caution for adhesion of filler surface to dielectric material. Otherwise a separation of filler and dielectric becomes a starting point of crack and makes a life shorter in contrary.

Figure 7.52 shows a typical failure mode under temperature, humidity, and bias stress test. There is a clear growth of copper dendrite from cathode to anode. However, a properly fabricated organic substrate will not show this failure mode by a harmful timing to product life. Copper migration in 35 μm thickness dielectric

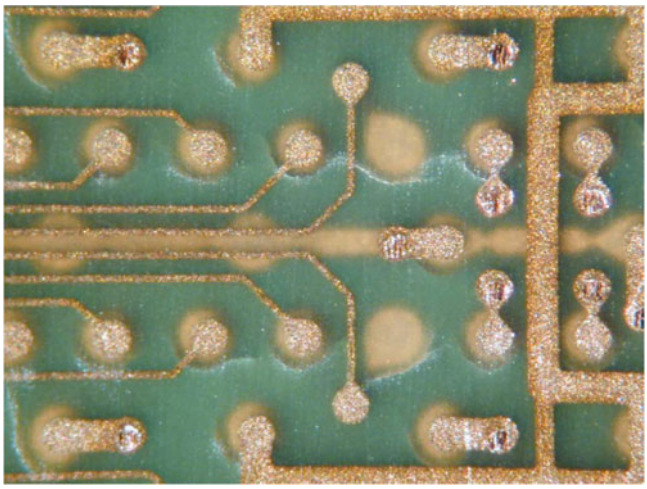

Fig. 7.51 Resin crack around internal pattern. After Tsukada [14] 2008

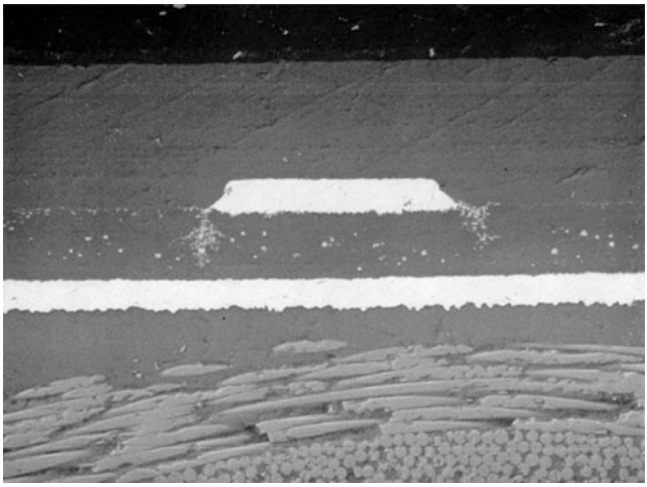

Fig. 7.52 Copper migration. After Tsukada [6], 1998

layer shown in the figure was obtained by more than 2,500 h under 85 °C, 85 %, 5 V stress condition. Since a radius of copper ion is less than an angstrom, a cross-link density of epoxy is not able to completely shut out from movement under electrical filed. Eventually copper metal migration occurs in epoxy based substrate and a consideration is just a matter of timing to a product life. Therefore, one has to have a cautious that insufficient cross-linking may cause a failure in a critical range to a product life and an acceleration factor of this failure will also vary by a bias voltage and change of electrical filed in a build-up layer. In some cases, stack up lines in

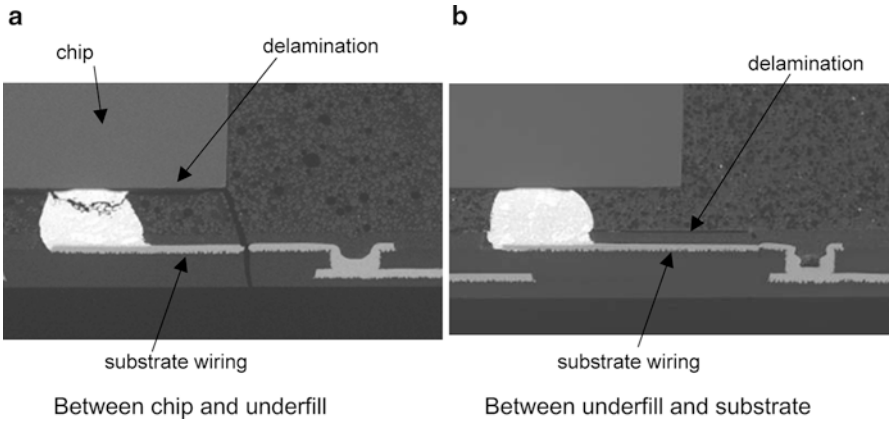

Fig. 7.53 Delamination between materials. (**a**) Between chip and underfill, (**b**) between underfill and substrate, after Tsukada [18] 2004

vertical direction by multi-layer build-up may create a stronger concentration of electrical field at the edge of line and cause a shorter life in copper metal migration.

One of typical failure of plastic material is a loss of adhesion. Since stress is distributed along with each material in an organic package as described previously, adhesion loss causes a stress concentration and ends up a breakdown of substrate wiring in most of the case. Figure 7.53 shows typical cases of such failure mode. In (a) photograph, there is a delamination between a chip and underfill. The separation cause a crack at the end of chip and the crack propagates to a direction of substrate along with a stress gradient at the point. The crack is extended into solder mask and dielectric layer. When a dielectric layer cracks, a wiring line breaks easily. In this case, there is a clear crack at the top of joint that was a result of the separation between a chip and substrate. In (b) photograph, there is a delamination between underfill and solder mask. The separation causes a stress concentration at a certain point and a dielectric resin cracks with breaking down a wiring line. As these examples, a separation of materials causes a fatal failure of a substrate and sometimes a joint failure at the same time.

Figure 7.54 shows a crack came out at the edge of underfill. Due to a nature of package bending caused by CTE mismatch of a chip and substrate, underfill fillet is under a high tensile stress since a chip and substrate tends to be separated at the edge of a chip. Normally, a modulus of underfill is higher compared with substrate materials since substrate materials have to flow and fill a space and corners between wires and/or pads. When a modulus of underfill is excessively higher than substrate materials such as solder mask and dielectric resin, substrate materials are broken down and crack is initiated at the fillet edge that propagates into the substrate as in the figure.

A substrate is the largest part of a flip chip package in its size. Figures 7.55 and 7.56 show a brief comparison of influence of substrate size on a system package size and performance. Figure 7.54 shows SiP package sizes with different size of BGA

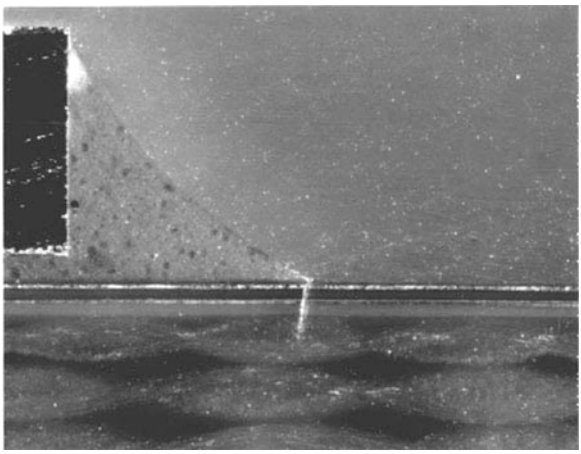

Fig. 7.54 Substrate crack at fillet edge. After Tsukada [18] 2004

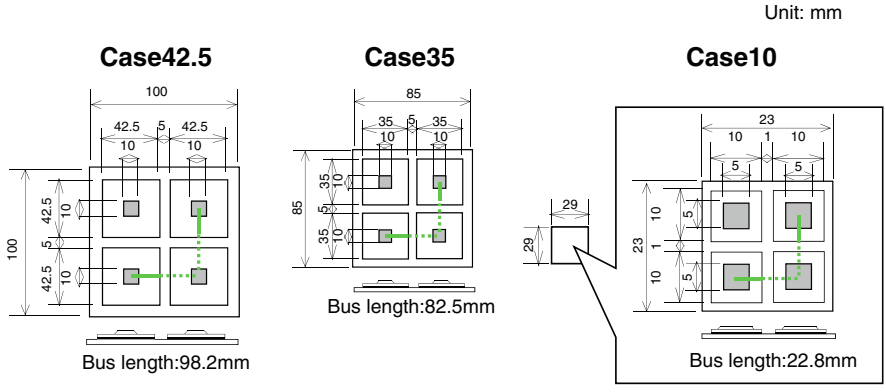

Fig. 7.55 Influence of package size for SiP size. After Tsukada [12] 2008

packages. In the figure, there are three cases depends on a substrate size of BGA to construct a SiP with four chips, i.e., four single chip packages. They are Case42.5 with 42.5 mm square BGA substrate, Case35 with 35 mm square BGA substrate and Case10 with 10 mm square BGA substrate as a case that is a several times higher density than other two cases. Four chips are lay out with these substrate size to form a SiP. To assume each substrate can contain 6,000 net for an application, each wiring rule and BGA pitch is defined.

For Case42.5; chip size: 10 mm square, substrate wiring line/space: 25/25 μm, BGA pitch: 1.0 mm.

For Case35: chip size: 10 mm square, substrate wiring line/space: 20/20 μm, BGA pitch: 0.8 mm.

For Case10: chip size: 5 mm square, substrate wiring line/space: 7.5/7.5 μm, BGA pitch: 0.2 mm.

A performance comparison is made with the worst case signal transmission with a pass right upper chip to left lower chip as a critical bus length. Resulted geometry in each case is as follows. In Case42.5, SiP size is 100 mm square and critical bus length is 98.2 mm. In Case35, SiP size is 85 mm square and critical bus length is 82.5 mm. In Case10, SiP size is 29 mm square and critical bus length is 22.8 mm.

With a signal transmission along a critical path, eye pattern of each case is shown in Fig. 7.55. Since a substrate size is large in Case42.5, eye pattern shows an possible operational frequency as 5 GHz. It improves in Case35, however the margin is not significantly increased. 10 GHz is the maximum before an eye pattern is deteriorated. In contrary to these two cases, Case10 shows a remarkable improvement on eye pattern with good margin for 20 GHz. It is obvious that a substrate size has significant influence on a total performance of package and, in addition, a unit cost of substrate becomes lower when the substrate size shrinks since a number of substrate per fabrication work size increases in reverse to the rate of shrink. Then, it allows to use higher cost material and higher cost processes with even an end cost becomes lower by such result of scaling action.

7.3.7 Historical Milestone

Figure 7.57 is a photograph of the first product in the world with a flip chip on an organic substrate that was shipped in the beginning of 1990. It was a 16 MB SIMM card for PC application with 18 chips attached directly on front and back of ordinary FR4 substrate. Chips were reinforced with underfill epoxy to protect a joint from stress caused by CTE mismatch. Since chips were memory that is low I/O, ordinary FR4 PCB was enough to work as a substrate for wiring I/O's necessary for a function of SIMM card.

Figure 7.58 shows the first build-up substrate product. Two logic chips 12 and 8.7 mm square in size at locations indicated by block arrows were attached directly to two layers build-up PCB as a substrate. (b) Shows a cross section of chip and (c) shows a cross section of build-up layers carrying micro-via holes. A dielectric material was a commercial solder mask and a micro-via hole was formed by photo etching process. Bare chips were processed through "burn-in" before installed to a build-up PCB substrate with using temporary carrier by chip attach and remove processes taking flip chip joint advantage of chip replacement technique. Since the technology was designed to handle a chip as one of a surface mount component, chips were attached in the same assembly line with other surface mount components. A function of the card was character recognition for Kanji letters.

Figure 7.59 shows the first BGA using organic substrate. 17 mm square ASIC chip with 1918 I/O's were attached on 33.5 mm square build-up substrate with four layers build-up on four layers FR4 (i.e., 4 + 4 + 4 construction). Micro-via holes were formed by photo process. There are four studs at four corners of substrate for securing heat sink. BGA joints are on a full grid array.

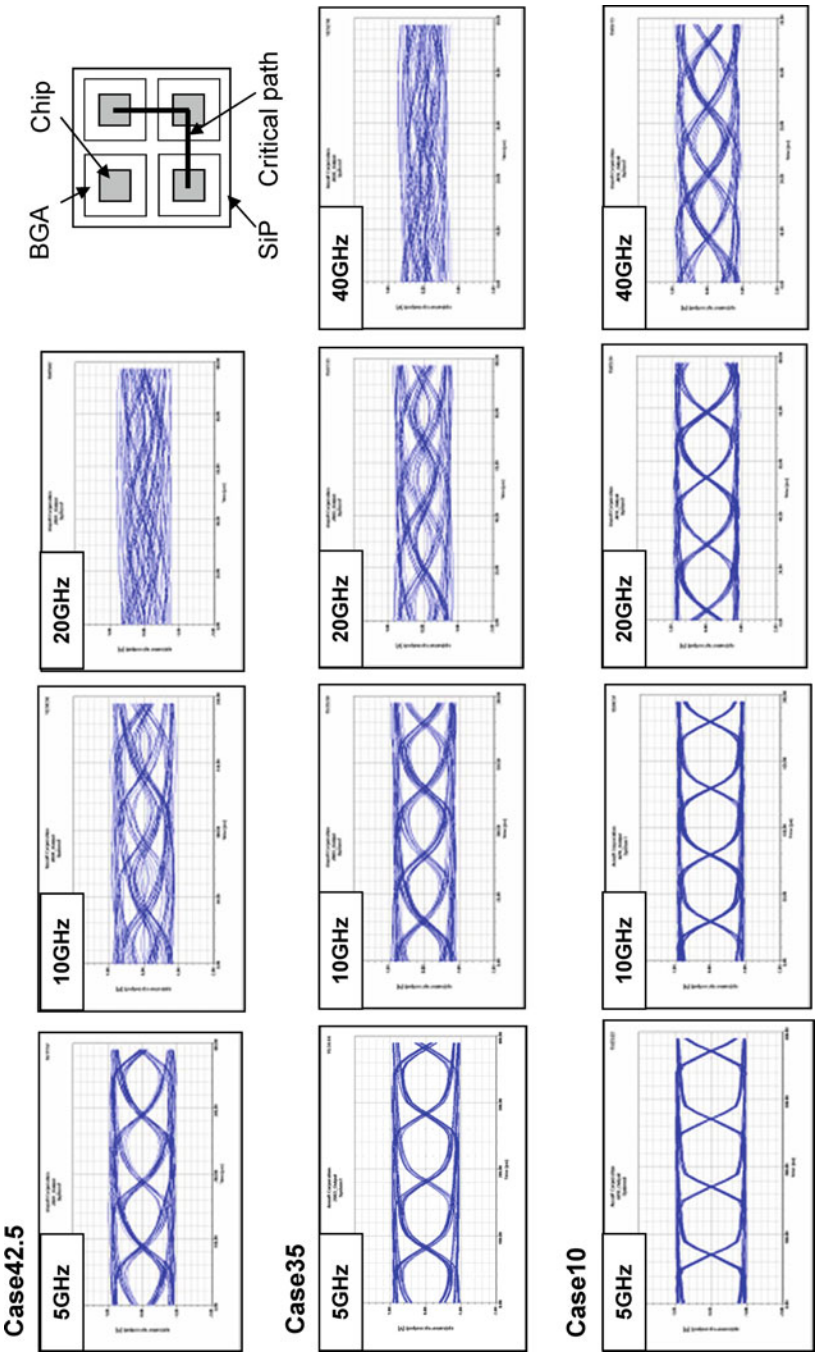

Fig. 7.56 Effect of size for performance. After Tsukada [12] 2008

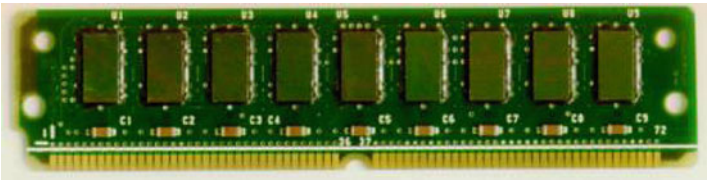

Fig. 7.57 First organic substrate product. After Tsukada [6] 1998

Figure 7.60 shows a cross-sectional photograph of the first organic substrate microprocessor for PC application. Pentium II from Intel Corporation started to use organic substrate in 1998. As shown in a photograph, a chip was attached to organic substrate with BGA package format. The BGA package was loaded onto pinned interposer to make a final format as PGA. The organic substrate employed a laser micro-via hole instead of photo via hole. A laser micro-via hole became a dominant process for organic substrate since this product.

Figure 7.61 shows photographs of the first supercomputer that employed an organic substrate package for main processor. A supercomputer named "Earth Simulator" located in Yokohama-city Japan was the first place of "Super computer TOP500" from June 2002 through November 2004. Table 7.4 describes a specification of package. A main processor package has an organic substrate that has four build-up on both sides of eight layer core ($4 + 8 + 4$ construction) with 140×112.5 mm in size. It carries a large processor chip with 19.84×21.04 mm in size that has 8960 I/O's. At the end of 2010, "Earth Simulator" is still running at 4th in supercomputer ranking with improvement in architecture and linked severs.

7.4 Z-Stack Type Substrate

Since a sequential build-up substrate is leading an organic substrate technology in cost/performance area such as CPU, GPU, and game processor substrates where a superior performance is required as well as low cost, there is not so many variations in its structure other than detail design elements. In the meantime, Z-stack type has more varieties in its application because it has been mainly used in low-end area such as mobile devices and consumer products. Not only applications, there are some unique features in each fabrication method.

7.4.1 Z-Stack Substrate With Pattern Transfer

In this section, Z-stack type substrate "CPCore" from KYOCERA SLC Technology Corporation is introduced as one of such examples. Figure 7.62 shows a process flow of this method. (1) A sheet of copper is attached to a polymer carrier film and a dry

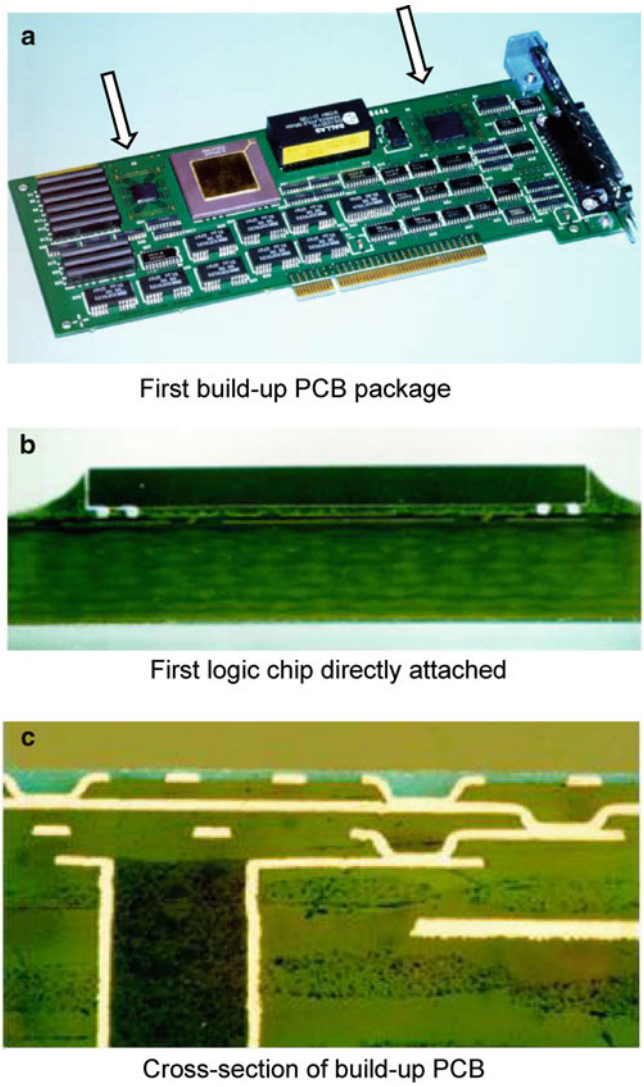

Fig. 7.58 First logic chip on build-up substrate. (**a**) First build-up PCB package, (**b**) first logic chip directly attached, (**c**) Cross section of build-up PCB. After Tsukada [6] 1998

film resist is laminated for circuit patterning. The resist is exposed and developed to form a wiring pattern of copper on the polymer carrier film. (2) In parallel, uncured (green) dielectric sheet is drilled by laser to form via holes. Then via holes are filled with conductive paste made of copper particles and resin binder. (3) The wiring pattern is transferred onto an uncured dielectric sheet. The uncured dielectric sheet with transferred circuit for each layer of substrate design are stacked, then, pressed

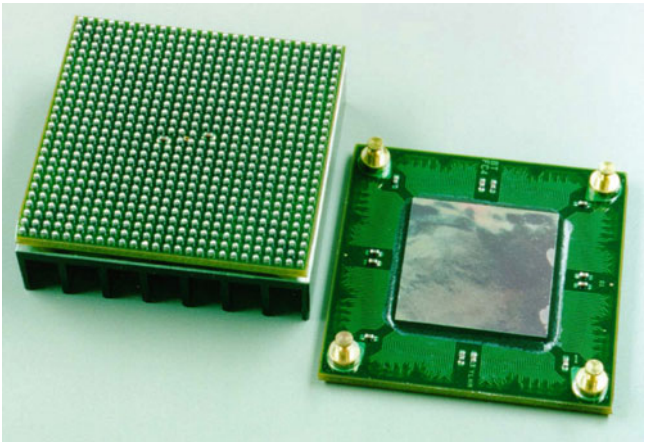

Fig. 7.59 First BGA using organic substrate. After Tsukada [14], 2000

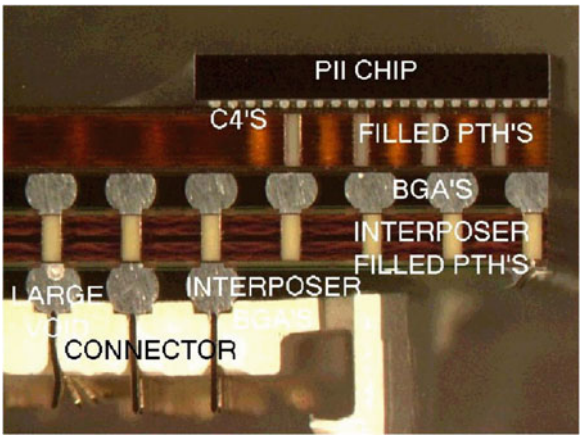

Fig. 7.60 First microprocessor on organic substrate. After Tsukada [13] 2008

and cured by a hot press for completing a substrate. The flow of the simultaneous curing process is similar to that of the green sheet process of ceramic substrate.

Figure 7.63 shows a connection of conductor copper to paste in via hole. In wiring pattern transfer process, a copper conductor pattern is buried into a prepreg by pressure. At the same time, conductive paste that fills a via hole is depressed by a thickness of buried copper conductor. The conductive paste that fills a via hole and copper conductor is firmly adhered by the depression action to secure the connection. Finally, CuSn intermetallic compound is formed in the interface of copper conductor and conductive paste to secure the reliability of connection.

Figure 7.64 shows a cross section of completed seven metal layers substrate. A prepreg is using a thermo setting PPE (Polyphenylene ether) for better processability and electrical characteristics.

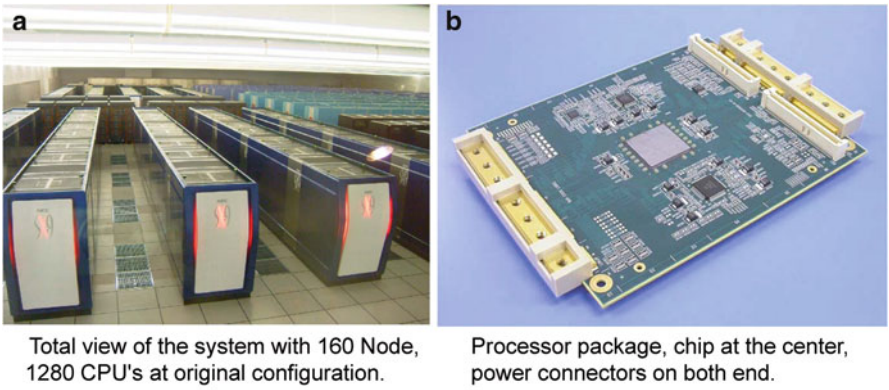

Fig. 7.61 First supercomputer with organic substrate package. (**a**) Total view of the system with 160 Node, 1280 CPU's at original configuration. (**b**) Processor package, chip at the center, power connectors on both end. Courtesy by Inasaka, NEC Corporation

Table 7.4 Package specification, courtesy by Inasaka, NEC Corporation

LSI I/O (Sig.)		8,960 (1,791)
LSI size (mm)		19.84 × 21.04
PKG size (mm)		140 × 112.5
FC joint		Sn/Ag/Cu
Cap.	On chip (nF)	1,020
	On PKG (uF)	103
Layer count		4Bu-8core-4Bu
PKG connection		Cable connector
PKG pins (Sig.)		2,628 (1,521)
Wire length (m)		80
CLK (GHz)		3.2
Power(W)		250

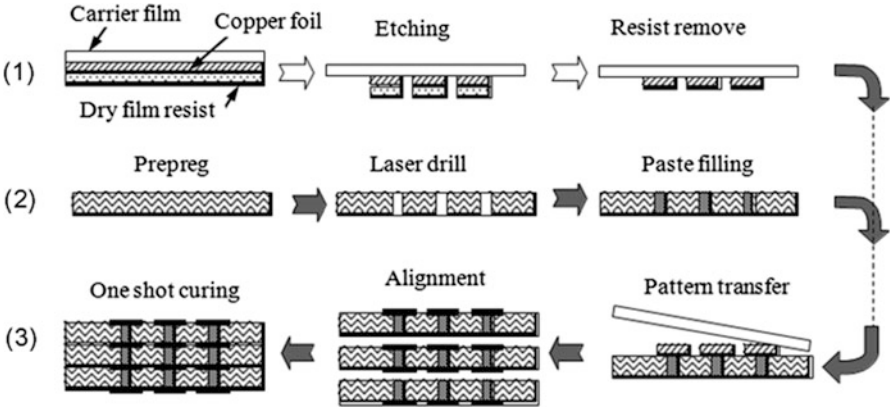

Fig. 7.62 Z-stack and pattern transfer. After Tsukada [18], 2004

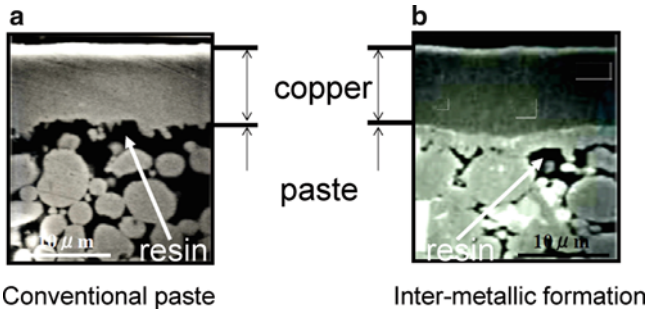

Fig. 7.63 Via hole connection. (**a**) Conventional paste, (**b**) intermetallic formation. After Tsukada [18], 2004

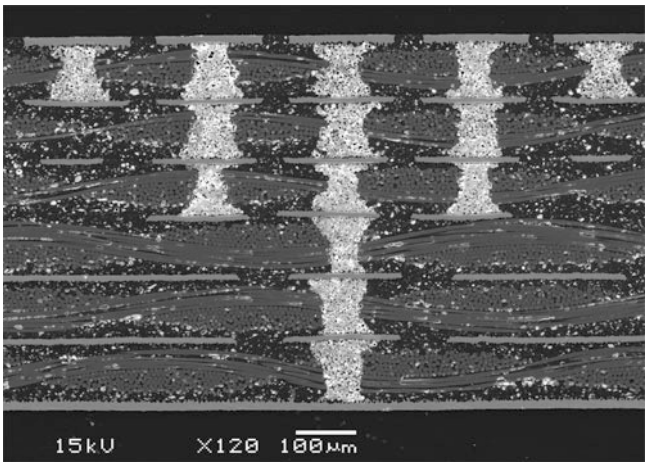

Fig. 7.64 Completed Z-stack substrate. After Tsukada [18], 2004

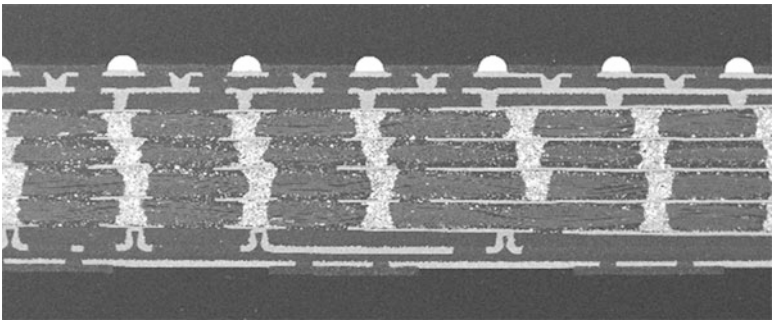

Fig. 7.65 Z-stack + build-up combined substrate. After Tsukada [18], 2004

Figure 7.65 shows a version of Z-stack and sequential build-up combined substrate for a higher density application.

7.4.2 Any Layer Via Substrate

There is a substrate called as "Any layer via." Originally "Any layer via" is the name put on a Z-stack type substrate. It was started with "ALIVH" from Panasonic. The name of "ALIVH" itself is a shorten version of "Any Layer Interstitial Via Hole." It does not have a core and all layer is a stack of same structure. Each layer of substrate is prefabricated with a laser drilled micro-via hole fill with conductive paste and stacked by press to complete a substrate. However, there is another type of substrate called "any layer via." It is essentially a sequential build-up substrate with a core at the center, but the core is very thin as it looks the same structure with build-up layers. Therefore, its cross section looks like coreless substrate. But the design rule is quite different since each layer is using a prepreg that has a glass fiber cloth inside. Though a very thin glass cross that is introduced also in this chapter is used, line and micro-via hole size are far coarse from the level of a regular build-up substrate. High yield with very low level wiring ground rule, a number of sequential build-up count is high as a several layers on each side of a core.

7.4.3 Embedded Component Substrate

An ordinally embedded component substrate is burying components at a core part of a sequential build-up type substrate. A core with buried components is fabricated first and the build-up layer is applied later. Since an embedded component substrate is an application oriented package, there are wide variations of its design in detail. In this section, as a unique example of embedded component substrate, "B^2it" (buried bump interconnection technology) from Dai Nippon Printing with embedded component is introduced. B^2it is one of a Z-stack type substrate with employing a unique bump via construction method. Figure 7.66 shows a basic process flow.

1. Printing: Ag paste is printed on Cu foil to form a conductive bump. A paste is cured and a bump is formed like conically shaped protrusion as shown in a photograph.
2. Piercing: A prepreg sheet is laid up and pressed so that a bump comes through prepreg by breaking and pushing aside a glass fiber.
3. A Cu foil is laminated and pressed to complete a via connection. Then, a laminate is forwarded to a patterning process.

After completing a patterning, proceed to a press process to complete a substrate as shown in Figure 7.67.

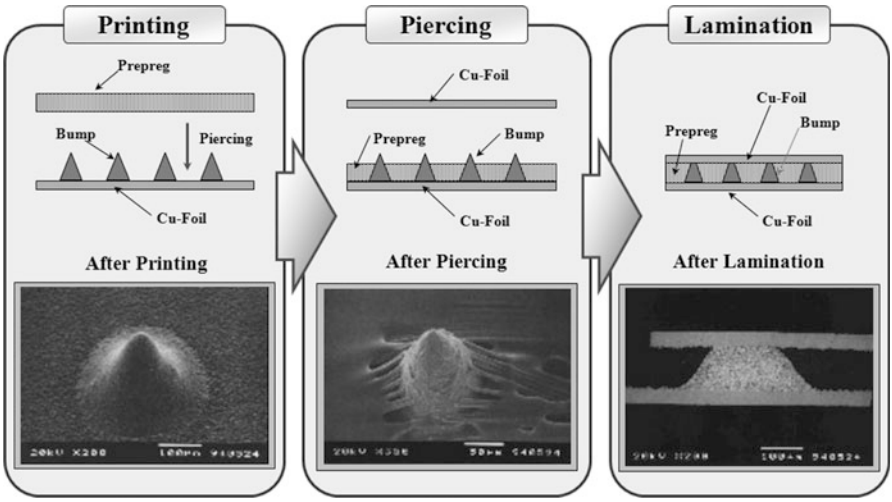

Fig. 7.66 Basic process flow. Courtesy of Dainippon Screen MFG. CO., LTD.

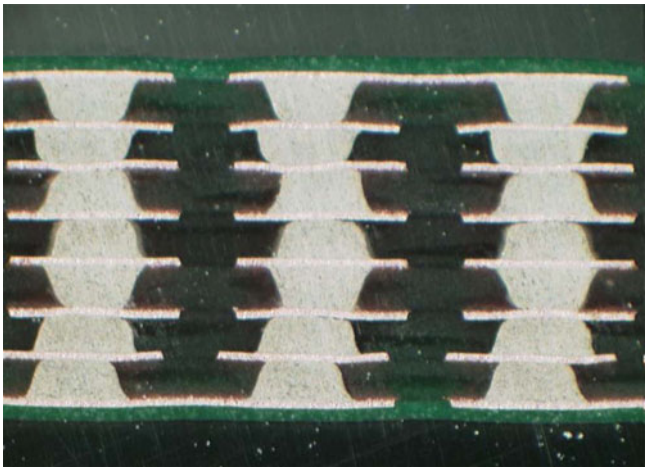

Fig. 7.67 Completed B^2 it substrate. Courtesy of Dainippon Screen MFG. CO., LTD.

Figure 7.68 shows a variation of substrate that is fabricated with other method. (a) Shows a photograph of combination with an ordinary thorough hole core. (b) Shows a combination with build-up layer with a laser micro-via hole.

Figure 7.69 shows an example of component embedded substrate. Buried components are three wafer level CSPs and total 18 passive components that are 1005C and 0603C. The substrate size is 9.2 mm square with 0.65 mm in thickness and constructed with six layer B^2it. A Halogen free dielectric material is used.

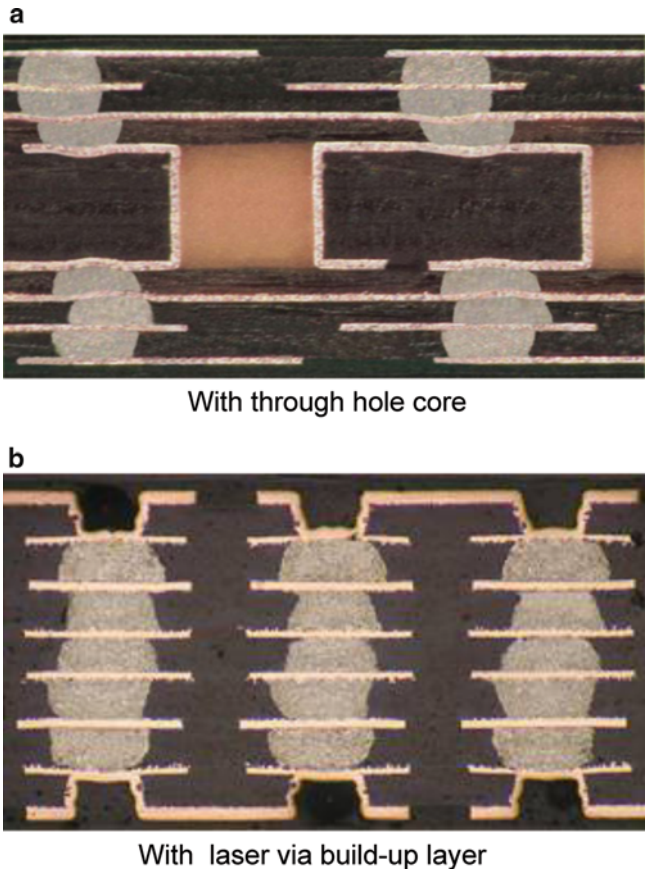

Fig. 7.68 Combination with other method. (**a**) With through hole core, (**b**) with laser via build-up layer. Courtesy of Dainippon Screen MFG. CO., LTD.

Figure 7.70 shows an example of active component embedded substrate. Buried components are a bare chip with 3.1 mm in size, 1005c and 0402C passives in total ten pieces. The substrate is 8.5 mm square with 0.48 mm in thickness with seven layers B^2it. Overall package thickness is 1.0 mm with 46 total components including a quartz. A function of the module is NFC (near field communication) that a requirement is getting high in recent days.

Figure 7.71 shows a process flow of embedded component substrate introduced in a previous figure. As the first step, front side layer and base layer by B^2it process are provided. Also a core part that carries internal wiring plane is provided. Assemble passive components onto a base layered by regular SMT process and a bare chip is attached with flip chip bonding. Bumping and prepreg lamination on one side of front layer and core part are done. Cavities for chip and passives are formed. Lay up all parts and lamination press process completes a stacking of layers. Solder mask is applied and assemble other necessary components to finish a product. Most of

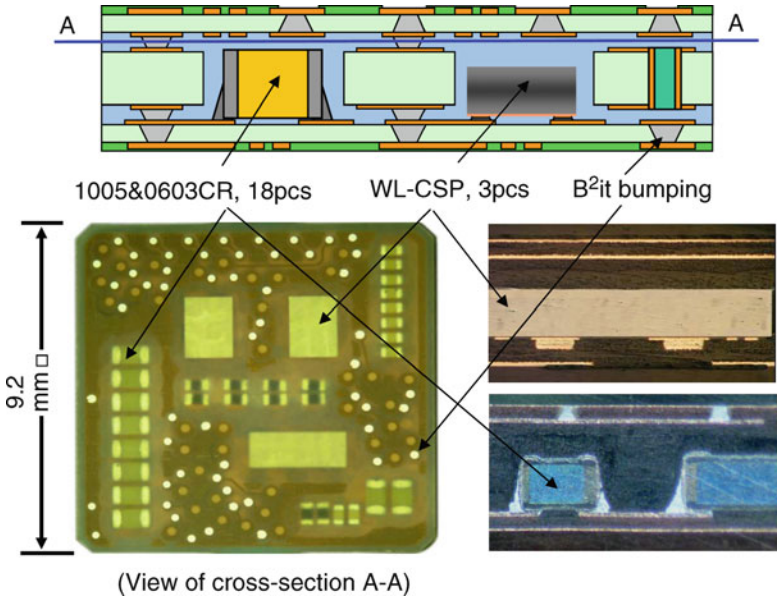

Fig. 7.69 Example of WL-CSP and passives imbedded. Courtesy of Dainippon Screen MFG. CO., LTD. [19] 2010

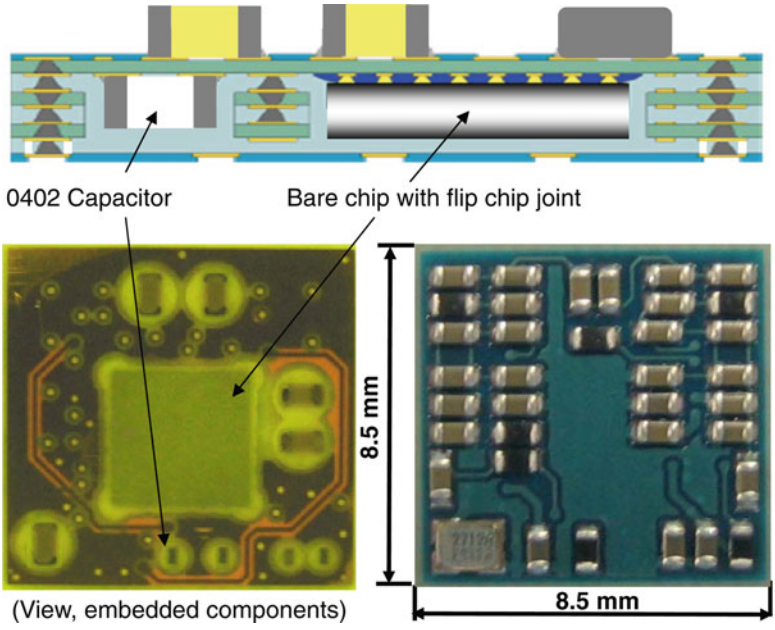

Fig. 7.70 Example of embedded active component. Courtesy of Dainippon Screen MFG. CO., LTD. [20] 2007

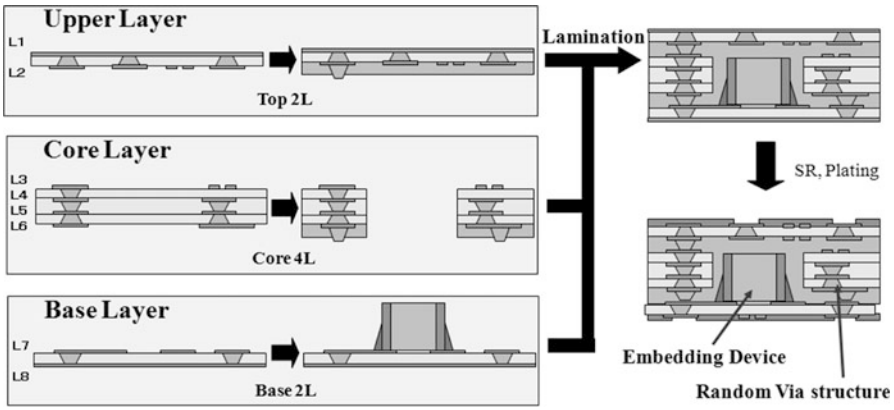

Fig. 7.71 Process flow of embed component substrate. Courtesy of Dainippon Screen MFG. CO., LTD. [20] 2007

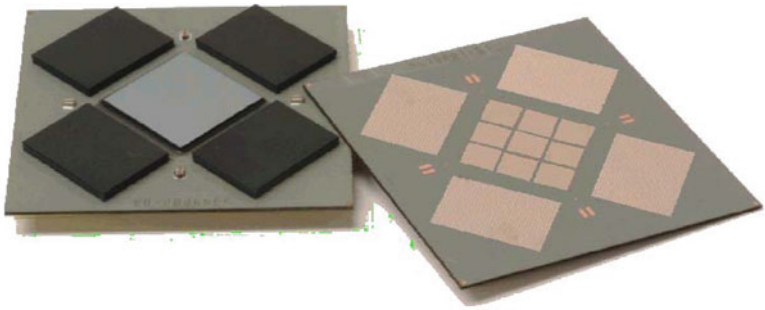

Fig. 7.72 Substrate with PTFE for high speed signal. Courtesy of Endicott Interconnect Technologies, Inc.

embedded component substrates are in peripherally of portable phone product in primacy of thin and small advantages.

7.4.4 Substrate With PTFE Material

Figure 7.72 shows a substrate that employs an unique material for high speed signal transmission. "HyperBGA" from Endicott Inter Connect Technologies, Inc. is a flouropolymer-based coreless semiconductor package that allows run a signal at extremely high rates of speed. The combination of the low loss, low dielectric constant material and strip line cross sections enable signal speeds surpassing 12 Gb/s. The material compliance of the PTFE, combined with the dimensional stability of a copper-invar-copper center plane, enables long field life, with none of the BGA joint wear out, die cracking, delamination or flip chip bump fatigue.

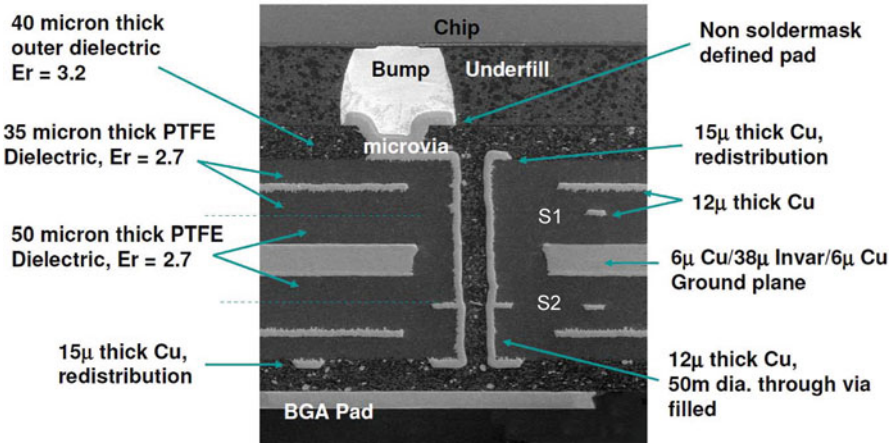

Fig. 7.73 Substrate cross section. Courtesy of Endicott Interconnect Technologies, Inc. [21], 2003

Table 7.5 Material property

PTFE dielectric constant	2.7 at 10 GHz
PTFE loss	0.003 at 1 MHz
Outer layer dielectric constant	3.2 at 1 GHz
Outer layer loss	0.0027 at 1 MHz
Composite flexural modulus	1.2 Mpsi
Coefficient of thermal expansion	10–12 ppm/°C

Figure 7.73 shows a unique coreless structure in cross section. At the center, a thick copper-invar-copper is set for controlling CTE and dimensional stability.

There are two signal layers S1 and S2 that are embedded in a strip line environment sandwiched between either voltage plane and center core (ground plane). Two redistribution planes located outer side of voltage planes support escape lines from flip chip joint to signal wiring. Top and bottom planes only provide a flip chip pad and a BGA pad, respectively. Interlayer connections are accomplished with micro-via holes and plated through-holes (PTHs).

Table 7.5 describes material property of this substrate. PTFE provides a low dielectric constant and low dielectric loss. And, overall low CTE and low modulus lower the stress at flip chip joints.

7.5 Challenges

7.5.1 Coreless Structure

Figure 7.74 shows a cross section of a coreless structure. One of weak points of sequential build-up type substrate is a construction of core, particularly a through

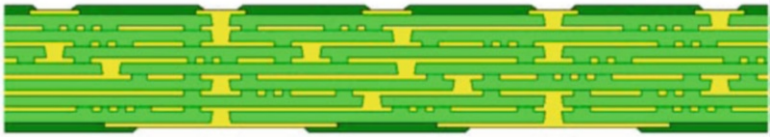

Fig. 7.74 Coreless substrate

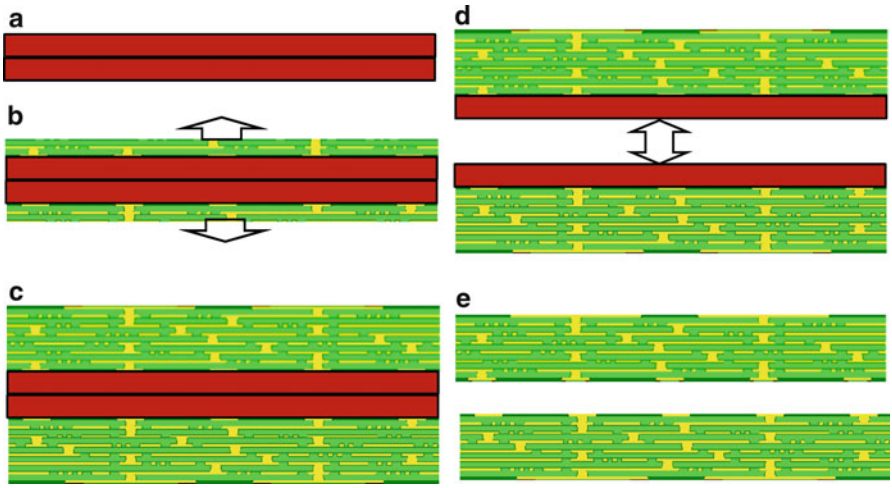

Fig. 7.75 Coreless process steps

hole. Since a core is carrying a role to provide a mechanical rigidity, it is normally thicker than build-up layers. A path from front side to back side is a through hole that is currently processed by a mechanical drilling process. It is larger in dimension compared with a micro-via hole and becomes an obstacle in terms of electrical performance. The idea is to delete a core portion from a standard sequential build-up structure.

However, problems are a low modulus of laminate that causes dimensional stability worse and a cost if it processed by sequential build-up in one side since an ordinary sequential build-up is processed on double side. To resolve a cost issue, as shown in Fig. 7.75, the development is focused to prepare a core made of two parts adhered using a dummy panel and process build-ups on both sides of the core. After finishing the fabrication, the work panel is separated and a remaining part of core that has been with a coreless part is removed. Finally, two sequential build-up coreless panel is made for a process to substrate pieces.

Even though taking such effort, there are fundamental issues on this type of substrate. One is a low modulus and dimensional stability of a finished part since build-up laminate material is a plastic that is essentially very low modulus like

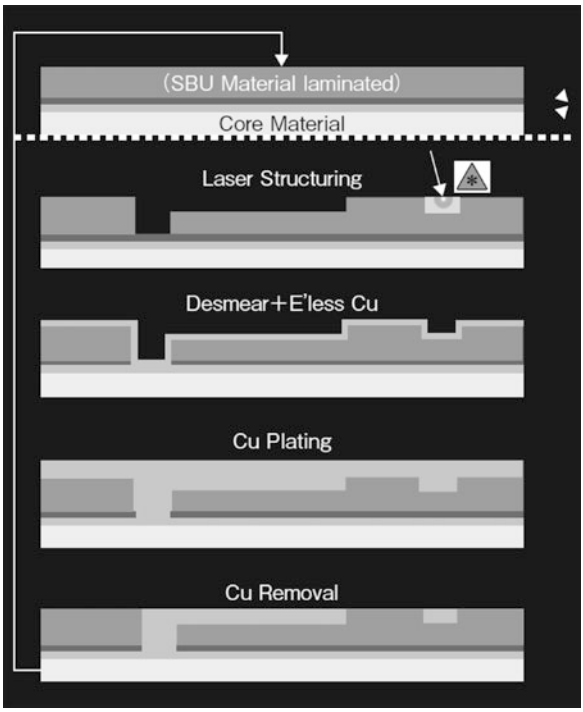

Fig. 7.76 Process flow of trench structure. Courtesy of Baron, Atotech Deutschland GmbH [23], 2011

5–7 GPa. Yet a copper in the laminate is high modulus compared with such resins. Therefore a finished laminate shows a bend, twist and distortion that are more in local area of substrate rather than a global uniform warpage compared with standard construction with a core. This nature will vary by each design since it depends on a conductor pattern. In addition, theoretically it is higher cost since a number of sequence to make a build-up is about twice of making a standard sequential build-up substrate that creates significant impact on yield loss since a lager build-up count becomes one of major weak point of sequential build-up process that is described in early part of this chapter. In standard sequential build-up substrate, a core is shared for power planes that is coarse in wiring rule with utilizing ordinary PCB process to lower the cost. In addition, it is said as disadvantage of core because a lower (back) side build-up wiring plane is not fully utilized since through hole density is not reach to the density of micro-via plane in build-up. However, particularly in BGA substrate, BGA side wiring density is not necessary high compared with front side that is high density since it contains chip area escape lines.

In recent disclosures, it was described as superior in performance and user company of a substrate took an effort to assemble a retainer for warpage counter-measure and implement an improvement on a positioning system in assembly process to avoid tipping of substrate [23].

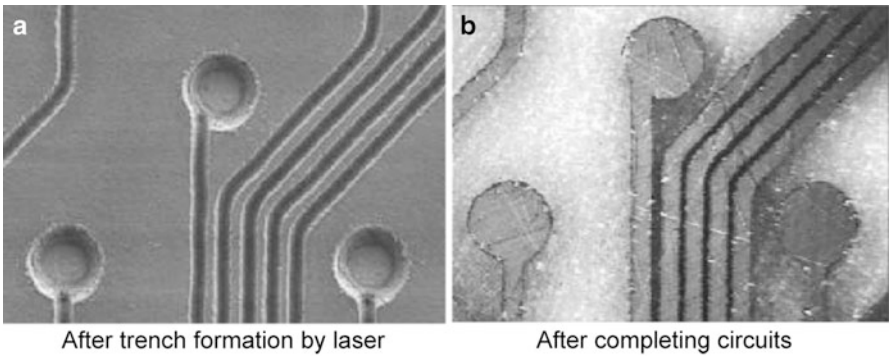

Fig. 7.77 Trench and finished circuit pattern. (**a**) After trench formation by laser, (**b**) after completing circuits. Courtesy of Baron, Atotech Deutschland GmbH [23], 2011

7.5.2 Trench Structure

Figure 7.76 shows a process flow of a substrate fabrication method named laser trench method named as "V2" from Atotech Deutschland GmbH. The process consists of laser curving and plating with planarization, and eliminating photo circuitization process that is carrying a major yield detractor in an organic substrate fabrication process. The first step is a laser abrasion after a lamination of dielectric material. Laser grooves lines and via holes. Since a depth control of UV-YAG laser can be done far finer than CO_2 laser due to its low energy per shot with high frequency, conductor and via depth are controlled. After a surface roughening of light desmear process, seed layer is formed by electro-less copper plating. Lines and via holes are by electroplating. Each circuit element is completed by planarization process and a substrate moves to next layer step.

Figure 7.77 shows grooved trenches. (a) Shows a trench pattern formed by laser grooving and (b) shows completed conductor lines and via holes. One of advantages of is method is to form lines and via holes by a single registration at laser tool compared with two registrations are involved that are laser process and photo process in case of ordinary build-up process steps.

Figure 7.78 shows a cross section of a pattern and via hole. By utilizing a plating additives specially designed for this purpose, filling of all pattern is possible with minimum dimple height with less than 10 μm plating thickness remained on the general area of dielectric surface.

Figure 7.79 shows a result of dense fine pitch lines and cross section of product substrate. It is said in the disclosure that key points for success are plating thickness control and planarization. Filler particle size in dielectric material relative to design rule is also important to achieve uniform geometry definition by laser abrasion. 355 nm UV-YAG and 248 nm excimer laser are capable below 10 μm wiring features.

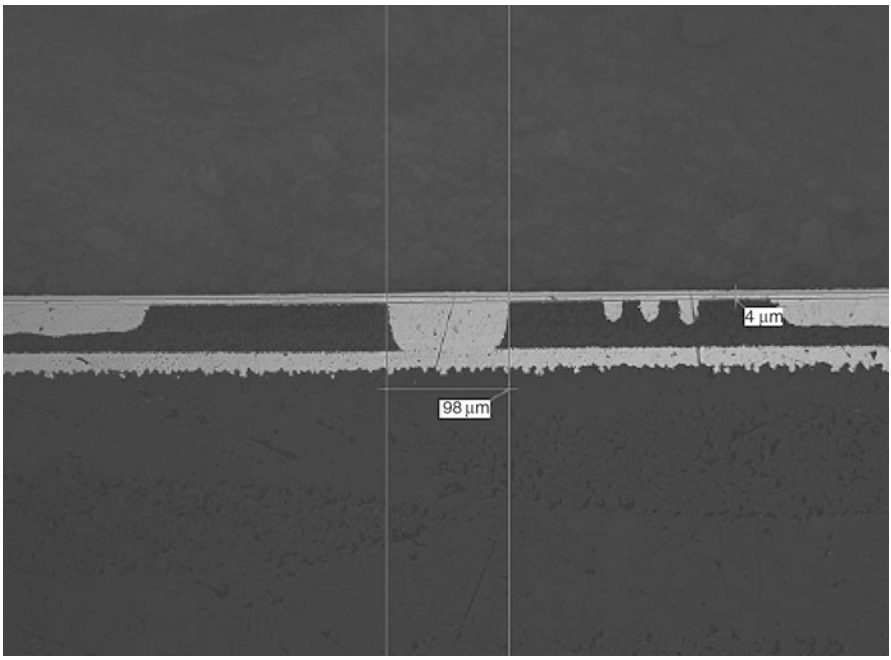

Fig. 7.78 Cross section after copper plating. Courtesy of Baron, Atotech Deutschland GmbH [23], 2011

7.5.3 Ultralow CTE

A basic issue of a current organic substrate is its high CTE due to carrying a conventional PCB material set. It has been a common understanding that an organic substrate CTE has to be lower to reduce a global miss-match of CTE with a silicon. A question has been how low the CTE is possible to be. Figure 7.80a shows a cross section of construction to reduce a CTE with a new material set. The configuration of three build-up layers on both side of two metal layer core. The core has organic fiber made of a poly-p-phenylenebenzobisoxazole (PBO) with a CTE as low as -6 ppm/°C and a high Young's modulus of 270 GPa. The fiber is impregnated with a polyamide resin. The uniqueness of a core is not only a material set but the way of impregnation. The fiber is featured in an unidirectional construction that achieves a resin content of the prepreg as low as 40 % to raise an effectiveness of fiber reinforcement on the CTE. The core CTE is shown as "0 + 0 cu %" in Fig. 7.79b that reaches to -1 ppm/°C. In (b) of the figure, the CTE of 3 + 2 + 3 composite is shown approximately 3.5 ppm/°C. Another point that needs attention in the figure is an influence of copper. Beside a composite CTE measurement that is done with 50 % copper ratio in wiring plane, a case with 100 % copper ratio is shown and tells us a copper has a significant influence to a global CTE of substrate due to high CTE as 17 ppm/°C with high modulus around 100 Gpa. It is a point to be emphasized in low CTE challenge in an organic substrate.

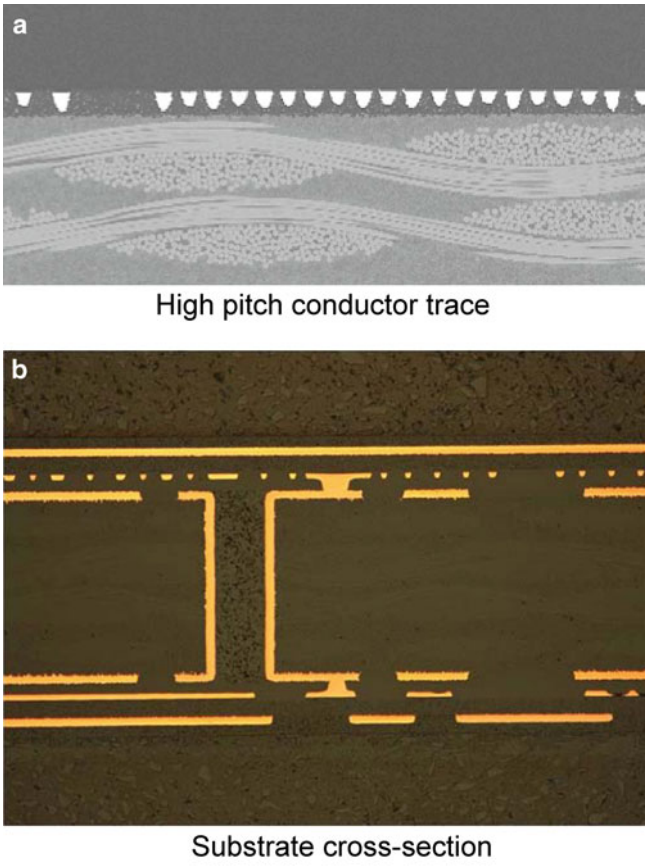

Fig. 7.79 Completed structure. (**a**) High pitch conductor trace, (**b**) substrate cross section. Courtesy of Baron, Atotech Deutschland GmbH [23], 2011

With an ultralow CTE construction, a product prototype is built as shown in Fig. 7.81 and cleared required stress tests target. The substrate size is 10 mm square with 100 μm pitch through holes in the core and 8–10 μm pitch lines in build-up layers with 100 μm pitch flip chip joint. These features accommodate the density of a chip I/O of 104 cm^{-2}, which is about ten times greater than that achieved in a current organic package and expected to satisfy the next generation requirement.

7.5.4 Substrate for Stacked Chip

In the last decade, there have been heavy research and development activities for stacking a semiconductor chip since the density increase has been getting to face higher wall to future generations. Figure 7.82 describes various issues and concerns

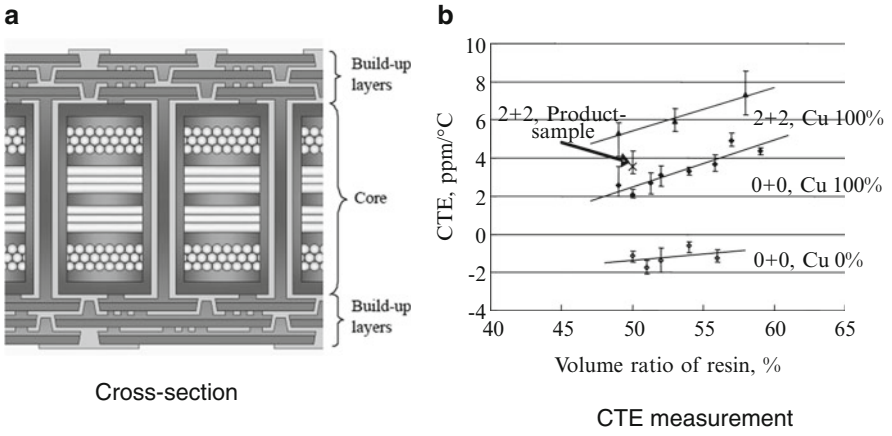

Fig. 7.80 Ultralow CTE substrate. (**a**) Cross section, (**b**) CTE measurement. Courtesy of KYOCERA SLC Technology corp. [24] 2009

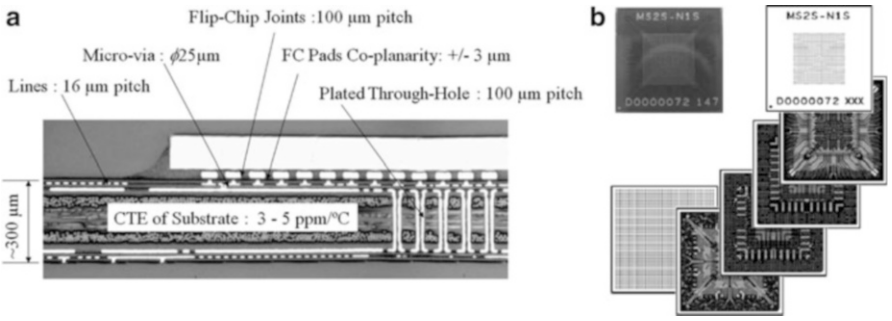

Fig. 7.81 Prototype of next level package. (**a**) Cross section, (**b**) layer patterns. Courtesy of KYOCERA SLC Technology corp. [24] 2009

relating to chip 3D stacking. Most of such efforts have been focused TSV (through silicon via) and the technology seems to become viable in these years. The work has been moving to other issues. Within others, issues connected by an curved arrow in the figure are to be grouped in terms of thermal stress management, i.e., "Chip Package Interaction." The cause is the same as described in the earlier section of this chapter for 2D packaging but more severe condition by a dimension compared with 2D. The key is that a reliability of package today is not just a reliability of packaged part but must be confirmed by loading the package on an application condition. If the package is used on an application PCB board, the reliability must be assessed with loading to the board. Within CPI related items, silicon substrate has been emphasized and significant numbers of papers and reports were disclosed,

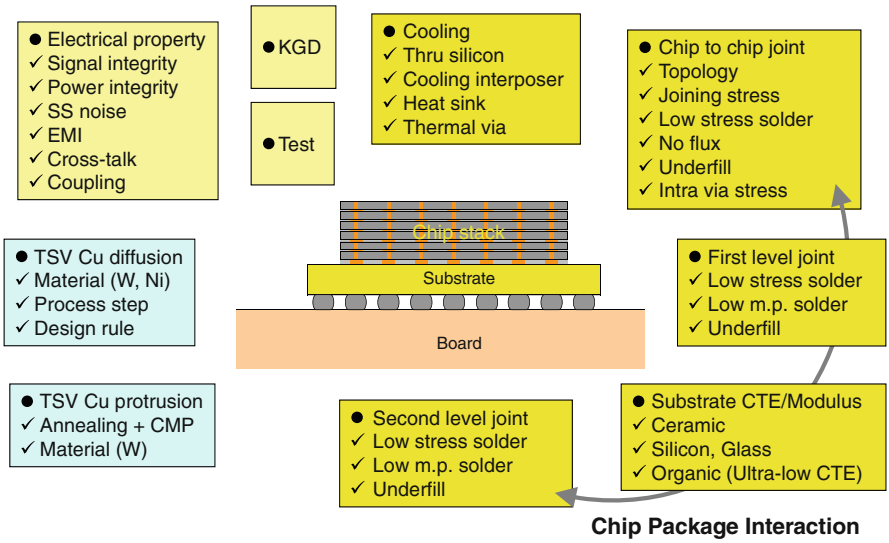

Fig. 7.82 Issues in 3D chip stacking

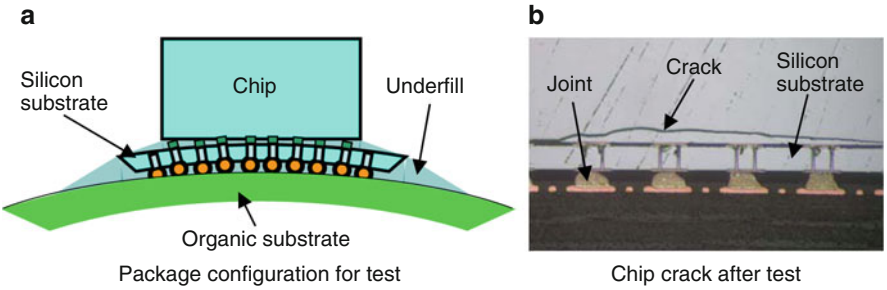

Fig. 7.83 Silicon substrate with IMC flip chip joint. (**a**) Package configuration for test, (**b**) chip crack after test. Courtesy of Orii, IBM Tokyo Research [25], 2010

but there found least reports regarding comprehensive reliability assessment including in an application condition by the time of this manuscript written.

Figure 7.83 is one of least disclosure of silicon substrate assembled on an organic substrate. In the disclosure, a chip was assembled on 150 μm thick silicon substrate. Gaps between chip to silicon substrate and silicon substrate to organic substrate were filled with underfill resin. An organic substrate can be regarded as an application board when a silicon substrate is directly used in an application. If there is no underfill between silicon substrate and organic substrate, the condition is almost the same with a case that bare chip is attached to organic substrate with no underfill and a joint does not withstand to a stress by thermal cycle. (b) Shows a result that the package was stressed under −55 to 125 °C ($\Delta T = 180$ °C) thermal cycle test. (b) Shows a resulted chip crack by the stress when a joint material was CuSn intermetallic. It is also

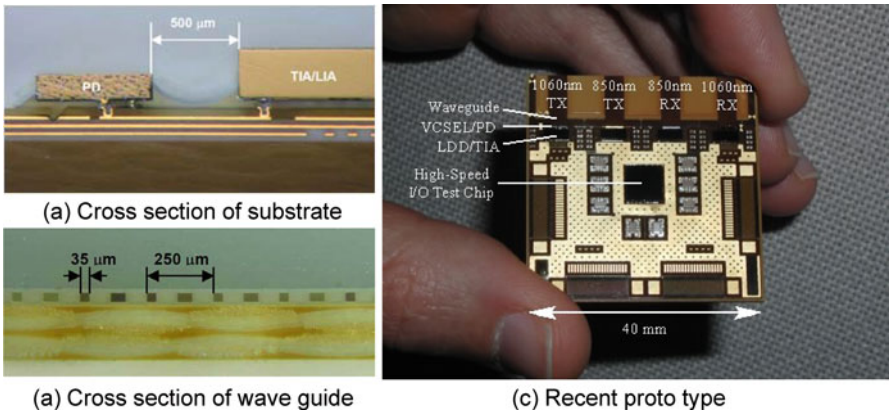

Fig. 7.84 Optical wave guide substrate. (**a**) Cross section of substrate, (**b**) cross section of wave guide, (**c**) recent prototype. After Nakagawa [26] 2008, After Tokunari [27] 2010

reported that there was no crack when a joint material is in that is quite soft compared with the intermetallic. This result indicates that if flip chip joints are harder than certain level, a CTE mismatch between silicon chip and organic substrate is enough to cause a damage to the chip even if there is underfill that tightly adheres the chip with an organic substrate and causes least displacement in *X*–*Y* direction. Hence, an attention to *Z*-direction stress has to be paid. This result clearly indicates that a reliability of 3D chip stack package must be assessed with an application condition, not just a package level reliability. It is the same nature that has been described about reliability in this chapter.

7.5.5 Optical Wave Guide

"Heat" is one of a major issue of today's high performance computer. Suppressing a clock frequency by a parallel processing with multi-core technology is on-going. However, since multi-core requires high bandwidth communication between processor and memory. A large number of electrical connection still require high power and generate heat. It is ideal if such communication is converted to optical technology that is already available to system gate and reaching to board level. Therefore, optical technology on a package level is required in near future. One of such development activity is to provide optical wave guide on substrate and prepare a MCM by flip chip technology. Figure 7.84 shows one of such activity. (a) shows a cross section of a prototype package with wave guide layer put on a build-up layer of a substrate, and a cross section photograph shows a dimension of wave guide tested that contains 35 μm core and 55 μm dummy pattern on 250 μm pitch [26]. (c) shows a latest prototype package that has demonstrated 20 Gb/s data rate per transmitter channel and the 40 mm square module can support 2 Tb/s bandwidth [27].

7.6 Ceramic Substrate

Figure 7.85 shows a typical ceramic substrate of flip chip bonding. Photo(a) shows the outside appearance of a substrate with front side (left) and back side (right). Photo(b) shows a cross section of substrate at a chip side. Vertical via connections with high number of layers are clearly seen.

Table 7.6 with Fig. 7.86 describes design dimensions for a flip chip substrate. Dimensions are in a set with via hole size as a primary parameter. Stacking layer count can be provided up to 35 layers as maximum. Majority is in 18–26 layers for a flip chip package.

Table 7.7 describes material properties available. There are a variety of materials for a substrate. Alumina has several types with detail arrangement. AlN (aluminum nitride) provides lowest CTE. LTCC (low temperature co-fired ceramic) provides low resistivity conductor such as Ag and Cu with sintering low temperature compared with other ceramics. There are unique items in LTCC. Than is a high CTE ceramic substrate material. An underfill effect is available on ceramic substrate. It is not the same magnitude as an organic PCB but enough to extend a flip chip joint life than no underfill flip chip bonding. Since a flip chip joint is protected by underfill, a high CTE substrate material is designed to share a protection more on BGA joint side.

7.7 Roadmap

7.7.1 JEITA

JEITA (Japan Electronics and Information Technology Industries Association) is an industry association for electronics and information industry and issues Japan Jisso Technology Roadmap in every other year that is subjected to fees. The latest was issued on May 2011. Within six working group in total, WG5 with 17 member firms is in charge for printed wiring board including substrate technology. Roadmap consists of ten sections partitioned with four groups and is made with referencing a questionnaire to Japanese material and PWB makers. In rigid PWB section includes build-up, multilayer, double side, and single side PCBs. FPC section includes multilayer, double side, and single side. TAB/COF is a short shingle section. Substrate section consists of tape, rigid, build-up, and ceramic in categories. There are common and difficult challenge parts in addition. In each section, roadmap parameters are described with 10 years outlook and categorized in three lines of numbers that are “class A: high volume production,” “ class B: advanced with limited makers” and “class C: challenge with no high volume production.” For a semiconductor package substrate, a product range is stated as, class-A for a low end product like Memory, class-B for a mid-range like CPU and class-C for a high-

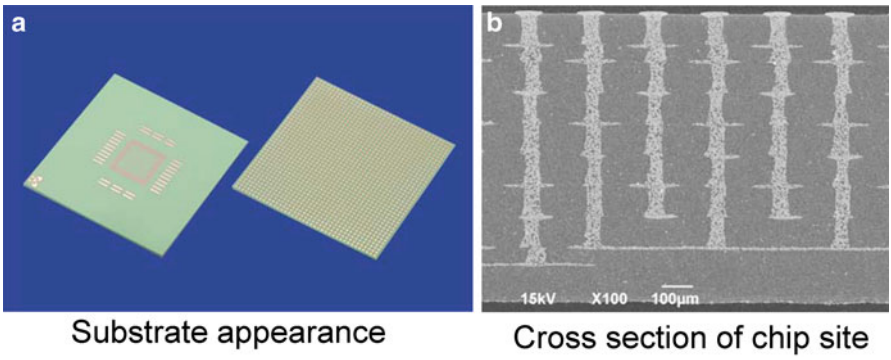

Fig. 7.85 Ceramic substrate. (**a**) Substrate appearance, (**b**) cross section of chip site. Courtesy of KYOCERA Corporation

Table 7.6 Design dimensions, courtesy of KYOCERA Corporation

Item	CC200 (mm)	CC100 (mm)	CC075 (mm)	CC050 (mm)
(a) Via hole dia	0.200	0.100	0.075	0.050
(b) Via cover dot dia	0.381	0.150	0.127	0.100
(c) Via center spacing	0.635	0.254	0.200	0.150
(d) Via cover dot to line clearance	0.254	0.127	0.075	0.050
(e) Line width	0.127	0.100	0.075	0.050
(f) Line to line clearance	0.127	0.100	0.075	0.050
(g) Via cover dot dia (on plane)	0.381	0.150	0.127	0.100
(h) Line width (on plane)	0.200	0.100	0.075	0.050
(i) Clearance dia	0.990	0.455	0.280	0.200
(j) Via pitch (on plane)	1.120	0.560	0.356	0.254
(k) Layer thickness	0.05–0.55	0.05–0.20	0.05–0.15	0.10

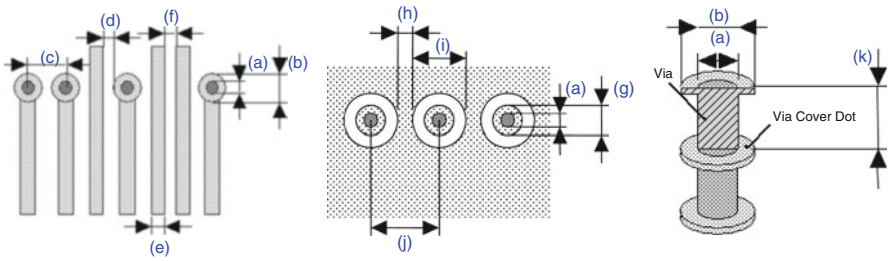

Fig. 7.86 Design element. Courtesy of KYOCERA Corporation

Table 7.7 Material properties, courtesy of KYOCERA Corporation

		Electrical				Thermal		Mechanical		
		Dielectric constant		Dissipation factor (×10E−4)						
Ceramic material options		1 MHz	2 GHz	1 MHz	2 GHz	CTE (ppm/K) (RT-400 °C)	Thermal conductivity (W/mK)	Flexural strength (MPa)	Young's modulus of elasticity (GPa)	Conductor material
Alumina (Al_2O_3)	A473	9.1	8.5	5	10	6.9	18	400	270	W, Mo
	A440	9.8	–	24	–	7.1	14	400	310	W, Mo
	A443	9.6	–	5	–	6.9	18	460	310	W, Mo
	AO600	9.0	8.8	10	21	7.2	15	400	260	CuW
	AO700	9.4	9.2	6	6	7.2	21	620	315	Mo
AlN	AN242	8.7	8.6	1	170	4.7	150	400	320	W
LTCC	GL940	–	18.7	–	2.5	10.7	3.5	220	188	Ag
	GL950	–	9.4	–	14	8.5	4.1	400	173	Ag
	GL330	7.8	7.7	4	5	8.2	4.3	400	178	Cu
	GL570	5.6	5.7	3	7	3.4	2.8	200	128	Cu
	GL771	5.3	5.2	8	36	12.3	2.0	170	74	Cu

Table 7.8 JEITA roadmap, substrate line/space (unit: μm)

Item	Class	2010	2012	2014	2016	2018	2020
Minimum width	A	15	12	10	7	7	7
	B	12	7	7	5	5	5
	C	7	5	5	3	3	3
Tolerance for width	A	±5	±4	±3	±3	±2	±2
	B	±3	±2	±2	±2	±2	±2
	C	±2	±1	±1	±1	±1	±1
Minimum space	A	15	13	10	8	8	8
	B	13	8	8	5	5	5
	C	8	5	5	3	3	3

Table 7.9 JEITA, hole and land diameter, pitch (unit: μm)

Item	Class	2010	2012	2014	2016	2018	2020
Mechanical drill min. hole diameter	A	100	100	100	75	75	75
	B	100	100	75	75	75	75
	C	75	75	75	50	50	50
Mechanical drill min. land diameter	A	220	205	205	180	180	180
	B	200	200	180	160	160	160
	C	140	140	120	120	120	120
Mechanical drill min. hole pitch	A	305	285	280	270	270	260
	B	225	215	210	205	200	190
	C	190	175	175	155	150	145
Laser drill min. hole diameter	A	100	75	75	75	50	50
	B	50	50	50	50	30	30
	C	50	50	50	30	30	30
Laser drill min. land diameter	A	200	180	170	160	150	150
	B	120	120	110	110	90	90
	C	100	100	90	80	80	80
Laser drill min. hole pitch	A	305	285	270	240	240	240
	B	185	175	160	155	140	140
	C	150	135	120	115	105	105

end like FPGA. In the substrate section, roadmap items are T_g, ε, tan δ, CTE x–y, CTE z, warpage, minimum line/space, minimum PTH minimum via/land, etc.

Table 7.8 is an example of the roadmap and describes a roadmap for a build-up substrate wiring line width and space. Shaded area is defined as "No solution in a current development scope." Table 7.9 is an example of the roadmap for hole parameters on a rigid substrate.

Table 7.10 Substrate related parameters in ITRS

Parameter	Year of production								
	2009	2010	2012	2014	2016	2018	2020	2022	2024
Chip to substrate interconnect land pitch (μm)	150	135	110	100	100	95	95	95	95
Min. finished substrate thickness (mm)	1.1	1.1	1.1	1.1	1.1	0.8	0.8	0.6	0.6
Min. line width/space (μm)	18/18	15/15	12/10	10/10	8/8	5/5	3/3	2/2	1/1
Min. conductor thickness (μm)	25	25	20	15	12	10	5	4	3
Min. through via diameter (μm)	100	100	80	80	70	70	70	60	60
Min. through via land diameter (μm)	250	250	200	200	150	150	150	120	120
Min. micro via diameter (μm)	60	60	60	50	50	30	30	20	20
Min. micro via land diameter (μm)	150	130	120	100	100	70	70	70	70
Min. through via pitch (μm)	300	300	275	275	275	250	250	250	250
Min. solder mask opening (μm)	80	80	60	60	50	50	40	30	30
Min. solder mask opening tolerance (μm)	20	20	18	18	15	15	10	8	8

7.7.2 ITRS

In ITRS (International Technology Roadmap for Semiconductor), there is an Assembly & Packaging chapter. Within the chapter, substrate related parts are sectioned application range as Low Cost (PBGAs), Handheld (FBGA), Mobile Products (SiP, PoP), Cost performance (CPU, GPU, Game Processor), High Performance (High End), and High Performance (LTCC). Table 7.10 describes a roadmap of dimensional parameters for Cost performance (CPU, GPU, Game Processor) as an example with relating to one of JEITA. Other than dimensional parameters, T_g, CTE (X–Y), CTE (Z), Dk@1 GHz, Df@1 GHz, Young's modulus, and water absorption for core material and build-up material are listed. ITRS roadmap is open in WEB.

In parameters, there is a minimum micro-via diameter that is 60 μm in these years. In fact, a micro-via hole diameter for processors of PC and game machines that are primary drivers of application of organic substrate has not been changed actually before year 2000 due to a technical fear in the reliability as previously described in this chapter. It means that a design ground rule of organic substrate has not progressed more than a decade because a true wiring capability of substrate is dominated by via hole density in a unit area. Fabricating a finer pitch line is rather easier compared with

reducing a via hole diameter. Technical establishment for a smaller via diameter has to be achieved for advancement of an organic substrate technology.

7.8 Summary

Flip chip is a superior technology in terms of performance, manufacturability, size and cost with scaling. Substrate material has been innovated from ceramic to organic. By the reduction of cost, applications are widely spreading in any part of electronic products today and will be growing in future. Yet, because of the high performance and density, one has to follow a sound engineering work to achieve its original advantages. In this chapter, it is tried to emphasize its growing element of technologies and applications, and, at the same time, basic technologies and backgrounds as well.

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