Chapter 2
Technology Trends: Past, Present, and Future

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Abstract Since the invention of flip chip technology by IBM about 40 years ago, there has been a continuous need for increased I/O density. More recently fine pitch technology is being enabled in Pb-free through Cu pillar and Sn–Ag solders. Stiffer Pb-free interconnection coupled with fragile low-k dielectric materials imposes a significant challenge on first level packaging. In response to increased number of interconnections and higher performance needs, additional technologies are emerging, such as the following: fine pitch flip chip (<60 μm pitch) interconnections, 3D with and without TSV's, liquid phase connections, and bond-on line. This introductory chapter covers these technologies and sets the stage for current and future flip chip technologies discussed throughout the book.

2.1 Evolution of Flip Chip Technologies in Response to IC and System Technology Trends

Flip Chip through solder connection between the semiconductor chip and the first level package using controlled chip collapsed connection (C4) was invented by IBM and it has been practiced at for more than 40 years [1]. In 1970, IBM started evaporating the UBM and the C4 Solder through a metal mask (Fig. 2.1). This process has evolved to finer and finer pitch utilizing a variety of solder deposition methods. Figure 2.2 depicts the various elements for the traditional first level packages. The first level package function is to redistribute the wiring to the printed wiring board (PWB) pitch while maintaining electrical signal integrity, and to provide a cooling platform for high-end ASICs applications. Flip chips were

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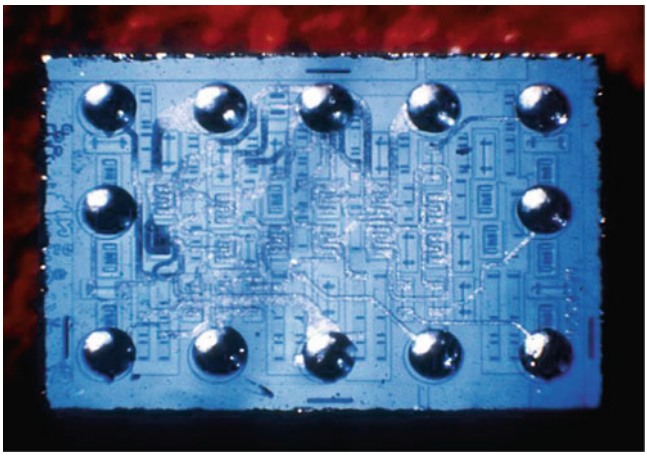

Fig. 2.1 High Lead solder on an IC (IBM, 1970)

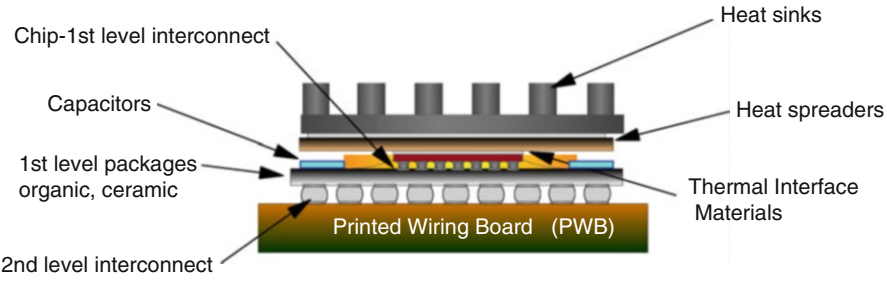

Fig. 2.2 First level package elements

initially joined mainly to ceramic substrates utilizing leaded solders. The introduction of surface laminar circuit (SLC) enabled the organic carriers to increase the wiring density and pitch making it the preferred chip carrier [2]. Low cost organic laminates are the main substrate base for single chip and dual chip modules.

A change from high Pb solders to eutectic solder (Pb63 %Sn) allowed the low temperature joining needed to implement flip chip on organic laminate carriers. However, to maintain mechanical and electromigration (EM) reliability, the usage of high Pb solders continues on the chip side while eutectic is selected for the laminate. Capacitors were subsequently added to either the top or bottom surface of the organic laminate. Underfills are applied after chip joining, and before module test.

The miniaturization in the chip ground rules has resulted in an increase of electrical resistance and the need for innovative thermal solutions to dissipate the heat. High-end processors utilize a thermal interface material (TIM), heat spreaders, and a heat sink. Junction temperatures of ~85 °C are now common.

The second level packaging refers to the module connecting to the PWB. It is here, at the board level, that all the peripheral are connected resulting in a final product.

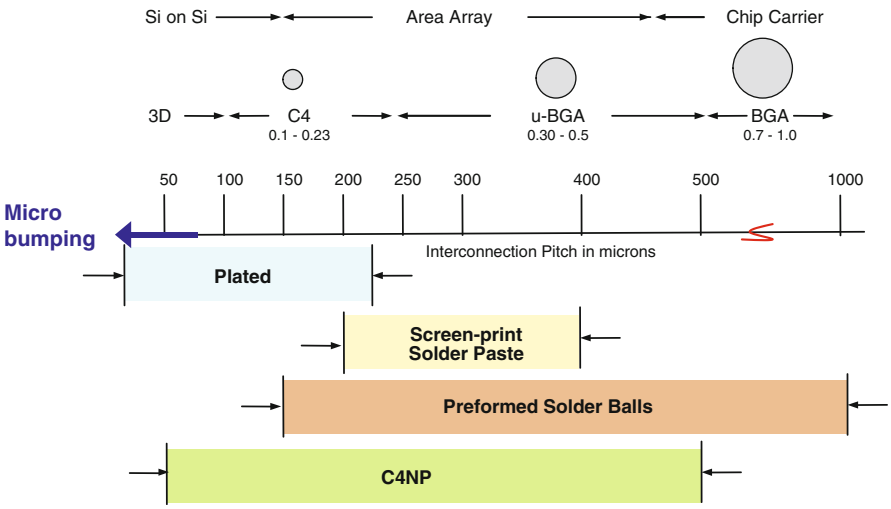

Fig. 2.3 Solder application for flip chip and module joining in first level packages

3D technology, as it will be discussed later, is enabling more and more peripherals to migrate to the chips and/or modules. Organic chip carriers are attached to the PWB through a solder connection, but at a much larger pitch, referred to as the Ball Grid array or BGA. The BGA pitch has been maintained around 1 mm but laminate technology improvements have driven the BGA pitch to 0.8 mm pitch and lower on advance products. A typical C4 will see at least four reflows: Initial solder attach, post test reflow (optional), C4 to laminate joining, BGA attach and BGA joining to PWB.

Wire bonding has been the lower cost technology for connecting the chips directly to the PWB. Its main limitation is that all the connections are through the chip perimeter, requiring a larger-than-chip area on the PWB surface. As the number of interconnection increased, more rows of wires are needed surrounding the chip.

Wafer level chip scale packages (WL-CSP) rearrange, through redistribution and solder connections, all the wire bond connections to an area array, thereby utilizing only the chip area on the PWB surface. The WL-CSP solder pitch is between 0.3 and 0.5 mm, with underfill as an option depending on the chip size and the component reliability requirements. Initially, eutectic Pb–Sn solder joints were used, but now Pb-free solder connections are the norm. There are multiple processes to deposit solders for area array connection. Figure 2.3 depicts solder deposition method base on the required interconnection pitch. Table 2.1 shows the four main technologies used for depositing solder. For completeness the table also include: anisotropic conductive adhesives (ACA), laser ball bump and Au Stud bumping.

The lowest cost deposition method is solder screening, but due to the large solder particle range, its coplanarity is poor, particularly at <200 μm pitch. Process improvements in solder screening volume control include changes in the screen mask (from a reusable metal mask to a disposable photo mask), and in a reduction of the solder particles grid size. Solder screening is the preferred method for

Table 2.1 Types and applications of Flip Chip joining-Test: Probers, testers, interfaces/hardware, etc.

	Applications	UBM required	Composition flexibility	High # of C4s	Volume control	Flux required	Propensity for voids	Underfill required
Ball drop	BGA and CSP	Y	Y	N	Y	Y	Y	Y
Laser ball bump	Sensors	Y	Y	N	Y	N	N	Y
Solder screening	PWB components	Y	Y	Y	N	N	Y	Y
C4NP	Flip chip, 3D	Y	Y	Y	Y	N	N	Y
Plating	Flip chip, 3D	Integrated	N	Y	Y	Y	N	Y
Au stud bump	Sensors	N	N	N	Y	N	N	N
ACA	Displays	Y	Y	Y	N	N	Y	N

depositing solder on to the laminate surface. When very large solder connections are needed, ball drop is the preferred method. As with Ball drop and solder paste, C4NP (developed by IBM in collaboration with Suss Microsystems) can deliver unique solder compositions with more than two metals [3].

2.2 Evolution of First Level Packaging

A series of technical challenges surfacing simultaneously are influencing the materials and process selection for the first level interconnection, i.e., increased power and thermal dissipation requirements, architectural shift to multi-cores giving increased I/O count and current density, and increased interconnection density.

2.2.1 Thermal Demands

Bipolar technology was the main semiconductor technology in the 1980s. In 1990, IBM ES9000 server system using bipolar technology required water cooling to support the ~13 W/cm^2 module heat flux (Fig. 2.4) [4]. With the movement to CMOS technology, the cooling requirements were reduced significantly. CMOS integration enabled full function integration into a single chip. However, as the semiconductor scaling continued, the current leakage generated by the increased wiring length and density (passive power) has increased exponentially and now, it has surpassed the active power in some high-end processors (Fig. 2.5) [5].

The increased power is affecting both thermal management and power delivery. The high junction temperatures coupled with the Joule heating in organic carriers is giving rise to EM concern for first and second interconnect levels, particularly in Sn-based Pb-free systems.

2.2.2 Increased Chip Size

The increase of bandwidth has resulted in an increase of I/O count requirements which in turn have decreased the solder pitch, from 200 to 150 μm. In addition, the chip size is increasing significantly to accommodate increase in functionality. A 20 × 20 mm chip size could be a common occurrence for high performance applications in the near future.

As chip size increased, underfill was introduced to compensate for the thermal mismatch between the Si die and organic carrier, enabling larger chips which otherwise would have failed thermal cycle testing. Organic laminates have a high coefficient of thermal expansion (CTE) of about 18 ppm compared to the 3 ppm of the Si chip. The underfill also protects the solder from corrosive environment.

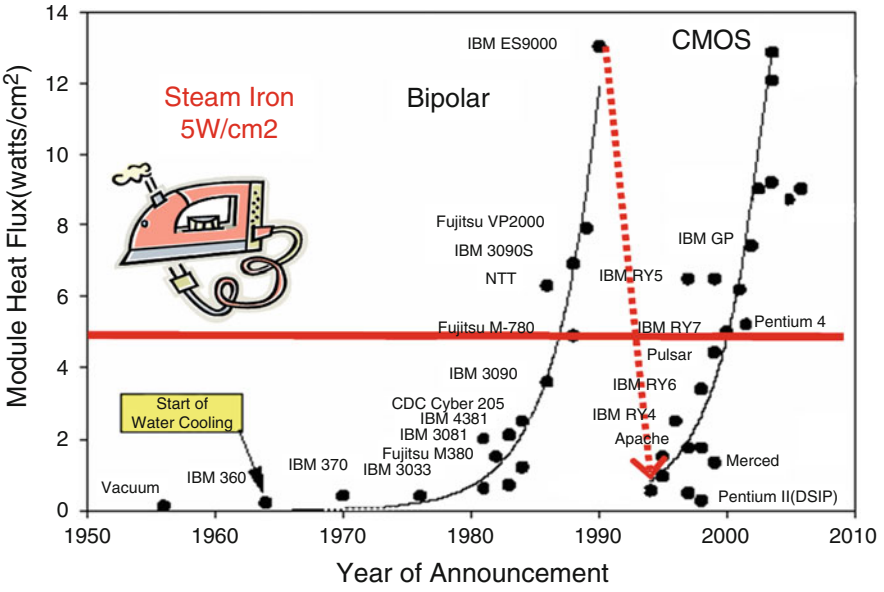

Fig. 2.4 Evolution of heat flux per module as a function of time

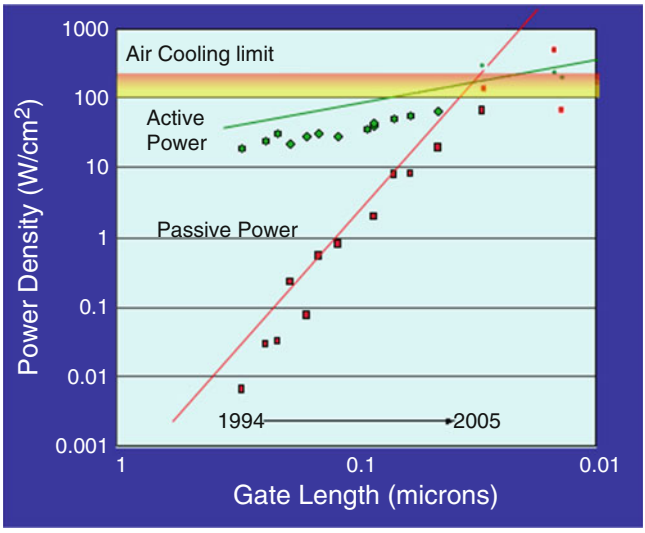

Fig. 2.5 Active and passive power effects as a consequence of scaling

A module sonoscan can confirm a void-free underfill, or crack-free chip corner. Underfills are available with a variety of CTE, Tg and modulus properties, which can be optimized for a particular application. These underfill properties are interrelated since CTE is controlled by the quantity of fillers which affects the material modulus.

2.2.3 Restriction of Hazardous Substances

The green compliance is managed by control of Hazardous Substances and Halogens in electrical or electronic products. RoHS [6], *Restriction of Hazardous Substances*, originated in the European Union in 2002, restricts the use of lead, mercury, cadmium, hexavalent chromium, and PBB's (polybrominated biphenyls) or PBDE's (polybrominated diphenyl ethers) as fire retardant, in new electrical or electronic equipments entered into force in February 2003. These directives came with provisions to exempt certain uses of otherwise restricted substances in specific cases where the negative effects were likely to outweigh the environmental, health, and/or consumer safety benefits of the substitution and requirements to review every 4 years to determine whether there is valid scientific data to support the continuation of each exemption. These restrictions and exemptions have been applicable since July 1, 2006. Following decision tree can be used determine if an electrical or electronic equipment is a subject of RoHS Directive (Fig. 2.6) [7].

Lead in solders for Flip Chip applications is the primary concern in electrical and electronic equipments since they are not expect to exceed the threshold of 1,000 ppm for mercury, hexavalent chromium, PBB, and PBDE and 100 ppm for cadmium.

Lead solder related exemptions include (4 year review cycle, next review in 2012)

- Spare parts for the repair of equipment that had been put on the market before 1 July 2006 and the equipment that was put on the market before the same date.
- Lead in high melting temperature solders (i.e., tin–lead solder alloys containing more than 85 % by weight or more lead)
- Lead in solders for server, storage and storage array systems, network infrastructure equipment for switching, signaling, transmission as well as network management for telecommunications
- Lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit Flip Chip packages.
- Expiration dates for the above exemptions are expected to range from 2013 until July, 2014 with no grandfather clause, although "repair as produced" is expected to be approved for upgrades and field repairs.

High melting temperature solders containing >85 % lead are often used for high reliability flip chip bumps, some soldering processes for ceramic packages, and die attach for high power, wire bonded devices. Current flip chip interconnections using Pb–*X*% Sn ($X < 15$) with ceramic substrates and using Pb–3 %Sn with Pb–67 %Sn solder on organic laminate meet the criterion of exemption from RoHS [8]. However, all BGAs have transition to Pb-free solders.

Lead bearing solders have been the primary alloys for the assembly processes used within electronic equipment for decades. The quest to replace these solders with lead-free alloys is a tremendous task that has been undertaken by the electronics industry. It was recognized that to require this transition to lead-free solders prematurely in high performance, high reliability electronic equipment such as servers, storage, storage arrays, network infrastructure and telecommunications equipment that perform critical tasks could pose a health and safety risk to the public. These systems are

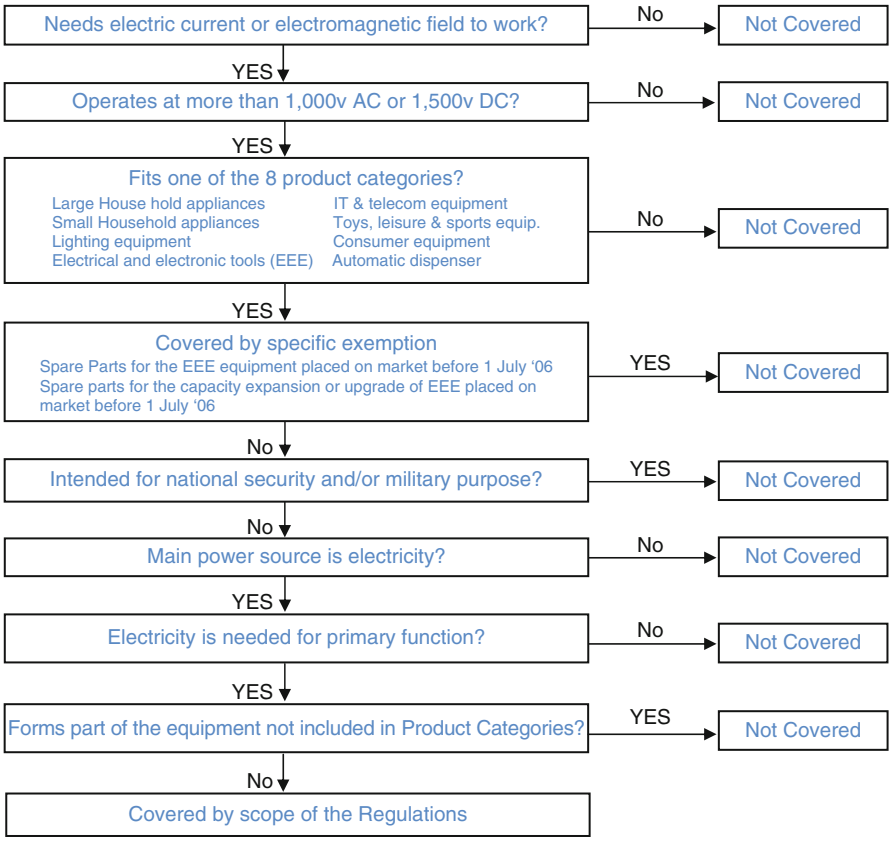

Fig. 2.6 Decision Tree for RoHS Pb-free regulations

expected to be in operation 24 hours a day, 7 days a week for at least 10 years with very little outage time during these years of operation. Until Pb-free solders could be proven as reliable for such high performance, high reliability applications, the need for the continued use of traditional lead–tin solder has been argued [8].

Two concerns have been identified as primary focus for development of Pb-free solder for flip chip interconnection; first, lack of adequate resistance to EM under severe operating conditions and second, compatibility with the fragile back end of line structure of the device. These two topics will be covered in detail in subsequent chapters.

2.2.4 Compliance Cost, and Future RoHS Directive

Initial compliance is estimated to have cost industry $32 billion, with a further $3 billion needed annually to maintain compliance, according to a study by

Technology Forecasters Inc (TFI) [9]. The Commissions own study puts the average overall cost related to RoHS at 1.9 % of the turnover. TFI survey also revealed 29 % companies lost sales due to RoHS (average loss US$1.84 million), 2/3 of these came from delayed new product or discontinued EU sales. In an attempt to reduce costs, resolve uncertainties increase market surveillance and enforcement, the European Commission revised the RoHS Directive in December 2008—with the objective "to develop a better regulatory environment, one that is simple, understandable, effective and enforceable."

The other component of green compliance comes from control of halogens, primarily bromine bearing compounds, such as PBB's, PBDE's, and TBBA's (Tetrabromobisphenol) used as fire retardants in a plastic package. In electronic products, thermoplastics, which include polycarbonate, acrylonitrilebutadien-styrene copolymer, and polystyrene, are mainly used in housings. Furthermore, thermosetting plastics—mainly epoxy resin compounds consisting of epoxyresin, hardener, and additives—are used as insulating materials for electronic parts.

In order to prevent fire from originating in electronic products, these plastics contain flame-retarding additives, most commonly in the form of organic halogen compounds such as brominated aromatic compounds. There is, however, a serious problem with such halogen compounds; as during burning they generate toxic substances that can injure people and contaminate the environment. In addition to the fire-related dangers, the treatment and recycling of the waste materials is also made extremely difficult.

The acute toxicity of the majority of the brominated flame retardants is low or very low. This is also the case for many of the breakdown products. The important risks of brominated flame retardants are therefore mainly connected to long-term effect; only relevant if the substance or its breakdown products may bioaccumulate. A substance that is fat soluble and stable, and that has a route of exposure to a specific organism may bioaccumulate. The third draft of the European Parliament and Council Directive on Waste Electrical and electronic Equipment, presented in 1999, required that member states phase out the use of PBBs and PBDEs by January 1, 2004.

Environmentally friendly flame-retardant plastics containing no toxic flame retarding additives such as halogen (bromine) compounds and phosphorus compounds have been developed for electronic products [10]. A polycarbonate resin containing a new silicone flame-retarding additive has been developed for use in housings. Furthermore, a self-extinguishing epoxy resin compound containing no flame-retarding additives was developed as a high-quality molding resin for electronic parts. These plastics show good general properties as well as high flame retardation [11].

2.2.5 Choice of Sn

Sn–Ag–Cu with a liquidus temperature of about 220 °C for the eutectic composition has been the solder composition of choice for most of Pb-free device applications.

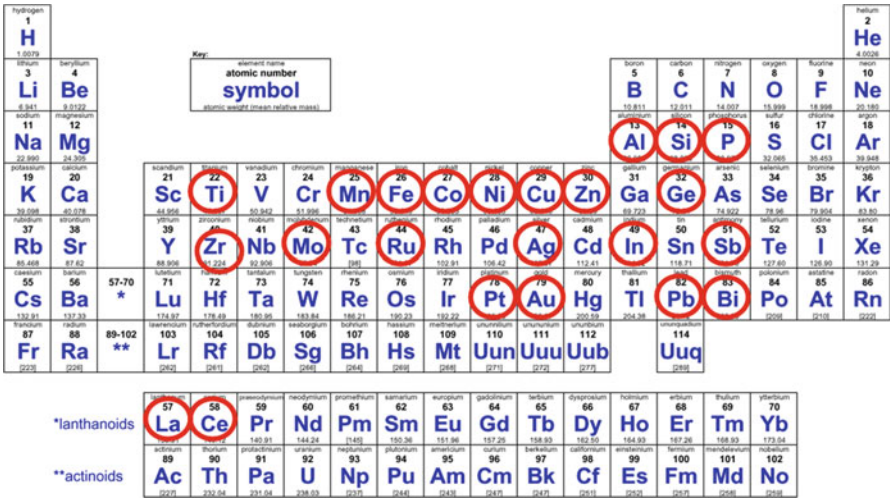

Fig. 2.7 Pb-free solder additive elements for specific applications

The individual composition is dependent on the design factors for a specific application. They include liquidus temperature, elimination of formation of rod-like Ag_3Sn precipitate, reduction in suppression of solidus, relatively low hardness, low undercooling and longer life expectation from the point of EM behavior. Pb-free solder composition effects on undercooling have been reported earlier for a BGA solder [12].

The precipitation of rod-like Ag_3Sn phase during chip-joining process has been observed in alloy containing as low as 2.3 %Ag. The ability of the solder to permit stress relaxation is measured in terms of its microhardness. J. Sylvestre of IBM studied various Sn <2.3 %Ag alloys joined to the laminates with Sn–0.7 %Cu or SAC 305, creating gradation of Ag compositions, and examined suppression of solidus and micro-hardness. Solder joint micro-hardness deceases as the percent of Ag in the interconnected bump deceases. This improvement on stress relaxation also resulted in a decrease in ultralow k dielectric delamination [13].

The quest for improved solder properties in a Sn-based system has resulted in an evaluation of many solder additives. Figure 2.7 shows many of the additives which have been reported in the literature. However, since pattern electroplating is the deposition method of choice for $\leq$150 μm pitch, solder additives are mainly of academic interest for fine pitch flip chip applications.

Finally, Sn Pest is another concern on Sn-based solders. It occurs when by β-Sn phase transforms to the α-phase, and has been reported at −18 and −40 °C requiring several years [14]. The α-Sn is readily crumbled and destroys the mechanical integrity of the solder joint. Sn pest has been observed in Sn–0.5Cu, Sn–3.5Ag, Sn–3.8Ag–0.7Cu, and Sn–3.0Ag–0.5Cu solders [14].

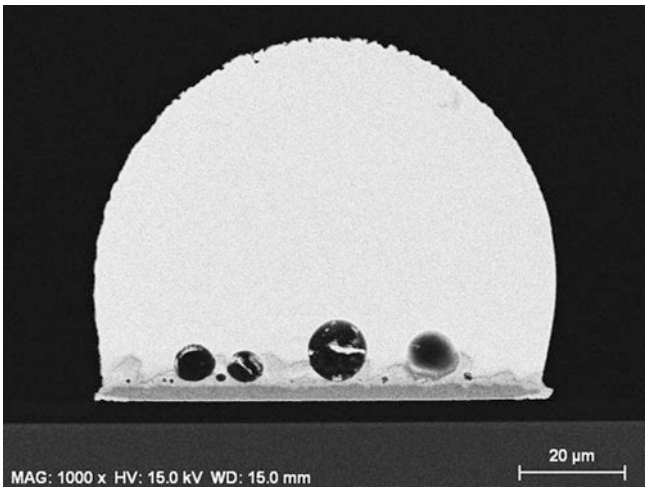

Fig. 2.8 Voids in a plated solder after reflow

2.2.6 Solder Void

Solder voids can be categorized in micro (0.1–1.0 µm) and macro (1–20 µm) scales. The macro voids are a result of entrapment of flux (for solder paste or ball drop) or plated volatiles (on electroplated solders). Figure 2.8 shows an example of a plated solder which was reflowed upside down, resulting in volatile entrapment at the UBM—solder interface.

Kirkendall voids are small voids which form during thermal aging. They start as microvoids within the Cu_3Sn IMC or at the Cu—Cu_3Sn interface when Cu is top layer of UBM, such as Cu OSP in the organic laminate. The Kirkendall voids formation results from a vacancy migration during inter-diffusion when the Cu in UBM and the Cu_3Sn reacts to form Cu_6Sn_5, with no Sn available from the bulk solder. As thermal aging continues, the small voids coalesce to form a crack [15]. Much has been written about Kirkendall voids, but reproduction of results does not always occur, indicating sensitivity to the Cu plated chemistry or Cu deposition parameters [16].

2.2.7 Soft Error and Alpha Emission

A soft error is a signal or datum which is wrong. After observing a soft error, there is no implication that the system is any less reliable than before. Soft error rate (SER) is the rate at which a device or system encounters or is predicted to encounter soft errors. It is typically expressed as either number of failures-in-time (FIT), or

mean-time-between-failures (MTBF). The unit adopted for quantifying failures in time is called FIT, equivalent to 1 error per billion hours of device operation. MTBF is usually given in years of device operation. To put it in perspective, 1 year MTBF is equal to approximately 114,077 FIT. Soft error can be caused by Alpha particles from package decay, Cosmic rays creating energetic neutrons and protons, and thermal neutrons. The mitigation of soft errors caused alpha particle emission of lead containing solder is of extreme importance to the electronic industry.

To give an overview, the problem with ^{210}Pb in solder is that it comes from the radioactive decay of ^{210}Po, which releases an energetic alpha particle (helium nucleus). Although it is easy to remove the ^{210}Po from the solder, the radioisotope ^{210}Pb will decay with a half life of 22.3 years to ^{210}Bi, which, in turn, decays with a half life of 5 days back to ^{210}Po. This point, where ^{210}Po is being replaced at about the same rate that it decays, is called "secular equilibrium" and is reached approximately in 2 years since refinement. Low alpha lead can be obtained from several sources, including "cold" lead ore, laser isotope separation process, and antiquity lead. Alpha emission rate is measured in terms of counts per centimeter square per hour. Lead-rich-solders with alpha emission rate of 0.02 per cm^2 per hour are commercially available for high-end-applications. Lead-free solders have alpha-emission due to trace impurities of Pb or Bi. Tin based Lead-free-solders with alpha emission rate of 0.002 per cm^2 per hour are commercially available for ultrahigh-end-applications. This level of alpha-emission presents challenges to reliable alpha-emission measurement technique, namely, stability of background, sample preparation, sample storage, measurement time, and sample size [17].

2.3 First Level Packaging Challenges

2.3.1 Weaker BEOL Structures

Semiconductor industry's continuous drive towards faster chips and smaller wiring has resulted in an increased capacitance and which drives need for insulators with lower dielectric constant. This is, generally, accompanied with reducing the insulator fracture toughness. Interconnect stress build-up during the cooling part of chip join cycle, due to the CTE mismatch between the device and the organic carrier coupled with the move to Pb-free solder, and increased solder hardness, can exceed device BEOL structure strength for specific design structures, resulting in interlayer delamination or cracking, see Fig. 2.9. The packaging trends, shown in Fig. 2.10, impose new restrictions on Pb-free systems. System optimization is needed to eliminate the stress cracks which occur during the cooling stage at the first chip joining [19]. Increase in polyimide thickness, acting as a cushion, and increase in thickness of interconnect metal Cu, are some of the variables used for increasing robustness of the BEOL Structure.

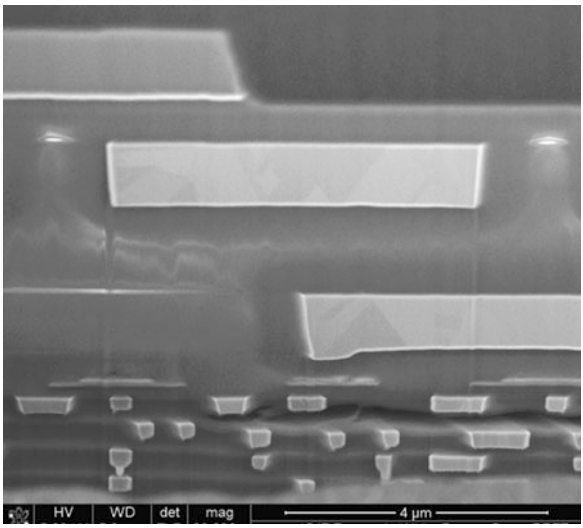

Fig. 2.9 X-section of ULK delamination

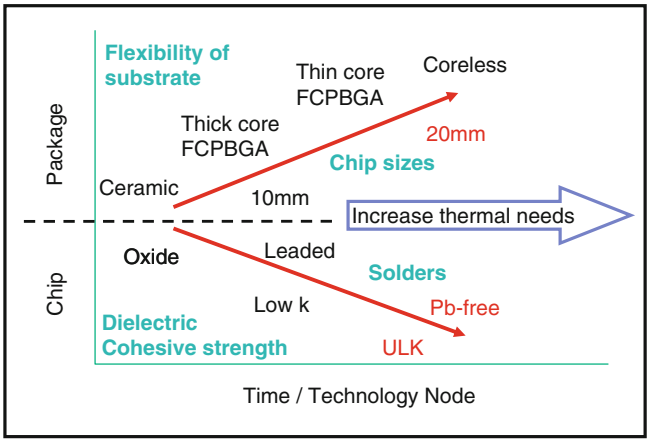

Fig. 2.10 Chip and package trends

2.3.2 C4 Electromigration

The EM performance of Pb-free interconnect has been the focus of recent studies due to the continuing demand for higher current density and circuit miniaturization. Different from the face center cubic structure of lead, tin (Sn) has a tetragonal crystal structure and tends to form large grains that exhibit highly anisotropic behavior in mechanical, thermal, electrical, and diffusion properties in the high Sn-based Pb-free

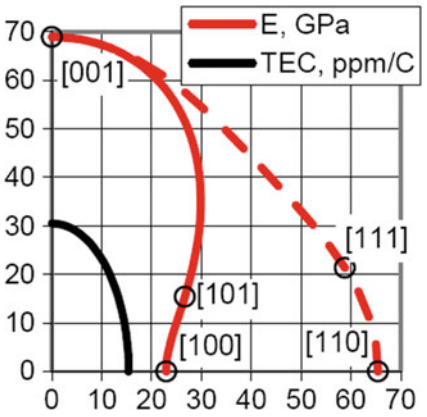

Fig. 2.11 Anisotropic elastic modulus and thermal coefficient of expansion on β-Sn at room temperature [18]

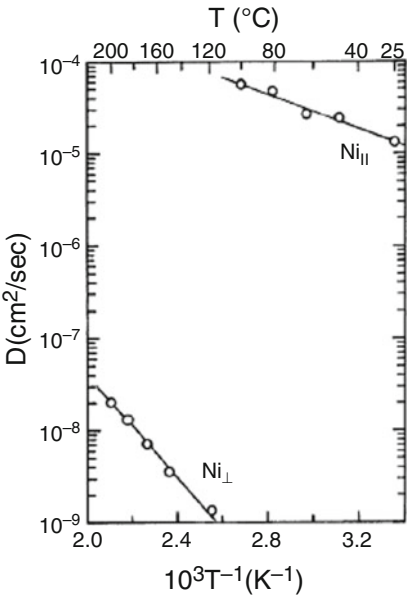

Fig. 2.12 Diffusion of Ni in Sn [20]

solder joint (see Fig. 2.11). Importantly, the noble and near noble metals are extremely fast diffusers in Sn and the diffusivity is highly anisotropic. For instance, the diffusivity of Ni along the tetragonal (*c*-) axis is ~7 × 10E4 times faster than that at right angles (*a*- or *b*-axis) at 120 °C (see Fig. 2.12). Experimentally it has been found that EM damage is strongly dependent on the Sn-grain orientation in Pb-free solders [21]. Figure 2.13 shows a SEM image of an EM stressed C4 with SnCu solder and the insertion of the Sn unit cell indicating the grain orientation. The grain on the right has the *c*-axis at nearly a right angle with respect to the current direction, where the rates of Cu and Ni diffusion in Sn are slow. Failure is characterized by Sn self-diffusion or lattice diffusion resulting in void formation between the IMC and solder,

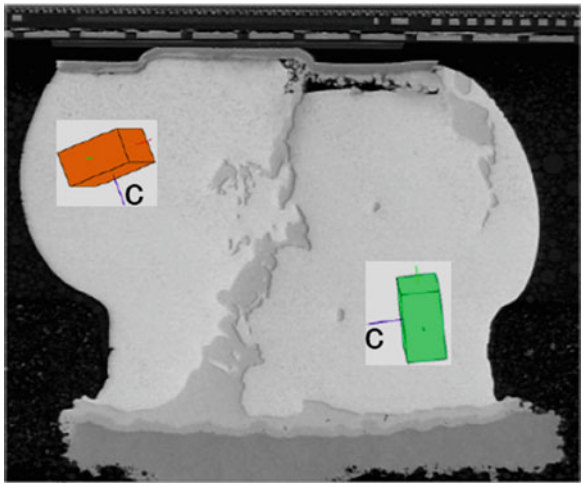

Fig. 2.13 SEM of an EM stressed C4 with SnCu solder failure. Courtesy of Minhua Lu of IBM Corp

referred to as mode-I failure [21]. The grain on the left, however, has its *c*-axis closely aligned with the current direction, which drives very fast Ni and Cu diffusion through the Sn grain. Mode-II failure is due to rapid depletion of intermetallic compounds and UBM. Since Mode-II failure usually occurs early, it is the mode which should be avoided.

In addition to the grain orientation, the solder and UBM interaction and solder alloy composition play an important role as well. Minhua Lu of IBM has reported the average time to failure for SnCu and SnAg(Cu) solders and three UBMs; Cu, Ni(P)/Au, Ni(P)/Cu surface finishes [22]. In general SnAg(Cu) solder performs better than SnCu solders and Ni UBMs are better than Cu UBMs. This study showed that Ag_3Sn intermetallic network is more stable than that of the Cu_6Sn_5 network under thermal and electrical stress, which is attributed to the much smaller diffusivity of Ag compared to Cu. Grain growth and grain reorientation is common in SnCu solder, while a much more stable cyclic twinning structure is more frequently found in SnAg solders, especially in high Ag solders. Although Cu_6Sn_5 is not stable against EM, this study shows that a certain amount of Cu on UBM to form a layer a Cu_6Sn_5 IMC after reflow is important to give an extra protection to Ni barrier layer. Effect of alloy composition such as Ag, Cu and other doping elements and UBM metallurgy on EM is complicated and convoluted.

2.3.3 Cu Pillar Technology

The Cu pillar technology adopted by Intel provides a uniform current distribution in the positive direction (current flowing from the chip to the package) where peak current has traditionally been a concern. The Cu pillar along with the lower volume

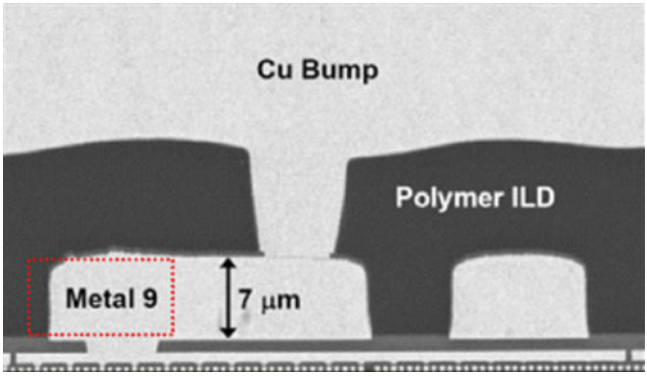

Fig. 2.14 Intel F-BEOL modifications for Cu Pillar technology

Pb-free solder results in a stiffer interconnect which requires a F-BEOL redesign involving three key elements: a 50+ μm of Cu pillar, a thick organic dielectric with a small via diameter, and a M9 metal (8 μm thick in the latest design) for better power distribution (See Fig. 2.14) [23]. Intel has selected not to put solder on the chip side, with all the solder being provided by the laminate side. This requires thicker and uniform solder on the laminate side. So far the implementation of the Cu pillar for leaded and lead-free solders has been limited to less than 15 mm chip size. The short distance between Cu pillar and laminate may improve EM as it approaches the Blech limit.

2.4 IC Technology Roadmaps: More Moore and More Than Moore

At the other end of the spectrum are portable devices, where main considerations are weight, size and cost. Portables mainly encompass handheld devices, such as smart phones, cameras, etc. It is these handheld devices that are driving the packaging innovation, such as WL-CSP (Fig. 2.15), wafer thinning, overmold, etc.

Gordon Moore postulated in 1965 that the semiconductor cost/performance ratio doubles every 18 months, now referred to as the Moore's Law [24]. For the next 40 years this trend was roughly maintained in great part due to the rapid scaling and miniaturization of the semiconductors pitch which has moved from micron-scale to nanoscale while increasing the wafer size from 25 mm to a current 300 mm. The effect of large wafer size and nanoscale lithography has placed a high cost burden in the industry's ability to keep up with the Moore's Law. Currently, a new FAB can cost around $5 billion, and research and development cost have maintained a 10 % increase over the last 10 years. How can this rate of technology progress, which has fueled an electronic revolution, keep up?

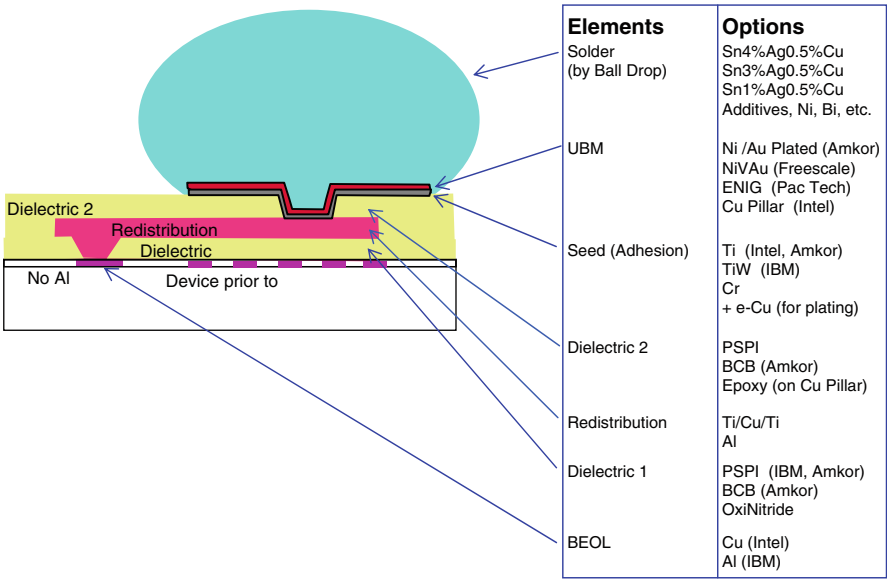

Fig. 2.15 Wafer Level Chip Scale Package elements

Research and Development consortiums are emerging as means to collaborate among companies while reducing the individual R&D costs. Both IBM and TSMC have formed joint development agreement with semiconductor FABs. Additionally, Sematech and SRC in the USA, IMEC in Europe, and ASAT in Japan, provide industry and university collaboration to train the workforce needed for future technology innovation. The European Union "Vision2020—Nanometrics at the Center for Change" is defining the path on how to become a global leader in nanoelectronics. Vision 2020 strategy is to integrate the supply chain with application side. ENIAC (the European Nanoelctronics Initiative Advisory Council), whose acronym was appropriately taken from the first multiple purpose general computer (Electronic Numerical Integrator And Computer), was created to define the means of achieving Vision 2020. ENIAC has proposed five key society areas for concentrated development focus: health, mobility, security, communications, and entertainment [25]. Technology drivers specific to these areas have been identified and grants are available for R&D.

"More Moore" refers to scaling specific technology advancements, in the device or associated structures, such as 3D. "More Than Moore (MtM)" is a new level of integration where non digital devices which were traditionally mounted to the printed-circuit wiring board (PWB) are migrated to package level. This reduction in distance also resulted in a reduction in passive power. Non digital devices such as RF, passive components, sensors and actuators, and power control have also reduced their dimensions, but not at the scale of semiconductor devices. Additionally, packaging improvements such as package on package (PoP), Multichip modules (MCM)

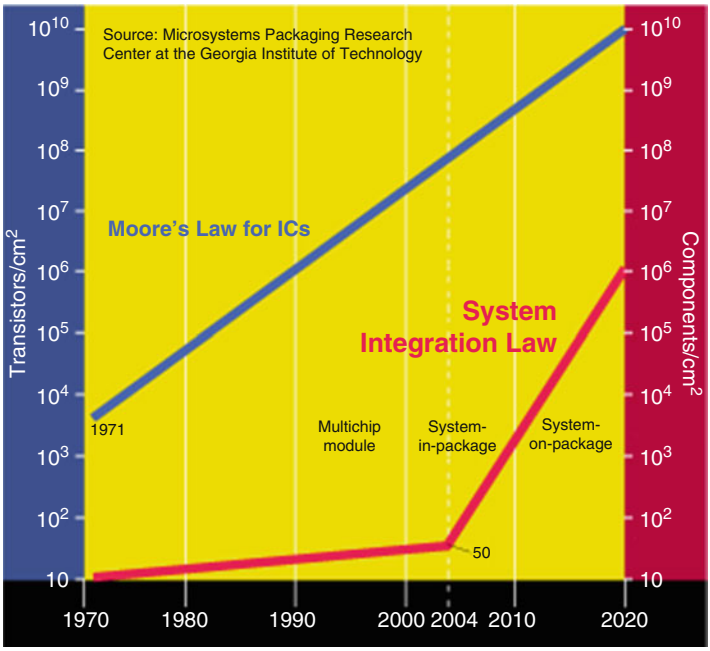

Fig. 2.16 Transistor evolution compared with the packaging integration

and system in package (SiP) have revolutionized system level interconnection. Figure 2.16 from Rao Tummala from GaTech University clearly depicts the effect of packaging integration in MtM, and the paradigm shift that it represents [26]. Packaging development focus is driven by the objective to reduce high module and assembly costs, when compared to the semiconductor devices.

The International Technology Roadmap for Semiconductors (ITRS) is a global organization that works diligently to provide semiconductor roadmaps, and more recently assembly and packaging roadmaps [27]. The ITRS has defined the "More Moore" applications to those where functional and performance scaling are enabled by both geometrical and equivalent scaling. Geometrical scaling refers to the vertical and horizontal shrinkage of features on the chip associated with speed and power advancements, while equivalent scaling refers to 3-dimensional device structures which complements geometrical scaling and enhances the electrical performance of the chip [27]. "More than Moore" integrates the More Moore innovations with the non-scaling technologies (such as analog/RF, passives, HV sensors, actuators and biochips) to produce high value system through functional diversification.

Heterogeneous integration, such as 3D or Multichip modules (vertical or horizontal connections), is providing the needed platform for new automobile, medical, aerospace and consumer applications which are emerging due to the lower costs and/or lower physical size. Software and application integrations are also contributing in improving cost/performance ratio.

Table 2.2 Ground rule evolution for the laminate technology

Item	Class	2006	2008	2010	2012	2014	2016
Min. line width (μm)	A	30	30	20	20	15	15
	B	20	15	15	7	7	7
	C	15	7	7	5	5	5
Min. space width (μm)	A	30	30	20	20	15	15
	B	20	15	15	7	7	7
	C	15	7	7	5	5	5
Land pad diameter for laser micro via (μm)	A	110	90	90	80	80	70
	B	90	70	60	60	50	50
	C	70	60	50	40	40	30

The non-digital devices integration in SiP and SoC applications started first with RF and passives components, followed closely by MEMS and Bio-devices, enabled by WL-CSP and embedded technologies. MEMS applications such as inductors, accelerometers and digital micro devices are being integrated within CMOS technology. By connecting the MEMS directly in the CMOS chip, thinner highly functional structures are achieved for applications such as Integrated RF, finger sensor, gyroscope, etc. [28].

2.4.1 Improvements in Laminate Ground Rules

As has been shown, the laminate technology is dominating the chip package industry, and with the assembly houses, it has enabled the WL-CSP revolution. The laminate technology improvements are not only in dimensional scaling as shown in Table 2.2, but it has been able to maintain the electrical parameters, such as impedance control, needed for high performance products [29]. The reduction in linewidth and in dielectric thickness are making the laminate substrate lighter, smaller and thinner, allowing for more function to be transfer in to the packages. One problem which the laminate substrate has is warpage control. Warpage occurs during the chip joining process affecting the laminate coplanarity. On large substrates, non-wetts or no C4 to laminate contact can result due to CTE mismatched coupled by the laminate warpage.

2.5 3D Flip Chip SiPs for Handhelds Require IC-Package-System Co-design

SIP refers to a semiconductor device that incorporates multiple components that make up a complete electronic system into a single package (Fig. 2.17). Electronic devices like mobile phones conventionally consist of several individually packaged IC's handling different functions, e.g., logic circuits for information processing, memory

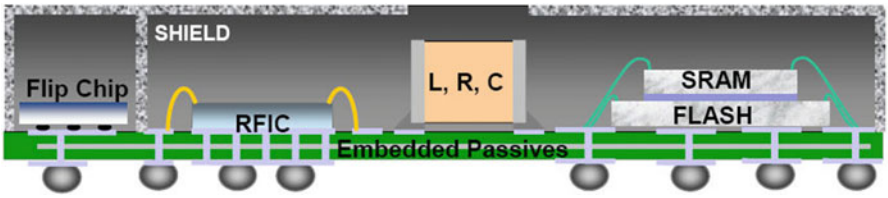

Fig. 2.17 SIP Concept; an Schematic SIP Package containing Chips, RFIC, passives (L, R, C), and memory [30]

for storing information, and I/O circuits for information exchange with the outside world. In a SIP all of these individual chips together with other devices like passives, filters, antennas are assembled into a single package using wirebond or/and, solder interconnect technologies, resulting into tremendous space savings and significant down-sizing of handheld wireless applications.

SIP is different from SoC or "System-on-a-Chip," which is a complete electronic system built on a single chip. SoC's suffer from long development cycle time, low yield, and high development costs; mainly because it is difficult to make an entire system of differently functioning circuit blocks work on a single chip. SoC's are generally, performance driven packages for specific applications such as medical or military. SiP technology, on the other hand, has proven to have lower cost, shorter development cycle, and unified solution to the system architect consisting of smaller system size, increased system density, and lower system power consumption.

SIP's are also designed using a 3D stacking of chips with following elements; thinned dies up to 40 μm thick, adhesive-with-silicon filled in between the chips and between the first chip and laminate, first chip may also be joined with underfill, wire bonding between the chips and flip chip between the first chip and carrier, low modulus mold compound encapsulating the wires, and organic carrier with ball grid array pitch >400 μm, (Fig. 2.18). H. Bottoms from ITRS has summarized classification for SIP structures, as shown in Fig. 2.19.

2.5.1 SIP Engineering Challenges and Co-design Tool

SIP's have engineering challenges like interaction among various stacked dies, variations of die stacking configurations, 3D nature of wirebonds, various configurations of bumps and balls, competing signaling architectures, heat dissipation, and test. Some of these engineering challenges can be addressed by a co-design tool encompassing design of various devices and the package. For example a co-design tool will create a design to address SIP heat dissipation and architecture testing in an economical and efficient way. The co-design tools enable package designers, package design service companies, and offshore assembly and test companies (OSAT) to participate in the multi-die SIP design chain using a

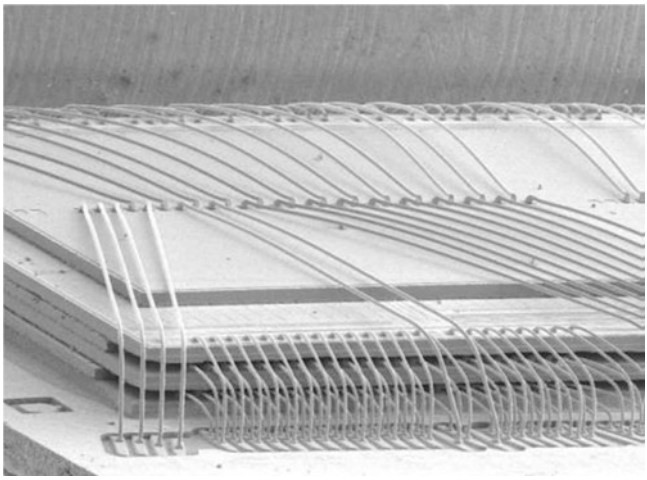

Fig. 2.18 Typical complexity of wire bond interconnections in a 3D chip stack [30]

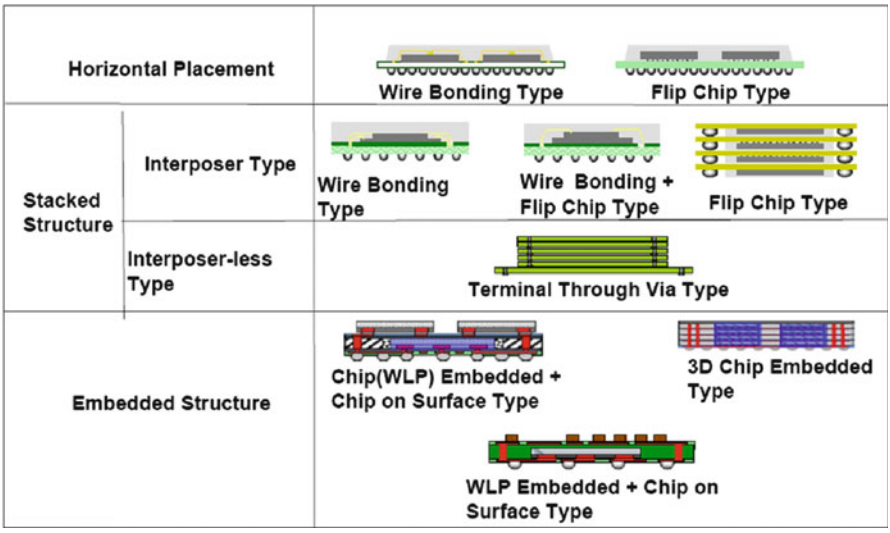

Fig. 2.19 Overview of SIP Categories [31]

co-design methodology. It enables data to be passed easily among design chain partners using co-design technology, such as Cadence [32].

For the test issues, open-architecture automated test equipment (OA-ATE) is considered a cost-effective solution that allows semiconductor manufacturers to specify their own test resource and instrumentation requirements. "Specialization" of test capability requires some standardized vital elements: for example an industry-standard bus structure, compatibility with industry-standard data formats, browser technology to access and control resources, a modular hardware and software

structure to enable re-configurability, and partitioned test supported by ATE and EDA tools.

SIP design allows manufacturers to bring together many IC, package assembly, and test technologies to create highly integrated products with optimized cost, size, and performance. EDA software suppliers provide advance technologies to help SIP design team members get control of the challenges, especially in the areas of co-design, advanced packaging, and RF module design. Successful implementation of SIP manufacturing offers many advantages that are important to the semiconductor industry of the future: shorter time-to-market, lower cost, flexibility, smaller size, etc.

2.6 PoP and Stacked Packages

PoP (Package-on-package) and PiP (Package in Package) technologies provide the least disruptive way to make 3D integrated micro-systems by vertically stacking fully tested prepackaged dies. Figure 2.20 depicts various PiP and PoP modules used in a cell phone application. Each individual package may have a different level of complexity. There are many versions of this 3D integration; wire-bonded-stack, perimeter BGA stack, or u-BGA through a laminate interposer (Fan-in PiP), flip chip C4's and a combination of these versions. One differentiation between PoP and PiP is that in a PoP the top and bottom packages are connected by BGA's, whereas in a PiP the top and bottom packages are connected by wirebond with or without using an interposer. Therefore laminate warpage can significantly affect the PoP connection yield [33]. Currently, 3D packages are widely used in many consumer portable

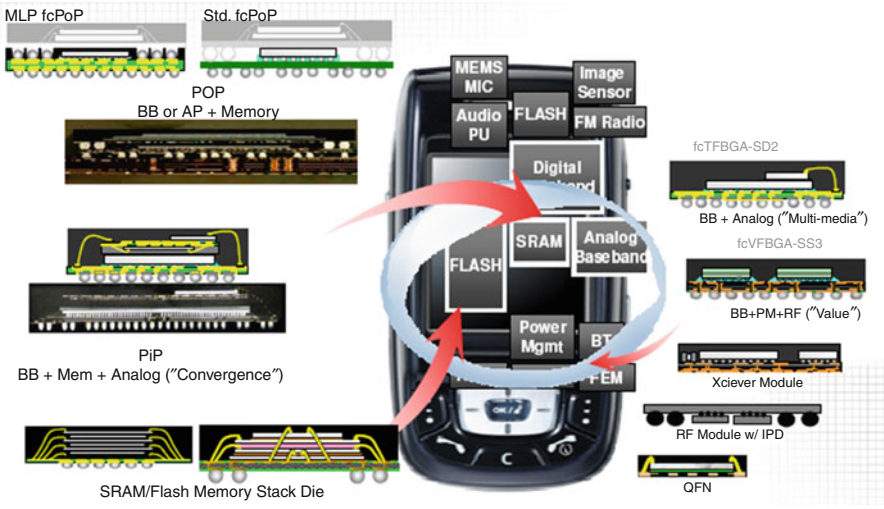

Fig. 2.20 Implementation of PoP and PiP in the cell phone. Courtesy of Raj Pense of StatsChipPac

applications; for example cell phones. Figure 2.20 shows many PoP's and PiP's, used in a cell phone assembly, varying in types, sizes of various devices, and interconnect methodologies used. A system level integration of various individual packages involving initial design validation and optimization in terms of mechanical, thermal and electrical performance is needed. Various software packages, such as, Ansoft SIP System Integration solution, are commercially available for such system level integration.

Stacked packages can contain all same die, as for memory PoP, or heterogeneous devices for graphics, ASICS, gamming, handheld devices where thin/light packages are needed. These dies can be without TSV (Through-Silicon-Via) or with TSV's. Stacked packages consist of either perimeter I/O (BGA) connections, or uBGA connection through a laminate interposer (Fan-in PiP). By using these package as an integration fabric to combine one or more ICs with discrete, embedded, and other packaged parts, a module can be created and used as a standard component for a POP assembly.

From a reliability perspective the PoP and PiP have shown that they can have a ball count of ~300 for 10 × 10 mm packages and ~600 for 15 × 15 mm packages and can have a junction temperature, T_j, as high as 110 °C. There is a need to improve/control package warpage to about 60 μm by materials and structural design. ITRS projection for 2014 stacked package include the following; Low cost/handheld 14 die/stack, High performance 5 die/stack, and low cost/handheld 15 die/SiP.

There is a large infrastructure of PoP with 10 OEMs in the portable Multi-media market, over 15 major (logic and memory) IDMs, and it is supported by the full service packaging houses (STATS ChipPAC, Amkor, & ASC)

Common design ground rules are allowing components from multiple vendors in a single PoP. All the flip chip structures discussed so far as characterized as fan-in, where the redistribution layer of the WL-CSP goes from perimeter array to u-BGA area array. A new kind of structure, called Fan-out, has been developed for cases where the number of required u-BGA exceeds chip area. Here the fan out redistribution occurs on molded areas around the chip [34].

2.6.1 Embedded Chip Packages

Embedded Chip technology was first developed by GE for military applications. The main idea of embedded chip packages is to build the laminate substrate around the chips. That is, the chip is placed first on a polymer film followed by a second polymer lamination cover the chip. Then, vias in the second polymer are opened through laser, exposing the metal pads on the chip. A metal wiring is defined which redistributes chip signal to the top of the second polymer film. The polymer lamination, via formation and wiring process is repeated several times, and the package is finished with u-BGA for further interconnection [34]. The alpha particles concerns are eliminated since the chips are surrounded by the laminated polymer. Reduced interconnection pitch is possible due to small via

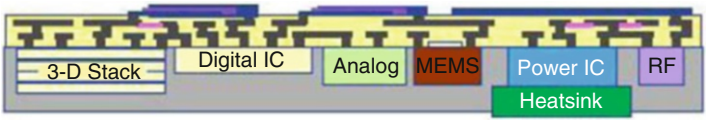

Fig. 2.21 Example of embedded chip package developed by GE

diameter. They are expected to have better EM since there is no solder to package connection.

The main limitation for embedded chips is high cost. Any yield losses in the fabrication of the package results in scrapping the electrically good chip. Additionally, unlike traditional laminate chip carriers which are fabricated on a ~350 × 500 mm panel size, the embedded chips are fabricated on wafer type tools on a 200 mm or 300 mm format. Most reported packages consist of a relative low number of I/O (<500 I/Os). Materials optimization for structural robustness is required to avoid chip, BEOL or organic dielectric cracks.

Commercialization has been slow but it is starting to take traction with cell phone applications where thin/light packages are needed, and high reliability is not required. Additionally, the embedded technology can be mapped with multiple chips per package, either by chips stacks or side by side. Intel published on embedded chips in 2002, but it has adopted the Cu-pillar joined to laminate technology instead. Fig. 2.21 shows a ACICs working test vehicle from GE containing four wiring layers and over 3,000 I/Os. Freescale. Shinko and the Institute of Microelectronics also have on-going development activities. IMEC is evaluating embedded chips on flex packages.

The embedded chip technology is extending to board manufactures with two new consortiums formed since 2007: HERMES, which is led by Fraunhofer and FlipChip, and Embedded Actives and Passives (EMAP) headed by PRC in GaTech.

2.6.2 Folded Stacked Packages

Folded Packages can have multiple flip chips joined to an organic tape which is folded onto itself with the net effect of stacking the chips, and significantly reducing the interconnection area. This represents a space reduction, similar to stacked packages, but the wiring lengths are similar to those in the 2D connection. Figure 2.22 shows a sample of this technology developed by Tessara. The prime features of this technology are described as following; a one-mil (25 μm) polyimide tape is used for low height, and better folding accuracy. The dies are thinned to 114 μm providing a smooth backside with laser dicing to eliminate die cracking. The die-to-die bond-line has a 12 μm thickness, and the back of die-to-tape attach adhesive is set to 25 μm. In a μBGA package with a compliant elastomer layer between active surfaces of die and substrate the 250 μm SAC solder ball results in a ball height of 140 μm after reflow.

Fig. 2.22 Three dies Folded Stacked Package [36]

2.7 Emerging Flip Chip Technologies

Through-silicon-via (TSV) have reduced the chip-to-chip connection length to the minimum. The TSV length is between 10 and 100 μm, depending on the amount of Si removed during the grinding process. The shorter path translates in speed increase and lower power loss due to less resistance, and to less switching noise due to lower inductance. The typical TSV fill materials are copper or tungsten, with polysilicon being mainly used in memory applications due to its high resistance. Wire bonding used extensively in PoP and PiP, which have a length between 1 and 5 mm, suffer from high inductance in the power leads, is not the preferred interconnection for high performance applications.

The 3D Wafer to wafer Bonding can occur in three ways:

Dielectric Bonding	Silicon Dioxide (SiO_2) fusion or Polymer adhesive
Metal Bonding or Hybrid Bonding	Metal (Cu) fusion, Intermetallic bonding, Solder Connection, or Au Thermosonic Concurrent Dielectric and Metal bonding

Dielectric bonding assumes that the TSVs will be fabricated after the bonding is completed, or what is referred to as TSV last. However, due to the high planarity and smoothness needed to yield oxide to oxide connection, dielectric bonding is not the preferred bonding method. Polymer bonding is mainly practiced in hybrid bonding.

Cu to Cu bonding also requires fairly parallel surfaces, which can be created by using standard damascene process, with an etch-back of the temporary oxide dielectric. Cu–Cu thermocompression bonding occurs at 400 °C for 30 min at pressure per mm of >40 N/mm. A good Cu–Cu bonding occurs when the Cu grains extend through the connection interface (see Fig. 2.23). Lu, et al., from RPI, has shown excellent hybrid connection using Cu–Cu bonding and BCB as the adhesive [37]. Yu, et al., from IBM have also demonstrated Cu–Cu bonding with ×1 polyimide as the adhesive using the transfer-joining (TJ) method. Figure 2.24 shows the TJ connection on a 200 mm wafer. Alternatively, to add structural integrity to the Cu–Cu bonding without using hybrid joining, polymer underfill can be done

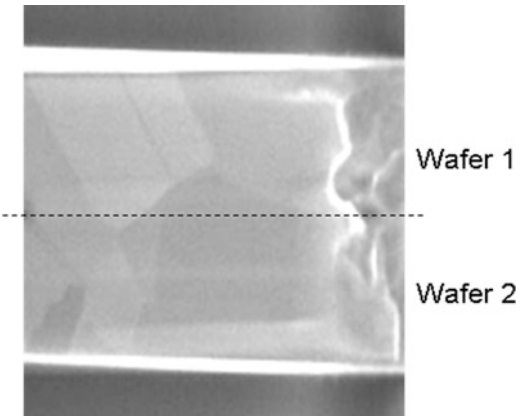

Fig. 2.23 Cu–Cu joining with shared grain growth

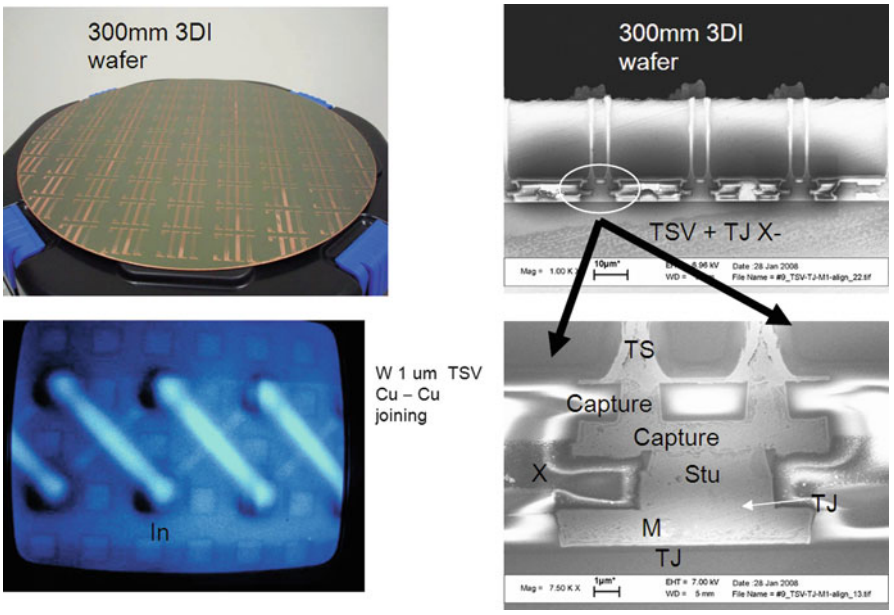

Fig. 2.24 The TJ connection on a 200 mm wafer. Courtesy of Roy Yu of IBM Corp

subsequently to the Cu–Cu joining. A gap of 10–15 μm is seeded for vacuum filled underfill, which is mainly practiced at the end of all wafer to wafer connections.

In some applications, the wafer is first bonded to a temporary carrier, such as Si or glass, with an adhesive. However, due to this limit on the maximum bonding temperature, a transient liquid phase (TLP) bonding is used, instead. During TLP or sometimes referred to as solid liquid interdiffusion, bonding results when solder (Sn or Sn3.5 %Ag) is used as the interconnection metal. The joining occurs at the solder melting temperature, with all the Sn converted to intermetallic, which has a

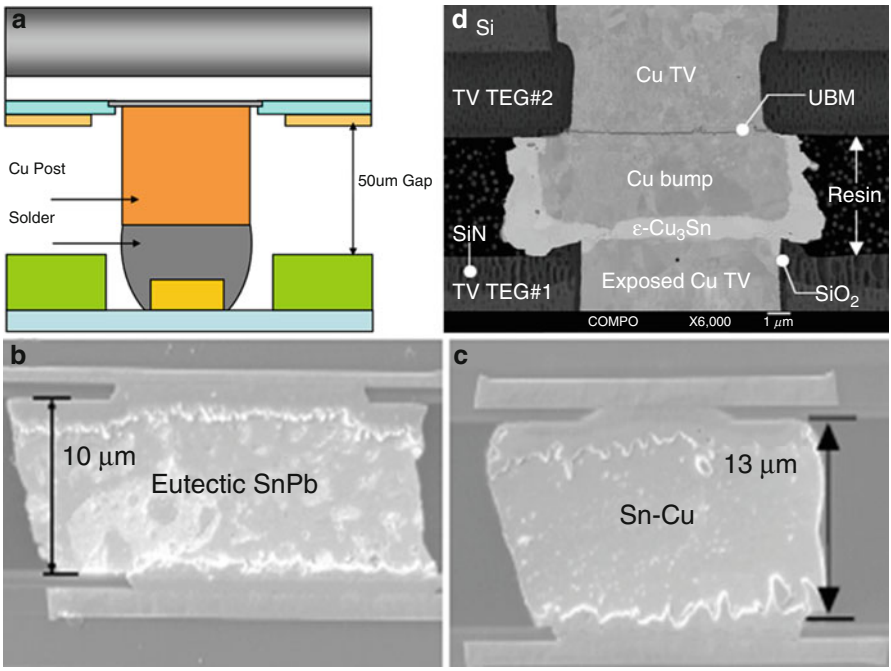

Fig. 2.25 Various fine pitch interconnects; (**a**) IBM's <70 μm pitch MPC-C2 process, (**b**) and (**c**) IBM 50 μm pitch report, and (d) ASAT 20 μm pitch TLP joining

much higher melting temperature, and can withstand the higher temperature needed for thermally decomposing the temporary adhesive. Intermetallic bonding by itself forms a brittle bond. Underfill is used for mechanical support and corrosion prevention purposes.

TLP and Cu-solder-Cu joints are most practiced on chip-to-Si interposer or chip-to-wafer. TLP joints should perform better in EM testing since all the Sn is consumed, eliminating a major EM failure mode. The Japanese Association of Advance Electronic Technologies (ASAT) has reported TLP bonding on 20 μm pitch [39]. They have reported importance of removing the Cu oxide to obtain good connection at joining. One main difference between TLP and solder joining is that TLP required thermal compression, while solder bonding does not. Solder joining is used on >40 μm pitch joining, mainly on chip-to-chip joining, and is a scaled down extension of the traditional chip joining, but on tight pitch requires a bonder to maintain placement accuracy during reflow. 50 μm pitch Cu-Solder-Cu evaluation was reported by IBM with excellent EM results [40]. The Metal Post Colder-chip connection (MPC-C2) process developed by IBM Japan, initially for chip to laminate can also be used on chip-to-chip connection for larger pitch and larger chip-to-chip gaps [41]. Figure 2.25 depicts various fine pitch technologies.

Emerging technologies, such as 3D, are further requiring the reduction of the solder pitch to 50 μm and lower, and in some cases elimination of the solder connection and replacing it with metal to metal connection.

2.8 Summary

Flip chip technology was invented and developed by IBM about 40 years ago, in response to the need for a relatively large number of highly reliable input/output connections in semiconductor devices. Since then, the continuously increasing need for even larger number of I/O's, for example 10,000 I/O's per chip, has led to the development of various solder deposition technologies enabling smaller solder bumps at finer pitch. Green movement requiring use of lead free solders has imposed additional challenges of developing solder materials in first level packaging for greater mechanical stability in view of weaker BEOL structure due to use of fragile ultralow-k dielectric materials, and the need for improvement in EM performance. Intel copper pillar structure is one of the possible solutions for lead-free interconnect challenges. Furthermore, from performance improvement point, the packaging development being in cost advantageous position when compared to semiconductor technology development has led to development of SIP, POP, PiP, versions of system level packaging. The co-design tools have enabled package designers to participate in the multi-die design chain using a co-design methodology. In response to meet increased number of interconnections and higher performance, the development of fine pitch flip chip interconnections, 3D with TSV's and without TSV's, temporary adhesive liquid phase connections, and Cu-solder-Cu connections is continuously striving for excellence.

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