# Chapter 14
# Microelectronic Packaging Trends and the Role of Nanotechnology

**Madhav Datta**

## 14.1 Introduction

The microelectronic packaging industry is undergoing major changes to keep pace with the ever-increasing demands imposed by high performing chips and by end-use system applications. Solutions using advanced materials for microprocessor interconnect scaling and chip package interconnects, novel concepts in heat management systems, and improvements in package substrates continue to drive major packaging efforts. Advances in electrochemical technologies have played an important role in the evolution of such solutions for miniaturization of microelectronic devices and packages. Indeed, since the development of through-mask plating for thin film heads in the1960s and 1970s, an enormous amount of industrial and academic R&D effort has positioned electrochemical processing among the most sophisticated processing technologies employed in the microelectronics industry today [1–4]. Electrochemical processing is perhaps better understood than some of the dry processing technologies used in the microelectronics industry. Compared to other competing dry processing technologies, it has emerged as a more environmentally-friendly and cost-effective fabrication method. Electrochemical processing has, thus, become an integral part of advanced wafer processing fabs and an enabling technology for nanofabrication [5]. As the electronics industry faces the challenges of extending Moore's law, electrochemical processing is expected to continue to enable further miniaturization of high-performance chip interconnects, packages, and printed circuit boards. Evolving novel approaches to electrochemical processing using nano-materials and nano-fabrication techniques have started to make tremendous impact on further miniaturization of high performance devices and packages. A detailed discussion of different facets of technology advances in electronic packaging is difficult to present in the limited space of this chapter. The current chapter, therefore, makes an effort to capture some of the key

M. Datta (✉)
Cooligy Precision Cooling, Emerson Network Power, 800 Maude Avenue, Mountain View, CA, 94043, USA
e-mail: madhav.datta@emerson.com

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developments in microelectronic packaging while highlighting the impact of electrochemical processing. Also included is a brief discussion of some of the foreseeable applications of nano-materials and nano-structures in advanced packaging.

## 14.2 Microelectronic Packaging

Electronic packaging is the methodology for connecting and interfacing the chip technology with a system and the physical world. The objective of packaging is to ensure that the devices and interconnections are packaged efficiently and reliably. With continued miniaturization trends in integrated circuits, a steadily increasing percentage of wiring migrates into the chip, thus, making the semiconductor thin film wiring a very important aspect of microelectronic packaging [6, 7]. A typical microprocessor packaging hierarchy consists of several levels of packaging. The chip level packaging includes chip interconnect wiring (metallization), and provisions for chip-package interconnection such as flip-chip bumping, wire bonding, and tape automated bonding (TAB) [6–9]. The first level of packaging involves joining of chip(s) to a substrate, which may form a single chip module (SCM) or a multichip module (MCM). Depending on the thermal cycle environment, the substrates for SCM/MCM may be either organic or ceramic packages. In the second level of packaging, packaged SCMs, MCMs, and other components are assembled on a printed circuit board (PCB) or card. PCBs are generally copper-clad sheets of epoxy-glass laminates with plated through-hole interconnections. In some cases, the chips (without a substrate) are directly attached to boards (direct chip attach) known as chip-on-board (COB). The third level of packaging may vary depending on the system. In a desktop, several PCBs are plugged into a motherboard, while in a hand-held calculator the outer shell is the third level of packaging. On the other hand, a workstation or a mainframe uses several motherboards within an enclosed box.

Figure 14.1 is a schematic diagram showing the key components of a microprocessor assembly. The assembly consists of a chip, a package, and a printed circuit board that are joined together to form a second-level packaging. Chips with C4 solder bumps are flipped over and joined to the package substrate by reflow. An underfill is often used to improve reliability of the chip-package interconnect assembly. This first level assembly is further connected to the printed circuit board using ball grid arrays (BGA's) or pins. For efficient heat dissipation from the chip, an integrated heat spreader and a finned heat sink are attached to the back side of the chip using thermal interface materials (TIM1 and TIM2) Electrochemical processing technologies employed in the fabrication of all of these components, include low-end electroless nickel/gold coating of the copper heat sinks, wiring of packages and boards by through-hole plating, fabrication of plated C4 solder bumps and the fabrication of extremely precise nano-scale features of chip interconnect metallization. Accordingly, the degree of sophistication of tools and processes varies depending on whether they are applied in package/board fabrication on macro/micro scale or in semiconductor wafer processing on micro/nano scale [5].

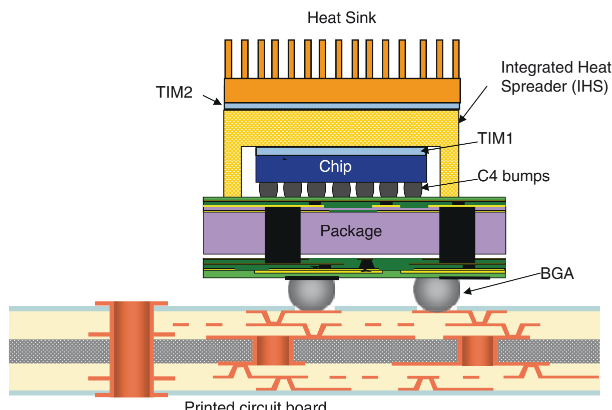


**Fig. 14.1** Schematic diagram of a microprocessor assembly showing different levels of packaging and thermal management solution using a heat sink. *TIM* thermal interface material, *BGA* ball grid array

## 14.3 Semiconductor Packaging: Cu Metallization and Flip-Chip Technology

Introduction of electroplated copper metallization replacing aluminum brought about a paradigm shift in chip interconnect technology [10]. Advanced microprocessors now use electroplated Cu technology because of several advantages associated with copper wiring, and with the electroplating technology that has enabled the high volume manufacturing of Cu chips [10]. Development of a defect-free dual Damascene electroplating process, and the semiconductor equipment industry's drive to develop and market electroplating and CMP tools were the key enabling factors that made the implementation of copper interconnect technology possible [5]. Indeed, the development and availability of high volume manufacturing of electroplating and CMP tools that are compatible with ultra-clean fab standards represented a major shift in the semiconductor industry's strategy that was hitherto focused on vacuum processing. These developments together with an aggressive integration scheme have enabled the development and manufacturing of advanced interconnects. The defect-free fabrication of nano-scale, multilevel interconnect structures on a 300 mm wafer with high yield demonstrates the exceptional strength of electroplating technology. All these developments have placed electrochemical processing on a firm footing as an enabling technology for nano-processing.

As the semiconductor industry prepares for the 45 nm node and beyond, issues related to integration of advanced interlayer dielectric (ILD) material into finer Cu lines has become the key challenge. Accordingly, novel electrochemical processing methods that address issues related to planarization of the fragile Cu/ILD structure and electromigration of copper interconnects are evolving . A combination of electrochemical and

mechanical means of Cu removal is being employed as a novel planarization technique. Following this direction, currently there are two different approaches being pursued by semiconductor equipment vendors [11,12]. In one approach, planarization is achieved during electroplating using electrochemical mechanical deposition (ECMD), which is then followed by electropolishing to remove the overburden, while in the other approach electroplating is followed by electrochemical mechanical polishing (ECMP). Both approaches emphasize electropolishing as the *key* metal removal method, thus positioning electropolishing at the center stage of planarization technologies for interconnect structure fabrication [11].

Another important development in chip interconnect is the use of electrolessly deposited capped nano-layer that reduces copper electromigration and provides improved interconnect current density capability. The PVD sputtered Ta(N) liner and PECVD Si(C)N cap technologies have been used as diffusion barriers for copper interconnects from the 0.25um to 65 nm process nodes [10, 13]. The PVD Ta(N) liner is a relatively high-resistance film and it accounts for ~15% of the metal area on lower metal layers. The key problem with the PECVD Si(C)N dielectric capping is that it forms a relatively weak chemical bond with copper that allows for excessive copper migration at the Cu-Si(C)N interface thus giving rise to electromigration problems, which limit the maximum current density in the underlying wire [13]. The PECVD Si(C)N cap film, also, has a high dielectric constant ($k \sim 7$).

Selective electroless deposition of cobalt alloys offers a novel approach for forming self-aligned metallic cap layers. Such films have better adhesion to copper than dielectric films.

An electroless metal cap deposition process is especially appealing because of low cost, intrinsic selectivity and superior film properties. Electroless deposition of Co and its alloys has been widely studied and interconnect capping processes using, Co, CoW, CoWP, and CoWB are available in literature [13–19]. Recent efforts have focused on developing Pd-free process for selective deposition of nano-layer of capped material [16, 17]. Long-term reliability data obtained in different research laboratories indicated that electroless CoW capping tremendously improved EM resistance [13, 17–19]. The electroless CoWP cap has also been shown to have excellent adhesion to copper, good corrosion and diffusion properties, as well as good selectivity. The semiconductor equipment industry is currently involved in the development and qualification of both Pd activation-based and Pd-free CoWP processes. Figure 14.2 shows SEM photographs of a CoWP-capped copper interconnect using a commercially developed Co alloy process and tool [19].

Chip-package interconnection technologies currently used in the semiconductor industry include wire bonding, TAB, and flip-chip solder connection. Flip-chip (C4) interconnection is an area array configuration in which the entire surface of the chip can be covered with bumps for the highest possible I/O counts. Various solder bumping technologies are used in high volume production, including evaporation, electroplating, and solder paste printing. IBM's original C4 technology involved evaporation of both seed layers and high melting temperature PbSn (90–97% Pb) solders and was mainly meant for high-end applications involving ceramic packages. However, with the increased demand of higher I/Os for consumer and mid-range products with

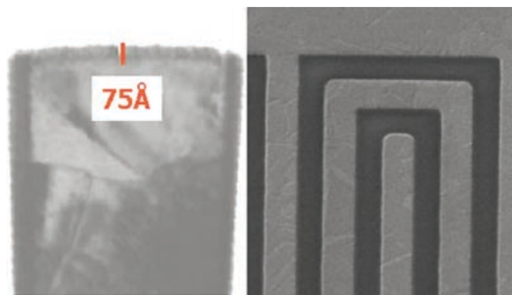


**Fig. 14.2** SEM photographs of copper interconnects capped with 7.5 nm thick CoWP. *Left* cross section view, *Right* top view. Ref. [19]

plastic packages, which required a cost-effective C4 process with lower melting temperature eutectic solders (63Sn37Pb), the limitations of evaporation became apparent and paved the way for electroplating. Screening of solder paste is another means of fabricating solder bumps on wafers and packages. While this method is cost-effective for certain applications, inability to fabricate metal screens with fine dimensions limits the bump size/pitch and issues related to solder voids limit the process to low-end products. Electrochemical fabrication of C4s has now become the industry standard for advanced microprocessor assembly [20].

Electrochemical fabrication of C4s is an extremely selective and efficient process, which is extendible to finer pitch, larger wafers, and a variety of solder compositions including some lead-free alloys [20, 21]. These advantages, coupled with the advantages of area array interconnections, are making the plated C4 technology a preferable chip-package interconnection for a variety of products. Besides through-mask electroplating of solder alloys, the C4 fabrication involves careful etching of the underlying seed/ball-limiting metallurgy (BLM) layers. For some selected BLM layers such as phased CrCu, electroetching methods have been found to be the only means for their removal. This led to the development of various manufacturing processes and tools for electroetching.

Currently, two types of as-plated bump shapes are common in the microelectronics industry: mushroom bumps and column bumps. While mushroom bump technology has the advantage of using industry-standard-thin (up to 25 μm) photoresist, it may not be applicable to advanced products with narrower pitch bumps and high I/Os, due to possible bridging problems associated with these bumps. Furthermore, volume uniformity of mushroom bumps is difficult to control. On the other hand, the use of a thicker photo-resist mask to restrict the bump-plating process within the photo-resist feature permits fabrication of column bumps. Column bumps are extendible to finer pitch and higher I/Os, and provide better volume uniformity control. With the availability of cost-effective thick photo-resist technology, the semiconductor industry is rapidly moving from mushroom bumps to column bumps.

Another new method of solder bumping is based on injection-molded solder technique. This technology, which is known as C4NP (C4-new process) was developed

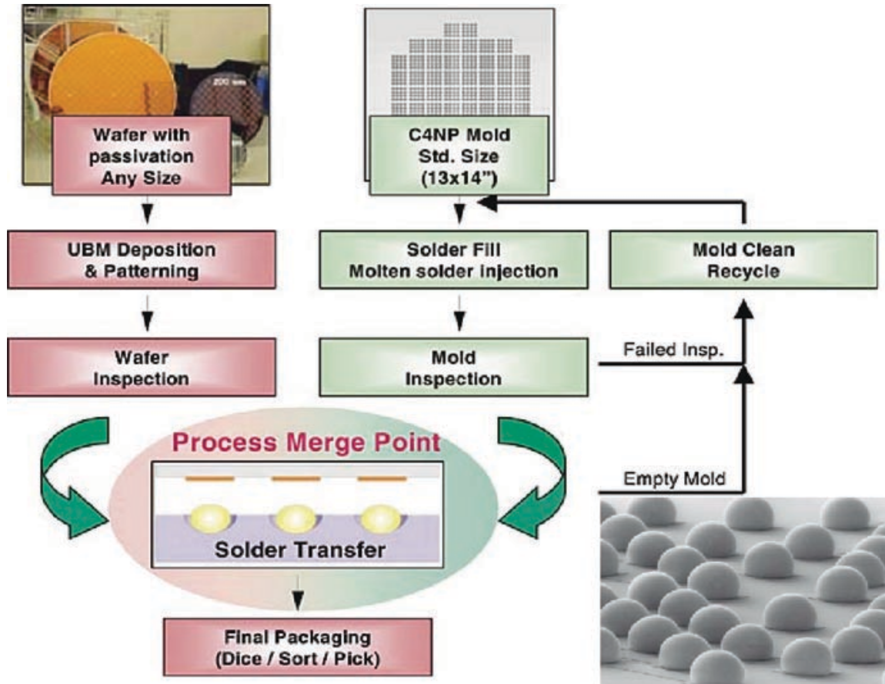


**Fig. 14.3** Process steps involved in the C4NP technology. Wafers with BLM and solder-filled molds are processed in parallel and joined together. Solder bumps are thus transferred to the wafer. *Inset*: Solder balls formed by C4NP process. Ref. [23] reproduced with permission of the Electrochemical Society

at IBM and is now commercialized by Suss MicroTec [22, 23]. C4NP is a solder transfer technology where molten solder is injected into prefabricated and reusable glass templates (molds). The sequence of process steps involved is shown in Fig. 14.3. Borofloat glass plates, with the coefficient of thermal expansion matching that of silicon, are used to form the molds. Lithographic patterning and etching processes are used to form cavities with well-defined bump pitch and whose diameter and depth precisely determine the volume of the solder bump. The mold cavities are precisely filled with solder by injecting molten solder through a solder-injection head. After inspection, molds and wafer are brought into contact and solder bumps are transferred onto the entire wafer. C4NP technology is capable of fine pitch bumping while offering alloy selection flexibility. The technology is, therefore, particularly suited for exotic ternary or quaternary lead-free solder-bumping application.

Lead-tin alloys are the most commonly used solder materials for microelectronic packaging. Pb and Pb-rich alloys have one of the most desirable characteristics of C4 solders in that they are soft and compliant. The compliant nature of these alloys act a cushion for absorbing thermal and mechanical stresses and transfer minimum stresses to the die during microprocessor assembly processes. On the other hand, the melting

temperature of these C4 materials is in the range of 310–328°C. The high joining temperatures required for these C4 solders make these materials incompatible with the advanced interconnect ILD materials and plastic packages. Indeed, integration of low-k/ULK dielectric in the chip necessitates a low temperature joining process, hence a low melting temperature solder. These integration issues coupled with increasing health and environmental concerns of lead-containing alloys, the microelectronic industry is now gearing up to the worldwide call for Pb-free solders.

In spite of a tremendous amount of effort for the search of lead-free C4s, no industry standard has evolved as yet. Commonly cited lead-free solders are Sn-rich alloys for which electroplating processes are available. The most popular lead-free solder among them is Sn3.9Ag0.6Cu with a melting temperature of 217°C. This solder is recommended by National Electronic Manufacturing Initiative (NEMI) and has been extensively studied and characterized by NIST. However, applicability of this solder as a C4 material in chips with advanced ILD is not known.

Indeed, Sn-rich solders present several issues, which need to be thoroughly examined for their applicability as advanced C4 materials. Sn-rich solders are normally 2.5–3.0 times harder than Pb-rich alloys (Table 14.1). Due to this reason, integration of Sn-rich C4s with fragile ULK will require significant modifications in the chip-package assembly process to avoid issues due to chip cracking. Another issue is high reactivity of Sn with copper. In some cases, Sn migration through BLM cracks may lead to chip failure [24, 25]. Sn-rich C4s, therefore, require selection of robust BLM layers and development of their etching processes. Finally, Sn-rich solders are prone to whisker growth, which may cause electrical shorts. Prevention of whisker growth, however, has been possible through alloying and through the use of additives in the plating bath.

Currently, there is no unique solution to lead-free C4 material that is available at this time. Based on the above discussions, it is anticipated that the selection of lead-free solder for C4s will be dictated by the interconnect materials in the chip and by the selected packaging solution. Therefore, the lead-free C4 material selection is expected to be application-specific.

The integrity of barrier layer metallurgy (BLM) is one of the key concerns for the reliability of microprocessor assemblies using Sn-rich solders. Commonly used BLMs consist of a combination of an adhesion layer and a solderable layer [20, 21].

**Table 14.1** Thermo-mechanical properties of lead and tin rich solders [11, 20]

| Solder type | Metal/alloy | Melting temperature, °C | Young's modulus, GPa |
|---|---|---|---|
| Lead-rich | Pb | 328 | 21 |
| | 97Pb3Sn | 310 | 22 |
| | 63Sn37Pb | 183 | 36 |
| Tin-rich | Sn0.75 Cu | 227–229 | 50 |
| | Sn3.5 Ag | 221 | 51 |
| | Sn3.9Ag0.6Cu | 217 | 51 |
| | Sn58Bi | 139 | 28.5 |
| | Sn52In | 117 | 23.6 |

Due to fast kinetics of the Sn–Cu reaction, diffusion of Sn through the BLM must be prevented. The refractory metals, such as Ti, W, and TiW, are applicable as a barrier layer for Cu. However, as shown in Fig. 14.4, cracks and other defects present in the barrier layer or induced during thermal cycling, may act as migration path for Sn, which may react with the Cu conductors thus creating electrical shorts and eventually causing failure of the device. An example of such die-package interaction leading to microprocessor failure is shown in Fig. 14.4. The reliability tests of assembled microprocessor led to failure after baking at 170°C for 480 h [24–26]. Failure analysis included EDX analysis of cross-sectioned chip surface, which showed the presence of CuSn intermetallic around final copper lines leading to shorting of lines and eventual microprocessor failure. Further analysis of the BLM layer after selective etching of the C4 solder and the solderable layer showed cracks on the Ti layer. These data indicated that migration of Sn through BLM cracks and its reaction with copper is indeed a possible mechanism that is responsible for microprocessor failure. Grain boundary diffusion in crystalline material is another possible mode of compromising barrier properties. The use of amorphous layers, such as TiW, help alleviate such issues. For good bonding, the intermetallic reaction between Cu in the BLM and the Sn in the solder produces Cu6Sn5 that adheres well both to the solder and to the Cu in the BLM. To obtain good adhesion, it is imperative that all Cu is not consumed in intermetallic reaction because the Cu6Sn5 intermetallic does not adhere well to the underlying Cr, Ti or TiW layer. With high tin-containing solders, complete consumption of the thin Cu in the BLM causes loss of adhesion and a weak interface. Therefore, one of the accepted processes used for eutectic 63Sn/37Pb solder bumping is the use of a Cu stud as the BLM. The copper stud is electroplated through a photo-resist mask on top of a sputtered TiW/Cu BLM. The function of the Cu stud (or "minibump") is to provide an increased solder wettable area and to provide a solder diffusion barrier. However, these functions of the Cu stud have to be evaluated vis-à-vis its impact on the solder fatigue life. The Cu stud process is also becoming widely popular for Sn-rich alloys that are being implemented as Pb-free solders for C4 bumping.

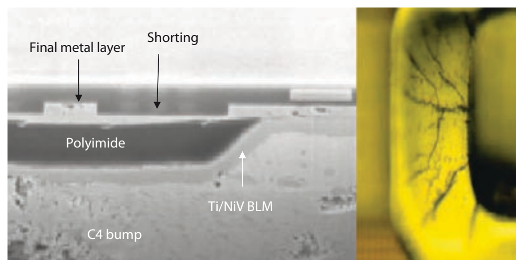


**Fig. 14.4** FIB cross section of a failed chip showing the two last layers of copper metallization and C4 bump (*left*). Migration of Sn through cracks in the BLM layer and its reaction with cooper metallization led to shorting and microprocessor failure. Cracks in the Ti layer (after selective etching of solder and solderable layer) is clearly visible (*right*)

## 14.4 First-Level Packages and Printed Circuit Boards

First-level packages provide interconnection between the printed circuit board and the chip. These packages must have the desired number of wiring layers, provide thermal expansion compatibility with the chip, provide a thermal path for heat dissipation from the chip, and keep electrical noise and transmission delay to the minimum. The two types of packages used are plastic packages and ceramic packages.

Plastic or organic packages offer many advantages over ceramic packages in terms of size, weight, performance, cost, and availability. Tremendous improvements in hermeticity, and reliability of organic packages have increased use of plastic packages in a wide range of products spanning from consumer to low-end to high-end microelectronic assemblies and account for 97% of the first-level package market [27]. The substrate technology is generally based on a single-level metal frame, which is the foundation of the molded plastic package. The two most common lead frame metals employed by the industry are nickel–iron alloy (alloy 42, 42%Ni/58%Fe), and copper alloy [27, 28]. The chip is bonded with a die attach adhesive onto the die paddle. Gold wire bonding is used to make the connections between the chip and the lead frame. Injection molding process is used to encapsulate the IC and bond wires. The outer leads are then solder-screened or plated for board mount. Plastic ball grid array (PBGA) package with an organic substrate technology has now become the technology of choice for IC packaging. It is based on the concept of printed circuit board manufacturing, which uses plated through-hole technology used to form the copper interconnections. Development of these denser but lighter packages were made possible through advances in electrochemical processing technologies including the ability to obtain micro-via plating coverage, fine wiring, and high aspect ratio through hole plating.

Ceramic packages use co-fired multilayer ceramic substrates and provide the highest wiring density of all packaging technologies. Co-firing of as many as 63 layers in full production and 100 layers in development have been reported [6]. Indeed, hermiticity and exceptional dimensional stability of ceramic substrates make these packages superior to organic packages. Since high density of wiring is possible in thin film layers, the addition of thin film layers on ceramic packages reduces the total number of layers required in the package. Electrochemical processing technologies played a significant role in the development of these packages. Some of these process steps include: electroplating and etching to form vias and conductor wires, electroless plating of Co(P) as diffusion barrier layer, electroless deposition of Ni/Au on sintered molybdenum pads, and chemical mechanical polishing for planar structures.

For PCB, plated through-hole technology enables interconnection of various layers through formation of vias and holes. The sequential lamination involves lamination of subassemblies with drilled and plated-through holes interconnection. Evolution of PCB industry owes much to the development in electrochemical processing technologies, which enabled efficient fabrication of circuits on non-metallic surfaces through the availability of high volume plating and etching technologies.

PCB wiring requires high ductility copper, for which both electroless and electrolytic baths have been developed [29, 30]. Electroless plating provides good throwing power, hence is suitable for high aspect ratio multilayered boards with densely packed inhomogeneous circuitry.

The on-going materials development efforts in the packaging industry are aimed at developing nano-engineered packages with polymers and metals having improved thermo-mechanical properties. Some of the challenges include nano-material synthesis, placement at nano-scale, material property control at molecular level, and new metrologies for characterizing morphology and properties at nano-scale.

## 14.5 Thermal Management

Microprocessor scaling for increased performance and reduced cost places significant challenges on power delivery and heat removal. Heat removal is essential for an electronic package to offer optimal performance without failure. The substrate and circuit often possess different rates of thermal expansion. Thermal cycling and other thermo-mechanical stresses can lead to breaks in interconnections and package failure. Solutions using advanced materials and thermal management systems such as heat spreaders and efficient cooling systems are needed to facilitate heat removal. Key thermal management challenges include increasing power dissipation and the need to cool regions of local power concentrations on the die known as hot spots. A typical microprocessor assembly shown in Fig. 14.1 includes thermal management features such as integrated heat spreader (IHS) to spread heat while transporting heat from the die to the heat sink, which in turn dissipates heat to the environment through a fan. Successful thermal management requires the use of a thermal interface material (TIM) that makes good thermal contact between the die and the integrated heat spreader and the heat spreader and the heat sink. TIMs are generally thermal greases and gels that are made up of a polymeric material loaded with thermally conducting metallic or ceramic fillers [31, 32]. Heat dissipation through these materials occurs through percolation. Metallic TIMs such as solders materials provide heat dissipation entirely through conduction. However, the integration of metallic TIMs in microprocessor assembly is an enormous challenging task involving issues related to stresses and expensive processing steps.

### *14.5.1 Advanced Cooling Systems*

Solutions using advanced materials and thermal management systems, such as heat spreaders and cooling systems, are currently employed to facilitate heat removal. Heat sinks and heat pipes are among the commonly used solutions for cooling microprocessor assemblies. In each case, successful thermal management requires the use of a TIMthat makes good thermal contact between the die and the heat sink and the

integrated heat spreader. TIMs are generally thermal greases or gels that are made up of a polymeric material loaded with thermally conducting metallic or ceramic fillers. Advanced thermal management solutions are now evolving, which include the use of cooling systems such as micro-channel (also known as micro-structure), liquid cooling, and attention to enhanced thermal conductivity TIMs. The use of a liquid-cooling system is attractive because of higher heat transfer coefficients or lower thermal resistance as compared to traditional heat pipe or heat sink solutions.

A liquid-cooling system (LCS) for cooling microprocessors is shown in Fig. 14.5, which shows the schematic of a closed-loop LCS for a typical application that requires cooling of two microprocessors [33]. Two microheat exchangers are attached to the microprocessors with a TIM in between the heat exchanger and the microprocessor. Cold liquid, driven by a pump, enters the microheat exchangers where the flowing liquid extracts the heat from the microprocessors. The warm liquid flows into a fan-cooled radiator where it rejects the heat to the air thus cooling the liquid in preparation for repeating the cycle.

A microheat exchanger is one of the key components of LCS. Figure 14.6a shows a schematic diagram of a typical microheat exchanger. The microheat exchanger base (also known as the cold plate) is placed on top of the heat source with a thermal interface material in between. Effective heat transfer in a cooling system requires the cooling fluid to be in contact with as much surface area as possible of the material that is designed to extract the heat. In microheat exchangers, where the non-dimensional heat transport rate, as expressed by its Nusselt number, is a constant quantity – the heat-transfer coefficient is inversely proportional to the

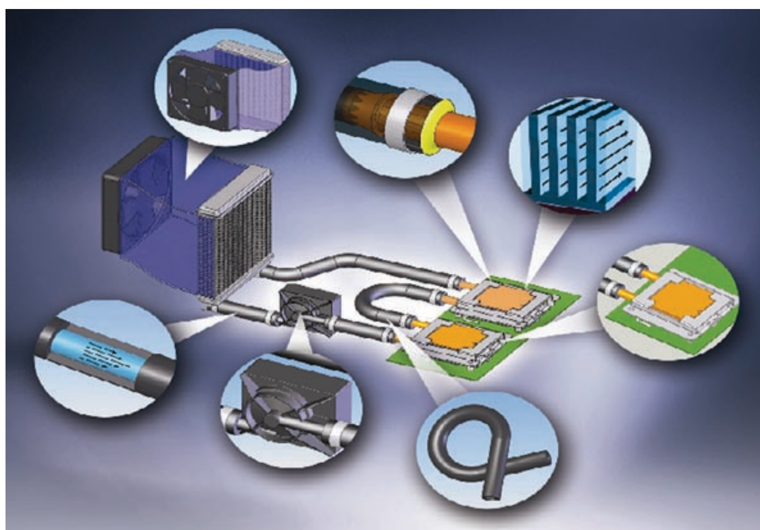

**Fig. 14.5** A commercially available Custom Designed Liquid Cooling System [33]

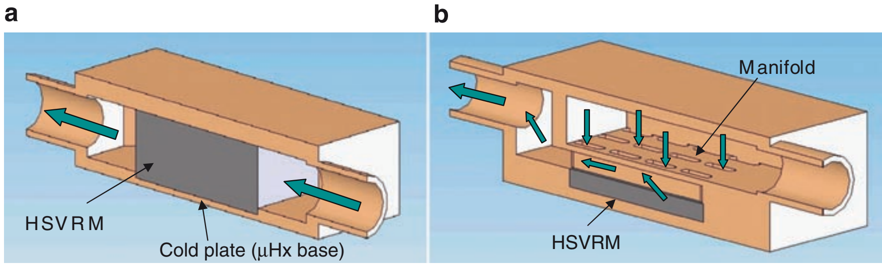


**Fig. 14.6** Schematic diagram showing cross section of microheat exchangers (**a**) without and (**b**) with manifold [33, 34]

hydraulic diameter. Heat exchangers with *high surface-to-volume-ratio microstructures* (HSVRMs) through which the liquid flows should, therefore, provide significantly enhanced heat transfer. Fabrication of heat exchangers with reliable and efficient HSVRMs is, therefore, extremely critical.

HSVRMs with very fine openings provide significantly enhanced heat transfer. However, the problem with fine openings is that they also increase the pressure drop, imposing additional requirements on the pumping system. This problem has been circumvented by incorporating a manifold into the heat exchanger, while retaining the microstructure adjacent to the surface to be cooled [34]. Use of a properly designed manifold helps to uniformly distribute the cooling liquid flow

through the HSVRM, thus significantly minimizing pressure drop. A typical microheat exchanger with a manifold over HSVRM is shown in Fig. 14.6b. It is apparent from the above discussion that developing a microheat exchanger with a high heat-transfer rate and minimized pressure drop is a challenging task that requires proper design of the HSVRM structure.

In addition to efficient microheat exchangers, high thermal performance of LCS require high efficiency radiator designs and the use of a high thermal conductivity cooling liquid that provide minimum resistance to heat transfer. Highly reliable and robust LCS marketed by Cooligy use a compact, low-noise, and reliable pumping system; optimized cooling liquid with particular attention to the highest level of corrosion protection by using film-forming inhibitors; and ultra-low permeability flexible tubing and robust triple-sealed joints that ensure a completely leak-proof system with insignificant water loss over the lifetime of microprocessors [33].

## 14.6 Nanotechnology in Advanced Packaging

Nano-processing and nano-materials are playing a key role in the advancement of microelectronics packaging. Steady miniaturization of silicon devices and interconnects represents an evolutionary nano-technology where nano-processing has been integrated with conventional microscale processing. An enormous amount of exciting

research is currently underway in the area of nano-processing that is expected to shape the next generations of electronic packages. Such topics include: the use of nano-particles to influence thermo-mechanical properties of solders for flip-chip, BGAs, and packaging materials; the use of carbon nano-tubes, nano-fibers and their metallic composites for advanced chip interconnects and thermal interface materials; fabrication of porous nano-structures and development of nano-fluids for advanced cooling systems; ink-jet printing for low-cost printed electronics; and precise fabrication of n- or p-type nano-films and nano-wires for application in thermoelectric coolers. Some of these topics are briefly discussed below.

### *14.6.1 CNT/CNF and Their Metallic Composites*

Carbon nanotube (CNT) is one of the most-researched topics of nanotechnology. A CNT is a long, thin, cylindrical, hexagonal lattice (graphene) of carbon molecules, one molecule thick, only 10 to 20 atoms around, and up to 100 micrometer long. CNTs display extraordinary mechanical, electrical, and thermal properties [35, 36]. They have much higher current carrying capability than copper, they conduct heat as well as a diamond, and are about 100 times stronger than steel at 1/6th of the weight per volume. Their characteristics vary depending on how they are rolled, and how thick they are (single or multi-walled). Depending on the direction in which CNTs are rolled up they demonstrate either metallic or semiconducting properties, which is one reason why they can carry very high currents while emitting little heat. Because of their extremely desirable properties of high mechanical and thermal stability, high thermal conductivity and large current-carrying capacity, CNTs have aroused a lot of research interest in their applicability as ULSI interconnects of the future [37, 38]. Mixing together nano-tubes with different electrical properties could simplify the design of future chips. Le et al. used PECVD to grow whisker-like CNTs on the surface of a silicon wafer [38]. A layer of silicon dioxide was then deposited to encapsulate the CNTs and the chip surface. The top part of the CNTs and part of the silicon dioxide layer are then polished by CMP planarization. Using this method processing of multilayer interconnects using vertical carbon nano-tubes was demonstrated. However, the establishment of a method to separate and sort CNTs of different conductivity types remains one of the most important topics in nano-tube research.

Carbon nano-tubes and carbon nano-wires (CNF) have unique thermal and thermoelectric properties that give rise to new opportunities in thermal management of electronic devices. However, long and free-standing tubes and fibers may not be able to withstand the rigorous thermo-mechanical stresses in packaging process flows. Gap-filling copper between vertically aligned CNFs provides a suitable mechanical anchor for the nano-fibers to the substrate while also serving as a lateral heat spreader. The robust physical characteristics of the CNF–Cu composite also allow one to take advantage of increased contact surface area to the target material. Carbon nano-fiber composites are a strong candidate material to provide thermal

solutions for advanced cooling systems. Ngo et al. used DC-powered PECVD to fabricate vertically aligned, free-standing CNF arrays on silicon wafers of ~500 um thickness [39]. Copper electrodeposition was used for gap-filling high aspect ratio trenches, thereby creating CNF–Cu composite array. Obtained data demonstrated the mechanical strength and efficient interfacial heat conduction of CNF–Cu composite arrays suitable for next-generation heat-sink devices. A layer of titanium (300 Å) was used as both an adhesion layer for a thin layer of nickel catalyst used for the CNF array growth and as a seed layer for the subsequent copper electrodeposition. As grown vertically aligned carbon nano-fiber arrays are shown in Fig. 14.7. A superfilling copper electrodeposition bath was employed that consisted of 100 ppm chloride ions ($Cl^-$), 400 ppm polyethylene glycol (PEG), 10 ppm bis(2-sulfopropyl) disulfide (SPS), 10 ppm Janus Green B (JGB), 0.6 mol/l copper sulfate, and 1.85 mol/l sulfuric acid. An etching/electropolishing step in 85% ortho-phosphoric acid solution was used to improve surface finish and to remove excess copper thereby revealing the nano-fiber ends. Ngo et al. compared the thermal resistance measurements for as grown CNF array versus CNF-Cu composite with the same length and diameter distribution of fibers. CNF-Cu composites showed lower thermal resistance indicating their potential applicability as efficient thermal interface materials in cooling devices.

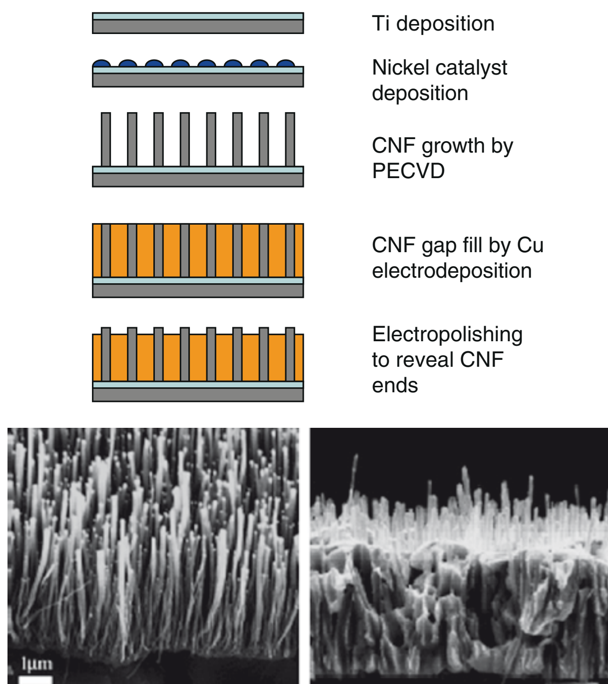


**Fig. 14.7** Top: Process steps involved in the fabrication of CNF-Cu composite. *Bottom left* SEM photographs of as grown CNFs, *Bottom right* CNF-Cu composite after copper electropolishing. Reprinted with permission from ref. [39]. Copyright (2004) American Chemical Society

Fabrication of carbon nanofiber-copper composite by electroplating was studied by Arai and Endo [40]. They used commercially available vapor-grown carbon nano-fibers fabricated by catalyst-assisted chemical vapor deposition as a filler material in a copper sulfate/sulfuric acid plating bath. The 20 mm long and 100–200 nm diameter carbon nano-fibres were fabricated by catalyst-assisted chemical vapor deposition. Two forms of polyacrylic acid, PA5000 and PA25000, were added to the bath to aid dispersion of CNFs with the aid of stirrer agitation. A relatively uniform dispersion of CNFs within copper grains was observed on the film. Cross section of the films indicated that CNFs were not only deposited on the surface but were distributed within the deposited thickness. These composites were easily separated from the substrate by ultrasonic waves in acetone, and by changing electrodeposition parameters the composites could be obtained in film or powder forms.

### *14.6.2 Nanoparticles in Advanced Packaging*

Nano-particles are expected to play a major impact in electronic packaging. Compared to their bulk counterparts, nano-scale materials exhibit large surface area and size-dependent distinct chemical, electrical, optical, thermal and magnetic properties. The thermo-mechanical properties of interconnect materials, packaging materials, and thermal interface materials can be significantly modified by the inclusion of nano-particles. Nano-particles are also finding increasing applications in nano-printing, and in nano-fluids for liquid-cooling devices. These aspects are briefly described in the following section.

#### 14.6.2.1 Nanoparticle Seeding for Interconnects

Electrochemical deposition is an effective method of seeding the inert barrier layer due to its inherent advantages in filling high aspect ratio features, as well as low processing cost. While palladium seeding is commonly used to initiate the autocatalytic reaction of subsequent electroless copper deposition, Pd reduces the stability of the electroless Cu plating bath and the formation of CuPd alloys increases the resistivity of electroless Cu deposits [41]. Li et al. studied the deposition of copper nano-particles to act as metal activation seed layers on TaSiN barrier films for subsequent electroless or electrolytic copper deposition applicable in nano-scale interconnect metallization [42]. The process is based on an electrochemical displacement mechanism in which the more noble metal ions in the organic solution are reduced to metal nano-particle crystals at the less noble solid metal substrate. The organic deposition solution consisted of conventional solvent extractants that are very poor electrolytic conductors but can sustain short-range spontaneous reactions. Additives consisting of low formula weight organics were used to enhance the copper nano-particle deposition. An aqueous15 g/L CuSO4 solution was mixed with an equal volume of organic extraction solution consisting of 30 vol%

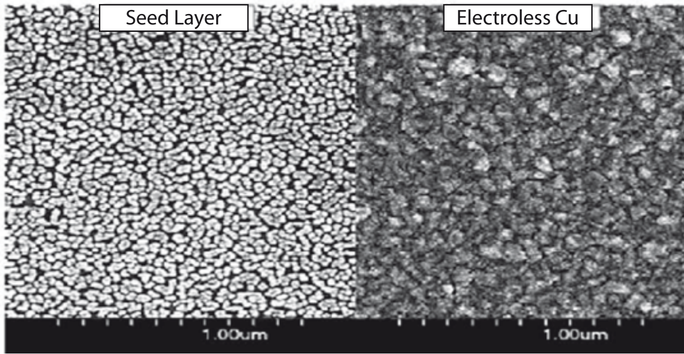


**Fig. 14.8** SEM photographs of Cu seeding on TaSiN (*left*) and subsequent electroless copper coating (*right*). Ref. [42] reproduced with permission for the Electrochemical Society

di-2-ethylhexy phosphoric acid, 20 vol% tri-*n* -butyl phosphate, and 50 vol% kerosene. The Cu concentration in the organic phase ranged from 10 to 300 ppm. A 2 vol% HF aqueous solution (50% concentration) was added into the deposition solution for in situ activation of the substrate surface. A proprietary additive was used, the concentration of which influenced the seed morphology. Without the additive, very few Cu nano-particles were present while the seed density increased with increasing additive concentration. A very dense, uniform Cu seed crystal layer was obtained with 10 vol% of the additive. Increasing the concentration of the additive to 20 vol% resulted in a bi-modal size distribution. The study of Li et al. demonstrated that the organic composition, degree of agitation, the seeding time, the additive type, and concentration all effect the morphology, density, and distribution of the Cu nano-particles [42]. Using optimized solution and deposition conditions, highly dense and uniform Cu nano-particles were successfully deposited on the TaSiN barrier at near ambient temperature and pressure. Electroless deposition of copper was performed on the Cu-seeded TaSiN. The morphology and quality of the electroless Cu plating was correlated with the morphology of the Cu seed layer. SEM photographs of Fig. 14.8 show that by using the optimized conditions for nano-particle seed layer deposition and electroless copper deposition, a very uniform and smooth cooper deposit could be obtained [42].

#### 14.6.2.2 Lead-Free Solders

The lead-free solders are mostly based on Sn-containing binary and ternary alloys. Among them, the Sn–Ag system is one of the earliest commercially available lead-free solders and has been recommended for general-purpose use as a substitute for Sn–Pb eutectic solder. Addition of nano-particles of second phase helps in improving thermo-mechanical properties such as melting temperature, mechanical strength, mechanical fatigue resistance, creep resistance and solder-joint reliability.

Lee et al. studies the influence of nickel concentration and inclusion of Ni3Sn4 nano-particles on the morphology of SnAgNi solders [43]. While inclusion of $Ni_3Sn_4$ nano-particles did not influence the melting temperature of the solder, the wettability of the solder to copper substrate increased significantly as evidenced by smaller contact angle of the $Ni_3Sn_4$ doped solders. Shen et al. studied the strengthening effects of $ZrO_2$ nano-particles on the microstructure and microhardness of Sn3.5Ag solder [44]. The addition of $ZrO_2$ nano-particles in Sn-3.5Ag solder resulted in a finely dispersed $Ag_3Sn$ phase. The refinement of microstructure is due to the adsorption of $ZrO_2$ nano-particles on the surface of the nucleating $Ag_3Sn$ phase during solidification. $ZrO_2$ nano-particles suppress growth of $Ag_3Sn$ intermetallic precipitates, and thus reduce the particle size of the formed $Ag_3Sn$ phase and lead to uniform dispersion of the phase. The finely dispersed $Ag_3Sn$ phase provides dispersion strengthening and therefore, enhances the microhardness of Sn-3.5Ag-$ZrO_2$ solder.

#### 14.6.2.3 Thermal Interface Materials

As shown in Fig. 14.1, in a microprocessor assembly, TIMs are used for conducting heat from chip to heat spreader and from heat spreader to heat sink. The TIMs are subject to challenging requirements, including the ability to reduce thermal stress between regions with vastly differing thermal expansion coefficients, the ability to be reworked, and high thermal conductivity [31, 32]. Commonly used TIMs include a variety of polymer-based materials with high thermal conductivity particle inclusions, typically with diameters of 2–25 μm. The effective thermal conductivities of particle-filled polymer interface materials are typically about an order of magnitude higher than the polymer matrix alone, i.e. of the order of 2 W/mK. Inclusion of nano-particles, in particular bundles of carbon nano-tubes or nano-fibres, is the subject of current research for improving the conductivity of interface materials. CNT/NF inclusions in soft materials promise near-ideal thermal and mechanical properties of TIMs. CNTs/CNFs offer very high directional thermal conductivities along with flexible geometry. This unique combination provides an opportunity for combining low-effective values of resistance and elastic modulus. In a recent study, thermal conductivities of silicone-based interface materials containing varying concentrations of nano-tubes and Ni particles were measured [32, 45]. The relative impact of an increase in CNT volume fraction was found to be amplified by the presence of nickel particles for CNT volume fraction above ~0.02%. This transition is consistent with a percolation model including thermal interconnections formed by CNTs between nickel particles.

#### 14.6.2.4 Nanofluids

Fluids containing suspensions of nanometer-sized solid particles are popularly known as nano-fluids. The solid nano-particles' or nano-fibers' size vary typically in the range of 1–100 nms. Nano-fluids have attracted great interest recently, particularly in

**Table 14.2** Thermal conductivities of selected solids and liquids [48]

| Material type | Material | Thermal conductivity (W/m – K) |
|---|---|---|
| Solids | Carbon nanotubes | 1,800–2,000 |
| | Diamond | 2,300 |
| | Graphite | 110–190 |
| | Fullerenes (film) | 0.4 |
| | Silver | 429 |
| | Copper | 401 |
| | Aluminum | 237 |
| | Nickel | 158 |
| | Silicon | 148 |
| | Alumina | 40 |
| Liquids | Water | 0.613 |
| | Ethylene glycol | 0.253 |
| | Engine oil | 0.145 |

liquid cooling systems, because of their greatly enhanced thermal properties. Solid materials have typically orders of magnitude larger thermal conductivity than liquids that are commonly used in heat transfer systems (Table 14.2). Because of the extremely HSVR of nano-particles, a dramatic improvement in the effective thermal conductivity is expected by decreasing the particle size in a solution compared to the incremental improvement that can be obtained by altering the shape of large particles. As an example, the surface-area-to volume ratio is 1,000 times larger for particles with a 10 nm diameter than that of a 10 um diameter particle. Nano-fluids are, therefore, expected to have superior heat-transfer properties compared to conventional fluids and fluids containing micrometer-sized particles. Indeed, a small amount (<1% volume fraction) of Cu nano-particles or carbon nano-tubes dispersed in ethylene glycol or oil is reported to increase the inherently poor thermal conductivity of the liquid by 40% and 150%, respectively [46, 47]. Nano-fluids with carbon nano-tubes are expected to possess even better heat-transfer properties due to the non-spherical shape of the carbon nano-tubes [48]. The optimization of nano-fluid thermal properties requires successful synthesis procedures for creating stable suspensions of nano-particles in liquids. Depending on the requirements of a particular application, many combinations of particle materials and fluids are of potential interest. For example, nano-particles of oxides, nitrides, metals, metal carbides, and non-metals with or without surfactant molecules can be dispersed into fluids such as water, ethylene glycol, or oils [46].

#### 14.6.2.5 Ink-jet Printing

Nanotechnology is bringing a paradigm shift in packaging through the development of low-cost printed electronics based on novel inks and printing fluids [49]. Ink-jet is noncontact digital printing that produces consistent drop volume with accurate drop displacement. It is an additive process that does not waste expensive material.

The deposition system consists of ink-jet, fluid, printer and software. Ink-jet printing allows the ability to print directly on package and substrates. Development of printable fluids containing nano-particles of conducting, semiconducting, dielectric, and insulating materials is central to the ink-jet technology for electronics. The sintering of nano-particles is significantly lower than the bulk materials. This property enables the printing of high-conducting metallic structures on packaging materials such as ceramics and polymers [49]. The ink-jet fluids can be manipulated and blended to build up layer-by-layer structures of electronic components. Linking computer-aided-design to the printer thus makes it possible to create functional electronic structures.

### *14.6.3 Active Micro and Nanostructures for Thermal Management*

As noted earlier, design and development of a high surface area active microstructure is an essential consideration of an efficient liquid cooling system. Indeed, effective heat transfer in a cooling system requires the cooling fluid to be in contact with as much surface area as possible of the material that is designed to extract the heat.

Several different types of High Surface to Volume Ratio Microstructures (HSVRM) and their use in microheat exchangers have been mentioned in the literature [50–56]. For brevity, we classify the HSVRMs into two types: (1) Microchannel type, and (2) Microporous type. Figure 14.9 shows typical microchannel type of HSVRMs. Silicon micro channels are one of the commonly cited heat collector structures used in liquid cooling systems [50]. High aspect ratio channels are easily fabricated by anisotropic etching of silicon, which has found widespread use in micromachining and MEMS. However, the low thermal conductivity of silicon makes it a less-effective heat exchanger material relative to metallic materials. Metallic microchannels are formed by different mechanical or electrochemical means including EDM, dicing, LIGA and plating through thick photo-resist masks. Folded fins are another class of microchannel HSVRMs that are used as heat exchanger structures and they can be straight or louvered fin types [52].

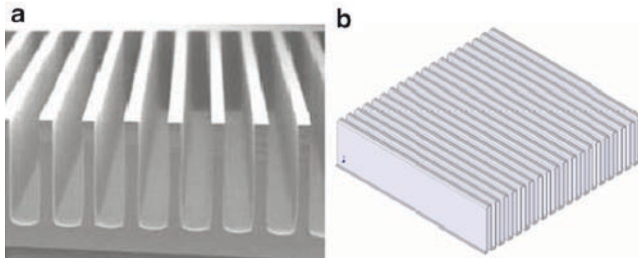


**Fig. 14.9** (**a**) Micro/minichannel, and (**b**) folded fin HSVRMs [50, 51]

Microprorous types of HSVRM structures provide higher values of surface area per unit volume than commonly used micro/minichannels. Porous structures can be ordered or un-ordered. Mesh and woven mesh structures shown in Fig. 14.10 are ordered porous structures. Woven mesh structures are made of metallic wires of defined diameter to produce parts of defined mesh numbers. These commercially available structures have been studied and reported in the heat transfer literature [53]. Mesh structures shown in Fig. 14.10 can be fabricated by mechanical, or wet-etching methods [54].

Metallic foams are the most common form of un-ordered microporous structures that have undergone thermal transport studies in the literature [55]. Open cell metal foams shown in Fig. 14.10 are created by a variety of methods including sintering, metal deposition by evaporation, CVD or electrodeposition. Metal sintering is the most cost-effective means of manufacturing metal foams. In this process, a polymeric foam substrate is coated with a slurry of metallic particles and is heated in a furnace. The polymer foam skeleton vaporizes and the metal particles sinter together leaving behind a metallic foam structure. The open-cell foams are generally compressed to a desired size for their application in heat exchangers.

Metal foams can also be created by electrodeposition. Indeed, the surface of area of electrochemically formed porous foam structure is several orders of magnitude higher than the other types of foams. Electrodeposition can easily create a 3-D dendritic structure. However, it is difficult to control the microstructure since trunks and branches in the porous dendritic structure are often unable to support the weight of numerous sub-branches. Shin et al. developed a technique of making self-supported nano-ramified deposits that involves electrodeposition accompanied by hydrogen evolution [56]. In this process, hydrogen bubbles function as a dynamic negative template. During the deposition, the growth of the dendritic copper structure was blocked by the hydrogen bubbles and they functioned as a

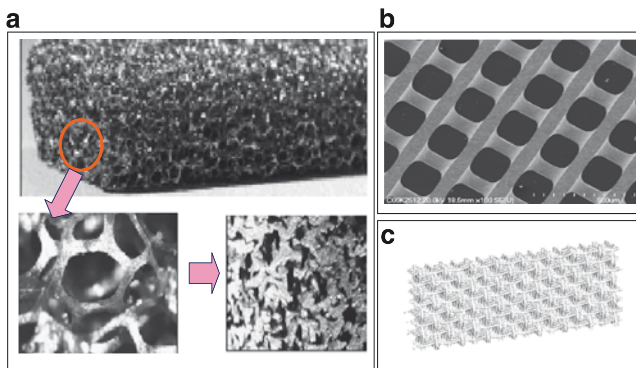


**Fig. 14.10** Microphotographs of porous HSVRMs [53–55]. (**a**) Metallic foam, (**b**) mesh structure, and (**c**) woven mesh structure

dynamic masking template during the deposition. The hydrogen bubbles depart from the surface, rise and merge into larger bubbles, and as a result, the pore size of the deposited copper structure increases with distance from the surface. The deposition process can be described as a competition between hydrogen evolution and coalescence away from the surface and metal deposition on to the surface. Using this technique, Shin et al. fabricated 3-D free-standing copper and tin foams with highly porous ramified (dendritic) walls. Figure 14.11 shows SEM photographs of porous copper deposits created by electrodeposition at different deposition times. The data indicted that the surface pore size increased with deposition time. Enhanced boiling heat transfer from nano-dendritic microporous copper structures was investigated by Furberg [57]. The study involved a detailed investigation of different fabrication parameters including current density, time, electrolyte concentration, additives, temperature and annealing. At low current density (<2 A/cm$^2$) the frequency and nucleation density of the hydrogen bubbles were low, resulting in a dense dendritic structure without any pores. At increasing current density (≥3 A/cm$^2$), the bubble population, frequency and coalescence increased to such an extent that the bubbles created permanent voids above the cathode and thereby functioned as a masking template, producing the desired structure. Longer deposition time and higher copper concentration in the electrolyte resulted in a thicker structure with larger pores.

Pore size and wall structure could be varied by using different additives. Hydrochloric acid, as an additive, considerably reduced the elementary branches in the structure thus influencing the pore shape. The influence of temperature on pore structure is shown in Fig. 14.12. The pore size increased considerably by increasing the electrolyte temperature from 20°C to 65°C. The dendritic branches comprised nano-sized grains between 10 and 20 nm. The electrical resistance decreased from 0.23 to 0.01 ohm after annealing at 500°C for 5 h [57].

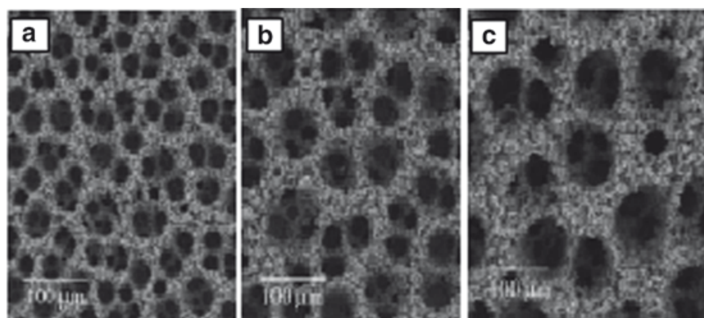


**Fig. 14.11** SEM photographs porous copper deposits at different deposition times of 5 s (**a**), 10 s (**b**), and 20 s (**c**). Ref. [56] Copyright Wiley-VCH Verlag GmbH & Co.KGaA. Reproduced with permission

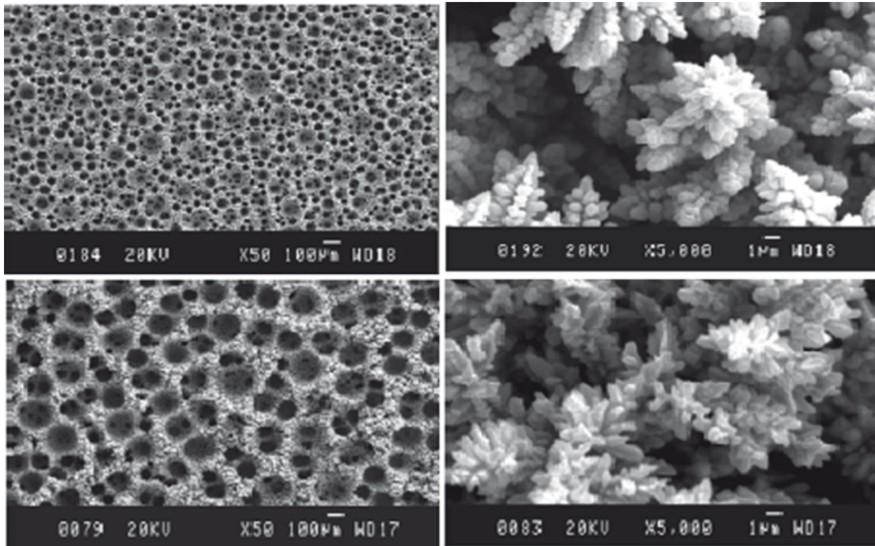


**Fig. 14.12** Electrodeposited micro-porous structures fabricated at 20°C (*top*) and at 65°C (*bottom*) electrolyte temperatures. Reproduced from ref. [57]

### *14.6.4 Nanowires for Thermoelectric Probes*

Thermoelectric temperature control systems are being used in an increasing number of applications. Typical applications of these systems are in thermal regulation of electronic enclosures, recirculating chillers for laser cooling, semiconductor process control and management of patient hypo- and hyperthermia. Thermoelectric coolers (TECs) are essentially solid state devices that pump heat against a temperature differential utilizing electrical energy. Based on the Peltier effect, each cooler consists of a matrix of thermoelectric p–n thermocouples connected electrically in series and thermally in parallel. Thermoelectric microprobes or arrays of such probes suitable for highly localized cooling and heating, in situ temperature sensing, and temperature control have potentially significant applications where thermal manipulation at micro/nano levels is required. A thermoelectric microprobe for temperature manipulation consists of an n-branch and a p-branch forming p–n junctions. When a current is supplied to the microprobe, the temperature will increase at one junction and decrease at the other. In order to be useful for the targeted applications, the thermoelectric microprobe or arrays must be from 500 to 750 μm tall.

Efficient thermoelectric devices require the use of high figure of merit thermoelectric materials. The thermoelectric figure of merit, ZT, can be expressed as $\alpha 2\sigma T/\kappa$, where $\alpha$ is the Seebeck coefficient, $\sigma$, the electrical conductivity, $T$, the temperature, and $\kappa$, the thermal conductivity. Among the various thermoelectric materials, bismuth telluride (Bi2Te3) has been the main focus of research because of its superior ZT near room temperature [58].

Bismuth telluride with the stoichiometric composition ratio ($Bi_2Te_3$) is electronically neutral. However, the common carrier of the bismuth telluride alloy can be modified by adjusting the percentage of tellurium or bismuth incorporated. If the alloy is telluride-rich, it can be n-type. In order to be p-type, the composition of the bismuth telluride alloy should be bismuth-rich instead of telluride-rich [59]. This is advantageous since the material deposition development can focus on a single material system which will yield both the n- and p-branches of the thermoelectric probes.

Yoo et al. studied the electrodeposition of n-type BiTe alloy thin films [60]. $Bi_xTe_y$ films were electrodeposited on a $Bi_2Te_3$ seed layer from an aqueous nitric acid bath at 23°C. The bath composed of 0 to 0.008 M $Bi^{3+}$ from $Bi(NO_3)_3$ and 0.01 M $HTeO_2^+$ from $TeO_2$ in 1 M $HNO_3$. The pH was maintained at pH 0.1, and a 1 μm thick $Bi_2Te_3$ seed layer was deposited on a $SiO_2$/Si wafer (lightly doped p-type) by rf sputtering. The film compositions, which varied from 57 to 63 at.% Te were strongly dependent on the deposition conditions. Surface morphologies varied from needle-like to granular structures depending on the deposited Te content. Electrical and thermoelectric properties of these electrodeposited $Bi_xTe_y$ thin films were measured before and after annealing and compared to those of bulk $Bi_2Te_3$. Annealing at 250°C in reduced hydrogen atmosphere enhanced thermoelectric properties by reducing film defects. In-plane electrical resistivity was highly dependent on composition and microstructure. In-plane Hall mobility decreased with increasing carrier concentration, while the magnitude of the Seebeck coefficient increased with increasing electrical conductivity to a maximum of −188.5 μV/K. The thermoelectric properties of electrodeposited n-type BiTe thin films after annealing were comparable to those of bulk BiTe films.

Theoretical analysis by Hicks and Dresselhaus indicated that ZT can be significantly enhanced by reducing the structural dimensions to a single dimension [61]. The analysis further showed that ZT for nano-wires will be significantly improved by decreasing the diameter. As a result, research into the fabrication and characterization of nano-wire structures of thermoelectric materials has received much attention in recent years [62–66].

Huang et al. used the LIGA(Lithographie Galvano Formung Abformung) process to fabricate bismuth telluride microposts of 150 μm diameter and heights up to 500 μm [62]. Bismuth telluride alloys were electrodeposited galvanostatically into microfeatures on a titanium substrate. The electrolyte was prepared by dissolving BiN and tellurium in nitric acid solution of zero pH. The monophasic BiTe alloy microposts had a polycrystalline structure with excellent adhesion to the substrate and good mechanical strength. By controlling the electrolyte composition and the current density either p- or n-type BiTe alloy microposts could be produced.

Synthesis of arrays of BiTe nano-wires by electrodeposition has been studied by different authors [63–66]. Li et al. employed pulsed electrodeposition into the nanochannels of porous anodized alumina membranes to fabricate nano-wire arrays of $Be_2Te_3$ [63]. The anodized alumina membrane with the pore sizes of about 40 and 60 nm were used. A 200 nm thick layer of Au film was sputtered onto one side of the anodized alumina membrane to serve as the working electrode in a two-electrode plating cell, and a graphite plate was used as the counter-electrode.

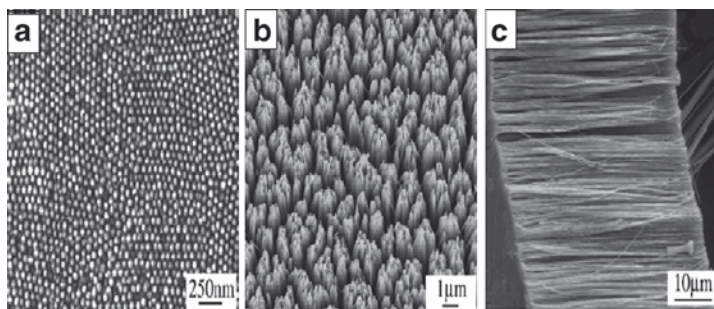


**Fig. 14.13** SEM photographs of the bismuth telluride array showing (**a**) bottom view, (**b**) surface view, and (**c**) cross sectional view respectively. Ref. [63] reproduced with permission of the IOP

$Bi_2Te_3$ nano-wire arrays were deposited under modulated voltage control and a potential of −1.3 V was applied between the two electrodes. During the pulse time, 3 ms, metal species were electrochemically reduced on the pore ground of the membrane. The delayed time, 10 ms, provided time for the recovery of the ion concentration. The electrolyte was prepared by dissolving 0.01 M $Bi(NO_3)_3 \cdot 5H_2O$ and 0.015 M $TeO_2$ in $HNO_3$ solution. The pH of the final electrolyte was adjusted to about 1 with $HNO_3$. High-filling-rate, highly oriented, and ordered $Bi_2Te_3$ nano-wire arrays could be thus fabricated. The $Bi_2Te_3$ nano-wires were single crystalline with a preferential orientation along the [015] direction. Optimum growth condition could be achieved by the proper choice of the pulsed parameters and the deposition potentials and ion concentrations in the electrolyte in Fig. 14.13. The electrical transport measurements showed that the $Bi_2Te_3$ nano-wires with the diameters between 40 and 60 nm exhibited typical semiconductor behavior, and the 40 nm nano-wires have lower resistance sensitivity to temperature than the 60 nm nano-wires. Similar studies were conducted by Sanders et al., who employed DC electrodeposition into porous anodic alumina template to fabricate nano-wire arrays of $Bi_2Te_3$ [64]. Purkayastha et al. developed a template-free method to synthesize rod-shaped rohmbohedral nanocrystals of bismuth telluride [65]. Menke et al. prepared polycrystalline bismuth telluride using step edge selective cyclic electrodeposition on highly oriented pyrolytic graphite surfaces [66]. Control of the number of cathodic/anodic scans allowed the diameter of bismuth telluride to be varied between 100 and 300 nm.

## 14.7 Concluding Remarks

This chapter provided a brief description of the current trends in microelectronic packaging technologies and some examples of the role of nanotechnology in the advancement of packaging materials and microelectronic packages. The discussion was mostly limited to topics that highlighted the impact of electrochemical processing

in microelectronic packaging. Dual Damascene plating for Cu chip metallization and electroplated C4 technology have enabled a paradigm shift in semiconductor packaging. As the industry moves to 45 node technology, implementation of electropolishing-based planarization and electroless-capped layer in manufacturing are the key challenges for the next generation of chip interconnects. Future planarization efforts are expected to focus on the development of integrated electropolishing method for barrier layer removal and elimination of final CMP process. Several different approaches are expected to evolve to address electromigration issues in chip and chip-package interconnects. In the chip-package interconnection arena, the current focus is on the development of low melting temperature, Pb-free flip-chip technology. Some other packaging trends include the use of novel materials for packages and boards with improved compliance and CTE mismatch and advanced approaches to heat dissipation.

While micro-scale technologies are expected to continue to thrive, nano-processing and nano-materials are already playing a key role in the advancement of microelectronic packaging. Steady miniaturization of silicon devices and interconnects has been possible due to smooth integration of nano-processing with conventional micro-scale processing. An enormous amount of exciting research is currently underway in the area of nano-technology that is expected to shape the next generations of electronic packages. Indeed, due to their high surface to volume ratio, nano-materials have the ability to revolutionize the packaging materials. A brief description of such applications has been presented, examples of which include: the use of nano-particles to influence thermo-mechanical properties of solders, adhesives, and packaging materials; the use of carbon nano-tubes, nano-fibers and their metallic composites for advanced chip interconnects and thermal interface materials; fabrication of porous nano-structures and development of nano-fluids for advanced cooling systems; ink-jet printing for low-cost printed electronics; and precise fabrication of n- or p-type nano-films and nano-wires for application in thermo-electric coolers. In summary, nano-materials and nano-processing are expected to address the key issues related to continued miniaturization and increased performance of next generation of microelectronic packages.

## References

1. Romankiw LT, Croll I, Hatzakis M (1970) IEEE Trans Magn 6:729
2. Romankiw LT (1997) Electrochim Acta 42:2985
3. Osaka T (1997) Electrochim Acta 42:3015
4. Datta M, Landolt D (2000) Electrochim Acta 45:2535
5. Datta M (2003) Electrochim Acta 48:2975
6. Rymaszewski EJ, Tummala RR, Watari T (1997). In: Tummala RR, Rymaszewski EJ, Klopfenstein AG (eds) Microelectronic packaging handbook, part I, 2nd edn. Chapman and Hall, New York
7. Tummala RR, Garrou P, Gupta T, Kuramoto N, Niwa K, Shimda Y, Terasawa M (1999). In: Tummala RR, Rymaszewski EJ, Klopfenstein AG (eds) Microelectronic packaging handbook, part II, 2nd edn. Kluwer Academic Publishers, Boston

8. D.P. Seraphim, D.E. Barr, W.T. Chen, G.P. Schmitt, and R.R. Tummala (1997). In: Tummala RR, Rymaszewski EJ, Klopfenstein AG (eds) Microelectronic packaging handbook, part III, 2nd edn. Chapman and Hall, New York
9. Datta M (2005). In: Datta M, Osaka T, Schultze WJ (eds) Microelectronic packaging, CRC Press, pp 3–27
10. Edelstein DC (1997). Tech Dig IEEE Intl electron devices conference, 773, 1997; IBM Res Mag, No. 4, 16
11. Datta M. In: Krongleb S, Bonhote C, Osaka T, Kitamoto Y (eds) Proceedings, 8th Intl. symposium on magnetic materials processes and devices, Electrochem Soc, NJ, PV2004-23, pp 126–143
12. Basol BM (2004) J Electrochem Soc 151:C765–C771
13. Hu C, Gignac L, Rosenberg R, Liniger E, Rubino J, Sambucetti C, Domenicucci A, Chen X, Stamper AK (2002) Appl Phys Lett 81:1782–1784
14. Dubin VM, Lopatin S, Kohn A, Petrov N, Eizenberg M, Shacham-Diamand Y (2004). In: Datta M, Osaka T, Schultze WJ (eds) Microelectronic packaging, CRC Press, pp 65–110
15. Kohn A, Eizenberg M, Shacham-Diamand Y, Israel B, Sverdlor Y (2001) Microelectronic Eng 155:297–303
16. Nakano H, Itabashi T, Akahoshi H (2005) J Electrochem Soc 152(3):C163–C166
17. Moon P, Dubin V, Johnston S, Leu J, Raol K, Wu C (2003). Proc IEDM, IEEE Intl, pp 35.1.1–35.1.4
18. Hu C, Gignac L, Liniger E, Herst B, Rath DL, Chen ST, Kaldor S, Simon A, Wang W-T (2003) Appl Phys Lett 83:869
19. Lee B, Ivanov I (2009). In: Shacham-Diamand Y, Osaka T, Datta M, Ohba T (eds) (2009) Advanced nanoscale ULSI interconnects: fundamentals and applications, Springer
20. Datta M (2004). In: Datta M, Osaka T, Schultze WJ (eds) Microelectronic packaging, CRC Press, pp 167–200
21. Datta M, Shenoy RV, Jahnes C, Andricacos PC, Horkans J, Dukovic JO, Romankiw LT, Roeder J, Deligianni H, Nye H, Agarwala B, Tong HM, Totta PA (1995) J Electrochem Soc 142:3779
22. Gruber PA, Belanger L, Brouillete GP, Danovitch DH, Landreville JL, Naugle DT, Oberson VA, Shi DY, Tessler CL, Turgeon MR (2005) IBM J Res Dev 49(4/5):621
23. Gruber PA, Budd RA, Buchwalter SL, Shi DY, Busby JA, Grant JJ, Giri AP, Knickerbocker SH, Longworth HP, Naugle DT. Abstract #1634, 120th ECS meeting, Oct. 29–Nov. 3, 2006, Cancun, Mexico
24. Datta M, Emory D, Huang T-L, Joshi SM, King CA, Ma Z, Marieb T, McKeag M, Suh D, Yang S. US Patent No. 6,740,427, May 25, 2004
25. Datta M, Emory D, Joshi S, Menezes S, Suh D. US patent no. 6,853,076, February 8, 2005
26. Moon P, Zhiyong Ma, Datta M. US patent no. 6,703,069, March 9, 2004
27. Pecht MG, Nguyen LT (1999). In: Tummala RR, Rymaszewski EJ, Klopfenstein AG (eds) Microelectronic packaging handbook, part II, 2nd edn. Kluwer Academic Publishers, Boston
28. Breedis JT (1986). J Metals AIME 48
29. Van Tiburg GC (1984) Plat Surf Finish 71(6):78
30. Houma H, Mizushima S (1984) Met Finish 82(1):47
31. Schelling PK, Shi L, Goodson KE (2005). Materials Today, 30–35
32. Parasher RS, Chang J-Y, Sauciuc I, Narasimhan S, Chou D, Chrysler G, Myers A, Prstic S, Hu C (2005). Intel Technol J 9(04)
33. Datta, M, Lin E, Choi H, McMaster M, Brewer R, Werner D, Hom J, Upadhya G, Gopalakrishnan S, Rebarber F (2007). Transactions of the Electrochemical Society, 6(8): 13–31
34. Brewer R, Upadhaya G, Zhou P, McMaster M, Tsao P. US patent # 7,188,662, March 13, 2007
35. Wei BQ, Vajtai R, Ajayan PM (2001) Appl Phys Lett 79(8):1172–1174
36. Collins PG, Hersam M, Arnold M, Martel R, Avouris Ph (2001) Phys Review Lett 86(14):3128–3131

37. Kreupl F, Graham AP, Duesberg GS, Steinhogl W, Lieban M, Unger E, Honlein W (2002) Microelectronic Eng 64:399–408
38. Li J, Ye Q, Cassell A, Ng HT, Stevens R, Han J, Meyyappan M (2003) Appl Phys Lett 82(15):2491–2493
39. Ngo Q, Cruden BA, Casselle AM, Sims G, Meyyappan M, Li J, Yang CY (2004) Nano Lett 4(12):2403–2407
40. Arai S, Endo M (2004) Electrochem Solid State Lett 7(3):C25–C26
41. Dubin VM (1992) J Electrochem Soc 139:633
42. Li J, You S, O'Keefe MJ, O'Keefe TJ (2006) J Elecrochem Soc 153(10):C722–C727
43. Lee H-Y, Duh J-G (2006) J Electronic Met 35(3):494–503
44. Shen J, Liu YC, Han YJ, Gao HX (2006) J Electronic Metals 33(8):1672–1679
45. Xu J, Fisher TS (2006) Int J Heat Mass Transf 49:1658–1666
46. Eastman JA, Choi SVS, Li S, Yu W, Thompson LJ (2001) Appl Phys Lett 78(6):718–720
47. Xuan Y, Li Q (2000) Int J Heat Fluid Flow 21:58–64
48. Marquis FDS, Chibante LPF (2005). JOM 57(12):32–43
49. Butler P (2006) The packaging professional. 6–7
50. Tuckerman DB, Pease RFW (1981) IEEE Electron Dev Lett 2(5):126–129
51. Kandilkar SG, Grande WJ (2003) Heat Transf Eng 24(1):3–17
52. Marthinuss J, Hall G (2004). Electronics Cooling
53. Park JW, Ruch D, Wirtz RA. American Association of Aeronautics and Astronautics, AIAA, 2002-0208, 1–9
54. Datta M, McMaster M, Brewer R, Zhou P, Tsao P, Upadhaya G, Munch M. Patent pending
55. Boomsa K, Poulikakos D, Zwick F (2003) Mech Mater 35:1161–1176
56. Shin H-C, Dong J, Liu M (2003) Adv Mater 15(19):1610–1614
57. Furberg R (2006) Enhanced boiling heat transfer from a novel nano-dendritic microporous copper structure, licentiate thesis, KTH School of Industrial Engineering & Management, Department of Energy Technology, Stockholm
58. Rowe DM (1995) CRC handbook of thermoelectrics. CRC Press, London
59. Yim WM, Rosi FD (1972) J Solid State Electron 15:1131–1140
60. Yoo BY, Huang C-K, Lim JR, Herman J, Ryan MA, Fleurial J-P, Myung NV (2005) Electrochim Acta 50:4371–4377
61. Hicks LD, Drwsselhaus MS (1997) Phys Rev B47:631
62. Huang L, Wang W, Murphy MC (1999) Microsystem Technol 6:1–5
63. Li L, Yang Y, Huang X, Li G, Zhang L (2006) Nanotechnology 17:1706–1712
64. Sander MS, Prieto AL, Gronsky R, Sands T, Stacy AM (2002) Adv Mater 14(9):665–667
65. Purkyastha A, Lupo F, Kim S, Borca-Tasciuc T, Ramnath G (2006) Adv Mater Des 18:496–500
66. Menke EJ, Li Q, Penner RM (2004) Nano Lett 4(10):2009–2014