Chapter 9
Reliability of Electronic Assemblies Under Mechanical Shock Loading

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9.1 Introduction

Reliability of portable electronic devices is becoming an important factor of success in the highly competitive global markets due to the fact that increasing heat dissipation, current densities and mechanical loadings of power components make electrical interconnections more vulnerable to failures. Portable electronic products encounter diverse environments in ordinary daily use and therefore their reliability should be studied with tests that simulate real-use strains and stresses as realistically as possible. Portable electronic products are exposed to temperature fluctuations due to either internally generated heat dissipation or the external operational environment, but they are especially prone to failure due to mechanical shock loads caused by accidental drops. These loadings are simulated with standardized reliability tests that also allow comparative studies of different material combinations.

The usage of lead-free solders, components under bump metallizations (UBM) or lead metallizations, and printed wiring board (PWB) protective coatings add to the complexity of the interconnection metallurgies. The number of different material combinations increased markedly as the traditionally used SnPb-based solders and protective coatings were replaced with different lead-free alternatives. Because microstructures significantly affect the reliability of soldered interconnections, reliability of each material combination is likely to be different. For these reasons, more extensive and comprehensive reliability testing of new products has become ever more important.

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Because reliability of electronic assemblies is chiefly determined by the ability of electrical interconnections to withstand various loadings during products' operational lifetime, it is of primary importance to investigate systematically metallurgical reactions in the effective joining region and the resulting microstructures within the solder interconnections. Lead-free solder interconnections can contain more complex intermaterial layers such as phosphides, which can markedly weaken solder interconnections. Moreover, the microstructures formed during soldering are not stable and will evolve during the operation of products. Hence, in order to ensure the best possible reliability of electronic assemblies against various loading conditions, much better understanding of interconnections microstructures, including interfacial reaction products, and their evolution is needed.

9.2 Effect Loading Rate on the Reliability of Solder Interconnections

Portable electronic equipment experiences during their use many different kinds of loading conditions, in which mechanical shocks and thermomechanical loadings are perhaps the most critical ones. These two fundamentally different loading conditions will evoke different failure mechanisms leading to dissimilar failure modes. Under thermomechanical loading, nucleation and propagation of cracks are controlled by the microstructures formed during soldering and their recrystallization behavior during use [1–5]. Mechanical shock impacts, on the other hand, are known to produce entirely different kinds of failure modes [6–13]. Cracks in the newly soldered interconnections do not propagate through the bulk solder of the interconnections, but mainly in the brittle intermetallic compound layers formed between solder and contact metallizations [4, 5, 7].

Several studies carried out with commercial portable electronic products have shown that impact forces generated when products are dropped onto the ground are transmitted through the product casing to the component boards and make the boards bend and vibrate excessively. The results from product-level tests have been used to develop board-level drop tests [14]. For example, JEDEC has published the JESD22-B111 board-level drop test standard for handheld electronic products.

The drop tester is composed of a mechanism to drop the board repeatedly in a specified orientation and a high-speed data acquisition system to record deceleration, strains on the component boards and the number of drops-to-failure. The condition B of the JESD22-B111 standard defines the deceleration pulse that has the shape of a half-sine with 0.5 ms width and the maximum at 1500 G. The shape of the deceleration pulse is not only a function of the drop height but depends on the characteristics of the strike surface: drop height determines the maximum deceleration and strike surface the pulse width.

The standardized layout of the test board along with its dimensions is presented in Fig. 9.1. The test board is attached horizontally on a fixture, and the components

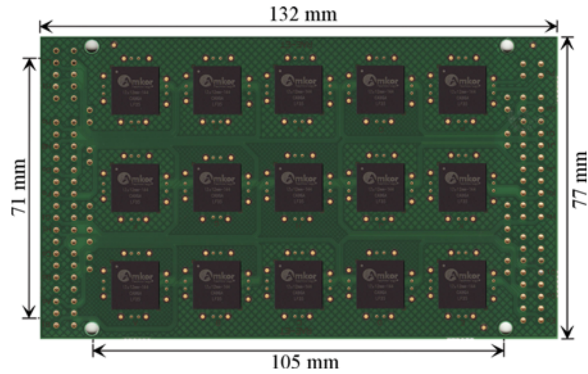

Fig. 9.1 Layout and dimensions of the drop test board

are facing downward during the test (Fig. 9.2b). The fixture is mounted on a sledge that is dropped down on a rigid surface from a specified height in a controlled manner with the help of guiding rails (see Fig. 9.2a). This is because the most detrimental factor for the assembly caused by dropping is not the mechanical shock itself, but the subsequent bending and vibration of the board [13, 15]. Placing the component boards horizontally achieves maximum flexure of the board and onsets the natural vibrating motion. Bending causes displacement between the board and the components resulting in component, interconnection, or board failures. The drop test can be considered an accelerated test because the test structure lacks the support provided by product casings and other adjacent structures and, therefore, during testing the test board experiences larger than real-use bending amplitudes.

Since the component board is allowed to bend freely at the shock impact, there are numerous different modes in which it can bend. The natural mode of the component board describes the shape in which the board bends, and the natural frequency describes how fast the bending takes place. Figure 9.3 shows three of the most significant natural modes of the JESD22-B111 compliant test board and their associated natural frequencies. Each of these natural modes vibrates at a characteristic frequency, and the total bending and frequency of the component board is their sum since the different natural modes act simultaneously. The shapes of the natural modes depend on the support structure of the component board, whereas the natural frequencies depend on the stiffness and mass of the component board. The natural modes with highest frequencies are usually not of great importance because their amplitude is relatively small and vibrations are attenuated quickly. Only the lowest frequencies, in the case of the JESD22-B111 board the lowest three, can be considered significant. Owing to the simultaneous action of many different natural modes and frequencies, and the fast attenuation of the vibration amplitude, the strain distribution on the test board changes very rapidly. Thus, the location of the highest stress changes quickly also. Figure 9.4 shows the longitudinal strain measured in the middle of the board layout on the opposite side of the board from the components. Figure 9.4a shows how the strain develops after the drop impact. The macroscopic oscillation is due to the natural mode with the

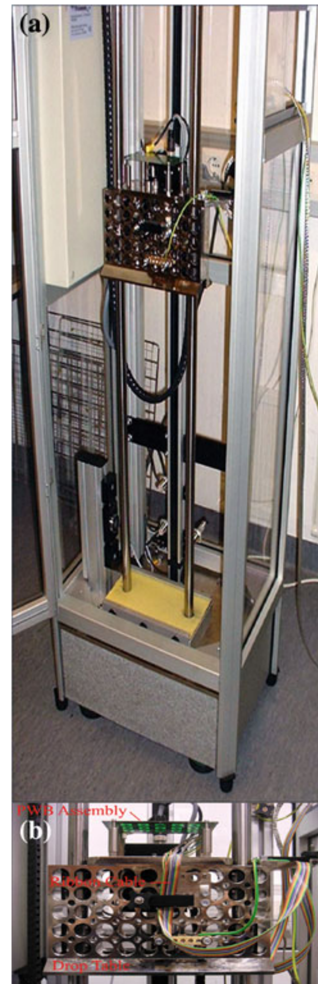

Fig. 9.2 JESD22-B111 compliant drop tester: **a** Structure of the tester, **b** Test board is attached from the four corners on a support pins and components are facing downward

lowest frequency. Oscillations at higher frequencies are embedded in the larger strains. The strains due to natural modes with higher frequencies are shown in Fig. 9.4b, which presents only the 0–5 ms time interval from Fig. 9.4a.

The failure mechanism under mechanical shock loading differs greatly from that under thermomechanical loading, where the localized recrystallization of the interconnections enables the nucleation and propagation of cracks in the bulk solder [1–5]. Besides temperature the most important difference between drop tests and thermal cycling tests is the deformation rate. The drop tests are typically carried out at room temperature ($\sim$295 K), which is relatively high (0.6 T_m) when compared to the melting point of the solder ($\sim$500 K). At such high (homologous) temperatures, the plastic behavior of the solder is strongly strain-rate dependent. As shown in Fig. 9.5, the solder becomes remarkably stronger as the strain rate

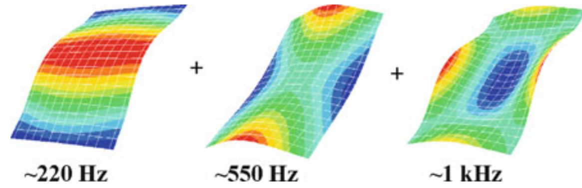

Fig. 9.3 Total flexure of the test board is the sum of the different natural modes. Three of the most significant natural modes of the JESD22-B111 compliant test board. *Different shades* of *gray* represent vertical displacement [15]

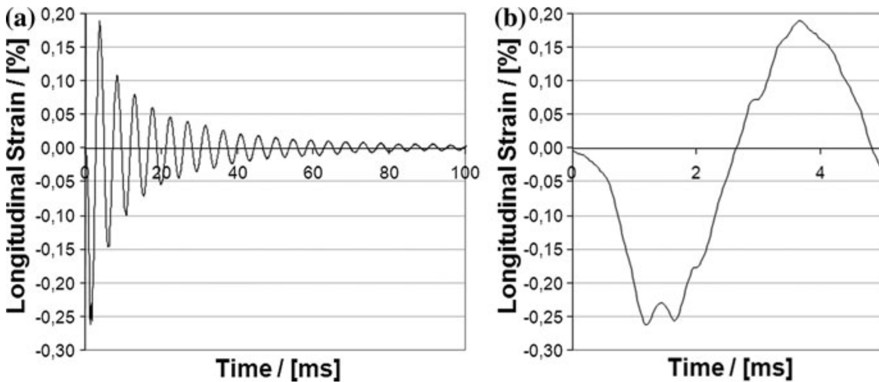

Fig. 9.4 Measured longitudinal strain at the center of the board

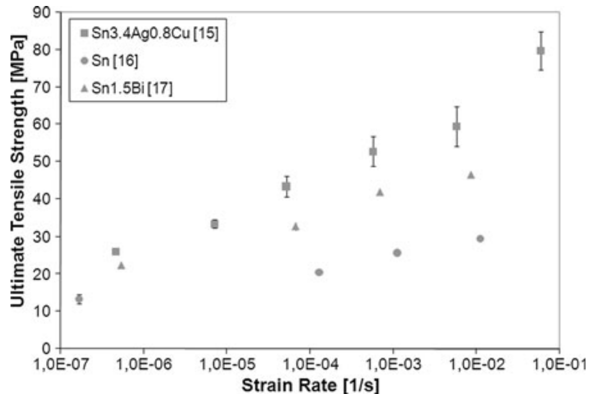

Fig. 9.5 Effect of strain rate on strength of Sn and two Sn-based solders [16–18]

increases from that used in thermal cyclic tests ($\sim 10^{-6}$–10^{-5} 1/s) to that used in drop tests ($\sim$1–10 1/s). As can be seen, the flow stress of solder is about two to three times as high when the strain rate is increased from that occurring in thermal cycling to that occurring in drop tests. Both the ultimate tensile strength and the yield strength increase with strain rate, but the yield stress is typically even more

strain-rate sensitive. Subsequently, the magnitudes and distributions of the stresses in the solder interconnections are different under thermal cycling and drop test conditions. Our finite element calculations have shown that as the strain rate increases not only stresses in solder interconnections increase but also they become more concentrated on the component side edges of the interconnections [6, 15]. Due to the much higher flow stress of the solder interconnections in the drop tests, the intermetallic compound layers will experience significantly higher stresses than those in thermal cycling. The same calculations showed that stresses at the solder|pad interface on the PWB side are less than half of that on the component side. The tensile strength of the solder increases above the fracture strength of the IMC, and this ultimately makes the fractures propagate inside the IMC layers, instead of the bulk solder. In thermal cycling, where the strain rates are relatively low, the cyclic thermomechanical loading of the interconnections generates plastic deformation, which ultimately leads to propagation of fatigue fracture through the solder interconnections.

9.3 Reliability of Lead-Free CSPs under Mechanical Shock Loading

In this study, the drop reliability of high-density electronic assemblies was studied by applying standardized JESD22-B111 test procedure for test vehicles that represent the technologies and lead-free materials typically used in portable electronic products. A large number of component boards were assembled in a full-scale production line to enable proper statistical and fractographic analyses. The test boards were assembled with different printed wiring board protective coatings, component under bump metallizations and solder pad structures. The component boards were drop tested and the times-to-failure of the various combinations were statistically analyzed.

The component used was a lead-free Sn0.2Ag0.4Cu (wt%)-bumped chip scale packaged (CSP) component with 144 bumps (500 μm in diameter) and bump pitch of 800 μm (denoted CSP144 in the following). The height of the bumps was 480 μm and the under bump metallurgy consisted of a ~0.6–0.8 μm-thick-electrochemical Ni, on top of which there originally was a thin gold layer before bumping. The structure of the component and materials used are shown in Fig. 9.6. The PWB was a double-sided (1 + 6 + 1) stack-up multilayer FR4 board with six inner copper layers in addition to the topmost resin-coated copper layers. The component boards for the drop tests were designed according to the JESD22-B111 drop test standard. The pad and conductor patterning on the board was the same on the two sides except that one side of the board had microvias in all of the soldering pads and the other did not. The PWBs were manufactured with either electroless Ni plating containing about 9 wt% (16 at%) P with flash Au finish on top (denoted Ni(P)|Au) or organic solderability preservative (denoted Cu|OSP) protective

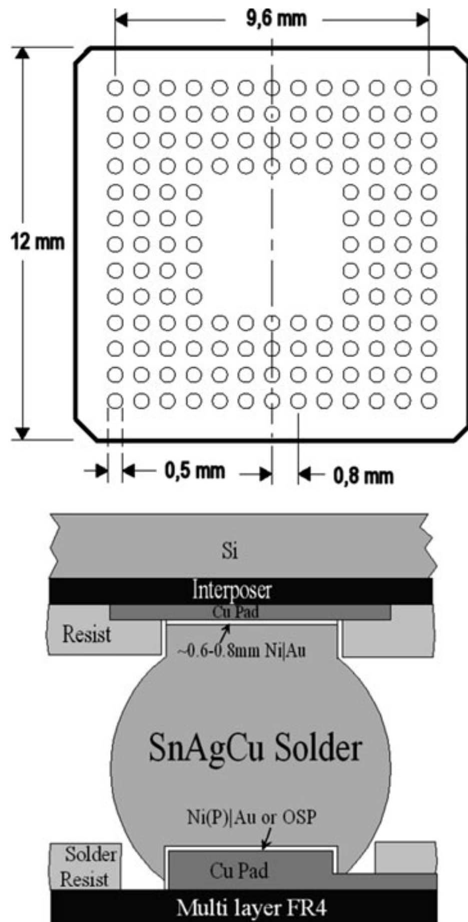

Fig. 9.6 Structure and dimensions of the CSP144 component

coating on the Cu soldering pads. The test boards were assembled by using the Sn3.8Ag0.7Cu solder paste. Although the board was double-sided, components were mounted on the non-microvia side only. The drop height was set to 82 cm in order to achieve the required peak deceleration of 1500 G for the duration of 0.5 ms (half-sine pulse). A failure was recorded when the resistance through the daisy chain network exceeded the 1.0 kΩ threshold resistance for more than 200 ns three times in a sequence of five drops.

Figure 9.7 presents the average drops-to-failure of the different material combinations of the experimental design. The significance of the differences between the material combinations was studied with the nonparametric Wilcoxon Rank-Sum Test (the numerical data failed the Shapiro–Wilk test for normality). The effect of both the factors, the *PWB coating* and the *component side metallization*, was statistically significant: the copper metallization on the component side was

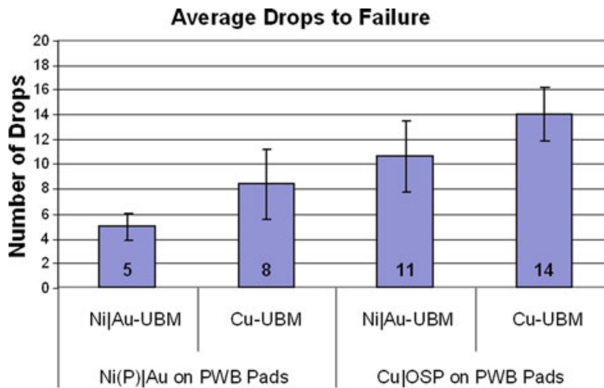

Fig. 9.7 Average drops-to-failure of the different material combinations with respective standard deviations

more reliable than the electrochemical nickel ($\alpha = 4.7\%$) and, on the PWB side the Cu|OSP was more reliable than the Ni(P)|Au ($\alpha = 0.2\%$).

The Weibull characteristic life times (η) of the Ni|Au-metallized and Cu-metallized components on the Ni(P)|Au-coated PWBs were 6 and 10 drops, respectively, while those on the Cu|OSP-coated PWBs were 12 and 16, respectively. Similarly the shape parameters (β) of the Nu|Au-metallized and Cu-metallized components on the Ni(P)|Au-coated PWBs were 1.7 and 1.5, respectively, while those on the Cu|OSP-coated PWBs were 1.9 and 3.7, respectively.

The primary failure modes identified at the failure analysis stage were different from those typically observed after the thermal cycling tests with similar components and the same lead-free materials [1, 3]. In addition, the modes were also different between the interconnections on the Ni(P)|Au and the Cu|OSP. The solder interconnections on the Cu|OSP-coated PWBs failed at the component side, where cracks propagated through the $(Cu,Ni)_6Sn_5$ or the Cu_6Sn_5 reaction layer depending on the component under bump metallization: Cu_6Sn_5 on the copper under bump metallization (see Fig. 9.8) and $(Cu,Ni)_6Sn_5$ on the Ni|Au metallization (see Fig. 9.9). (In the case of Cu-UBM, there should thermodynamically be a layer of Cu_3Sn between the Cu and the Cu_6Sn_5 but the thickness of the Cu_3Sn layer is too small to be observed in the images). Interconnections on the Ni(P)|Au failed from the PWB side interface, where cracks propagated between the $(Cu,Ni)_6Sn_5$ and the Ni(P) metallization (see Fig. 9.10). Cracks in the Cu|OSP interconnections typically nucleated at the corner of the interconnections, a varying distance away from the intermetallic compound (IMC) layers in the bulk solder (see e.g. Figs. 9.8, 9.9), but jumped very quickly into the IMC layers, which obviously provided a more favorable path for the crack to propagate due to the brittle nature of the compound. The fractures in the Ni(P)|Au interconnections propagated very close to the nickel metallizations underneath the $(Cu,Ni)_6Sn_5$ intermetallic layer, as shown in Fig. 9.10.

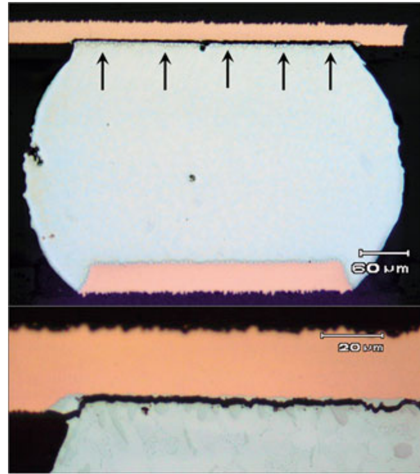

Fig. 9.8 The primary failure mode of the Cu-UBM interconnections on the Cu|OSP-coated PWBs

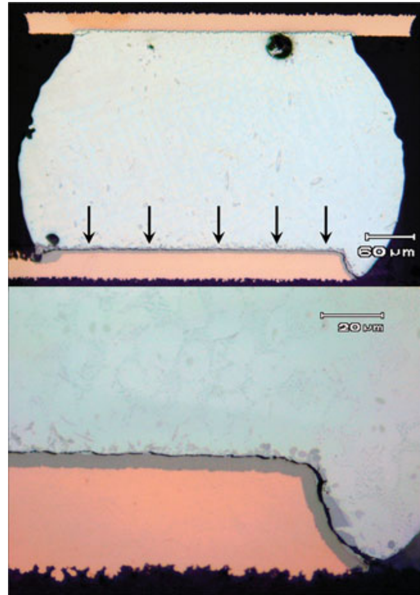

Fig. 9.9 The primary failure mode of the Ni-UBM interconnections on the Cu|OSP-coated PWBs

Fig. 9.10 The primary failure mode of the Cu-UBM as well as the Ni|Au-UBM interconnections on the Ni(P)|Au-coated PWBs

No recrystallization was observed in the drop-tested samples, even after several months of storage at room temperature. This is most likely because during drop testing the strength of the solder interconnections increases and the solder does not markedly deform plastically. As the strain rate is increased twinning mechanism is activated. Twins are typically observed in the regions of the interconnections where stresses are highest.

Despite the fact that the stresses at the PWB side interfacial regions of the interconnections are much smaller than at the component side [6, 15], the primary failure mode for the interconnections soldered on Ni(P)|Au was a fracture on the PWB underneath the $(Cu,Ni)_6Sn_5$ intermetallic layer. This emphasizes the weak nature of this interface. The fracture typically propagated completely through the solder interconnections at a single or very few impacts. The fracture path was always very smooth and straight, when compared with the Cu|OSP interconnection fractures discussed earlier.

9.4 Effects on Small Additions of Ni in the SnAgCu solder and in the Drop Reliability of BGA Component Boards

At the dawn of the adoption of the lead-free electronics manufacturing legislation (RoHS) at the EU region, compositions of the currently used lead-free solder alloys were decided mainly on the basis of their ability to replace the eutectic Pb-containing solder alloys in the existing assembly processes. However, recently the emphasis of research and development work has shifted toward the reliability issues related to the newly adopted compositions. Reliability improvements have been sought by modifications of the microstructures and mechanical properties of the near-eutectic SnAgCu solders by adding minor elements and optimizing their compositions. In addition to Ni, the effects of elements such as Co, In, Sb and Zn have been investigated [19].

As discussed earlier, the increased strength of solder interconnections caused by the strain-rate hardening under fast deformation rates is perhaps the most important reason for the increase in stresses at the interfacial regions of the solder interconnections above the fracture strength of the intermetallic layers (cracking of the interfacial layers) [4, 7]. Silver is know to be a very effective strengthener of tin, and the yield strength of the alloy increases with increasing silver content [20, 21]. Therefore, lower strength of low-silver SnAgCu alloys (lower than the about 3.5 wt%) may be advantageous for drop reliability because it allows plastic deformation of the solder interconnections and, thereby, the maximum stresses near the intermetallic layers are smaller. Furthermore, modifications of the intermetallic layers, for example by the introduction on minute amounts of nickel in the SnAgCu solders, can change the morphology and properties of interfacial reaction layers and, thereby, change their performance under reliability tests. It has recently been observed that very small addition of nickel, even below 0.1 wt%, in the SnAgCu alloy can retard the growth of the initially very thin layer of Cu_3Sn [20–23].

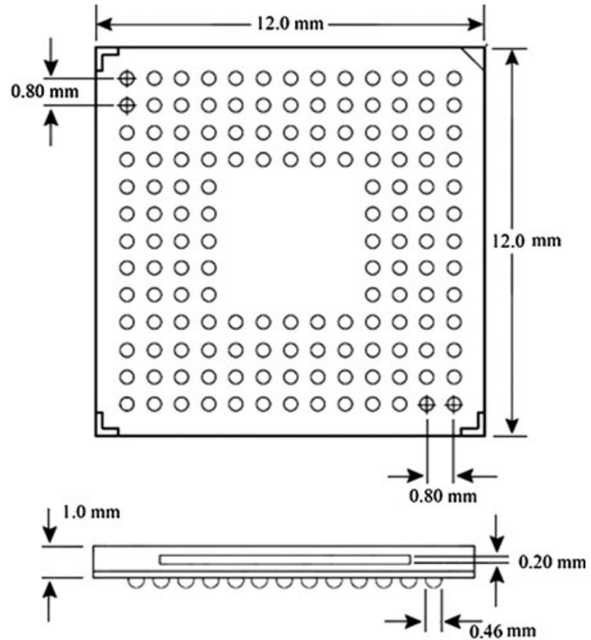

Fig. 9.11 Layout and dimensions of the component

Therefore, drop reliability of the CSP/BGA component boards soldered with different interconnections compositions was investigated. The commonly used near-eutectic SnAgCu solder alloy (Sn3.1Ag0.5Cu) was compared to the reliability of the component boards that were soldered with a low-silver nickel containing SnAgCu alloy (Sn1.1Ag0.5Cu0.1Ni). The reliability was studied by applying the JESD22-B111 drop test standard (condition B: 1500 G with 0.5 ms pulse width and the single component on board configuration). The component used in this study was a 12 mm × 12 mm chip scale sized BGA with 144 bumps, the pitch of 0.8 mm and a bump diameter of 0.5 mm (see Fig. 9.11). The component was bumped with either Sn3.0Ag0.5Cu (SAC305) or Sn1.2Ag0.5Cu 0.05Ni (LF35). There was no under bump metallization between the solder bumps and copper pads of the component. The printed wiring board (PWB) layout was designed according to the JESD22-B111. The copper soldering pads of the PWBs (1 + 6 + 1 build-up FR4) were coated with organic solderability preservative (Cu|OSP).

The two different interconnection compositions were formed by using different commercial solder pastes: (a) the SAC305-bumped components were reflow solder with the Sn3.8Ag0.7Cu to form the Sn3.1Ag0.5Cu and (b) the LF35-bumped components with the Sn0.7Cu0.1Ni to form the Sn1.1Ag0.52Cu0.01-0.1Ni after reflow compositions of the solder interconnections. The after reflow nominal composition of the interconnections was calculated by assuming complete filling of the stencil openings, perfect paste release from the stencil, and mixing of the bump and paste material volumes during the soldering. The component boards

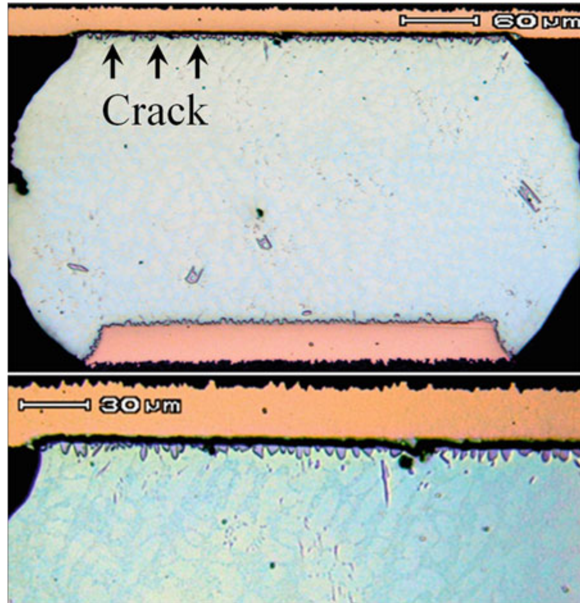

Fig. 9.12 Primary failure mode of the SnAgCu solder interconnections

were given a second reflow in order to give all test boards the same reflow treatment before testing. All together 46 component boards (23 replications of each interconnection compositions) were drop tested.

The reliability of the component boards was dependent on the solder composition. The average number of drops-to-failure of the component boards with the SnAgCu solder interconnections was 53 drops while that of the component boards with the SnAgCuNi interconnections was 71 drops. The SnAgCuNi solder interconnections are more reliable than the SnAgCu interconnections at 9.3% risk level (Wilcoxon Rank-Sum Test). The failure analysis of the drop-tested component boards revealed that the SnAgCu interconnections failed by cracking of the component side intermetallic layers, where cracks propagated inside the Cu_6Sn_5 intermetallic compound layer, as shown in Fig. 9.12. The primary cracks, i.e. the cracks that had failed the components electrically, had nucleated and propagated on the component side, while only some secondary cracks (cracks that do not cause electrical failures) were observed at the PWB side of the solder interconnection.

The SnAgCuNi interconnections, on the other hand, failed by cracking of the copper traces at the edge of the soldering pads on the PWB side of the interconnections. The copper traces had failed at the vicinity of the corner interconnections as shown in Fig. 9.13. Figure 9.14 shows a secondary failure mode, cracking of the bulk solder that was characteristic only to the low-silver, nickel containing interconnections. They were not observed to have caused electrical failures, and cracking of interfacial intermetallic layers was not observed in any of the SnAgCuNi solder interconnections.

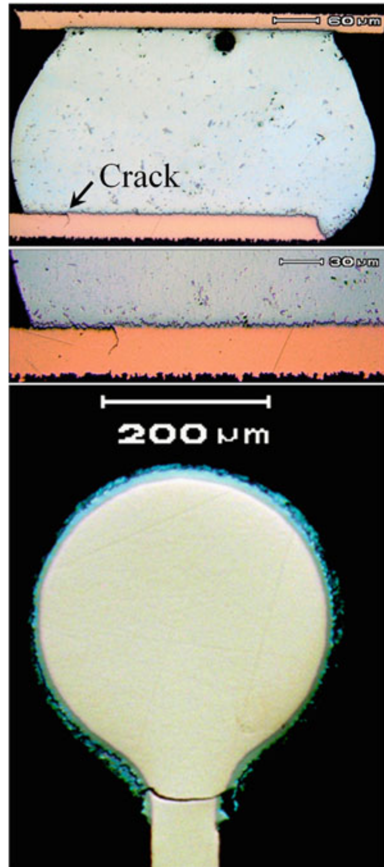

Fig. 9.13 Primary failure mode of the SnAgCuNi solder interconnections

The interfacial intermetallic layers were inspected with the help of the polarized light microscopy. Polarized light images make individual grains visible by showing grains in different grain orientations in different colors (asymmetric crystal structures have different refraction indices in different crystal directions and, therefore, cross-sections of grains in different orientation are seen in different colors when the reflected plane polarized light is cross-polarized). The micrographs in Fig. 9.15 show distinct differences in the morphology of the reaction layers. The interfacial reaction between the SnAgCu solder and copper pads forms a two-layered structure: Cu|Cu_3Sn|Cu_6Sn_5|solder. The Cu_3Sn layer in the SnAgCu interconnections (see Fig. 9.15) is clearly visible but not distinguishable in the SnAgCuNi interconnections. It seems that the nickel addition has not to have affected the total thickness of the reaction layers considerably but the grain size is notably reduced and the reaction layers are, consequently, much more uniform. The scallop-shaped morphology has changed to more granular-type morphology. It should be noted that in the case of the SnAgCu interconnections cracking took

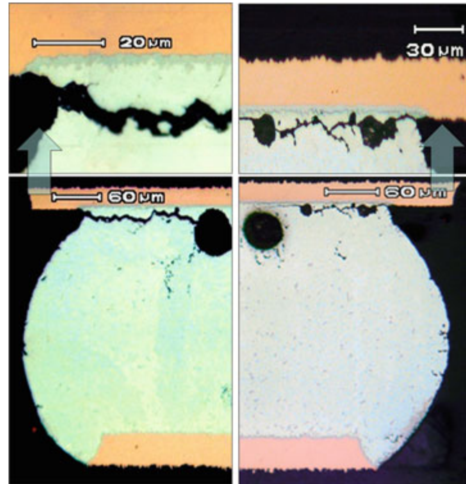

Fig. 9.14 Secondary failure modes of the SnAgCuNi interconnections

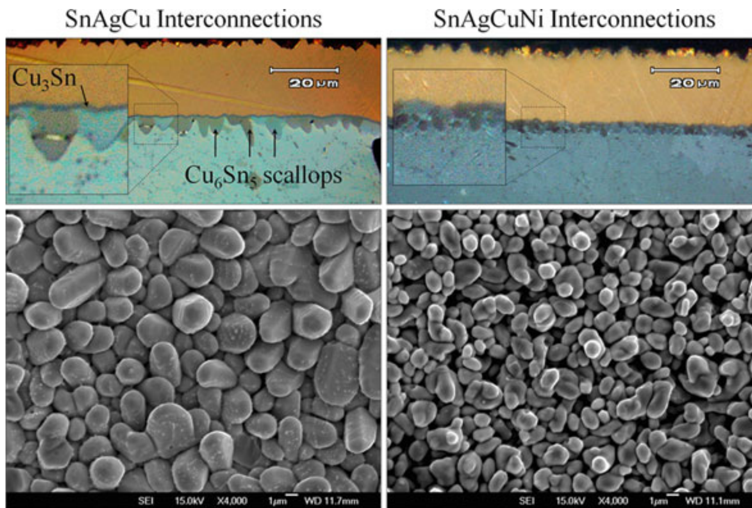

Fig. 9.15 Morphology of the interfacial reaction layers of the SnAgCu (*left*) and SnAgCuNi layers (*right*); *Top row*: cross-section of the intermetallic layer taken with cross-polarized light (different grain orientations appear in *different colors*), *bottom row*: top view of the intermetallic reaction layer taken with the SEM

place in the intermetallic layers, whereas in the case of SnAgCuNi interconnections cracks propagated in the copper trace of the PWB or in the bulk solder but never in the intermetallic layers.

9.5 Intermetallic Compounds Layers: Their Structure and Formation

Because the reliability of electronic assemblies under mechanical shock loading is very often dependent on the ability of intermetallic layers to withstand the stresses produced in their operation conditions, the formation and properties of intermetallic compound layers are discussed next. All the common base materials (coatings or metallizations) such as Cu, Ni, Ag, Ag–Pd and Au, form intermetallic compounds (IMCs) with Sn, which is the generally accepted major element in most lead-free solders. Chemical reactions occur between solders and conductor metals during soldering (i.e. component metallizations, boards surface finishes and underlying conductors), and IMCs will nucleate and grow at the solder/conductor interfaces (provided that the solder alloys do not contain such elements that can prevent the formation of IMC layer). It is well known that the presence of the IMCs between solders and conductor metals is an indication of good metallurgical bonding. A thin, continuous and uniform IMC layer is an essential requirement for good bonding. However, due to their inherent brittle nature and the tendency to generate structural defects, too thick IMC layer at the solder/conductor metal interface may degrade the reliability of the solder joints.

Even though there are some characteristic differences between the systems commonly used in electronics devices (Cu–Sn, Ni–Sn, Ag–Sn and Au–Sn) the intermetallic reaction layers are formed, in principle, in three consecutive stages: (a) dissolution of contact metallization to molten solder, (b) chemical reaction i.e. the formation of IMCs, and (c) solidification of the interconnections. Although the relative importance of each stage may vary between different systems depending on the solubility of conductor metal in tin. The general sequence of events during a soldering operation can be described as follows. Immediately after the flux has removed the oxides and permits metallurgical contact of solder with the conductor metal, the contacted metal starts to dissolve to the molten solder. Initially, the rate of dissolution is very high, particularly if the solder is not alloyed with the metal in question and, therefore, very high concentrations of solute elements can be realized locally. After a short period of time, the layer of molten solder that is adjacent to the contacted metal becomes supersaturated with the dissolved metal throughout the interface. Thermodynamically, at the local (metastable) equilibrium solubility, the solid IMC starts to form in this part of the solder. The formation of the IMC takes metal solutes out of the saturated liquid solder and causes some further dissolution of the contacted metal, especially if the intermetallic layer is not uniform on top of the substrate. During storage or in use of electronic devices, the IMCs generated during soldering grow further in thickness or increase in number, especially if the operational temperatures are well above the ambient. Therefore, both solid/liquid and solid/solid systems must be studied to have better understanding of the reliability of soldered assemblies. It should be noted that the microstructures formed during soldering are under continuous microstructural evolution during the use of the devices. The local equilibrium conditions in the

solder interconnections will change locally owing to the consumption of one or more of the components. This may then change the phases that can exist in local equilibrium accordingly and result in new interconnection microstructures. The microstructural changes thereby can affect the modes and mechanisms by which interconnections fail under loading. Thus, knowledge of the solder|conductor interaction and phase evolution in the solder interconnections is important not only to understand the reliability issues of the solder interconnections but also to the optimization of the soldering process from the metallurgical standpoint.

The lead-free materials used in the reliability tests were chosen to represent those typically used in portable electronic products. Ni(P)|Au or organic soldering preservative (OSP) protective coatings were used on the printed wiring boards (PWB), and Ni|Au or bare Cu were used as the under bump metallization (UBM) on the component side. SnAgCu-bumped components were reflow solder with different commercial near-eutectic SnAgCu solder pastes. Thus, there are three metallurgically different interfacial regions and each of them will be discussed in the following. A detailed review about the formation of intermetallic compound layers in different systems is available [24] and therefore only binary Cu–Sn, Ni–Sn and ternary Ni–P–Sn cases are shortly presented here.

9.5.1 Cu–Sn

Out of the material combinations studied in this work, the interconnections with copper in contact with the solder formed the most reliable interconnection structure under the mechanical shock loading. In the temperature range of interest (e.g. below 260°C), the interfacial reaction with molten Sn-based solder results in the formation of Cu_3Sn (ε) and Cu_6Sn_5 (η) layers.

In general, at temperatures typical for the soldering processes, i.e. below 260°C, Cu_6Sn_5 is the first phase to form at the liquid Sn/Cu conductor interface. The first stage of the reaction is the dissolution of Cu to liquid solder, until the solder becomes supersaturated with Cu more or less uniformly at the Cu/liquid interface (i.e. reaches the metastable solubility limit). The metastable solubility is important, because it essentially determines the dissolution rate of metal to liquid solder. The metastable solubility is always higher and typically it is 2–3 times the stable solubility. Here, it indicates the largest possible amount of Cu that can dissolve in the liquid without precipitating back as pure Cu. It is to be noted that when calculating metastable solubilities, one has to use the data being assessed both stable and metastable phases. If the data have not been optimized for metastable phase, the liquids are generally far too stable in their metastable regions and so the evaluation gives too high values for the metastable solubility.

When Cu comes into contact with molten Sn, it starts to dissolve rapidly [25, 26]. Initially, the dissolution is a non-equilibrium process and locally very high concentrations of Cu can be realized in the very vicinity of the Cu/liquid interface. Since there is large driving force for the chemical reaction between Cu and Sn

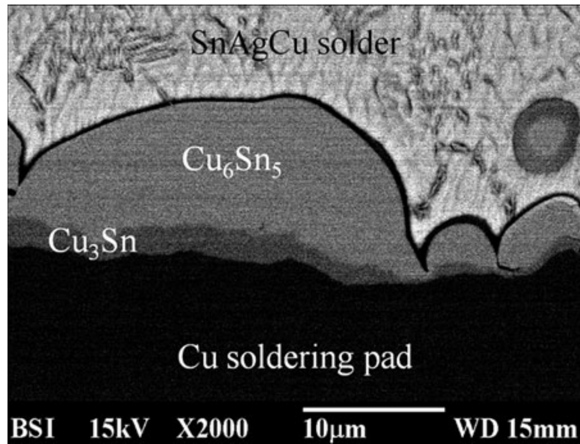

Fig. 9.16 Cu|SnAgCu interface annealed at 250°C for 1 h in order to detect the Cu_3Sn layer in between the Cu pad and the Cu_6Sn_5

atoms at the metastable composition, Cu_6Sn_5 crystallites can form very fast by the heterogeneous nucleation and growth at the Cu/liquid interface. In addition to the more or less uniform scallop-type Cu_6Sn_5 layer (uniphase), the (Cu_6Sn_5+Sn) two-phase layer can form next to the uniphase layer, most likely enhanced by the local constitutional supercooling of liquid. The final thickness and the morphology of the reaction layer is determined primarily by the rate of the dissolution of Cu in liquid and the chemical reaction between Sn and Cu and, secondarily, by the diffusion of Cu in the liquid. The metastable solubility of Cu in liquid solder is therefore the most important factor. On the other hand, the rate of diffusion of Cu atoms in the liquid determines the extent and morphology of the two-phase zone in front of the uniphase layer. Thermodynamically, there should also be a layer of Cu_3Sn layer between Cu and Cu_6Sn_5 (see Fig. 9.16). However, the thickness of the Cu_3Sn layer is much smaller than that of the Cu_6Sn_5 layer after reflow or wave soldering, and its formation usually requires extended contact times.

When one considers solid state reactions between Sn and Cu, it can be concluded that from room temperature up to 50–60°C only the η'-phase grows with an observable rate and the reaction is controlled by the release of Cu atoms from the Cu lattice. The main diffusing species at room temperature is Cu. Above 60°C, the ε-phase starts to grow with measurable rate and its fraction out of the total intermetallic layer increases as annealing continues. Between 60 and 200°C, diffusion of Sn starts to control the growth of the η-phase. This is rational, as the temperature is increased, volume diffusion starts to dominate and grain boundary and interstitial diffusion of Cu do not play such a big role anymore. During this temperature interval, the ε-phase continues to grow at the expense of the η-phase and both Cu and Sn are mobile during its growth. Consistent with the Cu_3Sn rule, Cu is the more mobile species in the ε-phase. As interdiffusion in the η-phase at temperatures 160–220°C requires higher activation energy, the fraction of the ε-phase out of the total intermetallic layer thickness is larger at temperatures 160–200°C than at 220°C. It should also be noted that if solid state aging follows

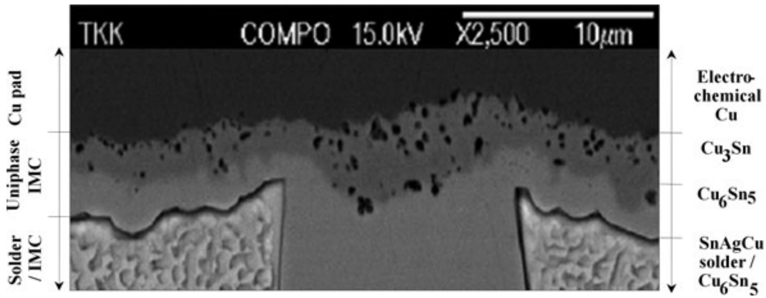

Fig. 9.17 Electrolytic Cu|Sn diffusion couple annealed at 125°C for 1000 h

soldering, the resulting morphology after aging is dependent on the initial morphology formed during the solid–liquid contact. Finally, excessive void formation and redistribution of impurities in Cu_3Sn phase already at low temperatures, as sometimes detected, induces some reliability concerns for Cu conductors and under bump metallization (see Fig. 9.17).

9.5.2 Ni–Sn

Ni is often used as a diffusion barrier layer between Cu and Sn, since the reaction rate of Ni with liquid Sn is typically smaller than that of Cu with Sn. This, in turn, results in thinner IMC layers in the Sn–Ni system than in the Sn–Cu system. The Sn–Ni system is well characterized. There are stable three IMCs (Ni_3Sn, Ni_3Sn_2 and Ni_3Sn_4) at the temperatures of our interest i.e. below 260°C. It has been reported that the Ni_3Sn_4 phase (or metastable phases) forms during soldering at the interface between liquid non-Cu-containing solders, such as SnPb, SnAg, or SnSb, and Ni metallization. The Ni_3Sn_4 phase forms even though it is thermodynamically the least stable of all the Ni–Sn compounds and it possesses the most complicated crystal structure. Similar arguments regarding the initial periods of dissolution and Ni_3Sn_4 nucleation are valid here as already discussed in the case of Cu. However, the solubility of Ni is much smaller and, therefore, its dissolution rate is much lower.

On the other hand, when using Pb-free solders that include even small amounts of Cu, the first phase to form at the interface changes so that it is the $(Cu,Ni)_6Sn_5$ instead of the Ni_3Sn_4. This was the case with the drop test results presented in Sect. 9.3 above where the component had Ni|Au under bump metallization and the bump was SnAgCu alloy. The incorporation of Ni in the Cu_6Sn_5 was observed to weaken the mechanical properties of intermetallic layer by producing severe cracking of the intermetallic phase (see Fig. 9.18). The cracking of the $(Cu,Ni)_6Sn_5$ is sometimes visible even after reflow.

Hence, to determine the critical Cu concentration (shown in Fig. 9.19), which causes the formation of $(Cu,Ni)_6Sn_5$ instead of $(Ni,Cu)_3Sn_4$, is of practical significance. The critical amount of Cu required to change the first forming phase is

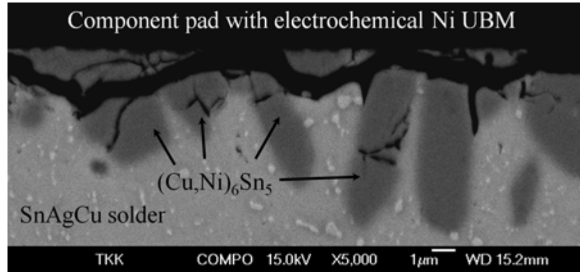

Fig. 9.18 Cracking of the $(Cu,Ni)_6Sn_5$ reaction layer is characterized by relatively large number of secondary cracks along the crack path

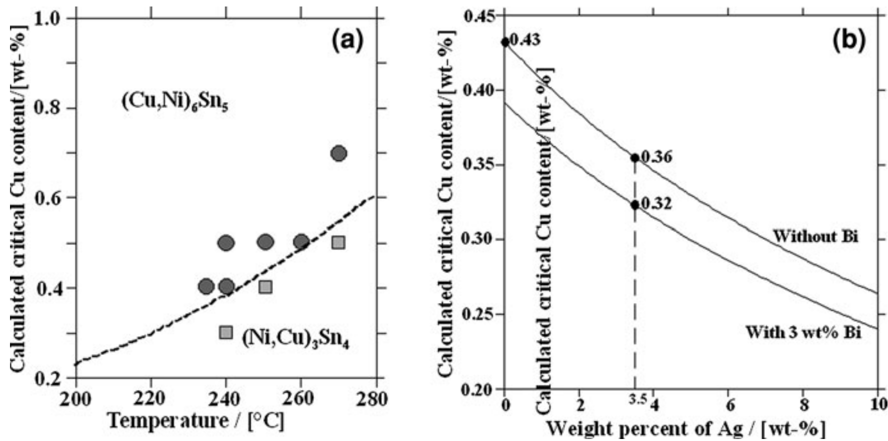

Fig. 9.19 **a** Calculated critical Cu content in liquid Sn to change interfacial reaction product from $(Ni,Cu)_3Sn_4$ to $(Cu,Ni)_6Sn_5$, as a function of temperature together with the experimental points. **b** Effect of alloying Ag and Bi to Sn on the critical Cu content at $T = 250°C$ [43]

dependent on temperature and other elements in the alloy. As shown in Fig. 9.19a, the critical Cu concentration increases with increased peak reflow temperature. On the other hand, the alloying elements, for example Ag and Bi shown in Fig. 9.19b, decrease the critical Cu content. The detailed thermodynamic explanation for this transition has been explained elsewhere [24, 43] and is therefore not repeated here.

9.5.3 *Ni–Sn–P*

During recent years, the electroless Ni|immersion Au coatings (denoted Ni(P)|Au) have been extensively used in high-density component assemblies as a surface finish on printed wiring boards (PWB) because they have many advantages over other surface finishes such as hot air solder levelling (HASL) SnPb finishes: Ni(P)|Au coatings provide desired flat and uniform pad surface and they maintain good wettability, even after multiple reflows. Furthermore, Ni(P)|Au coatings provide higher mechanical strength and resistance against thermal fatigue of

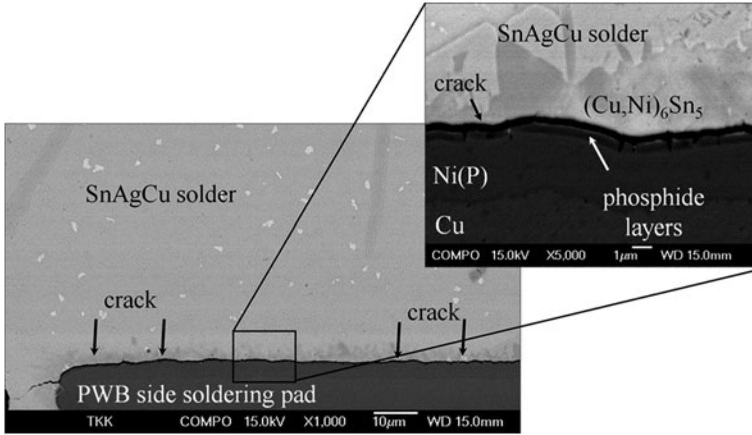

Fig. 9.20 Cracking of the PWB side interfacial reaction layers between the Ni(P)|Au and SnAgCu solder

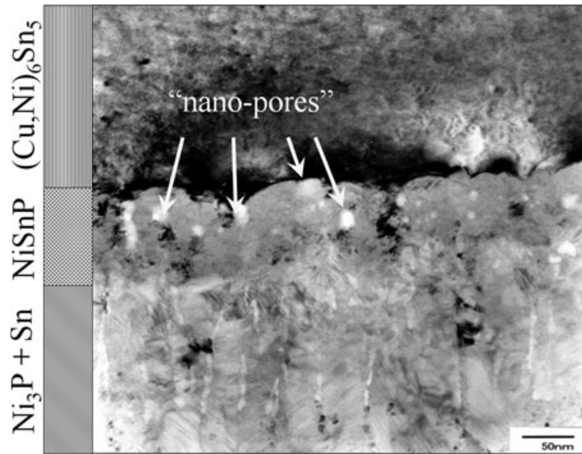

Fig. 9.21 Transmission electron micrograph from the interfacial reaction layer in the interconnections on the Ni(P)|Au metallization

lead-free solder interconnections than can be achieved when using organic solder preservatives on Cu pads. Moreover, as an insulating material OSP has a disadvantage when connectors are assembled on the same board. Finally, nickel acts as a diffusion barrier layer between Sn-based solders and copper conductors and prevents the underlying copper from reacting with Sn.

On the other hand, reliability problems have been reported when using Ni(P)|Au coatings with Sn-based solders. Under mechanical shock, loading cracks propagate in a very narrow reaction zone (NiSnP in Fig. 9.20) between the two-phase layer and the $(Cu,Ni)_6Sn_5$ intermetallic layer, as shown in Fig. 9.21. During the electroless coating process, Ni is deposited on Cu together with phosphorous, because hypophosphite is used as a reducing agent in plating baths. It is the presence of

phosphorus in the surface finish layers that has been observed to be associated with the above-mentioned reliability problems. Although the wetting occurs properly and the chemical reaction between Sn and Ni is evident, the interfacial strength is not adequate. The weakest interfacial reaction product readily fractures under mechanical stress even during cooling from soldering temperatures and leaves behind an open circuit. The formation mechanism of the interfacial reaction products that causes the reliability problem has not yet been identified with certainty.

When one considers reaction between liquid Sn (or SnAgCu solders) and Ni(P)|Au surface finish, the following reaction sequence takes place: Immediately after the solder has melted Au, Ni and P start dissolving rapidly into the liquid solder, which—due to the existence metastable liquid miscibility gap in the Sn–P–Ni system—is divided into Sn-rich liquid (L_1) and (Ni,P)-rich liquid (L_2). Because of high Ni content, the L_2 is unstable and it transits into the nanocrystalline NiSnP, which provides the substrate for the formation of the $(Cu,Ni)_6Sn_5$. Subsequently, the metastable NiSnP layer starts to transform into the columnar Ni_3P. In this transformation, Sn atoms and impurities, which do not dissolve into the Ni_3P, diffuse toward the remaining NiSnP layer. The impurities in this ternary layer are revealed as numerous small "pores" detected with the high-resolution transmission electron microscopy (see Fig. 9.21). More detailed description of the above presented reaction sequence can be found from the literature [27].

Under mechanical shock loading, the reliability of interconnections on the Ni(P)|Au is inferior to that of interconnections on the Cu|OSP due to the formation of the complex P-rich reaction layers between the Ni(P) coating and the solder. Cracks nucleate and propagate in the porous and highly brittle NiSnP layer between the columnar two-phase (Ni_3P+Sn) layer and the $(Cu,Ni)_6Sn_5$ intermetallic layer.

9.5.4 Effect of Alloying and Impurity Elements on Cu–Sn IMC Formation and Properties

Owing to the reasons discussed earlier, there is a continuous interest to better understand and influence the properties of IMC layers in order to increase the reliability of solder interconnections. One way to influence the interfacial reactions and the resulting product layers in a given system is to alloy either metallization (conductor) or solders with small amounts of additional elements. It is to be noted that also the presence of impurities in the interconnection system may have marked effects on the properties and growth of IMC layers. Additional elements can basically have three major effects on the reaction between the solder and the conductor metal: (a) they can increase or decrease the reaction/growth rate, (b) additives can change the physical properties of the phases formed (in the case of Cu and Sn, Cu_3Sn and Cu_6Sn_5), and (c) they can form additional reaction layers at the interface or they can displace the binary phases that would normally appear and form other reaction products instead. Further, these elements can be divided roughly into two major categories: (a) elements that only change the activities of

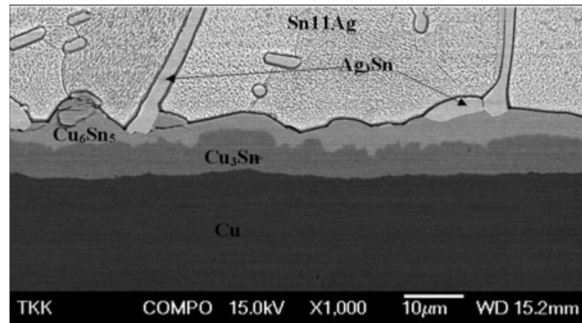

Fig. 9.22 Reaction layers formed in the reaction between Sn11Ag and Cu after annealing at 150°C for 2560 h

species taking part in the interfacial reaction and do not participate themselves (not extensively soluble in IMC layer) and (b) elements that take part in the interfacial reaction in question (generally show marked solubility in IMC layer). The elements belonging to the latter category usually have more pronounced effect on the IMC formation. Because the Sn–Cu system is the most important binary reaction couple associated with soldering, we will take it as the base system and consider the effect of one element from each category (a) Ag and (b) Ni on the binary reaction.

9.5.4.1 Effect of Ag

Figure 9.22 shows the interface between Sn11Ag (at%) and Cu after annealing at 150°C for 2560 h. The large Ag_3Sn IMCs are also clearly seen in the micrograph. The plot of IMC thickness as a function of square root of time for this couple is shown in Fig. 9.23.

As can be seen (see Figs. 9.23, 9.25) the growth behavior is very similar to that of 100Sn–Cu system (see Fig. 9.24) as shown also in previous publications [28–30] and indicated by the Sn–Ag–Cu phase diagram and thermodynamic data [31, 32].

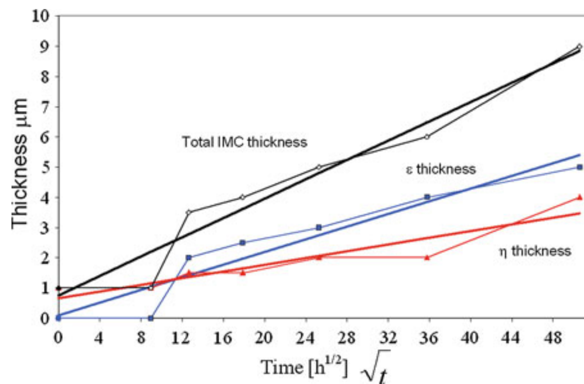

Fig. 9.23 The plot of IMC thickness as a function of square root of time (hours) for the Sn11Ag–Cu couple

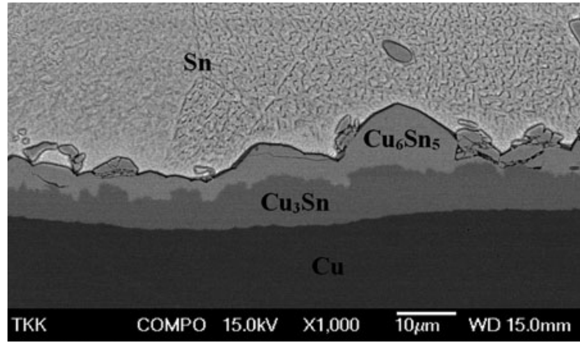

Fig. 9.24 Reaction layers formed in the reaction between pure 100Sn and Cu after annealing at 150°C for 2560 h

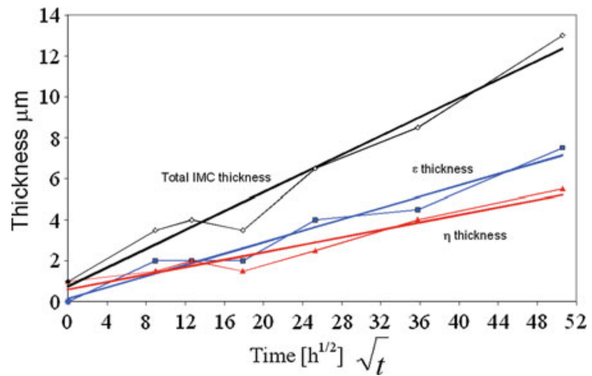

Fig. 9.25 The plot of IMC thickness as a function of square root of time (hours) for the 100Sn–Cu couple

The reasons for the observed behavior can be interpreted with the help of thermodynamic-kinetic information. As Ag does not dissolve in Cu_6Sn_5 or Cu_3Sn, the only way for it to influence the interfacial reactions is by influencing the activities of the reacting species, in this case that of Sn [32]. The presence of Ag slightly decreases the activity of Sn in the solder and, thus, reduces the driving force of the diffusion of Sn through the Cu_6Sn_5 layer. As Sn is the main diffusing species in Cu_6Sn_5 at these temperatures, the resulting decrease in the Sn flux through the layer favors the growth of Cu_3Sn, where Cu is the main diffusing species [24, 33–40]. It is to be noted, however, that the IMC growth behavior in the Cu–Sn system is not only strongly temperature dependent as already discussed in Sect. 9.5.1. The relative thickness of Cu_6Sn_5 and Cu_3Sn is changed as a function of temperature due to the changes of both driving forces and intrinsic diffusion fluxes of Cu and Sn in the phases. It should also be noted that if solid state aging follows soldering, the resulting morphology after aging is dependent on the initial morphology formed during the solid–liquid contact. In addition, it must be noted that the growth of the phases in a given multiphase reactive diffusion couple is not independent, but is affected by other growing layers [41].

Hence, Cu_3Sn consumes some of the Cu_6Sn_5 as it grows, and this effect is enhanced when the flux of Sn through Cu_6Sn_5 is reduced, as shown in previous publication [42]. This effect can be seen by comparing the diagrams in Figs. 9.23, 9.25, as not only the thickness of Cu_3Sn surpass that of Cu_6Sn_5 earlier that in the case of pure Sn–Cu couple, but also the total IMC thickness is somewhat reduced in comparison with Sn–Cu couple.

This is because as the flux of Sn through Cu_6Sn_5 is decreased, also the growth of Cu_3Sn is slowed down due to the reduced availability of Sn at the Cu_3Sn/Cu_6Sn_5 interface. Finally, it is to be noted that as the solubility of Ag in solid Sn is very small it has only minor effect on the activity of Sn [32]. Therefore, the difference between the growth kinetics of IMCs in Sn11Ag–Cu and 100Sn–Cu systems do not display marked differences. One can also ask whether the formation of Ag_3Sn platelets at the interface may play some role in the intermetallic compound formation by physically blocking the diffusion of Sn to Cu_6Sn_5 layer at specific locations. However, this effect is anticipated to be of much less of significance than the effect of Ag on the activity of Sn. This is because there still remain plenty of paths for Sn diffusion to Cu–Sn IMC layers despite the Ag_3Sn precipitates and it can even be argued that the phase interface between Ag_3Sn precipitates and Sn-based solder matrix offers fast diffusion paths for Sn atoms along the interface, thus acting against the above-mentioned "blocking effect".

9.5.4.2 Effect of Ni

Figure 9.26 shows the interface between Sn1Ni (at%) and Cu after annealing at 150°C for 2560 h. The plot of IMC thickness as a function of square root of time for this couple is shown in Fig. 9.27. When Figs. 9.25, 9.27 are compared, it can be seen that: (a) total IMC layer thickness is smaller than in the Sn–Cu case, (b) its growth does not follow parabolic kinetics and (c) especially the thickness of Cu_3Sn is drastically reduced. As the growth kinetics related to this system have been described in detail (both in liquid and in solid state) [42, 43] together with lengthy list of appropriate references, only a brief discussion is presented here.

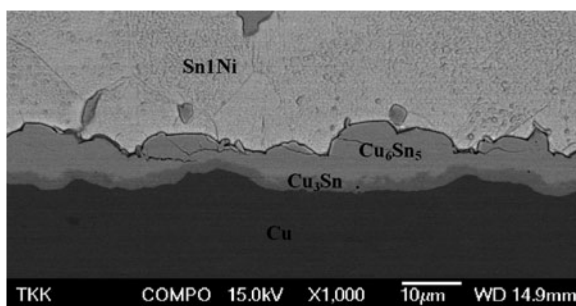

Fig. 9.26 Reaction layers formed in the reaction between Sn1Ni and Cu after annealing at 150°C for 2560 h

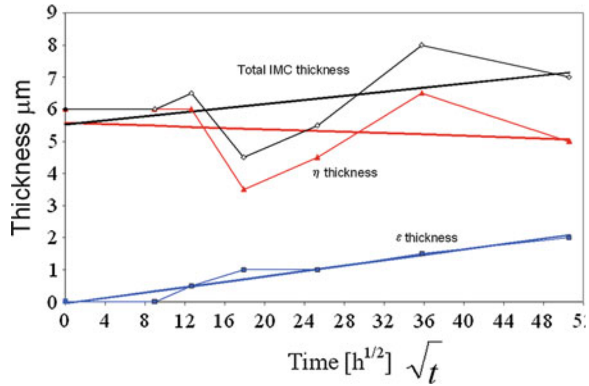

Fig. 9.27 The plot of IMC thickness as a function of square root of time (hours) for the Sn1Ni–Cu couple

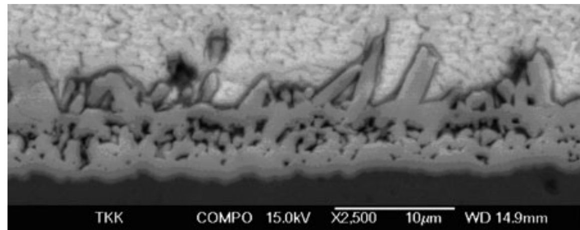

Fig. 9.28 Cu/Sn1Ni interface after reflow soldering

The deviation from the parabolic growth law of the total IMC comes mainly from the $(Cu,Ni)_6Sn_5$ layer, as it is seen that Cu_3Sn follows nicely diffusion-controlled growth kinetics (Fig. 9.27). The reason for the abnormal growth of $(Cu,Ni)_6Sn_5$ most probably has its origin in the liquid stage reaction. Because of the effect of Ni on the interaction between Cu and Sn atoms in the liquid (and thus also on the solubilities), the formation of a relatively thick and highly porous two-phase structure [$(Cu,Ni)_6Sn_5$+Sn] takes place (see Fig. 9.28), as explained in [43].

Thus, during the solid state annealing, sintering of this porous structure takes place first, and only after it transforms to the dense $(Cu,Ni)_6Sn_5$ structure, can the "normal" parabolic growth continue. Based on the experimental results, it seems that the sintering of the porous $(Cu,Ni)_6Sn_5$ layer has barely reached its end within the time frame of the annealing. On the other hand, the decreased growth of Cu_3Sn can be explained with the help of thermodynamic-kinetic considerations about the Cu–Sn–Ni system [44]. During soldering process, the solder is in molten state for about a minute. During such a short period of time, the ternary compounds that have been observed or proposed to be present in the system [45–47] cannot form. Therefore, the metastable phase diagram without these compounds can more realistically describe the equilibria between solder alloys and conductor metals [24, 41, 43]. Using the optimized dataset [32], the Gibbs free energy curves corresponding to this metastable phase diagram were calculated. When 1 at% of Ni is added to Sn, the Ni content of $(Cu,Ni)_6Sn_5$ is about 20 at% (measured by EDS) and its stability is increased markedly. The Cu_3Sn being in equilibrium with it is

practically free of Ni, and so its stability will remain practically the same as that of pure Cu_3Sn. As a result, the driving forces for the diffusion over the intermetallic compounds will change. The driving force for the diffusion of Sn through the $(Cu,Ni)_6Sn_5$ layer is now about ten times the driving force for the 100Sn–Cu couple. On the other hand, the driving force for the diffusion of Cu through Cu_3Sn reduces almost to zero. This means that through the Nernst–Einstein relation the fluxes through the Cu_3Sn and the $(Cu,Ni)_6Sn_5$ layers are markedly altered, thus resulting into the observed growth behavior (i.e. the marked decrease in the layer thickness of Cu_3Sn layer), as also previously shown [42, 43].

9.6 Summary

The ongoing trend toward ever smaller electronic products forces to larger scales of integration and to the use of smaller and finer pitch components, such as (wafer-level) chip scale packages and flip chips. Because of the small-scale interconnections, components become closer to the printed wiring boards and the strains and stresses experienced by solder interconnections are increased. These miniaturized interconnections must be able to withstand variety of different loadings out of which the sudden mechanical shocks are perhaps the most severe threat to their reliability. Hence, understanding why the different tests produce different failure mechanisms and, ultimately, different reliability performance is of importance. This can only be achieved by knowing how the stress states are produced, how the materials respond to different types of loading, and how the microstructures of solder interconnections affect the failure mechanisms. Therefore, the emphasis of this paper was placed on describing the loading condition under mechanical shock loading and how it differs from that of thermal cycling.

The failure modes under mechanical shock loads are different from those typically observed in the thermal cycling, where solder interconnections fail by cracking through the bulk solder assisted by the localized recrystallization. Under the mechanical shock, loading the strain-rate hardening of the solder forces cracks to propagate in the intermetallic layers on either side of the interconnections instead of the bulk solder.

The drop reliability of the high-density electronic assemblies was studied by applying standardized test procedures for test vehicles that represent the technologies and lead-free materials typically used in portable electronic products. The component studied in this work was a 12 mm × 12 mm Chip Scale Packaged Ball Grid Array component, which today is the most commonly used package in portable electronic products. The assembled component boards had optional under bump metallizations (Ni or Cu), printed wiring board coatings (Cu|OSP or Ni(P)|Au) and solder compositions (SnAgCu or low-silver SnAgCuNi). The reliability of interconnections on the Ni(P)|Au was inferior to that of the interconnections on the Cu|OSP due to the formation of the complex and mechanically poor P-rich reaction layers between the Ni(P) coating and the solder in the

Ni(P)|Au interconnections. Interconnections on Cu|OSP coatings, in turn, fail by cracking of the intermetallic compound layers on the component side. The binary Cu_6Sn_5 formed on bare Cu under bump metallization showed good structural integrity but the $(Cu,Ni)_6Sn_5$ formed on the Ni metallization is weaker. Solder interconnections with the low-silver nickel containing composition (SnAgCuNi) showed higher average number of drops-to-failure.

Three different failure modes were identified in the drop-tested component boards: (a) cracking of the interconnections in the component side intermetallic layer, (b) cracking of the copper trace on the PWB and (c) cracking of the bulk of solder interconnections on the component side. The mode (c) was found only in the SnAgCuNi interconnections, and the cracks were not observed to have propagated entirely through the interconnections. The SnAgCu interconnections failed by the mode (a) while the SnAgCuNi interconnections failed by the mode (b).

Because the reliability of electronic assemblies under mechanical shock loading is very often dependent on the ability of intermetallic layers to withstand the stresses produced in their operation conditions, the formation and properties of the three metallurgically different interfacial regions (Cu|SnAgCu, Ni|SnAgCu, Ni(P)|SnAgCu, and Cu|SnAgCuNi) were discussed in detail. Further, it was shown that alloying and impurity elements can have strong effects on the growth and properties of IMC layers. The binary Cu–Sn system was used as the base reaction couple. Based on the solubility of the alloying and impurity elements in the IMC layers, these elements can be divided into two categories: (a) alloying elements that do not dissolve in either Cu_6Sn_5 or Cu_3Sn and (b) elements that exhibit significant solubility in (usually) Cu_6Sn_5 and (possibly) Cu_3Sn. It was shown that the latter group of elements have markedly stronger effect on the growth behavior of IMC's in the Sn–Cu system than those belonging to the first group, because these (that do not dissolve in IMC's) can influence diffusion fluxes in the layers only indirectly through the activity of Sn. On the other hand, if the element dissolves in IMC layer it can alter its stability and probably also its microstructure, thus influencing the growth kinetics directly.

References

1. Mattila TT, Kivilahti JK (2004) Impact of printed wiring board coatings on the reliability of lead-free chip scale package interconnections. J Mater Res 19(11):3214–3223
2. Mattila TT, Kivilahti JK (2010) The role of recrystallization in the failure mechanism of SnAgCu solder interconnections under thermomechanical loading. IEEE Trans Compon Packaging Technol 33(3):629–635
3. Mattila TT (2005) Reliability of high-density lead-free solder interconnections under thermal cycling and mechanical shock loading, Espoo, HUT-EPT-13, http://lib.tkk.fi/Diss/2005/isbn9512279843/, Otamedia, p 202
4. Mattila TT, Laurila T, Kivilahti JK (2007) Metallurgical factors behind the reliability of high density lead-free interconnections. In: Suhir E, Wong CP, Lee YC (eds) Micro-and opto-electronic materials and structures: physics, mechanics, design, reliability, packaging, vol 1. Springer, New York, pp 313–350

5. Mattila TT, Marjamäki P, Kivilahti JK (2006) Reliability of CSP components under mechanical shock loading. IEEE Trans Compon Packaging Technol 29(4):787–795
6. Mattila TT, Kivilahti JK (2005) Failure mechanisms of lead-free CSP interconnections under fast mechanical loading. J Electron Mater 34(7):969–976
7. Mattila TT, James R, Nguyen L, Kivilahti JK (2006) Effect of temperature on the drop reliability of electronic assemblies. In: The proceedings of the 57th electronic component and technology conference, Reno, CA, May 29–June 1, 2007, IEEE/EIA CPMT
8. Mattila TT, Kaloinen E, Syed A, Kivilahti JK (2006) Reliability of SnAgCu interconnections with minor additions of Ni or Bi under mechanical shock loading at elevated temperatures. In: The proceedings of the 57th electronic component and technology conference, Reno, CA, May 29–June 1, 2007, IEEE/EIA CPMT
9. Mattila TT, Šimeček J, Kivilahti JK (2006) Failure modes of solder interconnections under mechanical shock loading at elevated temperatures. In: The proceedings of the 1st electronics systemintegration technology conference, Dresden, Germany, September 5–7, 2007, IEEE/ EIA CPMT, pp 195–202
10. Mattila TT, Marjamäki P, Nguyen L, Kivilahti JK (2006) Reliability of wafer-level chip scale packages under mechanical shock loading. In: The proceedings of the 56th electronic component and technology conference, San Diego, CA, May 30–June 2, 2006, IEEE/EIA CPMT, pp 95–101
11. Mattila TT, Kivilahti JK (2006) Reliability lead-free interconnections under consecutive thermal and mechanical loadings. J Electron Mater 35(2):250–255
12. Marjamäki P, Mattila TT, Kivilahti JK (2006) A comparative study of the failure mechanisms encountered in drop and large amplitude vibration tests. In: The proceedings of the 56th electronic component and technology conference, San Diego, CA, May 30–June 2, 2006, IEEE/EIA CPMT
13. JESD22-B111 (2003) Board level drop test method of components for handheld electronic products. JEDEC Solid State Technology Association, p 16
14. Marjamäki P (2007) Vibration test as a new method for studying the mechanical reliability of solder interconnections under shock loading conditions, Doctoral dissertation. Helsinki University of Technology, (to be published)
15. Reinikainen TO, Marjamäki P, Kivilahti JK (2005) Deformation characteristics and microstructural evolution of SnAgCu solder joints. In: The proceedings of the 6th EuroSimE conference, Berlin, Germany, April 18–20, 2005, IEEE, pp 91–98
16. Nikander R (1999) Characterization of the mechanical properties of the dilute tin based solder alloys, Espoo, master's theses, Helsinki University of Technology, p 79
17. Reinikainen T, Kivilahti JK (1999) Deformation behavior of dilute SnBi(0.5 to 6 at. pct) solid solutions. Metallurgical Mater Trans A 30:123–132
18. Amagai M (2006) A study of nano particles in SnAg-based lead free solders for intermetallic compounds and drop test performance. In: The proceedings of the 56th electronic components technology conference, San Diego, CA, May 30–June 2, 2006, IEEE/CPMT, pp 1170–1190
19. Amagai M, Watanabe M, Omiya M, Kishimoto K, Shibuya T (2002) Mechanical characterization of Sn–Ag-based lead-free solders. Microelectron Reliab 42(6):951–966
20. Che FX, Luan JE, Baraton X (2008) Effect of silver content and nickel dopant on mechanical properties of Sn-Ag-based solders. In: The proceedings of the 58th electronic components technology conference, Orlando, FL, May 27–30, 2008, IEEE/CPMT, pp 485–490
21. Garner L, Sane S, Suh D, Byrne T, Dani A, Martin T, Mello M, Patel M, Williams R (2005) Finding solutions to the challenges in package interconnect reliability. Intel Technol J 9(4):297–308
22. Tanaka M, Sasaki T, Kobayashi T, Tatsumi K (2006) Improvement in drop shock reliability of Sn-1.2Ag-0.5Cu BGA interconnects by Ni addition. In: The proceedings of the 56th electronic components technology conference, San Diego, CA, March 31–June 2, 2006, IEEE/CPMT, pp 78–84

23. Laurila T, Vuorinen V, Kivilahti JK (2005) Interfacial reactions between lead-free solders and common base materials. Mater Sci Eng R 49(1–2):1–60
24. Bader WG (1969) Dissolution of Au, Ag, Pd, Pt, Cu and Ni in a Molten Tin-Lead Solder. Welding J Res Suppl 48(12):551–557
25. Bader WG (1980) Dissolution and formation on intermetallics in the soldering process. In: Proceedings of the conference on physical metallurgy and metal joining, St. Louis, MO, Oct 16–17. Warrendale, USA
26. Haimovich J (1989) Intermetallic compound growth in Tin and Tin-Lead platings over nickel and its effects on solderability. Welding J Res Suppl 68(3):102–111
27. Vuorinen V, Laurila T, Yu H, Kivilahti JK (2006) Phase formation between Lead-free SnAgCu Solder and Ni(P)/Au Finished on PWB. J Appl Phys 99(2):3530–3535
28. Bae K, Kim S (2001) Interdiffusion analysis of the soldering reactions in Sn-3.5Ag/Cu couples. J Electron Mater 30(11):1452
29. Choubey A, Yu H, Osterman M, Pecht M, Yun F, Younghong L, Ming X (2008) Intermetallics characterization of lead-free solder joints under isothermal aging. J Electron Mater 37(8):1130
30. Moon K, Boettinger W, Kattner U, Biancaniello F, Handwerker C (2000) Experimental and thermodynamic assessment of Sn-Ag-Cu solder alloys. J Electron Mater 29(10):1122
31. IPMA (2009) The thermodynamic databank for interconnection and packaging materials. Helsinki University of Technology, Helsinki
32. Bhedwar H, Ray K, Kulkarni S, Balasubramanian V (1972) Kirkendall effect studies in copper-tin diffusion couples. Scr Metallurgica 6:919
33. Onishi M, Fujibuchi H (1975) Reaction-Diffusion in the Cu-Sn system. Trans Jpn Inst Metals 16:539
34. Oh M (1994) Growth kinetics of intermetallic phases in the Cu-Sn binary and the Cu-Ni-Sn ternary systems at low temperatures. Doctoral Dissertation, Lehigh University
35. Tu KN (1973) Interdiffusion and reaction in bimetallic Cu-Sn thin films. Acta Metall 21:347
36. Tu KN, Thompson R (1982) Kinetics of interfacial reaction in bimetallic Cu—Sn thin films. Acta Metall 30:947
37. Tu KN (1996) Cu/Sn interdiffusion reactions: thin film case vs bulk case. Mater Chem Phys 46:217
38. Revay L (1977) Interdiffusion and formation of intermetallic compounds in tin-copper alloy surface coatings. Surf Technol 5:57
39. Paul A (2004) The kirkendall effect in solid state diffusion. Doctoral Dissertation, Technical University of Eindhoven
40. Laurila T, Molarius J (2003) Reactive phase formation in thin film metal/metal and metal/silicon diffusion couples. Crit Rev Solid State Mater Sci 28:185–230
41. Vuorinen V, Laurila T, Mattila T, Heikinheimo E, Kivilahti JK (2007) Solid state reactions between Cu(Ni) alloys and Sn. J Electron Mater 36(10):1355–1362
42. Vuorinen V, Yu H, Laurila T, Kivilahti JK (2008) Formation of the intermetallic compound between liquid Sn and different CuNix metallizations. J Electron Mater 37(6):792–805
43. Yu H, Vuorinen V, Kivilahti JK (2007) Effect of Ni on the formation of Cu_6Sn_5 and Cu_3Sn intermetallics. IEEE Trans Electron Packaging Manuf 30(4):293–298
44. Oberndorff P (2001) Lead-Free solder systems: Phase relations and microstructures. Doctoral Dissertation, Technical University of Eindhoven
45. Lin C-H, Chen S-W, Wang C-H (2002) Phase equilibria and solidification properties of Sn-Cu-Ni alloys. J Electron Mater 31(9):907
46. Schmetterer C, Flandorfer H, Luef Ch, Kodentsov A, Ipser H (2009) Cu-Ni-Sn: A key system for lead-free soldering. J Electron Mater 38(1):10
47. Vuorinen V (2006) Interfacial reactions between Sn-based solders and common metallizations used in electronics. Doctoral Dissertation, Helsinki University of Technology