A new analytical approach of the impact of jitter on continuous time delta sigma converters

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Abstract. The performances of continuous time delta sigma converters are severely affected by clock jitter and no generic technique to predict the corresponding degradations is nowadays available. This paper presents a new analytical approach to quantify the power spectral density of jitter errors. This generic computational method can be applied to all kind of continuous time delta sigma converters. Furthermore, clock imperfections are described by means of phase noise spectrum, consequently all possible type of jitters can be taken into account. This paper also describes the temporal non ideal clock models that have been created to simulate the impact of jitter on delta sigma converters and validate the theoretical results.

1. INTRODUCTION

The current attractiveness for low pass continuous time delta sigma converter is largely due to the fact that it is possible to make them work at higher frequencies than their equivalent discrete time implementation. This specificity is widely used in order to increase the bandwidth or the resolution of the converters. This uninterrupted augmentation of sampling frequency induces an amplification of the ratio between jitter and clock period, making less and less negligible the influence of jitter on the converter performances.

Jitter impact on continuous time delta sigma converter is a tricky problem. The need of a better comprehension of the phenomena and an accurate estimation of the jitter degradations is nowadays still high. In the present paper, our new approach of the jitter problem will be described.

In section 2, after a quick reminder of the jitter impact on discrete time delta sigma converters, we will focus on the specificity of continuous time implementation regarding clock jitter and explain our approach to analyze this problem. Hence, we will derive the complete set of equations describing the impact of jitter on a 2^{nd} order modulator and discuss about the possibility to extend this result to more complex ar-

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chitectures. Finally in section 4, the equations accuracy will be verified via some numerical comparisons with simulations.

2. INFLUENCE OF JITTER ON DELTA SIGMA CONVERTERS

In a discrete time delta sigma (DTΔΣ), the input signal is sampled before being converted. So analyzing clock jitter on those converters is equivalent to the investigation of irregular sampling problem [1]. This assumption can be done as long as the imperfections of the clock do not perturb the transfer function of the converter loop. Under the assumption of a white phase noise for the clock signal, the maximum achievable signal to noise ratio (SNR) of a discrete time converter is given by:

$$SNR_{dB} = 10\log\left(\frac{OSR}{(2\pi f_{\max})^2 \sigma^2}\right) \qquad (\mathbf{1})$$

In this well known formula, σ is the standard deviation of the Gaussian distribution of jitter at each clock edge; OSR is the oversampling ratio of the converter and f_{max} is the maximal input frequency. Despite the important restrictions for the application of this equation, white phase noise and sinusoidal input, this formula is widely used for the design of DTΔΣ.

Unfortunately, in continuous time delta sigma converters (CTΔΣ) the jitter impact can not be reduced to the irregular sampling problem, and so (1) is inappropriate. The main reason why this equation is not valid any more is the fact that the sampling element in CTΔΣ is not in front of the loop but inside it, see figure 1. Moreover, in continuous time implementation the quantization noise introduced by the inner ADC is also responsible of losses linked to the clock imperfections. This phenomenon makes continuous time delta sigma converter much more sensible to clock jitter than discrete time analog-to-digital converters.

Several articles have already been published on the specific topic of jitter in CTΔΣ [2]-[4], giving us some interesting clues to understand the phenomena. In our approach of the jitter problem, we have decided not to make any initial assumption on the impact of this imperfection. So the first step of the study is to identify all possible errors introduced by jitter; only after this phase a mathematical estimation of the errors will be practicable.

If we consider that clock jitter has an impact on every continuous time function or signal, two kinds of jitter errors can be identified in a CTΔΣ. The first error, called sampling error, relates to the continuous input signal x(t) whereas the second one is introduced by the continuous time loop filter H(s). This second type of error is called integration error and is specific to continuous time delta sigma converters.

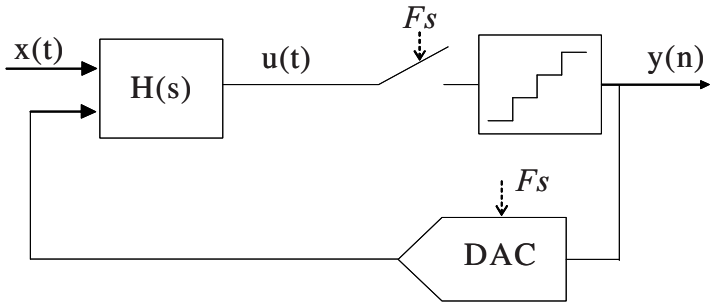

Figure 1. *Typical block diagram of a ΔΣ_CT*

2.1 Sampling error

The source of this error is the continuous time input signal x(t). Thus this error happens in both discrete and continuous time ΔΣ. However the quantity of noise introduced by sampling errors is quite different whether the implementation is continuous or discrete. In a CTΔΣ, the input signal is processed by the loop filter before being sampled.

2.2 Integration error

This kind of error is specific to continuous time delta sigma converters and is related to the couple DAC/loop filter. Indeed, the processing of the jittered DAC output by the loop filter is responsible for the introduction of errors.

It is obvious that every clock non ideality modifies the timing diagram provided by the DAC. Those slight timing variations, normally processed by the continuous time filter, introduce voltage errors on every stage of the loop filter. The errors introduced in the loop filter by the variation of the integration period are defined by the term "integration errors". The number of integration errors is equal to the modulator order since there is one voltage error at each integrator output.

In spite of the localization of integration errors inside the loop filter, the DAC implementation has a strong influence on those errors. Indeed the DAC is the triggering element of integration errors, so every modification of its implementation induces important changes in the resulting errors. It is for example well known that CTΔΣ using switched capacitor DAC are less sensitive to jitter than those with non return-to-zero (NRZ) DAC.

To conclude this phase of identification of the jitter errors, the impact of clock imperfections can be summarized as the introduction of N+1 errors for an N^{th} order modulator: one sampling error and N integration errors.

3. ANALYTICAL EVALUATION OF JITTER DEGRADATION

In the previous section, the errors introduced by jitter have been identified; we now need to quantify them in order to derive a mathematical expression of the performance degradations. First the complete set of equations for a 2nd order ΔΣ modulator with NRZ feedback will be established. Then we will show that it is possible to extend those formulas to other architectures.

3.1 Second order ΔΣ with NRZ feedback

The architecture of the considered converter and the localization of the integration errors are given on figure 2. For the following calculations the classical linear model of ΔΣ modulators will be used. This means that the non-linear quantizer is replaced by a white noise adder.

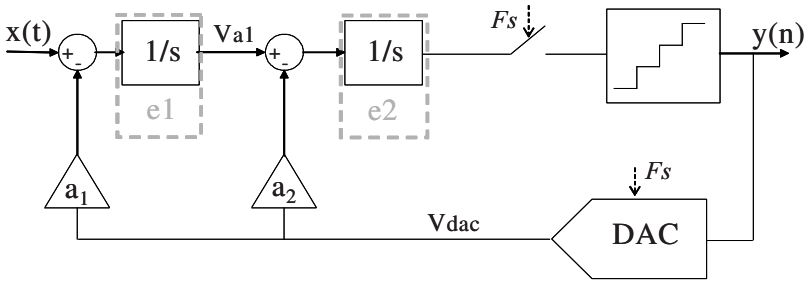

Figure 2. *Second order ΔΣ with NRZ feedback*

Estimation of integration errors

The input signal is continuous and directly applied to the loop filter; it is thus correctly processed by all the continuous time blocs preceding the sampler without introducing integration errors. Therefore to estimate the integration errors we simply assume that the input signal is nil.

Consider Δt the jitter error during the Nth clock period, that is to say from the instant t=nTS to t=(n+1)TS+Δt. Throughout the period, the voltage Vdac is constant and sent back to the loop filter trough a1 and a2, which is the principle of NRZ feedback DAC. The perturbation of the integration time due to the jitter Δt introduces two integration errors, e1 in the first integrator and e2 in the second stage of the modulator.

The error e1 is due to the fact that a1*Vdac is integrated during Ts+Δt instead of Ts. At the end of the nth clock period, that is to say at $t = (n+1)T_S + \Delta t$, the error introduced by jitter is equal to:

$$e1 = a_1 V_{dac} * \Delta t \tag{2}$$

This error is generated within the first stage of the ΔΣ thus an equivalent voltage error Ve1 at the input of the first integrator can be computed.

$$\int_{nT_S}^{(n+1)T_S+\Delta t} a_1 * V_{dac}\ dt = \int_{nT_S}^{(n+1)T_S} \left(a_1 * V_{dac} + a_1 * V_{dac} * \frac{\Delta t}{T_S} \right) dt \tag{3}$$

Therefore, we can write :

$$Ve1 = a_1 V_{dac} * \frac{\Delta t}{T_S} \tag{4}$$

In order to derive the power spectral density (PSD) of this error S_{ve} *(f)*, we can calculate the Fourier transform of its autocorrelation function. The autocorrelation function r_{Ve} of the error *Ve1* is given by:

$$\begin{aligned} r_{Ve1}(mT) &= E\left[\, Ve1(T) \cdot Ve1(T+mT)\, \right] \\ &= \left(\frac{a_1}{T_S} \right)^2 r_{Vdac}(mT) \cdot\ r_{\Delta t}(mT) \end{aligned} \tag{5}$$

where E denotes the expectation operator, r_{Vdac} and $r_{\Delta t}$ are respectively the autocorrelation functions of the feedback voltage and timing jitter. By applying the Fourier transform to (3), the error spectrum can be found:

$$S_{Ve1}(f) = \left(\frac{a_1}{T_S} \right)^2 S_{Vdac}(f) \otimes S\quad (f) \tag{6}$$

The symbol ⊗ represents the convolution operator.

If we multiply this spectrum by the signal transfer function STF of the modulator and replace the temporal jitter spectrum $S_{\Delta t}$ by the phase noise spectrum S_{θ}, the equation of the PSD of the error *e1* at the output of the converter can be computed.

$$S_{\Delta t}(f) = \left(\frac{T_S}{2\pi} \right)^2 S_{\theta}(f) \tag{7}$$

From equations (6) and (7), the expression of S_{Ve} at the output of the converter can be derived.

$$S_{Ve1}(f) = \left(\frac{a_1}{2\pi}\right)^2 \left[S_{Vdac}(f) \otimes S_{\theta}(f)\right] * STF(f) \quad (8)$$

Of course, the same calculation method can be applied to the error *e2*, introduced within the second stage of the modulator. The equation is just a little bit more complex because *e2* has got two components, the first part of the error is due to the single integration of $a_2 * V_{dac}$, and the second one to the double integration of $a_1 * V_{dac}$.

$$e2 = a_2 V_{dac} * \Delta t \left(1 + \frac{a_1}{a_2} T_S + \frac{a_1}{a_2} \frac{\Delta t}{2}\right) + V_{a1} * \Delta t \quad (9)$$

where V_{a1} is the output voltage of the first integrator, which is the integral of V_{dac}.

From this equation an equivalent second stage voltage error *Ve2* can be derived. Furthermore, the quantities *Ts* and Δt are quite smaller than 1; consequently two terms of (9) can be neglected and *Ve2* approximated to:

$$Ve2 \approx \left(a_2 V_{dac} + V_{a1}\right) \frac{\Delta t}{T_S} \quad (10)$$

Finally, if the Fourier transform of the autocorrelation function of *Ve2* is calculated and multiplied by the transfer function TF_{e2} between the input of the second stage and the output of the modulator, we can derive an expression for the PSD of *Ve2*.

Furthermore, we know that *Va1* is the continuous time integral of *Vdac*. The relation between those two signals is:

$$S_{Va1}(f) = \frac{a_1^2}{(2\pi f)^2} S_{Vdac}(f) \quad (11)$$

So, the PSD of *Ve2* is given by:

$$S_{Ve2}(f) = \frac{1}{(2\pi)^2} \left[\left[\left(a_2^2 + \frac{a_1^2}{(2\pi f)^2}\right) S_{Vdac}(f)\right] \otimes S_{\theta}(f)\right] * TF_{e2}(f) \quad (12)$$

In this chapter, the PSD expressions of the two integration errors have been calculated, in the special case of a second order delta sigma modulator with NRZ feedback DAC.

Estimation of the sampling error

In section 2, we have stated that one part of the jitter error is linked to the discretization of the input signal by the CTΔΣ. Even though this jitter degradation is easily

understandable, the input signal being sampled when it gets through the modulator, we lack a detailed explanation of the phenomenon allowing us to analytically define an exact formula of the sampling error PSD.

From extensive observations and simulations of jitter in CTΔΣ it comes out that, in NRZ feedback ΔΣ, the errors introduced by jitter in relation with the input signal are equal to the errors that would happen if the input signal was filtered by the STF of the modulator before being sampled. This behavioral analysis has no physical meaning since modeling a CTΔΣ by a STF equivalent block followed by a sampler is irrelevant. However it allows us to quantify the sampling error and to give an easy and understandable equation.

The PSD of the errors introduced by an isolated sampler is given in [5]:

$$S_{error}(f) = \left[\left(\frac{f}{F_s} \right)^2 S_X(f) \right] \otimes S_\theta(f) \tag{13}$$

If this equation is applied to our specific case, the following mathematical equation is obtained. This formula gives us the PSD of the errors introduced by clock jitter in relation with the input signal.

$$S_{Vin+jitter}(f) = \left[\left[\left(\frac{f}{F_s} \right)^2 S_{Vin}(f) \cdot STF(f) \right] \otimes S_\theta(f) \right] \tag{14}$$

From the three PSD equations, (6) (12) and (14), two essential remarks can be made. First, the dependency of jitter degradations to quantization noise, which is a specificity of CTΔΣ, is confirmed by (6) and (12). The second remark relates to the importance of phase noise profile. All formulas present a convolution involving phase noise, so the knowledge of the clock imperfections is a prerequisite for a good estimation of jitter degradations.

With the estimated PSD of all the errors introduced by the jitter in the CTΔΣ, it is quite simple to find the SNR degradation. Indeed, we just have to integrate (6), (12) and (14) on the right range of frequencies.

In section 4, we will express in figure some examples in order to attest of the formulas accuracy. First, the possible extension of those equations to generic converter architectures is discussed.

3.2 Nth order CTΔΣ with NRZ feedback

The above calculations have been conducted in the special case of a 2nd order converter to facilitate the comprehension of the phenomena; it is obviously possible to do exactly the same work with other architectures. However, the computation of the jitter equations, already time-consuming with the second order modulator, is becoming almost endless as soon as the order of the loop filter is increased.

In reality, it is not necessary to extract the whole set of equations every time the modulator architecture is changed. In fact, in high order modulators, the errors introduced by the integration stages that are close to the quantizer have a small influence on performances because there are shaped by the loop. Thus the set of equations, defined in the preceding section can be considered as a good approximation of the impact of jitter for every modulator with NRZ feedback DAC.

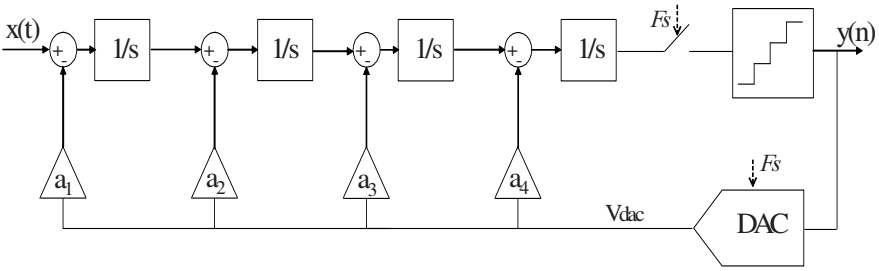

Figure 3. *4th order ΔΣ converter with NRZ feedback*

Let's consider a 4th order continuous time delta sigma converter with NRZ feedback DAC. We know from section 2 that this modulator owns one sampling error and 4 integration errors.

The conversion principle of this particular converter is comparable to the second order modulator described previously (feedback structure and NRZ DAC). Thus the formulation of the sampling error PSD is not changed. Therefore, equation (14) can be used again to estimate the impact of jitter, related to the input signal, for the considered 4th order modulator.

This result does not mean that the power of the sampling error introduced by the clock imperfections is similar. It is well known that the transfer function STF(f) of a CTΔΣ modulator depends on the loop filter architecture. So, the signal transfer function of a 4th order modulator is different from the STF of a second order modulator. Therefore, the numerical value of the sampling error PSD will be different as soon as the modulator is changed.

The number of integration error is equal to the number of integrators used to realize the continuous time loop filter. So, in the considered 4th order modulator, there is 4 integration errors.

The errors introduced inside the third and fourth stages of the loop filter will have a really small impact on the performances of the modulator in comparison with the integration errors of the first two stages. Integration errors are shaped by the loop transfer functions. Thus, the jitter error computation can be wisely reduced to the calculation of the first two integration errors only. The expressions for those two integration errors have already been derived in section 2, see equations (6) and (12).

So the set of equations derived for the second order modulator can be used without any modification to compute the degradations introduced by jitter for every CTΔΣ converter with NRZ feedback DAC.

3.3 Jitter compensation techniques : Switched Capacitor feedback and Finite Impulse Response DAC

In the last decade, different methods have been proposed to reduce the jitter sensitivity of CTΔΣ. Switched Capacitor (SC) DAC [6]-[8] and FIRDAC [9] [10] are two techniques which have proven their efficiency. If the computation principle previously described is applied to ΔΣ using those correction systems, the resultant benefit can be evaluated.

The main idea behind those two correction techniques is to reduce the impact of jitter by making the feedback DAC completely independent of the clock imperfections. In a continuous time delta sigma converter, the outputs of DACs are integrated by the loop filter. Therefore, the important parameter in a CTΔΣ is not the value of the current sent back in the conversion loop but the quantity of charges integrated during the clock period by the continuous time filter.

Switched capacitor DAC

Let's consider again the case of the second order modulator with a feedback architecture, see figure 2. But this time the NRZ feedback scheme is replaced by a switched capacitor DAC.

With this kind of digital to analog converter, the quantity of charges sent back in the loop during a clock period is controlled by the charge and the discharge of a capacitor. If the SC DAC and the loop filter are designed neatly, that is to say that time constants for the charge and discharge of the capacitors are quite smaller than the clock period, the quantity of charge sent back in the loop is independent of jitter. Therefore, the error *e1* introduced in the first integrator is nil and the integration error of the second stage *e2* is strongly reduced. No details of the computation of the following equations are given here, because the derivation of those two formulas is really similar to the work presented in section 3.1.

$$S_{Ve1}(f) = 0 \tag{15}$$

$$S_{Ve2}(f) = \frac{1}{(2\pi)^2}\left[\left[\frac{a_1^{\,2}}{(2\pi f)^2} S_{Vdac}(f)\right] \otimes S_{\theta}(f)\right] * TF_{e2}(f) \tag{16}$$

The power spectral density of the sampling error is modified too by the introduction of the SC DAC. Contrarily to the modulator with NRZ feedback, the sampling er-

ror is not sent back integrally in the conversion loop when SC technique is used. Therefore, the PSD of the sampling error is shaped by the loop filter:

$$S_{Vin+jitter}(f) = \left[\left[\left(\frac{1}{2\pi}\right)^2 S_{Vin}(f) \cdot STF(f)\right] \otimes S_{\theta}(f)\right] * TF_{e2}(f) \quad (17)$$

If the equations (15), (16) and (17) are compared with the equations derived in section 3.1 (formulas (6), (12) and (14)), the benefit from the utilization of switched capacitor DAC is clearly visible. Indeed the integration errors are reduced and the sampling errors are shaped by the conversion loop. However, the PSD of clock jitter errors is not equal to zero; this correction system is therefore not perfect.

In this paragraph, the case of switched capacitor ADC has been analyzed in details and the set of equations providing the jitter errors PSD has been derived. This study has shown that the calculations are really comparable to those detailed in paragraph 3.1. Some numerical results for a 3rd order modulator with a SC DAC will be given in section 4.

Finite impulse response DAC

The principle of this jitter correction is again to reduce the impact of jitter on the signal sent back in the loop filter by the DACs. However the strategy employed is completely different from the one used with SC DAC. The idea here is to spread the feedback current over several periods in order to limit the jitter influence. With the FIRDAC technique, the impact of clock imperfections are not corrected on each period, as it is the case with SC DAC. Nevertheless, jitter error PSD is reduced by a simple effect of averaging.

The modifications on the NRZ feedback DAC structure are really small. The digital to analog converters are just split in smaller elements in order to reduce the instantaneous current sent back in the loop during each clock period. On figure 4, a temporal diagram example of DAC currents is represented with a classical NRZ feedback and with a 4 stages FIRDAC correction.

FIRDAC technique is definitely less efficient than SC DAC, because it only realize an averaging of jitter errors. However, its implementation is easier and the impact on the analog loop filter is usually lower than the integration of switched capacitor DAC.

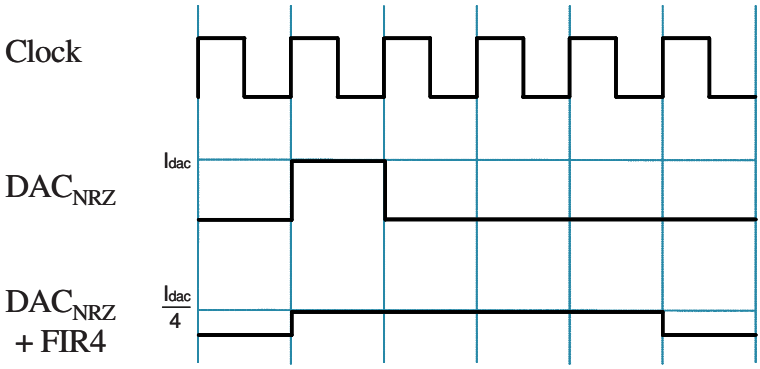

Figure 4. *FIRDAC impact on the feedback current*

4. VALIDATION OF THE ANALYTICAL JITTER ERRORS ESTIMATION

In the previous sections, our approach to estimate the impact of clock jitter on the output signal of CTΔΣ has been explained. To prove the accuracy of the given formulas, they will now be compared with simulations.

4.1 Clock jitter modeling

In order to simulate the impact of jitter on CTΔΣ, temporal models of non-ideal clocks are needed. To realize clock signals presenting different phase noise profile, a voltage controlled oscillator (VCO) has been modeled. This frequency synthesis circuit has been chosen because it is simple enough to be accurately modeled and it allows us to generate a wide range of jittered clocks. This non ideal clock model has been created with Matlab Simulink blocks and used to drive CTΔΣ modulators.

The phase noise profile of our VCO model is characterized by a -20dB/decade slope and a phase noise floor. The decreasing phase noise slope is a classical feature of an oscillator while the phase noise floor represents the bufferization of the clock signal. Thus, this model possesses two tuning parameters, the levels of the noise slope and noise floor, allowing us to generate different non ideal clocks. Moreover this VCO has been included in a phase locked loop (PLL) to create a more complex jittered clock.

The VCO phase noise profile can be easily translated to temporal imperfections using the classical relations between phase noise and temporal jitter [11]. In fact, the phase noise slope of the VCO corresponds to an accumulated Gaussian timing error while phase noise floor relates to an independent Gaussian temporal error. It is those two temporal imperfections that have been used to create the Matlab Simulink model of VCO.

The model accuracy has been validated using phase noise profile comparisons. Figure 5 shows a validation example of the VCO model. The black curve is the theoretical phase noise level while the grey one is the phase noise profile extracted from the simulation of the Matlab VCO model.

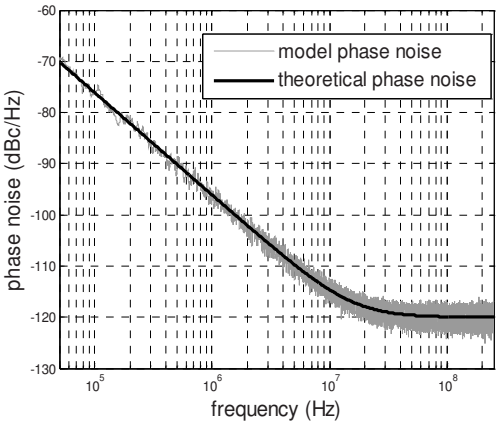

Figure 5. *VCO phase noise model validation*

4.2 Jitter equations comparisons with simulations

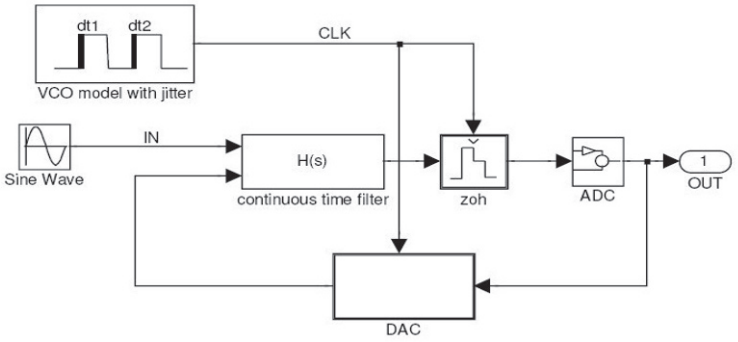

Figure 6. *CTΔΣ simulation with non ideal clock*

From the equations stated in section 3, we know that jitter degradations are related to the architecture of the converter, the phase noise profile and the input signal PSD. To prove the precision of our jitter impact computation, formulas and simulations have been compared for different CTΔΣ architecture and several phase noise profiles. The comparisons have focused on two criterions, the converter output PSD and the SNR value. To simulate the impact of jitter on the performances of CTΔΣ, the VCO model

described in the preceding paragraph has been used to drive different converters, see figure 6.

To explore the architecture dependency, three different converter architectures have been used:

– A 2nd order feedback modulator with NRZ DAC
– A 4th order feedback modulator with NRZ DAC
– A 3rd order feedback modulator with Switched capacitor DAC

All modulators used a 4-bits internal quantizer. Moreover, two sinusoidal signals with the same amplitude but different frequencies, Fin1=5MHz and Fin2=25MHz, have been used to illustrate the relation between the jitter degradation and the input PSD.

Finally, to demonstrate how the clock phase noise profile modifies the errors introduced by jitter, two dissimilar clocks have been defined. The frequency of both clocks is 500MHz. The first clock has a flat phase noise profile at -120dBc/Hz, whereas the second clock is a type 1 PLL, with a 500kHz cut off frequency. The PLL phase noise is equal to -90dBc/Hz at 500kHz and the phase noise floor is located at -120dBc/Hz. The phase noise profiles of those two clocks are represented on figure 7.

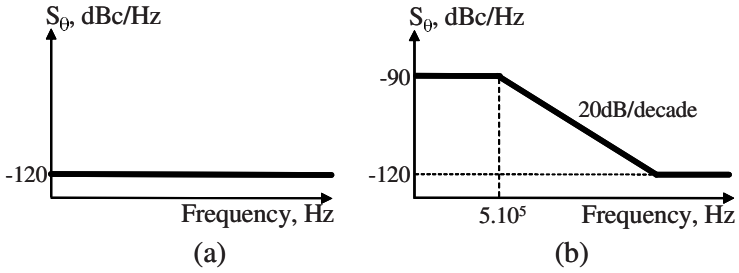

Figure 7. *Clocks phase noise profiles, (a) white noise, (b) PLL*

For all the possible combinations of architecture, input signal and clock, the converter output PSD and the SNR from 0 to 10 MHz have been derived from equations and simulations.

For each test case, the correct superposition of the simulated PSD with the calculated one demonstrates the reliability of our jitter impact estimation method. PSD comparison examples, with the two non ideal clocks, are shown in figures 8 and 9. The out of band PSD is not shown on those figures because it is dominated by quantification noise. The curves correspond to the output signals of the 2nd order feedback modulator with NRZ DAC and a sinusoidal input signal at 5MHz.

The PSD superpositions are evident, and they are confirmed by the calculation of SNR values. For the white phase noise clock comparison case, the SNR achieved by the simulated converter is equal to 64.82dB and the SNR given by the equation is 64.50dB. In the second test case, the SNR values are respectively 62.63dB and 62.59dB.

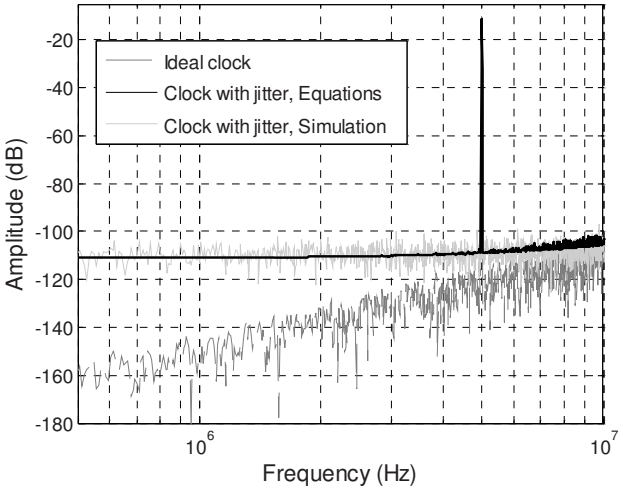

Figure 8. *Output spectrum comparison of a 2nd order CTΔΣ controlled by the white phase noise clock*

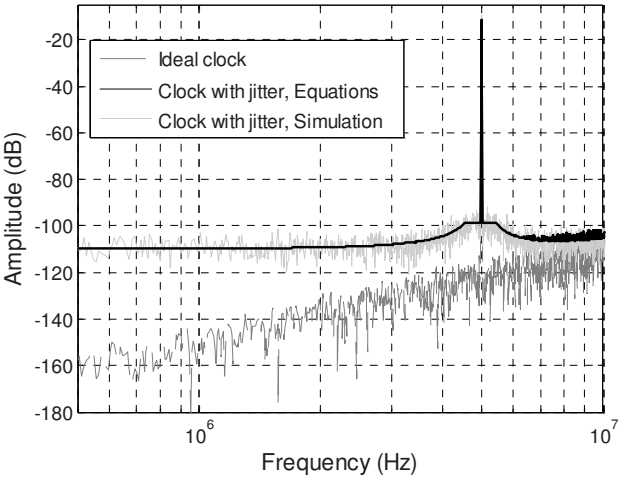

Figure 9. *Output spectrum comparison of a 2nd order CTΔΣ controlled by the PLL clock*

The same PSD and SNR comparisons have been done with the others converters and clocks and resulted in comparable conclusions on the accuracy of the jitter estimation method. The SNR values of the 12 test cases described above are summarized in table 1. The SNR from simulations are in regular characters, while those from formulas are in bold font. For information, the SNR value of the input signal sampled by non ideal clocks is also given in table 1. Those numbers correspond to the degradations introduced by a jittered clock if a DTΔΣ was used.

The SNR comparison, encapsulated in table 1, illustrates the accuracy of the mathematical jitter error estimation method presented in this paper. The discrepancies between calculated and simulated SNR values are indeed really small, always less than 1 dB.

Moreover, the jitter degradation dependence to the three key parameters (modulator architecture, phase noise and input signal) is highlighted by both simulations and equations. The validity of our approach of the jitter problem and the accuracy of the equations are clearly demonstrated by the given results.

	Ideal Clock	Clock 1 : white noise		clock 2 : PLL	
		Fin1	*Fin2*	*Fin1*	*Fin2*
Sampled input signal	∞	87.06dB **87.02dB**	73.17dB **73.04dB**	66.81dB **67.10dB**	72.21dB **72.99dB**
2nd order modulator with NRZ feedback	72.5dB	64.82dB **64.50dB**	63.73dB **63.94dB**	62.63dB **62.59dB**	63.64dB **63.91dB**
4th order modulator with NRZ feedback	95dB	71.05dB **70.65dB**	69.10dB **68.96dB**	65.20dB **65.53dB**	68.90dB **68.92dB**
3rd order modulator with SC return	86.6dB	80.80dB **81.25dB**	83.58dB **83.96dB**	66.17dB **66.81dB**	83.25dB **83.91dB**

Table 1. *SNR comparisons*

5. CONCLUSION

In this paper, a new analytical approach to solve the problem of clock jitter in CTΔΣ is presented. By focusing on continuous time components and signals, two kinds of jitter errors have been identified and mathematical equations of those errors PSD have been derived. Finally, the accuracy of the jitter errors formulas has been proven with exhaustive comparisons with simulated converters controlled by non ideal clocks.

The provided results quite clearly confirm the relation between the jitter errors and the converter architecture. This strong relationship automatically draws aside the possibility to derive a single and simple jitter error equation as it is the case for discrete time converters. However, the presented work provides an efficient mathematical method to specify the clock phase noise profile needed to achieve the targeted performances of CTΔΣ converters.

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