Chapter 1
Introduction

Kevin Zhang

Advancement of semiconductor technology has driven the rapid growth of very large scale integrated (VLSI) systems for increasingly broad applications, including high-end and mobile computing, consumer electronics such as 3D gaming, multi-function or smart phone, and various set-top players and ubiquitous sensor and medical devices. To meet the increasing demand for higher performance and lower power consumption in many different system applications, it is often required to have a large amount of on-die or embedded memory to support the need of data bandwidth in a system. The varieties of embedded memory in a given system have also become increasingly more complex, ranging from static to dynamic and volatile to nonvolatile.

Among embedded memories, six-transistor (6T)-based static random access memory (SRAM) continues to play a pivotal role in nearly all VLSI systems due to its superior speed and full compatibility with logic process technology. But as the technology scaling continues, SRAM design is facing severe challenge in maintaining sufficient cell stability margin under relentless area scaling. Meanwhile, rapid expansion in mobile application, including new emerging application in sensor and medical devices, requires far more aggressive voltage scaling to meet very stringent power constraint. Many innovative circuit topologies and techniques have been extensively explored in recent years to address these challenges.

Dynamic random access memory (DRAM) has long been an important semiconductor memory for its well-balanced performance and density. With increasing demand for on-die dense memory, one-transistor and one-capacitor (1T1C)-based DRAM has found varieties of embedded applications in providing the memory bandwidth for system-on-chip (SOC) applications. With increasing amount of on-die cache memory for high-end computing and graphics application, embedded DRAM (eDRAM) is becoming a viable alternative to SRAM for large on-die memory. To meet product requirements for eDRAM while addressing continuous technology scaling, many new memory circuit design technologies, which are often

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drastically different from commodity DRAM design, have to be developed to substantially improve the eDRAM performance while keeping the overall power consumption at minimum.

Solid-state nonvolatile memory (NVM) has played an increasingly important role in both computing and consumer electronics. Many new applications in most recent consumer electronics and automobiles have further broadened the embedded application for NVM. Among various NVM technologies, floating-gate-based NOR flash has been the early technology choice for embedded logic applications. With technology scaling challenges in the floating-gate technologies, including the increasing need for integrating NVM along with more advanced logic transistors, varieties of NVM technologies have been extensively explored, including alternative technology based on charge-trapping mechanism (Fig. 1.1). More efficient circuit design techniques for embedded flash also have to be explored to achieve optimal product goals.

With increasing demand of NVM for further scaling of the semiconductor technology, several emerging memory technologies have drawn increasingly more attention, including magnetic RAM (MRAM), phase-change RAM (PRAM), and ferroelectric RAM (FeRAM). These new technologies not only address some of the fundamental scaling limits in the traditional solid-state memories, but also have brought new electrical characteristics in the nonvolatile memories on top of the random accessing capability. For example, MRAM can offer significant speed improvement over traditional floating-gate memory, which could open up whole new applications. FeRAM can operate at lower voltage and consume ultra low power, which has already made it into "smart-card" marketplace today. These new memory technologies also require a new set of circuit topologies and sensing techniques to maximize the technology benefits, in comparison to the traditional NVM design.

With rapid downward scaling of the feature size of memory device by technology and drastic upward scaling of number of storage elements per unit area, process-induced variation in memory has become increasingly important for both memory technology and circuit design. Statistical design methodology has now

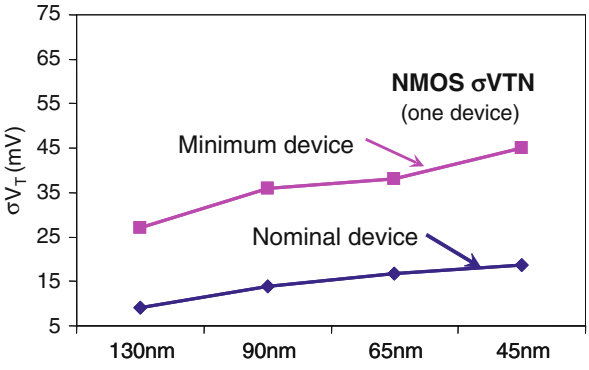

Fig. 1.1 Transistor variation trend with technology scaling [1]

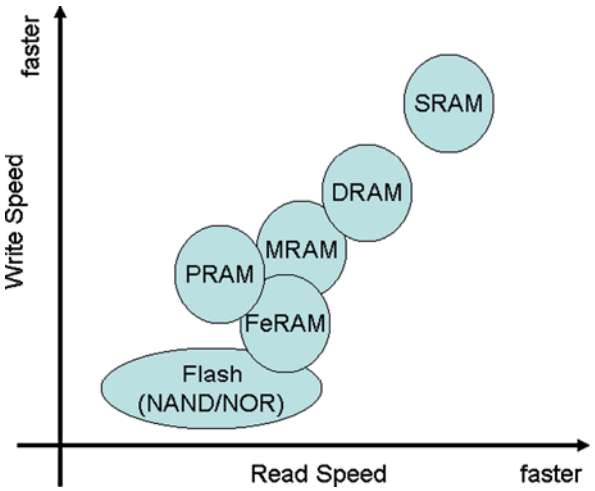

Fig. 1.2 Relative performance among different types of embedded memories

become essential in developing reliable memory for high-volume manufacturing. The required statistical modeling and optimization capability has grown far beyond the memory cell to comprehend many sensitive peripheral circuits in the entire memory block, such as critical signal development paths. Advanced statistical design techniques are clearly required in today's memory design.

In traditional memory field, there is often a clear technical boundary between different kinds of memory technology, e.g., SRAM and DRAM, volatile and non-volatile. With growing demand for on-die memory to meet the need of future VLSI system design, it is very important to take a broader view of overall memory options in order to make the best design tradeoff in achieving optimal system-level power and performance. Figure 1.2 illustrates the potential tradeoff among these different memories. With this in mind, this book intends to provide a state-of-the-art view on most recent advancements of memory technologies across different technical disciplines. By combining these different memories together in one place, it should help readers to gain a much broadened view on embedded memory technology for future applications. Each chapter of the book is written by a set of leading experts from both industry and academia to cover a wide spectrum of key memory technologies along with most significant technical topics in each area, ranging from key technical challenges to technology and design solutions. The book is organized as follows:

1.1 Chapter 2: Embedded Memory Architecture for Low-Power Application Processor, by Hoi Jun Yoo

In this chapter, an overview on embedded memory architecture for varieties of mobile applications is provided. Several real product examples from advanced application processors are analyzed with focus on how to optimize the memory

architecture to achieve low-power and high-performance goal. The chapter intends to provide readers an architectural view on the role of embedded memory in mobile applications.

1.2 Chapter 3: Embedded SRAM Design in Nanometer-Scale Technologies, by Hiroyuki Yamauchi

This chapter discusses key design challenges facing today's SRAM design in nano-scale CMOS technologies. It provides a broad coverage on latest technology and design solutions to address SRAM scaling challenges in meeting power, density, and performance goal for product applications. A tradeoff for each technology and design solution is thoroughly discussed.

1.3 Chapter 4: Ultra Low Voltage SRAM Design, by Naveen Verma and Anantha P. Chandrakasan

In this chapter, an emerging family of SRAM design is introduced for ultra-low-voltage operation in highly energy-constrained applications such as sensor and medical devices. Many state-of-the-art circuit technologies are discussed for achieving very aggressive voltage-scaling target. Several advanced design implementations for reliable sub-threshold operation are provided.

1.4 Chapter 5: Embedded DRAM in Nano-Scale Technologies, by John Barth

This chapter describes the state-of-the-art eDRAM design technologies for varieties of applications, including both consumer electronics and high-performance computing in microprocessors. Array architecture and circuit techniques are explored to achieve a balanced and robust design based on high-performance logic process technologies.

1.5 Chapter 6: Embedded Flash Memory, by Hideto Hidaka

This chapter provides a very comprehensive view on the state of embedded flash memory technology in today's industry, including process technology, product application, and future trend. Several key technology options and their tradeoffs are discussed. Product design examples for micro-controller unit (MCU) are analyzed down to circuit implementation level.

1.6 Chapter 7: Embedded Magnetic RAM, by Hideto Hidaka

Magnetic RAM has become a key candidate for new applications in nonvolatile applications. This chapter introduces both key technology and circuit design elements associated with this new technology. The future application and market trend for MRAM are also discussed.

1.7 Chapter 8: FeRAM, by Shoichiro Kawashima and Jeffrey S. Cross

This chapter introduces the latest material, device, and circuit advancement in ferroelectric RAM (FeRAM). With excellent write-time, random accessing capability, and compatibility with logic process, FeRAM has penetrated into several application areas. Real product examples are provided along with future trend of the technology.

1.8 Chapter 9: Statistical Blockade: Estimating Rare Event Statistics for Memories, by Amith Singhee and Rob A. Rutenbar

This chapter introduces a comprehensive statistical design methodology that is essential in today's memory design. The core of this methodology is called statistical blockade and it combines Monte Carlo simulation, machine learning, and extreme value theory in effectively predicting rare failure (> 5 sigma) event. Real design examples are used to illustrate the benefit of the methodology in memory design and optimization.

Reference

1. K. Kuhn, "Reducing Variation in Advanced Logic Technologies: Approaches to Process and Design for Manufacturability of Nanoscale CMOS," IEEE IEDM Tech Digest, pp. 471–474, Dec. 2007.