Chapter 8
Magnetic Nanowires for Domain Wall Logic and Ultrahigh Density Data Storage

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Abstract Spintronics describes the concept of attempting to use both the charge and the spin on the electron in microelectronic devices [1, 2]. One of the most highly sought after functionalities in microelectronics is non-volatility, i.e. the ability to retain memory even when power is removed. This is particularly true as the popularity of mobile electronic communication and computing devices grows. In principle, ferromagnetic materials could provide this functionality, due to the hysteresis, and hence memory, that accompanies most ferromagnets. Unfortunately, no suitable room temperature ferromagnetic semiconductor material has yet been identified [3]; the most common ferromagnetic materials are metals. The aim of this research has been to see how far we can push the properties of basic ferromagnetic metallic alloys, which are usually considered to have relatively simple magnetic and electrical properties, towards highly functional devices which mimic and complement the digital logic functions and non-volatile data storage functions of semiconductor microelectronics. Using the concept of the domain wall conduit, we show how information can be represented, moved, processed and stored in networks of ferromagnetic nanowires.

8.1 Domain Wall Propagation and Nucleation

All of the devices described in this chapter are based upon magnetic nanowires made from the common ferromagnetic alloy Permalloy ($Ni_{80}Fe_{20}$). Magnetic nanowires are nanometer-sized magnetic structures which are artificially fabricated using laboratory-scale versions of the lithographic techniques commonly used in microchip manufacture. In particular, the work in this chapter uses either electron beam lithography (EBL) or focused ion beam (FIB) milling [4]. A typical

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process will involve the deposition of a thin magnetic film, either using thermal evaporation or sputter deposition and the exposure of a computer-generated pattern by rastering either a focused electron beam (EBL) or a focused gallium ion beam (FIB). A development and pattern transfer step then transfers the exposed image into the deposited magnetic metal. The ability to create high-definition shapes of precisely the designer's choice is extremely important, since the underlying principle at work throughout this research is that magnetic properties may be artificially modified by changing the shape and size of the nanostructure. This principle is not commonly seen on the macroscopic scale: the coercivity and the anisotropy of a bulk material are usually intrinsic properties which do not depend strongly on the shape of the sample. On the nanometer scale, however, the local demagnetizing fields are of comparable strength to the exchange fields (the quantum mechanical interaction responsible for ferromagnetism). A rich interplay results which leads to magnetic properties being strongly dependent on shape and size.

Magnetic properties throughout this chapter are measured using a high-sensitivity laser probe [5] based on the Magneto Optical Kerr Effect (MOKE) [6]. The Kerr effect causes the polarization state of light to be slightly modified when it is reflected from a magnetic surface by an amount that is proportional to the component of magnetization in a given direction. Although the polarization rotations are small (typically 0.1° if all of the light is focused onto magnetic material, and proportionately less if the nanostructure is smaller than the focused beam size), MOKE is an excellent highly localized magnetometry.

Figure 8.1 shows an example of a magnetic nanowire that behaves as a so-called domain wall conduit. The nanowire is made from 8 nm thick Permalloy and is fabricated by electron beam lithography. One sees two hysteresis loops measured from the nanowire using the MOKE magnetometer described above. We apply a magnetic field which is oriented along the wire axis for most of its sweep, but which rotates to 45° towards the extrema of the loop. This guarantees the starting magnetization state in both arms of the L-shaped nanowire as the applied field sweeps back towards zero. We generate such an applied field sequence by controlling the current in two pairs of coils which apply fields in the X- (nanowire axis) and Y-(transverse) directions. If, as in the upper hysteresis loop, we choose the relative signs of the X- and Y-fields such that the 45° pulse is tangential to the corner of the L-shaped nanowire, then no domain wall exists in the wire and so the coercivity corresponds to a nucleation-limited reversal. In this case, we measure a coercivity of 205 Oe, which we define to be the *nucleation field*, H_n. If we now reverse the sign of the y-field, the 45° pulse becomes perpendicular to the corner, resulting in a single domain wall being created there. The coercivity is now defined as the *propagation field*, H_p, since reversal in the main length of the wire is achieved simply by pushing that already-created domain wall around the corner and along the wire. Remarkably, we find in the lower hysteresis loop a value of just 3 Oe for H_p. The coercivity of the nanowire has been modified by a factor of 65 simply by the presence of absence of a single domain wall.

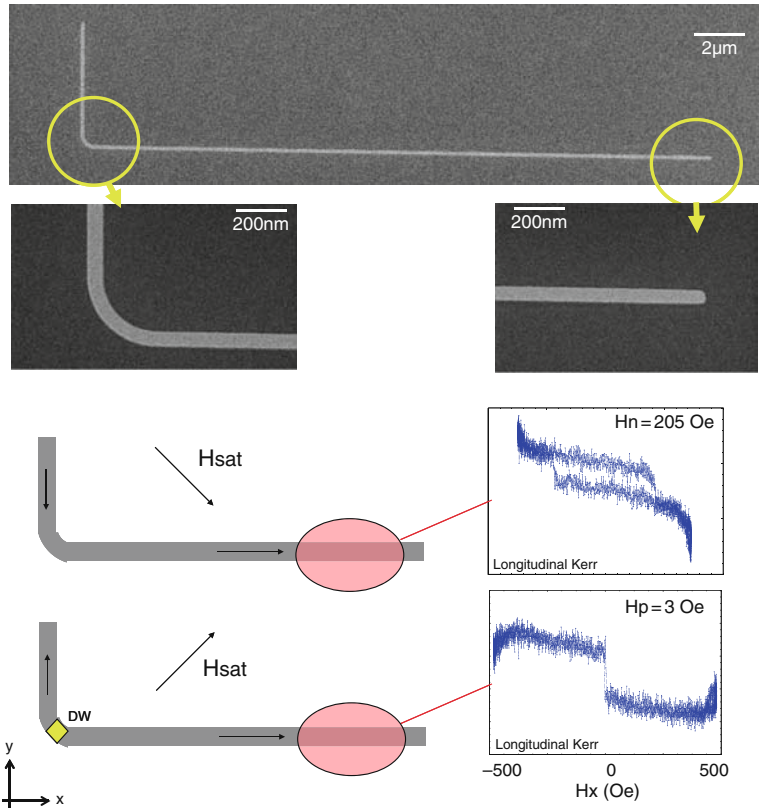

Fig. 8.1 Domain nucleation and domain wall propagation in a 120 nm wide, 8 nm thick Permalloy nanowire

8.2 Domain Wall Conduits

When the ratio between H_p and H_n is substantial, we describe the magnetic nanowires as *domain wall conduits*. This is because if one applies a magnetic field H in the range $H_p < H < H_n$, then the nanowire will accept any domain wall introduced to it and propagate it along the wire, but will not reverse if no domain wall is given. For the nanowires shown here, this range is very large (any field between 3 Oe and 205 Oe in the case of Fig. 8.1 will result in domain wall conduit behaviour). There is thus a parallel between electrical conductors and domain wall conduits: an electrical conductor transports the electrical potential applied at one end to the other by a flow of electrons; a domain wall conduit transports the magnetization direction applied at one end to the other by the flow of a single domain wall. Interestingly, electrical conduction results in losses due to the resistance of the conductor; the potential at the far end will always be slightly different to the potential at the near end. Although

there are also losses in the transport of a domain wall through spin wave emission by the wall as it moves, these energy losses are exactly compensated by the energy absorbed from the externally applied magnetic field, *H*. The externally applied magnetic field therefore has a parallel to a power supply, and the domain wall conduit should be considered as being an active component that can draw on that power supply, rather than the simpler passive 2-terminal component that is an electrical conductor. The propagation field is loosely analogous to a contact potential: it is the offset field which must be overcome before domain wall conduction will occur. The nucleation field is loosely analogous to breakdown: it is the strength of field at which the magnetization state of the domain wall conduit no longer relates to the input, but it is overridden by the externally applied magnetic field or power supply.

Domain wall conduits allow us to propagate magnetization states from one place to another, and so for spintronic applications it is natural to assign those magnetization states to Boolean states, allowing us to move information. We define a Boolean '1' as being when the magnetization direction is parallel to the direction in which information flows, and a Boolean '0' as being when the magnetization direction is anti-parallel to the direction in which information flows.

There is an additional complexity in propagating information through nanowire domain wall conduits, caused by the vector nature of magnetization. Figure 8.2 demonstrates the problem. Suppose we wish to propagate a data sequence made up of 1s and 0s. Domain walls in nanowires carry a magnetic charge, due to the divergence of magnetization which occurs at the wall. Walls that lie between the two heads of the magnetization arrows are called 'head-to-head' domain walls and carry a positive charge (since the magnetization has a positive divergence in the vicinity of the wall). Conversely, walls that lie between the two tails of the magnetization arrows are called 'tail-to-tail' domain walls and carry a negative charge. When a magnetic field is applied to the domain wall, positive walls move in the direction of the field, but negative walls move against the direction of the field. Consequently, any data pattern that is more complex than simply all 1s will not propagate correctly; rather, the 1s will expand and annihilate the 0s.

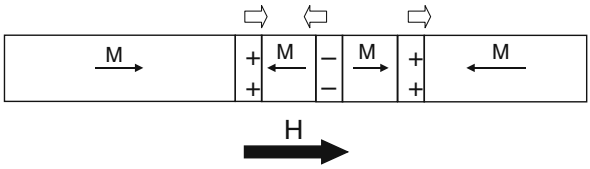

Fig. 8.2 The problem of propagating a data pattern in a nanowire under an externally applied magnetic field, *H*. The *white arrows* show the direction of motion of the different domain walls

What is required is some form of shift register which can be used to pump both head-to-head and tail-to-tail domain walls in the same direction. One possible approach to solving this problem is the use of spin-momentum transfer, in which a spin-polarized electrical current is used to drive the domain walls through the nanowire [7–10]. Spin-momentum transfer through a domain wall does not depend

upon the sign of the charge carried by the wall, and so all walls move in the same direction. However, this phenomenon is relatively weak and is not yet well understood. While it may provide an interesting solution in the future, at this stage we wish to find a way of using externally applied magnetic fields to pump the data. In particular, we choose to use devices that are constructed to operate within a globally applied rotating magnetic field. This rotating field acts as power supply and clock for all of the signals within a network of magnetic nanowires. Providing that the magnitude of the field is between the propagation and nucleation fields of the wires, the field serves to propagate domain walls around the network. This provides the basic interconnect architecture. To realize a proper shift register (and indeed other more complex logic functions), additional functionality must be created by careful shaping of the nanowires themselves.

8.3 The NOT Gate and Shift Register Element

Figure 8.3 shows a nanowire domain wall conduit which has been shaped into a cusp. See [11] for experimental detail. As the nanowire turns through the first quarter cycle of the cusp, the magnetization attempts to remain parallel to the nearest edge, in order to minimize its potential energy (the principle of shape anisotropy). The magnetization therefore rotates with the cusp. During the second quarter cycle of the cusp, the magnetization continues rotating, with the result that the magnetization on the input side of the cusp is 180° rotated with respect to that on the output side. There are two consequences of this rotation. The first is that data

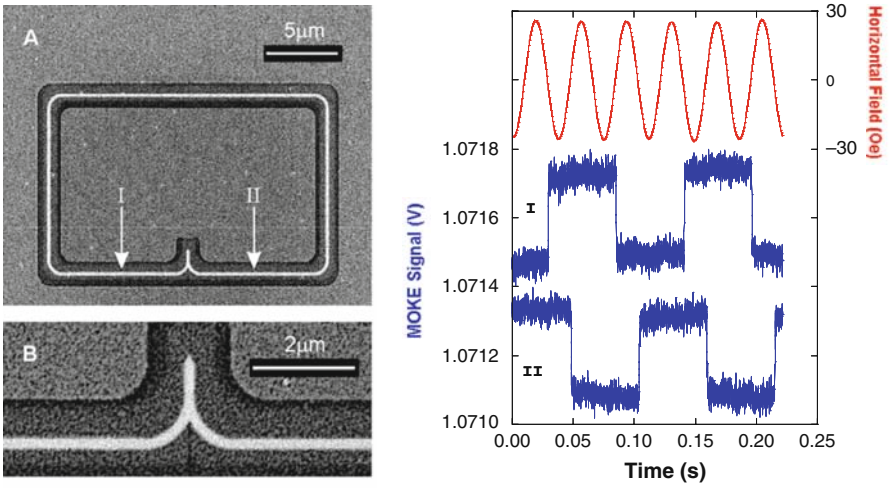

Fig. 8.3 A NOT gate in a closed loop to form a synchronous *ring* oscillator. The bright *white* shade is 5 nm thick Permalloy. Signal measurements are made by MOKE at the two positions I and II. The device is bathed in an in-plane rotating magnetic field, one component of which is plotted

values (as represented by the magnetization direction) have been inverted, i.e. we have performed the Boolean NOT function. The second is that we have introduced a synchronous delay of one half-cycle of the externally applied rotating field. Wherever there is a synchronous delay in digital electronics, there is an associated memory function and the possibility of shift register action.

The simplest way to test a NOT gate is by connecting its output to its input and thus forming a ring oscillator, as shown experimentally in Fig. 8.3. While in microelectronics this would result in a high-frequency oscillation, the frequency of which would be determined by the propagation delay on the gate, the synchronous nature of domain wall logic leads to a slightly different result. Figure 8.4 shows the equivalent electronic circuit. The half-cycle synchronous delay associated with propagating the domain wall through the cusp (or, put another way, because 1s and 0s propagate half a clock cycle apart in this architecture, the output of the NOT function must change half a cycle after its input) is shown as a T/2 delay, where T is the period of the rotating field. Additionally, there is a further delay of T due to the synchronous way in which the domain walls will move through the loop connecting the output to the input. The total loop time is therefore 3T/2, which simple analysis shows will lead to a self-sustained oscillation with a periodicity of 3T.

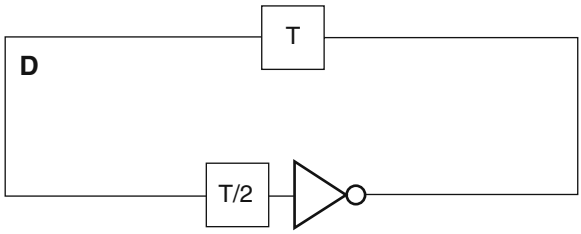

Fig. 8.4 The equivalent electronic circuit for the synchronous *ring* oscillator shown in Fig. 8.3. The *square blocks* are delay elements; *T* is the periodic time of the rotating magnetic field

Figure 8.3 shows the result of measuring the magnetization on firstly the input arm I and then the output arm II of the NOT gate using the MOKE laser spot while the entire chip is bathed in a rotating magnetic field. All of the expected features are visible. There is a half clock cycle delay between the rising edge on the input of the gate and the corresponding falling edge on the output of the gate. The periodicity of the result is also seen to be three times the rotating field frequency, as expected. Although in this experiment we do not see the domain wall directly, the response periodicity of 3T is the signature that everything is functioning correctly. See [12] for direct magnetic force microscopy images of the domain wall moving around the loop and through the gate.

Figure 8.5 demonstrates the ability to concatenate 11 NOT gates to form a serial shift register [11]. The measured circuit response shows a periodicity of 13*T* (*T* is the periodicity of the rotating field). This is exactly what would be expected: there is a loop delay time of 11/2 *T* due to the *T*/2 delay introduced by each of the 11 NOT gates, and then there is an extra *T* delay for the closed loop, making a total loop delay of 13/2 *T*, and hence an oscillating periodicity of 13*T*. Note in particular

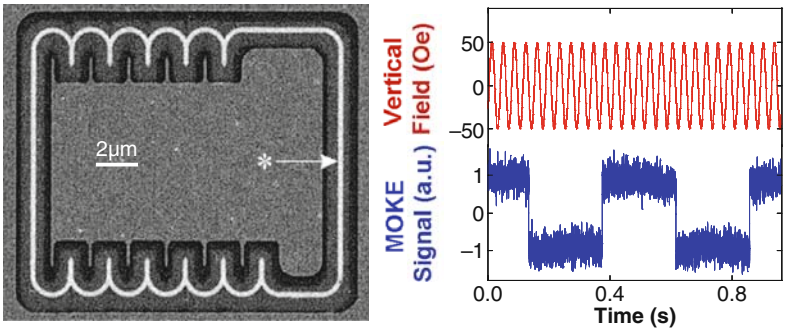

Fig. 8.5 Eleven NOT gates connected to form a serial shift register. A MOKE measurement at the asterixed point shows a synchronous oscillation at 1/13th of the rotating field frequency (one component of which is plotted)

that both positively charged head-to-head and negatively charged tail-to-tail domain walls are circulating in the same direction around the loops of Figs. 8.3 and 8.5 Unlike the simple case of Fig. 8.2, the propagation direction is determined by the NOT gate/shift register elements (and the relationship of the sense of their cusp to the sense of the externally applied rotating field) and not by the magnetostatic charge on the domain wall.

By extending the central stub of the NOT gate, an interim copy of the data held in the gate can be accessed. This allows a variation on the shift register theme to be formed, namely a serial-in-parallel-out (SIPO) shift register. Figure 8.6 shows an example of a ring oscillator connected to a SIPO shift register formed from a chain of NOT gates with accessible stubs. The ring oscillator in this case is simply providing a convenient signal to trace through the shift register. The shift in the MOKE signal as we move the laser probe from one nanowire to the next shows the correct operation.

The twists on the end of the nanowires perform an important role by preventing domain walls from reflecting and re-entering the system. Depending upon the precise shape of the end of a nanowire, a domain wall may or may not annihilate. If it does not annihilate, it will be back-propagate half a clock cycle later and may interfere with the correct operation of the logic gates. If annihilation at the end of the conduit cannot be guaranteed, the conduit can be correctly terminated by ensuring that there are two 90° corners between its end and the final logic element. The 180° turn forms what we refer to as a 'domain wall black hole': should a domain wall enter into it and not annihilate at the end, the rotating field will be unable to back-propagate it through the double corner, since these corners are of the wrong chirality. In the rotating field scheme, whatever goes into a black hole never re-emerges.

We have concentrated here on describing how nanowires can be shaped to perform shift register action. We have found that other logic functions are also possible. In particular, an AND gate has been demonstrated, as well as a fan-out structure and a cross-over structure. These are described more fully in reference [13].

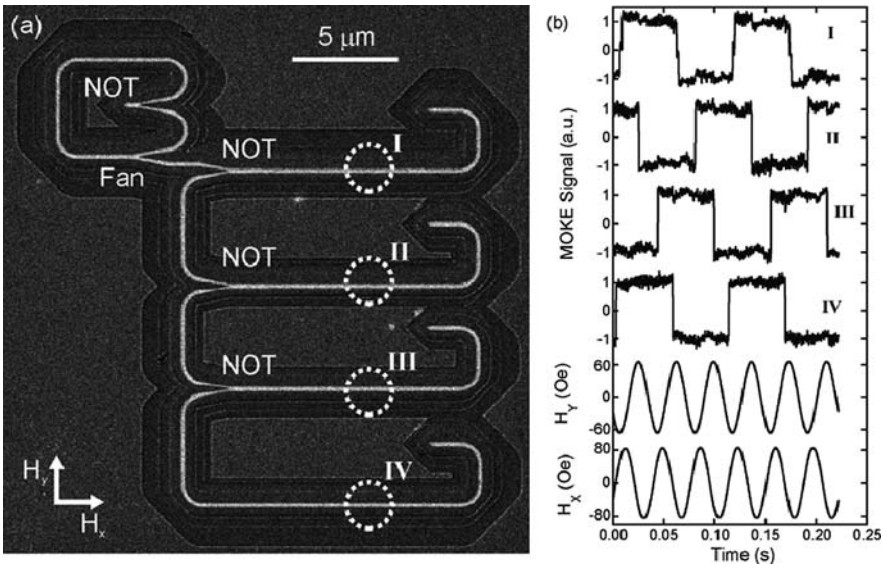

Fig. 8.6 A four-stage serial-in-parallel-out shift register nanocircuit which uses the central stub of the NOT gate to replicate the input signal

8.4 Data Input–Output

The recently developed technology of magnetic random access memory (MRAM) [14] has already solved most of the engineering issues involved in interfacing between a soft ferromagnetic layer and an underlying CMOS system. Specifically, in MRAM, data writing is achieved by passing an electrical current through a conductor placed close to the magnetic element, allowing the magnetic field generated around the current to nucleate a reverse domain in the magnetic nanostructure. Data reading is achieved by the use of a magnetic tunnel junction (MTJ) [15] in which the electrical resistance of two magnetic layers separated by a thin film of insulator is found to depend strongly on the relative magnetization directions. By fixing the magnetization direction of one layer, it becomes a reference against which the magnetization direction of the other layer may be measured. Signal levels large enough to interface directly to CMOS transistors are achieved by this method. We intend to piggyback off these developments for interfacing signals between the magnetic system and the conventional electronics. Domain wall logic can be considered as an extension to MRAM. In MRAM, the data storing magnetic layer is very simple and is only used to store a single bit of information. The concepts developed in magnetic logic can be used to extend the functionality of that storage layer, allowing data to be processed as well as stored.

We have developed an alternative data input method which may be important if 3D structures are implemented in domain wall logic. One of the major limitations to creating ultrahigh density 3D microelectronic circuits is the cost of making

connections to the multiple layers. A useful strategy for realizing the ultrahigh data density of 3D structures without increasing the cost is to attempt to find a way in which the input and output to the 3D structure is maintained in two dimensions. Figure 8.7 shows a device we have developed which allows this to be done with domain wall logic. See reference [13] for further experimental details. The figure shows a chain of eight NOT gates, where one gate has had its central stub enlarged. This reduces the shape anisotropy in that stub and hence reduces its nucleation field a little. Consequently, if the *globally applied* rotating magnetic field is modulated in amplitude slightly, it is possible to cause nucleation in the NOT gate with the elongated pad, thus forcing its data state to the direction of the global field. Importantly, the strength of modulation needed to achieve this is not so strong as to lie outside of the operating margin of all of the other gates in the chain, and so they continue to work normally. Thus, by modulating the global field, we can write data directly into the serial shift register and then shift that same data throughout the rest of the shift register. In this case, the globally applied rotating magnetic field is not only serving as a power supply and clock, as it does in all other domain wall circuits, but also acting as a serial input data channel. Figure 8.7 shows a working demonstration of this experiment, where we have written the data sequence 11010 into the shift register by modulating the rotating field. This writing sequence is applied only once. An hour later, we then begin cycling the rotating field without modulation and use the MOKE laser probe to read the serial data circulating around the shift register. We see the sequence 11010 repeatedly, as it goes around the circular shift register. We have thus succeeded in injecting data into the nanoscale storage ring, even though the source of field modulation was 1 cm away from the chip itself. As a

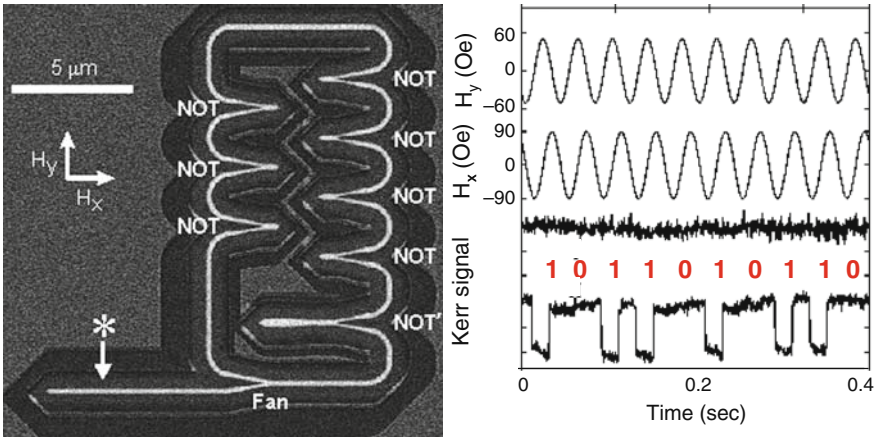

Fig. 8.7 A serial shift register formed from eight NOT gates, with the central stub of one NOT gate enlarged to form a data input element. The data sequence 11010 is written into the shift register by modulating the rotating magnetic field. The signal traces show the recovered data sequence circulating around the shift register, as well as a flat trace showing the result when the writing sequence is not performed

control experiment, we show also in Fig. 8.7 a straight trace, obtained during reading when the 11010 sequence had not been previously written. The reasons that we do not see a 10*T* periodic signal as might be expected based on earlier results is that there is an even number of NOT gates in this loop, which prevents it from acting as a ring oscillator.

This result is significant because it demonstrates the ability to write data into nanoscale storage rings from a distance. This immediately opens up the possibility of a 3D data storage cube, in which all magnetic field generation and sensing is performed on the bottom CMOS layer, but where data can be remotely targeted to specific parts of the 3D volume simply according to where one places the NOT gate with the enlarged stub [16]. Such a device would have the storage density of a 3D device but the fabricational cost structure of a 2D device. This idea will be explored further later in this chapter.

8.5 Using the Chirality of the Transverse Domain Wall

So far in this chapter, it has been the magnetization direction of the *domains* separated by the domain walls that have been used to represent data. There is, however, a further degree of freedom accessible in these domain wall conduit structures, namely the chirality of the domain wall itself. Figure 8.8 shows a schematic of the transverse domain walls that are expected to exist in such nanowires [17]. The magnetization in the centre of the domain wall points is seen to point at 90° to the nanowire axis. However, there are two possible states: it may turn clockwise or anticlockwise, leading to two different chiralities of transverse domain wall. In a simple nanowire, these two states are energetically degenerate and could possibly be used to code data. The V-shape that is seen in the centre of the domain wall is coupled to the transverse magnetization direction and is not an independent degree of freedom.

Using the chirality of the transverse domain wall to code data is interesting because it separates the data value from the direction of the force that an external

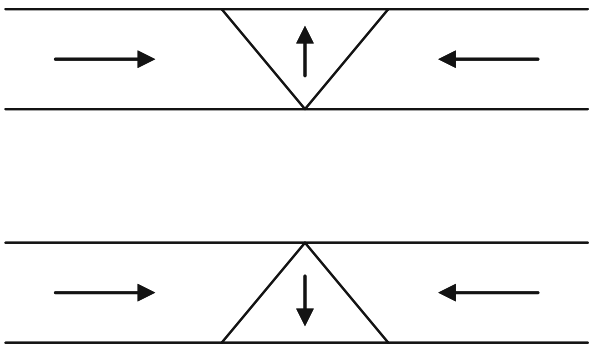

Fig. 8.8 The two chiralities of transverse domain walls in magnetic nanowires

field applies to a domain wall. We have already discussed how head-to-head and tail-to-tail domain walls respond oppositely to an applied magnetic field, leading to the need for shift register structures if data are to be propagated unidirectionally. In contrast, there is no dependence of the way that the domain wall responds to an external field on the domain wall's chirality. Shift register structures will still be needed using chirality coding since both head-to-head and tail-to-tail domain walls will still be present, but they may become simpler since the charge on the wall (i.e. head-to-head or tail-to-tail) can become predictable and independent of the data value being carried.

In order to use the domain wall chirality, two key questions need to be addressed. The first is how stable is the chirality. It is known that in general when a domain wall moves quickly, the direction of magnetization in the centre precesses [18]. In the ribbon geometry of our nanowires, this precession takes the form of occasional nucleation of an anti-vortex at one end of the wall, followed by the propagation of the anti-vortex along the length of the wall, resulting in a 180° reversal of the transverse part of the magnetization [19]. We have performed a number of experiments to determine the distance that a domain can move on average before such reversal occurs. Figure 8.9 shows an example of the one of the experimental structures. The domain wall is nucleated (with known chirality, depending on whether the 'P' structure or the 'AP' structure is fabricated) at the corner of the wire in the same fashion as in Fig. 8.1. The wall then runs a certain distance before it meets a cross arm. The cross arm acts as a chirality filter. We find that if the transverse component of

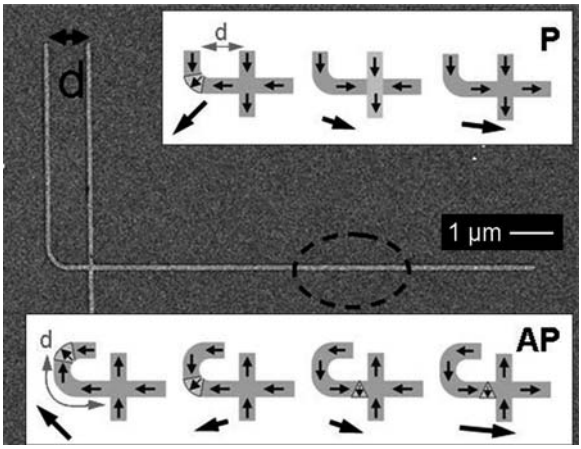

Fig. 8.9 SEM image of an L-shaped nanostructure with a cross at a distance *d* from the corner (the lower part of the transverse arm extends 5 μm below the *cross*); the position of the MOKE measurement is indicated by the *dashed ellipse*. Insets: (P) *left to right*: first half of field sequence (*black arrows*) for L-shaped nanostructure, and schematics indicating magnetization configurations in the absence of chirality reversal. (AP) First half of field sequence for C-shaped structure. The labels P and AP indicate that the DW is created with core magnetization initially parallel or anti-parallel to the magnetization in the transverse arm

the domain wall magnetization lies parallel to the magnetization in the cross arm, then the domain wall is able to pass across the arm relatively easily. If, conversely, the transverse component of the domain wall magnetization is anti-parallel to the magnetization in the cross arm, the domain wall is heavily repelled and is unable to pass. The cross arm thus acts like an analyzer for domain wall chirality. By putting the MOKE probe on the right-hand side of the cross, we can probe the chirality of the domain wall at the instant it arrived at the cross: one chirality leads to switching of the nanowire to the right of the cross, the other chirality does not. This is a very powerful experimental technique as it effectively amplifies the number of spins that need to be detected: the magnetization in the entire nanowire to the right of the cross arm is much larger than the magnetization in the core of the domain wall itself.

Figure 8.10 shows a summary of the results. For structures that have a distance of 1 μm or less between the starting point and the analyzer, the domain wall is found to be transmitted through the cross 100% of the time, i.e. the chirality of the domain wall was preserved. For distances greater than this, there is a finite probability of the chirality reversing. We can thus define a coherence length for the chirality, i.e. a distance over which the chirality is predictable. Figure 8.10c shows measurements of this coherence length as a function of applied field strength. An interesting feature of these experiments is that we find that the coherence length is reset every time the domain wall passes through a cross. Figure 8.11 shows a nanowire that has been periodically patterned by crosses to form a comb structure. We find that the domain wall is able to propagate all the way to the end of the wire (and indeed backwards

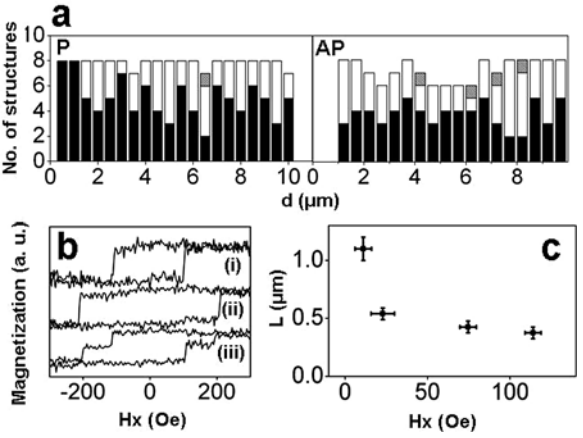

Fig. 8.10 (**a**) Number of structures showing each type of switching pattern as a function of distance, *d*, for both P and AP cases as shown in Fig. 8.1. *Black*: switching corresponding to the DW reaching the cross with the chirality set by the initial field pulse; *gray*: switching corresponding to DW reaching the cross with the opposite chirality; white: double transition. Chirality reversal is not observed for $d \leq 1\,\mu m$. (**b**) Typical MOKE loops, vertically offset for clarity. (i, ii) MOKE loops showing single transitions at H_T and H_N. (iii) MOKE loop showing double transition. (**c**) Measured coherence length, L, as a function of field

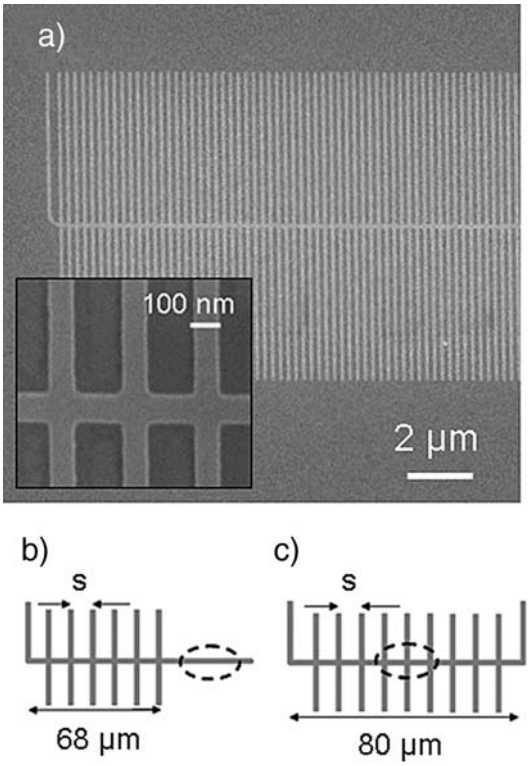

Fig. 8.11 Comb structures. (**a**) SEM image of left-hand part of comb structure with cross spacing $s = 250$ nm. (**b**) Schematic of L-shaped comb. (**c**) Schematic of U-shaped comb. The position of the MOKE measurement is indicated by the dashed ellipse

and forwards many times) without any chirality flipping, because each cross acts as an error corrector, suppressing any chirality reversal that was about to occur. Thus, although chirality is not perfectly stable, careful design of the nanowire structures does allow it to be used as a predictable vector for data.

The second key question has already been touched on in the previous paragraphs and concerns how easy it is to manipulate and control the chirality of a domain wall. The cross structures used in the previous experiment give one example of chiral control and filtering. Figures 8.12 and 8.13 give a related example in which a high-efficiency domain wall switch is presented. We find that a T-stub interacts even more efficiently with the chirality of the domain wall, largely because both the direction of the transverse magnetization within the wall and also the shape of the V-structure contribute to the discrimination between chiral states. We find that when the chirality of the domain wall is such that the transverse magnetization is parallel to the T-stub magnetization, the domain wall is able to pass through the gate with virtually no increase in propagation field; when anti-parallel, the field to transmit through the gate becomes greater than or equal to the nucleation field of the wire, i.e. there is perfect discrimination between the two chiral states. Such a highly discriminating structure could form the basis of a number of new spin-dependent devices that work with the domain wall chirality.

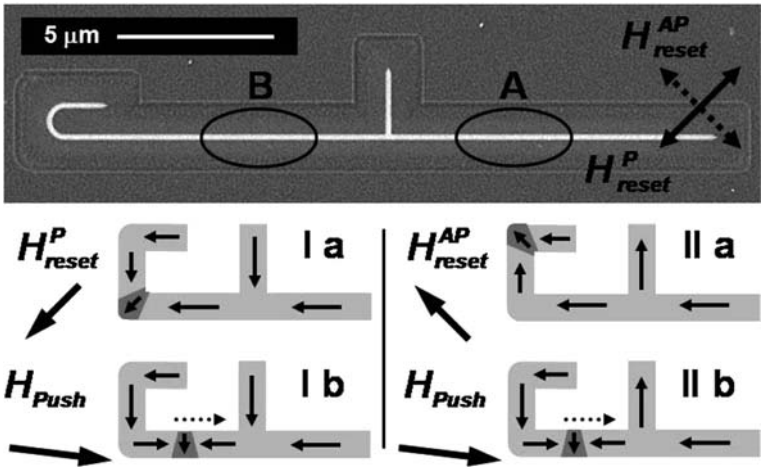

Fig. 8.12 Secondary electron image by FIB irradiation of a 200 nm wide Permalloy structure with a DW gate at its *middle*. Ellipses A and B show the two positions of the laser beam during MOKE measurements; the *double arrows* show the directions H_P reset and $H^{AP}{}_{reset}$. *Bottom*: schematics illustrating the field sequences used to measure the switching properties of the structures. Ia, b, illustrate the creation and displacement of a head-to-head domain wall in the parallel configuration; IIa, b, show the anti-parallel configuration. The large *arrows* indicate the direction of the external magnetic field, the narrow *arrows* show the direction of the magnetization in the nanostructure, and the *dotted arrows* show the direction of displacement of DWs

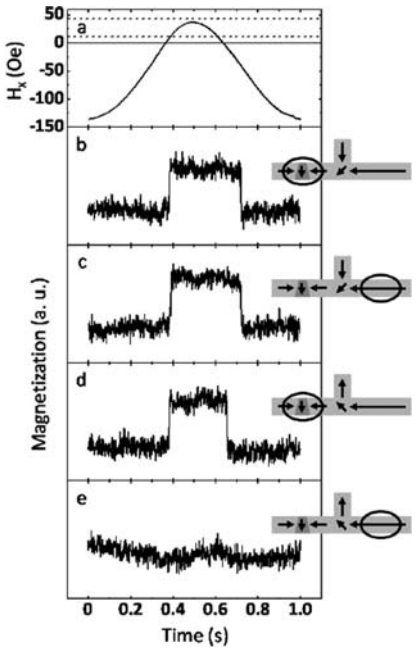

Fig. 8.13 Horizontal field Hx (**a**) and MOKE traces (**b, c**) measured after the gate when the magnetization in the core of the incoming DW is (**b**) parallel to the magnetization in the gate and (**c**) anti-parallel. The DW is created during the negative part of Hx and pushed towards the trap during the positive part. The *upper dotted line* indicates the transmission field for parallel configuration, the *lower dotted line* for anti-parallel configuration

8.6 Potential Applications of Domain Wall Logic

Domain wall logic is not a contender for a wholesale replacement of CMOS microelectronics. CMOS is a highly mature technology with many advantages, and still has many years of scaling available to it. However, a strong trend in microelectronics which is expected to apply to the relationship between CMOS and many other areas of nanotechnology in the future is to combine multiple technologies on a single platform: the System on Chip (SoC). Mature economies usually break into a large number of specialists each doing what he or she does best. The same principle applies to complex microelectronic devices. In this context, domain wall logic brings another item to the menu of available technologies. So what does domain wall logic do well?

- It gives high level of functionality to relatively simple structures. To implement shift register in CMOS would take several transistors; domain wall logic achieves it simply by bending a nanowire into a cusp.
- The power dissipation per logic gate is extremely low. Microelectronic engineers usually measure dissipation from a gate by the power-delay product, that is to say the product of how much power is dissipated multiplied by how long the gate takes to process a single function. The units of this quantity are energy, corresponding to the energy dissipated during the evaluation of the function performed by the gate. CMOS' power-delay product depends upon the size of the devices. In order to compare like with like, we therefore take the 200 nm minimum feature size CMOS value of 10^{-2} pJ [20]. On very general magnetic grounds, we can say that an upper bound for the power-delay product for domain wall logic is $2M_sVH$, where M_s is the saturation magnetization of the magnetic material, V is the volume of magnetic material in a gate and H is the amplitude of the applied field. Applying the parameters for a typical 200 nm domain wall logic gate gives 10^{-5} pJ, i.e. 1000 times lower than the equivalent CMOS device. Because of the inefficiencies inherent in the generation of high-speed magnetic fields (see above), this does not necessarily mean that domain wall logic chips will not consume much power. What it does mean, however, is that the waste heat will be generated from the global field generator and not from the logic devices themselves. This is of particular relevance if one comes to stack the devices into 3D neural-like circuits. The two key technical difficulties to doing this in CMOS are (i) distributing the power and clock to everywhere inside the volume of network; (ii) extracting the waste heat from the centre of the network so that the device does not melt. We believe that domain wall logic is an excellent choice of primitive for 3D architectures.
- Non-volatility comes as standard. In a world of mobile computing and portable (or even wearable) devices, the concept of 'instant-on' is becoming increasingly important. Users accept that devices cannot be expected to operate when there is no power. However, as soon as power becomes available, users want the device to be ready, and not have to undergo a long boot process, or to have forgotten what it was doing when the power last failed. Since there are currently very few non-volatile memory technologies available which can be embedded directly

into CMOS, a data transfer process is usually required between a high-speed, volatile memory register in the heart of the CMOS logic and an off-chip low speed, non-volatile store where the state variables of the system are stored. With domain wall logic, all of this becomes redundant. Providing that the rotating field is properly controlled so that it stops gracefully as power fails and does not apply intermediate levels of field leading to data corruption, the domain wall logic circuit should simply stop and retain all of its state variables. As soon as the power returns, the logic continues from where it left off.

- Domain wall logic can make use of redundant space on top of CMOS. Because no complex heterostructures are required, the logic elements can sit in a single layer fabricated as a Back End Of Line process after the CMOS has been laid down. This can improve the efficiency of the underlying CMOS by farming out some space-consuming task to the domain wall logic on top. Since this space was never accessible to CMOS itself anyway, it all counts as a gain.
- Being metals, the basic computational elements of domain wall logic are automatically radiation hard and so are suitable for use in space or in military applications.
- We have already demonstrated that domain wall logic is very good at forming high-density shift registers. These could be used as non-volatile serial memory. Serial memory is used for storing entire files, and so does not require high-speed random access. The hard disk drive and NAND Flash devices (e.g. as used to store the photographs in a digital camera) are examples of non-volatile serial memory. Both of these devices are currently 2D in form. Shift registers made from domain wall logic elements have the potential to be stacked into three dimensions without incurring extra wiring complexity, since data and power can be transmitted remotely through magnetic fields, as demonstrated earlier in this chapter. In a hard disk drive, the data are stored as rows of magnetic domains, and this would remain the same in a domain wall logic serial memory. What would differ is that in a hard disk, the domains are mechanically rotated on their disk underneath a static sensor, while in domain wall logic the domains themselves would move under the action of an externally applied magnetic field along static domain wall conduits, potentially stacked into an ultrahigh density 3D array.

The weaknesses of domain wall logic are (i) limited operational speed and (ii) unconventional synchronous interconnect. Whether the latter should be regarded as an advantage or a disadvantage is open to debate, since it is the same property which makes domain wall logic so suitable for high-density serial memory. Nevertheless, interfacing with conventional design tools remains a challenge.

8.7 Conclusion

While bulk magnetic alloys usually exhibit very simple linear properties, structuring on the nanoscale introduces more complex, non-linear behaviour which can be used for a new generation of spintronic devices. In particular, the coercivity of the

magnetic material, which is usually an intrinsic property in the bulk, becomes very dependent on whether the magnetization reversal mechanism is limited by domain nucleation or by domain wall propagation. We have demonstrated modifications to the coercivity of as much as a factor of 65 simply by whether a domain wall is artificially injected or not. The huge ratio between the domain wall propagation field and domain nucleation field that exists in magnetic nanowires has allowed us to introduce the concept of the domain wall conduit, in which the nanowire can be considered to be a highly efficient conductor for domain walls. If information is encoded by the domains, then domain wall conduits allow that information to be moved around an arbitrary network, and the possibility of building computational devices emerges. Furthermore, we have shown that by precisely modifying the shape of the nanowire, we can exert control over the information and hence implement Booloean gates. An alternative approach to information coding has also been demonstrated, in which the chirality of the domain wall itself rather than its magnetostatic charge is used to code data. In this case, propagation of data along nanowires is possible providing the coherence length of the chirality is respected. Very high-efficiency gates, switches and filters can be implemented by intersecting nanowires in the shapes of crosses or T-stubs.

We have discussed the strengths and weaknesses of domain wall logic when compared against other mainstream digital technologies and concluded that like most nanoscale devices, domain wall logic is not a one-stop replacement for all areas of digital logic, but rather should be used selectively to perform the functions that it does best. We have highlighted in particular the benefits of forming 3D shift registers from domain wall logic elements for the purpose of ultrahigh density data storage.

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