Chapter 9
Heterogeneous Integration: Building the Foundation for Innovative Products

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Abstract This chapter gives an introduction to the future of electronic system integration as a combination of "More Moore" and "More than Moore" components, combined in one package ("system-in-package" or SiP). More Moore will very likely continue to be at the forefront of electronics development for the next decade. It is difficult, however, to integrate non-digital functions, such as sensors and power electronics, for example, monolithically with these technologies. For this reason the future belongs to integration technologies that combine several components into a highly integrated assembly in one package – "wafer-level packaging" processes, the use of ultrathin components, and multifunctional interposers will all play a key role in this context. Often two dimensions do no longer suffice. Because of signal propagation delays, wiring density, or confined available space many future applications require considerably more compact components. 3D integration can help overcome this bottleneck. Examples of 3D integration start with silicon 3D integration with through-silicon vias and go up to stacking of packages or modules at all technological levels. Functional packaging goes one step further. It takes the application system and its requirements as a starting point and then adapts the microelectronic functions.

Keywords System-in-package • Wafer-level integration • Board-level integration • Integrated passives • Functional layer technology • Thin chip integration • Module integration technologies • Embedding of passive components • Chip-in-polymer • Chip embedding into flexible substrates • Functional packaging • Integration of biological functionalities • 3D integration • Package stacking • Through-silicon vias

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G.Q. Zhang and A.J. van Roosmalen (eds.), *More than Moore: Creating High Value Micro/Nanoelectronics Systems*,
DOI 10.1007/978-0-387-75593-9_9,

9.1 Introduction

Heterogeneous integration, at the center of any micro/nanosystem creation, which is the bridge between nanotechnology and microtechnology with macroscale applications, is the final manufacturing process transforming multifunctional devices into products for the end users. It provides electrical and physical connections (e.g., bioconnection for bio-SiP) for multisignal transmission, power input, and voltage control. It also provides for thermal dissipation, construction carrier, and the physical protection required for reliability. To develop commercially feasible and reliable micro/nanosystems, Heterogeneous Integration plays an essential role as the key enabler governing the multifunctional performance, interface to the application environment, size, weight, cost, and reliability of the final products. Heterogeneous integration has to ensure not only the integration of devices based on different technologies and materials but also the target of miniaturization. Therefore, most of the innovative micro/nano devices, materials, concepts, and prototypes cannot lead to economic success without cost-effective and reliable heterogeneous integration technologies. This chapter describes the technologies and processes associated with heterogeneous integration. The associated strategic research issues and their solutions are also discussed.

Heterogeneous integration bridges the gap between nanoelectronics and its derived applications. Two main forces drive progress in this area – emerging device technologies and new application requirements. New technologies and architectures are needed to integrate the progress made in nanoelectronics, microsystem technologies, and bioelectronic and photonic component technologies into electronic systems or MEMS.

In terms of applications, a strong link exists between the development of components and system-oriented integration technologies such as system-in-package. The operation environment, which has traditionally been defined by the needs of electronics, is nowadays increasingly determined by the application, such as by "under-the-hood" environments in the automotive industry or by the human body for implantable medical devices. Because of the increasingly central role of electronics in ensuring system reliability and functionality, the reliability of electronics will be a primary issue in the future.

In terms of integration, both *More Moore* as well as *More than Moore* solutions are aiming at single component solutions. As far as technically and economically feasible solutions are considered "system on chip" (SoC) or *More than Moore* solutions will be chosen. But increasingly applications demand product-specific integration technologies or the flexible integration of highly complex systems with digital and nonelectronic functions. Thus, the future of electronic system integration will see a combination of *More Moore* and *More than Moore* components, combined in one package (*system-in-package* or SiP) (Fig. 9.1). Such SiP solutions have two main advantages - first, a level of miniaturization comparable to *system on chip* (More Moore) solutions combined with the enhanced functionality of *More than Moore* solutions, and second, the use of optimized process technology to fabricate each part of the system.

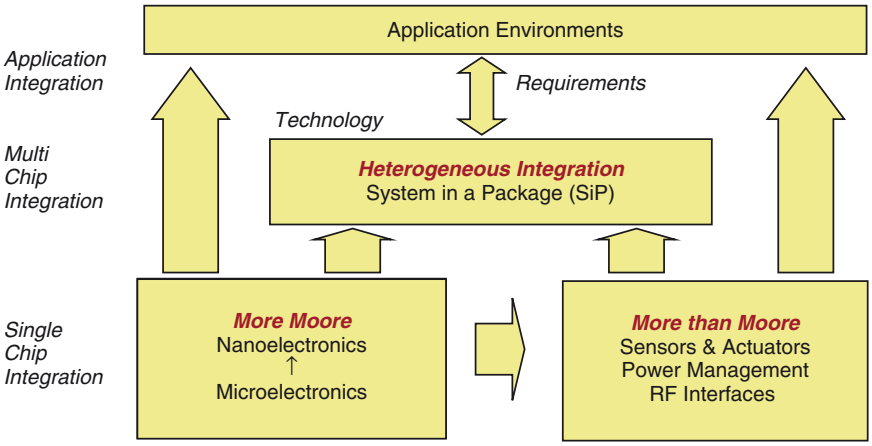


Fig. 9.1 Different levels of system integration

Using heterogeneous integration such as *system on chip* or *More than Moore* for subsystems makes highly flexible solutions possible. This equals lower costs and risk assessment compared primarily with SoC as well as *More than Moore* solutions to some extent. Further advantages include a shorter time to market cycle and a higher degree of flexibility.

In terms of technology heterogeneous integration combines different components and technologies into one package and also provides an interface to the application environment. Although *More Moore* and *More than Moore* technologies are based on CMOS-compatible processes and are therefore limited to a certain set of materials, heterogeneous integration technologies have to ensure that components based on very different technologies and materials can be integrated, such as power devices, photonic or RF components (using InP or GaAs), energy harvesting or storage components (thermoelectrics, fuel cells, thin-film batteries, supercaps), or smart displays. Reliability standards will see failure rates expressed as failures per billion parts, rather than per million parts, as is currently the case. Achieving this is made even more difficult by the fact that it will become necessary to integrate nondigital functions, such as MEMS, optical, RF, or power devices. To increase integration density in terms of the number of integrated components or in terms of geometry requires three-dimensional design methods such as stacking, as well as, due to the market demand, design for operation in less than ideal conditions. These include automotive applications at higher temperatures and harsh environments.

At present, system integration is still dominated by single-chip packaging and the few stacked-die SiP solutions employed are primarily based on wire bonding (Fig. 9.2).

High-density interconnect (HDI) multilayer boards are the most advanced substrate boards currently available. Unlike in the integrated circuit industry, where electrical, thermal, and mechanical characterization is undertaken on the complete design, in SiP solutions, the chips, package, and board continue to be designed separately. However, this will not be sufficient to meet the requirements of advanced SiP

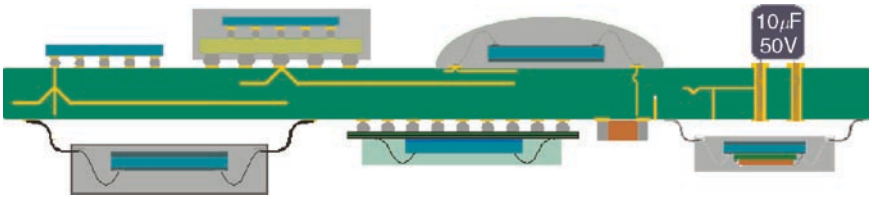


Fig. 9.2 Present status of system integration

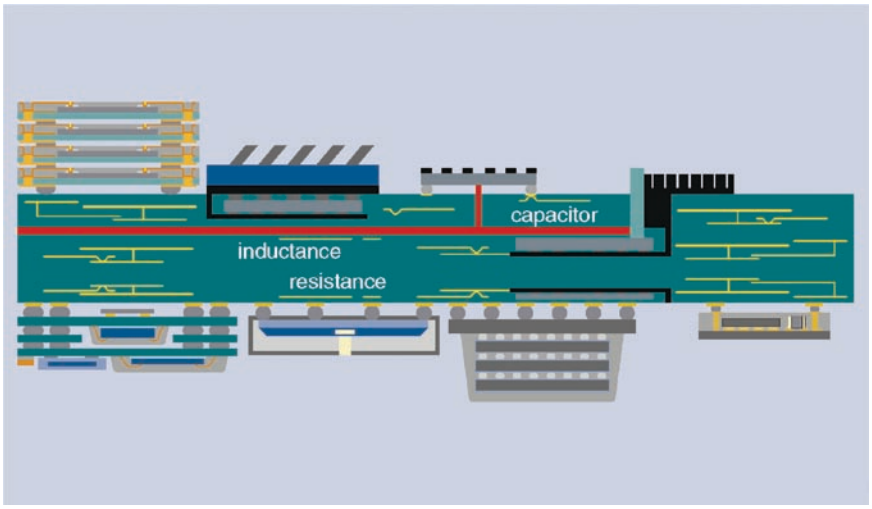


Fig. 9.3 Future system integration

solutions in the future, as the level of miniaturization and reliability requirements will be extremely high. Thermal and mechanical stress management has to be optimized beginning with the point at which heat is generated to the outside of the package. It will be further complicated by integration of additional functions into the package, such as sensors, actuators, RF interfaces, or power supply components, which may be highly sensitive to heat, stress, etc. Additionally, the application environment in which the SiP will ultimately be used will also need to be taken into account.

To meet these challenges, new architectures have to be developed. It will also be necessary to develop advanced assembly and handling technologies for thin wafers and chips to reach the required level of miniaturization. The integration of nano-ICs, sensor chips, actuator components, passives, and displays into 3D architectures will see the development of new design methodologies, as well as reliable ultrathin metallic interconnect technologies. An example of such system integration is proposed in Fig. 9.3.

The board will be transformed from a simple carrier for packages to a system carrier with optical and electrical wiring. Geometric limitations will be overcome by employing embedded passive components to include even smaller and increasing

numbers of such components. Integrated active components will ensure higher reliability, better RF ability, and increased integration density.

9.2 Physical Package Characterization, Lifetime Modeling, and Design for Reliability for Heterogeneous System Integration

In future electronic systems, the boundaries between semiconductor devices, packaging, and system technologies will blur. It will no longer be possible to design packages independently of chip and system design. All aspects of devices, packages, and systems will need to be considered simultaneously as part of an overall process, and optimizing the complete system will require trade-offs between chip, package, and system design and the analysis of many complex design parameters. Rethinking system layout to effectively improve performance, while at the same time reducing cost across a diversified technology base, is adding to design process complexity, both in terms of design tools and the need for more accurate information about the system itself, as well as system and material parameters. Reliability will become paramount. For example, driver assistance and safety systems will require a level of reliability similar to that of avionic electronics but at much lower cost. To ensure such product quality over a product's life span, "design for reliability" will become the catchphrase, along with the drive to better understand the factors determining reliability. The reliability of a SiP can be described as (1) the reliability of components, (2) the reliability of interfaces among components, as well as among components and package, and (3) the reliability of the system packaging. Especially the point (2) is not yet understood well enough on a microscale. Improvements in reliability will require greater understanding of interface behavior, including complex thermomechanical and other failure modes, as well as integrating this knowledge into the design process.

Localization, preparation, and analytics of failures, as well as testing of complex SiPs, will become a huge challenge. Ageing models for materials and material interfaces (e.g., adhesion and interconnect degradation) will also be required to assess life-time performance. Reliability models for life-time estimation will need to be based on nanomaterial and interface simulation, closing the gap between macroscale continuum mechanics and molecular modeling. In addition to these design-related models, new field testing methodologies will be needed to close the gap between field testing and design.

9.3 Wafer-Level Integration

Following Moore's law, the complexity of future components will increase dramatically. Using Rentsch's rule, chips with up to 6,000 inputs/outputs are expected, and on-chip and chip-to-board frequencies are likely to increase. The package has to

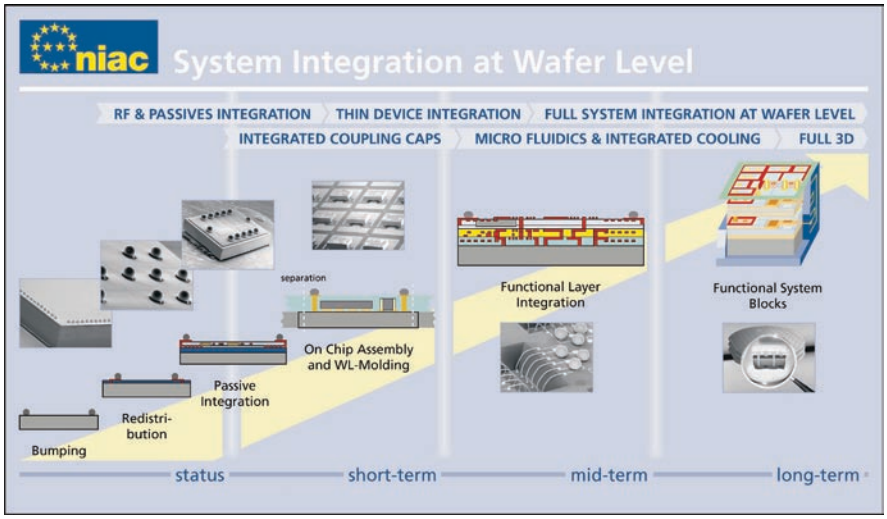


Fig. 9.4 Technology roadmap: wafer-level system packaging [8]

provide additional interconnects that exceed the current capacity of the "back-end of line" (BEOL) network. Even though the energy consumption per transistor will decrease, the total energy demand per chip and the energy density will increase due to the larger number of transistors and their higher frequency of operation. In addition, future systems will require additional radiofrequency and nonelectronic functions such as sensors, actuators, power supply components, passives, and displays (MEMS integration), which often require the use of alternative materials and new processes. However, integration of these alternative materials and processes into manufacturing often reduces yield and/or increases cost. Ultra high-density wafer-level integration technologies must therefore be able to successfully combine different technologies while also meeting yield and cost requirements under the constraint of highest reliability. A number of wafer-level integration technologies are being researched to achieve these goals. An overview of the technology roadmap is shown in Fig. 9.4.

The present state of technology comprises bumping, redistribution layers, and integration of passives. Further integration steps include layer deposition techniques to create embedded components, embedding ultrathin devices into cavities or polymer layers, creating high surface-area honeycomb structures for integrated capacitors, and nanowires to integrate III/V materials (InP, GaAs) and SiGe components. The following text discusses several of these approaches in detail.

9.3.1 Integrated Passives

Compared with integrated circuits, passive SMD components have only minimally decreased in size. Since the ratio of passives to ICs is in the range of 12:1 to 25:1 in cellular phones, passives are a major hurdle for further miniaturization of

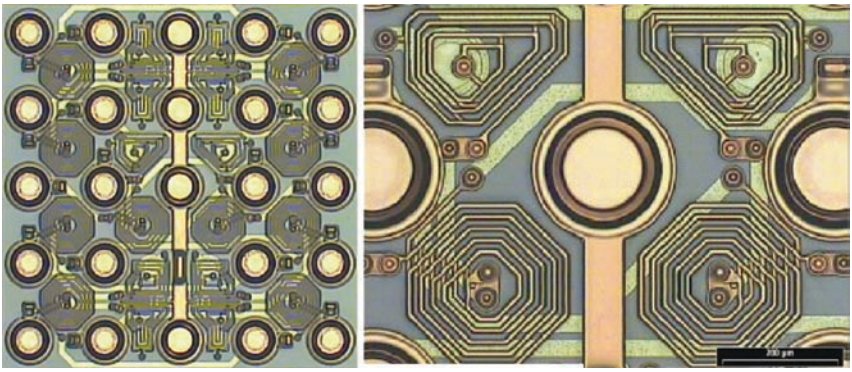


Fig. 9.5 Integration of coils into a redistribution (WLP using Cu/BCB)

electronic products. One loophole is the integration of resistors, capacitors, and inductors onto the wafer, which can be performed at BEOL by using the existing wafer-level packaging infrastructure. An example of the integration of coils into a redistribution layer is shown in Fig. 9.5.

The integration process for integrated passive devices (IPD) is based on Cu/BCB multilayer wiring using thin-film technology [13]. It uses semiadditive structuring of copper by electroplating and lithographic structuring of spin-coated photosensitive BCB as base processes for creating alternating routing and isolation layers. To date, buildups with up to four copper layers and five BCB layers have been realized. The high conductivity of the copper combined with the low dielectric constant and the low loss tangent of the BCB makes it possible to realize high-performance wiring systems, which feature low propagation delay, low cross talk, and low transmission losses. Since the technology is very flexible as to the number of layers, as well as layer thickness, the necessary layer buildup must be derived from the selected types of passive components. It should be noted that integrating all three types of passives will prove to be the most complex challenge.

Integrating coils requires at least two copper layers, separated by a BCB layer. In the case of a simple single-layer coil, one copper layer is required for the windings, while the other is employed for the underpasses, which connect the inner with the outer contacts of the coil. In the case of double-layer coils, windings are realized in both copper layers. To enable a proper processing of the second copper layer the BCB has to be thick enough to planarize the structures in the bottom copper layer as well as to reduce the capacitive coupling between the two layers sufficiently.

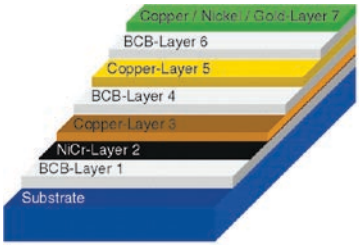
The same layer setup as used to integrate coils can be used to create metal–insulator–metal (MIM) capacitors [14]. The two wiring layers are used for the realization of top and bottom electrodes and the interdielectric layer is used as dielectric material. To ensure a high capacitance density, the BCB between the copper layers has to be as thin as possible.

Thus, two copper layers, which are separated by one BCB layer, are the minimum number of layers for an integration of coils and capacitors into one assembly. The corresponding layers are indicated with the numbers 3, 4, and 5 in the schematic drawing (Fig. 9.6).

Since copper is highly conductive, a separate material must be employed for the resistor structures. Processing compatibility issues render NiCr or TaN most suitable. Both materials can be deposited in the required sheet resistance and are compatible to the deposition and structuring processes of the other materials. Because NiCr resistors need copper structures for their connection, they are fabricated before (and beneath) the copper layers (Fig. 9.6). In Figure 9.6, the NiCr layer can be identified as Layer 2. Furthermore, nonwavy surfaces are preferable for production to minimize deviation in resistor lengths from nominal values, which is another reason for placing the copper layers as close as possible to the substrate.

Including the NiCr, at least four other layers are necessary for the integration of coils, capacitors, and resistors into one thin-film buildup. Additionally, to protect the passive structures and to ensure that the thin-film buildup can be correctly connected to the next system level, additional layers are required. At least one overall BCB passivation layer, as well as one final metallization layer (copper, nickel, or gold), is necessary, increasing the total number of layers to 6.

These process sequences make fabricating coils with arbitrary or regular forms such as squares, rectangles, octagons, or circles possible. The coils can be configured as single-layer or double-layer coils. A single-layer coil, with a height of 10 μm and a width of 10 μm, 4.5 square turns, and an inner window of 400 μm has an inductance of 17.8 nH. To adjust the inductance of such coils, both the number of turns and the length of the inner window can be altered. Changing the number of turns alters the inductance in large steps, whereas changing the inner window length makes minor adjustments possible. Inductance values between 0.5 and 27 nH can be achieved with single-layer coils with 1.5–5.5 turns and inner window length between 100 and 400 μm. Double-layer coils, which have an additional, identical spiral in the first metal layer, reach up to four times higher inductance values than the corresponding single-layer coils. Thus, values between 1 and 110 nH can be achieved with double-layer coils. The quality factors and resonance frequencies of such coils are strongly dependent on their type, form, and size as well as the



	L	C	R
Layer 1	(x)	(x)	(x)
Layer 2	-	-	x
Layer 3	x	x	x
Layer 4	x	x	-
Layer 5	x	x	-
Layer 6	x	x	x
Layer 7	x	x	x

Fig. 9.6 Overview of the layers necessary for the integration of coils, capacitors, and resistors into one assembly

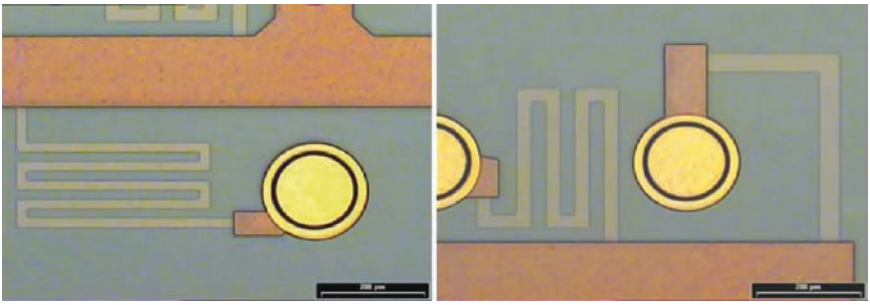


Fig. 9.7 Integration of resistors into a wafer-level package

substrate employed. In the case of ceramic or glass substrates, small coils with inductances below 10 nH produce resonance frequencies above 10 GHz and quality factors larger than 30. Using silicon as the substrate diminishes quality factors due to substrate losses.

Decoupling capacitors play a major role in reducing the switching noise for high-speed digital electronic systems. As the switching speed is well above 1 GHz and the power supply voltage simultaneously decreases, power supply noise is an issue. Large capacitance density and small leakage current are required. The capacitors should have very thin dielectric thickness and be mounted as close as possible to the chips to minimize parasitic inductance.

In case of the resistors, straight and meandered forms with resistance values between 100 and 150 kΩ have been produced by using line widths between 20 und 80 μm. The resistors are based on a sheet resistance of the NiCr layer of 100 Ω per square area, with sheet resistance defined as the resistance value of a square area of the NiCr layer. Figure 9.7 shows typical resistors fabricated with the technology presented here.

Similarly, new technologies will be needed for the wafer-scale integration of antennas (24–80 GHz), photonic components, batteries and energy scavengers, biointerfaces, microfluidics, and MEMS. Wafer-level encapsulation technologies using nanofilled materials (wafer molding), alternative technologies for 3D integration [e.g., through-silicon via (TSV) technology], and new isolation and shielding technologies for RF have to be investigated. To reliably manufacture wafers with such a high degree of wafer-level integration, advanced assembly and handling technologies for thin wafers and chips will need to be developed. Improved approaches for thermal management will also be required.

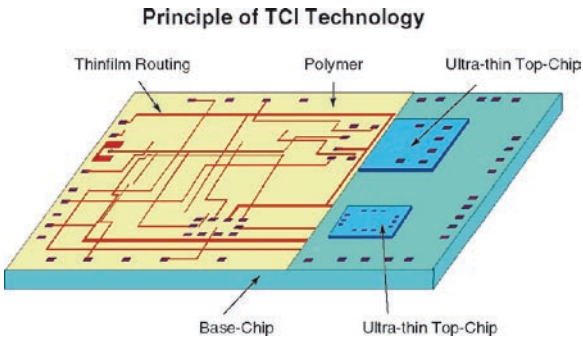
9.3.2 Extension of Redistribution Layers: Thin-Chip Integration

A base chip at wafer level is used as an active substrate for smaller and thinner dies. These thinned active components are mounted in flip-chip fashion on the base IC wafer using solder interconnects. To avoid the need for flip-chip bonding, the thin-chip

integration (TCI) concept can be used [15]. Key to this approach are extremely thin ICs (down to 20-µm thickness), which are incorporated into the redistribution layer (Fig. 9.8).

The process flow for TCI modules begins with the bottom wafer carrying large base chips. The completely processed device wafers for the top IC have to be mounted on a carrier substrate by a reversible adhesive bond and undergo a backside thinning process until the thinned wafers show a remaining thickness of approximately 20 µm. The thinned top wafer and its carrier substrate are diced by a conventional wafer saw, thus producing thin chips that can be handled by its carrier chip just like any other standard die. The chip separation is performed using silicon dry etching. The bottom wafer is coated with a thin epoxy film and the thinned top chips are placed and mounted into this adhesive layer. Next, the photosensitive low-*k* dielectric BCB polymer is deposited onto the surface to planarize the 20-µm topography of the mounted thin chips. A high degree of planarization (DOP), which is one of the advantages of photo BCB, is very important for this first polymer layer to overcome the height difference between the surface of the bottom chip and the thinned chips (Fig. 9.9).

Fig. 9.8 Principle of TCI



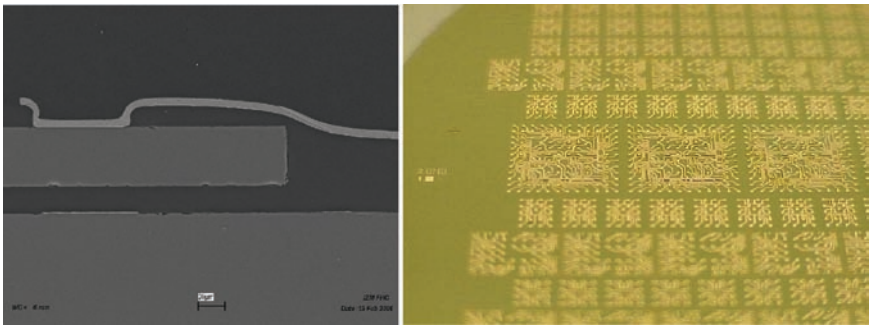


Fig. 9.9 A thinned chip (40-µm chip thickness) planarized with a thick BCB layer and additional Cu routing (*left*: cross section, *right*: video image)

Vias to the I/O pads of the thinned chips are opened using photolithography. Finally a thin-film metal layer connects the circuits of the top and base chips. A final CSP process, using a solderable metal layer and solder bump deposition, completes manufacturing of the TCI module.

9.3.3 *Functional Layer Technology*

Intermediate testing is one advantage of a process using flexible polymer layers with integrated passive and active components [9]. The schematic procedure is shown in Fig. 9.10.

The polymer layers are processed on reusable support wafers. The separation of the built-up layers is based on dissolving a release layer with a solvent. For the realization of the polymer layers a photosensitive polyimide precursor is used, which has excellent flexible properties as a freestanding film after release. The process sequence is similar to that described for the IPD. Examples are given in Fig. 9.11.

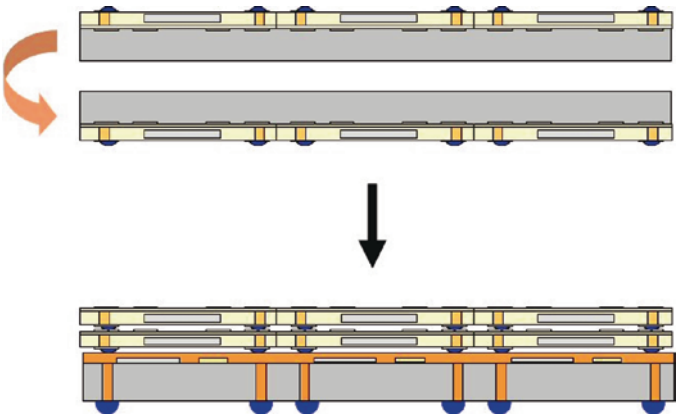


Fig. 9.10 Principle of the functional layer technology

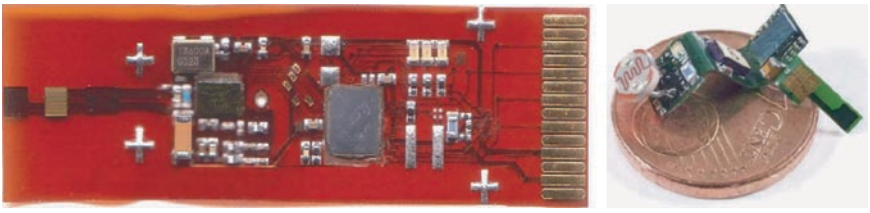


Fig. 9.11 Examples of functional layer technology (sensor nodes)

The sensor node's dimensions in the right figure are 9.8 mm (w) × 31.2 mm (l) × 0.035 mm (d).

9.4 Module Integration Technologies

Most of the earlier discussion of wafer-level integration also applies to substrate-level integration, which represents the next level of interconnect/integration. Nowadays electronic systems are realized on module level through an organic printed wiring board on which individual components are placed. Traditionally, the wiring board is used exclusively for the electrical and mechanical functions. However, diverse research and requirements in the development of modern electronic products have lead to the integration of further system functions onto the board.

Future board and substrate technologies have to ensure a cost-efficient integration of highly complex systems, with a high degree of miniaturization and sufficient flexibility to allow them to be adapted for different applications. Their functionality will be considerably extended by the integration of nonelectronic functions such as MEMS, antennas, or optical components. New production methods will ensure a high throughput at very low cost. To ensure high data transmission and processing rates, new cost-effective cooling technologies and 3D packaging concepts will ensure a stable operation mode. The following priorities can be identified for multifunctional board and substrate technologies (Fig. 9.12):

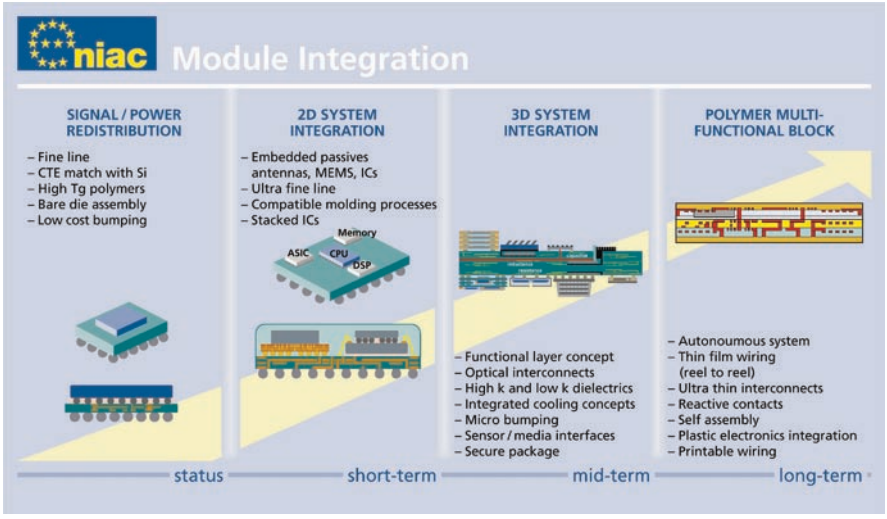


Fig. 9.12 Technology roadmap for module level system integration [8]

- Embedded device technologies (MEMS, passives, antennas, ICs)
- Low-cost substrates and interposers with finer liners and smaller vias
- Impedance-controlled wiring
- Flexible substrates (reel-to-reel manufacturing)
- Integrated optical interconnects

Technologies for embedded devices, such as MEMS, passive or active components, antennas, and power management will be the key to highly integrated modules. To make these possible, new materials for substrates, embedding, and encapsulation have to be developed, such as high-K and low-K dielectrics and high-T_g polymers, and the coefficient of thermal expansion (CTE) of these materials must be adjusted to the dies and substrates in question. Additionally, inside substrates and interposers with finer lines and smaller vias must be made available at lower cost. These advances will be followed by flexible substrates for reel-to-reel manufacturing and integrated optical interconnects. In the long term, printable wiring on organic substrates will increase productivity and lower environmental impact.

9.4.1 Embedding of Passive Components

The embedding of passive components into the printed wiring board is a promising approach for increasing the functional density of assembled electronic systems (Fig. 9.13). The development of materials and technologies for embedding resistors and capacitors was significantly advanced by the advanced embedded passives technology (AEPT) consortium in USA between 1999 and 2003 [1]. The application of such technologies in flexible printed circuits is, at present, the topic of the European project "Smart High Integration Flex Technologies" [2].

Printing technology for polymer thick-film (PTF) components is mainly used for fabricating resistors (although capacitors can also be produced with this technology). With appropriate paste compositions and component layout, resistors in the

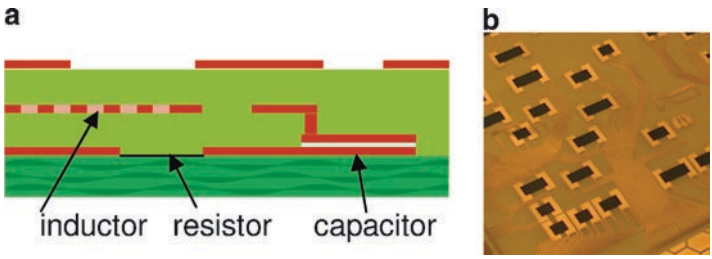


Fig. 9.13 (**a**) Embedded inductor, resistor, and capacitor in the build-up layers of a printed wiring board; (**b**) Printed resistors on a flexible printed wiring board before lamination into a build-up layer

range between 10 Ω and 10 MΩ can be realized. Since these printed resistors are in the range of ±20%, the resistors must be trimmed if smaller tolerances are required. The stability of PTF resistors under temperature and humidity load is an issue with many commercially available paste compositions.

Resistors and capacitors can be produced using sequential lamination and photostructuring. The variances of components here depend on the process capabilities of the manufacturer and are generally smaller than those of PTF components. However, the value range of embeddable resistors has tighter limits (10 Ω to 10 kΩ) and capacitance strongly depends on the used material (commercially available capacitors sheets are around 1 nF/cm^2).

Embedded capacitors have proven to be of interest for decoupling [4]. Since they can be designed and produced for placement close to the component (chip), inductances are reduced. Finally, cascades of SMD capacitors can generally be substituted by a single embedded capacitor.

9.4.2 Chip-in-Polymer

A new concept for the integration of active components is the so-called chip-in-polymer (CiP) technology [3, 5], which is based on the embedding of ultrathin chips into build-up layers of printed circuit boards (PCBs). The interconnect structure, which is neither a flip chip nor a wire bond, is shown in Fig. 9.14.

The basic idea of CiP is slotting thin semiconductor chips into standard PCB constructions. This technique can be used to fabricate 3D stacks of multiple dies, too. To achieve a contact pad surface on the wafer suitable for PCB metallization, the Al contact pads are covered by Cu bumps. To ensure that the bare dies can be embedded into build-up layers, wafers are thinned down to 50°µm. Subsequently, the chips are bonded using an adhesive. Precise thickness control of the bond line is essential for maintaining uniform thicknesses of the build-up dielectric on top of the chip. Here, new thin-chip handling and assembly solutions using die attach film or adhesive paste printing have been explored. RCC (resin-coated copper) layers with thin Cu are used for the lamination. Process parameters had to be fine-tuned to prevent damage to the chips during lamination. The chip contacts are produced with laser-drilled microvias followed by PCB-compatible Cu plating. All process steps in this technology have been optimized for large-scale manufacturing, using panel sizes of 18″ × 24″ in combination with high-accuracy positioning methods

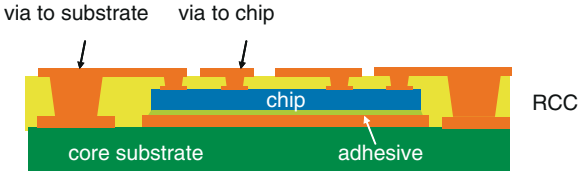


Fig. 9.14 Interconnect principle of an embedded chip in a PCB build-up layer

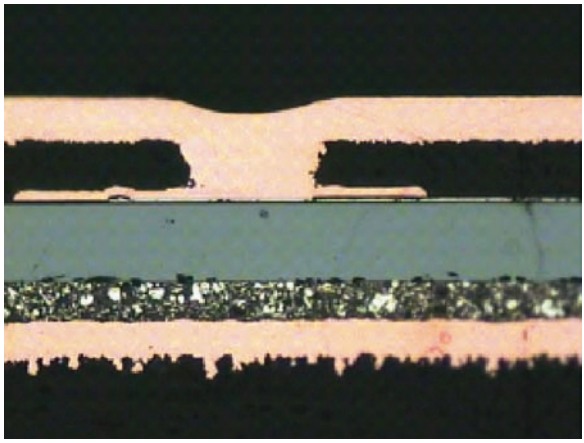


Fig. 9.15 Cu interconnect to embedded chip

using local fiducials for die placement, laser drilling, and laser direct imaging. Figure 9.15 shows a cross section of a Cu interconnect to an embedded chip.

Reliability evaluations of embedded chips have shown excellent reliability. For the evaluation, chips of 2.5 × 2.5 mm^2 size were embedded in 10 × 10 cm^2 test vehicles with a 0.5-mm FR4 core. All chips passed the following tests without any defect:

- Temperature storage at 125°C for 1,000 h
- Thermal shock condition; air-to-air −55±126°C; 2,000 cycles
- Humidity storage at 85°C/85% rel. humidity for 2,000 h
- JEDEC moisture sensitivity, level 3

9.4.3 Chip Embedding into Flexible Substrates

By embedding chips into flexible wiring boards, the functional density of electronic systems can be dramatically increased. The benefits of flex substrates, that is, light weight and high wiring density, will be combined with the complexity of the active chip. However, to maintain the basic flex substrate characteristics, the buildup with an integrated chip has to be as small as possible. Chips with a thickness of only 20 µm are used and the interconnection should not exceed a couple of microns.

The technology relies on a flip chip-type mounting of the thin chip onto the flex substrate and lamination of the structure on both sides (Fig. 9.16). Contacts to outer layers are realized by through holes. Further layers can be added to the buildup. The electrical interconnections are extremely thin and the mechanical coherence of the chip to the substrate is ensured by the no-flow underfiller. Process technologies for embedding passive and active components into flex wiring boards are also being developed and investigated in a European Union funded project [6].

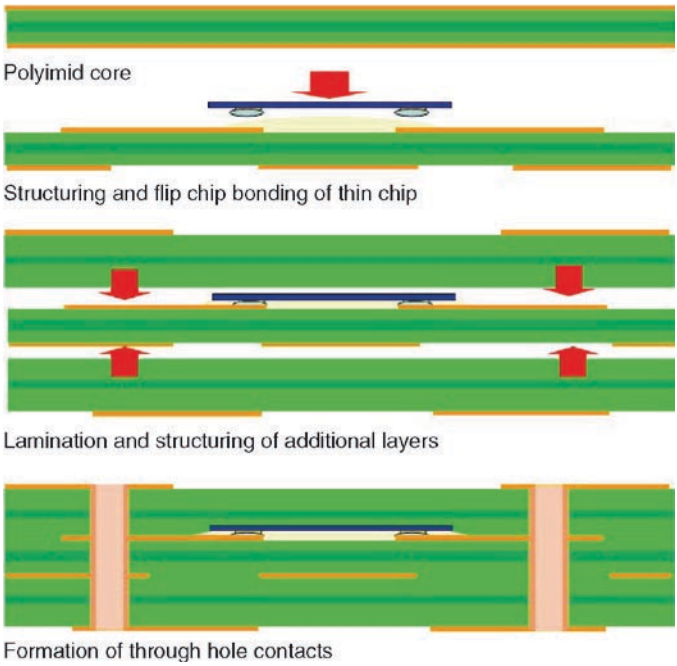


Fig. 9.16 Schematic process flow of embedding of thin chips into a flexible wiring board

9.4.4 Functional Packaging

Functional packaging goes one step further. It takes the application system and its requirements as a starting point and then adapts the microelectronic functions. One example is a radar sensor for the safety cocoon of a car, which is currently being developed by several partners as part of a project supported by the German Federal Government (Fig. 9.17). To equip midsize cars with this sensor technology, production cost is projected to be significantly lower than that of the predecessor model, which is presently used in the luxury class. This is to be made possible by a combination of two innovative embedding technologies. First, active and passive components are integrated into a plastic package by means of molding ("Chip in Duromer" [18]). This method ensures highly precise and fast mounting of the components. The subsequent molding process evens out the various component heights and makes lasting, precise alignment between the components possible.

The modules are then embedded into a PCB in the same way as described earlier in the "chip-in-polymer" paragraph and are bonded by means of a technique that ensures HF suitability (substrate embedding or chip in polymer [5]). A second layer of HF-suited PCB materials is laminated on top of the first layer and the respective antenna structures are realized by standard PCB processes. The two layers are then

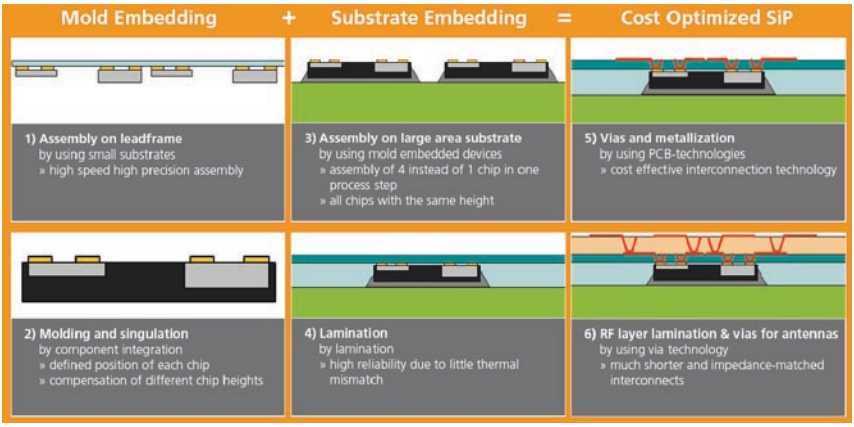
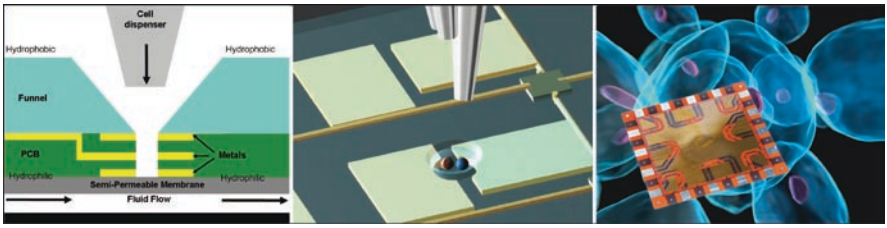


Fig. 9.17 Functional packaging for a cost-optimized radar sensor for active driver assistance systems [11]



Microwell Cross Cut | Principle of dielectrophoretic multi-well sensor | Implementation in PCB-Technology

Fig. 9.18 Using PCB technologies for lab on substrate [19]

electrically connected by means of µ-vias. Thanks to the low thermal mismatch – this embedding process promises high reliability with simultaneously improved HF characteristics as a result of shorter electrical contacts, which have been adjusted to impedance requirements [11].

9.4.5 Integration of Biological Functionalities

Merging new fabrication techniques and handling concepts with microelectronics enables the realization of intelligent microwells suitable for future applications, e.g., improved cancer treatment [19]. For the implementation of a dielectrophoresis enhanced microwell device a technology based on standard PCB technology has been developed in a European project, funded by the EU (Fig. 9.18). Because materials from PCB technology, such as copper or FR4, are not biocompatible, new materials have

to be selected. Aluminum has been selected as the base conducting metal layer, structured by laser micromachining in combination with etching, and laminated successively to obtain minimum registration tolerances of the respective layers.

The microwells are also laser machined into the laminate, allowing capturing, handling, and sensing of individual cells as well as cell-to-cell interactions within a dielectrophoretic cage realized by the structured aluminum. Furthermore, surface treatments for hydrophobic and hydrophilic surface modification with, e.g., thiols and fluorinated acrylates on different materials were evaluated and analyzed by surface tension and wetting analysis to allow designing the microfluidic networks required for the microwell device [19].

9.5 3D Integration

Future microelectronic applications require significantly more complex devices with a high degree of miniaturization and flexibility. A possible answer to this challenge is 3D system integration technology that enables the combination of different optimized technologies with the potential for low-cost fabrication through high yield, smaller IC footprints, and multifunctionality. 3D system integration also has the potential to overcome the wiring crisis of signal propagation delay at both board and chip level – thanks to minimal interconnection lengths and the elimination of speed-limiting intra and interchip interconnections. The first 3D packaging technologies were developed in the early 1980s, primarily for space and military applications, and were based on enhanced MCMs (multichip module). The major hurdles were yield and cost. The infrastructure for KGD (known good dies), which is essential for most of the stacking approaches, was not yet established. Therefore, 3D approaches were not used for industrial products. Since the beginning of the twenty-first century the need for further miniaturization and higher performance has led to a comeback in 3D approaches (Fig. 9.19).

Three different 3D packaging approaches are currently discussed:

- Stacking of packages (PoP, PiP)
- Embedding of active and/or passive devices
- Stacking of bare dies without through-silicon wires (TSV)
- Stacking of bare dies with TSV

9.5.1 Package Stacking

The stacking of assembled and tested packages enables a 3D integration of high-density logic and memory device combinations at overall cost when considering both one of and ongoing development and production cost. Hence, industry is adopting package stacking solutions. This technology holds technical and business

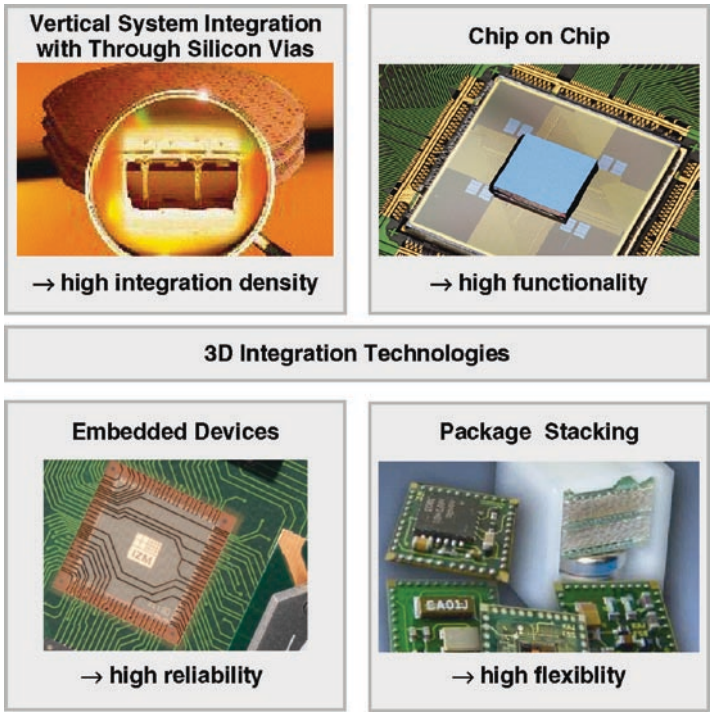


Fig. 9.19 3D integration technologies

benefits for each step in the supply chain. Examples of package stacking solutions include digital camera and cell phone applications with, at the present technological level, two-package stacks for logic and memory architectures. High-density DRAM and flash memory modules are stacked up to four packages high, with stacks of eight pieces possible [10].

The 3D module stacking method is a casing concept that is able to produce small, reliable, and highly robust systems rapidly and cost effectively [9]. The construction kit enables a hierarchic assembly of the chosen manufacturing technology Fig. 9.20. While the particular modules are fabricated by means of complex production technologies (e.g., usage of components without housing), the modules are later assembled using conventional SMD processes. With this concept, enterprises are able to produce complex customer-specific systems without owning a corresponding production line. At the same time it is possible to produce the particular modules utilizing the economy of scale for high quantities by producing each module in higher quantities. For highest integration, a reliable miniaturized interconnection technology for a wide range of different components as, for example, sensors or active and passive components is crucial. Chip-on-board technologies, using bare dies, wire bonding, and e.g., 01005 SMD components, are one approach. By using advanced flip chip technology with thinned bare silicon dies, the realization of even

smaller volume assemblies is possible for each particular module. Handling and soldering of 10-µm thin dies with 10-µm bump height has already been demonstrated. Another advanced technology for miniaturization of each particular module is – as shown in chapter 9.4 – the embedding of active and passive components into the substrates (Fig. 9.21).

A similar concept for package stacking is using advanced technologies for embedding active and passive components into rigid substrates. One approach uses – as described in Sect. 9.4 – thin chips that are die bonded and embedded by lamination of RCC layers for ultrathin stackable packages. Initial fabrication of highly integrated system-in-package modules, followed by assembly of a standard package, is also possible.

Apart from the reductions in size by using thin flexible substrates, a 3D buildup can be realized by folding the flex, which also leads to a decrease in footprint (Fig. 9.11). The chips are soldered or glued to flex substrates, followed by embedding in an adhesive layer. Further layers can be applied or other components can be assembled by conventional technique on top. Chapters 9.3 and 9.4 detail the process.

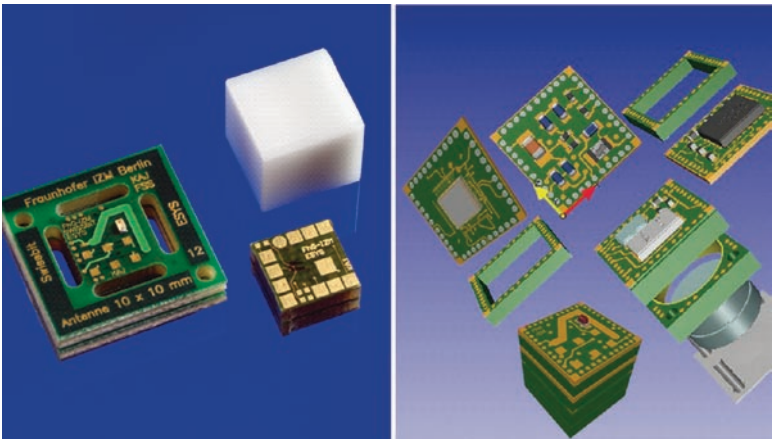


Fig. 9.20 Module stacking concept [9]

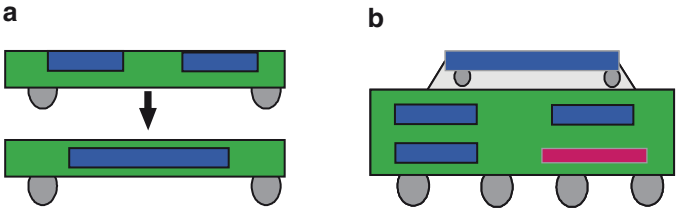


Fig. 9.21 Potential of embedded chips for 3D integration: (**a**) ultrathin stackable packages, (**b**) highly integrated system-in-package module

9.5.2 Embedding of Active and/or Passive Devices

The embedding of active and passive components into redistribution layers of a wafer or into the printed wiring board is a challenging approach for increasing the integration density of assembled electronic systems. Details are described in Chapters 9.3.2 and 9.4.1–9.4.3.

9.5.3 Stacking Without Through-Silicon Vias

Die stacking makes integrating multiple chips in one package possible. Wire bonding techniques for stacking three and more dice are now well established and can be used for both digital and nondigital components. Another focus is on state-of-the-art chip-on-chip technologies based on flip chip interconnects. The approach requires a base die with redistribution traces to match the I/O layout of both dice. This makes combining the performance advantage of FC with the option of integration of passive components into the redistribution layer possible. Figure 9.22 shows a stacked FC-BGA with a flip chip-mounted microcontroller on a second silicon chip with redistributed IC pads. The interconnection from the interposer to the board is achieved by wire-bonding technique.

In this approach a functional base chip on wafer level is used as an active substrate for FC-bonding of a second die [16]. The electrical and mechanical interconnection is carried out using eutectic solder balls, which are deposited by electroplating. The base chip is redistributed to an area array of a solderable UBM. The redistribution consists of electroplated copper traces, which ensures a low electrical resistance. Dielectric isolation is achieved using low-*k* photo-BCB. Integrating passives on the large die is possible.

The SOLID process (solid-liquid-interdiffusion) is a similar process but Cu/Sn layers are used instead of solder (Fig. 9.23).

The formation of intermetallics is the basis for the physical and electrical interconnection [12].

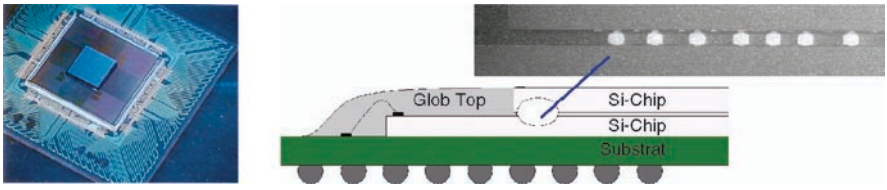


Fig. 9.22 Chip-on-chip integration using FC-bonding

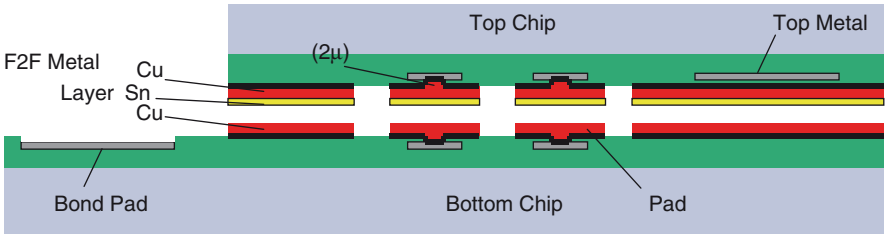


Fig. 9.23 Principle of the SOLID process

9.5.4 Stacking with Through-Silicon Vias

One of the first packages manufactured with TSV was introduced by Schott Electronic Packaging. It was strongly focused on optical applications and is a smart combination of wafer-level packaging and MEMS processing technology [17]. Optical packaging and most MEMS packages have to solve a very basic problem when advanced assembly techniques are to be applied to the device: the sensor surface has to interact with the environment without the packaging restricting the sensor in any way and, at the same time, protecting the sensor device against the environment. Wafer-level packaging is possible if the active area of the sensor is on one side of the device and the grid array contacts for the interconnection are placed on the reverse side. For an image sensor chip, silicon-via-contacts are central to this approach.

Standard silicon device wafers were the starting point of the SCHOTT OPTO-WLP, which is schematically represented in Fig. 9.24. These device wafers, i.e., image sensors – both CCD or CMOS – as well as surface-MEMS devices, typically have an active sensor surface on one side of a silicon substrate. In between the silicon and/or material comprising this active surface, an interdielectric layer may be found, which may consist of a wide range of dielectric materials, such as silicon oxide and/or silicon nitride. Standard contact pads, typically metallic, are on top of the same insulating layer. Later in the process, these contact pads are directly connected by the silicon-via-contacts. This means that the same pads used for testing or wire bonding are used for packaging as well. The first step in the SCHOTT OPTO-WLP process is the protection of sensitive active structures by a high-quality cover glass. A specialized adhesive wafer bonding process was developed, which can either perform a full area bond or a selective coverage of the adhesive within that bond layer. In the next step, the bonded silicon–glass sandwich is thinned from the silicon side (reverse side). The thickness of the silicon is reduced to about 100 µm, ensuring low-profile, chip-size optical packages for the intended devices (Fig. 9.25).

The actual thickness of the silicon can be adjusted according to the device application: stress-sensitive devices may need a very different residual silicon thickness compared with more robust sensors, where 50-µm residual silicon thickness might

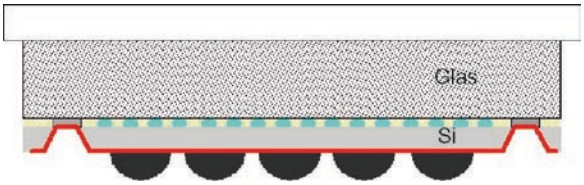


Fig. 9.24 Principle of OPTO WLP (courtesy of Schott Electronic Packaging)

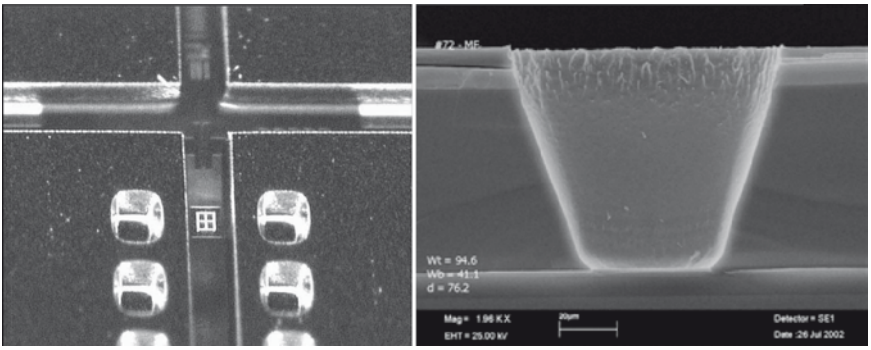
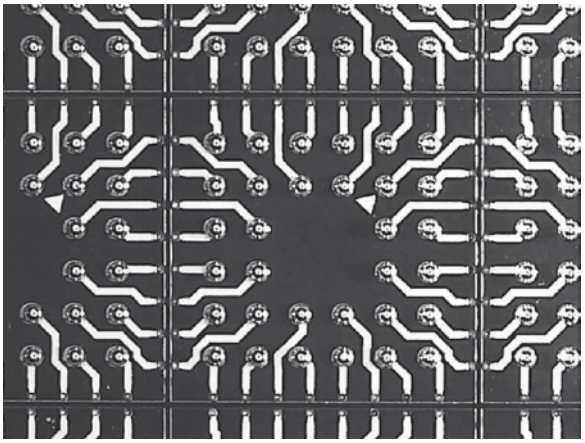


Fig. 9.25 TSV, left: video image; right: cross section (SEM)

Fig. 9.26 Video image of bumped CCD-WLP



be preferred. A highly specialized plasma etching process is used to structure the silicon. Preferably, tapered side walls are used for all structures. The deposition of dielectric layers over the silicon guarantees electrical isolation during the subsequent redistribution process, which is based on polymer/Cu or Al. After UBM deposition, the wafer is ready for the balling and dicing process (Fig. 9.26).

The introduction of microstructured glass will further improve this packaging concept. This new deposition technology will add hermetic sealant to MEMS WLP [7].

Vertical system integration is characterized by very high density vertical interchip wiring by through-Si vias with diameters of approximately 2 μm that can be positioned as required. Based on thinning, adjusted bonding, and vertical metallization of completely processed device substrates, the requirements for VSI are precise thinning technologies, reliable formation of interchip vias (ICV), and a suitable bonding process. In general, technologies largely relying on standard wafer fabrication processes exhibit a favorable cost structure. On the other hand, wafer yield and even more importantly chip area issues speak against plain wafer stacking concepts. Consequently, chip-to-wafer technologies, mainly based on wafer-level processes utilizing known good dice, are preferable. So-called ICV-SLID technology is optimized for chip-to-wafer stacking and provides a very high vertical interconnect density based on ICV between metallization levels of stacked dice. Both the mechanical and vertical electrical connections are realized by solid–liquid interdiffusion (SLID) of thin electroplated and structured copper/tin layers. The thinned chips with tungsten- or copper-filled ICV are connected to the bottom device wafer by the SLID system (Cu, Cu_3Sn, Cu). This fully modular concept makes multiple device stacks possible [13].

9.6 Conclusion

Smart innovative systems linked into networks and used in an extremely broad range of applications are the future of electronics. They will contain electrical and nonelectrical functions. The task of heterogeneous integration will be integrating such functions into one system. For the fabrication of heterogeneous systems, new architectures and system integration technologies are necessary, which have to ensure the realization of reliable systems at minimal sizes and at low production costs. Adequate interfaces for different application environments have to be created. By optimizing heterogeneous system integration one will meet the following requirements:

- Integrated on-chip off-chip design as well as system partitioning/modularization
- Highly reliable systems
- Integration of electrical and nonelectrical components
- Integrated wireless communication
- Integrated power conversion and storage
- Integration of different functions in one module/package
- Application of “add-on” technologies to increase system functionality
- Ultrahigh density component integration
- Short time-to-market processes and low-cost solutions

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