Chapter 3

Junction Barrier Controlled Schottky Rectifiers

In the case of Schottky rectifiers, it is necessary to trade-off the on-state (or conduction) power loss against the reverse blocking power loss by optimizing the Schottky barrier height[1]. As the Schottky barrier height is reduced, the on-state voltage drop decreases producing smaller conduction power loss. At the same time, the smaller barrier height produces an increase in the leakage current leading to larger reverse blocking power loss. The power loss can be minimized by reducing the Schottky barrier height at the expense of a reduced maximum operating temperature. This optimization process is exacerbated by the rapid increase in the leakage current with increasing reverse bias voltage due to the Schottky barrier lowering and pre-breakdown multiplication phenomena.

The first method proposed to ameliorate the barrier lowering effect in vertical silicon Schottky rectifiers utilized shielding by incorporation of a P-N junction[2,3]. Since the basic concept was to create a potential barrier to shield the Schottky contact against high electric fields generated in the semiconductor by using closely spaced P^+ regions around the contact, this structure was named the *'Junction-Barrier controlled Schottky (JBS) rectifier'*. In the JBS rectifier, the on-state current is designed to flow in the un-depleted gaps between the P^+ regions when the diode is forward biased to preserve unipolar operation. In addition to reducing the leakage current, the presence of the P^+ regions improves the ruggedness of the diodes. Detailed optimization of the silicon JBS rectifier characteristics has been achieved with sub-micron dimensions for forming the P^+ regions[4]. Minimization of the area consumed by the P^+ regions reduces the spreading resistance of the drift region below the Schottky contact resulting in a lower on-state voltage drop.

In the previous chapter, it was also demonstrated that the increase in leakage current with reverse bias voltage is much stronger for the silicon carbide

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Schottky rectifiers. This is due to a larger Schottky barrier lowering effect associated with the larger electric field in silicon carbide drift regions and the onset of thermionic field emission (or tunneling) current. It is therefore obvious that the methods proposed to suppress the electric field at the Schottky contact in silicon diodes will have even greater utility in silicon carbide rectifiers.

This chapter discusses the application of the junction barrier controlled shielding concept to reduce the electric field at the metal-semiconductor contact in silicon and 4H-SiC Schottky rectifiers. In addition to analytical models, the physics of operation of these structures is analyzed by using two-dimensional numerical simulations. It is demonstrated that the JBS concept improves the performance of silicon devices and can be extended to silicon carbide devices[5] to achieve even greater improvements in performance.

3.1 Junction Barrier Schottky (JBS) Rectifier Structure

The Junction Barrier controlled Schottky (JBS) rectifier structure is illustrated in Fig. 3.1. It consists of a P^+ region placed around the Schottky contact to generate a potential barrier under the metal-semiconductor contact in the reverse blocking mode to shield the Schottky contact. The magnitude of the potential barrier depends upon the separation between the P-N junctions and the junction depth. A smaller separation and larger junction depth favors an increase in the magnitude of the potential barrier leading to a greater reduction of the electric field at the Schottky contact. A reduction of the electric field at the Schottky contact produces a smaller barrier lowering and field emission effect, which is beneficial for reducing the leakage current at high reverse bias voltages.

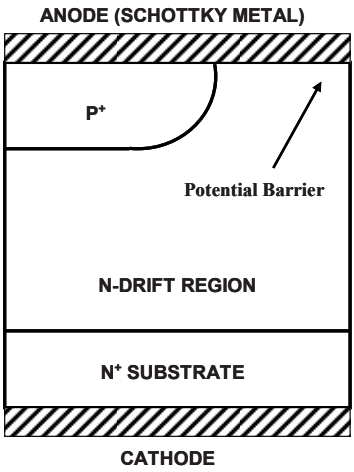

Fig. 3.1 Junction Barrier controlled Schottky (JBS) Rectifier Structure.

The space between the P^+ regions is also chosen so that there is an un-depleted region below the Schottky contact during on-state operation to enable unipolar conduction through the structure. In the JBS rectifier, the voltage drop across the diode is insufficient to forward bias the P-N junction. Silicon devices with low breakdown voltages operate with on-state voltage drops (around 0.45 volts) well below the 0.7 volts needed for inducing strong injection across the P-N junction. The margin is even larger for silicon carbide due to its much larger band gap. Typical silicon carbide Schottky rectifiers have on-state voltage drops of less than 1.5 volts due to the low specific resistance of the drift region. This is well below the 3 volts required to induce injection from the P-N junction. Consequently, the JBS concept is well suited for development of silicon carbide structures with very high breakdown voltages.

The P^+ region is usually formed by ion-implantation of P-type dopants using a mask with appropriate spacing to leave room for the Schottky contact. For processing convenience, the same metal layer is used to make an ohmic contact to the highly doped P^+ region as well as to make the Schottky barrier contact to the N- drift region. The space between the P^+ regions must be optimized to obtain the best compromise between reducing the on-state voltage drop and reducing the leakage current.

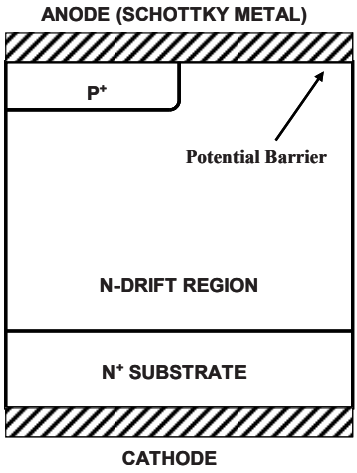

Fig. 3.2 Silicon Carbide Junction Barrier controlled Schottky (JBS) Rectifier Structure.

In silicon devices, the P-N junction is formed with an annealing cycle that creates a planar junction with its extension in the lateral direction as shown in Fig. 3.1. The additional area consumed by the lateral diffusion must be accounted for during the analytical modeling of the JBS rectifier structure. In addition, the cylindrical shape of the junction allows encroachment of the cathode potential towards the Schottky contact producing an enhancement of the electric field at the contact with increasing reverse bias voltage. In the case of silicon carbide devices,

there is no significant diffusion during the annealing of the ion implants. A rectangular shape for the P-N junction is appropriate for these structures as illustrated in Fig. 3.2.

It is worth pointing out that the reverse blocking voltage is supported in the JBS rectifier structure by the depletion region formed below the P^+/N junction. This junction is usually used to simultaneously form the edge termination for silicon diodes. For these low voltage silicon structures, it is usually sufficient to utilize a cylindrical edge termination with a field plate to enhance the breakdown voltage. The breakdown voltage is therefore reduced to about 80 percent of the ideal parallel-plane value. The doping concentration for the drift region must be computed after accounting for this reduction in the breakdown voltage:

$$N_D = \left(\frac{5.34x10^{13}}{BV_{PP}} \right)^{4/3} \quad \textbf{[3.1]}$$

where BV_{PP} is the breakdown voltage for the parallel-plane case after accounting for the edge termination.

An error that is often made during design of these devices is to make the thickness of the drift region below the P-N junction equal to the depletion width for the ideal parallel-plane junction with the above doping concentration. In actuality, the maximum depletion width is limited to that associated with the breakdown voltage (BV) of the structure, as given by:

$$t = W_D(BV) = \sqrt{\frac{2\varepsilon_S BV}{qN_D}} \quad \textbf{[3.2]}$$

The thickness of the drift region required below the P-N junction is therefore less than the depletion width for the ideal parallel-plane junction with the above doping concentration. The resistance of the drift region below the Schottky contact is consequently enhanced above that for the ideal parallel-plane case due to current transport between the junctions and the lower doping concentration of the drift region.

3.2 Forward Conduction Models

Analysis of the on-state voltage drop of the JBS rectifier requires taking into consideration the current constriction at the Schottky contact due to the presence of the P^+ region and the enhanced resistance of the drift region[6] due to current spreading from the Schottky contact to the N^+ substrate. Several models can be developed for the spreading resistance, which are appropriate to different JBS rectifier designs. In addition, the different shape for the P-N junction in silicon carbide warrants a unique model as well. These models are developed below. In all the models, it is assumed that the voltage drop in the on-state for the JBS rectifier is well below the voltage required to induce current flow across the P-N junction.

3.2.1 Silicon JBS Rectifier: Forward Conduction Model A

The current flow pattern in the forward conduction mode for Model A for a silicon JBS rectifier is illustrated in Fig. 3.3 with the shaded area. The model takes into account the presence of a depletion layer at the P-N junction which increases the current density at the Schottky contact. The current through the Schottky contact flows only within the un-depleted portion (with dimension 'd') of the drift region at the top surface. Consequently, the current density at the Schottky contact (J_{FS}) is related to the cell (or cathode) current density (J_{FC}) by:

$$J_{FS} = \left(\frac{p}{d}\right) J_{FC} \qquad \textbf{[3.3]}$$

where p is the cell pitch. The dimension 'd' is determined by the cell pitch (p), the size of the ion-implant window (2s), the junction depth of the P^+ region, and the on-state depletion width ($W_{D,ON}$):

$$d = p - s - x_J - W_{D,ON} \qquad \textbf{[3.4]}$$

In deriving this equation, it has been assumed that the lateral diffusion is equal to the junction depth. Depending up on the lithography used for device fabrication to minimize the size (dimension 's') of the P^+ region, as well as the junction depth

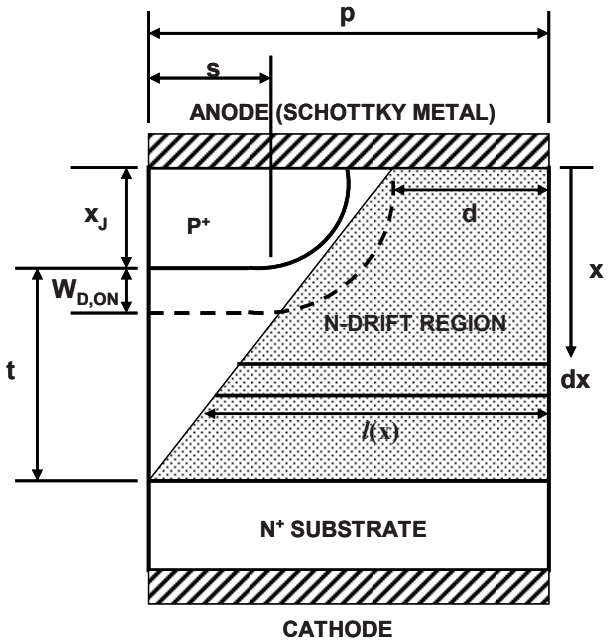

Fig. 3.3 Current Flow Pattern in the Silicon JBS Rectifier Structure during Operation in the On-State: Model A.

(x_J) created during the diffusion process, the current density at the Schottky contact can be enhanced by a factor of two or more. This must be taken into account when computing the voltage drop across the Schottky contact given by:

$$V_{FS} = \phi_B + \frac{kT}{q}\ln\left(\frac{J_{FS}}{AT^2}\right) \quad \textbf{[3.5]}$$

After crossing the Schottky contact, the current flows through the un-depleted portion of the drift region. The resistance of the drift region is larger than the specific on-resistance discussed in the previous chapter due to current spreading from the Schottky contact to the N^+ substrate as illustrated for Model A in the figure. In this model, it is assumed that the current spreads from the Schottky contact region (width d) to the entire cell pitch (p) at the bottom of the drift region. In order to obtain this spreading resistance, consider a sliver of the conduction region with a thickness dx located at a depth of x from the surface. The width l(x) of this segment is given by:

$$l(x) = d + \frac{(p-d).x}{(x_J + t)} \quad \textbf{[3.6]}$$

The resistance of the segment is given by:

$$dR_{drift} = \frac{\rho_D.dx}{l(x).Z} = \frac{\rho_D.(x_J + t).dx}{[d.(x_J + t) + (p-d).x]Z} \quad \textbf{[3.7]}$$

where Z is the length of the cell in the direction orthogonal to the cross-section shown in the figure. The resistance of the drift region can be obtained by integration of this resistance between the surface (x = 0) and the N^+ substrate ($x = x_J + t$):

$$R_{drift} = \frac{\rho_D}{Z}\left(\frac{x_J + t}{p-d}\right).\ln\left(\frac{p}{d}\right) \quad \textbf{[3.8]}$$

The specific resistance for the drift region can be calculated by multiplying the cell resistance by the cell-area (p.Z):

$$R_{sp,drift} = \rho_D.p.\left(\frac{x_J + t}{p-d}\right).\ln\left(\frac{p}{d}\right) \quad \textbf{[3.9]}$$

In addition, it is important to include the resistance associated with the thick, highly doped N^+ substrate because this is comparable to that for the drift region in some instances. The specific resistance of the N^+ substrate can be determined by taking the product of its resistivity and thickness. For silicon, N^+ substrates with resistivity of 1 mΩ-cm are available. The specific resistance contributed by the N^+ substrate with a typical thickness of 200 microns is 2×10^{-5} Ω-cm^2.

The on-state voltage drop for the JBS rectifier at a forward cell current density J_{FC}, including the substrate contribution, is then given by:

$$V_F = \phi_B + \frac{kT}{q}\ln\left(\frac{J_{FS}}{AT^2}\right) + \left(R_{sp,drift} + R_{sp,subs}\right).J_{FC} \quad \textbf{[3.10]}$$

When computing the on-state voltage drop using this equation, it is satisfactory to make the approximation that the depletion layer width can be computed by subtracting an on-state voltage drop of about 0.45 volts from the built-in potential of the P-N junction. In addition, it is important to recognize that the doping profile at the junction is linearly graded leading to half the depletion occurring on the P-side of the junction. Consequently:

$$W_{D,ON} = 0.5.\sqrt{\frac{2\varepsilon_S\left(V_{bi}-0.45\right)}{qN_D}} \quad \textbf{[3.11]}$$

where V_{bi} is the built-in potential of the abrupt P^+/N junction. In the case of silicon JBS rectifiers with breakdown voltage in the range of 30 to 60 volts, the depletion width ($W_{D,ON}$) is about 0.1 to 0.15 microns.

3.2.2 Silicon JBS Rectifier: Forward Conduction Model B

The current flow pattern in Model B for the forward conduction mode of a silicon JBS rectifier is illustrated in Fig. 3.4 with the shaded area. The current density at the Schottky contact (J_{FS}) is enhanced as already discussed for Model A due to the presence of the P^+ diffusion and the depletion layer at the P-N junction. This increases the voltage drop across the Schottky contact as defined by Eq. [3.3] – Eq. [3.5]. After crossing the Schottky contact, the current flows through the un-depleted portion of the drift region between the junctions. In Model B, it is assumed that the current flows through a region with a uniform width 'd' until it reaches the bottom of the depletion region and then spreads to the entire cell pitch (p) at the bottom of the drift region.

The net resistance to current flow can be calculated by adding the resistance of the two segments. The resistance of the first segment of uniform width 'd' is given by:

$$R_{D1} = \frac{\rho_D.\left(x_J + W_{D,ON}\right)}{d.Z} \quad \textbf{[3.12]}$$

The spreading resistance of the second segment can be derived by using the same approach used for Model A:

$$R_{D2} = \frac{\rho_D}{Z}\left(\frac{t - W_{D,ON}}{p-d}\right).\ln\left(\frac{p}{d}\right) \quad \textbf{[3.13]}$$

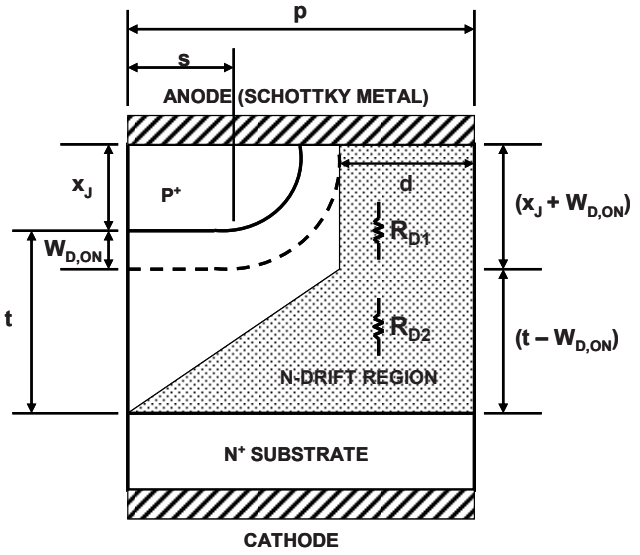

Fig. 3.4 Current Flow pattern in the Silicon JBS Rectifier Structure during Operation in the On-State: Model B.

The net spreading resistance of the drift region is then given by:

$$R_{drift} = \frac{\rho_D.\left(x_J + W_{D,ON}\right)}{d.Z} + \frac{\rho_D}{Z}\left(\frac{t - W_{D,ON}}{p - d}\right).\ln\left(\frac{p}{d}\right) \qquad \textbf{[3.14]}$$

The specific resistance for the drift region can be calculated by multiplying the cell resistance by the cell-area (p.Z):

$$R_{sp,drift} = \frac{\rho_D.p.\left(x_J + W_{D,ON}\right)}{d} + \rho_D.p.\left(\frac{t - W_{D,ON}}{p - d}\right).\ln\left(\frac{p}{d}\right) \qquad \textbf{[3.15]}$$

The on-state voltage drop for the JBS rectifier at a forward cell current density J_{FC}, including the substrate contribution, is then given by:

$$V_F = \phi_B + \frac{kT}{q}\ln\left(\frac{J_{FS}}{AT^2}\right) + \left(R_{sp,drift} + R_{sp,subs}\right).J_{FC} \qquad \textbf{[3.16]}$$

When computing the on-state voltage drop using this equation, it is satisfactory to make the approximation that the depletion layer width can be computed by subtracting an on-state voltage drop of about 0.45 volts from the built-in potential of the P-N junction. In addition, it is important to recognize that the doping profile at the junction is linearly graded leading to half the depletion occurring on the P-side of the junction. Consequently:

$$W_{D,ON} = 0.5.\sqrt{\frac{2\varepsilon_S\left(V_{bi}-0.45\right)}{qN_D}} \quad \textbf{[3.17]}$$

where V_{bi} is the built-in potential of the abrupt P^+/N junction. In the case of silicon JBS rectifiers with breakdown voltage in the range of 30 to 60 volts, the depletion width ($W_{D,ON}$) is about 0.1 to 0.15 microns.

3.2.3 Silicon JBS Rectifier: Forward Conduction Model C

When the ion-implant window (2s) for the P^+ region is reduced with improved lithographic design rules, the current path in the drift region can overlap before reaching the N^+ substrate. The current flow pattern for this case (Model C) is illustrated in Fig. 3.5 with the shaded area. The current density at the Schottky contact (J_{FS}) is enhanced in Model C as already discussed for Model B due to the presence of the P^+ region and the depletion layer at the P-N junction. This increases the voltage drop across the Schottky contact as defined by Eq. [3.3] – Eq. [3.5]. After flowing across the Schottky contact, the current flows through the un-depleted portion of the drift region between the junctions. In Model C, it is assumed that the current flows through a region with a uniform width 'd' until it reaches the bottom of the depletion region and then spreads to the entire cell pitch (p) at a 45 degree spreading angle. The current paths overlap at a distance ($s + x_J + W_{D,ON}$) from the bottom of the depletion region. The current then flows through a uniform cross-sectional area.

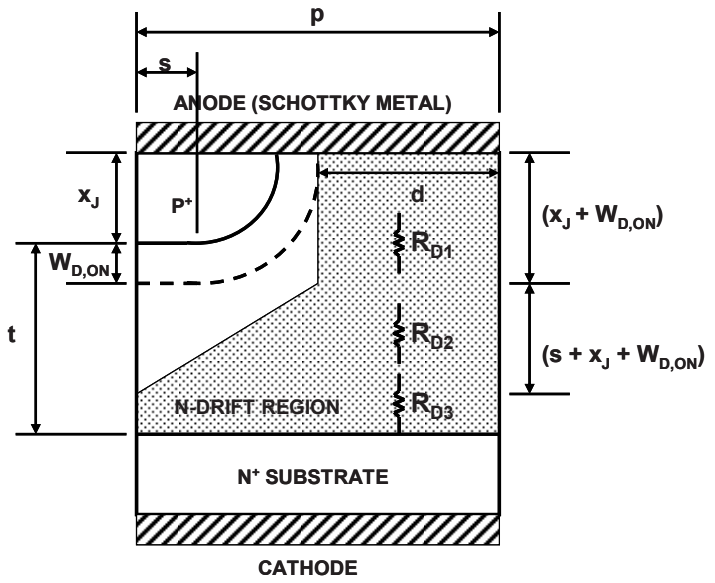

Fig. 3.5 Current Flow pattern in the Silicon JBS Rectifier Structure during Operation in the On-State: Model C.

The net resistance to current flow can be calculated by adding the resistance of the three segments. The resistance of the first segment of uniform width 'd' is given by:

$$R_{D1} = \frac{\rho_D.\left(x_J + W_{D,ON}\right)}{d.Z} \quad \textbf{[3.18]}$$

The resistance of the second segment can be derived by using the same approach used for Model A. However, the width of the segment for the current flow path in this case is given by:

$$l(x) = d + x \quad \textbf{[3.19]}$$

because of the 45 degree spreading angle. Using this expression, the resistance for the second segment is given by:

$$R_{D2} = \frac{\rho_D}{Z}\ln\left(\frac{p}{d}\right) \quad \textbf{[3.20]}$$

The resistance of the third segment with a uniform cross-section of width p is given by:

$$R_{D3} = \frac{\rho_D.\left(t - s - x_J - 2W_{D,ON}\right)}{p.Z} \quad \textbf{[3.21]}$$

The specific resistance for the drift region can be calculated by multiplying the cell resistance ($R_{D1} + R_{D2} + R_{D3}$) with the cell-area (p.Z):

$$R_{sp,drift} = \frac{\rho_D.p.\left(x_J + W_{D,ON}\right)}{d} + \rho_D.p.\ln\left(\frac{p}{d}\right) + \rho_D.\left(t - s - x_J - 2W_{D,ON}\right) \quad \textbf{[3.22]}$$

The on-state voltage drop for the JBS rectifier at a forward cell current density J_{FC}, including the substrate contribution, is then given by:

$$V_F = \phi_B + \frac{kT}{q}\ln\left(\frac{J_{FS}}{AT^2}\right) + \left(R_{sp,drift} + R_{sp,subs}\right).J_{FC} \quad \textbf{[3.23]}$$

When computing the on-state voltage drop using this equation, it is satisfactory to make the approximation that the depletion layer width can be computed by subtracting an on-state voltage drop of about 0.45 volts from the built-in potential of the P-N junction. In addition, it is important to recognize that the doping profile at the junction is linearly graded leading to half the depletion occurring on the P-side of the junction. Consequently:

$$W_{D,ON} = 0.5.\sqrt{\frac{2\varepsilon_S\left(V_{bi} - 0.45\right)}{qN_D}} \quad \textbf{[3.24]}$$

where V_{bi} is the built-in potential of the abrupt P^+/N junction. In the case of silicon JBS rectifiers with breakdown voltage in the range of 30 to 60 volts, the depletion width ($W_{D,ON}$) is about 0.1 to 0.15 microns.

3.2.4 Silicon JBS Rectifier: Example

In order to understand the differences between the above models for forward current flow in the JBS rectifier structure, it is instructive to consider a specific example of a device with breakdown voltage of 50 volts. If the edge termination limits the breakdown to 80 percent of the ideal value, the parallel-plane breakdown voltage is 62.5 volts. This voltage can be supported by a depletion region width of 2.85 microns in the drift region with doping concentration of 8 x 10^{15} cm^{-3}. The depletion region width in the N-drift region calculated for this case under the assumption of an on-state voltage drop of 0.45 volts is 0.13 microns. If the JBS structure has a cell pitch (p) of 1.25 microns, and a P^+ region with depth of 0.5 microns is created using an ion-implant window (2s) of 0.5 microns, the dimension 'd' is found to be 0.37 microns. Consequently, the current density at the Schottky contact region where the current is transported is enhanced by a factor 3 times when compared with the cathode (or average cell) current density.

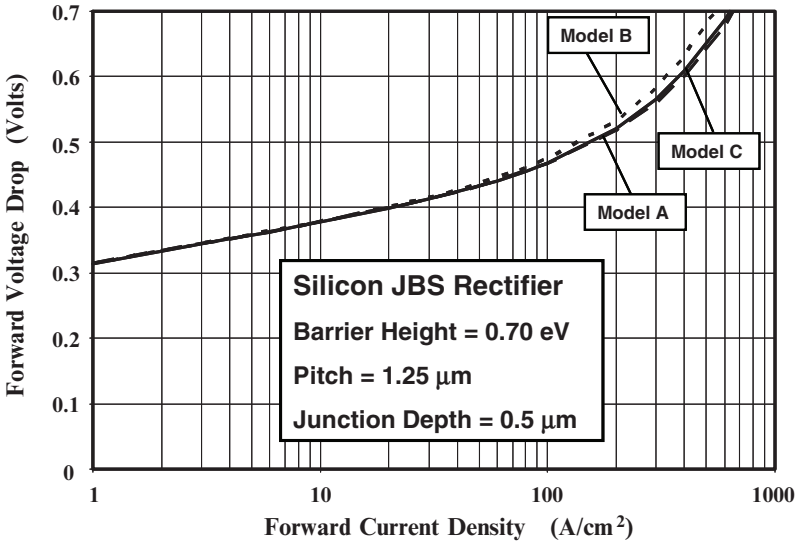

Fig. 3.6 Forward Characteristics of a 50V Silicon JBS Rectifier Structure.

The on-state *i-v* characteristics obtained by using the three models for the above JBS rectifier structure are shown in Fig. 3.6. A Schottky barrier height of 0.70 eV was used for this analysis. Although Model B is slightly pessimistic when compared with the other two models, their predictions are very close to each other for determination of the on-state voltage drop. The on-state voltage drop for this

JBS rectifier structure is found to be 0.467 volts at an on-state current density of 100 A/cm^2.

The impact of changing the cell pitch (p) on the on-state characteristics can be predicted by using any one of the three models. The results obtained by using model C are shown in Fig. 3.7 for the case of a Schottky barrier height of 0.7 eV. The *i-v* characteristic of a planar Schottky rectifier with the same drift region parameters is included for comparison. The impact on the on-state voltage drop is small as long as the pitch is more than 1.25 microns. However, the on-state voltage drop increases by 10 percent when the pitch is reduced to 1.00 microns because of current constriction at the Schottky contact. Since a smaller cell pitch and space 'd' favors a smaller leakage current as discussed below, it is necessary to carefully choose, and precisely control, the cell pitch in the JBS rectifier in order to optimize its characteristics.

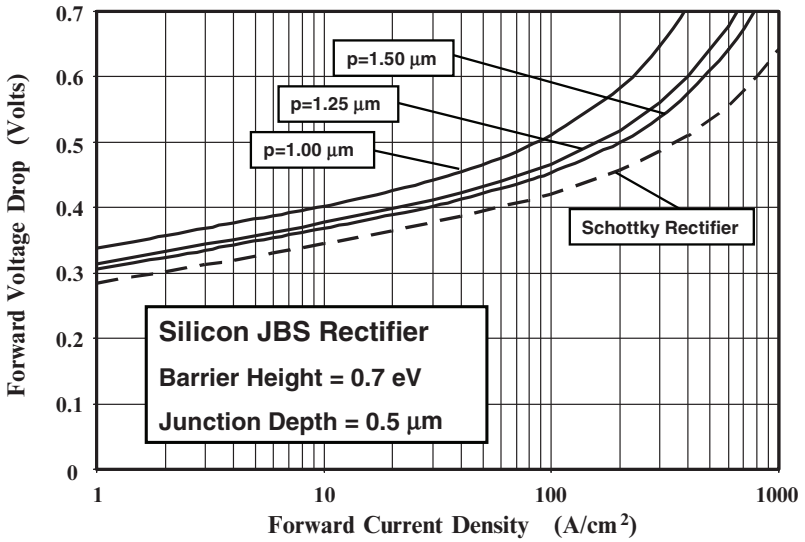

Fig. 3.7 Forward Characteristics of 50V Silicon JBS Rectifier Structures.

The degree of shielding of the Schottky contact by the P-N junction also depends upon the depth of the junction. A deeper junction improves the *aspect ratio* (defined later) of the region between the planar junctions. A larger aspect ratio has been found to provide greater shielding in the case of the vertical junction field effect transistor leading to a larger blocking gain[7]. However, a deeper junction increases the cell pitch and the resistance of the first segment in Model C leading to a larger on-state voltage drop. This is illustrated in Fig. 3.8 where the analytically calculated forward *i-v* characteristics are shown for two junction depths. Increasing the junction depth from 0.5 to 1 micron increases the on-state voltage drop from 0.467 to 0.487 volts.

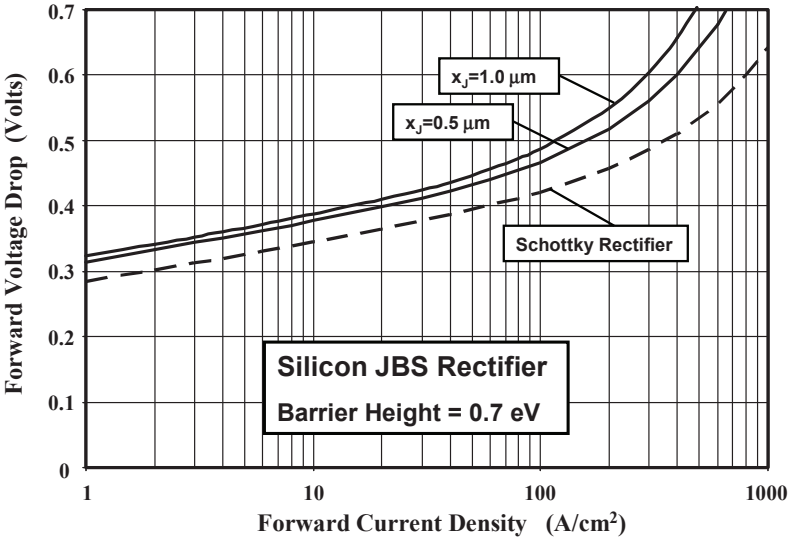

Fig. 3.8 Forward Characteristics of 50V Silicon JBS Rectifier Structures.

Simulation Example

In order to validate the above model for the on-state characteristics of the silicon JBS rectifier, the results of two-dimensional numerical simulations on a 50 V structure are described here. The structure had a drift region thickness of 3 microns with a doping concentration of 8 x 10^{15} cm^{-3}. The P^+ region had a depth of 0.5 microns with an ion-implant window (dimension 's' in Fig. 3.5) of 0.25 microns. A three-dimensional view of the doping profile for the structure is provided in Fig. 3.1E. The P^+ region is located on the upper left-hand side of the figure. The junction extends to 0.75 microns along the top surface, leaving 0.5 microns for the metal-semiconductor contact. However, a portion of this region is depleted by the junction potential.

The on-state *i-v* characteristics, obtained by using a barrier height of 0.7 eV, for the JBS rectifier with a cell pitch 'p' of 1.25 microns are shown in Fig. 3.2E. This plot includes the total current (cathode current) flowing through the structure together with the current flowing through the Schottky contact (dotted line) and the P^+ region (dashed line). It can be observed that the current flowing through the P^+ region is extremely small unless the on-state voltage drop exceeds 0.7 volts. At an on-state current density of 100 A/cm^2, the on-state voltage drop is 0.45 volts indicating that there is no significant injection from the junction and all the current is flowing via the Schottky contact. The current flowing via the P^+ region is 6 orders of magnitude less than the current flowing via the Schottky contact. This ensures minimal impact of injection of any minority carriers from the P-N junction on the reverse recovery behavior of the JBS rectifier structure.

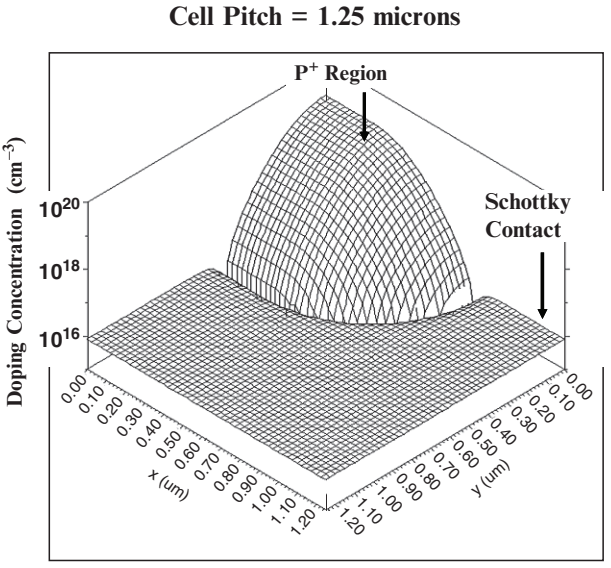

Fig. 3.1E Doping Profile for the 50V Silicon JBS Rectifier.

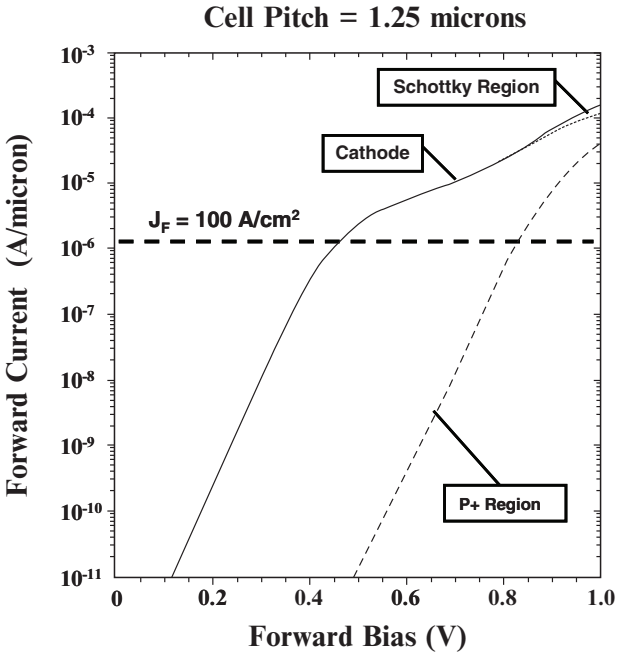

Fig. 3.2E On-State Characteristics for a 50V Silicon JBS Rectifier.

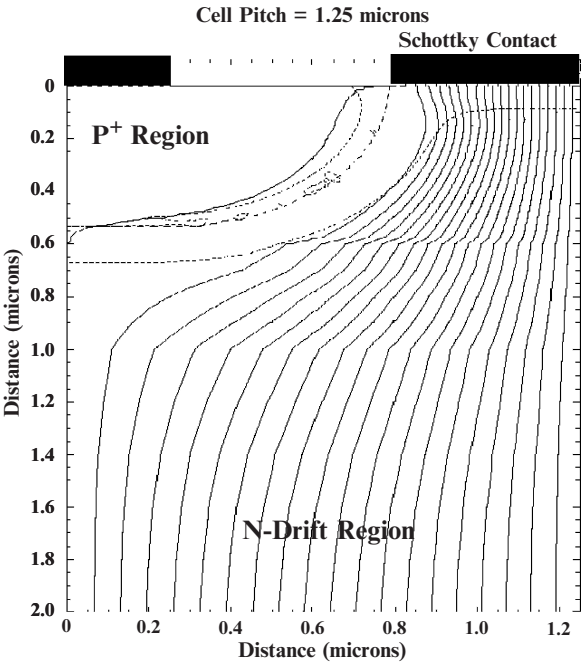

Fig. 3.3E On-State Current Distribution in a 50V Silicon JBS Rectifier.

The current flow-lines for the above JBS rectifier structure, shown in Fig. 3.3E at an on-state voltage drop of 0.5 volts, can be used to confirm that it operates in a unipolar current conduction mode. It can be seen that all the current flow-lines converge to the Schottky contact located on the upper right-hand-side of the structure demonstrating that no current flows via the P^+ region. The current flow pattern is consistent with Model C with an approximately uniform cross-section until the bottom of the depletion region followed by a spreading of the current at an angle of about 45 degrees. The current then becomes uniformly distributed below a depth of 1.5 microns from the surface. This justifies the use of a three region model for the series resistance of the drift region in Model C.

The on-state *i-v* characteristics of 50 V JBS rectifiers with cell pitch of 1.00 and 1.25 microns are compared with that of a Schottky rectifier with cell pitch of 1.25 microns in Fig. 3.4E. All the structures had a Schottky contact with barrier height of 0.7 eV. In the JBS rectifiers, the P^+ region was implanted through a window (2s) of 0.5 microns and had a depth of 0.5 microns. It can be observed that the on-state voltage drop for the JBS rectifiers is increased by the presence of the P^+ region. After accounting for the difference in the areas of the structures, the on-state voltage drop at an on-state current density of 100 A/cm^2 was found to be 0.45 V, and 0.49 V for the JBS rectifier structures when compared with 0.41 volts for the Schottky rectifier. As expected, there is an inflection in the curves for the JBS rectifiers at an on-state voltage drop of about 0.8 volts due to the on-set of injection from the P-N junction, which is not observed for the Schottky rectifier. These results are very close to those predicted by the analytical model (see Fig. 3.7) confirming its utility for analysis of the JBS rectifier structure in the on-state.

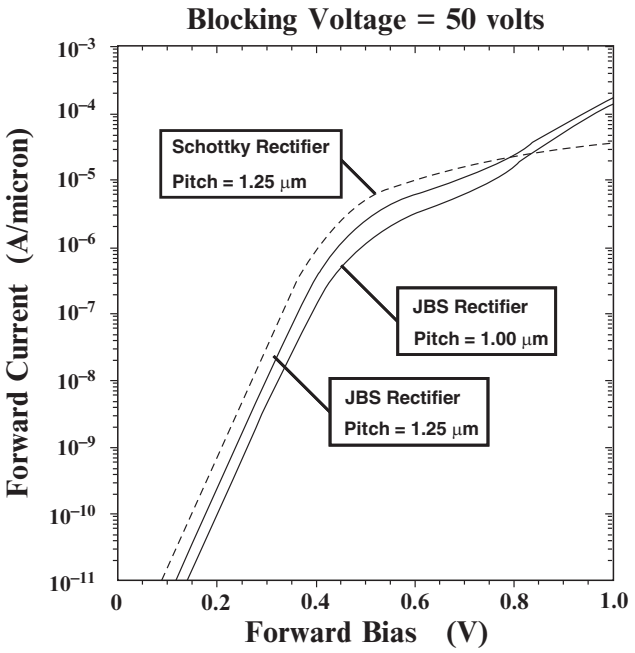

Fig. 3.4E On-State Characteristics for 50V Silicon JBS Rectifiers.

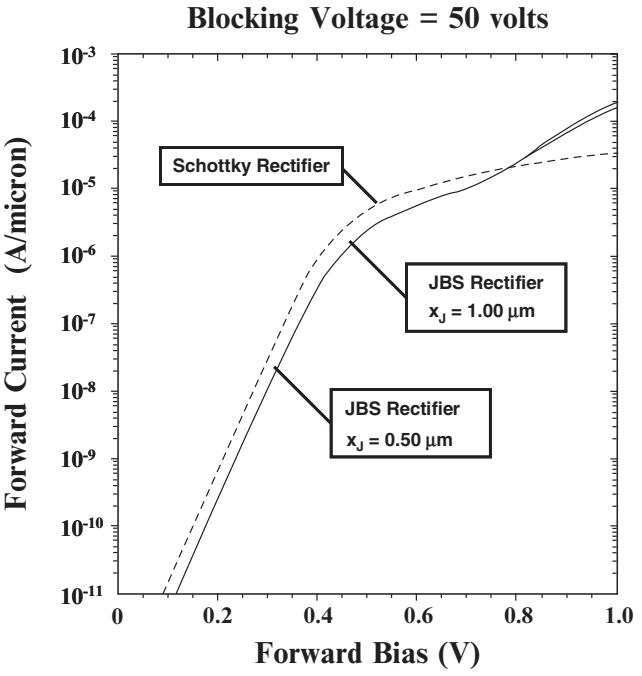

Fig. 3.5E On-State Characteristics for 50V Silicon JBS Rectifiers.

In the JBS rectifier, an increase in the junction depth improves the shielding of the Schottky contact. However, it also increases the resistance of the current path from the Schottky contact to the cathode. The impact of increasing the junction depth from 0.5 to 1.0 micron in the JBS rectifier structure was examined using numerical simulations by simultaneously increasing the cell pitch by 0.5 microns to retain the same Schottky contact size. The on-state *i-v* characteristics for this structure are compared with the structure with 0.5 micron junction depth in Fig. 3.5E. The i-v characteristics of the structures coincide because they have the same Schottky contact size and their cell resistances are almost equal. However, it is important to recognize that the cell area for the two structures is not equal. After accounting for this difference in cell areas, the on-state voltage drop at the same on-state current density of 100 A/cm^2 is not equal for the JBS rectifier structures. The on-state voltage drop for the structure with a junction depth of 1.0 microns is found to be larger than that for the structure with junction depth of 0.5 microns by 0.02 volts. This is in excellent agreement with the predictions of the analytical model (see Fig. 3.8).

3.2.5 Silicon Carbide JBS Rectifier: Forward Conduction Model

As discussed earlier for the silicon JBS rectifier structure, the three models produce close to the same on-state characteristics. Only a single model for the silicon carbide JBS rectifier is therefore developed in this section based upon the current flow pattern illustrated in Fig. 3.9 with the shaded area. This model, similar to Model C for the silicon JBS rectifier, accounts for the absence of lateral diffusion in silicon carbide junctions. In this model, it is assumed that the current

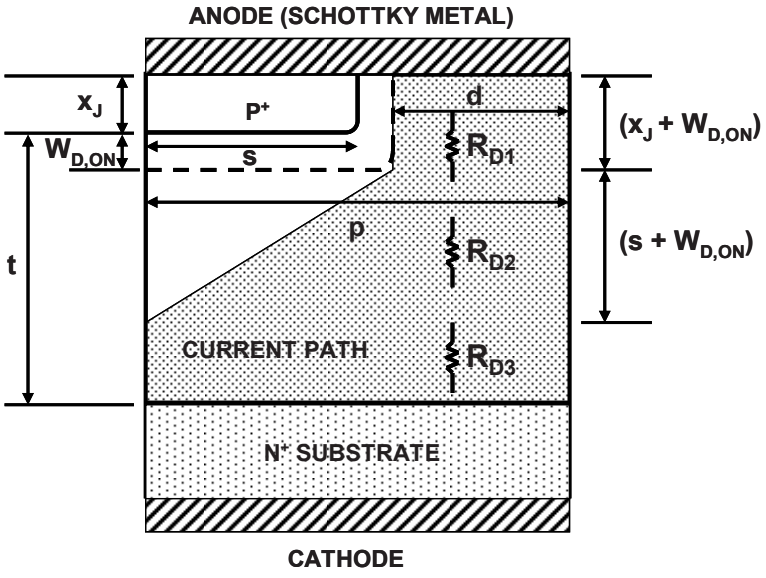

Fig. 3.9 Current Flow Pattern in the Silicon Carbide JBS Rectifier Structure during Operation in the On-State.

through the Schottky contact flows only within the un-depleted portion (with dimension 'd') of the drift region at the top surface. Consequently, the current density at the Schottky contact (J_{FS}) is related to the cell (or cathode) current density (J_{FC}) by:

$$J_{FS} = \left(\frac{p}{d}\right) J_{FC} \qquad \textbf{[3.25]}$$

where p is the cell pitch. The dimension 'd' is determined by the cell pitch (p), the size of the ion-implant window (s), and the depletion width ($W_{D,ON}$):

$$d = p - s - W_{D,ON} \qquad \textbf{[3.26]}$$

In deriving this equation, it has been assumed that there is no straggle in the ion-implant. Depending up on the lithography used for device fabrication to minimize the size (dimension 's') of the P^+ region, the current density at the Schottky contact can be enhanced by a factor of two or more. This must be taken into account when computing the voltage drop across the Schottky contact:

$$V_{FS} = \phi_B + \frac{kT}{q} \ln\left(\frac{J_{FS}}{AT^2}\right) \qquad \textbf{[3.27]}$$

After flowing across the Schottky contact, the current flows through the un-depleted portion of the drift region. In the model, it is assumed that the current flows through a region with a uniform width 'd' until it reaches the bottom of the depletion region and then spreads to the entire cell pitch (p) at a 45 degree spreading angle. The current paths overlap at a distance (s + $W_{D,ON}$) from the bottom of the depletion region. The current then flows through a uniform cross-sectional area.

The net resistance to current flow can be calculated by adding the resistance of the three segments. The resistance of the first segment of uniform width 'd' is given by:

$$R_{D1} = \frac{\rho_D . \left(x_J + W_{D,ON}\right)}{d.Z} \qquad \textbf{[3.28]}$$

The resistance of the second segment can be derived by using the same approach used for Model C for the silicon JBS rectifier:

$$R_{D2} = \frac{\rho_D}{Z} \ln\left(\frac{p}{d}\right) \qquad \textbf{[3.29]}$$

The resistance of the third segment with a uniform cross-section of width p is given by:

$$R_{D3} = \frac{\rho_D.(t - s - 2W_{D,ON})}{p.Z} \quad \textbf{[3.30]}$$

The specific resistance for the drift region can be calculated by multiplying the cell resistance ($R_{D1} + R_{D2} + R_{D3}$) by the cell-area (p.Z):

$$R_{sp,drift} = \frac{\rho_D.p.(x_J + W_{D,ON})}{d} + \rho_D.p.\ln\left(\frac{p}{d}\right) + \rho_D.(t - s - 2W_{D,ON}) \quad \textbf{[3.31]}$$

In addition, it is important to include the resistance associated with the thick, highly doped N^+ substrate because this is substantially larger than for silicon devices. The specific resistance of the N^+ substrate can be determined by taking the product of its resistivity and thickness. For 4H-SiC, the lowest available resistivity for N^+ substrates is 20 mΩ-cm. If the thickness of the substrate is 200 microns, the specific resistance contributed by the N^+ substrate is 4 x 10^{-4} Ω-cm^2. The on-state voltage drop for the JBS rectifier at a forward cell current density J_{FC}, including the substrate contribution, is then given by:

$$V_F = \phi_B + \frac{kT}{q}\ln\left(\frac{J_{FS}}{AT^2}\right) + (R_{sp,drift} + R_{sp,subs}).J_{FC} \quad \textbf{[3.32]}$$

The depletion layer width for silicon carbide is also substantially larger than for silicon due to the larger built-in potential. However, these structures operate at a relatively larger on-state voltage drop of around 1 volt. Consequently, when computing the on-state voltage drop using the above equation, it is satisfactory to make the approximation that the depletion layer width can be computed by subtracting an on-state voltage drop of 1 volt from a built-in potential of about 3.2 volts for the P-N junction:

$$W_{D,ON} = \sqrt{\frac{2\varepsilon_S(V_{bi} - 1.0)}{qN_D}} \quad \textbf{[3.33]}$$

where V_{bi} is the built-in potential of the P-N junction. Due to the abrupt junctions formed in silicon carbide by the ion implant process, it is appropriate to assume that the entire depletion occurs on the lightly doped N-side of the junction. For a 4H-SiC JBS rectifier fabricated using a doping concentration of 1 x 10^{16} cm^{-3}, corresponding to a breakdown voltage of about 3000 V, the zero bias depletion width is about 0.5 microns. Based upon this, it can be concluded that it is even more important to take the depletion width into account for silicon carbide JBS rectifiers.

The forward characteristics of 3kV JBS rectifiers, calculated using the above analytical model with a Schottky barrier height of 0.8 eV, are shown in Fig. 3.10 with the cell pitch (p) as a parameter. The width of the P^+ region (2s) was kept at 1.0 microns for this analysis because the small diameters for the silicon

carbide wafers preclude the use of smaller geometries. A junction depth of 0.5 microns was used with a drift region thickness of 20 microns below the junction to support the 3000 volts. In comparison with the Schottky rectifier characteristics (shown by the dashed line in the figure), the increase in on-state voltage drop at a forward current density of 100 A/cm^2 is small (less than 0.1 volts) as long as the cell pitch is more than 1.1 microns. This cell pitch is sufficient to obtain substantial reduction of the electric field at the metal-semiconductor contact as shown later in the chapter.

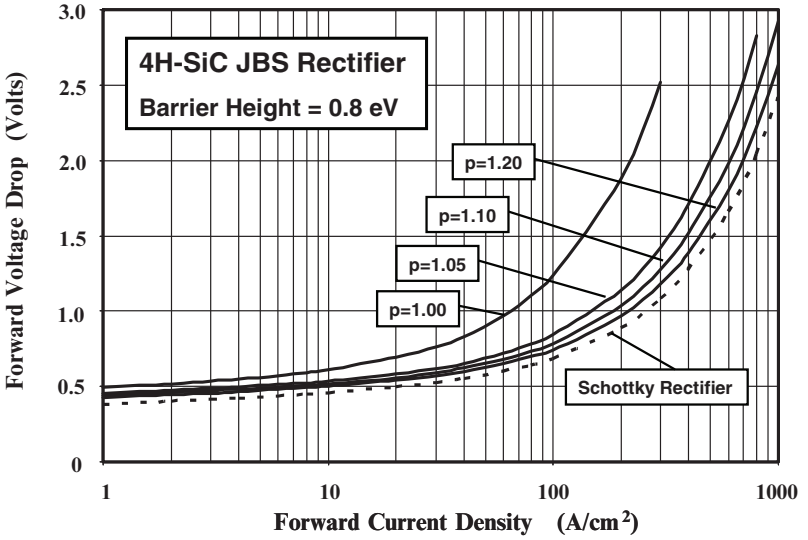

Fig. 3.10 Forward Characteristics of 3kV 4H-SiC JBS Rectifiers.

Simulation Example

In order to validate the above model for the on-state characteristics of the silicon carbide JBS rectifier, the results of two-dimensional numerical simulations on a 3000 V structure are described here. The structure had a drift region thickness of 20 microns with a doping concentration of 1 x 10^{16} cm^{-3}. The P^+ region had a depth of 0.5 microns with an ion-implant window (dimension s in Fig. 3.9) of 0.5 microns. No lateral diffusion was assumed to occur for the implanted region.

The forward *i-v* characteristics of a 3000 V JBS 4H-SiC rectifier obtained from the numerical simulations are shown in Fig. 3.6E for the case of a cell pitch of 1.25 microns and contact with work-function of 4.5 eV. This corresponds to a Schottky barrier height of about 0.8 eV based upon an electron affinity of 3.7 eV for 4H-SiC. The on-state voltage drop at a current density of 100 A/cm^2 is 0.7 volts which is similar to the results obtained using the analytical model in the previous section providing validation for the model. It is worth pointing out that the diode exhibits the desirable positive temperature coefficient for the on-state voltage drop with no kinks in the characteristics.

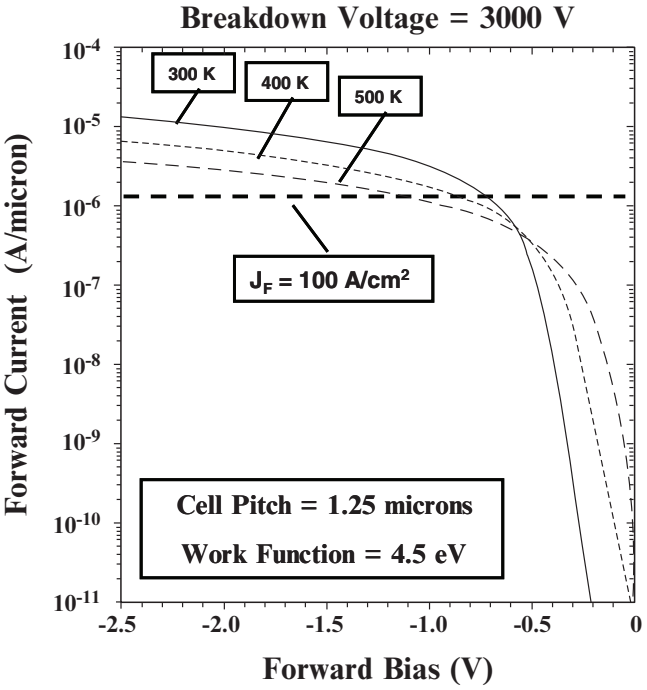

Fig. 3.6E Forward Characteristics of 3 kV 4H-SiC JBS Rectifier.

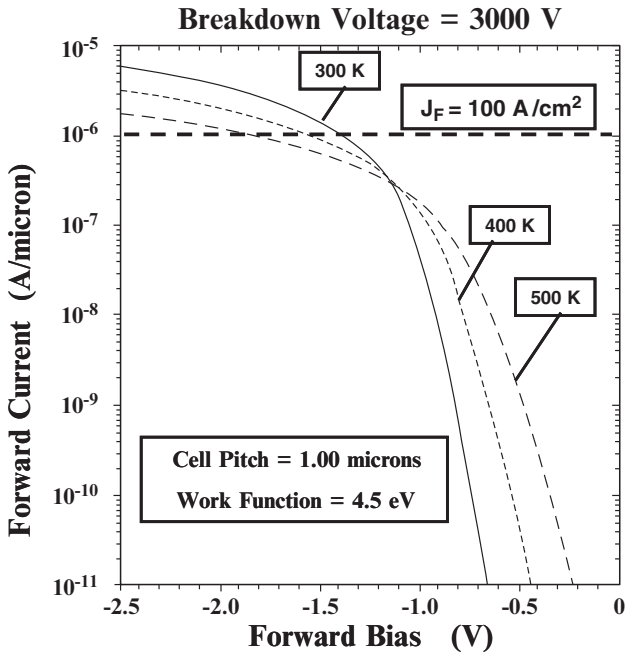

Fig. 3.7E Forward Characteristics of 3 kV 4H-SiC JBS Rectifier.

However, the forward characteristics were found to degrade substantially as shown in Fig. 3.7E, when the cell pitch was reduced to 1.0 microns, as predicted by the analytical model. The on-state voltage drop increases by 0.7 volts when the cell pitch is reduced, which is also consistent with the analytical model. The reason for the increase in the on-state voltage drop is the much greater constriction of the current at the Schottky contact for the smaller cell pitch because the dimension 'd' is reduced to only 0.014 microns for the pitch of 1.00 microns. It will be shown later in this chapter that a cell pitch of 1.2 microns is adequate to suppress the electric field at the Schottky contact.

3.3 JBS Rectifier Structure: Reverse Leakage Model

The reverse leakage current in the JBS rectifier is reduced when compared with the Schottky rectifier due to the smaller electric field at the metal-semiconductor interface. In addition, the area of the Schottky contact is a fraction of the total cell area resulting in a smaller reverse current contribution. In the case of the silicon JBS rectifier, the reduced electric field at the Schottky contact suppresses the barrier lowering effect. In the case of the silicon carbide JBS rectifier, the reduced electric field not only decreases the barrier lowering but also mitigates the influence of thermionic field emission. The impact of the reduction of the electric field at the Schottky contact in the JBS rectifier structure on the leakage current is analyzed in this section. The presence of the P-N junction also diverts the avalanche multiplication current from the Schottky contact reducing the pre-breakdown multiplication effect.

3.3.1 Silicon JBS Rectifier: Reverse Leakage Model

In the case of the JBS rectifier, the leakage current model must take into account the smaller Schottky contact area within the cell and the influence of the smaller electric field generated at the Schottky contact due to the shielding from the P-N junction. The leakage current for the silicon JBS rectifier is therefore given by:

$$J_L = \left(\frac{p - s - x_J}{p} \right) A T^2 \exp\left(- \frac{q\phi_b}{kT} \right) . \exp\left(\frac{q\beta \Delta\phi_{bJBS}}{kT} \right) \qquad \textbf{[3.34]}$$

where β is a constant to account for the smaller barrier lowering closer to the P-N junction as discussed below. In the previous chapter on Schottky rectifiers, it was demonstrated that the high electric field at the Schottky contact produces a reduction of the effective barrier height due to the image force lowering phenomenon. In contrast with the Schottky rectifier, the barrier lowering for the JBS rectifier is determined by the reduced electric field E_{JBS} at the contact:

$$\Delta\phi_{bJBS} = \sqrt{\frac{qE_{JBS}}{4\pi\varepsilon_S}} \qquad \textbf{[3.35]}$$

The electric field at the Schottky contact varies with distance away from the P-N junction. The highest electric field is observed at the middle of the Schottky contact with a progressively smaller value closer to the P-N junction. In an analytical model with a worst case scenario, it is prudent to use the electric field at the middle of the contact to compute the leakage current. Until the depletion regions from the adjacent P-N junctions produce a potential barrier under the Schottky contact, the electric field at the metal-semiconductor interface in the middle of the contact increases with the applied reverse bias voltage as in the case of the Schottky rectifier. A potential barrier is established by the P-N junctions after depletion of the drift region below the Schottky contact. The voltage at which the depletion regions from the adjacent junctions intersect under the Schottky contact is referred to as the *pinch-off voltage*. The pinch-off voltage (V_P) can be obtained from the device cell parameters:

$$V_P = \frac{qN_D}{2\varepsilon_S}\left(p - s - x_J\right)^2 - V_{bi} \qquad \textbf{[3.36]}$$

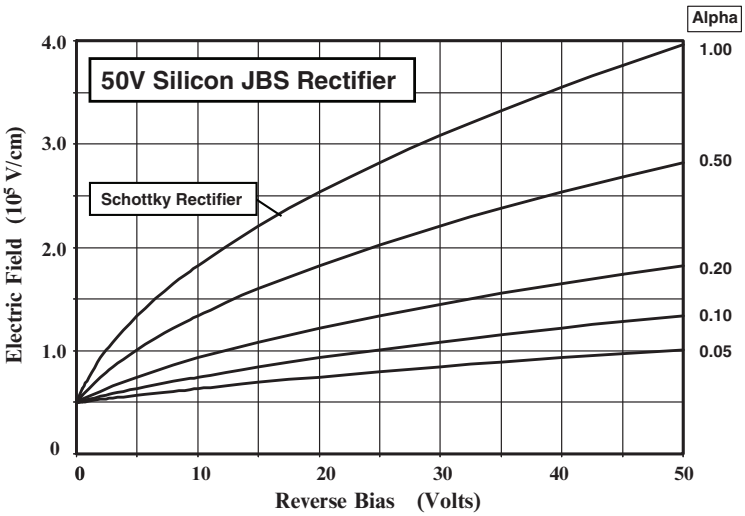

Fig. 3.11 Electric Field at the Schottky Contact for 50 V Silicon JBS Rectifiers.

Although a potential barrier begins to form after the reverse bias exceeds the pinch-off voltage, the electric field continues to rise at the Schottky contact due to encroachment of the potential to the Schottky contact. This problem is more acute for the silicon JBS rectifier because of the open shape of the planar junction. In order to analyze the impact of this on the reverse leakage current, the electric field E_{JBS} can be related to the reverse bias voltage by:

$$E_{JBS} = \sqrt{\frac{2qN_D}{\varepsilon_S}(\alpha V_R + V_C)} \qquad \textbf{[3.37]}$$

where α is a coefficient used to account for the build up in the electric field after pinch-off and V_C is the Schottky contact potential.

As an example, consider the case of the 50 volt silicon JBS rectifier discussed earlier in the chapter with a cell pitch (p) of 1.25 microns and a P^+ region with dimension 's' of 0.25 microns. The pinch-off voltage for this structure is only 1 volt for a drift region with doping concentration of 1×10^{16} cm^{-3}. Due to the two-dimensional nature of the planar P-N junction in the silicon JBS rectifier structure, it is difficult to derive an analytical expression for alpha. However, the reduction of the electric field at the Schottky contact can be predicted by assuming various values for alpha in Eq. [3.37]. The results are shown in Fig. 3.11 for alpha values ranging between 0.05 and 1.00. An alpha of unity corresponds to the Schottky rectifier structure with no shielding. It can be observed that substantial reduction of the electric field at the Schottky contact is obtained as alpha is reduced.

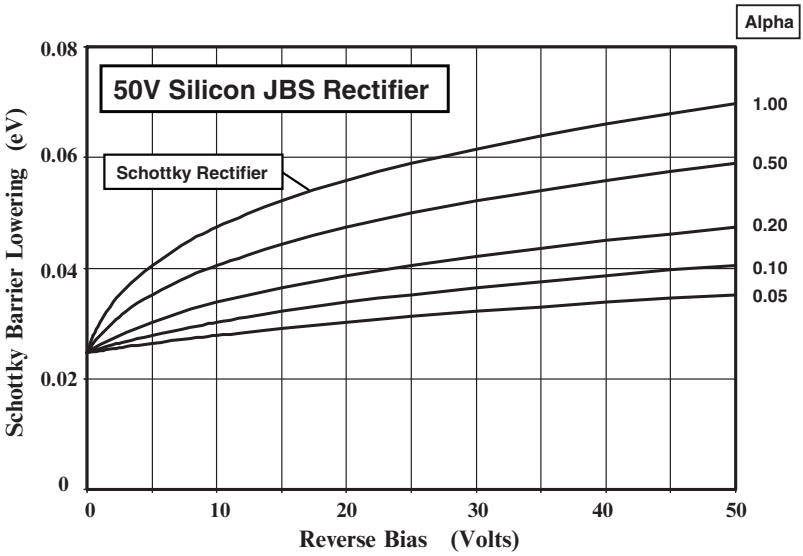

Fig. 3.12 Schottky Barrier Lowering in 50 V Silicon JBS Rectifiers with various Alpha Coefficients.

The impact of the reduction of the electric field at the Schottky contact on the Schottky barrier lowering is shown in Fig. 3.12. Without the shielding by the P-N junction, a barrier lowering of 0.07 eV occurs in the Schottky rectifier. The barrier lowering is reduced to 0.05 eV with an alpha of 0.2 in the JBS rectifier structure. Although this may appear to be a small change, it has a large impact on the reverse leakage current as shown in Fig. 3.13. For these plots, a value of 0.7 was assumed for the constant β based upon the results of the numerical simulations discussed below. For the JBS structure with pitch of 1.25 microns, an implant window (2s) of 0.5 microns, and junction depth of 0.5 microns, the Schottky contact area is reduced to only 40 percent of the cell area. This results in a

proportionate reduction of leakage current at low reverse bias voltages. The suppression of the Schottky barrier lowering and pre-breakdown multiplication, by the presence of the P-N junction, reduces the rate of increase in leakage current with increasing reverse bias. The net effect is a reduction in leakage current density by a factor of 35x when the reverse bias reaches 50 volts for the case of an alpha of 0.5. This demonstrates that a very large improvement in reverse power dissipation can be achieved with the JBS rectifier structure.

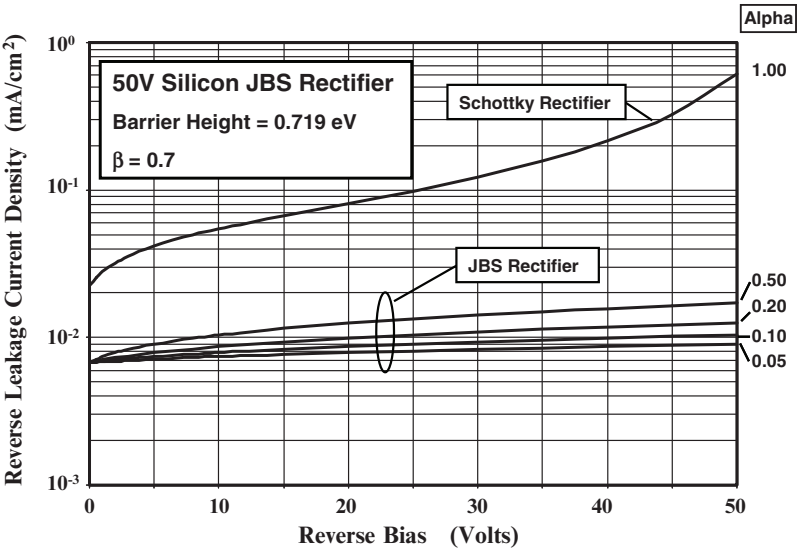

Fig. 3.13 Reverse Leakage Current for 50 V Silicon JBS Rectifiers with various Alpha coefficients.

Simulation Example

In order to validate the above model for the reverse characteristics of the silicon JBS rectifier, the results of two-dimensional numerical simulations on a 50 V structure are described here. The structure had a drift region with a doping concentration of 8 x 10^{15} cm^{-3} and a thickness of 3 microns. The P^+ region had a depth of 0.5 microns with an ion-implant window (dimension s in Fig. 3.5) of 0.25 microns. The work function of the Schottky metal was chosen to obtain a barrier height of 0.65 eV.

A three dimensional view of the electric field distribution in the JBS rectifier cell is shown in Fig. 3.8E. The Schottky contact is located on the lower right-hand-side in the figure with the P^+ region located at the top of the figure. A high electric field (4 x 10^5 V/cm) is observed at the P-N junction. However, the electric field at the middle of the Schottky contact is greatly reduced (2.45 x 10^5 V/cm). It can also be seen that the electric field becomes smaller when proceeding towards the P-N junction. Consequently, a worst case analysis of the leakage current can be performed by using the electric field at the middle of the Schottky contact.

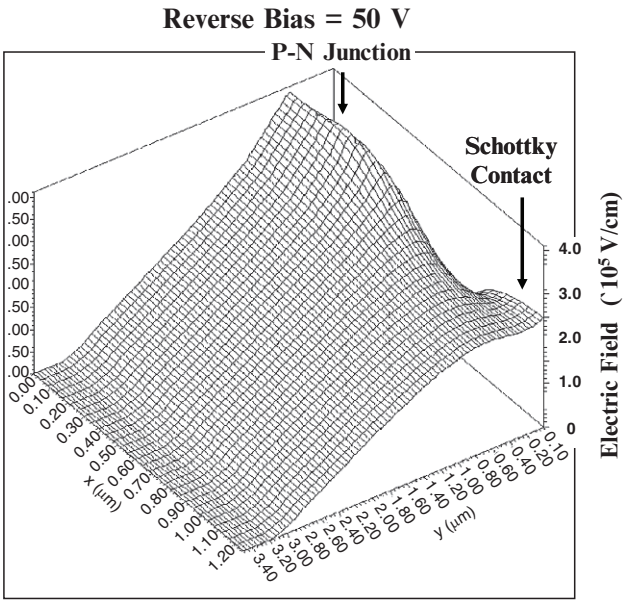

Fig. 3.8E Electric Field Distribution in a 50 V Silicon JBS Rectifier.

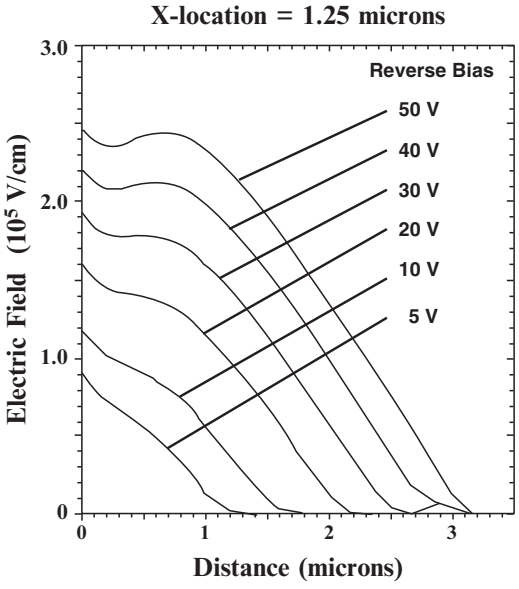

Fig. 3.9E Growth of the Electric Field at the Middle of the Schottky Contact in a 50 V Silicon JBS Rectifier.

The increase in the electric field at the middle of the Schottky contact in the JBS rectifier structure with cell pitch of 1.25 microns is shown in Fig. 3.9E. To contrast this behavior with the Schottky diode, the growth of the electric field for

the Schottky rectifier is shown in Fig. 3.10E. From these figures, it is apparent that the electric field at the Schottky contact is suppressed in the JBS rectifier due to the incorporation of the P-N junction. An even greater suppression of the electric field at the Schottky contact can be obtained by reducing the cell pitch as shown in Fig. 3.11E for a structure with pitch of 1.00 microns.

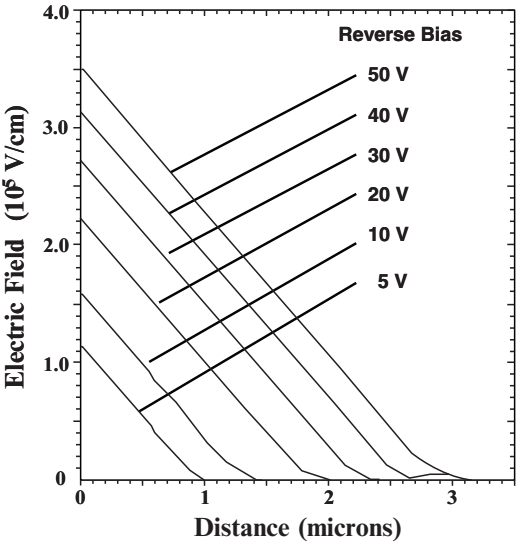

Fig. 3.10E Growth of the Electric Field in a 50 V Silicon Schottky Rectifier.

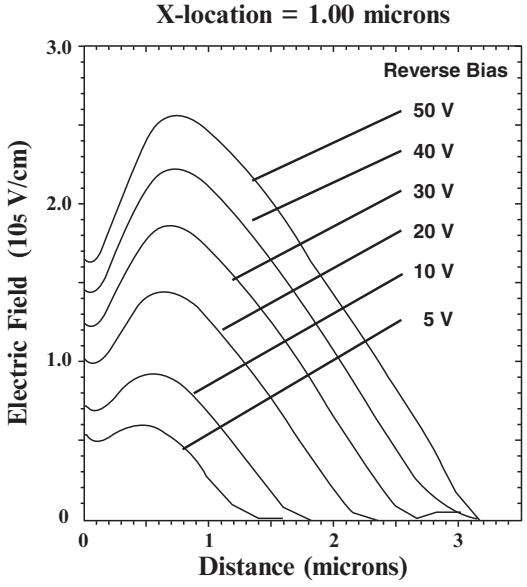

Fig. 3.11E Growth of the Electric Field at the Middle of the Schottky Contact in a 50 V Silicon JBS Rectifier.

The coefficient alpha, that governs the rate at which the electric field increases at the middle of the Schottky contact in the analytical model for the JBS rectifier structure, can be extracted from the results of the two-dimensional numerical simulations. The increase in the electric field at the middle of the Schottky contact, obtained from the numerical simulations, is shown in Fig. 3.12E for the JBS rectifiers with cell pitch (p) of 1.25 and 1.00 microns by the symbols. The results of calculations based upon using the analytical equation [3.37] are shown by the solid lines with the values fro alpha adjusted to fit the results of the numerical simulations. The case with alpha of unity fits the Schottky rectifier quite well as expected. The value for alpha for the JBS rectifier with pitch of 1.25 microns is found to be 0.45 while that for a pitch of 1.00 microns is 0.18. With these values of alpha, the analytical model accurately predicts the behavior of the electric field at the middle of the Schottky contact. It can therefore be used to compute the Schottky barrier lowering and leakage current in JBS rectifiers.

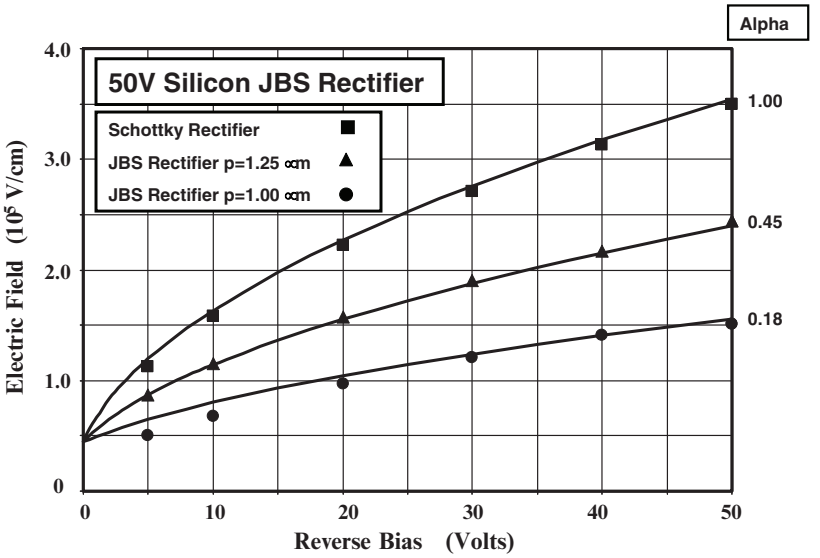

Fig. 3.12E Growth of the Electric Field at the Middle of the Schottky Contact for Silicon 50V JBS Rectifiers.

The reverse *i-v* characteristics of the 50 V Silicon JBS rectifier with a cell pitch of 1.25 microns obtained from the numerical simulations are shown in Fig. 3.13E together with those for the Schottky rectifier for comparison. Both devices had a cross-sectional width of 1.25 microns with a depth of 1 micron. The breakdown voltage for the JBS rectifier cell is observed to be 64 volts. This is consistent with an edge termination limited breakdown voltage of 50 volts at 80 percent of the parallel-plane breakdown voltage. The leakage current at small reverse bias voltages is 2.5x times smaller in the JBS rectifier structure. This is consistent with the reduction of the Schottky contact area by a factor of 2.5x in this JBS rectifier structure. The leakage current for the Schottky rectifier increases by a factor of 100x when the reverse voltage increases to 60 volts. In contrast, the reverse leakage current for this JBS rectifier increases by a factor of only 4x when the reverse voltage is

increased to 60 volts. This increase is consistent with predictions of the analytical model. Based upon the simulation results, the leakage current for the JBS rectifier with pitch of 1.25 microns is 75x smaller than for the Schottky rectifier at a reverse bias of 60 volts.

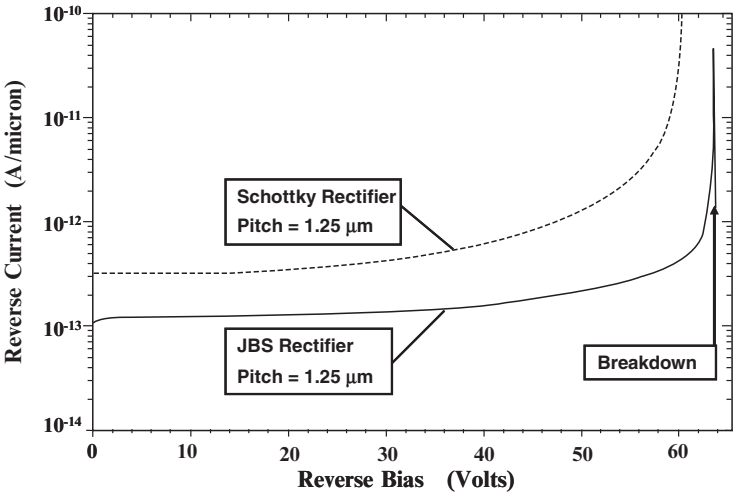

Fig. 3.13E Reverse Blocking Characteristics for a Silicon 50V JBS Rectifier.

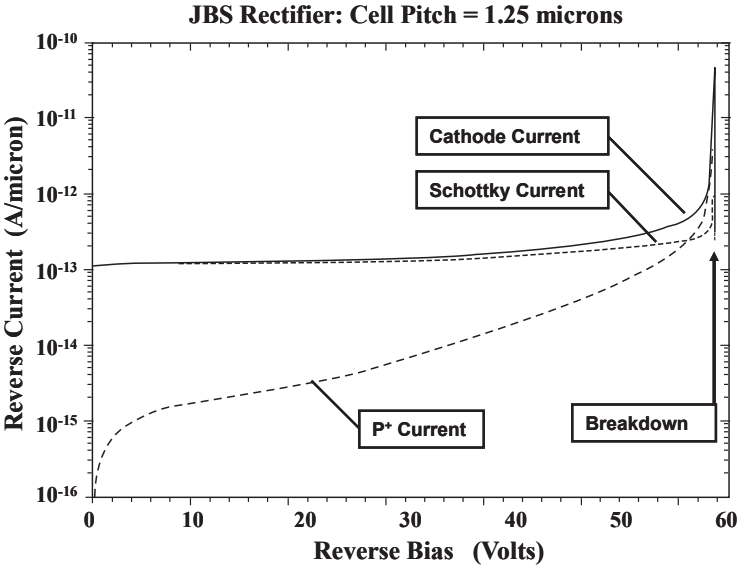

Fig. 3.14E Reverse Blocking Characteristics for a Silicon 50V JBS Rectifier.

The numerical simulations provide insight into the current flow within the JBS rectifier structure during the reverse blocking mode. The total reverse current flowing through the cathode electrode is compared with the currents flowing

through the Schottky contact and the contact to the P^+ region in Fig. 3.14E. At reverse bias voltages below 50 volts, the cathode current is essentially equal to the current flowing through the Schottky contact. The current flowing through the contact to the P^+ region increases rapidly when the reverse voltage exceeds 30 volts and becomes comparable to the current in the Schottky contact at reverse bias voltages above 55 volts. It is worth pointing out that the breakdown occurs due to a very rapid increase in the current flowing through the contact to the P^+ region indicating that the avalanche multiplication occurs below the P^+ region due to the much larger local electric field as shown in Fig. 3.8E. This shields the Schottky contact against damage if the JBS rectifier is forced into breakdown during circuit operation.

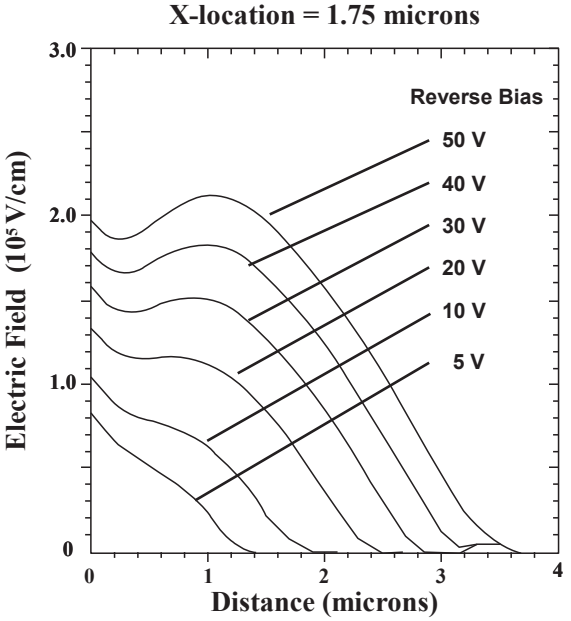

Fig. 3.15E Growth of the Electric Field at the Middle of the Schottky Contact in a 50 V Silicon JBS Rectifier.

The shielding of the Schottky contact in the JBS rectifier structure can be enhanced by using a larger junction depth. In order to illustrate this, the case of increasing the junction depth to 1.00 microns is considered here. For comparison purposes, the size of the Schottky contact for this structure was chosen to be equal to that for the JBS rectifier structure with a pitch of 1.25 microns and junction depth of 0.5 microns. The electric field profile for the structure with junction depth of 1.00 microns is shown in Fig. 3.15E for various reverse bias voltages. By comparison with the electric field profiles in Fig. 3.9E for the structure with junction depth of 0.5 microns, it can be observed that the electric field at the middle of the Schottky contact has been reduced. This indicates that the value for alpha has been reduced by the larger junction depth.

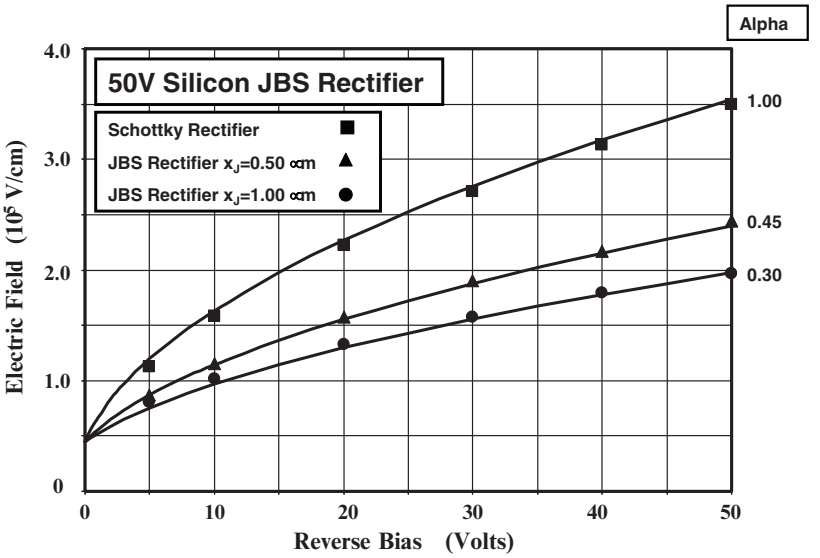

Fig. 3.16E Growth of the Electric Field at the Middle of the Schottky Contact for Silicon 50V JBS Rectifiers.

The growth of the electric field with reverse bias voltage for the JBS rectifier structures with the different junction depths is compared in Fig. 3.16E. In this figure, the value for alpha in the analytical model was adjusted to match the simulation data. It can be seen that the alpha is reduced from 0.45 to 0.3 with the larger junction depth due to the larger aspect ratio. This is beneficial for suppressing the Schottky barrier lowering and decreasing the leakage current. A deeper junction can also be utilized for the edge termination to enhance the breakdown voltage.

3.3.2 Silicon Carbide JBS Rectifier: Reverse Leakage Model

The leakage current in the silicon carbide JBS rectifier can be calculated using the same approach as for the silicon JBS rectifier structure. Firstly, it is important to account for the smaller Schottky contact area in the JBS rectifier cell. Secondly, it is necessary to include Schottky barrier lowering while accounting for the smaller electric field at the Schottky contact due to shielding by the P-N junction. Third, the thermionic field emission current must be included while accounting for the smaller electric field at the Schottky contact due to shielding by the P-N junction. After making these adjustments, the leakage current for the silicon carbide JBS rectifier can be calculated by using:

$$J_L = \left(\frac{p-s}{p}\right) A T^2 \exp\left(-\frac{q\phi_b}{kT}\right).\exp\left(\frac{q\Delta\phi_{bJBS}}{kT}\right).\exp\left(C_T E_{JBS}^2\right) \qquad \textbf{[3.38]}$$

where C_T is a tunneling coefficient (8 x 10^{-13} cm^2/V^2 for 4H-SiC). In contrast to the Schottky rectifier, the barrier lowering for the JBS rectifier is determined by the reduced electric field E_{JBS} at the contact:

$$\Delta\phi_{bJBS} = \sqrt{\frac{qE_{JBS}}{4\pi\varepsilon_S}} \qquad \textbf{[3.39]}$$

As in the case of the silicon JBS structure, the electric field at the Schottky contact varies with distance away from the P-N junction. The highest electric field is observed at the middle of the Schottky contact with a progressively smaller value closer to the P-N junction. When developing an analytical model with a worst case scenario, it is prudent to use the electric field at the middle of the contact to compute the leakage current.

Until the depletion regions from the adjacent P-N junctions produce a potential barrier under the Schottky contact, the electric field at the metal-semiconductor interface in the middle of the contact increases with the applied reverse bias voltage as in the case of the Schottky rectifier. A potential barrier is established by the P-N junctions after depletion of the drift region below the Schottky contact. As in the case of the silicon JBS rectifier structure, the pinch-off voltage (V_P) can be obtained from the device cell parameters:

$$V_P = \frac{qN_D}{2\varepsilon_S}(p-s)^2 - V_{bi} \qquad \textbf{[3.40]}$$

It is worth pointing out that the built-in potential for 4H-SiC is much larger than for silicon. Although the potential barrier begins to form after the reverse bias exceeds the pinch-off voltage, the electric field continues to rise at the Schottky contact due to encroachment of the potential to the Schottky contact. This problem is less acute for the silicon carbide structure than in the silicon JBS rectifier because of the rectangular shape of the P-N junction resulting from the very low diffusion coefficients for dopants in 4H-SiC. In order to analyze the impact of this on the reverse leakage current, the electric field E_{JBS} can be related to the reverse bias voltage by:

$$E_{JBS} = \sqrt{\frac{2qN_D}{\varepsilon_S}(\alpha V_R + V_{bi})} \qquad \textbf{[3.41]}$$

where α is a coefficient used to account for the build up in the electric field after pinch-off.

As an example, consider the case of the 3kV silicon carbide JBS rectifier discussed earlier in the chapter with a cell pitch (p) of 1.25 microns and a P^+ region with dimension ‘s’ of 0.5 microns. The pinch-off voltage for this structure is only 2 volts for a drift region with doping concentration of 1 x 10^{16} cm^{-3}. Due to the two-dimensional nature of the P-N junction in the JBS rectifier structure, it is difficult to derive an analytical expression for alpha. However, the reduction of the electric

field at the Schottky contact can be predicted by assuming various values for alpha in Eq. [3.41]. The results are shown in Fig. 3.14 for alpha values ranging between 0.05 and 1.00. An alpha of unity corresponds to the Schottky rectifier structure with no shielding. It can be observed that substantial reduction of the electric field at the Schottky contact is obtained as alpha is reduced.

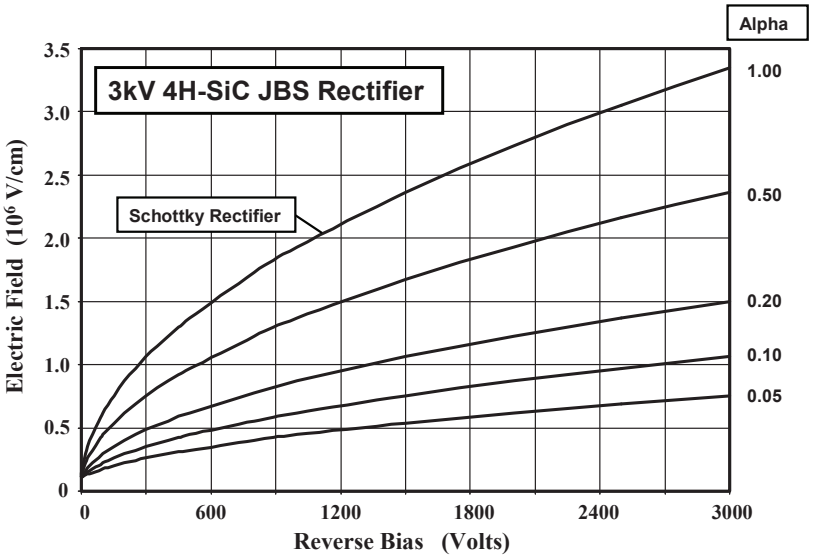

Fig. 3.14 Electric Field at the Schottky Contact for 3 kV Silicon Carbide JBS Rectifiers.

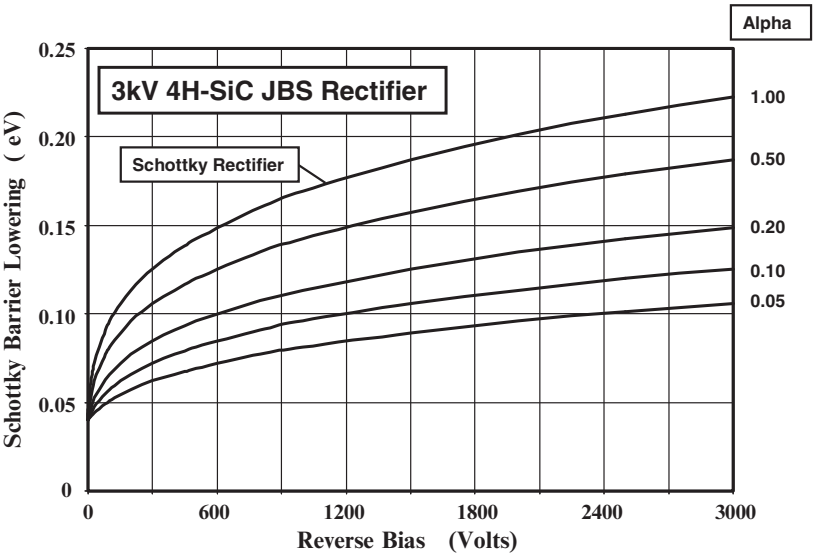

Fig. 3.15 Schottky Barrier Lowering in 3 kV Silicon Carbide JBS Rectifiers with various Alpha Coefficients.

The impact of the reduction of the electric field at the Schottky contact, due to the shielding by the P-N junction in the JBS structure, on the Schottky barrier lowering is shown in Fig. 3.15. Without the shielding by the P-N junction, a barrier lowering of 0.22 eV occurs in the Schottky rectifier. This is much greater than for silicon devices due to the larger electric field at the contact. The barrier lowering is reduced to 0.15 eV with an alpha of 0.2 in the 4H-SiC JBS rectifier structure. These smaller values for alpha are appropriate for the silicon carbide structure because the rectangular shape of the P-N junction favors a stronger shielding of the Schottky contact.

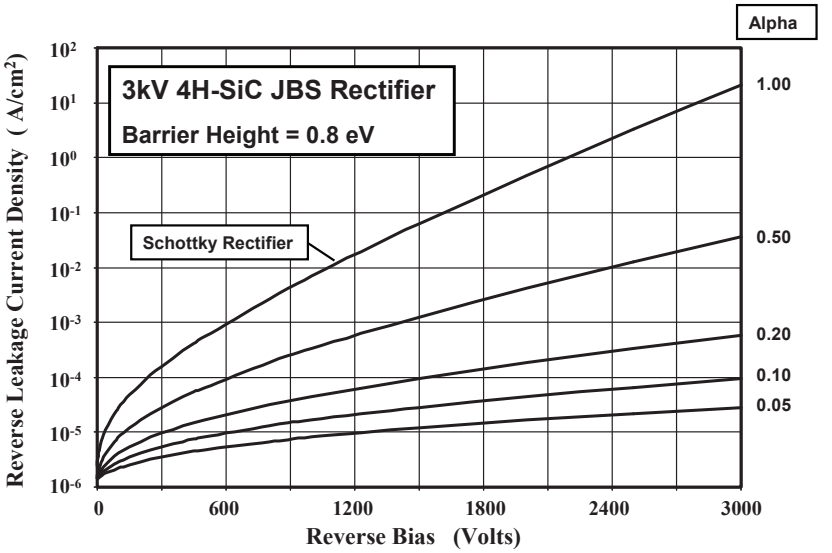

Fig. 3.16 Reverse Leakage Current for 3 kV Silicon Carbide JBS Rectifiers with various Alpha coefficients.

As discussed in Chapter 4, the larger barrier lowering for silicon carbide, in conjunction with the thermionic field emission current, results in an increase in leakage current by six-orders of magnitude when the voltage increases to 2500 volts for the 3 kV Schottky rectifier. This is reproduced in Fig. 3.16, as the plot with alpha of unity by using a barrier height of 0.8 eV. It can be seen that the leakage current is greatly reduced by the shielding in the JBS rectifier structure. For the 4H-SiC JBS rectifier structure with pitch of 1.25 microns, an implant window (s) of 0.5 microns, and junction depth of 0.5 microns, the Schottky contact area is reduced to 60 percent of the cell area. This results in a proportionate reduction of leakage current at low reverse bias voltages. More importantly, the suppression of the electric field at the Schottky contact, by the presence of the P-N junction, greatly reduces the rate of increase in leakage current with increasing reverse bias. The net effect is a reduction in leakage current density by a factor of 570x when the reverse bias reaches 3 kV for the case of an alpha of 0.5 and a factor of 36,000x for an alpha of 0.2. This demonstrates that a very large

improvement in reverse power dissipation can be achieved with the 4H-SiC JBS rectifier structure with a modest increase in the on-state voltage drop.

However, the leakage current density observed with a Schottky barrier height of 0.8 eV leads to a power dissipation of 100 W/cm^2 at a reverse bias of 3000 volts for a JBS rectifier with alpha of 0.5 even at 300 ^{o}K. The power dissipation in the reverse blocking mode can be reduced by increasing the Schottky barrier height. As an example, if the barrier height is increased from 0.8 to 1.1 eV, the leakage current is reduced by 5-orders of magnitude as shown in Fig. 3.17. This is adequate to reduce the power dissipation in the reverse blocking mode to below that in the forward conduction mode even at elevated temperatures ensuring stable operation of the rectifier. This change in barrier height will increase the on-state voltage drop by 0.3 volts by shifting the *i-v* characteristics, shown earlier in Fig. 3.10, to larger voltages. The on-state voltage drop for the 4H-SiC JBS rectifiers with a barrier height of 1.1 eV is only 1 volt, which is a very good value for a rectifier designed to support 3000 volts.

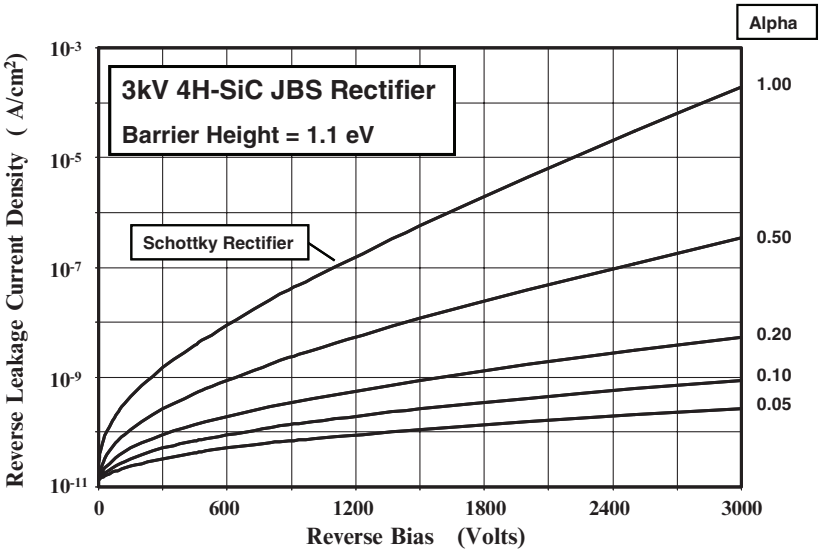

Fig. 3.17 Reverse Leakage Current for 3 kV Silicon Carbide JBS Rectifiers with various Alpha coefficients.

Simulation Example

In order to validate the model for the reverse blocking characteristics for the silicon carbide JBS rectifier structure, a structure with breakdown voltage of 3000 volts, using a drift region with doping concentration of 1 x 10^{16} cm^{-3} and thickness of 20 microns, will be considered here. The two-dimensional numerical simulations were performed with various spacing between the P$^+$ regions by varying the pitch (p) while maintaining an implant window (2s) of 1 micron. The depth of the P$^+$ region was also varied to examine its impact on the electric field reduction at the Schottky contact.

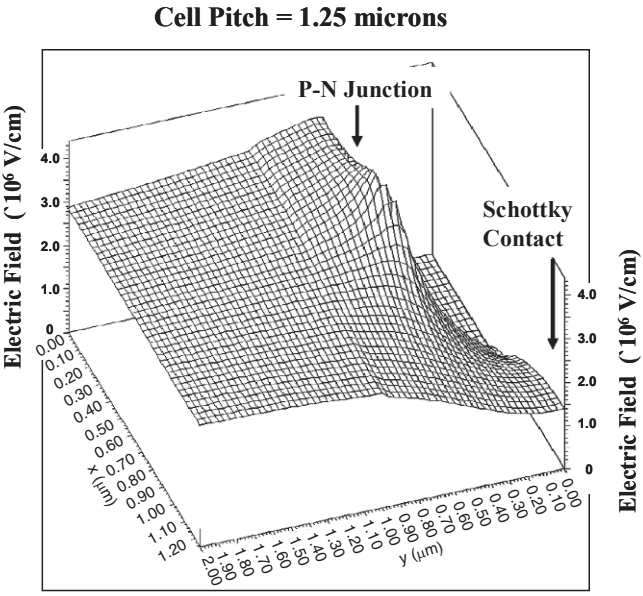

Fig. 3.17E Electric Field distribution in a 3 kV 4H-SiC JBS Rectifier.

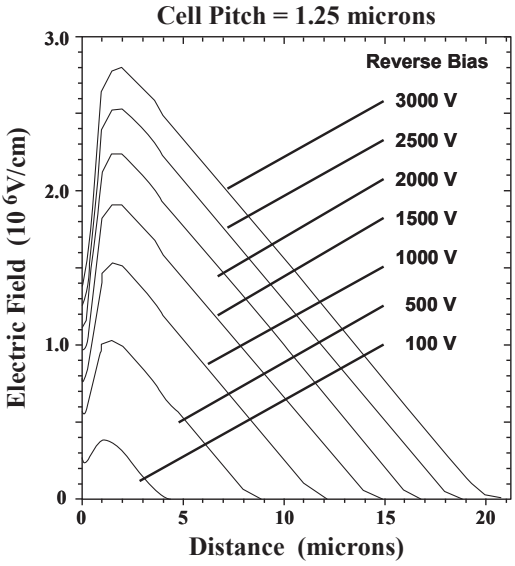

Fig. 3.18E Electric Field variation with Reverse Voltage in a 3000 V 4H-SiC JBS Rectifier.

A three-dimensional view of the electric field distribution in a 3000 volt 4H-SiC JBS rectifier structure with cell pitch of 1.25 microns is shown in Fig. 3.17E at a reverse bias of 3000 volts (just prior to breakdown). It can be seen that the highest electric field occurs at the P/N junction and that the electric field is suppressed at the Schottky contact. It is worth pointing out that the maximum

electric field at the Schottky contact occurs at the location furthest away from the P-N junction (at x = 1.25 microns for the structure in Fig. 3.17E). Consequently, the largest leakage due to barrier lowering and tunneling components will occur at this location. For this reason, the highest electric field at the Schottky contact will be used to analyze the reverse leakage characteristics for the 4H-SiC JBS rectifiers.

The electric field profile at the center of the Schottky contact is shown in Fig. 3.18E for the case of a cell pitch of 1.25 microns. It can be observed that the electric field at the surface under the contact is significantly reduced when compared the peak electric field in the bulk. The peak of the electric field occurs at a depth of about 2 microns. At a reverse bias of 3000 volts, the electric field at the Schottky contact is only 1.4 x 10^6 V/cm compared with 2.8 x 10^6 V/cm at the electric field maxima which occurs in the bulk at a depth of 1.5 microns.

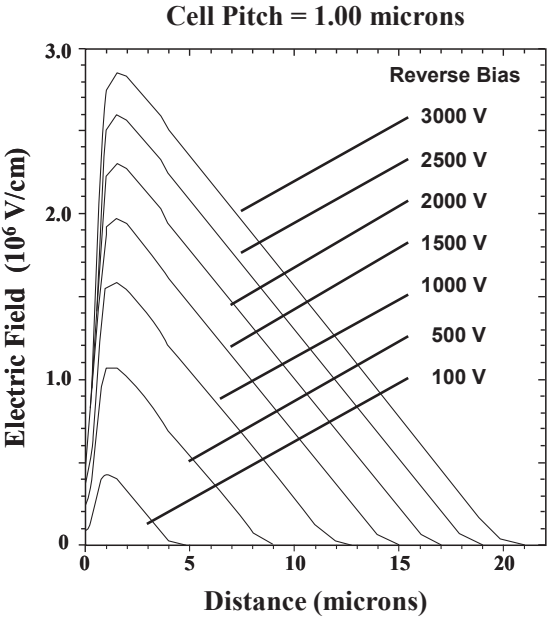

Fig. 3.19E Electric Field variation with Reverse Voltage in a 4H-SiC JBS Rectifier.

An even greater reduction of the electric field at the Schottky contact can be achieved by reducing the cell pitch while maintaining the same size for the window used to form the P^+ region. This is illustrated in Fig. 3.19E for the case of a cell pitch of 1.00 microns. Here, the electric field at the Schottky contact is only 7 x 10^5 V/cm compared with 2.8 x 10^6 V/cm at the maxima when the reverse bias voltage reaches 3000 volts. The larger reduction of the electric field at the Schottky contact occurs due to the depletion of the space between the P^+ regions at a smaller reverse bias voltage and the formation of a larger potential barrier under contact due to the larger channel aspect ratio. The larger potential barrier suppresses an increase in the electric field at the Schottky contact with increasing reverse bias voltage. This in turn has a very strong impact on reducing the increase in the leakage current with increasing reverse bias voltage.

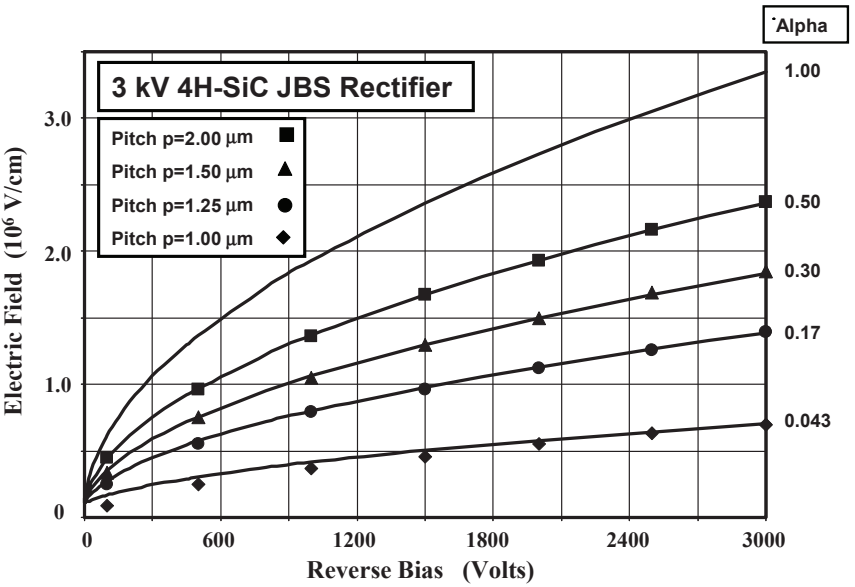

Fig. 3.20E Electric Field variation with Reverse Voltage in 4H-SiC JBS Rectifiers.

The increase in the electric field at the Schottky contact with increasing reverse bias voltage, obtained from the numerical simulations, is plotted in Fig. 3.20E for various cases of the cell pitch. These data points are compared with the calculated values obtained using the analytical model as shown by the solid lines. Here, the value for alpha was adjusted to obtain a good match to the simulation data for each cell pitch. The value for alpha is smaller for the silicon carbide JBS rectifier structure when compared with the silicon JBS rectifier structure with the same junction depth and spacing 'd'. This is due to the rectangular shape for the junction in the silicon carbide structure in comparison with a planar cylindrical shape for the junction in the silicon structure. The rectangular shape for the junction produces a stronger potential barrier under the Schottky contact which suppresses the electric field at the contact to a greater degree. This is accounted for in the analytical model by a smaller value for the alpha coefficient in Eq. [3.41].

For the silicon carbide structure, the electric field at the contact becomes close to the maximum value in the bulk when the pitch is over 2 microns. However, when the pitch is reduced to 1.25 microns, the electric field at the Schottky contact becomes less than half that for the normal Schottky rectifier structure. This reduced electric field at the contact is beneficial for suppressing the Schottky barrier lowering effect. The Schottky barrier lowering computed for the 4H-SiC JBS rectifiers by using the analytical model is compared with that in the normal Schottky rectifier structure in Fig. 3.21E. It can be observed that the Schottky barrier lowering for the JBS rectifier with a cell pitch of 1.25 microns is only 0.143 eV when compared with 0.223 eV for the normal Schottky rectifier.

The smaller electric field at the contact in the 4H-SiC JBS rectifier structures greatly reduces the leakage current because of not only suppressing the Schottky barrier lowering effect but also suppressing the tunneling current. This reduction of the leakage current is shown in Fig. 3.22E. With a cell pitch of 1.25

microns, the leakage current is reduced by a factor of 100,000 at reverse blocking voltages near the breakdown voltage. Since a pitch of 1.25 microns was demonstrated to produce excellent on-state characteristics (see Fig. 3.6E), this value is optimal for the 4H-SiC JBS rectifier with a blocking voltage of 3000 volts.

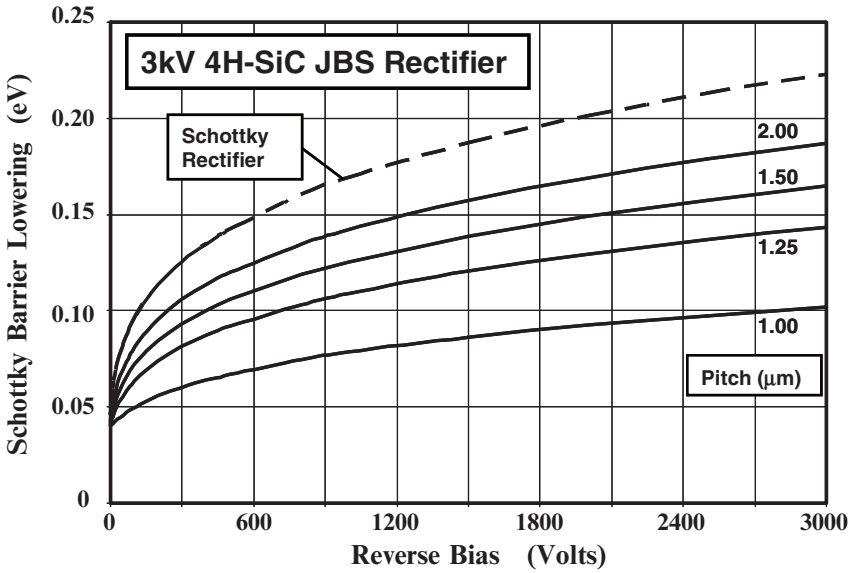

Fig. 3.21E Schottky Barrier Lowering in 4H-SiC JBS Rectifiers.

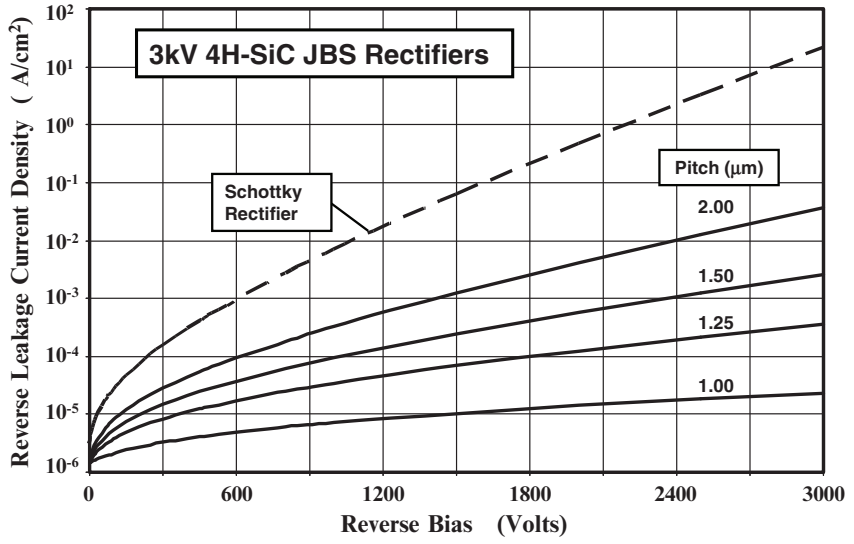

Fig. 3.22E Leakage Current Suppression in 4H-SiC JBS Rectifiers.

An even greater suppression of the electric field at the contact in the 4H-SiC JBS rectifier can be achieved by increasing the junction depth of the P^+ region. This can be accomplished by using boron ion implantation with various energies. As an example, the results of numerical simulations for the case of a junction depth of 0.9 microns are provided here. Unlike the case of silicon structures, the cell pitch does not have to be enlarged in the case of silicon carbide structure because of the lack of lateral diffusion during the annealing of the ion implanted layer. A three-dimensional view of the electric field distribution in a 3000 volt 4H-SiC JBS rectifier structure with cell pitch of 1.25 microns is shown in Fig. 3.23E at a reverse bias of 3000 volts (just prior to breakdown). It can be seen that the electric field is suppressed at the Schottky contact to a greater degree than for the junction depth of 0.5 microns. The maximum electric field at the Schottky contact has reduced from 1.4 x 10^6 V/cm (see Fig. 3.17E) to 0.6 x 10^6 V/cm.

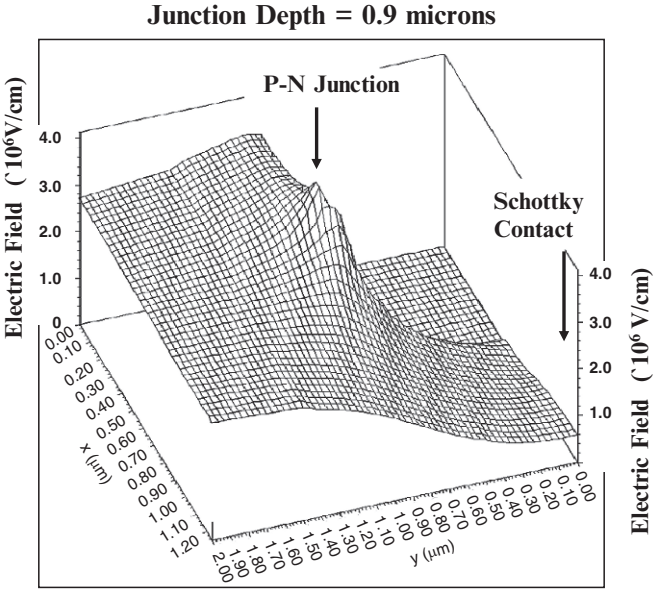

Fig. 3.23E Electric Field distribution in a 3 kV 4H-SiC JBS Rectifier.

The impact of the junction depth of the P^+ region on the degree of suppression of the electric field at the Schottky contact can be observed in Fig. 3.24E. In this figure, the cell pitch was maintained at 1.25 microns while the junction depth was increased from 0.1 to 0.9 microns. The data points provide the values extracted from the two dimensional numerical simulations. The solid lines provide the values obtained by using the analytical values with various values of alpha selected to match the data acquired from the numerical simulations. It can be observed from the figure that the value for alpha decreases with increasing junction depth because a stronger potential barrier is formed under the metal contact when the junction depth is made larger. Based up on these results, it can be concluded that a junction depth of 0.5 microns is adequate for suppressing the electric field under the Schottky contact for a JBS rectifier with a cell pitch of 1.25 microns.

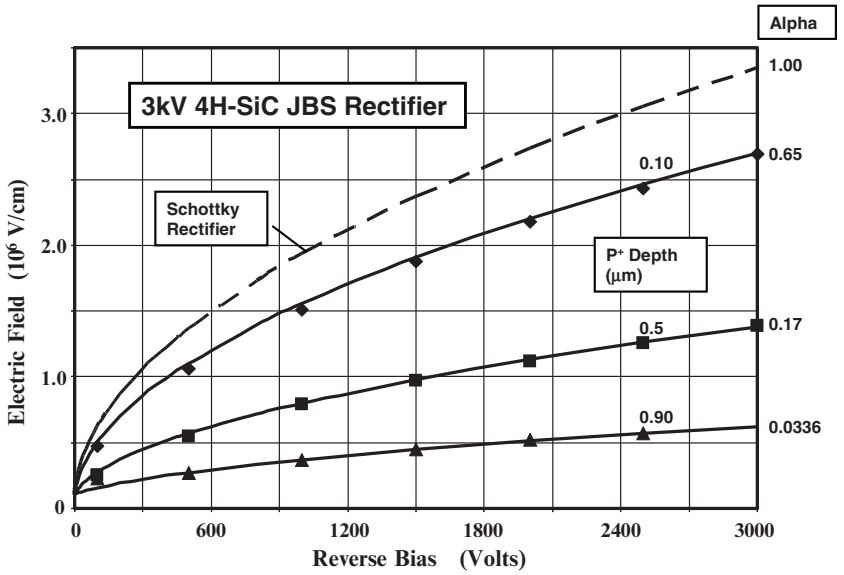

Fig. 3.24E Electric Field variation with Reverse Voltage in 4H-SiC JBS Rectifiers.

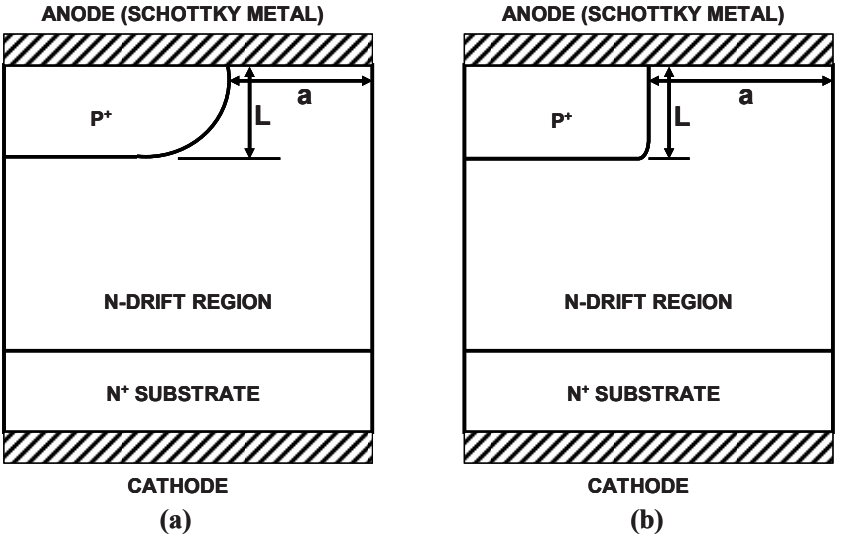

Fig. 3.25E Aspect Ratio Parameters for (a) the Silicon JBS Rectifier and (b) the Silicon Carbide JBS Rectifier.

The aspect ratio of the current conduction region located below the Schottky contact in the JBS rectifier has a strong influence on the suppression of the electric field at the contact, which is quantified by the coefficient alpha (α) in Eq. (3.37) and Eq. (3.41). The aspect ratio is defined as:

$$AR = \frac{L}{2a} \qquad \textbf{[3.42]}$$

where L is the length and 2a is the width of the channel in a JFET structure[8]. The equivalent dimensions are provided in Fig. 3.25E for (a) the silicon JBS rectifier structure and (b) the silicon carbide JBS rectifier structure. Based upon this diagram, the aspect ratio can be computed by dividing the junction depth (x_J) of the P^+ region to the space between the P-N junctions at the contact in the JBS rectifier. In the silicon JBS rectifier structure, the space between the junctions at the contact can be obtained by using $2(p - s - x_J)$ because the lateral diffusion of the P^+ region must be taken into account. In the case of the silicon carbide JBS rectifier structure, the space between the junctions at the contact can be obtained by using $2(p - s)$ because the lateral spread of the P^+ region is negligible.

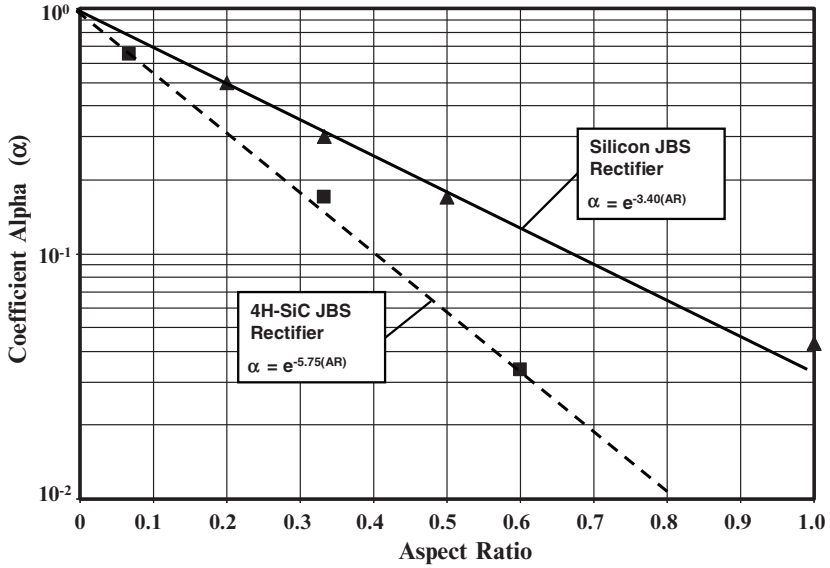

Fig. 3.26E Impact of Aspect Ratio on Alpha for JBS Rectifiers.

The variation of the coefficient alpha (α) with aspect ratio, obtained from the numerical simulations, is shown in Fig. 3.26E for silicon and silicon carbide JBS rectifiers. It can be observed that the coefficient alpha (α) varies exponentially with the aspect ratio. It is smaller for the case of silicon carbide devices when compared with silicon devices with the same aspect ratio because the electric field is not suppressed to the same degree in silicon devices due to the cylindrical shape of the P^+ region when compared with the rectangular shape for silicon carbide devices. The JBS structure is therefore particularly well suited for improving the performance of silicon carbide Schottky rectifiers.

3.4 Trade-Off Curve

In the textbook[1], it is demonstrated that the power dissipation can be minimized for a particular duty cycle and operating temperature by varying the Schottky barrier height during optimization of the Schottky rectifier structure. A smaller barrier height decreases the on-state voltage drop reducing conduction power losses while a large barrier height decreases the leakage current reducing reverse blocking power losses. Depending upon the duty cycle and the temperature, minimum power loss occurs at an optimum barrier height. A fundamental trade-off curve between on-state voltage drop and the leakage current was developed in the textbook based upon these considerations which does not depend upon the semiconductor material. However, the fundamental trade-off curve excludes the impact of the series resistance on the on-state voltage drop. More significantly, it excludes the strong influence of Schottky barrier lowering and pre-avalanche multiplication on the increase in leakage current for Schottky rectifiers.

When the voltage drop in the drift region is included for computing the on-state voltage drop of the silicon Schottky rectifier and the influence of Schottky barrier lowering and pre-breakdown multiplication are factored into the calculation of its leakage current, the trade-off curve degrades substantially as shown in Fig. 3.18 by dashed line corresponding to the triangular data points. In this figure, the trade-off curve for the silicon Schottky rectifier was generated by varying the Schottky barrier height. For an on-state voltage drop of 0.45 volts, the leakage current for the Schottky rectifier increases by two-orders of magnitude when compared with the fundamental trade-off curve.

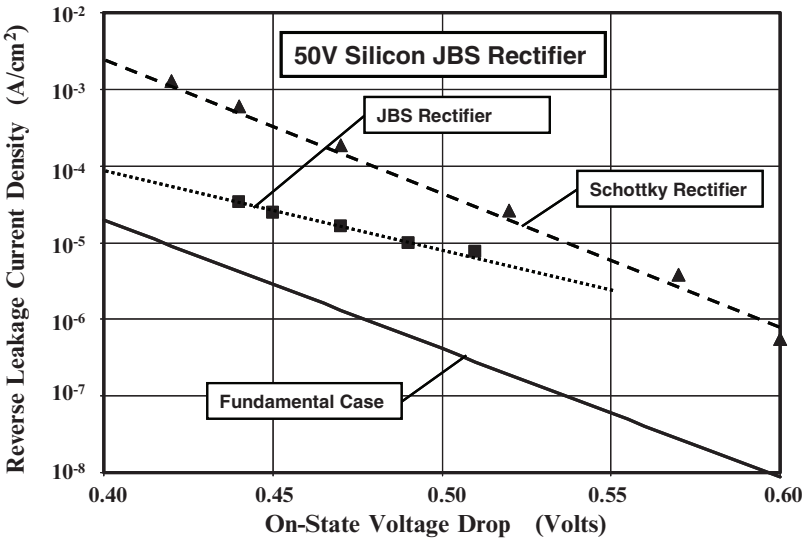

Fig. 3.18 Trade-Off Curve for the 50 V Silicon JBS Rectifier compared with that for a Schottky Rectifier.

In the silicon JBS rectifier, the Schottky barrier lowering effect is ameliorated by the reduced electric field at the contact. In addition, the pre-breakdown multiplication of the current flowing through the Schottky contact is suppressed by the much lower electric field at the vicinity of the Schottky contact. As pointed out earlier in the chapter, the breakdown shifts to the P-N junction in the JBS rectifier due to the larger electric field in this location. The trade-off curve for the JBS rectifier structure, computed by using the analytical models provided in the previous sections of this chapter in conjunction with the values for alpha extracted based upon the numerical simulations, is also shown in Fig. 3.18 by the dotted line corresponding to the square data points. For these silicon JBS rectifier structures, the pitch was varied while maintaining the same barrier height. For an on-state voltage drop of 0.45 volts, the leakage current for the JBS rectifier is reduced by an order of magnitude when compared with the Schottky rectifier. This implies that lower overall power dissipation can be achieved by using the JBS rectifier structure. In addition, it can be concluded that the JBS rectifier can be operated at a larger temperature before the on-set of thermal runaway.

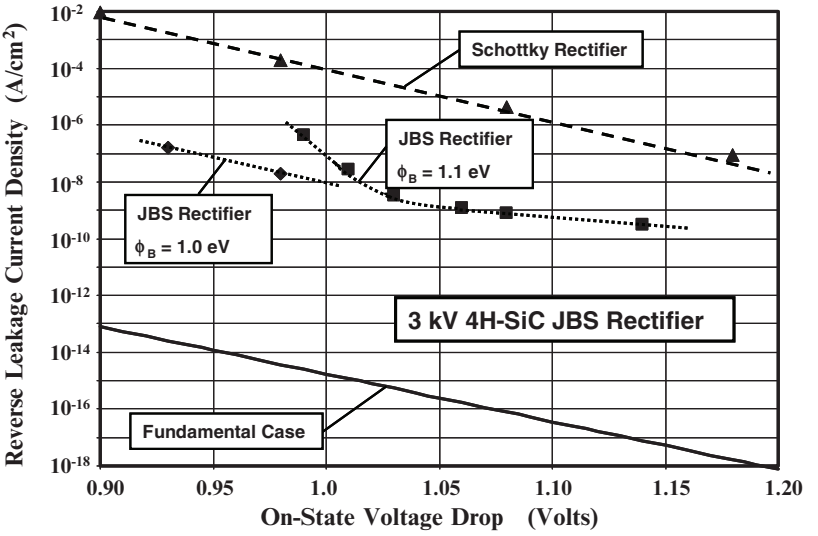

Fig. 3.19 Trade-Off Curve for the 3 kV 4H-SiC JBS Rectifier compared with that for a Schottky Rectifier.

A similar analysis can be performed for the silicon carbide JBS rectifier. In this case, a major improvement in reverse blocking characteristics occurs due to suppression of the Schottky barrier lowering and the thermionic field emission current due to the reduced electric field at the Schottky contact. When these phenomena are included in the analysis of the leakage current for the 4H-SiC Schottky rectifier, the trade-off curve for the case of devices designed to support 3000 volts obtained by varying the Schottky barrier height degrades significantly as shown in Fig. 3.19 by the dashed line corresponding to the triangular data

points. It can be observed that the leakage current increases by more than 10 orders of magnitude when compared with the fundamental curve.

For the silicon carbide JBS rectifier structure, the Schottky barrier lowering and thermionic field emission phenomena are suppressed producing greatly reduced leakage currents at large reverse bias voltages. The trade-off curves obtained for these structures by varying the cell pitch are also shown in the Fig. 3.19 by the dotted lines. It can be observed that the leakage current is four orders of magnitude smaller than for the Schottky rectifier for the same on-state voltage drop in the range of 1.0 to 1.1 volts. For a barrier height of 1.1 eV, the minimum on-state voltage drop that can be obtained for the JBS rectifier by increasing the cell pitch is about 0.97 volts. Consequently, its performance begins to approach that for the Schottky rectifier when the cell pitch is increased beyond 1.5 microns. However, if the Schottky barrier height is reduced to 1.0 eV while keeping a small cell pitch to suppress the leakage current, the trade-off curve for the JBS rectifier remains four orders of magnitude better than for the Schottky rectifier even for on-state voltage drops below 1 volt as shown in the figure.

3.5 Summary

In this chapter, it has been demonstrated that a significant improvement in the leakage current of Schottky rectifiers can be achieved by incorporation of a P-N junction to shield the Schottky contact against high electric fields generated in the semiconductor. In the case of silicon devices, the reduction of the electric field at the contact suppresses the Schottky barrier lowering and pre-breakdown multiplication phenomena. This reduces the leakage current by an order of magnitude while the increase in on-state voltage due to loss of Schottky contact area is small. In the case of silicon carbide devices, the reduction of the electric field at the Schottky contact suppresses the Schottky barrier lowering and the thermionic field emission current leading to a reduction of leakage current by four orders of magnitude. Consequently, this approach has become quite popular for the development of Schottky rectifiers from silicon carbide[9,10,11].

The use of a P-N junction to improve the performance of Schottky rectifiers has also been utilized for creating high performance anti-parallel diodes within silicon power MOSFET structures[12] that are used as synchronous rectifiers in switch mode power supply circuits. In this application, the power MOSFET is used in place of a diode in the buck converter circuit topology. During on-state current conduction, gate voltage is applied to the power MOSFET to turn-on the channel resulting in current flow with an on-state voltage drop that is smaller than that of Schottky rectifiers. However, to avoid a shoot-through problem during the switching transients, it is necessary to carry the load current for a short time through an alternate path. If this current flows through the body diode in the power MOSFET structure, circuit operation is disrupted by the slow reverse recovery time for this bipolar diode. It is therefore preferable to incorporate a Schottky

rectifier in parallel with the P-N body diode. The JBS structure has been found to be well suited for the integration of the Schottky rectifier with the power MOSFET because it enables the use of the contact metal for the source region of the MOSFET as the Schottky contact metal in the JBS diode. Although the barrier height for this contact is relatively small making the leakage current for the normal Schottky rectifier prohibitively large, the leakage current in the JBS structure is suppressed by using the shielding from the P-N junctions. The P-base region within the power MOSFET structure can be utilized for forming these P-N junctions with no additional processing steps.

References

[1] B.J. Baliga, "Fundamentals of Power Semiconductor Devices", Springer Scientific, New York, 2008.
[2] B.J. Baliga, "The Pinch Rectifier: A Low Forward Drop High Speed Power Diode", IEEE Electron Device Letters, Vol. 5, pp. 194-196, 1984.
[3] B.J. Baliga, "Pinch Rectifier", U. S. Patent 4,641,174, Issued February 3, 1987.
[4] M. Mehrotra and B.J. Baliga, "Very Low Forward Drop JBS Rectifiers Fabricated using Sub-micron Technology", IEEE Transactions on Electron Devices, Vol. 41, pp. 1655-1660, 1994.
[5] B.J. Baliga, "Silicon Carbide Power Devices", World Scientific Publishing Company, 2005.
[6] B.J. Baliga, "Analysis of Junction Barrier controlled Schottky Rectifier Characteristics", Solid State Electronics, Vol. 28, pp. 1089-1093, 1985.
[7] B.J. Baliga, "Modern Power Devices", Chapter 4, John Wiley and Sons, 1987.
[8] B.J. Baliga, "Modern Power Devices", Krieger Publishing Company, Malabar, FL, 1992.
[9] R. Held, N. Kaminski, and E. Niemann, "SiC Merged P-N/Schottky Rectifiers for High Voltage Applications", Silicon Carbide and Related materials – 1997, Material Science Forum, Vol. 264-268, pp. 1057-1060, 1998.
[10] F. Dahlquist, et al, "A 2.8 kV JBS Diode with Low Leakage", Silicon Carbide and Related materials – 1999, Material Science Forum, Vol. 338-342, pp. 1179-1182, 2000.
[11] J. Wu, "A 4308 V, 20.9 mO-cm^2 4H-SiC MPS Diodes based on a 30 micron Drift Layer", Silicon Carbide and Related materials – 2003, Material Science Forum, Vol. 457-460, pp. 1109-1112, 2004.
[12] B.J. Baliga and D. Alok, "Paradigm Shift in Planar Power MOSFET Technology", Power Electronics Technology Magazine, pp. 24-32, November 2003.