Architectures for High Dynamic Range, High Speed Image Sensor Readout Circuits

Sam Kavusi, Kunal Ghosh, and Abbas El Gamal

Department of Electrical Engineering, Stanford University, Stanford CA 94305, USA

Abstract. The stringent performance requirements of many infrared imaging applications warrant the development of precision high dynamic range, high speed focal plane arrays. In addition to achieving high dynamic range, the readout circuits for these image sensors must achieve high linearity and SNR at low power consumption. We first review four high dynamic range image sensor schemes that have been developed for visible range imaging and discuss why they cannot meet the stringent performance demands of infrared imaging. We then describe a new dynamic range extension scheme, Folded Multiple Capture, that can meet these performance requirements. Dynamic range is extended using synchronous self-reset while high SNR is maintained using few non-uniformly spaced captures and least-squares fit to estimate pixel photocurrent. We conclude with a description of a prototype of this architecture targeted for 3D-IC IR focal plane arrays.

1 Introduction

Precision high dynamic range (HDR), high speed imaging is finding growing applications in the automotive, surveillance, tactical, industrial, and medical and diagnostic instrumentation (e.g., fluorescence detection and spectroscopy) arenas. These applications can be broadly segmented into those operating in the visible range (typically $400\text{nm} < \lambda < 800\text{nm}$) and those operating in the infrared (IR) range (typically $4\mu\text{m} < \lambda < 12\mu\text{m}$). Precision HDR, high speed IR imaging applications, specifically, are fraught with challenges. In addition to the ability to capture scenes with large variations in irradiance due to object temperatures, the imaging system must be able to deal with undesirable scene disturbances, due to, for example, sun reflection or laser jamming. The imaging system must also have highly linear, shot noise limited readout in order to achieve the stringent sensitivity requirements. In [1], it is argued that low power IR focal plane arrays (FPAs) with $>$ 120dB dynamic range operating at 1000 frames/sec are needed for such applications. These performance requirements are far more aggressive than is achievable with present-day IR FPAs.

The advent of 3D-IC technology, which has increased the effective pixel area available, enables implementation of recently-developed HDR schemes with high pixel count. In this chapter, we discuss the main design and implementation challenges that limit the performance of these architectures. We find that these

Please use the following format when citing this chapter:

Kavusi, S., Ghosh, K. and El Gamal, A., 2007, in IFIP International Federation for Information Processing, Volume 249, VLSI-SoC: Research Trends in VLSI and Systems on Chip, eds. De Micheli, G., Mir, S., Reis, R., (Boston: Springer), pp. 1–23

architectures cannot achieve the high speed, HDR requirements without a significant penalty in pixel area and power consumption, and therefore do not lend themselves well to the aforementioned IR imaging applications. We then describe an HDR extension scheme, called Folded Multiple Capture (FMC) [7], that can achieve all the requirements stated in [1].

The rest of this chapter is organized as follows. In Section 2, we first briefly review the fundamentals of image sensors and introducing some needed terminology. In Sections 3-6, we discuss several of the recently-developed HDR schemes. In Section 7, we discuss the architecture and operation of FMC, implementation of a prototype, and experimental results obtained.

2 Background

An image sensor consists of an array of photodetectors followed by circuits for readout. Sensor performance is therefore a function of both the photodetector used and the readout circuits. Each photodetector in a conventional image sensor, e.g., CCD, CMOS APS, or IR FPA, converts incident photon flux into photocurrent i_{ph}. In visible range imaging, the incident photon flux corresponds to light reflected off of objects in the scene, while in IR imaging, the incident photon flux corresponds to object thermal radiation. A simplified Signal-to-Noise ratio (SNR) of the integrated photocurrent is given by

$$\mathrm{SNR}(i_{ph}) = \frac{(i_{ph}t_{\mathrm{int}})^2}{qi_{ph}t_{\mathrm{int}} + q^2\sigma^2_{\mathrm{Readout}}}, \quad \text{for } i_{ph} \leq \frac{qQ_{\max}}{t_{\mathrm{int}}},$$

where t_{int} is the integration time, q is the charge of an electron, $Q_{\max}$ is the saturation charge or well capacity, and $\sigma_{\mathrm{Readout}}$ is the readout noise. Note that this simplified SNR only considers integrated shot noise and readout noise and assumes that correlated-double-sampling (CDS) is performed, thus eliminating the reset noise and offset contributions. We also assume that gain FPN and dark current are either negligible or calibrated for, as is usually the case for state-of-the-art visible and IR sensors.

Image sensor dynamic range (DR) is defined as the ratio of the largest non-saturating photocurrent to the minimum detectable photocurrent, typically defined as the standard deviation of the noise under dark conditions. In visible range imaging, this corresponds to the range of intrascene illumination levels that can be imaged, while in IR imaging, this corresponds to the range of intrascene temperatures that can be imaged. Assuming the above sensor model, $i_{\max} = qQ_{\max}/t_{\mathrm{int}}$ and $i_{\min} = q\sigma_{\mathrm{Readout}}/t_{\mathrm{int}}$ and dynamic range is given by

$$\mathrm{DR} = \frac{i_{\max}}{i_{\min}} = \frac{Q_{\max}}{\sigma_{\mathrm{Readout}}}.$$

Since the dynamic range of image sensors is generally limited by the readout circuitry, HDR extension schemes modify a conventional sensor's readout circuits to improve its DR. Extending DR at the low end requires reducing $i_{\min}$, which

can be achieved by either reducing σ_{Readout} or increasing t_{int}. DR extension at the low end obtained by decreasing the diode or sense node capacitance to reduce σ_{Readout}, as is usually done in visible range image sensors, reduces $Q_{\max}$ which is not desirable for IR imaging. Extending dynamic range at the high end requires increasing $i_{\max}$, which can be achieved by adapting the integration times to photocurrent or increasing the effective well capacity.

In the following sections we review some of the recently developed HDR architectures.

3 Time-to-Saturation

The time-to-saturation scheme [9] attempts to achieve high dynamic range with high SNR by converting each photocurrent i_{ph} into its time-to-saturation $t_{\text{sat}}(i_{ph}) = qQ_{\max}/i_{ph}$. A block diagram of the scheme and plot of the integrator output as a function of time are given in Figure 1. After the photodiode and the time reference capacitor $C_{\text{T-Ref}}$ are reset, the output of the integrator is read out for CDS. Photocurrent is then integrated and converted to voltage, which is compared to a reference $V_{\max}$. Concurrently, $C_{\text{T-Ref}}$ follows the time-ramp. When the integrator output reaches $V_{\max}$, the comparator flips and $t_{\text{sat}}(i_{ph})$ is stored on $C_{\text{T-Ref}}$. At the end of integration, $v(t_{\text{int}})$ and t_{sat} are read out. If $t_{\text{sat}} < t_{\text{int}}$, the signal is estimated as $qQ_{\max}/t_{\text{sat}}$, otherwise the signal is estimated using $v(t_{\text{int}})$ only.

The filter is defined by

$$\hat{i_{ph}} = \frac{Cv(t)}{t_{\text{sat}}}.$$

Note that the minimum detectable signal is given by $i_{\min} = q\sigma_{\text{Readout}}/t_{\text{int}}$, which has the same form as that of the conventional sensor. The maximum nonsaturating signal depends on the comparator delay and offset as well as the noise associated with $t_{\text{sat}}(i_{ph})$ due to time-ramp noise, kTC of $C_{\text{T-Ref}}$, and the readout noise. Let σ_{sat} be the total rms of the noise added to $t_{\text{sat}}(i_{ph})$, then the maximum detectable signal is given by $i_{\max} = qQ_{\max}/\sigma_{\text{sat}}$. Therefore, the maximum achievable dynamic range for a given t_{int} is given by

$$\text{DR} = \frac{Q_{\max} t_{\text{int}}}{\sigma_{\text{Readout}} \sigma_{\text{sat}}}.$$

To calculate SNR, note that $qQ_{\max}$ corresponds to the expected value of the integrator charge at t_{sat}. Assuming CDS the integrator charge is given by

$$Q(t_{\text{sat}}) = \frac{1}{q}\left(i_{ph} t_{\text{sat}} + Q_{\text{Shot}} + Q_{\text{Readout}}\right).$$

Note that t_{sat} has an Inverse Gaussian distribution [8]. Linear approximation of $\hat{i}_{ph}$ can be used to calculate the error term caused by T_{Error}, readout noise of

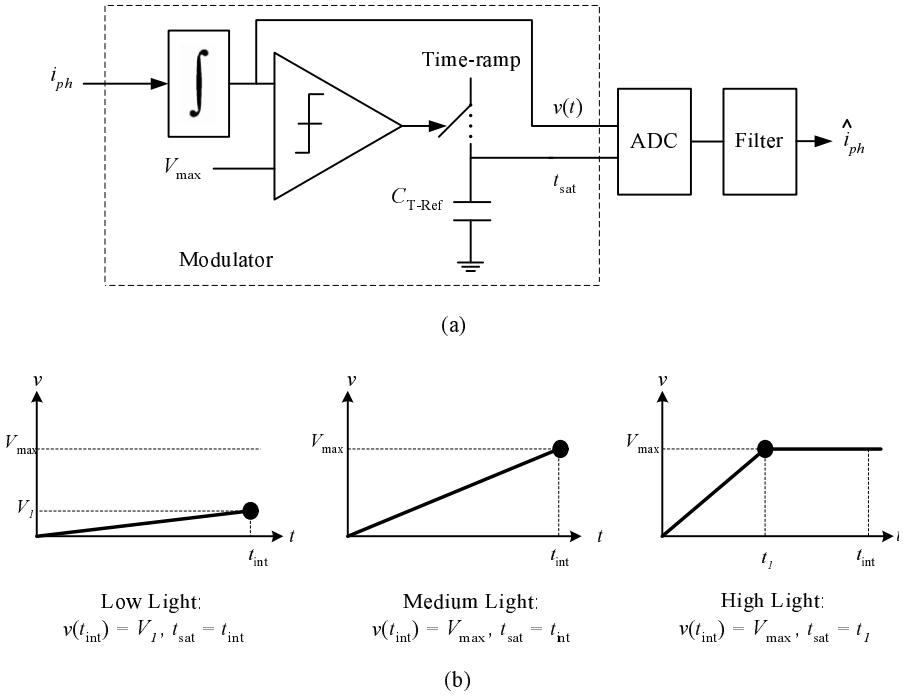

Fig. 1. Time-to-saturation block diagram.

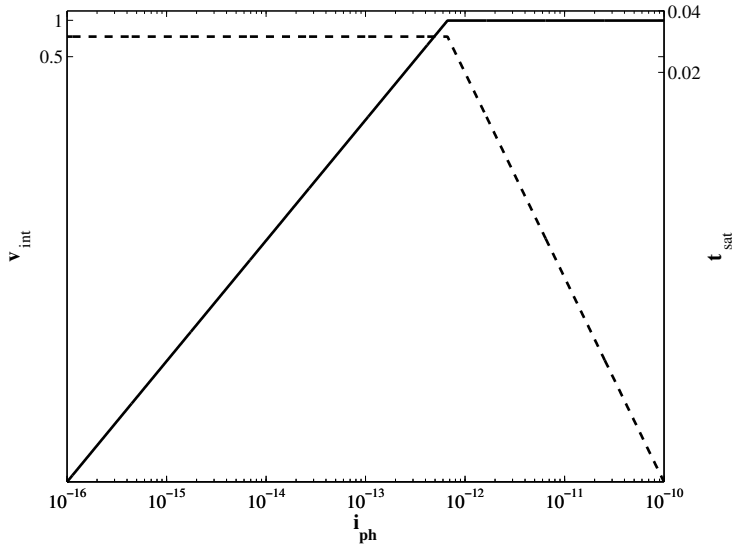

Fig. 2. Time-to-saturation signals.

time-to-saturation:

$$\begin{aligned}\hat{i}_{ph} &= \frac{qQ_{\max}}{t_{\text{sat}} + T_{\text{Error}}} \\ &= \frac{(i_{ph}t_{\text{sat}} + Q_{\text{Shot}} + Q_{\text{Readout}})}{t_{\text{sat}} + T_{\text{Error}}} \\ &\approx i_{ph} + \frac{Q_{\text{Shot}}}{t_{\text{sat}}} + \frac{Q_{\text{Readout}}}{t_{\text{sat}}} - i_{ph}\frac{T_{\text{Error}}}{t_{\text{sat}}}\end{aligned}$$

Therefore, the total output noise power is given by

$$\sigma_i^2 = \begin{cases} \frac{qi_{ph}}{t_{\text{int}}} + \frac{q^2\sigma^2_{\text{Readout}}}{t^2_{\text{int}}} & \text{if } i_{ph} \le \frac{qQ_{\max}}{t_{\text{int}}} \\ \frac{qi_{ph}}{t_{\text{sat}}(i_{ph})} + \frac{q^2\sigma^2_{\text{Readout}}}{t_{\text{sat}}(i_{ph})^2} + \frac{(qQ_{\max})^2\sigma^2_{\text{sat}}}{t_{\text{sat}}(i_{ph})^4} & \text{if } i_{ph} > \frac{qQ_{\max}}{t_{\text{int}}}, \end{cases}$$

and SNR is thus given by

$$\text{SNR}(i_{ph}) = \begin{cases} \frac{(i_{ph}t_{\text{int}})^2}{qi_{ph}t_{\text{int}} + q^2\sigma^2_{\text{Readout}}} & \text{if } i_{ph} \le \frac{qQ_{\max}}{t_{\text{int}}} \\ \frac{(qQ_{\max})^2}{q^2Q_{\max} + (i_{ph}\sigma_{\text{sat}})^2 + q^2\sigma^2_{\text{Readout}}} & \text{if } i_{ph} > \frac{qQ_{\max}}{t_{\text{int}}}. \end{cases}$$

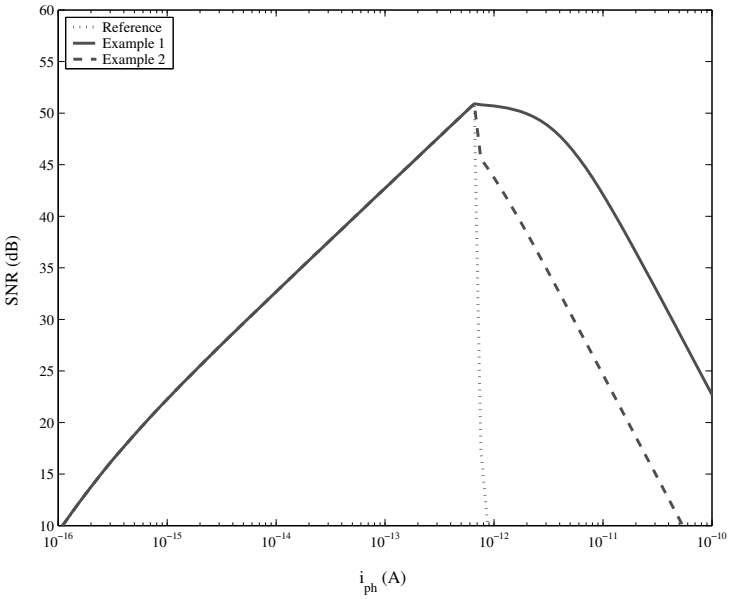

Fig. 3. SNR versus i_{ph} for time-to-saturation for two different examples.

Figure 3 plots SNR versus i_{ph} assuming $Q_{\rm sat} = 125,000e-$, $\sigma_{\rm Readout} = 5e-$, $t_{\rm int} = 30m$sec. Example 1 assumes $\sigma_{\rm sat} = 0.0005t_{\rm int}$ and achieves DR= 156dB. Example 2 assumes $\sigma_{\rm sat} = 0.004t_{\rm int}$ and achieves DR= 136dB.

Note that SNR is identical to that of the reference sensor within the reference DR. For larger i_{ph}, SNR drops monotonically as $1/i_{ph}^2$ (-20dB per decade) due to the effect of $\sigma_{\rm sat}$. Thus, DR is increased but at the expense of reduction in SNR. In Example 2 $\sigma_{\rm sat}$ is the dominant term degrading SNR at high end.

In the original implementation [10] only the time-to-saturation of the pixel is readout and therefore at low end cannot be differentiated producing $t_{\rm sat} = t_{\rm int}$(see Figure 2). By adding the residue readout in [9,11] the time-to-saturation is combined with a conventional readout and achieve very high dynamic range. The digital samples read out include the integrator voltage $v(t_{\rm int})$ and the time to saturation $t_{\rm sat}$ shown in Figure 2. Using this readout, the integrating capacitor dynamic range is multiplied by the dynamic range of $C_{\rm T-Ref}$ and thus a much wider dynamic range is achieved in a small area.

More details concerning implementation and correction for several nonidealities can be found in [9,11]. Note that the implementation in [9] actually uses two time-ramps and two capacitors to reduce $\sigma_{\rm sat}$. We accounted for this indirectly by using small $\sigma_{\rm sat}$ in the examples.

4 Multiple-Capture

The multiple-capture scheme [12, 13] increases dynamic range by sampling the signal nondestructively multiple times during integration. The HDR image can be constructed using the last-sample-before-saturation algorithm [12] as illustrated in Figure 4. Note that with this algorithm DR is only increased at the high end. DR at the low end can be increased by a combination of image blur prevention and weighted averaging [15], which requires significant on-chip memory and DSP capability.

To define DR and SNR, we assume uniform sampling time $t_{\rm capt}$ and that the filter only performs last-sample-before-saturation and digital CDS. The maximum nonsaturating signal is given by $i_{\rm max} = qQ_{\rm max}/t_{\rm capt}$ and the minimum detectable signal is given by $i_{\rm min} = q\sigma_{\rm Readout}/t_{\rm int}$. Thus

$$\mathrm{DR} = \frac{Q_{\rm max}t_{\rm int}}{\sigma_{\rm Readout}t_{\rm capt}}.$$

To define SNR note that it follows that of a conventional sensor for $t_{\rm sat}(i_{ph}) \geq t_{\rm int}$. In the extended range we use

$$\mathrm{SNR} \approx \phi(i_{ph})Q_{\rm max}$$

approximation, where ϕ is the normalized integrator output voltage. Note that $\phi(i_{ph}) = t_{\rm last-sample}(i_{ph})/(t_{\rm sat}(i_{ph}))$, where $t_{\rm sat}(i_{ph}) = qQ_{\rm max}/i_{ph}$.

Note that when $t_{\rm sat}(i_{ph}) < t_{\rm int}$

$$t_{\rm last-sample}(i_{ph}) = \left\lfloor \frac{t_{\rm sat}(i_{ph})}{t_{\rm capt}} \right\rfloor t_{\rm capt},$$

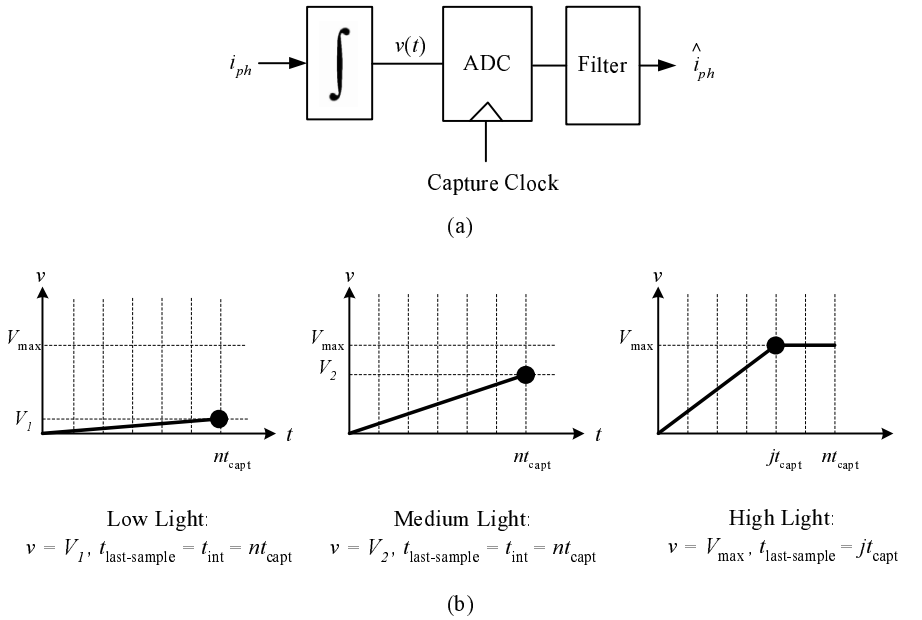

Fig. 4. Multiple-capture block diagram.

and therefore $(1 - t_{\text{capt}}/t_{\text{sat}}(i_{ph}))\, Q_{\max} < \text{SNR}(i_{ph}) < Q_{\max}$.

Figure 5 plots SNR versus i_{ph} assuming $Q_{\text{sat}} = 125,000e-$, $t_{\text{int}} = 30m$sec. Example 1 assumes 10 bit ADC, $\sigma_{\text{Readout}} = 35e-$, $t_{\text{capt}} = 150\mu$sec and achieves DR= 117dB. Example 2 assumes 9 bit ADC, $\sigma_{\text{Readout}} = 70e-$, $t_{\text{capt}} = 100\mu$sec and achieves DR= 114dB. The parameters t_{capt} and σ_{Readout} assume comparison time of 100ns and readout time per row per bit of 10nsec and 512×512 pixel array.

Note that unlike time-to-saturation, SNR does not degrade in the extended range, since $t_{\text{last}-\text{sample}}$ has the same accuracy as the multiple capture clock. However, DR suffers at the low end due to the large quantization noise of the per pixel ADC.

Moderate dynamic range increase has been also achieved using dual capture technique for CCD and CMOS APS sensors [18]. In dual capture, a scene is imaged only twice, once using a short integration time and another using a much longer integration time, and the two images are combined into a high dynamic range image. In [14] the authors cleverly take a second capture with a short integration time while the rest of the image is read out using dual outputs. There is a trade-off between the extension achieved by dual capture and the minimum SNR over the extended range. To find the SNR dip over its peak, minimum ϕ can be calculated. For example in [14] $\phi = 1/64$ and minimum SNR = 30dB with $Q_{\max} = 60,000e$.

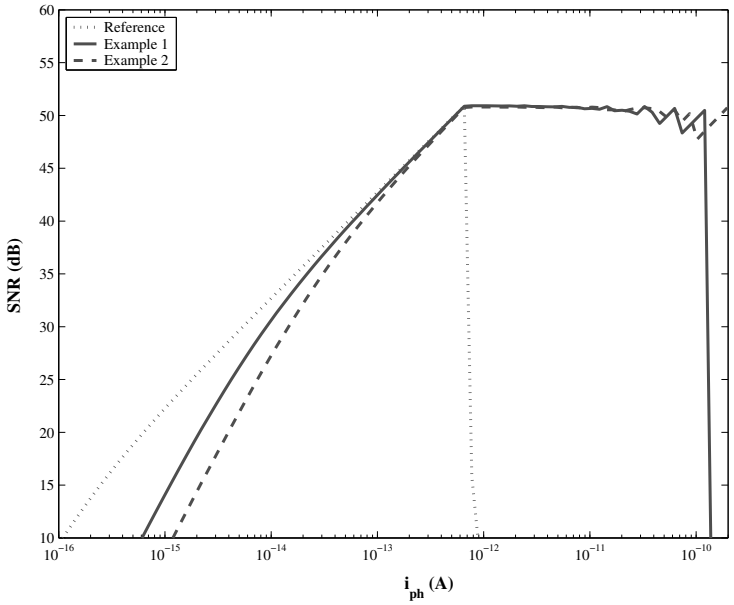

Fig. 5. SNR versus i_{ph} for multiple-capture for two different examples.

5 Extended Counting $\Sigma\Delta$

We first discuss the first order $\Sigma\Delta$ readout scheme and its variations. In Subsection 5.2, we analyze the extended counting scheme.

5.1 First Order Incremental $\Sigma\Delta$

The block diagram of the first order single-bit $\Sigma\Delta$ [19] is shown in Figure 6. At each clock cycle, the integrator output $v(t)$ is compared to the threshold value $V_{\max}/2$. If the comparator flips, $V_{\max}/2$ is subtracted off $v(t)$, thus preventing saturation of the integrator. The subtraction is typically implemented using a switched capacitor circuit. Note that the number of resets during the exposure time is proportional to the photocurrent value. A filter, which can be as simple as a counter, is used to estimate the photocurrent from the binary comparator output sequence. In *incremental* $\Sigma\Delta$ [17], the integrator is reset at the beginning of each frame. Such resetting improves SNR [19], because, unlike the free-running case, the integrator value at the beginning of each frame is known [5]. We, therefore, focus on incremental $\Sigma\Delta$.

To quantify the SNR and DR achieved by incremental $\Sigma\Delta$, we use the equivalent integrator output ramp shown in Figure 7. Note that the output sequence from the $\Sigma\Delta$ modulator is identical to the sequence generated by comparing the

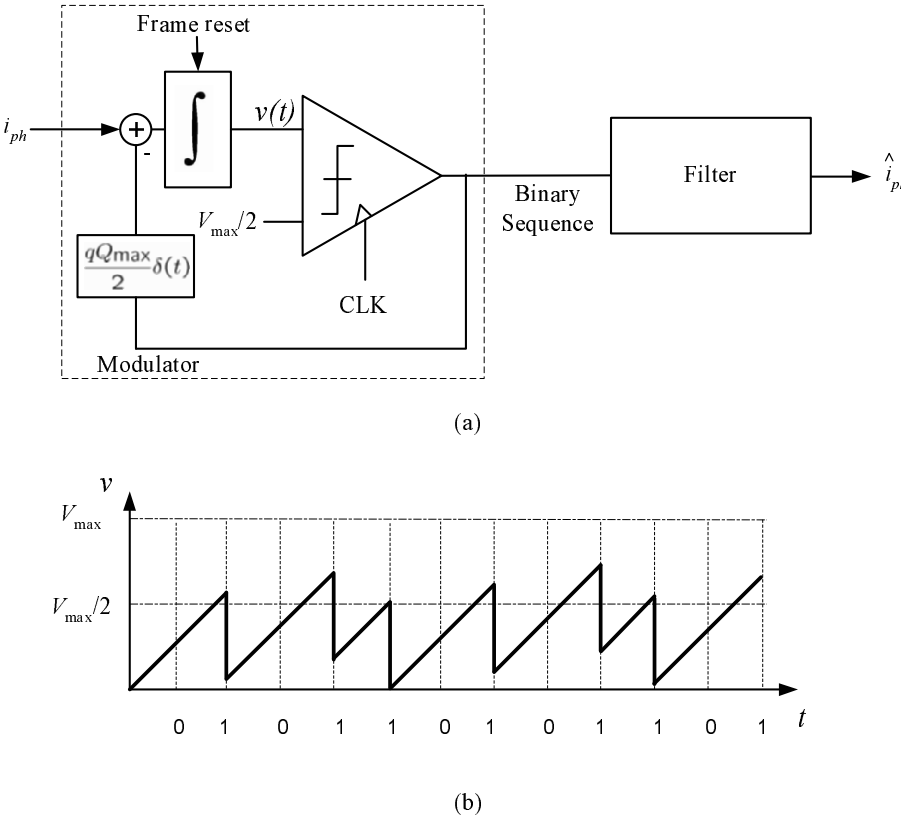

Fig. 6. Single-bit incremental $\Sigma\Delta$ block diagram.

equivalent ramp to the cumulative sum of the sequence, scaled by and biased by $V_{\max}/2$.

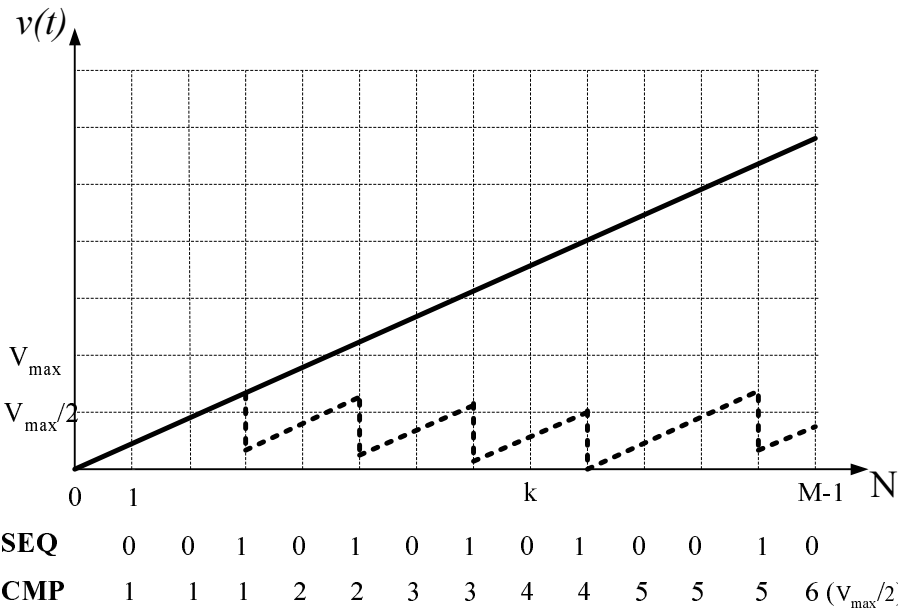

Fig. 7. Equivalence of $\Sigma\Delta$ output sequence (SEQ) to the sequence obtained by comparing the equivalent ramp (solid line) to the cumulative sum (CMP) of the sequence scaled and biased by $V_{\max}/2$.

Assuming that a counter is used for decimation, then at the end of integration time, the counter value is

$$n_{\text{counter}}(i_{ph}) = \lfloor 2 i_{ph} t_{\text{int}} / C V_{\max} \rfloor.$$

Now, assuming that the $V_{\max}/4$ bias in the counter readout is compensated for, and that quantization noise is signal independent and uncorrelated with other noise sources, the standard deviation of the effective readout noise is approximately given by

$$\sigma_{\text{Readout-eff}} = \sqrt{\frac{(CV_{\max})^2}{48q^2} + n_{\text{counter}}(i_{ph})\sigma^2_{\text{Switch}} + \sigma^2_{\text{Reset}}},$$

where, σ_{Switch} is the noise due to charge subtraction and σ_{Reset} is the reset noise. The first term in $\sigma_{\text{Readout-eff}}$ corresponds to quantization noise $\Delta^2/12$ with $\Delta = V_{\max}/2$. Therefore, the minimum detectable signal is given by

$$i_{\min} = q\sigma_{\text{Readout-eff}}/t_{\text{int}} \approx CV_{\max}/4\sqrt{3}t_{\text{int}}.$$

From Figure 7, the maximum non-saturating signal is given by

$$i_{\max} = CV_{\max}/2t_{\text{clk}}.$$

Therefore, the maximum achievable dynamic range for a given t_{int} is given by

$$\text{DR} = \frac{2\sqrt{3}t_{\text{int}}}{t_{\text{clk}}}.$$

In order to derive SNR, we need to consider the variation in charge subtraction, which translates into gain FPN. Denoting the standard deviation of charge subtraction by σ_{Offset}, we obtain

$$\text{SNR}(i_{ph}) = \frac{(i_{ph}t_{\text{int}})^2}{qi_{ph}t_{\text{int}} + (q\sigma_{\text{Readout-eff}})^2 + (n_{\text{counter}}q\sigma_{\text{Offset}})^2}.$$

Figure 8 plots SNR versus i_{ph} and compares it with SNR of the reference sensor. Both examples assume $Q_{\max} = 125,000e-$, $t_{\text{int}} = 30m\text{sec}$, $t_{\text{clk}} = 10\mu\text{sec}$, $\sigma_{\text{Switch}} = 57e-$ and achieve DR= 80dB. Example 1 assumes $\sigma_{\text{Offset}} = 0.0005Q_{\max}$. Example 2 assumes $\sigma_{\text{Offset}} = 0.01Q_{\max}$.

Note that with the same $Q_{\max}$ and t_{int} the DR of this scheme is shifted to the right with respect to the reference sensor DR, that is, this scheme has very poor low signal performance. Also note that SNR at the low end is quantization limited, whereas at the high end, it becomes gain FPN limited. The reason for the SNR degradation at the low end is the coarseness of the single-bit quantization and the filter used.

Reducing the size of the integrating capacitor or lowering $V_{\max}$ may improve low end performance. However, these solutions increase σ_{Offset}, which would degrade SNR at the high end. SNR at the low end can also be improved by using more sophisticated filters such as triangular, zoomer, recursive, etc. To demonstrate the extent of possible SNR improvement, in Figure 9 we compare the performance using a counter to that using the optimal filter [5]. Examples assume $Q_{\max} = 125,000e-$, $t_{\text{int}} = 30m\text{sec}$, $t_{\text{clk}} = 10\mu\text{sec}$, $\sigma_{\text{Switch}} = 57e-, \sigma_{\text{Offset}} = 0.0005Q_{\max}$ and achieve DR= 80dB. Note that substantial improvement in SNR is possible, but at the expense of higher digital circuit complexity and increased power consumption, required to achieve thermal noise level below quantization noise. As discussed, SNR at the high end is limited by the gain FPN due to variation in charge subtraction.

The extended counting scheme we discuss in the following section solves the coarse quantization problem of the single-bit $\Sigma\Delta$ schemes by quantizing the residue at the end of integration, $v(t_{\text{int}})$, using a multi-bit ADC.

5.2 Extended Counting

A block diagram of the extended counting scheme [16] is shown in Figure 10. Except for the additional residue ADC step, the architecture is identical to the single-bit $\Sigma\Delta$ architecture with a counter, discussed in the previous section.

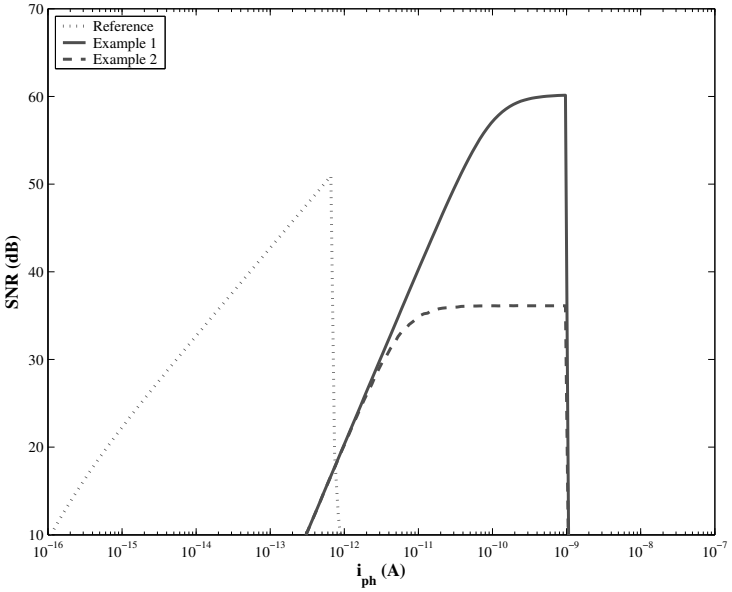

Fig. 8. SNR versus i_{ph} for single-bit incremental $\Sigma\Delta$ ADC for two different examples.

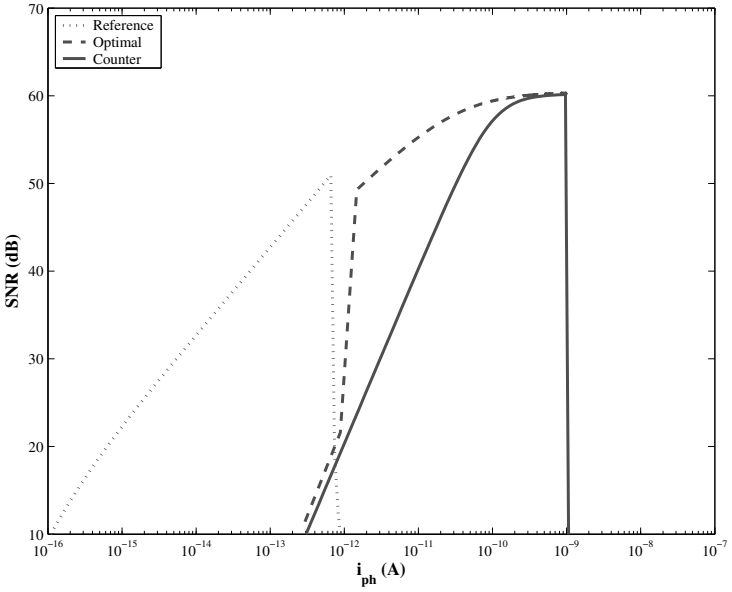

Fig. 9. SNR versus i_{ph} for single-bit $\Sigma\Delta$ with counter and optimal filter.

The counter value at the end of the integration time and the digitized residue are combined to estimate the photocurrent as

$$\hat{i}_{ph} = \frac{qQ_{\max}}{t_{\text{int}}} \left(\frac{1}{2} n_{\text{counter}} + \frac{v(t_{\text{int}})}{V_{\max}} \right).$$

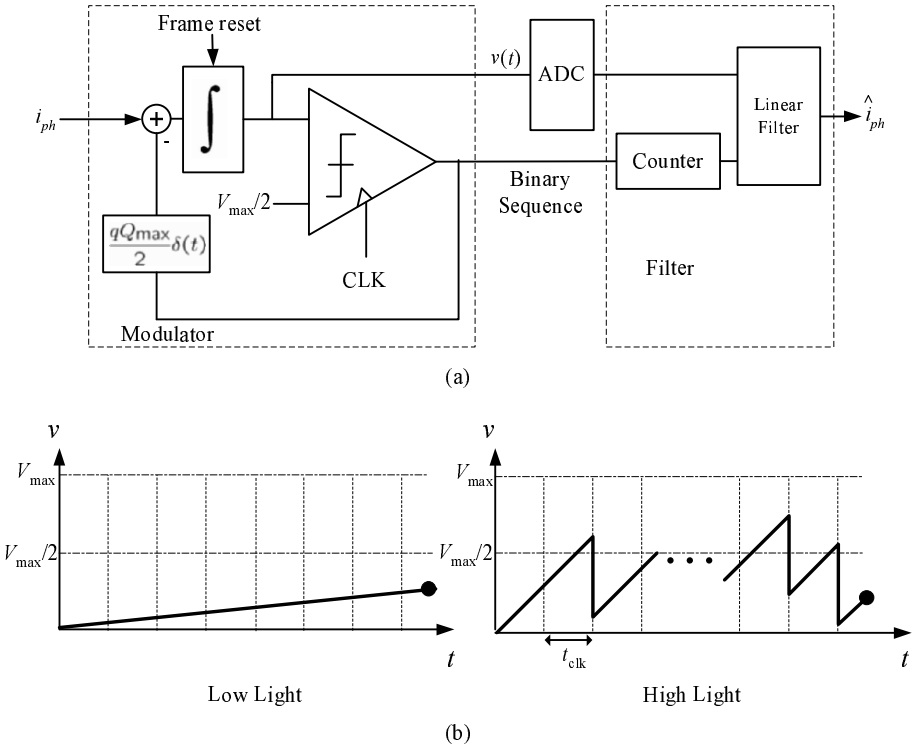

Fig. 10. Extended counting block diagram.

In order to calculate DR and SNR, we note that the standard deviation of the effective readout noise is given by

$$\sigma_{\text{Readout-eff}} = \sqrt{\sigma^2_{\text{ADC-Readout}} + n_{\text{counter}}(i_{ph})\sigma^2_{\text{Switch}} + \sigma^2_{\text{Reset}}},$$

where, $\sigma_{\text{ADC-Readout}}$ is the quantization noise, σ_{Switch} is the switched capacitor noise due to charge subtraction, σ_{Reset} is the reset noise and $n_{\text{counter}}(i_{ph})$ is the counter output at the end of t_{int}. Thus, the minimum detectable and maximum non-saturating signals are

$$i_{\min} = q\sigma_{\text{Readout-eff}}/t_{\text{int}} = q\sqrt{\sigma^2_{\text{ADC-Readout}} + \sigma^2_{\text{Reset}}}/t_{\text{int}}, \text{ and}$$

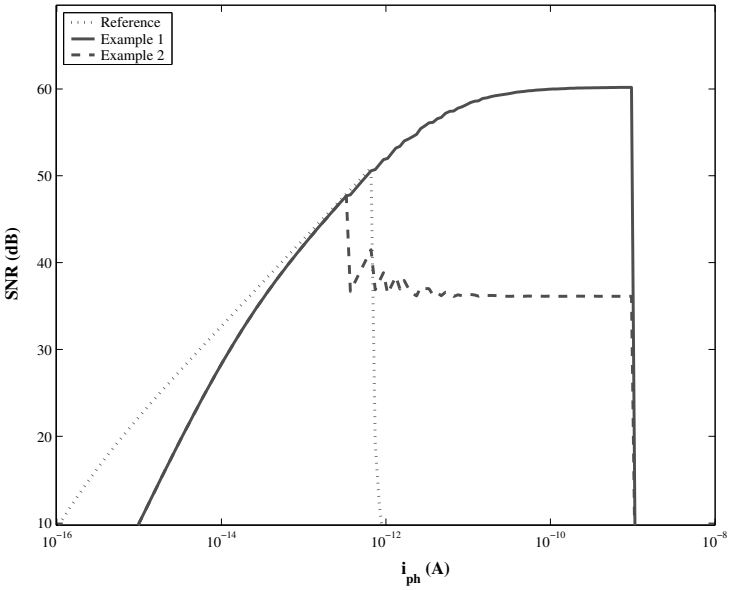

Fig. 11. SNR versus i_{ph} for extended-counting for two different examples.

$$i_{\max} = CV_{\max}/2t_{\text{clk}}.$$

Therefore, the maximum achievable dynamic range for a given t_{int} is given by

$$\text{DR} = \frac{Q_{\max}t_{\text{int}}}{2\sqrt{\sigma^2_{\text{ADC-Readout}} + \sigma^2_{\text{Reset}}}t_{\text{clk}}}.$$

In order to derive SNR, note that any variation of charge subtraction, σ_{Offset} will translate to gain fixed pattern noise. Thus SNR is given by

$$\text{SNR}(i_{ph}) = \frac{(i_{ph}t_{\text{int}})^2}{qi_{ph}t_{\text{int}} + (q\sigma_{\text{Readout}})^2 + (n_{\text{counter}}q\sigma_{\text{Offset}})^2}.$$

The SNR is plotted versus signal in Figure 11 assuming $\sigma_{\text{Switch}} = 57e-$, $\sigma_{\text{ADC-Readout}} = 9e-$ and achieving DR= 130dB. Example 1 assumes $\sigma_{\text{Offset}} = 0.0005Q_{\max}$. Example 2 assumes $\sigma_{\text{Offset}} = 0.01Q_{\max}$.

6 Synchronous Self-reset with Residue Readout

In this section we discuss the synchronous self-reset with residue readout scheme proposed in [21]. The scheme is described in Figure 12. The photocurrent is integrated and converted into voltage $v(t)$, which is periodically compared to a

reference voltage $V_{\max}$. If $v(t) \geq V_{\max}$, the comparator switches, the integrator is reset, and the counter is incremented. At the end of integration, the digitized value of $v(t_{\text{int}})$ and the reset count are combined to estimate the photocurrent. Let n_{Reset} be the number of resets, then

$$\hat{i}_{ph} = \frac{qQ_{\max}}{t_{\text{int}}} \left(n_{\text{Reset}} + \frac{v(t_{\text{int}})}{V_{\max}} \right).$$

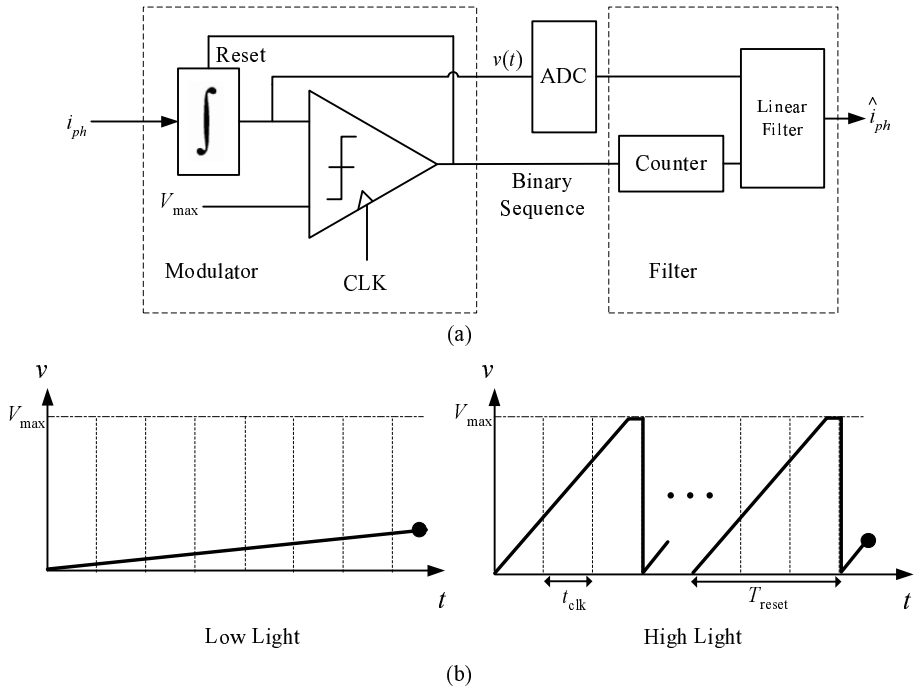

Fig. 12. Synchronous self-reset block diagram.

To compute DR and SNR, we first compute the distortion due to the underestimation of charge resulting from saturation before synchronous resetting takes place (see the waveform in Figure 8(b)). At the high end, assuming no noise $T_{\text{reset}} = \lceil qQ_{\max}/(i_{ph}t_{\text{clk}}) \rceil \, t_{\text{clk}}$, and the counter output is given by $n_{\text{Reset}} = \lfloor t_{\text{int}}/T_{\text{reset}} \rfloor$. Therefore, we can write

$$i_{ph} - \frac{i_{ph}t_{\text{clk}}}{t_{\text{int}}} \times \left\lfloor \frac{t_{\text{int}}}{\lceil qQ_{\max}/(i_{ph}t_{\text{clk}}) \rceil \, t_{\text{clk}}} \right\rfloor < \hat{i_{ph}} < i_{ph}.$$

The total average distortion power is therefore given by

$$\sigma^2_{\text{Distortion}} = \frac{1}{3}\left(\frac{i_{ph}t_{\text{clk}}}{t_{\text{int}}} \times \left\lfloor \frac{t_{\text{int}}}{\lceil qQ_{\max}/(i_{ph}t_{\text{clk}})\rceil\, t_{\text{clk}}} \right\rfloor\right)^2.$$

To find the total noise power we need to add contributions from shot noise, reset noise, residue readout noise, and gain FPN. To estimate the average noise power due to shot noise, we approximate the total integration time for shot noise by t_{int}. Gain FPN in the extended DR is due in part to the comparator and reset offsets that result in offset variation, σ_{Offset}, in $Q_{\max}$. Combining these noise terms with the distortion, we obtain the total noise power

$$\sigma_i^2 = \sigma^2_{\text{Distortion}} + \frac{qi_{ph}}{t_{\text{int}}} + (n_{\text{Reset}}+1)\left(\frac{q\sigma_{\text{Reset}}}{t_{\text{int}}}\right)^2 + \left(\frac{q\sigma_{\text{Readout}}}{t_{\text{int}}}\right)^2 + \\ + \left(\frac{q\sigma_{\text{Offset}}n_{\text{Reset}}}{t_{\text{int}}}\right)^2 + (\sigma_H i_{ph})^2.$$

Therefore SNR is given by

$$\text{SNR}(i_{ph}) = \frac{(i_{ph}t_{\text{int}})^2}{\sigma_i^2}.$$

To compute DR for the scheme, note that $i_{\min}$ is given by $i_{\min} = q\sqrt{\sigma^2_{\text{Readout}} + \sigma^2_{\text{Reset}}}/t_{\text{int}}$ and $i_{\max} = \sqrt{3}qQ_{\max}/t_{\text{clk}}$. Therefore,

$$\text{DR} = \frac{\sqrt{3}Q_{\max}t_{\text{int}}}{\sqrt{\sigma^2_{\text{Readout}} + \sigma^2_{\text{Reset}}}t_{\text{clk}}}.$$

Figure 13 plots SNR versus i_{ph} for two examples, assuming $Q_{\text{sat}} = 125,000e-$, $\sigma_{\text{Readout}} = 35e-$, $t_{\text{int}} = 30m\text{sec}$, $t_{\text{clk}} = 1\mu\text{sec}$, Example 1: $\sigma_{\text{Offset}} = 0.001Q_{\max}$, Example 2: $\sigma_{\text{Offset}} = 0.01Q_{\max}$, both achieve DR= 161dB. Note that SNR in the extended DR first increases as i_{ph} (10dB per decade) then drops as $1/i^2_{ph}$ (-20dB per decade). In particular note the sudden decrease in SNR for the example with high σ_{Offset}.

This technique suffers from poor quantization at the high end. Figure 14 shows the transfer function assuming no noise. Note that the plot is logarithmic in both axes and the quantization regions are growing. Constant SNR can be achieved if the number of quantization regions were the same in all decades; however, as shown in Figure 14 this number is decreasing with i_{ph}.

In the following section, we discuss the new Folded Multiple Capture HDR scheme [7], which by combining features of the synchronous self-reset and multiple capture schemes discussed above, can satisfy the precision imaging requirements in IR with low power consumption and robust circuits. We first discuss the architecture and operation of FMC. We then describe a prototype of the architecture and experimental results obtained.

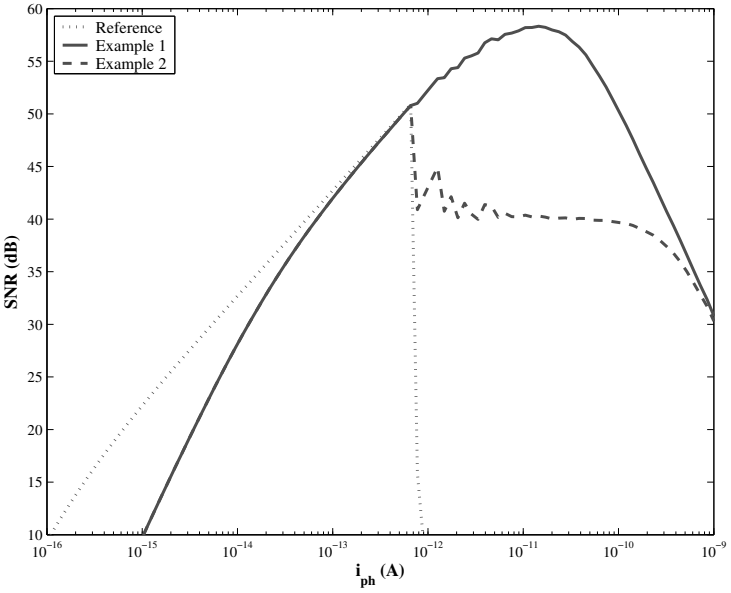

Fig. 13. SNR versus i_{ph} for synchronous self-reset for two different examples.

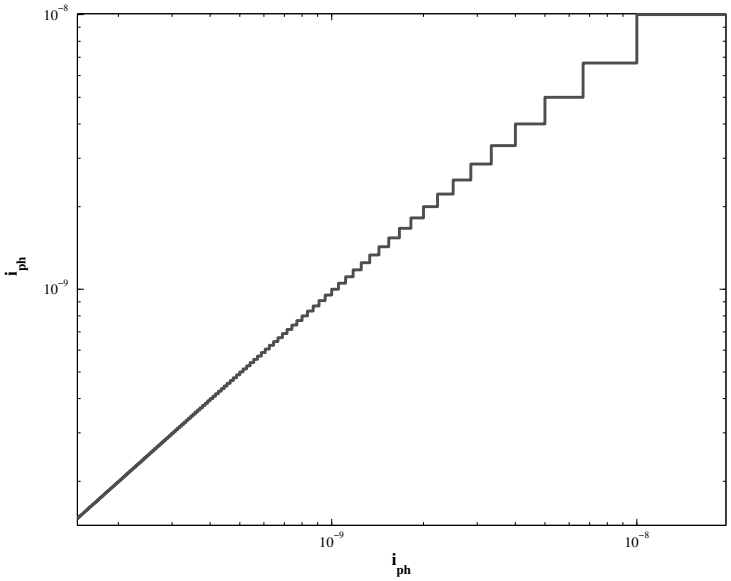

Fig. 14. Transfer Function of the synchronous self-reset scheme assuming no noise.

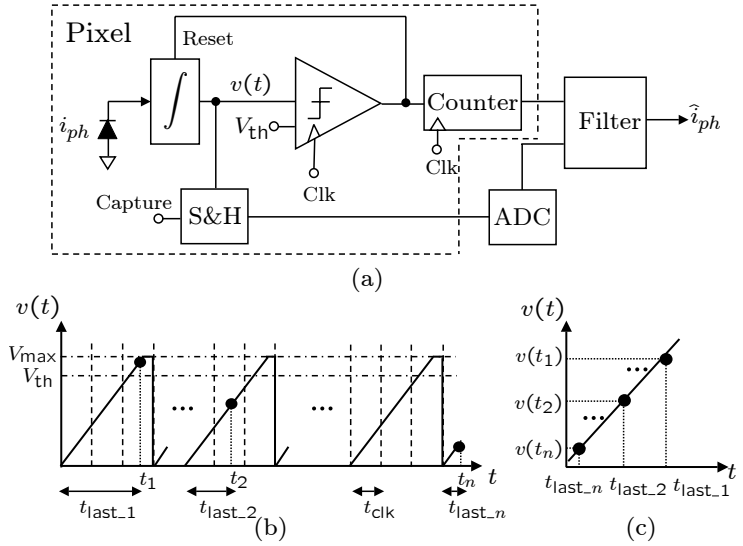

Fig. 15. Above: FMC architecture. Below: FMC operation.

7 Folded Multiple Capture

A block diagram of the FMC architecture is shown in Fig. 15(a). Each pixel consists of an integrator, with reset that is controlled by a comparator, a counter, and a sample-and-hold (S&H). The S&H output is digitized by a fine ADC, whose output along with the counter values are fed to a filter that generates the photocurrent estimate. At each clock cycle, the integrated photocurrent, $v(t)$, is compared to a threshold voltage V_{th}. The integrator is reset when the comparator output flips creating the folded waveform shown in Fig. 15(b). Meanwhile, the integrator output is sampled and digitized at predefined sampling or capture times $t_1, t_2, \ldots, t_n$. The capture times are synchronized with Clk, shifted by $t_{\text{Clk}}/2$ to avoid simultaneous reset and capture. The counter is incremented by the clock and reset by the comparator output signal. Its value, which corresponds to the *effective integration time* $t_{\text{last\_i}}$ (the time from the last reset), is read out at each capture time. The slope of the linear least-squares fit of the digitized capture values and their corresponding integration times is used to estimate the photocurrent (see Fig. 15(c)). In effect, FMC performs n regular captures during an exposure time and combines them to achieve a high fidelity estimate of the photocurrent. Dynamic range is extended by $2t_{\text{int}}/t_{\text{Clk}}$ over the integrating capacitor dynamic range. For example, for $t_{\text{int}}/t_{\text{Clk}} = 1000$, DR increases by 66dB. Fig. 16 shows example waveforms for $t_{\text{int}}/t_{\text{Clk}} = 8$ and four capture times. A low input photocurrent (see Fig. 16(a)) results in no reset and the scheme reduces to a conventional FPA with Fowler readout [20]. A high photocurrent (see Fig. 16(c, d)) results in periodic reset. Unlike other self-reset schemes discussed earlier, however, the number of resets is not used to estimate the signal.

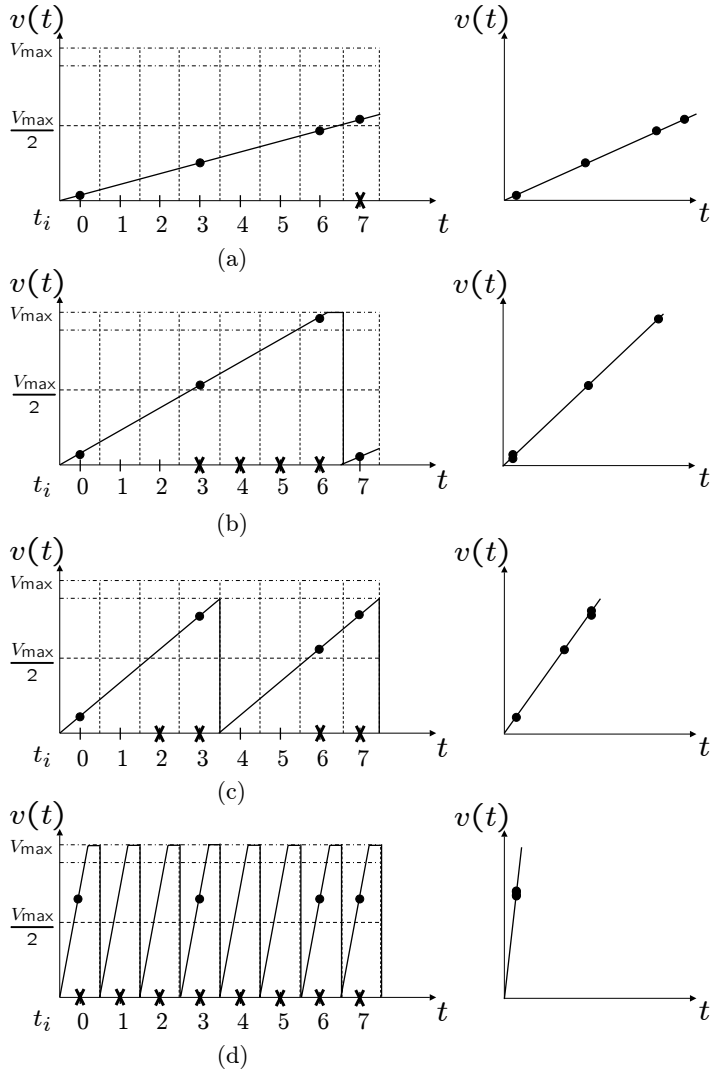

Fig. 16. Integrator output (left) and corresponding least-squares estimate (right) for four photocurrent values with capture times, $(t_1, t_2, t_3, t_4) = (0, 3, 6, 7)t_{\mathrm{Clk}}$. The $\times$ indicate capture times that satisfy $Q_{\mathrm{int}} > Q_{\mathrm{max}}/2$.

For low power, the number of captures used in achieving the high fidelity estimate of the photocurrent must be small. A surprising fact about FMC is that only 3 to 4 scene-independent globally set captures are needed to achieve uniformly high SNR. We wish to select capture times to guarantee a minimum SNR of $Q_{\max}/2$, for photocurrents $\geq qQ_{\max}/t_{\text{int}}$. Note that a single capture only guarantees this requirement for a certain range of photocurrents. To illustrate this point, consider the example in Fig. 16 again. A capture at $t_4 = 7t_{\text{Clk}}$ satisfies the above SNR condition for the examples in Fig. 16(a),(c),(d). However, using only this capture results in SNR ≈ 0 for example (b). The problem is solved by using another capture, e.g., between $3t_{\text{Clk}} \leq t_3 \leq 6t_{\text{Clk}}$. It can be shown that capture times $(t_2, t_3, t_4) = (3, 6, 7)t_{\text{Clk}}$ for $t_{\text{int}}/t_{\text{Clk}} = 8$ ensure that for all photocurrent values, at least one of the capture values has a value higher than $Q_{\max}/2$. To perform offset cancelation, a low value capture, e.g., at $t_1 = 0$, is also required.

While the above algorithm guarantees minimum SNR of $Q_{\max}/2$, least-squares fit of the captures and corresponding effective integration times to estimate photocurrent further improves SNR by canceling offsets, e.g., due to integrator and readout, and reducing the read, shot, and 1/f noise (see [20]). Note that since all signals in FMC are synchronized with a low jitter clock, SNR is not affected by timing inaccuracies. Further area and power reductions are achieved by relaxing the comparator specifications. As discussed earlier, the variation of the reset period with comparator offsets results in fixed pattern noise (FPN) that typically degrades SNR of HDR schemes. Since in FMC reset periods are not used to estimate photocurrent, the associated FPN is avoided and a simple regenerative architecture can be used for the comparator, obviating the need for a larger, power consuming gain stage. A relaxed comparator design also means that the highest clock frequency is not limited by the comparator speed, but by the settling time of the S&H circuit.

7.1 Implementation

A prototype of the FMC architecture has been implemented in a 0.18μm CMOS double-poly, five metal-layer process. The chip micrograph is shown in Fig. 17. Four columns have pixels with NWELL/PSUB diodes and the fifth has pixels driven by external current sources. Provisions have been made for bump-bonding IR detectors adjacent to the diodes. The analog and digital periphery circuits are placed at opposite ends of the pixel array. The Timing Control block generates all control signals. The clock rate (and thus dynamic range) and capture times are programmable via a scan chain. Each pixel occupies an area of 30μm $\times$ 150μm (40% analog, 60% digital). In a 3D-IC implementation of the fully integrated imaging system [1], each pixel is estimated to be 30μm $\times$ 30μm with 2 analog and 1 digital circuit layers.

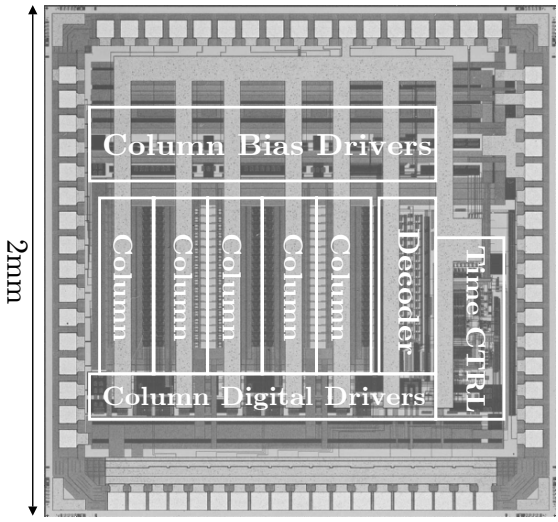

Fig. 17. FMC chip micrograph.

7.2 Experimental Results

A uniform LED illuminator is used as the light source for characterization. The chip analog column outputs, digitized using an on-board ADC, and the chip digital column outputs are transferred to a PC via an FPGA-based data acquisition board. Least-squares fit of the digitized capture values and corresponding effective integration times to estimate photocurrent is then performed in software.

The linearity and SNR are characterized locally at multiple random intervals. Experimental SNR versus i_{ph} results are shown in Figure 18. Read noise is expected to be lower with test setup improvements.

The power consumption per pixel is 25.5μW and dominated by the analog front-end. This corresponds to energy consumption of 25.5nJ for each pixel readout with DR = 138dB and SNR = 60dB. Note that this power consumption can be significantly reduced, e.g., using switched biasing, with knowledge of the detector parameters.

8 Conclusion

This chapter discusses the need for precision high dynamic range, high speed focal plane arrays for IR imaging applications. High dynamic range schemes targeted for visible range imaging are reviewed. A new HDR scheme, Folded Multiple Capture, that meets the stringent performance requirements of IR imaging applications is discussed. A prototype of the architecture targeted towards 3D-IC IR FPAs is described.

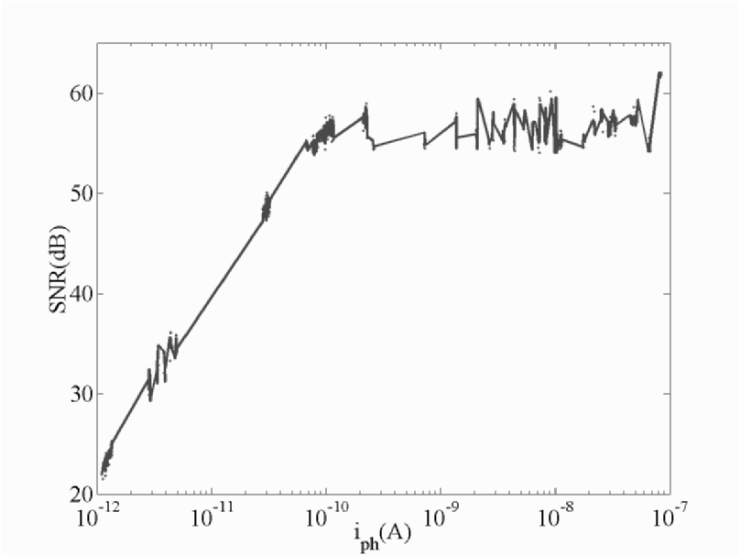

Fig. 18. Experimental scatter plot of SNR vs. i_{ph} for FMC.

References

1. R. Balcerak,"Vertically Integrated Sensor Arrays (VISA)," DARPA/MTO Photonics Symposium, Dec 2004.
2. S. Kavusi and A. El Gamal, "Quantitative Study of High-Dynamic-Range Image Sensor Architectures," Proceedings of the SPIE, vol. 5301, pp. 264-275, Jun 2004.
3. S. Kavusi, H. Kakavand, and A. El Gamal, "Quantitative Study of High Dynamic Range $\Sigma\Delta$-based Focal Plane Array architectures," Proceedings of the SPIE, vol. 5406, pp. 341-350, Aug 2004.
4. S. Kavusi, K. Ghosh, A. El Gamal, "Architectures for High Dynamic Range, High Speed Image Sensor Readout Circuits," *invited*, IFIP VLSI-SoC, pp. 36-41, Oct 2006.
5. S. Kavusi, H. Kakavand, A. El Gamal, "On Incremental Sigma-Delta Modulation with Optimal Filtering," IEEE Transactions on Circuits and Systems-I: Regular papers, vol. 53, no. 5, pp. 1004-1015, May 2006.
6. S. Kavusi and A. El Gamal, "Per-Pixel Analog Front End Architecture for High Dynamic Range Disturbance-Tolerant IR Imaging," Proceedings of the SPIE, vol. 5406, pp. 351-360, Aug 2004.
7. S. Kavusi, K. Ghosh, K. Fife and A. El Gamal, "A 0.18μm CMOS 1000 frames/sec, 138dB Dynamic Range Readout Circuit for 3D-IC IR Focal Plane Arrays, IEEE Custom Integrated Circuits Conference, pp. 229-232, Sep 2006.
8. V. Seshadri, *The Inverse Gaussian Distribution: A Case Study in Exponential Families*, Oxford University Press, 1994.
9. D. Stoppa et al., "Novel CMOS Image Sensor with a 132-dB Dynamic Range," IEEE Journal of Solid-State Circuits, vol. 37, no. 12, pp. 1846 -1852, Dec 2002.
10. V. Brajovic, T. Kanade, "A Sorting Image Sensor: an Example of Massively Parallel Intensity-to-time Processing for Low-latency Computational Sensor," Proceedings

of the 1996 IEEE International Conference on Robotics and Automation, vol.2, pp. 1638-1643, Apr 1996.
11. T. Lulé, B. Schneider, and M. Bohm, "Design and Fabrication of a High Dynamic Range Image Sensor in TFA Technology," IEEE Journal of Solid-State Circuits, vol. 34, no. 5, pp. 704-711, May 1999.
12. D. Yang, B. Fowler, A. El Gamal, and H. Tian, "Image Sensor with Ultrawide Dynamic Range Floating-Point Pixel-Level ADC," IEEE Journal of Solid-State Circuits, vol. 34, no. 12,pp. 1821-1834, Dec 1999.
13. W. Bidermann et al., "A 0.18μm High Dynamic Range NTSC/PAL Imaging System-on-Chip with Embedded DRAM Frame Buffer," IEEE International Solid-State Circuits Conference, pp. 212-213, Feb 2003.
14. O. Yadid-Pecht, E. R. Fossum, "Wide Intrascene Dynamic Range CMOS APS Using Dual Sampling," IEEE Transactions on Electron Devices, vol. 44, no. 10, pp. 721 - 1723, Oct 1997.
15. X. Q. Liu, A. El Gamal, "Synthesis of High Dynamic Range Motion Blur Free Image From Multiple Captures," IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 50, no. 4, pp. 530-539, Apr 2003.
16. C. Jansson, "A High-Resolution, Compact, and Low-Power ADC Suitable for Array Implementation in Standard CMOS," IEEE Transactions on Circuits and Systems-I, vol. 42, no. 11, pp. 904-912, Nov 1995.
17. J. Markus, J. Silva and G.C. Temes, "Theory and applications of incremental $\Delta\Sigma$ converters,"IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, volume 51, number 4, pp. 678-690, April 2004.
18. O. Yadid-Pecht "Wide Dynamic Range Sensors," Optical Engineering, vol. 38, no. 10, pp. 1650-1660, Oct 1999.
19. B. Fowler, A. El Gamal, and D. Yang, "A CMOS Area Image Sensor with Pixel-Level A/D Conversion," IEEE International Solid-State Circuits Conference, pp. 226-227, Feb 1994.
20. A. M. Fowler and I. Gatley, "Noise Reduction Strategy for Hybrid IR Focal Plane Arrays," Proceedings of the SPIE, vol. 1541, pp. 127-133, Jul 1991.
21. A. Bermak, A. Bouzerdoum, and K. Eshraghian, "A Vision Sensor with On-Pixel ADC and Built-in Light Adaptation Mechanism," Microelectronics Journal, vol. 33, no. 12, pp 1091-1096, 2002.